DATASPEED TAPE TO TAPE SYSTEM
TYPE 1 AND TYPE 2 TAPE SENDERS AND RECEIVERS
ELECTRONIC CIRCUITRY
SCHEMATIC DIAGRAMS AND
CIRCUIT BOARD DRAWINGS

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1. INTRODUCTION
1.01 This section provides the schematic diagrams and circuit board drawings for the 1A and 2A Tape Senders and 1B and 2B Tape Receivers used in the DATASPEED Tape to Tape System. The actual wiring diagrams for the Sender and Receiver are provided in a separate section.

1.02 This section is reissued to rearrange text and to include the latest diagram drawing issues.

2. GENERAL

2.01 The schematic diagrams make use of circuit logic symbols to represent a group of electrical components arranged on a printed circuit board so as to perform a specific function or functions. Each logic symbol is designated by two numbers: a "Z" number, and an "EC" number. The "Z" number denotes the physical location of the circuit board in the electronic module assembly represented by the schematic diagram. The "EC" number refers to the specific type of circuit board used in that location; one type of circuit board may be used in more than one location.

2.02 Each circuit board drawing carries two numbers: a six digit number, and an "EC" number. The six digit number is considered as the part number of the circuit board, and should be used (prefixed with TP) when ordering replacement circuit boards. The last three digits of the part number are the same as the three digits of the "EC" number; for example, part number TP172322 is circuit board EC322. The circuit board drawing consists of a parts list, a parts layout of the circuit board, a schematic diagram of the circuit, a circuit description and a drawing of the circuit logic symbol.

2.03 The index (Part 3.) lists the subject matter of each diagram and drawing included in the section. In addition, it also lists the numbers of the WD and EC drawings. Finally, to determine which have been changed from the previous section issue, a cross-reference between section issue and diagram or drawing issue is provided.
### SECTION 592-800-400

#### 3. DIAGRAM INDEX

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<td>- - B</td>
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<td>Sending Distributor</td>
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<tr>
<td>Flip-Flop</td>
<td>172359</td>
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<td>Integrator</td>
<td>172361</td>
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<td>Magnet Pulser</td>
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<td>Squaring Amplifier</td>
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<td>Pick-Up Amplifier</td>
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<td>Variable One-Shot (0.9 to 1.5 Milliseconds)</td>
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<tr>
<td>Time Delay Relay Driver</td>
<td>177543</td>
<td>- - 3</td>
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</table>

*Original Issue

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Attached:
- Teletype Corporation
- Wiring Diagrams (WD)
- Circuit Board Drawings (EC)

Page 2
2 Pages and Attachments
This relay consists of two power amplifiers which can be used as relay drivers. The smaller will operate both transistors (2N398) with 35 watts at 12 volts. The larger will operate the 2N398 and 2N398B with 100 watts at 12 volts, which turns "OFF" and appropriate for higher currents. The operation of the motor would be applied to the base of 2N398, which would turn off the relay for operation.

Design which require controlling voltages and currents greater than 35 watts and 100 watts should not be used with these elements.
This card consists of one Relay Driver and one receiving Input Amplifier. The Relay Driver consists of an input signal, an input bias with a resistive input, and the correct amplifier voltage. The amplification occurs at the point where the Input Amplifier output is applied. The Input Amplifier is biased off with no input signal. When input voltage is applied on input (E), it is biased "OFF" and all voltage appears on the base of Q2. In this position, Q2 is biased "OFF" driving Q1 off and thereby turning it "ON", thereby energizing the relay. With Gnd applied at input (F), Q2 is biased "ON" driving Q1 to "OFF" and thereby turning it "OFF", thereby de-energizing the relay. The receiving Input Amplifier is used to convert an 8 volt input into a 0 or 5 volt output. With 8 volts at input (N), Q1 is biased "OFF" driving Q2 to "OFF" and thereby turning it "OFF", thereby de-energizing the relay. With ground applied at input (N), Q1 is biased "ON" driving Q2 to "OFF" and thereby turning it "OFF", thereby de-energizing the relay.
This card consists of a Relay Driver circuit and the receiving input amplifier. The Relay Driver consists of an NPN Darlington transistor (Q1) and an n-channel JFET. The input to the circuit is an open collector gate (N) which is biased "ON" to a low level of +5 volts with respect to ground. When a +5 volt signal is applied to this input, Q1 is turned "OFF" and the collector of Q1 becomes a low level signal which in turn is applied to the base of the JFET. The JFET is turned "ON" and a +5 volt signal is applied to the output (L). The input amplifier is used to convert a +5 volt signal into a zero, -5 volt output. With a +5 volt input (N), Q3 is biased "OFF" making output (L) a zero level signal. With a -5 volt input (N), Q3 is biased "ON" placing output (L) at approximately +5 volts or ground.
THE PURPOSE OF THIS CIRCUIT IS TO...

THE INPUT SIGNAL TO THE NORMAL OUTPUT SIGNAL...
Symmetrical Emitter Follower.

This circuit is used to provide current gain with no inversion or change in signal level. With zero volts applied at base of NPN and PNP transistors, zero voltage appears on output. With 6 volts applied at input, 6 volts appears at output. The symmetrical emitter follower provides low output impedance on both positive and negative going voltage transitions.

Input

Output

Note: Refer to symbols for markings information.

Part No.

Symbol

Circuit Board EC 323

Symmetrical Emitter Follower

Circuit Board EC 323

This circuit is used to provide current gain with no inversion or change in signal level. With zero volts applied at base of NPN and PNP transistors, zero voltage appears on output. With 6 volts applied at input, 6 volts appears at output. The symmetrical emitter follower provides low output impedance on both positive and negative going voltage transitions.

Note: Refer to symbols for markings information.
**NOTE TO TECHNICIAN:**

Refer to 5016WO for marking information.

**NAME AND DESCRIPTION:**

<table>
<thead>
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<th>NAME AND DESCRIPTION</th>
<th>LOCATION</th>
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<td>C1</td>
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<td>TP2</td>
<td>F-22</td>
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<tr>
<td>TP3</td>
<td>1200 OHMS COLLECTOR LOAD</td>
<td>COLLECTOR LOAD</td>
<td></td>
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<tr>
<td>TP4</td>
<td>1200 OHMS COLLECTOR LOAD</td>
<td>COLLECTOR LOAD</td>
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</table>

**CIRCUIT BOARD EC324**

**INVERTER AND PULSE AMPLIFIER**

**NOTE:**

card connections are represented by letters.

test points are represented by numbers.
OUTPUT AMPLIFIER AND VOLTAGE BIAS

This card basically consists of two common-emitter amplifiers and a voltage bias network.

The output of Q1 is connected to the grid of Q3 by means of a strap in the connector between points E and H.

Q1 and Q2 have base-emitter voltages of 0.7 volts. The base current of Q1 is approximately 0.01 mA. The collector current of Q1 in this case is determined by the value of R6. The bias current of Q2 is determined by the value of R3, which is in series with R1 and R2.

The output of the circuit at point P is approximately 6 volts. With 12 volts applied at point F, Q1 conducts, which in turn drives Q2 into conduction. The output at point P therefore becomes -6 volts. -12V +6V...

NOTE

Card connections are represented by letters.

Test points are represented by numbers.
The circuit is a general purpose emitter follower used to provide current gain with inversion or change in the signal level. With zero voltage applied at the base, zero voltage applied at the collector. The output signal is fed from the collector.

The PNP emitter follower is used to provide line output terminals (low-current gain) in the positive going voltage transition (4 to 0 V).
This card consists of two common emitter amplifier circuits used to produce narrow pulses having a rapid rise time. A +1.5 V at the base applied through R4 raises the emitter of Q2. With a negative going 6 V transition applied to the base, the collector potential will be at 0 V for the duration of the pulse applied at the base. The theory of operation for Q2 is identical to Q1.

**EC 347**

**PULSE AMPLIFIER (2)**

**CIRCUIT BOARD EC 347**

**NOTE:** Connections are represented by letters. Test points are represented by numbers.
The purpose of this circuit is to generate a signal of variable width as determined by the input signal applied to point A.

A signal applied to point A will turn the transistor off and remain off until C) can discharge to approximately 0 volts, returning to +1.5 volts at +1.5 volts and keeping base potential at approximately +1 volt.

Part of discharge path through C and R will charge the coupling resistor C to approximately 6 volts positive pulse applied to Terminal C will trigger circuit, however, if Terminal E is at 0 volts a positive pulse will be produced to trigger a signal of variable width as determined by the input signal applied to point A.
Note: Directly designated on Capitol ba.
In a sense, a "sub-plug" without a fixture required.

One pole is used in this circuit, where 2 or more voltage levels, low, 0.8, 0.3, etc.,
are used, each with a single pole of the 2 poles.

The circuit is used to open the voltage 0.3, etc., and
floating positive 0.3 is applied by an external source.

The circuit is used to apply most circuits, for instance, probe circuits between
input circuits.

NOTE: CONNECTING ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS
The circuit shown is a flip-flop circuit. It consists of two transistors, one of which is conducting when the other is cutoff. The circuit is designed to switch between two states. When the base of one transistor is driven high, the other transistor is driven to a cutoff state, and vice versa. This switching action is controlled by the input pulses applied to the circuit. The circuit is typically used in digital electronics to store or switch digital information.
**INTEGRATOR**

THE CARD CONSISTS OF THE ORIGINAL INTEGRATOR CIRCUITS.

THE INPUT SIGNAL IS APPLIED THROUGH 100 OHM DROPPING RESISTORS AT TERMINALS A, B, C, D, AND E. THE LEADING EDGE AND TRAILING EDGE OF THE INPUT SIGNAL WILL BE DELAYED DUE TO RELATIVELY LONG TIME CONSTANT OF THE CAPACITOR AND 1800 OHM RESISTOR. THE CIRCUIT IS DESIGNED FOR INPUT SIGNALS FROM MECHANICALLY OPERATED CONTACTS. THE PURPOSE OF THE CIRCUIT IS TO PREVENT NOISE FROM CONTACT BOUNCE TO GET INTO SUCCEEDING STAGE.

**CARD CONNECTIONS**

Test points are represented by numbers.

- **A**
- **B**
- **C**
- **D**
- **E**
- **F**
- **G**
- **H**
- **I**
- **J**
- **K**
- **L**
- **M**
- **N**
- **O**
- **P**
- **Q**
- **R**
- **S**
- **T**
- **U**
- **V**
- **W**
- **X**
- **Y**
- **Z**

**TEST POINTS**

- **A**
- **B**
- **C**
- **D**
- **E**
- **F**
- **G**
- **H**
- **I**
- **J**
- **K**
- **L**
- **M**
- **N**
- **O**
- **P**
- **Q**
- **R**
- **S**
- **T**
- **U**
- **V**
- **W**
- **X**
- **Y**
- **Z**

**NOTE**

Test points are represented by numbers.
**CIRCUIT BOARD EC 363**

**FILTER (2)**

This card consists of two 45 filters. Various voltage inputs to each module are applied through this filter.

The function of this filter is to reject high frequency noise inputs. Inputs are applied at points B and P. Outputs at C and R.

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### Symbols

**A**
- Bottom View
- Bottom View of Transistor

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### Card Connections

- **B**: Bottom View
- **C**: Bottom View of Transistor

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### Component Information

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<th>Function</th>
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<td>...</td>
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<td>L1, L2</td>
<td>Filter Inductors</td>
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<td>R1, R2, R3, R4</td>
<td>Resistors</td>
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### Notes

- Card connections are represented by letters.
- Test points are represented by numbers.
The diagram represents a circuit board with labeled components and connections. The symbols used are consistent with standard electrical schematic notation. The circuit includes a collector, base, and emitter, with various resistors and capacitors connected as per the schematic notation. The text on the diagram refers to specific components and connections, indicating their function within the circuit. The labels for each component are clear and concise, providing a comprehensive guide for understanding the circuit's operation.
This circuit consists of two "OR" gates and one "AND" gate. Diodes CR1 and CR2 together with R2 comprise one "OR" gate, while diodes CR3 and CR4 together with R3 comprise the second "OR" gate.

When 0 volts is applied to any one or more of the inputs of an "OR" gate (C, D, M and N) the output of that gate is 0 volts (A and L).

When -6 volts is applied to all inputs of an "OR" gate, the output is -6 volts.

When 0 volts is applied to any one or more of the inputs to an "AND" gate (E and F), the output of that gate is -6 volts (B). When 0 volts is applied to all inputs of an "AND" gate, the output is 0 volts.

**NOTE:**
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS
This card consists of two identical circuits, which are basically common emitter amplifiers.

They are connected in such a way that they can act as an inhibit gate (or 'and' gate) when the base and emitter potentials are -6 to 0 volts (commonly, 0 to 5 volts) and the collector output is 0 volts (commonly, 0 to 5 volts). When this condition is met, Q1 and Q2 conduct, and the collectors clamp at -6 volts when non-conducting.

In order for Q1 and Q2 to conduct, there must be a coincidence of -6 volts applied at points B and D and 0 volts applied at points A and N. When this condition is met, the collector potentials are 0 volts (Q1 and Q2) and the collectors clamp the collectors at -6 volts when non-conducting.

<table>
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<th>NAME</th>
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<td>10k</td>
<td>Resistance</td>
<td>Gate to Base</td>
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<td>R2</td>
<td>10k</td>
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<td>Gate to Base</td>
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<td>Transistor</td>
<td>Common Emitter</td>
<td>Inhibit Gate</td>
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<tr>
<td>Q2</td>
<td>Transistor</td>
<td>Common Emitter</td>
<td>Inhibit Gate</td>
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</table>

**NOTE:**
- Card connections are represented by letters.
- Test points are represented by numbers.
START - STOP

SYMBOLS

OSCILLATOR

OSC.

OSCILLATOR IS ARRANGED TO OSCILLATE AT A FREQUENCY OF 1050 CPS.

THE NEGATIVE HALF CYCLE OF THE SINE WAVE IS PRODUCED IMMEDIATELY WHEN 0 VOLTS (GROUND) IS APPLIED AT THE INPUT.

THE CIRCUIT EMPLOYS TWO PNP JUNCTION TRANSISTORS.

Q1 IS CONNECTED AS A HARTLEY WITH THE OUTPUT TAKEN ACROSS THE RESONANT CIRCUIT L1.

WHEN THE INPUT IS AT 'SW', Q1 CONDUCTS DUE TO LOW RESISTANCE IN ITS PARALLEL CIRCUIT (ITS 'Q DOWN TO A VALUE TOO LOW TO SUSTAIN OSCILLATION).

IN THE STATIC, THE OUTPUT IS CLAMPED APPROXIMATELY 1.5 VOLTS DURING SUSTAINED OSCILLATION.

A SMALL RANGE ADJUSTMENT FOR FREQUENCY IS PROVIDED TO ADJUST FEEDBACK CURRENT TO SUSTAIN OSCILLATION.

NOTE: CONNECTIONS ARE REPRESENTED BY LETTERS; TEST POINTS ARE REPRESENTED BY SAMS.
The purpose of this circuit is to generate a pulse of 200 microseconds in width in response to an input. Normal (positive supply) and inverted outputs are provided. The quiescent state of this circuit is that Q2 is saturated, receiving its bias current primarily through R1 and R2 connected in parallel with R1, R3. The collector of Q2 is approximately -6V, while the collector of Q1 is maintained cut-off by C2 coupling of C1 and R1 returned to +15V, holding the base potential of Q1 at approximately +15V. The common emitter potential is 0V since C1 will now pass positive polarity transitions.

The circuit is triggered as follows: a "positive transition applied at point C drives Q2 into cut-off, which, in turn, allows Q1 to conduct. As the collector of Q1 approaches -6V, C2 conducts, allowing Q1 to maintain Q2 in cut-off. Q2 remains cut-off until Q1 can discharge sufficiently through C1 to inhibit conduction of Q1. The period of conduction of Q1 is linearly determined by the size of Q1 and R3.
The circuit 4 a magnet pulser is essentially a power oscillator whose output is provided by an NPN transistor. The output is feedback to produce a -8V to 0 signal to 12.5 em. in circuit.

**Diagram Description:**

In static condition Q2 is biased to 15V through R2 and Q3, Q1 acting as an emitter follower holding Q2 in cutoff condition. The output is at 15 volts with this voltage being applied to the collector lead (emitter point).

A positive pulse (10 - 100 microsec) applied to the input gate at Q1 will be applied only when the input signal of Q2 of the gate is at a 0 volts or slightly positive. The signal through Q2 and R5 is transmitted to Q2 and the output of Q2. Q2 is then turned on by applying a 15V to 15V pulse. The output voltage depends on the voltage applied to 

The input signal of Q2 has approximately a 15 to 15 microsec rise time and requires a large number of pulses to start a given. A positive signal higher than ground is turned off and the collector voltage is reached. Commonly Q2 will hold close to approximately 1 volt turning Q1 off.

**Diagram Elements:**

- **Q1:** NPN transistor
- **Q2:** PNP transistor
- **R1:** Resistors
- **C1:** Capacitors

**Legend:**

- **NPN:** Negative base, negative collector, positive emitter
- **PNP:** Positive base, negative collector, positive emitter

**Table:**

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>Resistors</td>
</tr>
<tr>
<td>C1</td>
<td>Capacitors</td>
</tr>
</tbody>
</table>
This card consists of two identical NPN common emitter amplifiers which provide an inverted output signal.

Q1 and Q2 have a reverse bias of approximately 6 volts with respect to Q3 and Q4. With a negative 6 volt stand applied at point 3 and 0, Q1 and Q2 are cut off immediately, causing the collector potentials to rise to +6 volts. Q3 and Q4 are used to provide a balanced signal for the duration of the light stand.

NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS.
This circuit is designed to operate in conjunction with the operating amplifier (17240 to 17240). The circuit is basically a hermetic representative amplifier and a regenerative detector. It is designed to amplify the ac input signal and produce a corresponding ac output pulse.

In the static condition -6 volts is applied to terminal 10, Q1 will conduct, the collector and emitter goes to +15 volts, and Q2 is off. The voltage of 6 volts at junction 0, and thus Q2 turns off. The transistor oscillator is turned on the collector of Q2 is about 0 volt and the oscillator is turned on at +6 volt (Q2). Since the emitter of Q2 is low, and in the junction of the emitter and collector of Q2 is negative, the collector potential will go to 0 volt during this time. A square-wave pulse will be produced once for every cycle of operation of the oscillator.

When the input goes positive and reaches a voltage level slightly higher than +1.2, Q2 will conduct and the collector will go to +12 volts. The collector potential is negative, and Q2 will conduct. Since the collector voltage will appear at output terminals 1 and 2.

NOTE:

AC CONNECTIONS ARE REPRESENTED BY LETTERS

TEST POINTS ARE REPRESENTED BY NUMBERS
### Circuit Description

**Pickup Amplifier**

**NOTE:**

The circuit consists of a signal generator connected to an amplifier. The input signal is applied to the base of Q1, which is biased for forward conduction. The signal is amplified and passed to the collector of Q1. The collector signal is fed to the base of Q2, which is also biased for forward conduction. The signal is further amplified and passed to the collector of Q2.

**Amplifier Circuit**

- **Q1**: PNP transistor
- **Q2**: PNP transistor
- **R1, R2**: Resistor values
- **C1, C2**: Capacitor values
- **L1**: Inductor

**Board Layout**

- **Inputs and Outputs**: Connections are labeled with letters and numbers for identification.
- **Components**: Transistors, resistors, capacitors, and inductors are labeled with their respective values.

**Test Points**: Test points are represented by numbers and are used for troubleshooting.

**Related Applications**

- **172 231**

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### Table: Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>10kΩ</td>
</tr>
<tr>
<td>R2</td>
<td>22kΩ</td>
</tr>
<tr>
<td>C1</td>
<td>0.1μF</td>
</tr>
<tr>
<td>C2</td>
<td>1μF</td>
</tr>
<tr>
<td>L1</td>
<td>56μH</td>
</tr>
</tbody>
</table>

**Diagram**: Detailed circuit diagram showing the connections and layout of the components on the board.

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**Note:**

Connections are represented by letters and test points are represented by numbers for easier identification and troubleshooting.
The purpose of this circuit is to generate a pulse of some width in the range of 0.5 to 1.5 milliseconds in response to an input. Normal transistor input and output signals are provided.

The output state of the circuit is to cut off all Q2 if the input signal, however small, is removed. Q1 is collected as soon as the output is generated by means of input signal through some diode connected to the output of Q1, Q2 and Q3 to Q1. The collector of Q1 is connected and the output is generated by means of input signal through some diode connected to the output of Q1, Q2 and Q3 to Q1. The output of Q1 is connected to the output of Q1, Q2 and Q3 to Q1. The output of Q1 is connected to the output of Q1, Q2 and Q3 to Q1.
This circuit consists of a RC integrator comprised of R1, R2 and C1, and a two stage regenerative amplifier comprised of Q1 and Q2. There is no polarity reversal between input and output signal, however there is a time delay between transitions. The integrator circuit will only permit pulses of relatively long duration to be applied to R3.

With a negative 6 V potential applied at point C, Q2 is biased in a forward direction, causing Q1 to be cut-off. Q1 and Q2 collector potentials are clamped at -6 V by CR1 and CR2.

With a positive 6 V transition applied to Q2 will cut-off after a time delay of 50 microseconds during which Q1 conducts, causing Q2 collector potential to rise from -6 V to 0 V. C2 and R7 provide regenerative feedback.

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basically of two relay drivers, each of which is composed of a relay driver circuit.

In the steady or "off" condition, Q1 is off. A negative voltage is applied to the base of Q1, which is connected through CR1, which is forward biased. A small amount of current flows from the base of Q1 to the anode of CR1. This current flows through resistor R1 and causes the voltage across CR1 to be more negative. A small amount of current flows from the base of Q3 to the anode of CR1. This current flows through resistor R1 and causes the voltage across CR1 to be more negative. A small amount of current flows from the base of Q4 to the anode of CR1. This current flows through resistor R1 and causes the voltage across CR1 to be more negative.

When a 5-volt signal or greater is applied to input M, Q4 is turned off. Collector load of Q3 is relay L coil. When signal or greater is applied to input M, Q4 is turned off. Collector load of Q3 is relay L coil.