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| REPORT DOCUMENTATION PAGE | | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|---|
| 1. REPORT NUMBER | 2. GOVT ACCESSION NO. | 3. RECIPIENT'S CATALOG NUMBER<br>CTR-830001 |
| 4. TITLE *(and Subtitle)*<br>QUARTERLY TECHNICAL REPORT<br>AN/PSC-3 - AN/VSC-7 | | 5. TYPE OF REPORT & PERIOD COVERED<br>Quarterly 25-September-82<br>25-December-82 |
| | | 6. PERFORMING ORG. REPORT NUMBER<br>Fifth Quarter |
| 7. AUTHOR(s)<br>Frank M. Brauer<br>Clem W. Munninghoff | | 8. CONTRACT OR GRANT NUMBER(s)<br>DAAK80-81-C-0185 |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS<br>Cincinnati Electronics Corporation<br>2630 Glendale-Milford Road<br>Cincinnati, Ohio 45241 | | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS<br>0012AA |
| 11. CONTROLLING OFFICE NAME AND ADDRESS<br>USA CECOM<br>Ft. Monmouth, NJ 07703 | | 12. REPORT DATE<br>15 January 1983<br>13. NUMBER OF PAGES<br>38 |
| 14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*<br>USA SATCOMA<br>DRCPM-SC-40<br>Ft. Monmouth, NJ 07703 | | 15. SECURITY CLASS. *(of this report)*<br>Unclassified<br>15a. DECLASSIFICATION/DOWNGRADING SCHEDULE<br>N/A |

16. DISTRIBUTION STATEMENT *(of this Report)*

Distribution limited to U.S. Government agencies only; Test and Evaluation; 15 January 1983. Other requests for this document must be referred to Commander; USA SATCOMA, Ft. Monmouth, NJ.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

N/A

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Modems, Signal Path, Synthesizer, Power Supply, Power Amplifier, System

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The AN/PSC-3 Program is progressing with small deviations from the proposed tech approach. The areas of deviation are summarized in a block-diagram "theory of operation" description.

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SECTION I

## 1.0 INTRODUCTION

This report describes the technical efforts during the fifth quarter of the AN/PSC-3 and AN/VSC-7 Production Program. The lead-in engineering to production is progressing with minor deviations to the proposed approach. In an effort to summarize the changes to the proposed approach, this report presents a block-diagram "theory of operation" description of the RT-1402 ( )/G, as presently configured for First Article build. All modifications to date are included in the "theory of operation" discussion. A separate section is included for 2400 bps modifications required under ECP-1. Not discussed, and unchanged since the last report, are the AN/VSC-7( ) and ancillary items such as battery box, antennas, etc.

SECTION II

## 2.0 TECHNICAL DETAILS

### 2.1 FRONT PANEL (AI8) AND FREQUENCY SELECTION (See Figure 1)

Summary - The Front Panel assembly consists of a front panel, a CPU (Central Processing Unit) PC Card and a Display PC Card. The Frequency Selection Circuits control the Display and command the RT's synthesizer. Frequencies between 225.000 MHz and 399.995 MHz (25 KHz increments in LOS; 5 KHz increments in SAT) may be selected by Front Panel Switches. Four satellite offsets may be selected with positive or negative frequency values between 000.000 MHz and 174.995 MHz. The CPU calculates all legal receive frequency combinations while in SAT mode of operation and flashes the DISPLAY if the resultant frequency is illegal.

### 2.2 FREQUENCY CONTROL AND DISPLAY

Summary - The Frequency Control is the controller for the RT. It controls whether the radio is to operate in LOS or SAT or any of the eight modes of operation as designated on the Mode switch.

Technical Description - Figure 1 is a block diagram of the Frequency Control and Display Assembly. The design incorporates a RCA CDP 1802 8-bit Microprocessor referred to as the CPU. The processor and associated circuitry are CMOS for low power consumption. An 8K-byte EPROM contains the operation and diagnostic program and 128 bytes of RAM with battery back-up hold frequency offsets and scratch pad locations. All circuitry is contained on two boards, with the microprocessor, memory, address decoding, synthesizer

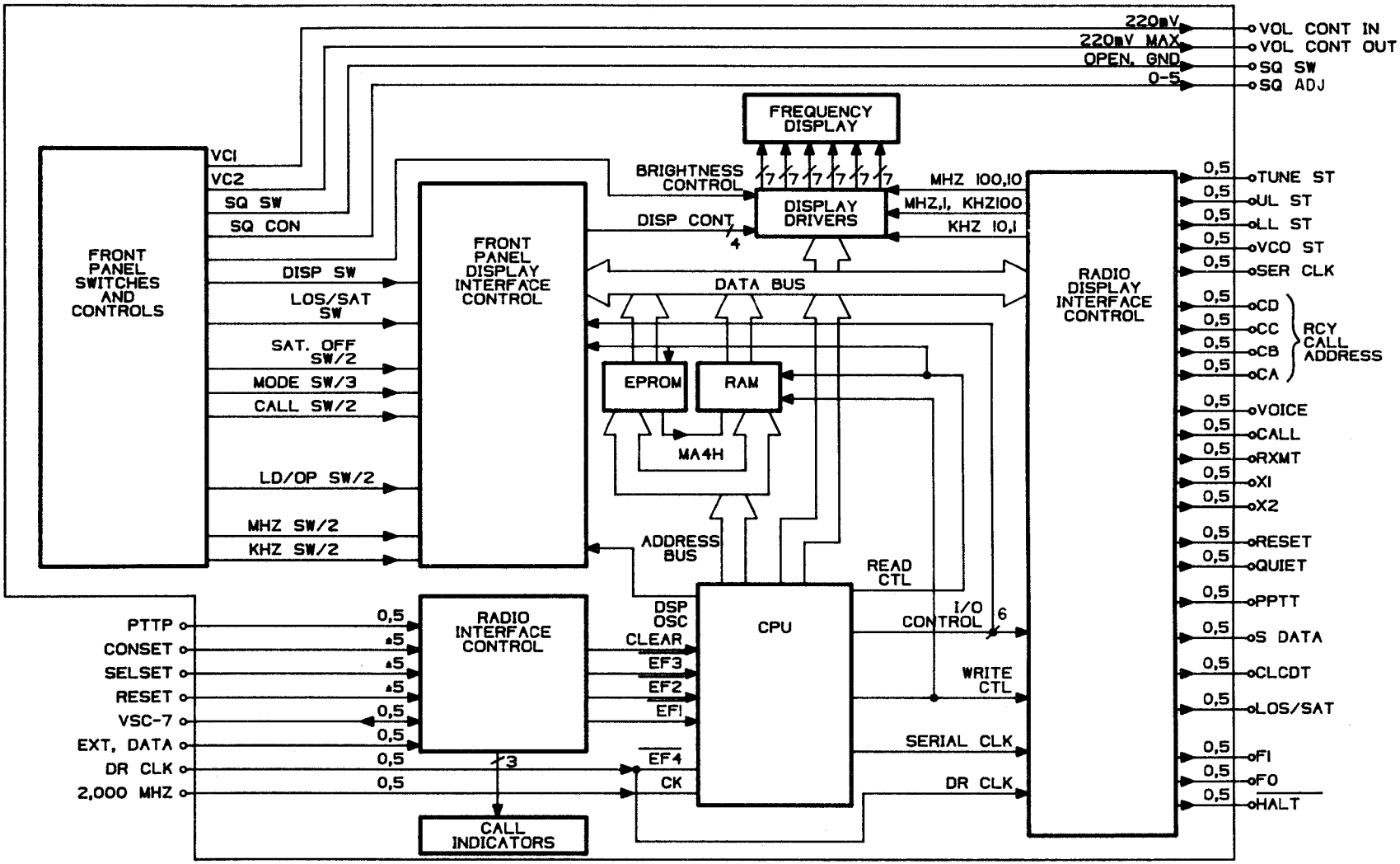


Figure 1. Frequency Control and Display Assembly

command latches, and Transmit Call Generator on one board and the display, display drivers, and wake-up circuitry on the other. This partitioning requires a minimum number of interconnections between boards and allows dual-in-line IC packages to be used rather than the hybrids used in the AN/PSC-1.

A N-line I/O controller is used in the frequency controller instead of the previously proposed memory-mapped I/O concept. The N-line I/O controller reduces the parts count and makes better use of the CDP 1802 capabilities. For example, if it is desired to write a value to the display, an "OUT" instruction will place the value on the data bus and the N-line I/O controller will cause the display strobe to be generated which latches the data value into the display. The Frequency Control switches are read in a similar manner. An "INPUT" instruction causes the appropriate switch buffer to be selected which latches the switch status to the data bus. The value of the data word which appears at the data bus is dependent upon the switches at that moment the "INPUT" instruction is executed.

At power up the microprocessor proceeds to initialize registers and then checks the RAM memory to determine if the frequency and status information is still valid. If the data in RAM is found to be invalid then the microprocessor re-initializes the RAM memory with 000.000 OFFSETS and then proceeds to tune the radio to 300.000 MHz. The invalidity implies either the back-up battery should be changed or the modules were recently separated. Activation of an external switch or a change in frequency selection cause the frequency controller to read the switches, compute and display the new frequency and send corresponding synthesizer commands, then after a short time delay shuts itself off via a pseudo "INPUT" request. This minimizes

the possibility of radio interference due to microprocessor clocks. Display activation is under software control. The Display brightness is adjustable from full brightness to complete darkness for blackout operations. When all operations have been completed and not any new status changes have been monitored the CPU will issue an "INPUT" instruction which will gate off the incoming clock and the microprocessor will "sleep." The CPU will awaken if a front panel switch has been moved.

The LOAD/OPERATE switch located on the CPU PC board can be reached by removing the bottom plate of the RT. For normal RT operation the LD/OP switch must be in position 2. Positions 1 and 3 are reserved for loading negative and positive satellite offset frequencies respectively. For example, if a negative 41.275 MHz is wished to be loaded as satellite offset B, the LD/OP switch would be placed in position 1. Next, by using the MHz and KHz switches, display the frequency on the display. Now rotate the LD/OP switch to position 2 for normal operation. The same procedure can be used for loading positive offsets except the LD/OP switch must be in position 3. If no offsets have been loaded into the RT then the default offset frequency will be 000.000 MHz.

The synthesizer D/A generator pre-position voltages and Tuner commands are nonlinear functions of the tuned frequency and are generated via a look-up table. The N and A counters for the Lower and Upper Loops in the synthesizer are generated by number crunching.

Several features which were not included in the AN/PSC-1 frequency controller have been added for AN/PSC-3. The first new function is control over the transmission of Call messages. It is a simple matter to store the Barker

word format and Call message structure in memory and then monitor the Call switch for a SEND command. This method saves considerable circuitry over that used in the original AN/PSC-1 and also simplifies the interface of the RT and the NCS Applique in the AN/VSC-7 since serial information regarding the Selective Call to be transmitted can be fed directly to the microprocessor. The second new feature is a complete diagnostics program in program memory. This software feature eases testing of CPU PC boards and greatly enhances the troubleshooting of the board and pinpoints bad parts with far greater accuracy.

2.3 SIGNAL PATH (See Figure 2)

The AN/PSC-3's receive signal path consists of the Harmonic Filter (FL1), Tuner (A2), 69.4 MHz IF (A7), and 10.6 MHz IF (A8). The received signal enters the Antenna connector and passes through the Harmonic Filter to the T-R relay. In receive mode, the signal is applied to the Tuner module; in transmit mode, the T-R relay connects the Harmonic Filter to the output of the Power Amplifier.

Tuner (A2) and Harmonic Filter (FL1) - The signal input to the Tuner module passes through a high-pass filter which attenuates HF and VHF signals, to prevent interference from co-located transmitters (for example, in retransmission mode). Embedded within the high-pass filter is an active attenuator which senses the presence of high-level input signals and protects the low-noise stages from damage from signals up to +30 dBm CW. The two-stage broadband low-noise amplifier provides high gain, and is the major contributor to the low system noise-figure. After the low-noise amplifier, the signal passes through a voltage-tuned bandpass filter, which reduces response to spurious and image signals. (The bandpass filter is tuned by the output

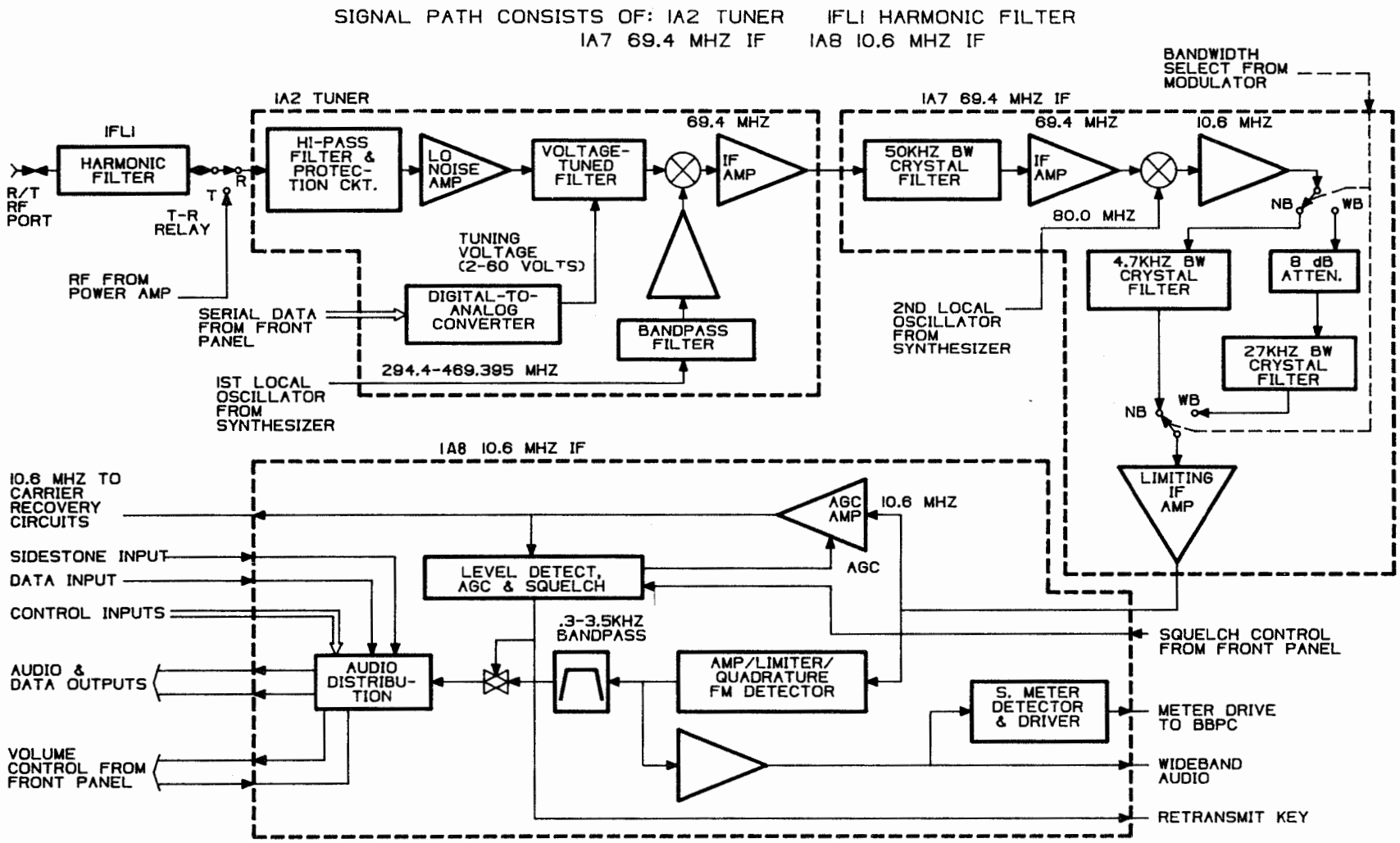


Figure 2. AN/PSC-3 Signal Path

of a digital-to-analog converter, which is addressed from the serial data stream sent by the Front Panel module.) The output of the bandpass filter is applied to a passive mixer for conversion to the first intermediate frequency, 69.4 MHz. The first Local Oscillator signal, applied to the Tuner module by the VCO module (part of the Synthesizer), is passed through a bandpass filter and amplified for use as the pump of the passive mixer. The mixer output, the 69.4 MHz IF, is fed to a low-noise amplifier, amplified, and applied to the 69.4 MHz IF module through a low-pass filter. This filter attenuates the first Local Oscillator signal, which can leave the Tuner module and generate spurious responses throughout the 225-400 MHz range.

69.4 MHz IF - The first IF signal, applied to the 69.4 MHz IF module, is passed through a four-pole 50 KHz BW crystal filter and a low-noise amplifier. (Referenced to the antenna, this low-noise amplifier is the last contributor to the system noise-figure). A passive mixer follows the amplifier, converting 69.4 MHz to the second IF, 10.6 MHz. The second Local Oscillator, 80.0 MHz, is applied to the 69.4 MHz IF module from the Reference module (part of the Synthesizer). The second IF signal is amplified and applied to one of two crystal bandpass filters. For Call and Data modes, a 4.7 KHz filter is used; 27 KHz bandwidth is required for Voice and X-modes of operation. An 8dB attenuator is included in the wideband path to assure constant noise power in the second IF. The bandlimited second IF is amplified and fed to the 10.6 MHz IF module. The second 10.6 MHz amplifier is linear for low signal levels, limiting only for "strong" signals. (Linear operation at low C/KT improves BER by about 1dB over a limited signal.)

10.6 MHz IF - The 10.6 MHz IF module passes the second IF signal through a gain-controlled amplifier and level detector, and outputs the AGC'd second IF signal to the Carrier Recovery #1 module. Demodulated data is returned to the 10.6 MHz IF module for distribution through the RT's various I/O ports. For wideband modes (Voice, X1, and X2) the second IF signal is tapped off into an integrated circuit amplifier/limiter/quadrature detector for demodulation. Wideband audio is supplied to the X-mode connector, and detected for use as a signal-to-noise indication in the wideband modes. (The level detector embedded in the AGC system is used for squelch and retransmit key generation.) Wideband audio is also passed through a bandpass filter, gated by the squelch and control systems, and distributed to the various RT I/O's. During transmit operation, sidetone is returned to the 10.6 MHz IF to be supplied to the handset. When power output drops below 11 watts (SAT) or 0.6 watts (LOS), the sidetone is muted to notify the operator of a fault condition.

## 2.4 SYNTHESIZER (See Figure 3)

The AN/PSC-3's synthesizer consists of the VCO (A3), Upper Loop (A4), Lower Loop (A5), and Reference (A6) modules. The synthesizer provides first and second local oscillator injections and the modem's phase-reference in receive mode, and a modulated on-channel output for transmit mode.

Reference (A6) - The Reference module provides the RT with a series of highly-stable signals which are essential to the proper operation of any satellite communications system. A temperature-compensated crystal oscillator provides the basic 4.0 MHz signal from which all other synthesizer signals are derived. After suitable buffering, 4.0 MHz reference is supplied to the Carrier Recovery, Bit Sync, and Modulator portions of the modem, and

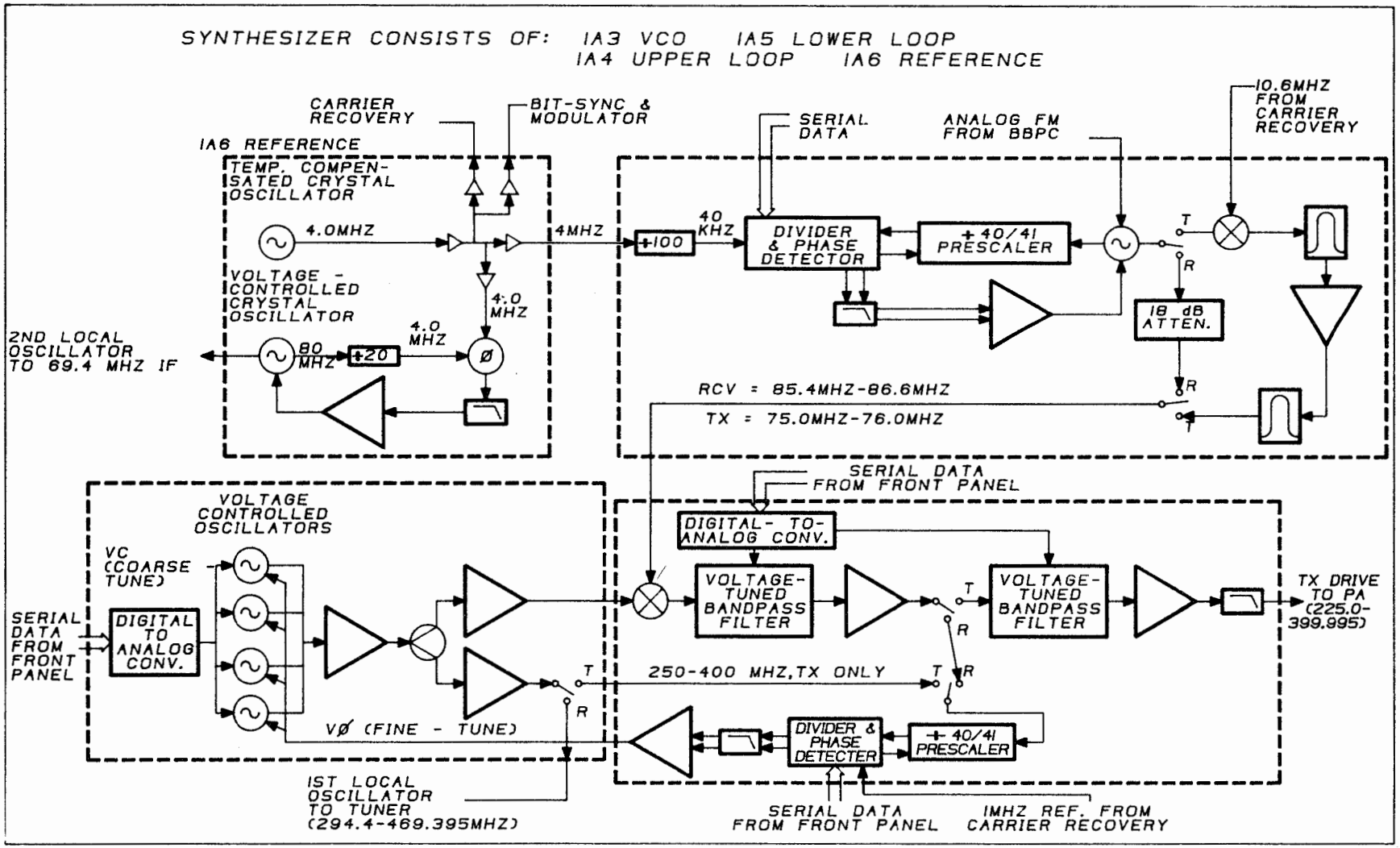


Figure 3. AN/PSC-3 Synthesizer

to the Lower Loop module. 4.0 MHz is also applied to a passive phase-detector; the output of a 80.0 MHz crystal oscillator, divided by 20, provides the second input to the phase-detector. The phase-difference output is low-pass filtered, amplified, and returned to the 80.0 MHz oscillator's control input, phase-locking the 80.0 MHz to the 4.0 MHz system reference. The 80.0 MHz signal is applied to the 69.4 MHz IF module as the second local oscillator.

Lower Loop - The 4.0 MHz signal from the Reference module is divided by 100 and the resulting 40 kHz is applied to a monolithic phase-locked loop integrated circuit where it is divided by eight, and the resulting 5 kHz becomes the reference for a phase-frequency detector.

A voltage controlled oscillator provides an output from 85.4 to 86.6 MHz. Part of this output is fed to a dual-modulus (÷ 40/41) prescaler, whose output is fed to the PLL IC. Using the prescaler, two internal counters, and control logic, the PLL IC divides the VCO signal to 5 kHz and applies it to the phase-frequency detector. The phase-difference output from the phase-frequency detector is low-pass filtered, amplified, and applied to the VCO to phase-lock the VCO to a 5 kHz increment, from 85.4 through 86.6 MHz. A serial data stream from the Front Panel Module loads the divisors into the PLL IC, determining the specific VCO frequency.

In receive mode, the Lower Loop's VCO signal is attenuated by 18 dB and supplied to the Upper Loop module.

For transmit, the Lower Loop's VCO output is mixed with a 10.6 MHz signal obtained from the Carrier Recovery #1 module. In CALL, DATA, and X2 (TSEC/KY-57) modes the 10.6 MHz signal is modulated, and the resulting difference

frequency (75.0 to 76.0 MHz) is therefore identically modulated. During Voice and X1 (TSEC/KY-65) modes, the 10.6 MHz is unmodulated and a frequency-modulation input to the Lower Loop's VCO is enabled. Analog information from the Baseband Processing and Control module is used to FM the VCO, at rates from 300 to 3500 Hz, and the difference frequency (75.0 to 76.0 MHz) is FM'd identically to the VCO. (The modulating frequencies applied to the VCO are higher than the phase-locked loop's response capability and therefore do not cause the PLL to break lock.)

The mixer output is bandpass filtered to remove the VCO and sum signals, leaving only 75.0 to 76.0 MHz; the signal is then amplified by a monolithic amplifier configured as a limiter and passed through a second bandpass filter to further attenuate mixing products and harmonics generated in the mixer and limiting amplifier. (The limiting action is required due to the method of generation of, and crystal filter in the path of, the modulated 10.6 MHz received from the Carrier Recovery #1 module by the Lower Loop. Rapid changes in phase and magnitude of two quadrature signals used to generate the modulated signal cause amplitude variations in the output, and nonlinearities in the phase response of the modulator's crystal bandpass filter convert phase-shift to amplitude variations in the modulated 10.6 MHz. This AM, if allowed to propagate through the Lower Loop and Upper Loop transmit path can induce unwanted phase-shift caused by changes in DC currents in its vicinity of the Upper Loop's phase-detector.)

The Lower Loop output, either 85.4 to 86.6 MHz in receive mode or modulated 75.0 to 76.0 MHz in transmit mode, is passed to the Upper Loop module.

VCO (A3) - Four voltage-controlled oscillators, covering the range from 250.0 to 469.395 MHz, are used to provide the signals required for proper operation of the synthesizer. Transmit operation uses three oscillators to generate 250 through 400 MHz; receive operation requires two of the oscillators used in transmit, and a third unique to receive mode, to generate 294.4 through 469.395 MHz. Two control signals, which are determined by the frequency displayed on the front panel and the SAT OFFSET selected (in SAT mode only), are sent by the Front Panel module as a part of the Lower Loop's serial data stream, latched into the Lower Loop's PLL IC's shift register, and output to the VCO module as OSC SEL A and B. These binary control signals are decoded by the VCO module and determine which of the four oscillators is energized.

All four oscillators are tuned by varactor diodes. A "pre-position" or "coarse tuning" voltage is applied to the cathodes of all four varactors in parallel (since only one oscillator is powered at any given time, and the varactors are well decoupled from each other at RF, there is no interaction between the four varactors). The "coarse tune" voltage, or Vc, is supplied by a digital-to-analog converter on the VCO module; the digital word determining the Vc voltage is sent as part of the serial data stream from the Front Panel module. The anodes of the four varactors are similarly decoupled and parallelled; the "fine tuning" of the oscillators is performed by the VØ line, which is the output of a phase-detector/loop-filter combination on the Upper Loop module.

The outputs of the VCO's are parallelled through PIN diode switches, which isolate all the oscillators except the one to which power has been applied. After amplifying, padding, and splitting, the oscillator output is sent to

the Upper Loop module as the pump for a mixer, and either to the Tuner module (as the 1st Local Oscillator) or to the Upper Loop as the input to a dual modulus prescaler.

Upper Loop (A4) - The Upper Loop module controls the frequency of the oscillators on the VCO module, and is essentially the heart of the Synthesizer.

In receive mode the Lower Loop output (85.4 to 86.6 MHz) is mixed with an output of the VCO module (294.4 to 469.395 MHz) and the resulting sum or difference frequency (in the range of 229 to 400 MHz) is bandpass filtered and applied to the input of a dual-modulus (÷ 40/41) Prescaler. (The bandpass filter used is voltage-tuned, and is identical to the filter used within the Tuner module. A digital-to-analog converter, also identical to the one used by the Tuner, provides the tuning voltage required by the voltage-tuned filter, under the command of the serial data stream transmitted by the Front Panel module.) The output of the dual-modulus prescaler is fed to a PLL IC. Using the prescaler, two internal counters, and control logic, the PLL IC divides the filtered sum or difference frequency to 125 kHz, which is applied to PLL IC's phase-frequency detector. Information required by the PLL IC is sent by the Front Panel module as a part of the serial data stream. A 1 MHz signal, divided from the 4.0 MHz system reference in the Carrier Recovery #1 module, is applied to the PLL IC where it is divided by 8 to 125 kHz, and forms the reference input to the PLL IC's phase-frequency detector. The phase-difference output from the phase-frequency detector, after suitable low-pass filtering and amplification, is applied to the VCO module as the fine-tune (V$\phi$) signal, locking the sum or difference of the Lower Loop and VCO signals to a multiple of 125 kHz and therefore the first Local Oscillator signal to the required frequency. See Table 1 for the fre-

Table 1.

| DIAL (TRANSMIT) OR ACTUAL (RECEIVE) FREQ. | MODE | OSC. SEL. A | B | LOWER LOOP VCO FREQUENCY | UPPER LOOP FREQUENCY | UPPER LOOP D/A "ADDRESS" |
|---|---|---|---|---|---|---|
| 225.0 - 266.995 | T | 1 | 0 | 86600 - (KHZ DIAL) | 76 + (MHZ DIAL) (301→342MHZ) | MHZ DIAL |
| 267.0 - 324.995 | T | 0 | 1 | 86600 - (KHZ DIAL) | 76 + (MHZ DIAL) (342→400MHZ) | MHZ DIAL |
| 325.0 - 369.995 | T | 0 | 0 | 85600 + (KHZ DIAL) | (MHZ DIAL) -75 (250→294MHZ) | MHZ DIAL |
| 370.0 - 399.995 | T | 1 | 0 | 85600 + (KHZ DIAL) | (MHZ DIAL) -75 (295→324MHZ) | MHZ DIAL |
| 225.0 - 244.995 | R | 1 | 0 | 86600 - (ACTUAL KHZ) | 158 + (ACTUAL MHZ) (381→400MHZ) | → |
| 245.0 - 272.995 | R | 1 | 0 | 85400 + (ACTUAL KHZ) | (ACTUAL MHZ) -16 (229→258MHZ) | → |
| 273.0 - 331.995 | R | 0 | 1 | ↓ | (257→315) | ↓ |
| 332.0 - 399.995 | R | 1 | 1 | ↓ | (316→383) | ↓ |

OSC 00→250.0 - 294.0
10→294.4 - 342.395
01→342.4 - 401.395
11→401.4 - 489.395

quencies used for generation of the Lower Loop, first Local Oscillator, and TX Drive signals. (In receive mode, the first Local Oscillator frequency is the actual receive frequency [dial frequency in LOS, or dial plus offset frequency in SAT] plus 69.4 MHz. The column marked "Upper Loop Frequency" shows the frequency to which the PLL will force the input of the dual-modulus prescaler when the Upper Loop is phase-locked. In transmit mode, the true Lower Loop output signal is 10.6 MHz less than the Lower Loop VCO frequency shown.)

In transmit mode a VCO output is fed directly into the dual-modulus prescaler, and the Upper Loop PLL system forces the VCO signal to lock to a multiple of 125 kHz. (The necessary information for the PLL IC, as in receive mode, is sent on the serial data stream by the Front Panel module.) The same VCO frequency, obtained from a different path from the VCO module, mixes the Lower Loop signal to the transmit output frequency; the proper mixing product (either sum or difference) is selected by the voltage-tuned filter, amplified, and filtered by another voltage-tuned filter (2-pole vs. 4-pole like the Tuner). This well-filtered product is then amplified to a level greater than 10 milliwatts, low-pass filtered, and supplied to the Power Amplifier module.

2.5 CARRIER RECOVERY #1 (See Figure 4)

Receive Mode - The 10.6 MHz receive signal from the IF (the 10.6 module) is switched into a mixer which has a LO of nominally 11.6 MHz. The 1 MHz product of this mix is selected by a 1 MHz Lowpass filter. This filtered output is amplified then applied to a quadraphase demodulator, which has a LO of 1 MHz, divided from the 4 MHz system reference. This quadraphase demodulator has an I channel and a Q channel output. The I channel is the

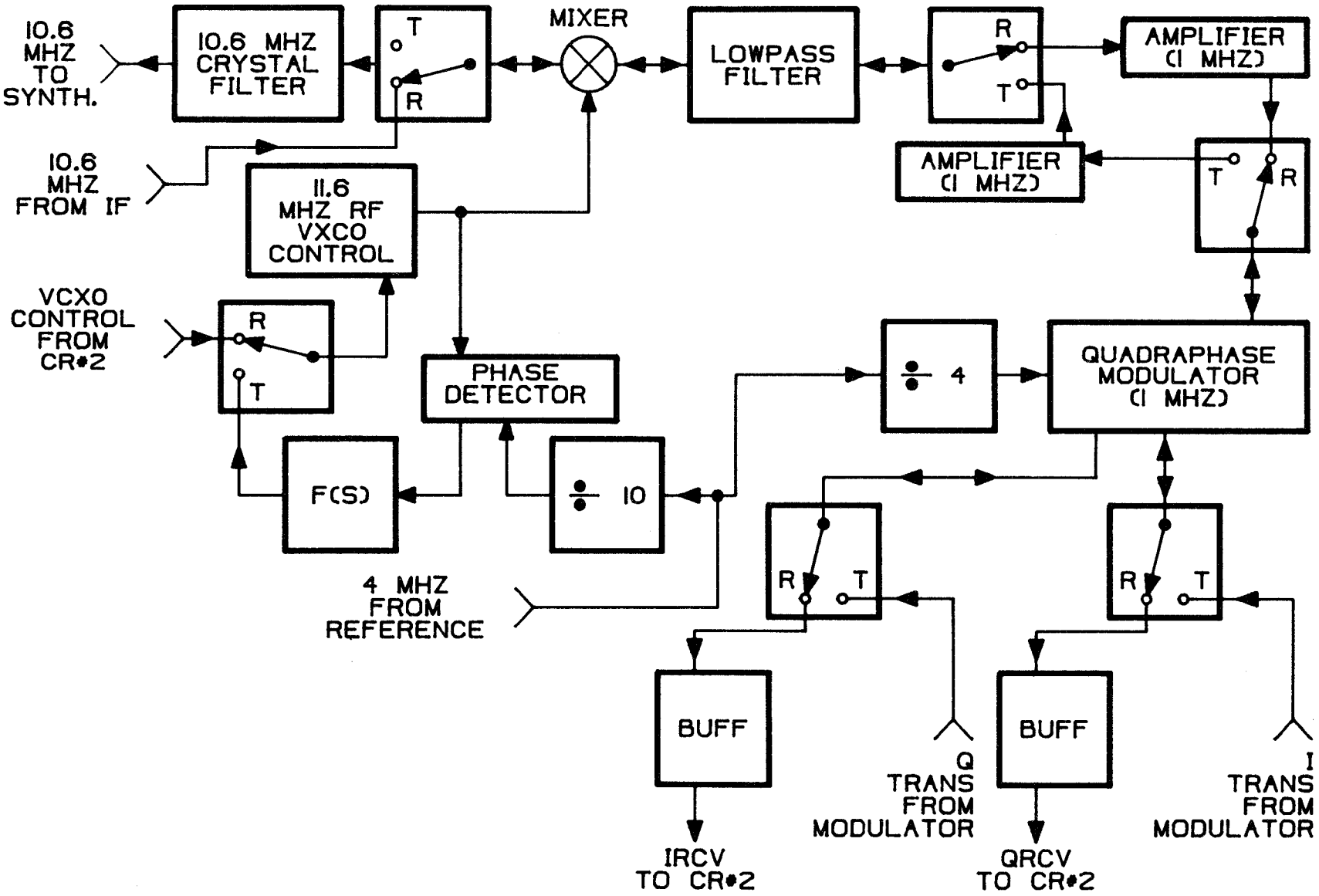


Figure 4. CR #1

inphase projection of the receive signal upon the reference phase and the Q channel is the projection of the receive signal upon the reference phase plus 90°. The two baseband signals are sent to CR#2, which serves as the receive loop phase detector and generates a correction voltage to the 11.6 MHz VCXO to bring the carrier recovery system into phase-lock with an incoming signal.

Transmit Mode - I TRANS and Q TRANS waveforms from the modulator board are switched into the quadraphase modulator which has a LO of 1 MHz. The resulting 1 MHz phase or frequency modulated signal is switched into an amplifier which drives the input to the lowpass filter through another switch. The output of this lowpass filter is mixed with 11.6 MHz. The result of this mix is switched into the 10.6 MHz crystal filter to yield an output of 10.6 MHz to the synthesizer. In Data, CALL and FSK modes, the 10.6 MHz output is phase or frequency modulated by the data. In Voice mode the 10.6 MHz is unmodulated.

In order to ensure 10.6 MHz frequency accuracy, the 11.6 MHz VCXO is phase-locked to the 4 MHz reference. 4 MHz divided by 10 is used as the sample frequency in a harmonic phase detector with the 11.6 MHz as the sampled input. The error output is applied to a loop filter (F(S)) which drives, through a switch, the 11.6 MHz VCXO control line. The result is to lock the 11.6 MHz VCXO to the 29th harmonic of the 400 kHz sample frequency.

CARRIER RECOVERY #2 (See Figure 5)

Receive - Carrier lock is necessary for BPSK data modes. CR#2 provides a correction voltage to the VCXO on CR#1 to bring the VCXO into phase-lock with the incoming signal, yielding coherent phase demodulation.

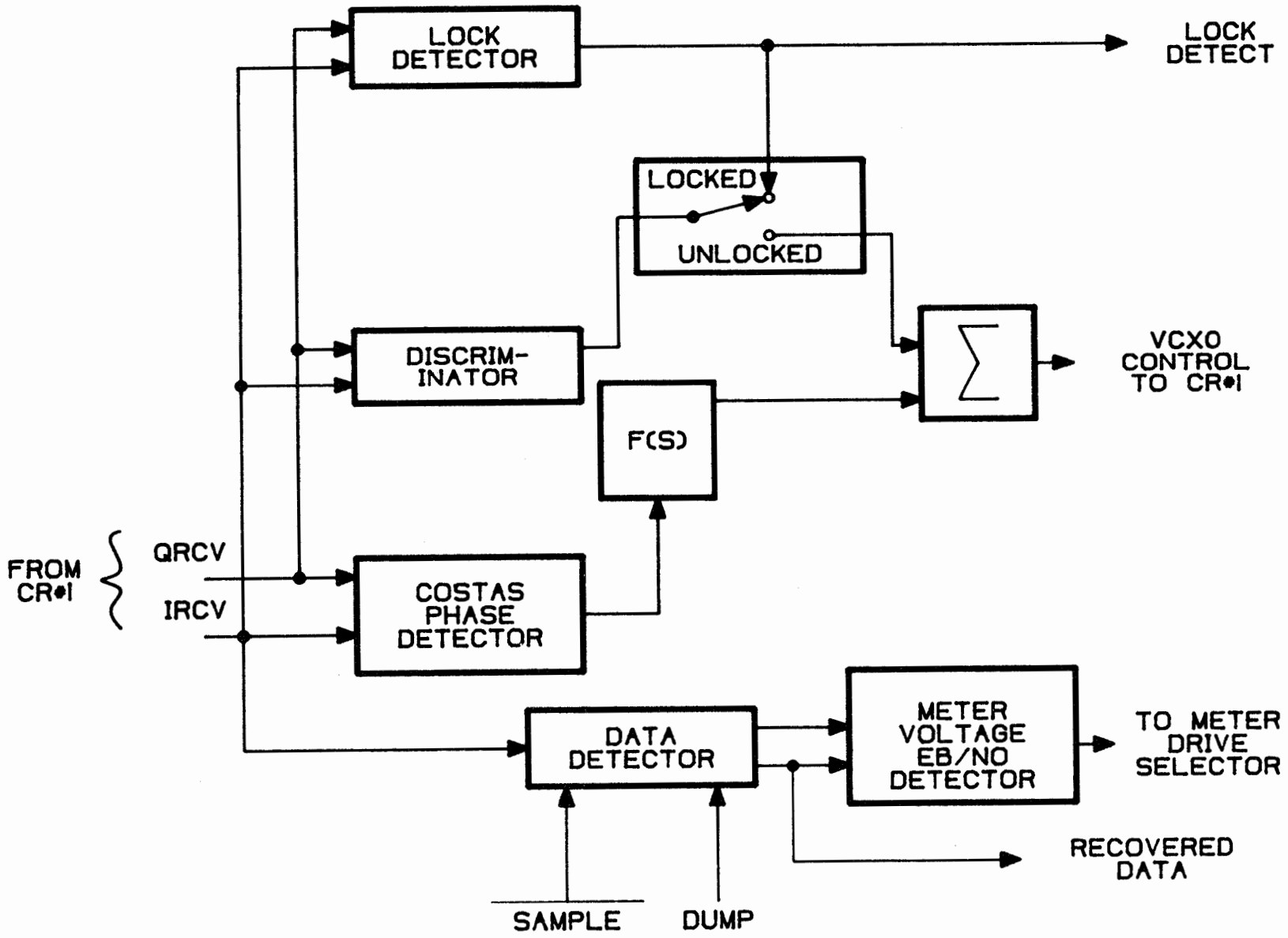
LOCK DETECTOR
LOCK DETECT
LOCKED
UNLOCKED
DISCRIM-INATOR
VCXO CONTROL TO CR•I
F(S)
FROM CR•I
QRCV
IRCV
COSTAS PHASE DETECTOR
DATA DETECTOR
METER VOLTAGE EB/NO DETECTOR
TO METER DRIVE SELECTOR
RECOVERED DATA
SAMPLE
DUMP

Figure 5. CR #2

CR#2 is needed only for DATA 300, 1200, 2400 and CALL modes.

I RCV and Q RCV baseband signals from CR#1 are applied to a Costas phase detector, a discriminator, and a lock-detect circuit. The I RCV also goes to the data detector. The Costas phase detector output goes through a loop filter (F(S)) and is summed with the output of a frequency discriminator when the loop is not locked. The discriminator serves to move the VCXO toward the frequency required to convert the incoming signal to 1 MHz. Once the discriminator has pulled the VCXO close enough to the proper frequency for the Costas phase detector to contribute phase corrective voltage to the VCXO control line, the lock detector circuit will indicate a locked condition if the signal is large enough to be useful, and the frequency discriminator will be disconnected from the loop.

Bit Sync #1 (See Figure 6) - The primary function of the Bit Sync is to provide a data-rate clock in phase with received data or external data to be transmitted.

BS#1 accepts the received I channel from CR#1 in receive mode and accepts data to be transmitted from the Modulator while in transmit mode.

The data recovery circuitry digitally integrates the data in 16 steps over each bit period and compares this bit period energy to a set threshold and determines if the information during each particular bit period is a data high or data low. This recovered data goes to BS#2 where it is used in the synchronization process as polarity information. It is not gated to the outside world.

The phase detector compares the energy between two halves of a bit period of the data and determines whether there is equal energy indicating synchroni-

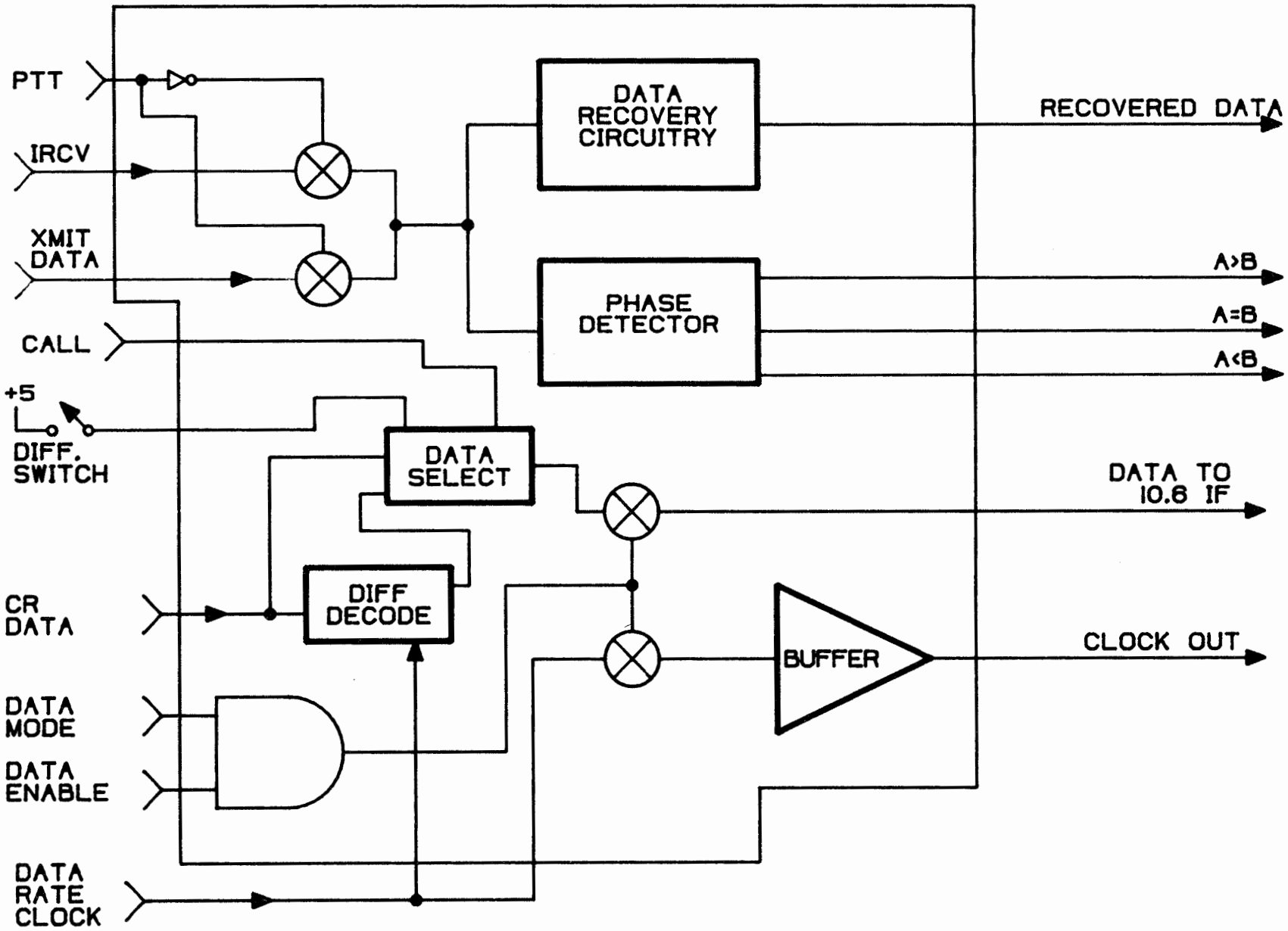


Figure 6. Bit Sync #1

zation of data and clock or, if not, which phase direction the clock should move to become in sync with the data. The information is sent to BS#2.

In receive, recovered data from CR#2 enters BS#1 and is differentially decoded. A data selector chooses either differentially decoded or non differentially decoded data depending on the position of a switch located on the inside case of the radio. Non-differentially decoded data will always be selected when the radio is in CALL mode.

If the radio is in one of the Data modes and all loops are locked, this data will be gated to the 10.6 IF module.

The data rate clock from BS#2 is gated and buffered and sent to the 5-pin Audio/Data interface connector.

Bit Sync #2 (See Figure 7) - Phase information from BS#1 enters BS#2 and is integrated over a number of bit periods at which point an advance or retard phase signal is sent to a variable ÷ N counter which will then advance or retard the data-rate clock. The rate of clock frequency change is determined by the offset select circuitry and controlled by the "step size" signal which is generated on the Baseband Processing and Control board. The clock is quickly brought close to the required frequency during acquisition by changing the frequency by a large amount. After lock, small frequency changes are used to minimize clock jitter.

The output from the variable ÷N counter goes to the selectable clock generators which output the data-rate clock and other multiples of the clock which are used elsewhere.

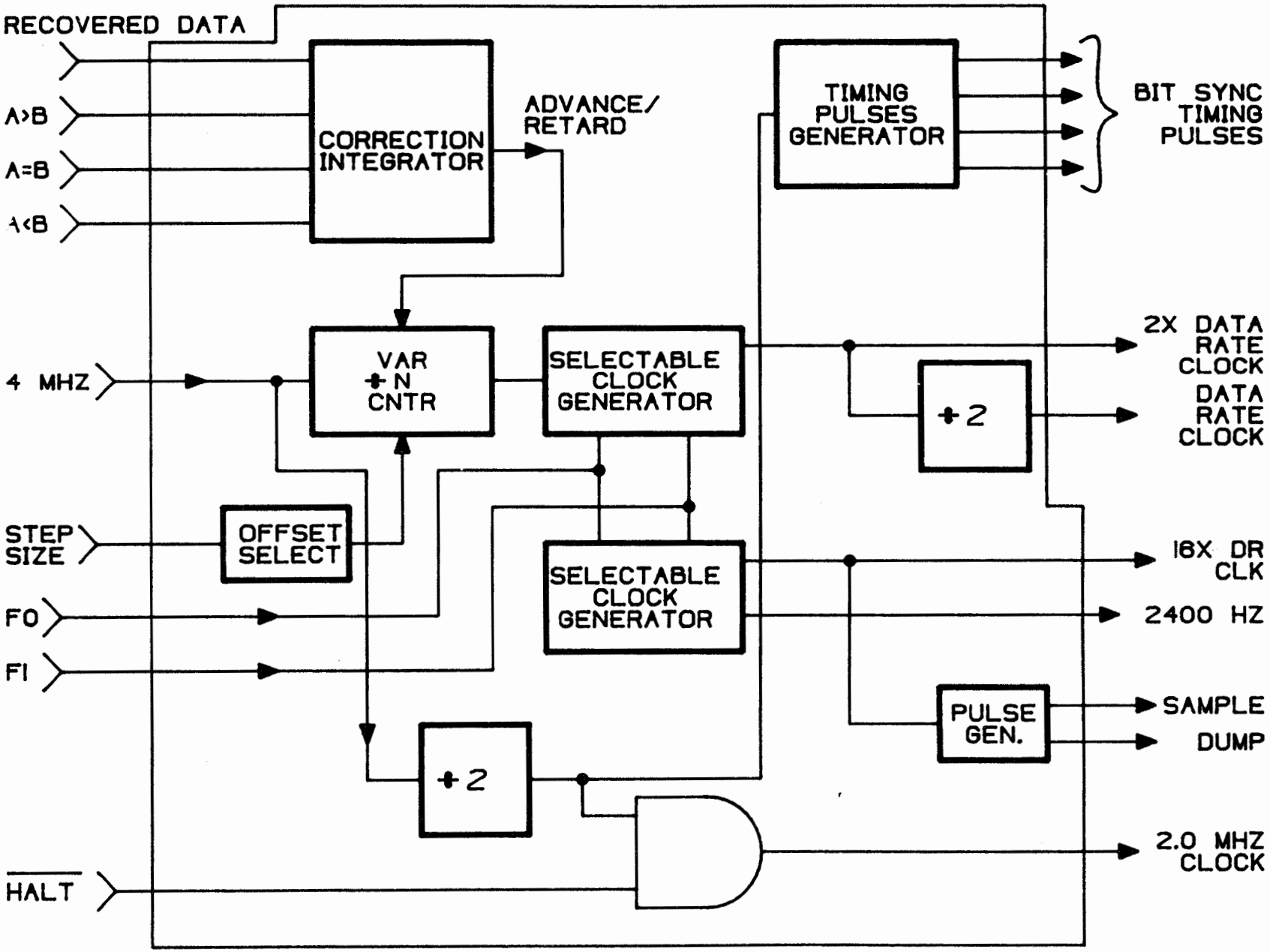


Figure 7. Bit Sync #2

The frequency of the data-rate clock is controlled by F0 and F1 which are mode signals from the front panel.

A pulse generation circuit generates synchronous "sample" and "dump" timing signals used by CR#2 in recovering data.

The 4 MHz is divided down to 2 MHz which is gated to the front panel microprocessor and is controlled by the signal $\overline{\text{HALT}}$ which is generated by front panel circuitry.

The 2 MHz is also used to generate timing pulses used by the Bit Sync.

Modulator (See Figure 8) - Data to be transmitted is differentially encoded. A "data selector" chooses either non-differentially encoded data or differentially encoded data depending upon the position of the differential decode switch. The data pulser produces a pulse in sync with the 4 MHz clock for every data transition.

The 4 MHz is divided down by a variable divider. The resultant frequency is dependent upon whether the radio is in BPSK mode or FSK mode.

The UP/DOWN counter drives two digital to analog converters. The divided 4MHz is used as the clock to the UP/DOWN counter and the UP/DOWN line is controlled in part by the data pulses and also by other control circuitry dependent upon whether the radio is in BPSK mode or FSK mode.

The end result is orthogonal I and Q channels which are used on CR#2 to rotate the carrier phase using a quadrature modulator.

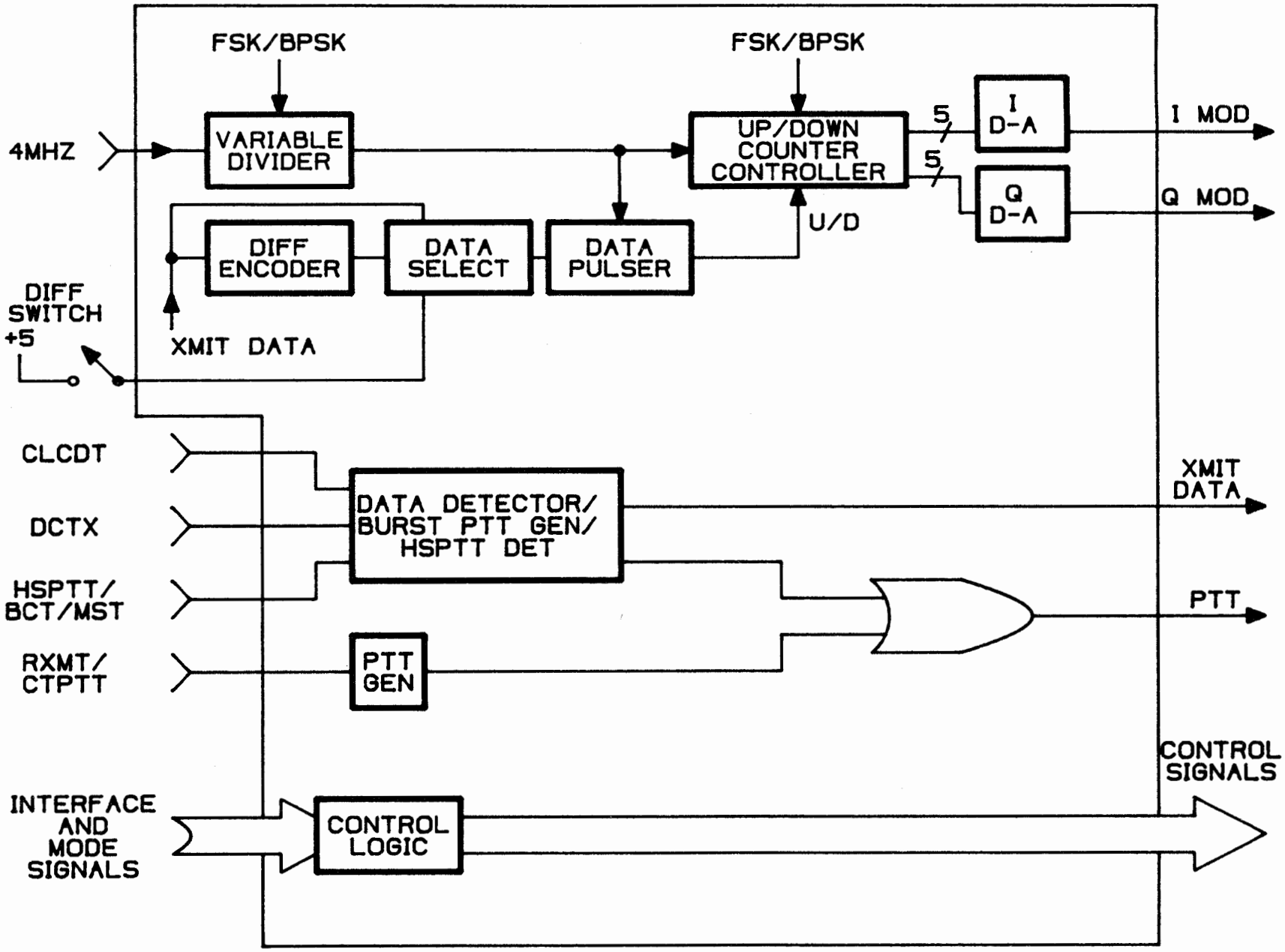


Figure 8. Modulator

Also present on the Modulator board is transmit interface circuitry.

Three sources of data are detected: Call code transmit data from the microprocessor, digital cipher-text transmit data from a KY-57 and Mil-Std data from a DMDG. The presence of Burst data at HSPTT/BCT/MST from a DMDG in Data Modes will cause a PTT signal to be generated. In voice mode, GND closure from a handset at HSPTT/BCT/MST will generate PTT.

A GND closure at RXMT/CTPTT from any of the RXMT radios or XMODE devices will generate PTT.

Other various interface and mode signals are processed and control signals are generated.

Call Decode (See Figure 9) - A call message is made up of a number of 7-bit Barker words. In CALL RCV mode, received data and the data-rate clock from BS#1 go to the Barker word decoder. Provided the received data is a valid Call message, the Barker decoder decodes the receive data and obtains the Call message sent which will be the number 0-15. This information is sent to the message comparator. If the message is zero a Conference Call is indicated. If not, the message comparator compares the received number to the number preset at the on-board 16 position switch or, if the radio is in the NCS applique, it will compare the received number to that set on the NCS applique. A signal from the NCS applique controls a selector to choose which preset number is compared.

If the received number is the same as the preset number then a Selective Call is indicated.

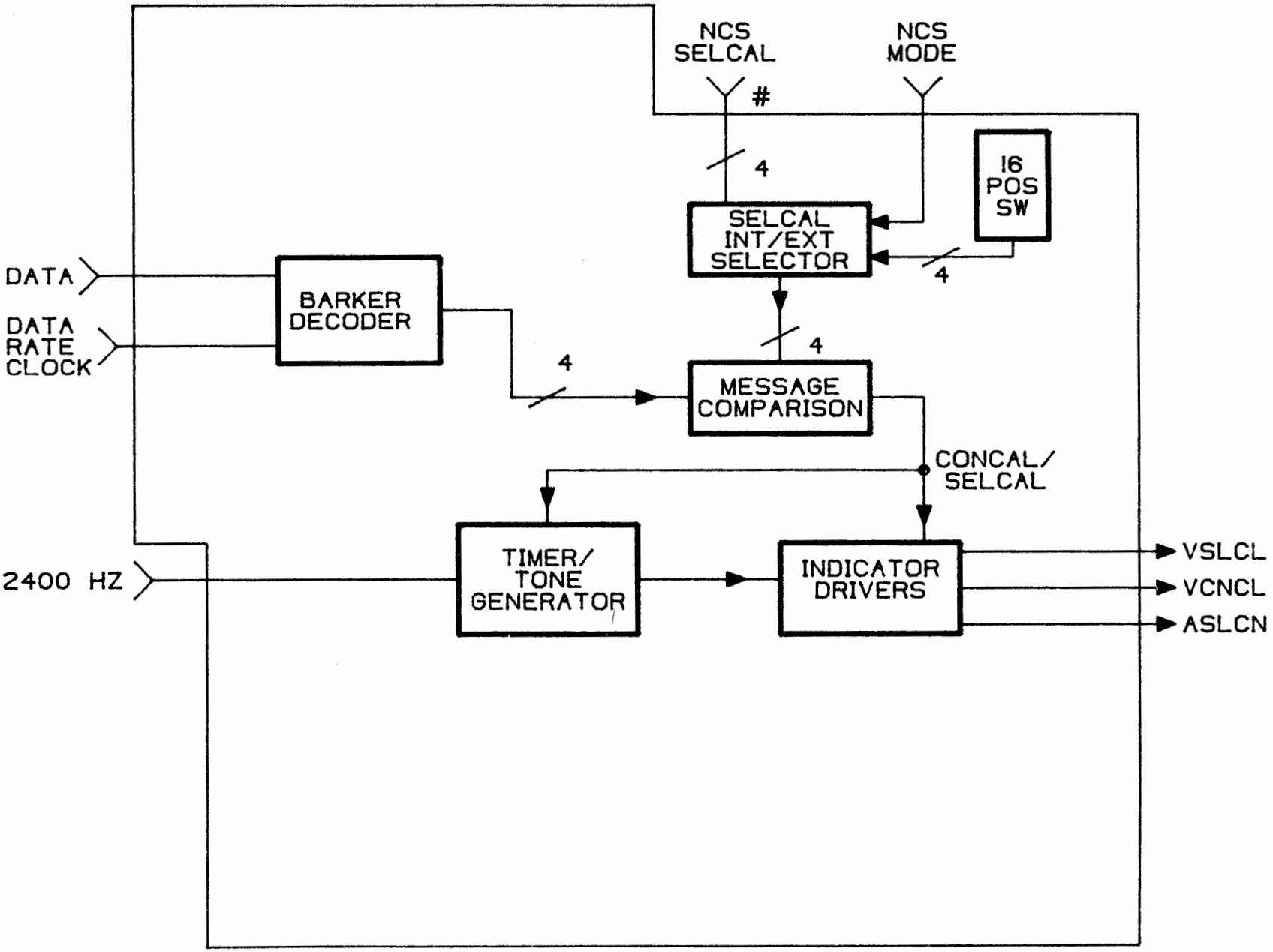


Figure 9. Call Decode

The CONCAL or SELCAL signal goes to the indicator drivers and the timer and tone generator. The indicator drivers drive the visual latching indicators and the buzzer. The timer/tone generator produces indicator pulses and buzzer tone and also a 60 sec timeout of the CALL circuitry following the detection of a Conference or Selective call.

## 2.6 BASEBOARD PROCESSING AND CONTROL (See Figure 10)

Front panel status information is buffered and processed by control logic to provide control signals used throughout the radio.

Loop-lock indications from the Carrier Recovery Loop, Lower Loop and Upper Loop are processed and delayed appropriately (based on the bit-rate) to provide lock control signals which go the PA and Bit Sync.

Signal-strength meter drives (0-1v.) from several sources are switched and processed to provide the appropriate signal-strength meter drive current for the various modes.

Audio inputs from a handset, KY-65, KY-57, or RXMT radio are switched appropriately, amplified, and AGC'd in the MIC AMP circuitry; the MIC AMP output goes to the Lower Loop to be transmitted and to the 10.6 IF board for sidetone.

## 2.7 POWER SUPPLY (A17) (See Figure 11)

The function of the Power Supply module is to generate the voltages required by the radio. The source of power is from either the battery pack in the AN/PSC-3 manpack configuration, or the Control Converter (formerly called NCS Applique) in the vehicular or equipment rack configurations of the

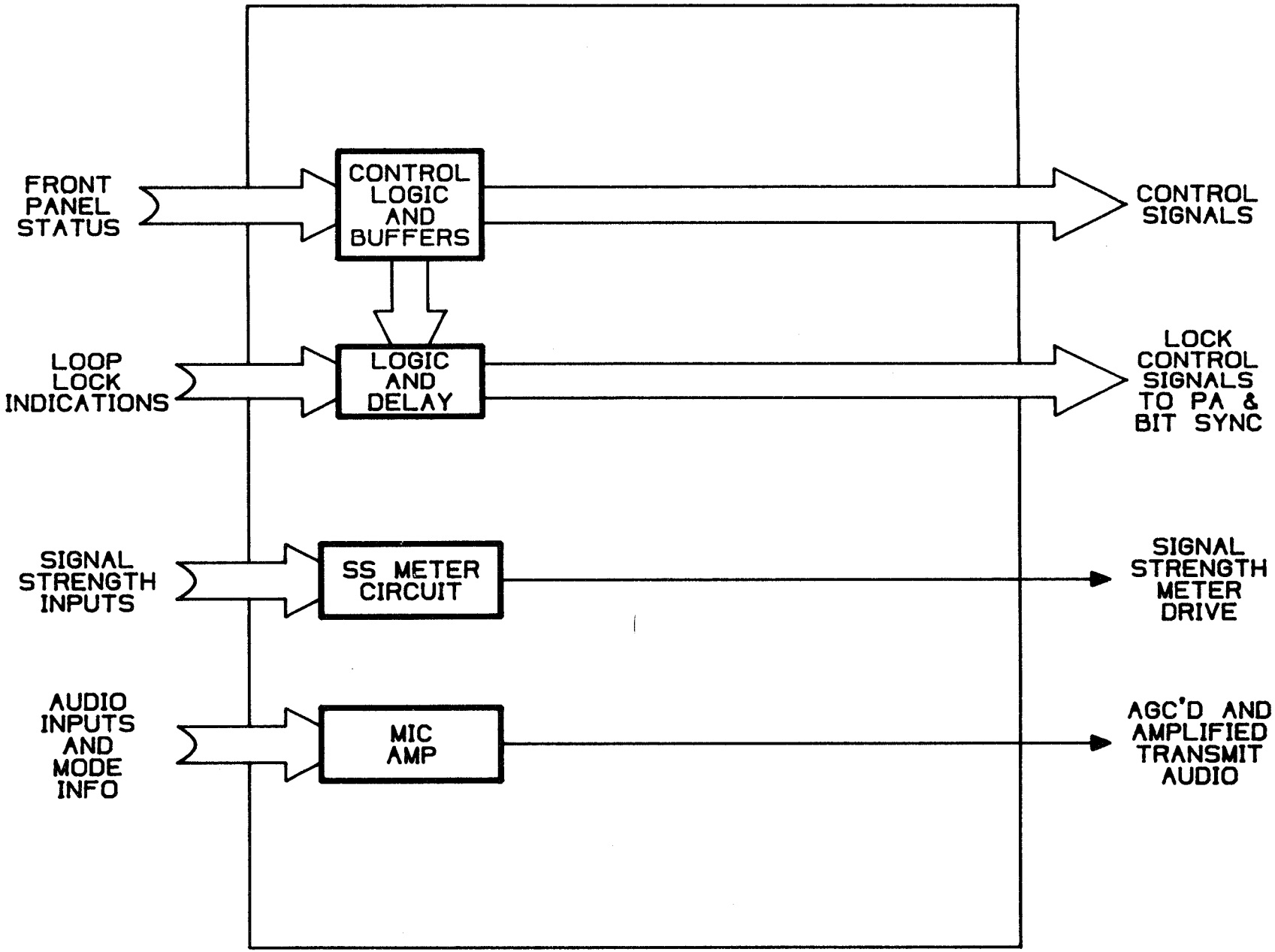


Figure 10. Baseband Processing and Control

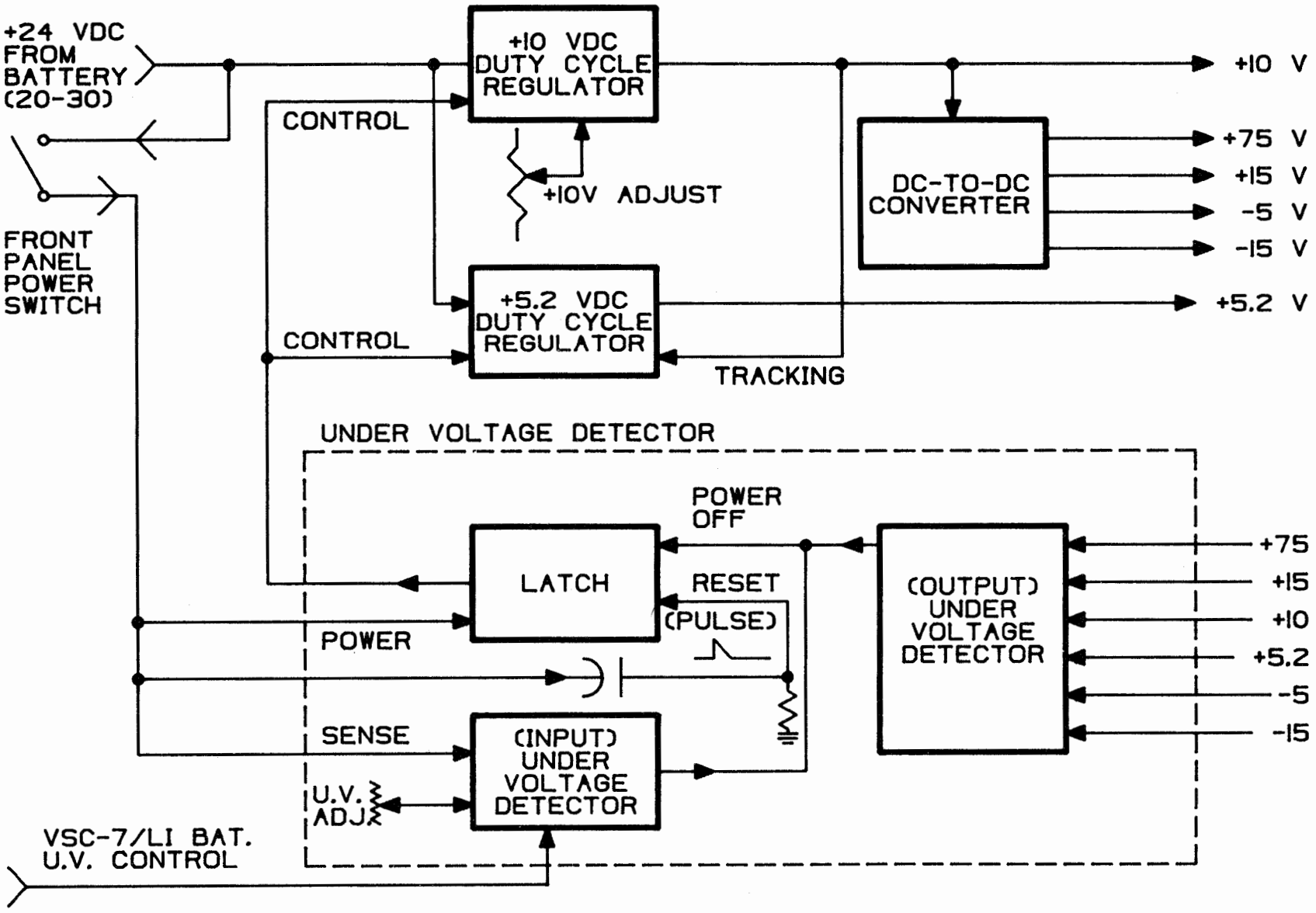


Figure 11. (A17) Power Supply

AN/VSC-7. Voltage regulation is required to stabilize the outputs over the supply voltage range from 20 to 32 Vdc. Protection circuits prevent destruction of the supply in the event of external overload.

Figure 11 is a block diagram of the Power Supply. The four major blocks are:

1. +10V Duty Cycle Regulator
2. +5V Duty Cycle Regulator
3. DC-to-DC converter
4. Under-voltage detector

The input voltage is connected directly to the +10V and +5V Duty Cycle Regulators; however, they will not produce any output until the control voltage is present. Power turn-on occurs when the front panel power switch is closed. The fast-rise voltage through a R-C circuit generates a pulse which resets the latch circuits in the Under-voltage Detector. This connects the input power line to the control inputs of the two regulators and operation starts.

The +10V Duty Cycle Regulator produces a well regulated +10 volts DC with high efficiency. The output is used to power the radio as well as the Power Supply's DC-to-DC Converter. A potentiometer provides adjustment of the output voltage.

The +5.2V Duty Cycle Regulator powers the radio, including the front panel indicators. The output is controlled by two fixed resistors and uses the +10Volts as a reference. This results in the +5.2V output tracking the +10V output.

The DC-to-DC Converter is required to generate those voltages required by the radio which are negative with respect to ground and those which are higher than the input supply voltage. The outputs are +75V, +15V, -5V and -15V DC. Although the +15 could be obtained by direct series regulation of the input voltage, specified as 20 to 30 Vdc, in actual practice, the voltage can be less than 20 Vdc due to transients and ripple imported to the equipment.

The Under-voltage Detector has two main functions:

1. Protect the power supply from shorts on overloads which occur in the radio, and
2. Shut down the radio when the lithium batteries drop below 19V.

In one section of the Under-voltage Detector, all six of the output voltage lines are monitored by individual detectors. If any one of the six outputs is below the threshold, a turn-off command is sent to the Latch circuit which removes the control power to the +10V and +5V Duty Cycle Regulators. Because this is a latching circuit, removal of a short or overload will not result in automatic restoration of power. Rather, a recycling procedure must be followed of turning OFF the front panel power switch, clear the problem if required, wait 1 or 2 seconds, then turn the power switch to ON.

The other part of the Under-voltage Detector senses the input voltage. When the input voltage falls below the threshold, a turn-off command is sent to the latch which turns off the supply. As with the output voltage detector, the supply is turned off and will not resume operation when the voltage is increased. Only by increasing the voltage and recycling the front panel power switch will operation resume. A time delay is incorporated so that

the voltage must remain below the threshold for a minimum of .15 seconds for shutdown to occur. Two different threshold voltages are establisheed by the VSC-7/LI BAT U. V. control line. In a manpack configuration where operation is from the attached battery pack, LI BAT, operation must be terminated when the lithium battery's terminal voltage drops below 19 Vdc. Because of a reverse voltage protection diode in series with the input power lead, the power supply's input U.V. detector is adjusted for 18.5V DC. Latching action is required because when the load is removed from the battery, the terminal voltage has been observed to return to near normal. Non-latching detectors result in power cycling.

In the AN/VSC-7 vehicular/rack configuration, the input voltage can go lower and outputs will be maintained down to 16 V, with shutdown by 10 V. No damage to the Power Supply has been observed at these lower input voltages.

## 2.8 POWER AMPLIFIER (A1) (See Figure 12)

The Power Amplifier module consists of two boards connected by standoff spacers, the Radio Frequency Amplifier and the Coupler and Control. The module bolts directly to the left inside of the R/T case, allowing the case to act as a heat sink for power dissipated in the amplifier. The RF Amp cannot be operated without the Coupler and Control - no electrical power connections are made directly to the RF AMP from the R/T.

The low-power driver stage is gain-controlled by a low current DC voltage source provided by the Coupler and Control. This ALC control is used to keep the output power constant into a low VSWR load and to reduce output power when the load VSWR is above 1.66:1 to protect the output transistors. The ALC signal is derived from a stripline dual directional coupler on the

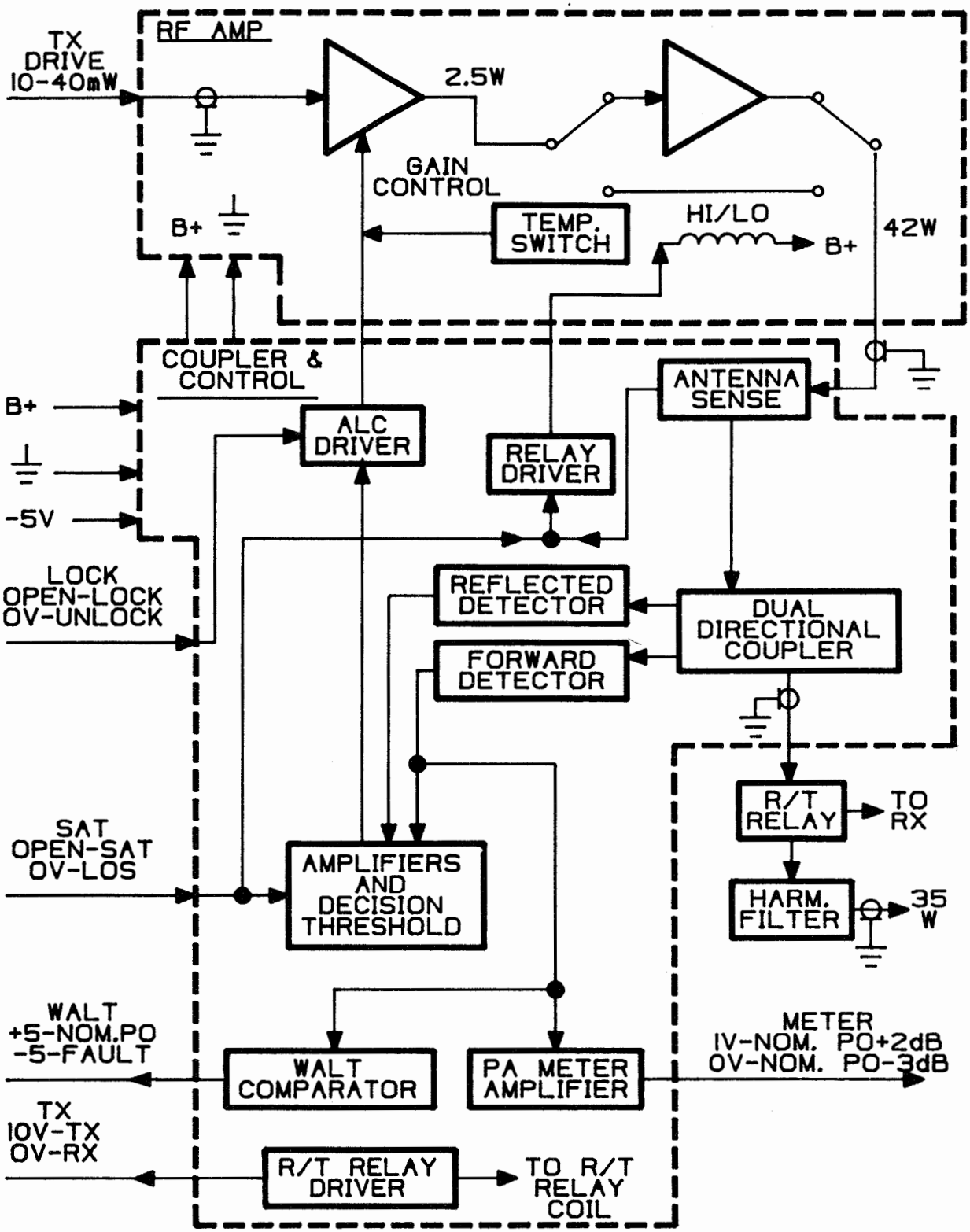


Figure 12. Power Amplifier

C&C board, which samples forward and reflected power. These samples are converted to DC voltages by detectors, then amplified and compared in a diode decision threshold circuit. During low VSWR conditions, the forward feedback loop controls the ALC voltage, forcing the detector voltage, and thus output power, to a predetermined reference. The reflected loop controls the ALC voltage when the reflected power becomes excessive.

The forward power sample is also used to drive metering functions to provide the operator with information concerning power output. A linear output is used to drive the front panel meter, with nominal power output indicating approximately center scale. A single-bit digital output gates the operator handset sidetone when power output falls below nominal power minus 5 dB.

The push-to-talk sequence is designed to minimize the delay between the operator PTT and appearance of transmitted signal. The TX signal arrives first, which allows the C&C to ready the internal regulator, R/T relay, and HI/LO power relay, if low-power mode is selected.

The synthesizer requires the longest duration to stabilize after operator PTT. When it does, the Lock signal arrives at the PA and releases its control on the ALC line. The full power output is then achieved in about 1 millisecond. The amplifier temperature-sensing switch also acts upon the ALC driver to shut down the RF Amp if a temperature of over 100°C is reached at the final output transistor mounting flanges.

The decision to transmit in satellite (high) or line-of-sight (low) power mode is made by the operator. The SAT signal is generated by the BBPC module and is sent to the PA. The SAT line command for high power may be overriden by the PA if the whip antenna is in use. The coupler and control

senses the DC resistance of the antenna, and if it is over about 10K ohms, will prohibit high power operation. This scheme protects the operator from a potential safety hazard of transmitting high power with the whip antenna very close to his body. The medium and high gain antennas have a few ohms of DC resistance, and are normally operated at a safe distance from the operator.

SECTION III

## 3.0 2400 BPS (ECP-1)

Carrier Recovery - Acquisition difficulties were encountered at 2400 bps due to the carrier-recovery loop locking-up onto data sidebands. The addition of a 100 millisecond preamble eliminated this problem. The AN/WSC-3 preamble of an unshaped one, one, zero, zero pattern appears to cause no acquisition problem.

A one-zero pattern at 2400 bps yields sidebands 1200 Hz above and below the center frequency. The carrier-recovery loop can lock to these sidebands. The problem is aggravated by a frequency offset which can make a data sideband appear closer to 0 Hz offset than the actual center-frequency of the received signal. To avoid problems with locking on sidebands, the AN/PSC-3 transmits a 100 millisecond carrier-only preamble. This preamble allows the receiving AN/PSC-3 radio to lock to the proper frequency, then when data appears, the carrier-recovery loop stays locked regardless of the data pattern.

The AN/WSC-3 does not transmit a carrier-only preamble, but instead transmits a one, one, zero, zero pattern with no shaping. The closest sideband spurs for this pattern are plus and minus 600 Hz. If the loop is at one of the 600 Hz removed sidebands, the main carrier is close enough in frequency for the baseband discriminator in the carrier-recovery loop to pull away toward the main carrier.

Circuitry was added to the carrier recovery system for 2400 bps acquisition and data-recovery time constants.

Modulator - In order to keep 94 percent of the transmitted energy in a 5 kHz channel at 2400 bps, shaping for BPSK is required. We use 50 percent shaping which yields approximately 95% of the energy in the channel. Since data shaping puts energy in the Q channel, and transmitted power remains the same, a degradation occurs in BER and acquisition performance. For 50 percent shaped BPSK, this degradation is equivalent to about 1.66 dB.

Shaping is accomplished at baseband in the Modulator module. Mode selection circuitry in the Modulator module was changed to accommodate 2400 bps.

Bit Sync - Incorporating 2400 bps operation in the Bit Sync required modifications in divider circuitry mainly, since the time constants change with clock rate automatically.

Performance at 2400 bps (tested at module level) -

C/KT = 42.1 dB

Acq. time = 70 milliseconds

$10^{-3}$ BER @ 42.3 dB C/KT