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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The AN/PSC-3 Program is progressing with small deviations from the proposed tech approach. The areas of deviation are in the MODEM and synthesizer.

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SECTION I

1.0 INTRODUCTION

This report describes the technical efforts during the third quarter of the AN/PSC-3 and AN/VSC-7 Production Program. The lead in engineering to production is progressing with minor deviations from the proposed approach. Again, only the areas of deviation are discussed in detail in Section 2.0. In the areas unchanged from the proposed approach, the proposal is to be used as the reference. Areas unchanged since the proposal and last quarterly report include RT Power Supply, PA, Call Decode Logic, Carrier Recovery, Bit Sync/ Data Recovery, NCS Power Supply and NCS Power Conditioning.

SECTION II

2.0 TECHNICAL DETAILS

2.1 SIGNAL PATH

All AGC detection is now performed by the wideband signal-strength and squelch detector in the 10.6 MHz IF Module. Previously, AGC detection in PSK data modes was to be performed by the Carrier Recovery #2 module. However, that included the AGC time-constant within the Costas' Loop, which increased the acquisition time. Additionally, module interchangeability is enhanced since no adjustments are required to set interface levels.

2.2 SYNTHESIZER

Figure 1 is a block diagram of the proposed AN/PSC-3 synthesizer. Changes to the proposed synthesizer and status of the various modules comprising the system are as follows:

Reference - Minor changes to several component values.

Lower Loop - Minor changes anticipated to suppress spurious outputs caused by the 4 MHz Reference and the nominal 2 MHz output of the ÷ 40/41 prescaler. These spurious outputs appear on the Lower Loop output in transmit mode only.

VCO - The use of fiberglass-epoxy PWB material, necessitated by the requirement of reliable plated-through holes, has added additional parasitic capacitance to the frequency-determining tank circuit. This added capacity, and

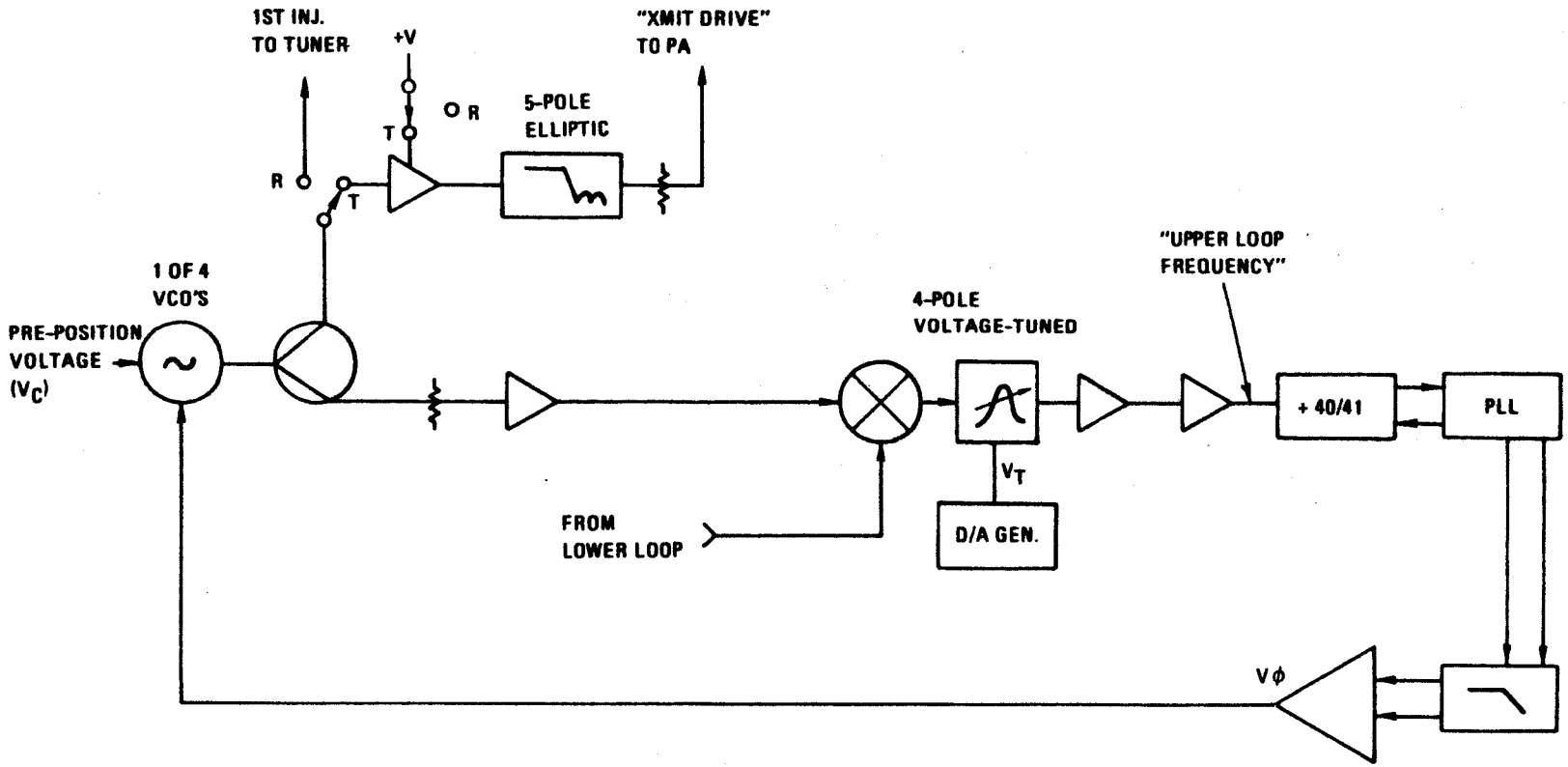

Figure 1. AN/PSC-3 Proposed Synthesizer

the stray inductance contributed by mica coupling capacitors, restricts the tuning range of the oscillators. The PWB is currently undergoing a re-layout for the removal of ground-plane, and to utilize chip capacitors for a reduction of stray lead inductance.

The amplifier driving the elliptic-function low-pass filter will be removed due to a change in the method of transmit-frequency generation. (See below).

Upper Loop - The transmit-frequency generation method is now Alternative #2 (See Quarterly Report for April 1982, TR-820008, pages 8 and 10 and Figure 3). Alternative #1 was eliminated due to the limitations of the propagation time for the clock to modulus-control output of the synthesizer integrated-circuit. Alternative #3 was found to require excessive PWB area, and was dropped from consideration.

Figure 2 shows the transmit-frequency generation scheme currently underway. The amplifier eliminated from the VCO, between the power-splitter and the elliptic-function low-pass filter, is no longer required due to the small amount of drive needed by the ÷ 40/41 prescaler.

PWB's are on hand, and various subsystems of the Upper Loop module have been assembled and are currently under evaluation.

2.3 BASEBAND PROCESSING AND CONTROL (BBPC)

Several functions are implemented on the BBPC board. They are as follows:

Mic amp - Provides amplification and AGC of plain text, retransmit and KY65 X-Mode audio. Originally proposed to be a single integrated circuit, the mic amp is now a discrete parts design shown in Figure 3. The integrated circuit was not used because of its high power consumption.

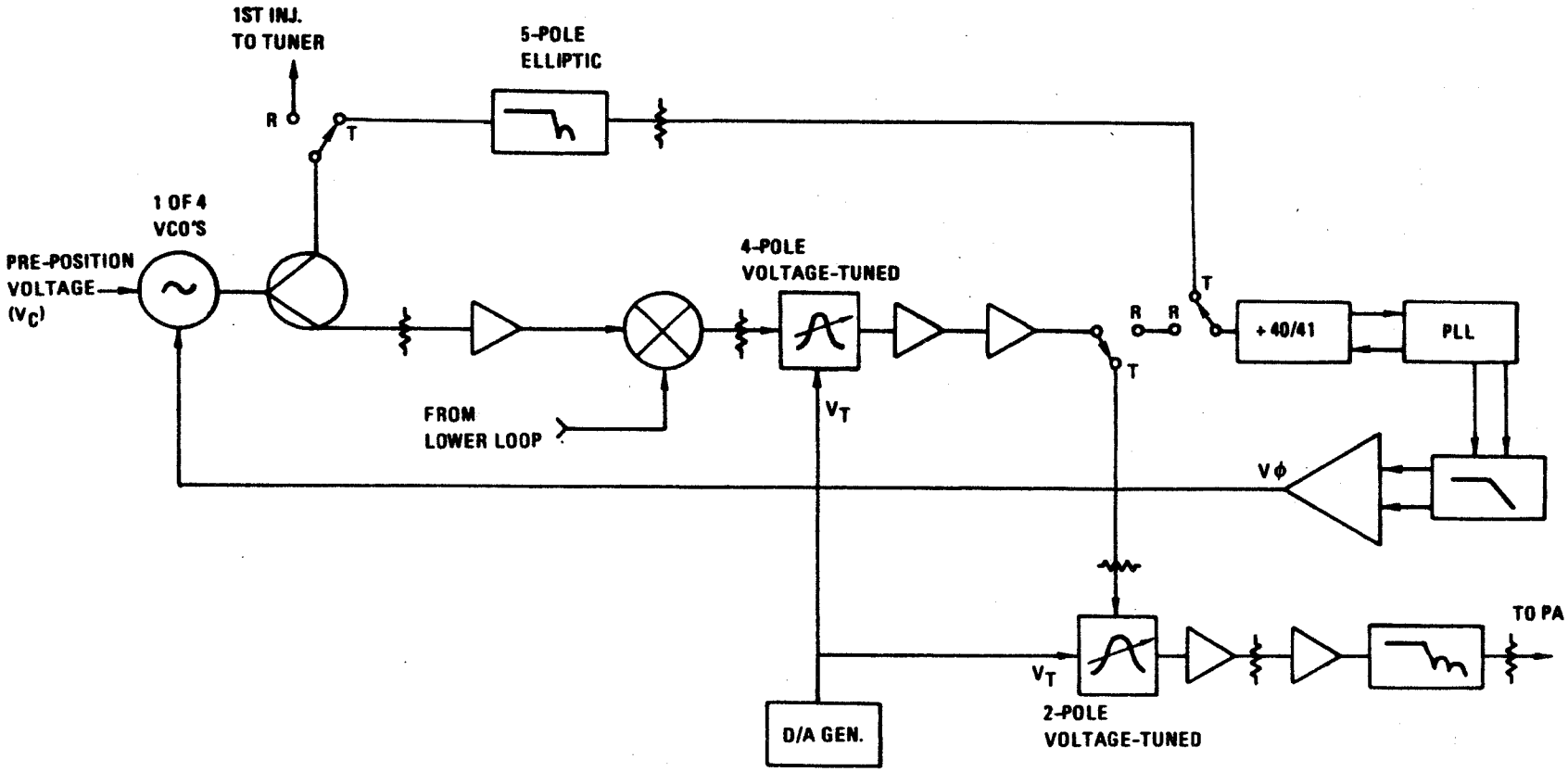

Figure 2. Mixing Generation of Modulated Transmit Signal

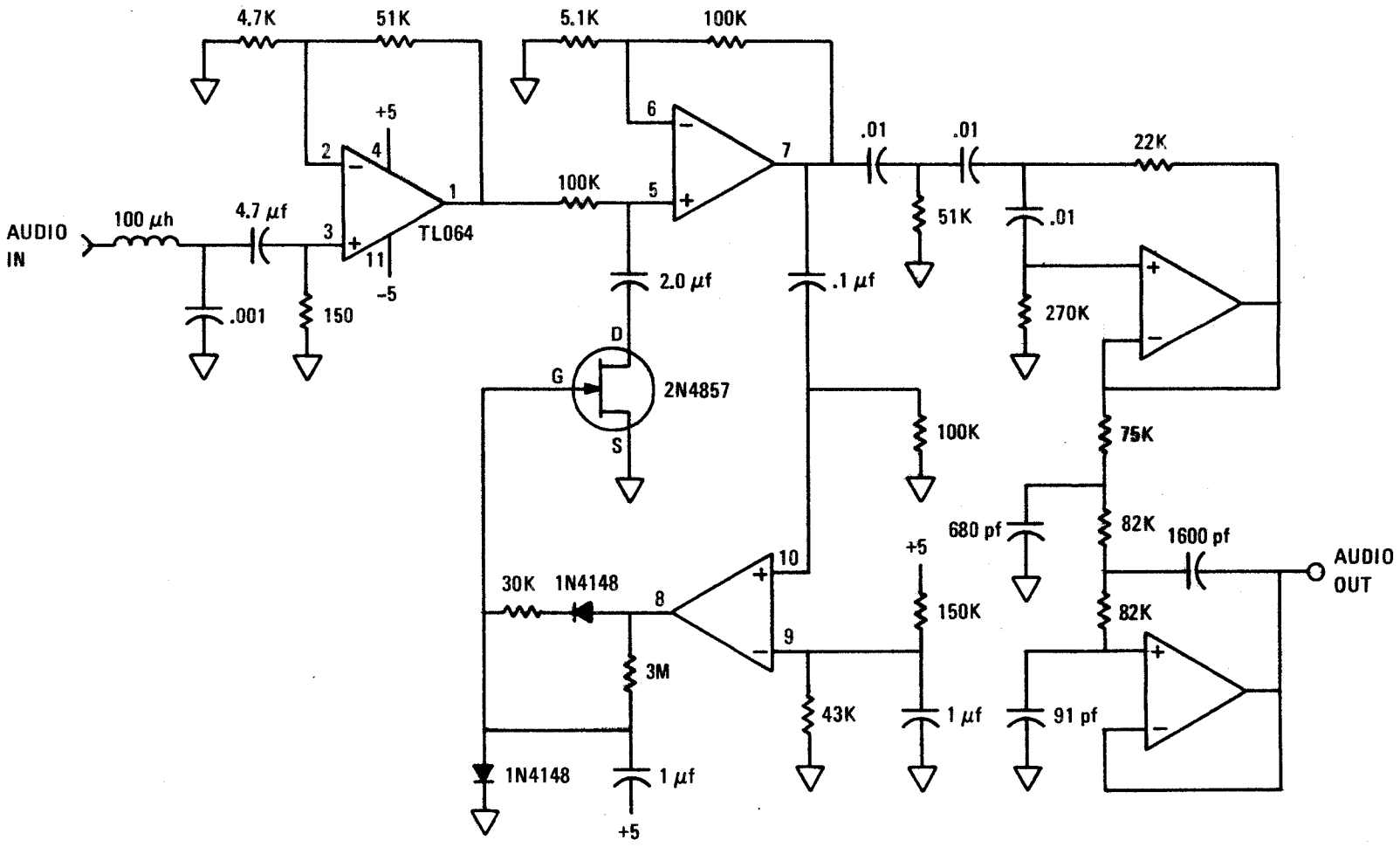

Figure 3. MIC-Amp

Level translators - Translates 5V CMOS logic levels from the CPU to + 5V CMOS levels used throughout the rest of the radio.

Signal strength meter interface - Switches and translates voltages from several sources to a 0 - 100 μA current to drive the signal strength meter.

Control circuitry - CMOS logic and timing circuitry which generates control signals for other areas of the radio.

2.4 TRANSMIT INTERFACES

Problems with the RT keying up at power turn on forced the digital interface to be changed to an unbalanced configuration (thresholds not symmetrical around signal ground). The 16 kbps cipher text data interface remains balanced. This circuitry is included on the Modulator board.

2.5 RECEIVE INTERFACES

All receive interface circuitry is included on the 10.6 IF board except the output clock interface which is included on the BIT SYNC #1 board. For the secure voice mode, receive interfacing consists of 0.74 VRMS to the audio connector, rather than 220 mv RMS to the X-Mode connector as initially stated in the proposal. This change was made to simplify the receive-interfaces and associated cables.