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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The AN/PSC-3 Program is progressing with small deviations from the technical approach discussed in Cincinnati Electronics Proposal of 20 April 1981. The most significant areas of deviation are in the areas of the Modem Design and Mechanical Design of the RT Unit.

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1.0 INTRODUCTION

This report covers the technical effort during the first quarter of the AN/PSC-3 and AN/VSC-7 production program. The development of the AN/PSC-3 and AN/VSC-7 is progressing with only minor deviations from the approach detailed in Cincinnati Electronics proposal of 20 April 1981. The areas of deviation are discussed in detail in Section 2. In the technical areas unchanged from the proposed approach, the proposal should be used as the reference. As other technical changes to the proposed approach are incorporated into the design of systems, the Quarterly Technical Reports will update the proposed technical approach and provide data to support the selected approach. Areas unchanged since the proposal (and therefore not discussed herein) include Power Amplifier, Harmonic Filter, Synthesizer, and Power Supply of the R/T as well as ancillary items of antennas and carrying harness.

2.0 TECHNICAL DETAILS

2.1 MODEM

The modem section of the radio includes the functions of carrier recovery, bit synchronization, data detection, call message detection, and interfacing.

2.1.1 Call Decoder Logic

The Call decoder logic circuitry has been designed and breadboarded. Two differences exist between the proposed Call decoder and that designed (see Figure 2-1).

First, the present Call decode scheme allows random noise to be present between the detection of two identical valid call messages. If, however, a valid message has been detected and the next message detected is not identical to the first, the system will be reset. This differs from the proposed approach which states that after detection of one valid message another identical message must be detected after 42 bits for a Call indication to be made. This scheme increases the probability of detecing a Call message when one is present while the probability of activating the Call indication when no call is being made still remains insignificant.

Second, the visual indicators are reset when the operator moves the Call switch to the reset position or the R/T is cycled OFF and ON as proposed. In addition the indicators are reset when the operator moves the mode switch to any position other than Call.

The indicator driver circuitry has been designed but not yet breadboarded since a choice of indicators has not yet been made. Selection of the indicators will depend primarily upon mechanical layout considerations.

A test procedure is presently being written and testing is in progress. Testing to date has included insertion of a repeated data sequence consisting of 6 words of 7 bits/word (framing, polarity and 4 valid Barker words pertaining to a conference Call) interspersed with a pseudo-random binary sequence of $2^{20} - 1$ bits after every odd word into the Call decoder at 1000 times the proposed rate of 300 bps. After 5 hours at this rate (equivalent to 5000 hours at 300 bps) no take Call indication had occurred.

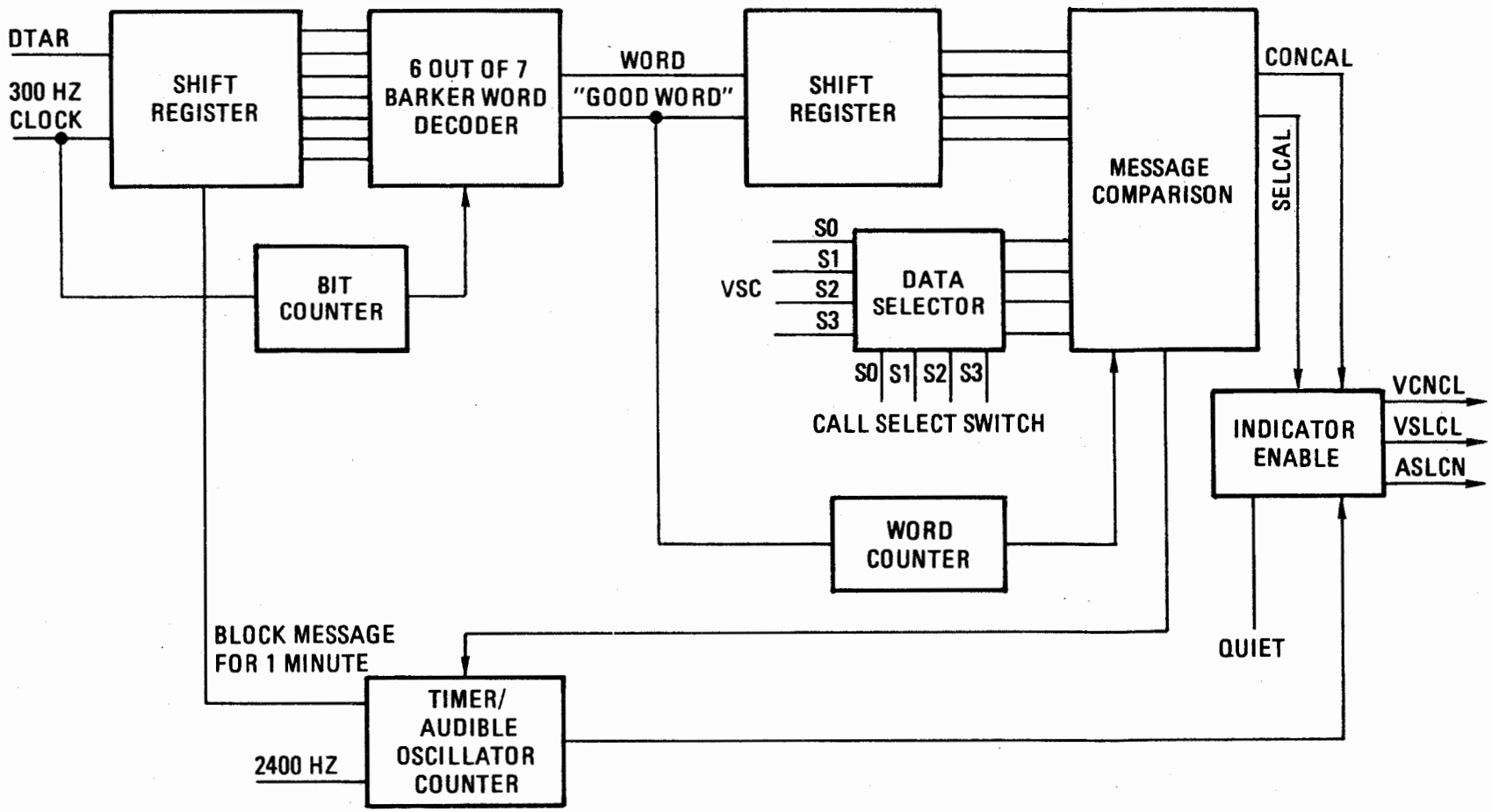

Figure 2-1. Call Decoder, Block Diagram

The preamble and CALL transmission sequences are being generated by the front panel microprocessor. The software is presently being written for this generation as part of the front panel design.

2.1.2 Bit Sync/Data Detector

The Bit Sync/Data Detector design shown in the block diagram, Figure 2-2, was developed by Cincinnati Electronics on an IRAD program. This design was incorporated in Cincinnati Electronics secure multichannel system. The circuit used in multichannel system has undergone minor changes to make the circuit more universal. Cincinnati Electronics is presently in the process of incorporating the Bit Sync circuitry into a semi-custom CMOS gate array for use in other Cincinnati Electronics designs or for sale as a component. This effort is being funded under an IRAD program. The semi-custom CMOS circuit will be packaged in a 40-pin, side-brazed, ceramic dual inline package. The use of this semi-custom MSI will significantly reduce the parts count of the Bit Sync/Data Detector circuitry and enhance the reliability of the AN/PSC-3.

The results of a BER Test using the Bit Sync/Data Detector breadboard are shown in Figure 2-3.

2.1.3 Carrier Recovery

Work is proceeding satisfactorily in the carrier recovery area. The design effort is estimated to be 30% complete. The main areas of concentration have been system signal flow, Costas loop implementation, and acquisition. In addition to hardware design and bench testing, a parallel computer simulation of the carrier recovery loop has been used to evaluate various configurations.

2.1.3.1 Acquisition

The technical proposal indicated that frequency sweeping would be used to aid loop acquisition, as was done in the AN/PSC-1. We have searched for alternative assist strategies for two reasons. First, we wish to have WSC-3 compatibility. The WSC-3 does not transmit a carrier only preamble in the PSK modes, as did the AN/PSC-1. Instead, an alternating 1-0 pattern is transmitted, generating discrete spectral lines at multiples of one half the data rate. Since at 300 and 1200 bps the spectral lines are within the ± 700 Hz frequency uncertainty window, it is necessary to distinguish false locks on sidebands from the correct lock point during sweeping. (In fact, a Costas loop will false lock at any multiple of 1/2 the data rate irregardless of the data pattern.) While the phase detector error characteristic

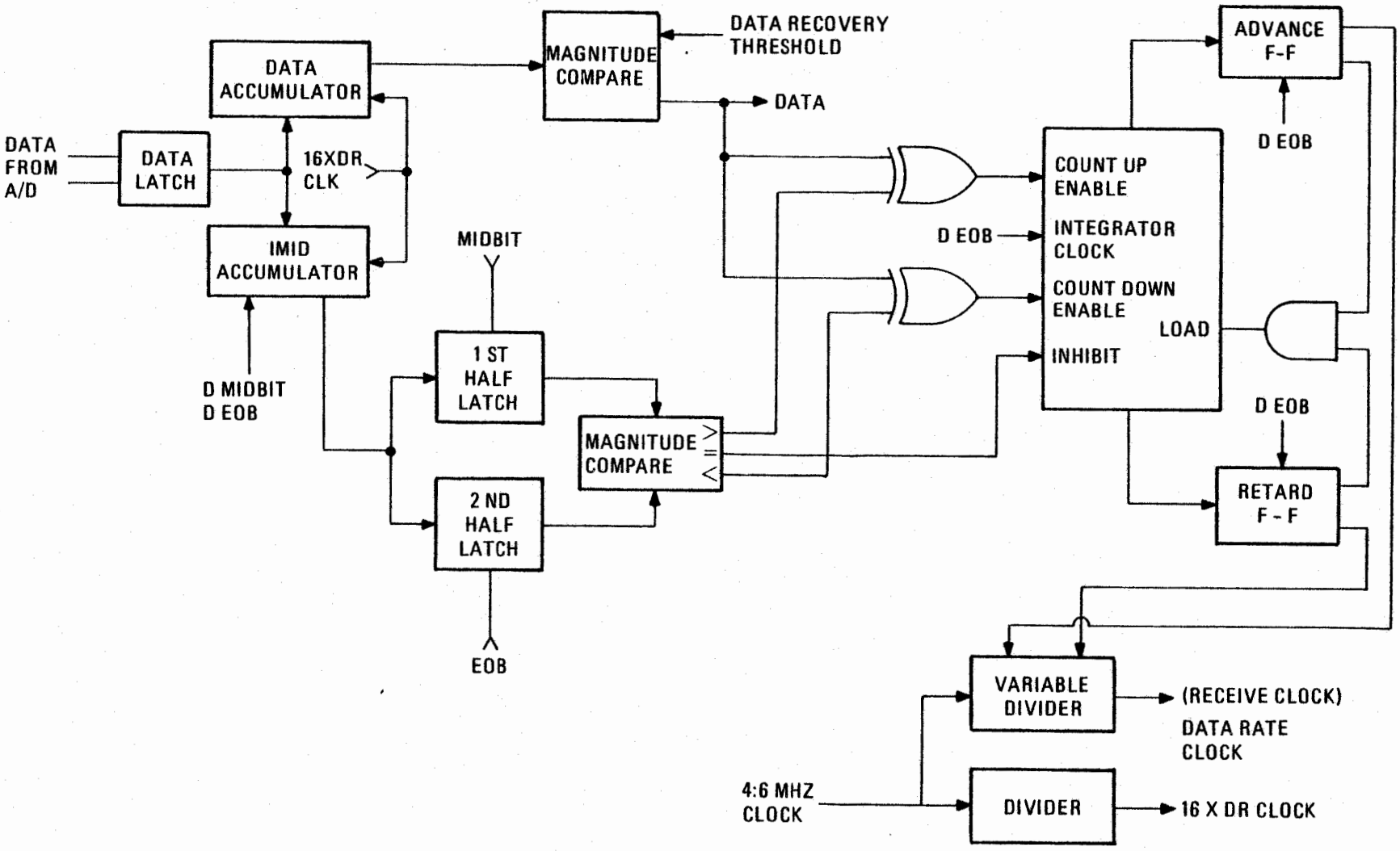

Figure 2-2. BIT Sync, Block Diagram

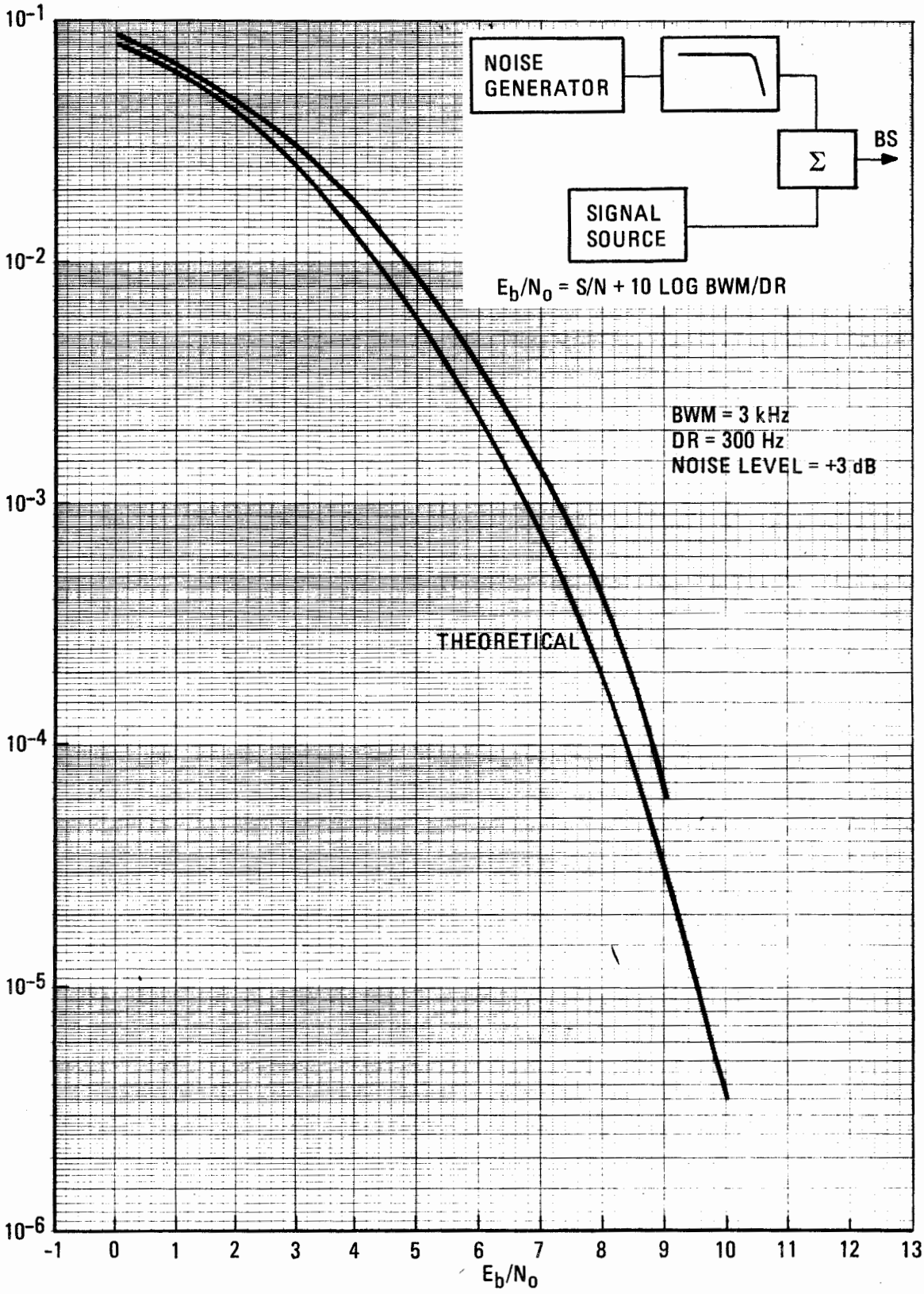

Figure 2-3. BER Performance for Baseband (Sheet 1 of 2)

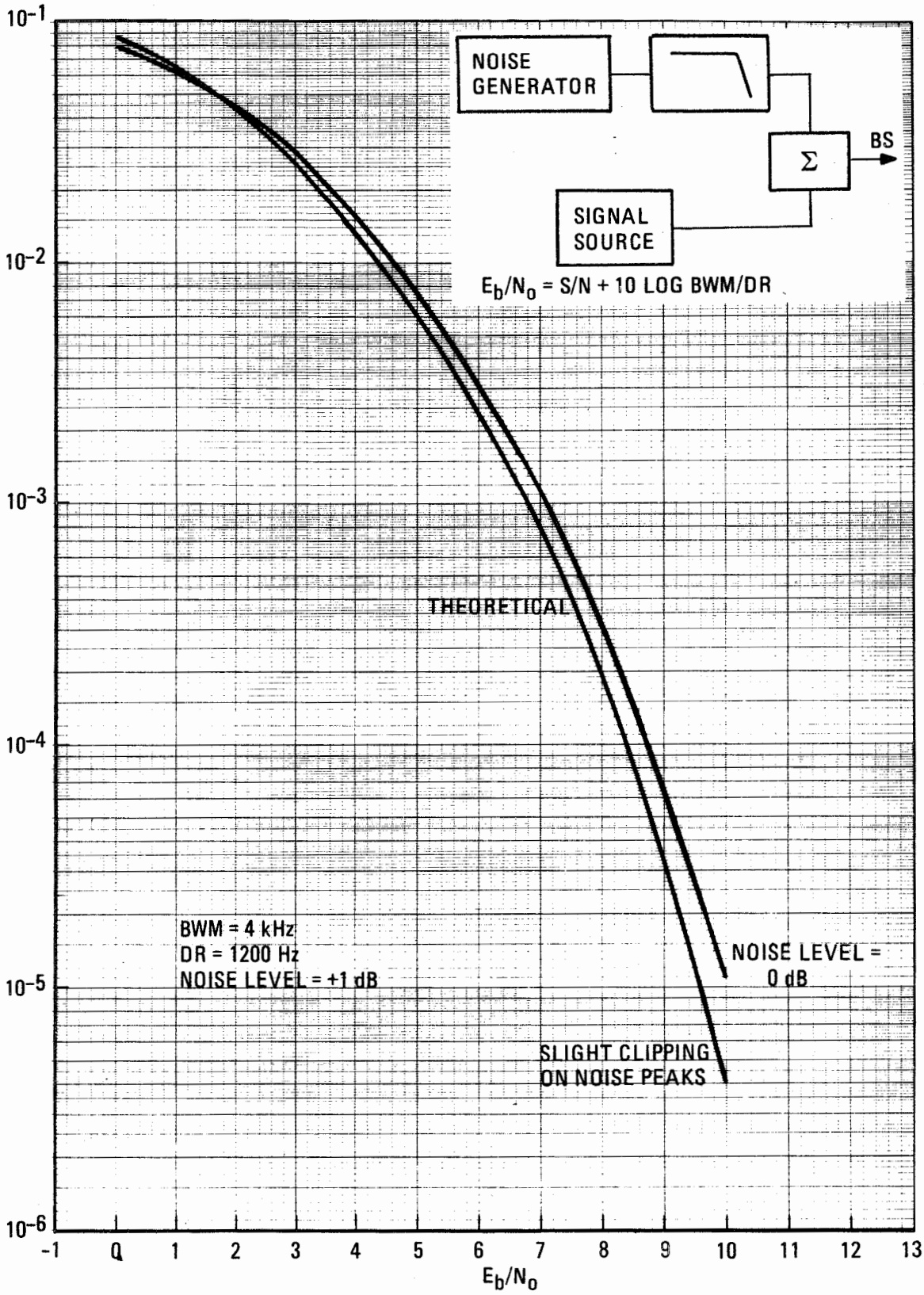

Figure 2-3. BER Performance for Baseband (Sheet 2 of 2)

is degraded at the false lock points through lower loop gain, there is sufficient energy to stabilize (false lock) the loop, especially for strong signals. Therefore, it is necessary for a swept frequency system to reject data sidebands when encountered and proceed to the correct carrier frequency. It is possible to build a lock detector which can identify a sideband false lock, but this is much more difficult than the alternative method discussed below.

A second reason to find an alternate to swept acquisition is that experience during the AN/PSC-1 program demonstrated the difficulties with a swept acquisition, the primary one being recognition of phase lock before the sweep has carried the VCO past the signal. This has been a difficult problem requiring critical bench adjustment of various parameters by trained personnel for each radio.

The above considerations have led us to consider discriminator aided acquisition as an alternative to swept acquisition. Figure 2-4 shows a block diagram of such a loop. In addition to the phase detector, a frequency detector of some sort is necessary. The output of the frequency detector drives the VCO to approximately the correct frequency, where the phase detector takes over and completes acquisition. The bandwidth of the frequency locked loop is chosen to be less than the bandwidth of the phase locked loop so that the main contribution to the VCO phase error is jitter of the phase loop rather than the frequency loop. Alternatively, we may disable the frequency control loop after acquisition has been detected. The discriminator aided loop provides not only the best acquisition time for a given loop bandwidth, but it is also effective for countering the Costas false lock phenomenon. This is so because the frequency detector responds to the centroid of the input spectrum and will therefore generate an error signal at the false lockpoints mentioned earlier.

Because of the threshold effect, a standard discriminator is not suitable as the frequency detection element. At 29.1 dB C/KT, the specified level for CALL performance, the IF SNR is -5.7 dB (assuming a 3 kHz IF BW), well below the threshold of a conventional discriminator. A type of discriminator which does not exhibit a threshold was first proposed by Richman[1] in 1954 for color phase synchronization in television receivers, called the "quadri-correlator". We are examining a variation of this detector, shown in Figure 2-5. Some simple trigonometry will show that the inputs to the multipliers of both versions exhibit a differential phase shift proportional to the frequency of the beat note at the quadrature mixer ports. The original version of

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[1]Color - Carrier Reference Phase Synchronization Accuracy in NTSC Color Television, Donald Richmond Proceeding of IRE, January 1954, pgs. 106 - 133.

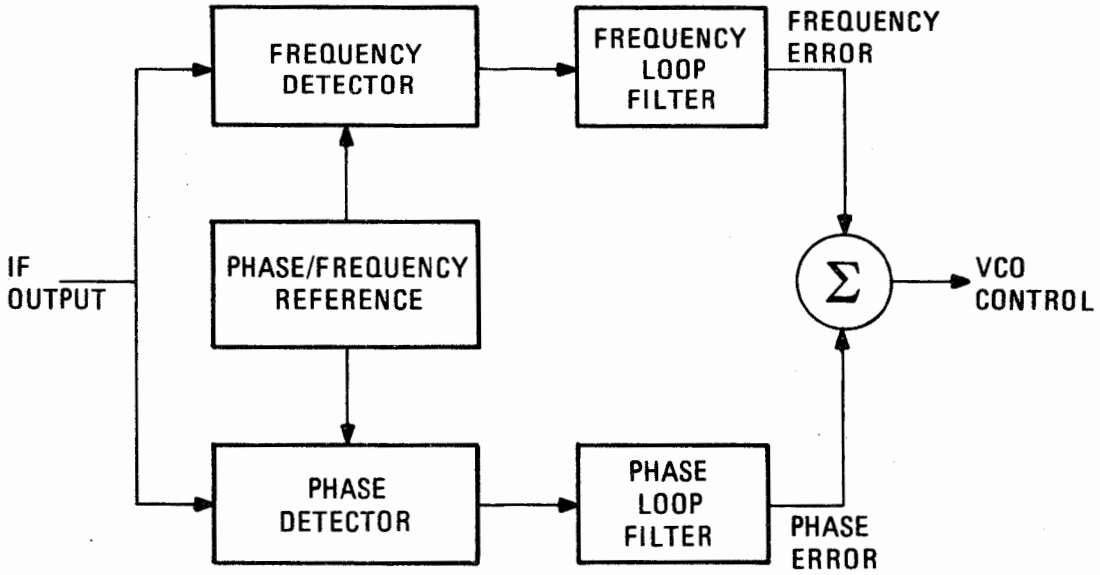
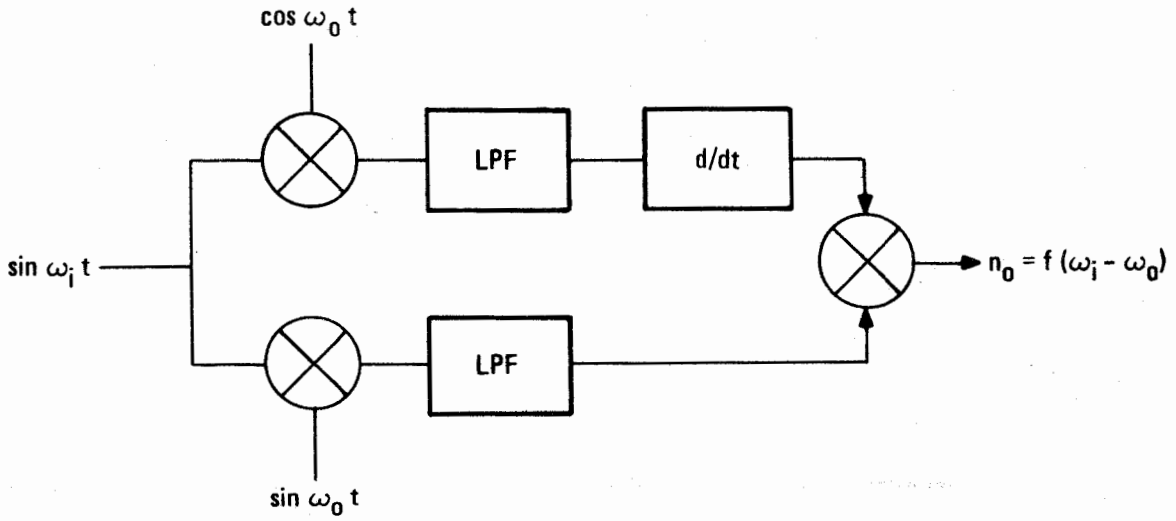
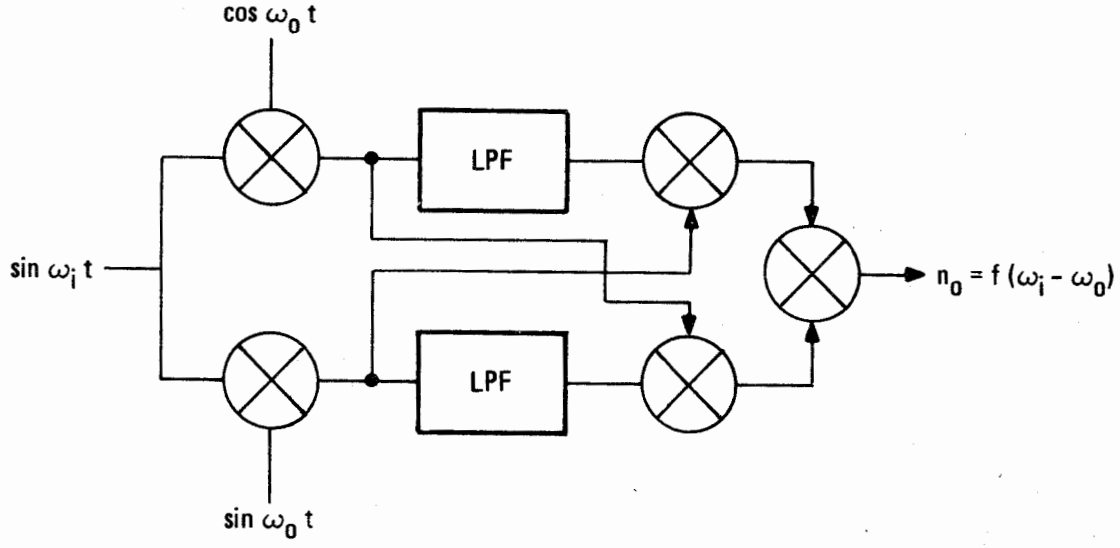


Figure 2-4. Discriminator Aided Loop, Block Diagram



ORIGINAL 'QUADRICORRELLATOR'



MODIFIED 'QUADRICORRELLATOR'

Figure 2-5. Quadricorrelator Variation

this detector incorporates a differentiator and is undesirable at low SNR's because it enhances the higher frequency noise components. The modified version retains the essential property (a relative phase shift or time delay) without the use of a differentiator. A computer simulation of this detector showed very good performance for very low SNR's. We are currently breadboarding this system to experimentally verify its performance. Thus far the results indicate good false lock rejection and reliable lock detection at moderate to high SNR's (> 0 dB).

The primary unresolved difficulty is related to the fact that the frequency detector output is proportional to the centroid of the input spectrum. While beneficial in discriminating against false locks, this action can create lock up difficulties. At very low IF SNR's, as long as the VCO is centered within the translated IF filter bandwidth, the frequency detector is reliable, but the accuracy is degraded as the VCO deviates from the IF center frequency since the frequency detector begins to respond to the centroid of the noise, rather than the signal. This effect is still under study. There appear to be basically two alternatives. First, we may place the IF filters within the loop, which centers the VCO automatically. Second, with a combination of increased baseband filtering and moderately increased IF bandwidth, we may be able to keep the frequency detector from "seeing" the skirts of the IF filter. Both these approaches are currently under investigation.

It is important to note that the quadrature detectors employed by the frequency detector are already available as the phase detector of the Costas loop. Therefore, implementation of the discriminator aided loop is relatively simple and will result in a net loss of components relative to frequency sweeping.

2.1.3.2 Phase Detector

Figure 2-6 shows a simplified schematic of the phase detector currently under consideration for the AN/PSC-3. The design incorporated by the AN/PSC-1 used conventional quad, diode double balanced mixers with a 90°, 3 dB hybrid power splitter. The proposed design is essentially a single balanced design, suppressing the LO energy but not the RF. The switching elements are conventional CMOS analog gates (CD4066) rather than diodes, as are used in a conventional mixer. The quadrature signals for the switches are derived digitally from a simple 4 state Johnson counter driven by the 4 MHz TCXO. This design can be used at a 1 MHz final IF frequency, but the CMOS parts will not operate reliably at the 6.6 MHz IF frequency used by the PSC-1. This is a minor change to the system signal path design and is discussed further in paragraph 2.2. The advantages of the design are large dynamic range, low DC offset, and accurate stable 90° phase

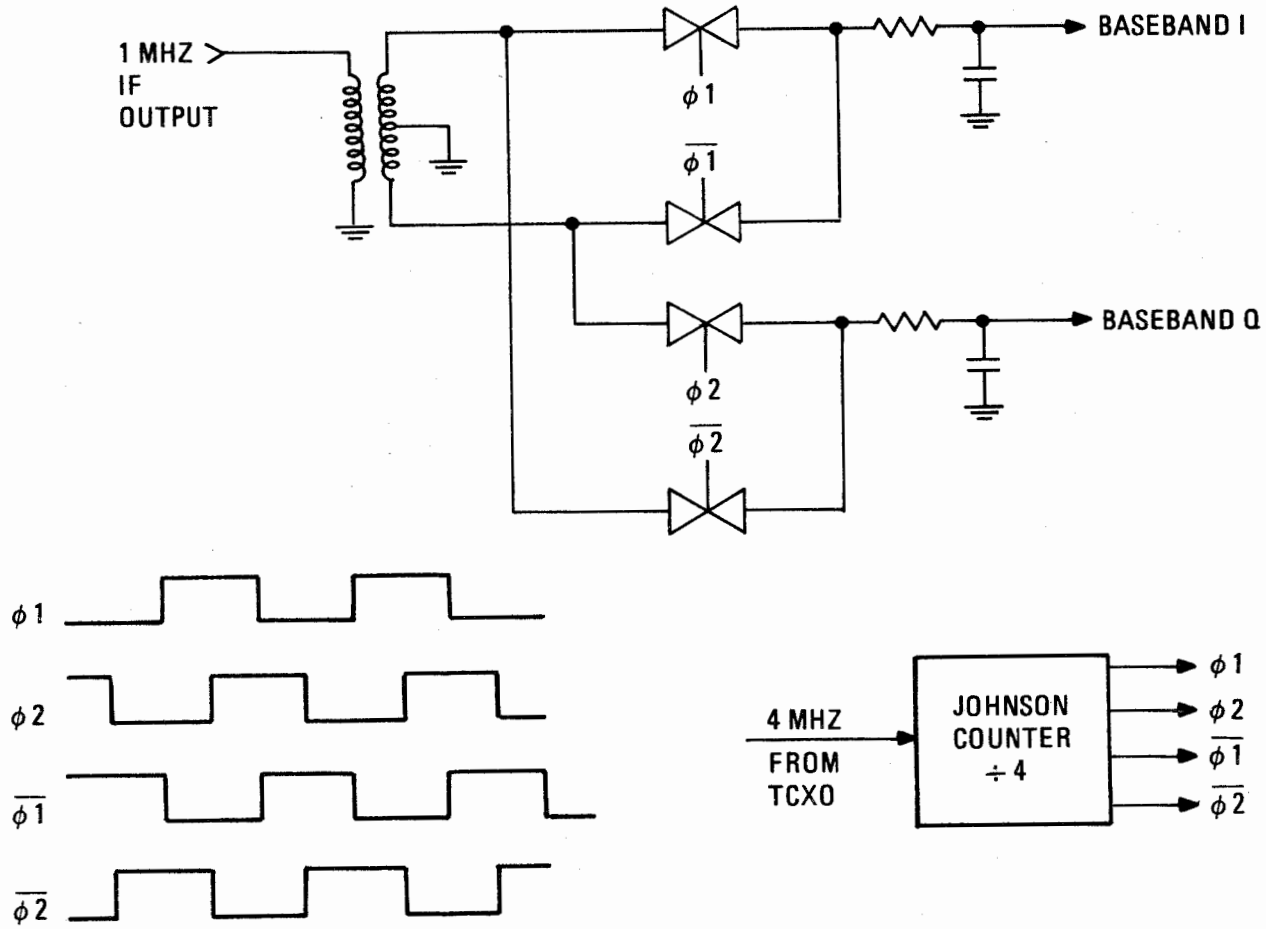


Figure 2-6. Phase Detector, Simplified Schematics

shifts. The brassboard exhibits a maximum offset of approximately 2 mV DC, a 10 VP-P maximum linear range, and less than 1° phase error. Additionally, this phase detector requires less PC board area and has a significantly lower parts cost.

2.1.3.3 Acquisition Simulation

Figures 2-7 and 2-8 show typical phase plane trajectories for a Costas loop with and without the frequency detector assistance. In Figure 2-7, which is without the discriminator function, the initial starting condition is a frequency and phase error of 130 Hz and 50° respectively, with a total time duration of about 0.5 second displayed on the plot. The loop parameters are such as to yield satisfactory loop SNR for 300 data acquisition ($B_L \doteq 200$ Hz). Note the weak error force indicated by the closely spaced lines of consecutive cycles during the pullin process. Figure 2-8 is the same loop, but includes the frequency detection function. For this case, the frequency discriminator effect is obtained by unbalancing the I and Q arm post-detection filters. We have since completely separated the frequency loop from the phase loop to provide more independent adjustment of loop parameters. Note that the widely spaced lines of successive cycles indicate a strong error force driving the loop towards lock. This loop locks from an initial frequency error of 1000 Hz in about 60 msec. Figure 2-9 shows a plot of VCXO control voltage versus time for this loop at 29.1 dB C/KT, no offset, while Figure 2-10 is a plot of the lock detector output. Note that phase lock occurs in about 1.4 seconds, and the lock indication is unambiguous. Figures 2-11 and 2-12 are plots of the same loop parameters for a 700 Hz frequency offset required by specification. For this case phase lock occurs at the end of the simulation at about 3.5 seconds. Again, the indication of phase lock is unambiguous.

2.2 SIGNAL PATH

Figure 2-13 shows a simplified block diagram of the PSC-3 signal path from the 69.4 MHz IF to the carrier recovery carrier loop phase detector. The AN/PSC-1 design involved an intermediate mix from 10.6 MHz to 6.6 MHz, the operating frequency of the loop phase detector. The LO input to the phase detector was derived from a 13.2 MHz VCXO. In the current design, the 10.6 MHz IF signal is directly converted to 1 MHz with an 11.6 MHz VCXO, with the phase detector now operating at 1 MHz. This design change enables us to use the digitally clocked 1 MHz phase detector with improved performance described in 2.1.3.2 and delete the parts associated with the 6.6 MHz IF and mix.

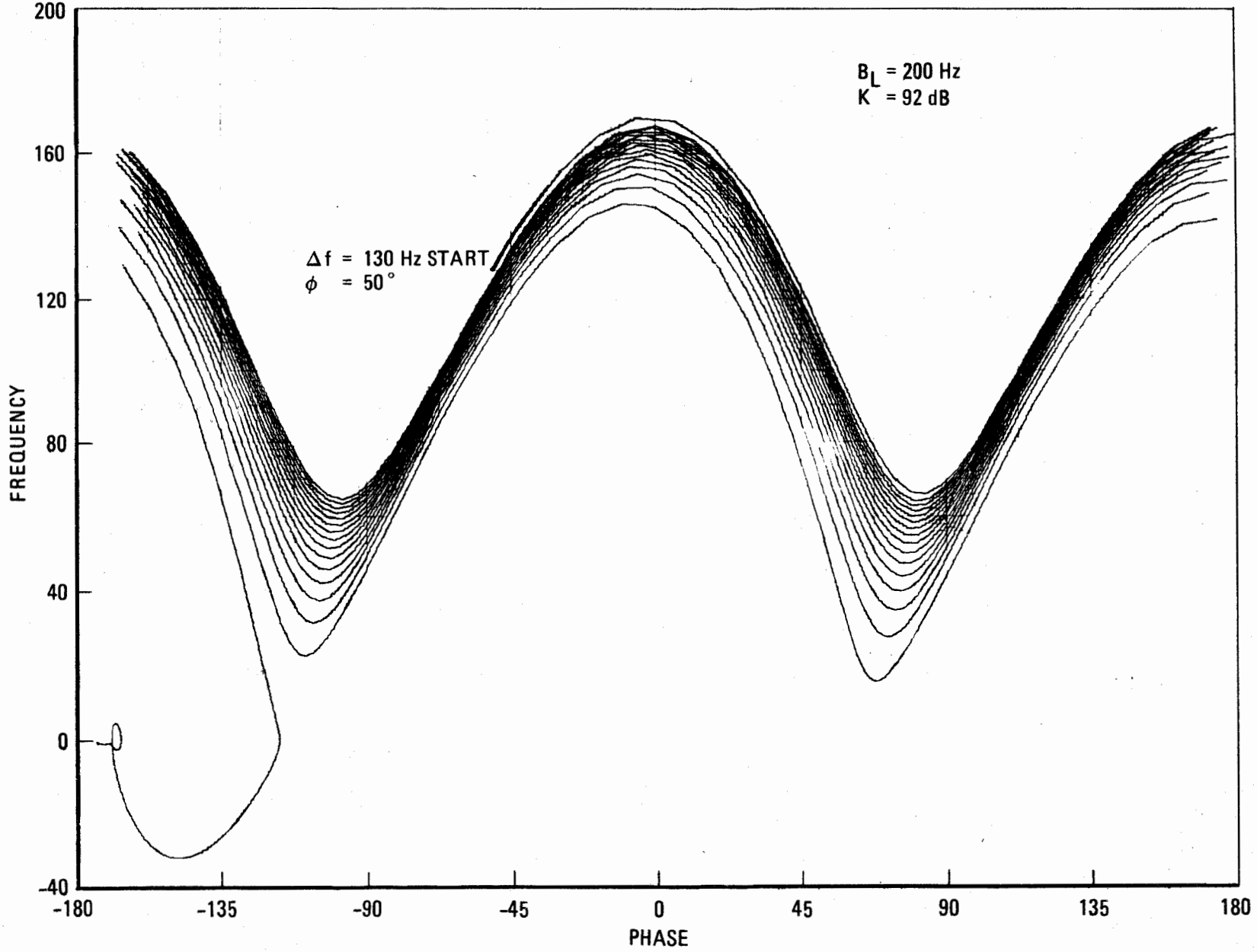


Figure 2-7. Phase Trajectory, No Frequency Detector Assist - Time 0.5 Sec.

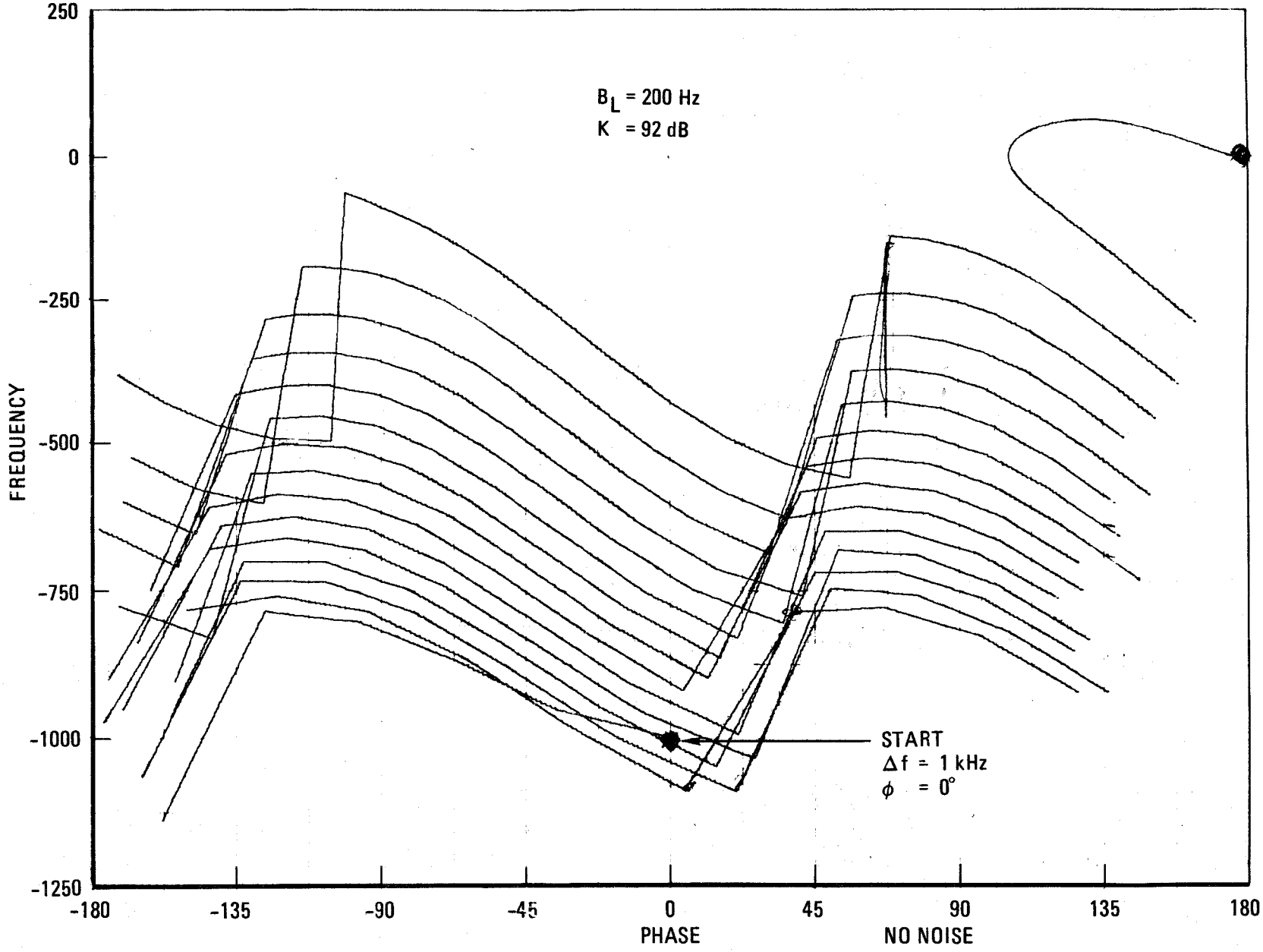


Figure 2-8. Phase Trajectory With Frequency Detector Assist - Time = 60 mSec.

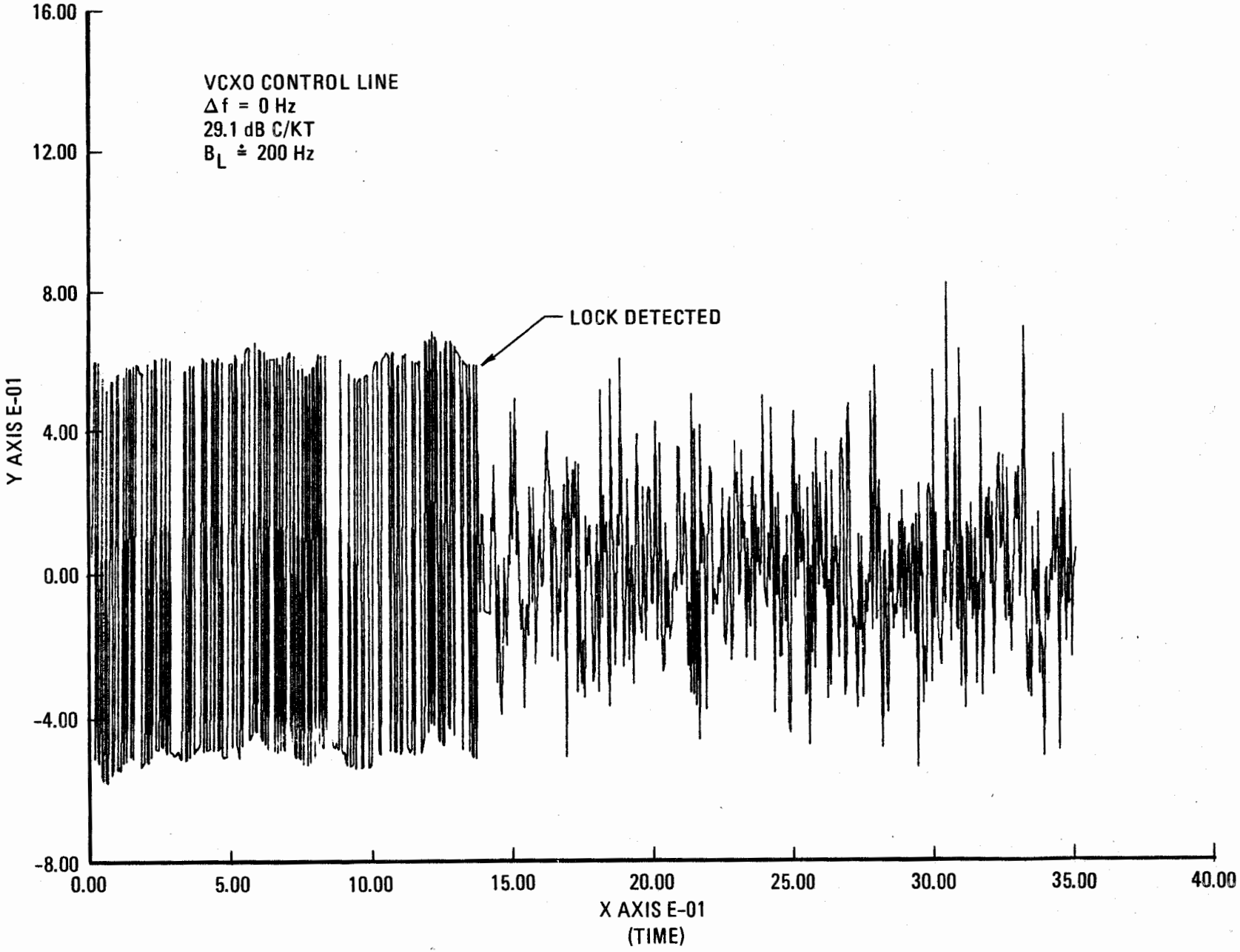


Figure 2-9. Plot of VCXO Control Voltage Versus Time - Δf = 0 Hz

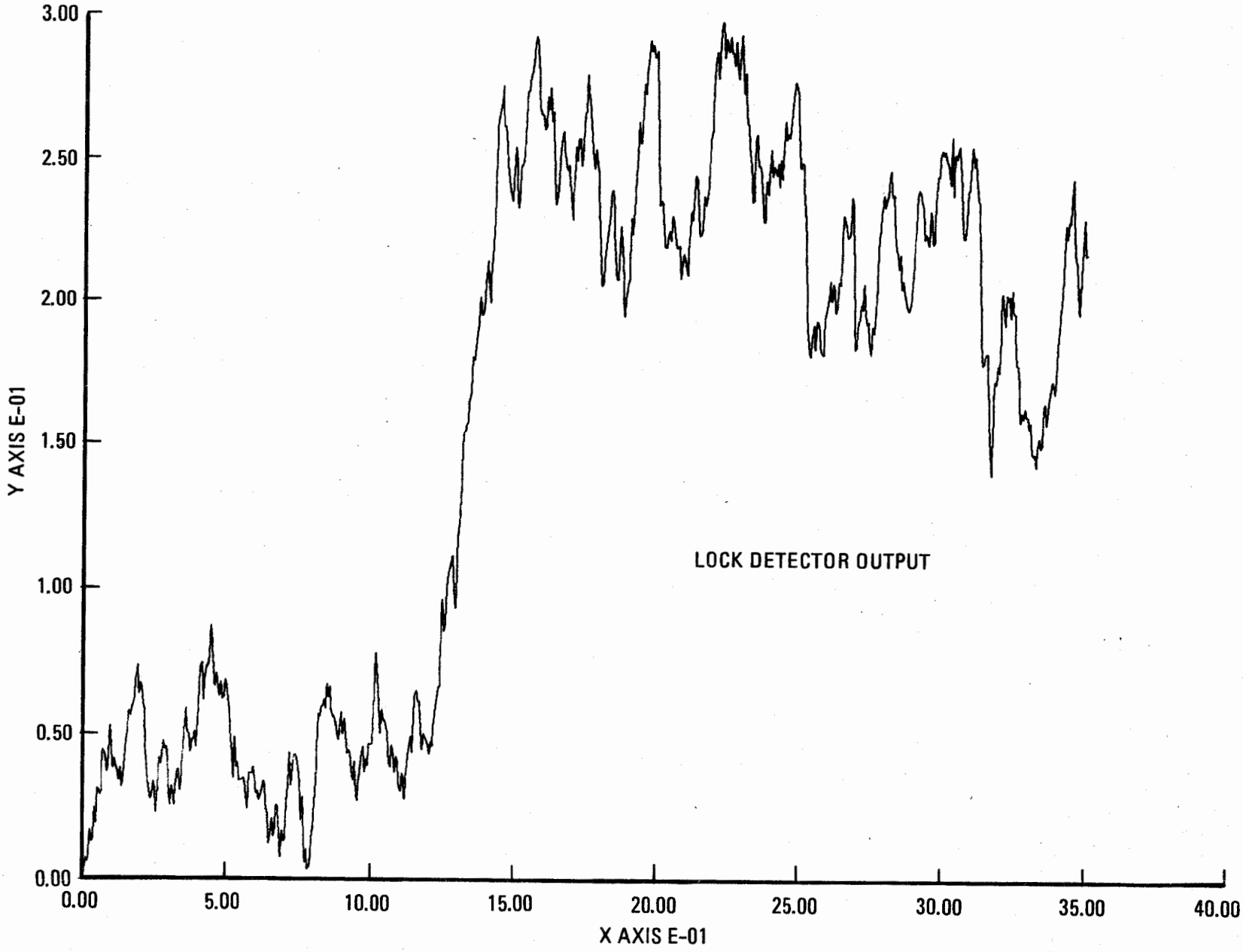


Figure 2-10. Plot of Lock Detector Output Versus Time - Δf = 0 Hz

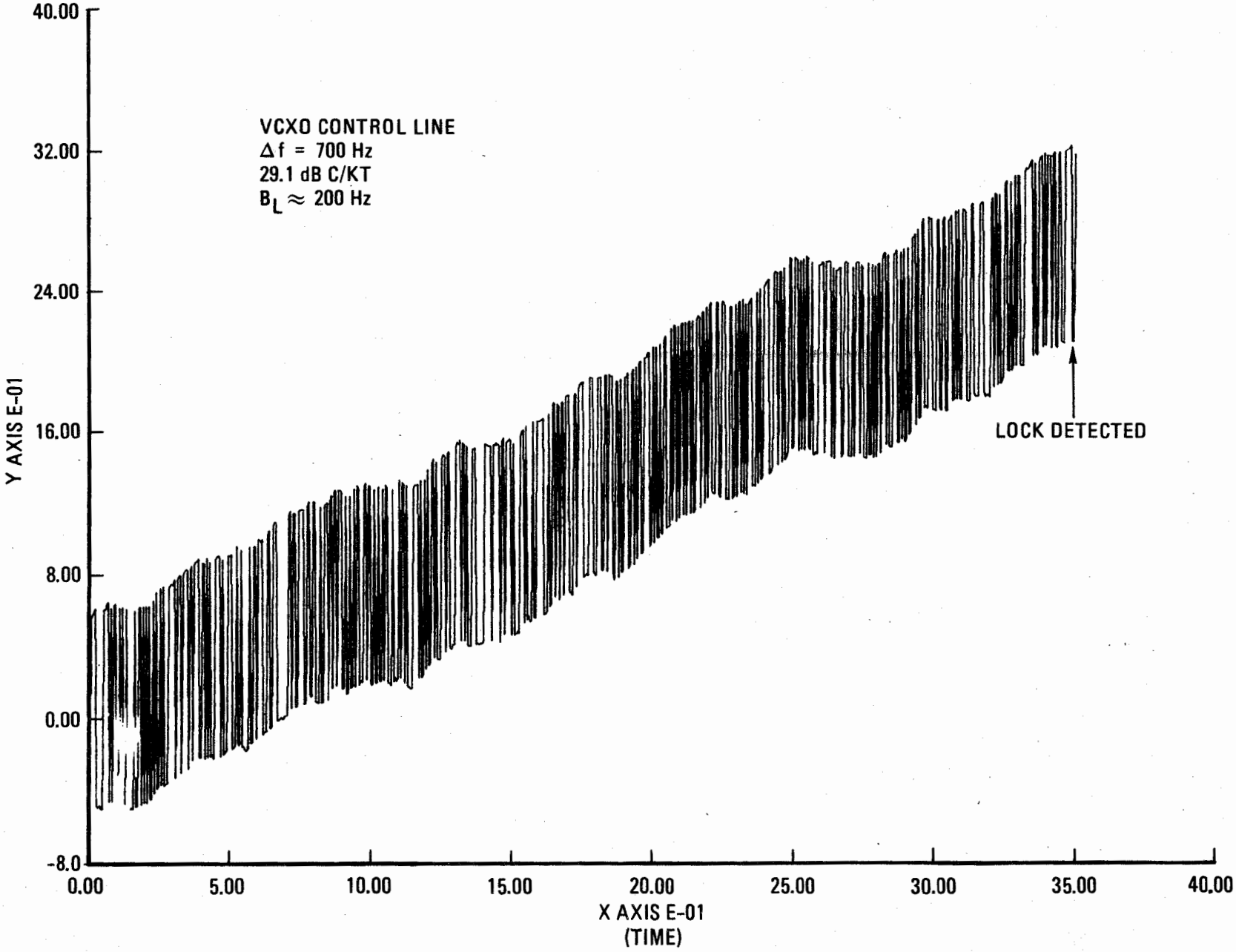


Figure 2-11. Plot of VCXO Control Voltage Versus Time - Δf = 700 Hz

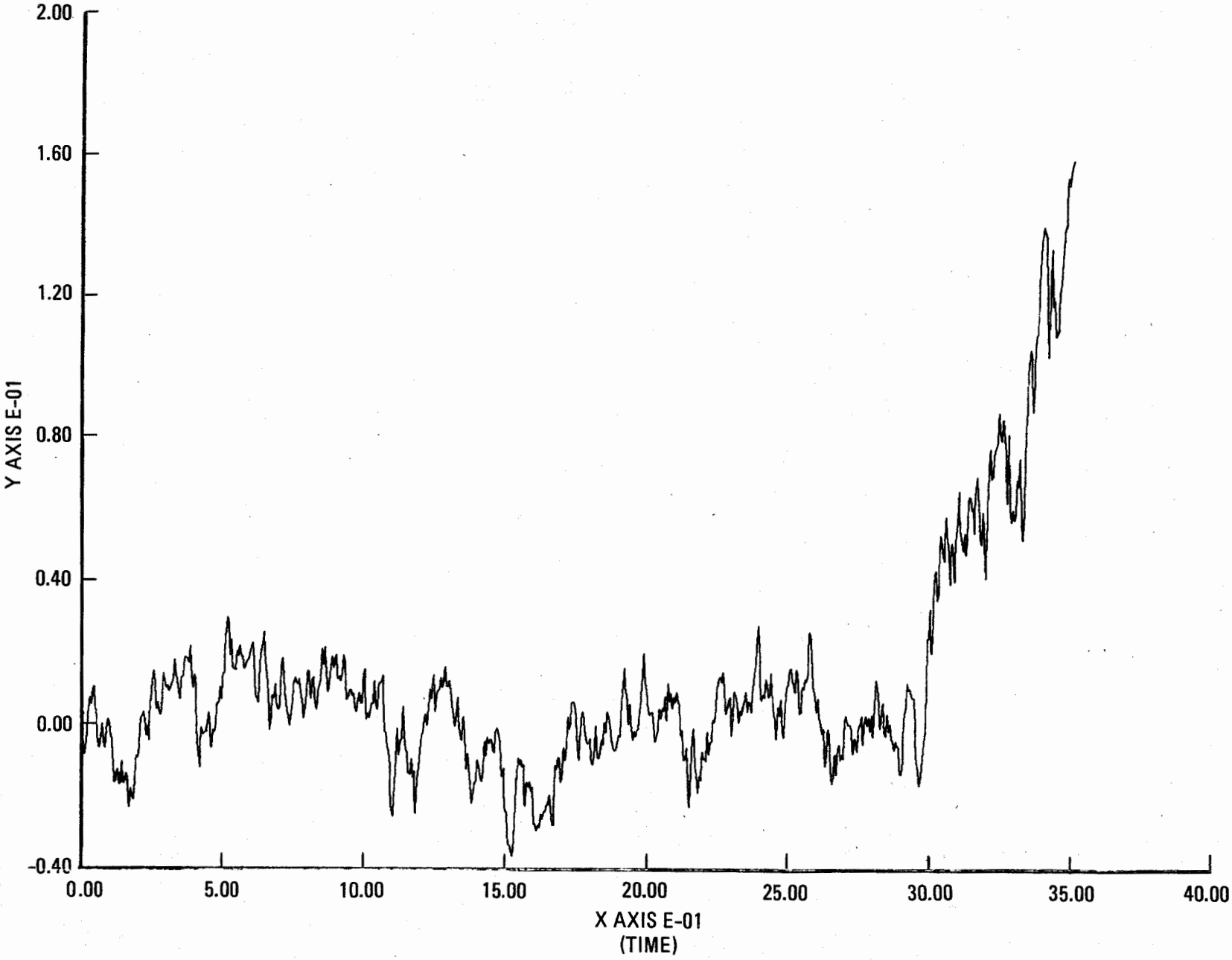


Figure 2-12. Plot of Detector Output Versus Time - Δf = 700 Hz

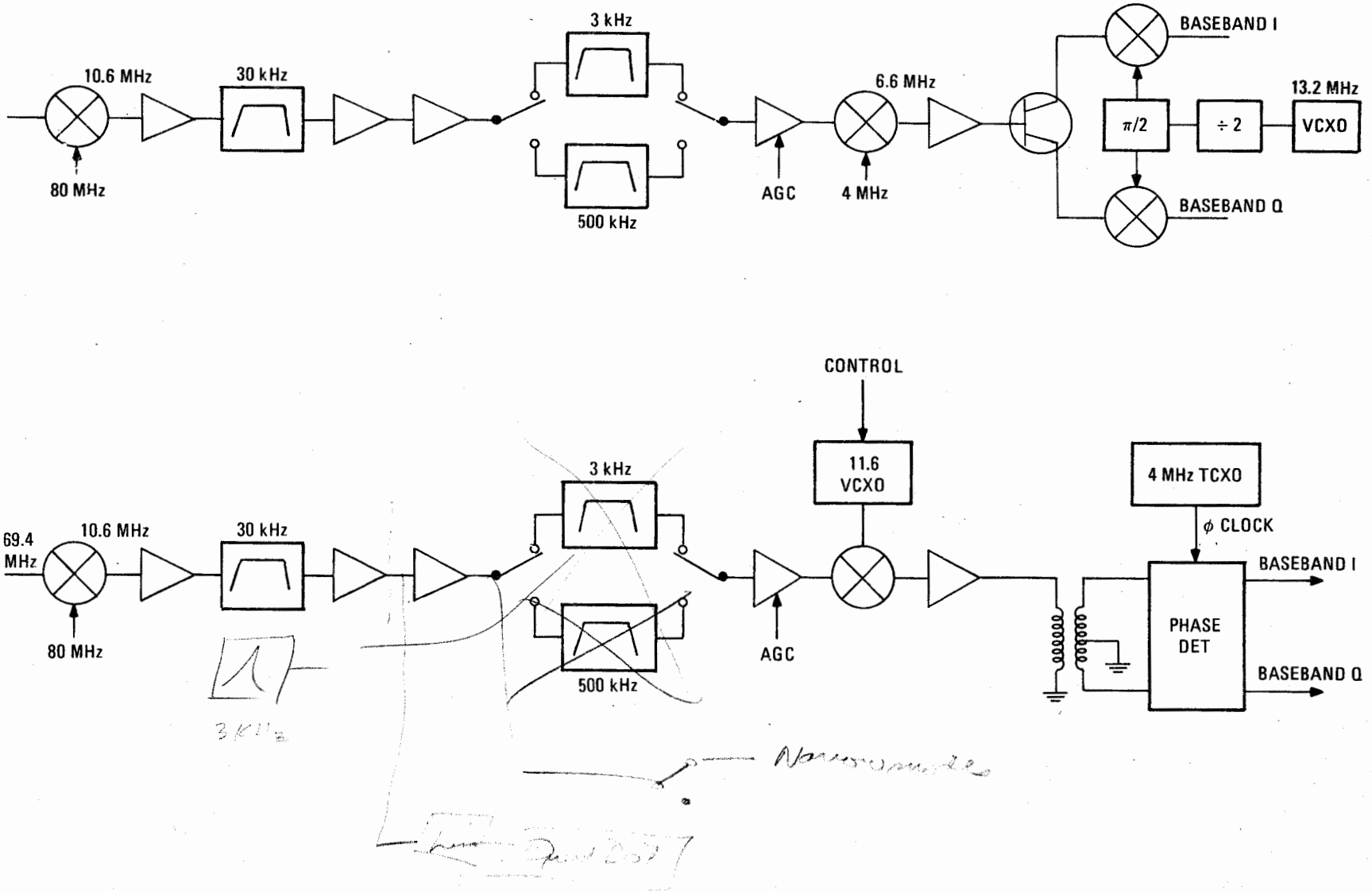


Figure 2-13. AN/PSC-3 Signal Path, Simplified Block Diagram

2.3 FRONT PANEL

The design of the front panel of the PSC-3 includes the capability of remote control of the frequency control and display. The remote control is accomplished by a serial data stream input through an unused pin the front panel XMODE connector. The external serial data will be in a format which tells the frequency controller to ignore the front panel switches and to accept the stimulus from the remote source. This change provides a highly desirable means for testing of the front panel and entire R/T.

An N-line I/O controller is used in the front panel instead of the previously proposed memory mapped I/O concept. The N-line I/O controller reduces the parts count and increases the reliability.

2.4 R/T MECHANICAL

The external dimensions of the R/T have been increased. This increase in size is due to the additional requirement that the R/T mate with the PRC-70, BB-542 battery without the use of a separate adapter. While this significantly increases the outside volume of the R/T, it does not increase the effective consumed volume, because no dimension is larger than the dimensions of the flange previously proposed to mate with the BB-542 battery. The additional internal volume created by this change has not been utilized in order to keep the weight increase to a minimum.

An internal shield has been added to the rear wall of the R/T, for increased EMI protection. All connections from the batteries are filtered as they pass through this shield.

The module locating tabs are cast into the module cases rather than the covers. This allows the use of a thinner, lighter weight, sheet metal cover on the modules.

A module connector with integral guide pins has been selected in lieu of the connector and separate guide pin arrangement previously used in the modules. Keying is accomplished by varying the location of the connector on different modules.

2.5 BATTERY BOX

The battery box housing the two BB-590/U or BA-5590/U batteries has been increased in size to mate with the larger sealing flange on the rear of the R/T. The larger battery box is being constructed of plastic (ABS-Marbon T-Grade cycolac) to minimize its weight. This weight reduction reduces the impact of the R/T weight gain, when considered as a unit ready for field

use. This type of case has more than adequate strength as it is the same material used in the AN/PRC-70 battery case BB-654. Both the battery and the radio are heavier for the AN/PRC-70 than the AN/PSC-3.

2.6 NCS MECHANICAL

The NCS case will be a one-piece investment casting which will be 15.06 ± .040 wide x 11.90 ± .030 deep x 8.00 ± .020 high. It will have two cavities, one large cavity in the bottom with a cover and one cavity in the back. The cover for the cavity in the back will be finned and serve as the heat sink for the Power Amplifier. There will also be a thermostatic controlled blower to provide additional air flow over the heat sink. There will be four connectors on the back, one A/C power connector, one antenna connector, and two connectors for the preselector. Along with these four connectors there will be the D/C power connector that mates with the MT-1029 shock mount. The antenna connector was proposed to be mounted on the front surface, but the installation in both the TSC-99 and 1/4 ton truck lends itself the rear mounted approach. The rear mounted approach will also reduce the cabling internal to the NCS and minimize the cable loss in the receive path.

The front panel of the NCS will have a power switch which is also a circuit breaker, two Selective Call switches, and the RF input connector.