NAVSEA 0967 -LP-000-0120

# ELECTRONICS INSTALLATION AND MAINTENANCE BOOK

## ELECTRONIC CIRCUITS

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## BOX SCORE ELECTRONIC CIRCUITS HANDBOOK NAVSEA 0967-LP-000-0120

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ELECTRONIC CIRCUITS

## PREFACE

#### POLICY AND PURPOSE

The Electronics Installation and Maintenance Book (EIMB) was established as the medium for collecting,' publishing, and distributing, in one convenient source document, those subordinate maintenance and repair policies, installation practices, and overall electronic equipment and material-handling procedures required to implement the major policies set forth in Chapter 400 of the Naval Ships' Technical Manual. All data contained within the EIMB derive their authority from Chapter 400 of the Naval Ships' Technical Manual, as established in accordance with Article 1201, U.S. Navy Regulations.

Since its inception the EIMB has been expanded to include selected information of general interest to electronic installation and maintenance personnel. These items are such as would generally be contained in textbooks, periodicals, or technical papers, and form (along with the information cited above) a comprehensive reference ,document. In application, the EIMB is to be used for information and guidance by all military and civilian personnel involved in the installation, mainntenance, and repair of electronic equipment under cognizance, or technical control, of the Naval Sea Systems Command (NAvSEA). The information, instructions, and procedures, in the EIMB supplement instructions and data supplied in equipment technical manuals and other approved maintenance publications.

#### INFORMATION SOURCES

Periodic revisions are made to provide the best current data In the EIMB and keep abreast of new developments, In doing this, many source documents are researched to obtain pertinent information. Some of these sources include the Electronics Information Bulletin (EIB), the NAVSEA Journal, electronics and other textbooks, industry magazines and periodicals, and various military installation and maintenance-related publications. In certain cases, NAVSEA publications have been incorporated into the EIMB in their entirety and, as a result, have been cancelled. A list of the documents which have been superseded by the EIMB and are no longer available is given in Section 1 of the General Handbook.

#### ORGANIZATION

The EIMB is organized into a series of handbooks to afford maximum flexibility and ease in handling. The handbooks are stocked and issued as separate items so that individual handbooks may be obtained as needed.

The handbooks fall within two categories: general information handbooks, and equipmentoriented handbooks. The general information handbooks contain data which are of interest to all personnel involved in installation and maintenance, regardless of their equipment specialty. The titles of the various general information handbooks give an overall idea of their data content; the General Handbook includes more complete descriptions of each handbook.

The equipment handbooks are devoted to information about particular classes of equipment. They include general test procedures, adjustments, general servicing information, and field change identification data.

All handbooks of the series are listed below with their STOCK numbers.

#### HANDBOOK TITLE STOCK NUMBER

**EIMB General Information Handbooks** 

General	0967-LP-000-0100
Installation Standards	0967-LP-000-0110
Electronic Circuits	0967-LP-000-0120
Test Methods & Practices	0967-LP-000-0130
Reference Data	0967-LP-000-0140
EMI Reduction	0967-LP-000-0150
General Maintenance	0967-LP-000-0160

#### EIMB Equipment-Oriented Handbooks

Communications	0967-LP-000-0010
Radar	0967-LP-000-0020
Sonar	0967-LP-000-0030
Test Equipment	0967-LP-000-0040
Radiac	0967-LP-000-0050
Countermeasures	0967-LP-000-0070

CHANGE 1

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PREFACE



#### DISTRIBUTION

<u>Initial Set</u>: An "AF" Restriction Code has been **assigned** to NAVSEA 0967-LP-OOO-OOO0 to control **the** over-requisitioning of the EIMB Series. Fleet and shore activities requiring an initial set of the EIMB Series (13 handbooks with all changes and heavy-duty binders) should submit their-requisition- (DD Form 1348 with written justification) through their Supply Officer or area, for issue approval to:

> Commander Naval Sea Systems Command SEA 05L32 Washington, DC 20362

Use the following data on the DD-1348, Block A - 288 NAVPUBFORMCEN PHILA Stock No. - **Ø967-LP-ØØ-ØØØ** Unit of Issue - SE Fund -00

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<u>Changes and Revisions</u>: The EIMB is continuously being updated. For efficiency these changes and **revisions** are automatically distributed to using activities who are on the Automatic Distribution List for the EIMB. Requests and/or changes to the EIM8 Automatic Distribution List and any problems in

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Individual Handbooks: To order individual handbooks and changes, use the stock numbers listed in the Box Score on page ii. Using the stock number for the "BASIC" provides the handbook (with vinyl cover) and all applicable changes.

#### SUGGESTIONS/CORRECTIONS

NAVSEA recognizes that users of the EIMB will have occasion to offer corrections or suggestions. To encourage more active participation, a pre-addressed **Comment** sheet is provided in the back of each handbook change. Complete information should be given when preparing suggestions. Suggesters are encouraged to include their names and addresses so that clarifying correspondence can be initiated when necessary. Such correspondence will be by letter directly to the individual concerned.

If a cotnnent sheet is not available, or if correspondence is lengthy, corrections or suggestions should be directed to the following:

> Commander Naval Sea Systems Command SEA 05L32 Washington, DC 20362

CHANGE 1

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#### SECTION 1 INTRODUCTION

#### PURPOSE

The purpose of the Handbook of Electronic Circuits is to provide Naval personel with an informative reference which describes basic electronic circuits employed in **all** types of electronic equipment. In addition, this handbook is used to support circuit descriptions contained in equipment technical manuals.

#### USE

The Handbook of Electronic Circuits will find use as a convenient reference for personnel in three general categories, as follows:

#### a. Experienced Technician

The experienced technician will have no great difficulty in coping with maintenance problems because of previous experience and developed maintenance skills. This individual will use the handbook as reference or review material and to increase his knowledge of electronics as new circuits are added to the handbook.

#### b. Technician Out-of&hool

This category of technician is represented by the individual who has completed Navy training courses and has been in the fleet for some time, but his experience is limited to equipments covered in training courses and to equipment types serviced and maintained during his tour of duty with the fleet. The handbook should prove extremely valuable to this individual, especially when confronted with newer equipments, because the circuit descriptions in the handbook will help familiarize him with circuits employed in the newer equipment. Furthermore, it is likely that the technical manuals accompanying newer type equipments will refer the reader to the Handbook of Electronic Circuits for information on basic functional circuits, rather than discussing the circuits in detail.

#### c. Trainae or Student h-school

The trainee or student should **find** the information contained in the handbook useful as reference material while in training and later as review and reference material while on duty with the fleet. As a training aid, the individual circuit descriptions may be used as suggested materird for reading assignments.

The reader of the Handbook of Electronic Circuits may readily locate the circuit of interest by consulting the Table of Contents. Each circuit description includes information on the circuit application, its important characteristics, an anrdysis of circuit theory and operation, and a failure analysis based upon signal output indications. Since only basic circuits are presented and described, some variations in design will be found in production equipments because of one or more of the following factors: distributed inductance, capacitance, and resistance; mechanical and physical layout of component parts; circuit deviations necessitated by peculiarities in design and licensing agreements; modifications to enable operation under environmental extremes; etc. However, if the reader thoroughly understands the operation of a basic circuit presented in the handbook, he can reason out the circuit variations without too much difficulty.

The semiconductor device has become one of the outstanding scientific achievements in the electronics field in recent years. As a result, new techniques of circuit design, miniaturization, reliability, and maintenance concepts are being developed. These advances mean that the electronics technician must be prepared to maintain electronic equipments in which semiconductors are employed. To ensure that he will have the circuit information available for attaining proficiency in the maintenance of semiconductor equipment, this handbook includes semiconductor equivalents of the electron-tub circuits, whenever such equivalents exist, and in addition, includes some semiconductor circuits for which there are no electron-tube equivalents.

The Handbook of Electronic Circuits is used as supporting information for technical manuals covering electronic equipment. Technical manuals written and produced in accordance with recent publication specifications do not require a detailed theory treatment of so-called "standard" circuits,

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but instead may refer to the Handbook of Electronic Circuits for a discussion of a particular functional circuit. Since the Handbook of Electronic Circuits describes a basic functional circuit and may not describe a circuit identical with the circuit employed in the equipment, the equipment technical manual discusses the circuit differences which are unique and peculiar to the equipment, or differences which represent changes or modifications to the basic functional circuit described in the handbook. Thus, the handbook will describe a basic circuit which is typical and performs a given function. If necessary, the equipment technical manual will treat only circuit differences in detail, building upon the discussion given in the Handbook of Electronic Circuits.

#### SCOPE

Preliminary studies made by the National Bureau of Standards leading toward electronic circuit standardization indicate that a large percentage of circuit functions could be standardized without adverse effect on equipment performance. Further, many circuits already in use for several years represent designs which have proven to be extremely reliable and have undergone only minor improvements since their initial use. Today there exists a large number of commercial and military equipments employing similar circuits to perform identical electrical functions. Thus, many similar electronic circuits can be reduced to a "commondenominator" circuit representing a basic circuit from which others performing an identical electronic function have been derived either through modification or other engineering improvements. As a result, the technician is frequently confronted by new equipments introduced to the fleet which contain circuits reflecting design improvements.

Frequently, it is up to the individurd to familiarize himself with new equipment by means of the technical manual supplied with the equipment. Furthermore, circuits may be incorporated which are totally unfamiliar to the individual. In this case the use of the Handbook of Electronic Circuits should prove extremely valuable, since the circuit or group of circuits in question can likely be reduced to one or more "commondenominator" circuits. When these basic circuits, described in the handbook, are understood by the individual, similar circuits employed in new equipment, together with their modifications or differences, can be more readily understood by the individual.

The Handbook of Electronic Circuits has been divided into sections based upon the circuit function, rather than being classified according to use as communications, radar, or sonar equipment. Severrd sections are devoted to general circuit information applicable to either electron-tube or semiconductor circuits. When an electron-tube circuit is described, generally the most common or likely tube type (triode, pentode) is utilized in the handbook description. Where the basic electronic theory is the same for either electron-tube or semiconductor circuits, the basic theory is discussed within the description of the electron-tube circuit and referenced from the semiconductor circuit description; thus, repetition of text is reduced.

Each description of an electronic circuit employing an electron tube or semiconductor is divided into four main parts: application, characteristics, circuit analysis, and failure analysis.

#### a. Application

This part of the circuit description states briefly how the circuit is employed, its common uses, and the types of equipments employing the circuit.

#### **b.** Characteristics

This part of the circuit description consists of short statements concerning technical data and other useful information to assist in circuit identification.

#### c. Circuit Analysis

The circuit analysis section of the description is written to outline in general terms the circuit function and to name the component parts of the circuit, to describe critical elements or component parts in detail, and to present the theory of operation of the circuit. A schematic with reference designations is used to illustrate the circuit; the associated text utilizes the reference designations when discussing the circuit. Actual values of parts do not normally appear in the text or on the schematic. Additional illustrations, such as ~\_\_\_

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## NOTES

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idealized waveforms and simplified diagrams, are provided where deemed necessary to supplement the text.

#### d. Failure Analysis

This portion of the circuit description is written from an output-indication standpoint based upon possible degradation of performance, changing vrdues of components, etc. The critical circuit components affecting amplitude, time (or frequency), and waveshape are treated in the circuit analysis section. These critical components are again mentioned in the failure analysis discussion, but in this instance from the standpoint of the output signal observed.

The failure analysis discussion is intended to assist the reader in the development of a **logical** approach to trouble shooting. The failure analysis, as **written** for an individual circuit, does not pinpoint (or name) parts which "could be" defective but, in effect, encourages the reader to think logically and determine defective or deteriorating parts from the output indications noted. The text, therefore, discusses in broad terms the various troubles that might logically be suspected as the cause of an abnormal (output) indication.

Abnormal output indications observed in equipments are actually symptoms which can be elaborated upon to further localize trouble with a functional circuit. Output indications as discussed in the text elaborate on the circuit analysis text to assist the reader in analyzing a failure; thus, an arbitrary conclusion as to the source of trouble or failure is discouraged and logical reasoning is stimulated. Typical indications discussed are: no output, distorted output, low output, and incorrect output frequency. In these discussions, the reader's attention is called to the improper function within the electronic circuit. Furthermore, so-called "critical" parts (or components) were discussed in the circuit analysis portion of the circuit description from the theoretical and operational standpoint; thus, a complete story is given for the circuit. Logical thinking, therefore, can be applied to the problem of localizing the failure within the circuit after the reader has studied the entire circuit description given in the handbook.

#### HANDBOOK CHANGES

The handbook, as sectionalized, permits the future addition of circuits to keep the handbook

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abreast of electronic developments. Also, the layout of the handbook is designed to permit the addition of new electron-tube or semiconductor circuits, as well as to permit the revision of the existing circuits.

Changes to this handbook **will** be publicized in the Electronic Information Bulletin (EIB), NAV-SHIPS 0967-001-3000 and automatically distributed to holders of the EIMB series. Recommendations for changes and corrections to the handbook should be addressed to:

Commander, Naval Ship Engineering Center Technical Support Branch Technical Data and Publications Section (SEC 6181C) Department of the Navy Prince George's Center

I line George's Center

Hyattsville, Maryland 20782

#### DEFINITIONS OF LETTER SYMBOLS USED

Throughout this technical manual a number of letter symbols are used to indicate components, sources of voltage and current, and to differentiate between points not at the same power and voltage levels. Since the technician must be able to read, speak, and understand the jargon of the trade, he should also learn to recognize the letter symbols used as a form of shorthand notation in technical discussions and on engineering drawings and schematic diagrams. To avoid any conflict or confusion, standard letter symbols are used where available. Since definitions and usage change from time to time, an alphabetical listing of symbols used throughout this manual is included for reference (they need not be memorized).

While the basic symbol such as the capital letters E and I always indicate voltage and current, the lower case and subscript letters (or numbers) are assigned as described in the following list of symbols. Therefore, it is recommended that the user of this manual refer to this list to determine the correct meanings of the letter symbols used in the circuits in this technical manual.

#### a. Construction of Symbols

The letter symbols are made up of single letters with subscripts or superscripts in accordance with the following conventions:

1. Maximum, average, and root-meansquare values are represented by capital (upper case) letters; for example: I, E, P. 2. Where needed to distinguish between values in item a above, the maximum value may be represented by the subscript "m"; for example: Em, Im, Pm.

3. Average values may be represented by the subscript "av"; for example:  $E_{av}$ ,  $I_{av}$ ,  $P_{av}$ .

NOTE

When items 2 and 3 above are used, then item 1 indicates rms, or effective, values.

4. Instantaneous values of current, voltage, and power which vary with time are represented by the lower case (small) letter of the proper symbol; for example: i, e, p.

5. External resistance, impedance, etc, in the circuit external to a vacuum-tube electrode may be represented by the upper case symbol with the proper electrode subscripts; for example:  $R_s > R_{sc}, Z_s, Z_{sc}$ .

6. Values of resistance, impedance, etc, inherent within the electron tube are represented by the lower case symbol with the proper electrode subscripts; for example:  $r_s, Z_s, r_p, Z_p, C_{gp}$ . 7. The symbols "g" and "p" are used as

7. The symbols "g" and "p" are used as subscripts to identify instantaneous (ac) values of electrode currents and voltages; for **example**: eg,  $e_p$ ,  $i_e$ ,  $i_p$ .

8. The total instantaneous values of electrode currents and voltages (dc plus ac components) are indicated by the lower case symbol and the subscripts "b" for plate and "c" for grid; for example: ib, e, i, eb.

9. No-signrd or static currents and voltages are indicated by upper case symbol and lower case subscripts "b" for plate and "c" for grid; for example: E., Ib, Eb I.

10. RMS and maximum vahres of a varying component are indicated by the upper case letter and the subscripts "g" and "P"; for example: Eg, Ip, Ep, Ig.

11. Average values of current and voltage for the with-signal condition are indicated by adding the subscript "s" to the proper symbol and subscript; for example: Ibs, Ebs.

12. Supply voltages are indicated by the upper case symbol and double subscript "bb" for **plate**, "cc" for grid, "**ff**" for **filament**; for example: Eff,  $E_{cc}$ , Ebb.

#### b. List of Symbols

Since the rules above are somewhat complex, an alphabetical list of the commonly used symbols is presented below.

Symbols	Definitions		
с	Capacitor, capacitance		
C <sub>c</sub>	Coupling capacitor		
Cd	Distributed circuit capacitance		
C	Grid-leak or grid capacitor		
c &	Grid-cathode capacitance		
Cgp	Grid-plate capacitance		
C <sub>k</sub>	Cathode capacitor		
Cn	Neutralizing capacitor	)	
C <sub>n</sub>	Plate capacitor		
Cnk	Plate-cathode capacitance		
Csc	Screen capacitor		
Csun	Suppressor capacitor		
E, V	Voltage		
Ea	Applied voltage		
E	Average voltage		
Eb	Plate voltage static de value		
Ebb	Plate voltage source		
200	(supply voltage)		
Ec	Capacitor voltage		
E	Grid voltage, static dc (bias) vahre		
 Ecar	DC voltage applied to produce		
-Cai	carrier		
Е	Grid bias supply voltage		
E 1	Control grid supply		
Ecc2	Screen grid supply		
E <sub>m</sub> 3	Suppressor grid supply		
E	Negative tube cutoff voltage		
Ef	Filament voltage		
Eff	Filament supply voltage		
E	Root-mean-square value of grid		
8	voltage		
Eem	Maximum value of varying grid		
B	voltage component	$\smile$	
Ein, Ei	Input voltage		
Er	Reactive voltage drop		
Em. E	Maximum voltage		
Emin	Minimum voltage		
E E t	Output voltage pack		
$\mathbf{E}_{o}, \mathbf{E}_{out}$	Plate voltage rms value		
	Peak voltage		
~рсак, ~рк Ер	Resistive voltage drop		
France State	rms voltage value		
E	Screen voltage de value		
	Server , onuge, de vulue		

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INTRODUCTION

e	Instantaneous voltage	i,	Instantaneous ac component of
еЪ	Instantaneous plate voltage	P	plate current
ec	Instantaneous grid voltage	it	Current per instant of time
ecar	Instantaneous carrier voltage	iZ	Instantaneous current through
eg	Instantaneous ac component of	-	impedance
	grid voltage	L	Inductance inductor
El	Instantaneous voltageon element	t 1 P	Power
e <sub>m</sub>	Maximum instantaneous voltage	Pa	Grid dissipation power
eo	AC component of output voltage	Pi	Input power
e	Instantaneous ac component of	Po	Output power
	plate voltage	Pp	Plate dissipation power
e <sub>pri</sub>	Instantaneous ac component of	Pa	Reactive power
-	secondary voltage	Ps	Apparent power
er	Instantaneous resistive voltage	Q	Figure of merit
1	dron	R	Resistance, resistor
esc	Instantaneous screen voltage	RG	Generator internal resistance
esec	Instantaneous ac component of	R <sub>g</sub>	Grid resistance
	primary voltage	RL	Load resistance
esia	Instantaneous signal voltage	Rk	Cathode resistance
e <sub>su</sub>	Instantaneous suppressor voltage	R	Plate resistance, dc
f	Frequency	RS	Series resistance
fo, fr	Resonant frequency	R <sub>Sc</sub>	Screen resistance
gm	Transconductance	гL	AC load resistance
Ĭ	Current	r	Plate resistance, ac
Iav	Average current	SWR	Standing-wave ratio
Ib, 1 <sub>0</sub>	Static dc plate current	t	Time
IC	Capacitive current	td	Deionization time
I <sub>c</sub>	Static dc grid current	tf	Pulse fall time
If	Filament current	tk	Cathode heating time
I	Grid current, rms value	tp	Pulse duration time
<b>I</b> Ľ	Inductive current	t <sub>r</sub>	Pulse rise time
I, Imax	Maximum current	Т	Transformer
Imi*	Minimum current	TC	Time constant
1 <sub>P</sub>	D-C plate current, rms value	V,v, E	Voltage, volts
Ir	Current in resistor	W	Watts
Irk	Cathode current	Х	Reactance
I <sub>rms</sub>	rrns current value	x <sub>C</sub>	Capacitive reactance
Іт	Total current	XL	Inductive reactance
It	Current for time interval (usually	Y	Admittance
-	used with subscripts as the t2 etc.	Z	Impedance
ih	Instantaneous plate current	Zin	Input impedance
ic	Instantaneous grid current	zL	Load impedance
ī.	Instantaneous ac component of	7	
g	grid current	<b>L</b> .	Unaracteristic impedance, surge
iı	Instantaneous inductive current	7.	Impedance
- L.	instantaneous inductive current	≁out	Output impedance

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#### SECTION 2 POWER SUPPLIES

#### **PART 2-O. INTRODUCTION**

#### **ELECTRON TUBE DIODE PRINCIPLES**

#### General.

A diode electron tube consists basically of only two elements: a cathode (or filament) and a plate. The cathode is responsible for the primary emission of electrons, while the plate collects the electrons emitted by the cathode. The general arrangement of the elements within a diode electron tube is shown in the figure below. This is also the basis of. operation for **all** types of electron tubes.



A. Electron Flow When Plate is Positive



B. Electron Flow When Plate is Negative

When heat is applied to the cathode circuit by the filament, the cathode emits electrons into the space surrounding it (the *Edison Effect*). With no voltages applied to the cathode or plate, this space *charge will* move randomly between the two elements, and no current will flow in the tube circuit.

When the positive side of the battery is connected to the plate of the diode and the negative side of the battery is connected to the cathode (refer to part A of the figure), the electrons emitted from the cathode will move toward the plate, since unlike charges attract each other, and current flow results in the tube circuit. If the connections are reversed as shown in part B of the figure so that the cathode is positive with respect to the plate, the electrons in the space charge will instead be attracted toward the cathode. Additionally, the negative charge of the plate further repels these electrons toward the cathode, and no current flow results in the tube circuit. Thus, in a diode tube circuit, it can be seen that electron flow can only exist if the plate is positive with respect to the cathode.

#### **ELECTRON TUBE DIODE RATINGS**

#### General.

Three important ratings used in connection with diode electron tubes are discussed in the following paragraphs.

**Peak Forward Anode Voltage.** This voltage is the maximum instantaneous anode **(plate)** voltage that can be applied to the tube without damage to the tube structure.

**Peak Inverse Anode Voltage. This** voltage is the maximum (reverse) instantaneous voltage that can be applied to the anode (plate) during non-conducting periods. When the diode is used in power supply circuits for rectilication, the alternating voltage applied to the diode plate will go highly negative with respect to the cathode. If the maximum peak inverse voltage is exceeded, the plate can become so negative with respect to the cathode that the tube can arc from the negative plate to the positive cathode. When this happens, the tube is generally permanently damaged.

**Peak Anode Current. This** current rating is the maximum instantaneous plate current that can be conducted by the diode without tube damage.

#### SEMICONDUCTOR DIODE PRINCIPLES

#### General.

Semiconductor diodes are employed for rectification and detection similarly to electron-tube diodes;

in addition, they have special properties that make them particularly useful for bias and voltage stabilization. Since junction diodes can be made of the same material as the transistor and have the same temperature coefficient and resistance, they will *track* better over the same temperature range, providing nearly ideal thermal compensation. Likewise, application of the avalanche breakdown phenomena provides a special voltage-stabilizing (Zener) diode.

Junction Diode Theory. When P-type and N-type germanium are combined in manufacture, the result is a P-N junction diode, which has characteristics similar to that of the electron-tube diode. If properly biased, the junction diode will conduct heavily in one direction and very lightly or practically not at all in the other direction. The P and N sections of the diode are analogous to the plate and cathode of the electrontube diode. The direction of heavy current flow is in the forward, or easy current, direction; the flow of light current (back current) is in the reverse direction. To produce a forward current flow, it is necessary to bias the junction diode properly. Proper bias comections for forward and reverse currents are illustrated below. The triangle in the graphical symbol (sometimes called an arrowhead) points against the direction of electron current flow. It is evident that the polarities and electron current flow of the junction diode are identical with those of the vacuum-tube diode and the crystal semiconductor (point-contact) diode. Because of the reverse (back) current flow



**Diode Biasing Circuits** 

(which is not present in any appreciable amount in a vacuum-tube) and the resistivity of the semiconductor, the operation and theory of a junction diode differ somewhat from that of the electron tube diode.

A discussion of the operation of the PN (and the NP) junction and its application to the transistor is included at this point, since an understanding of current flow through the junction and how it varies with external applied bias is essential to circuit operation in later discussions. In semiconductor theory two types of current carriers are encountered, namely, electrons and holes. At room temperature heat energy imparted to a semiconductor causes some electrons to be released from their valence bands with sufficient energy to place them in the conduction band. The resultant vacancy created in the valence band possesses a positive charge and is called a *hole*. When holes are present in the valence band, electrons can change their energy state, and conduction is possible by hole movement. Likewise, electrons in the conduction band can change their state, and conduction is possible by *electron* movement. Thus, conduction within the semiconductor is caused by the movement of positive (hole) and negative (electron) carriers. Although the movement of holes is the result of the movement of electrons, the charge which moves is positive; therefore, it is common to speak of hole movement in the valence band rather than electron movement. In contrast, in a pure conductor such as copper the conduction band and valence bands overlap and are not separated by a forbidden region; thus there is an excess of electrons available, and conduction is spoken of only in terms of electron movement.

An intrinsic semiconductor is one to which no impurities have been added, and in which an equal number of electron and hole carriers exist. An extrinsic semiconductor is one to which an impurity has been added, and in which conduction takes place primarily by one type of carrier. Although the amount of impurity is extremely small (on the order of one part in one million or less), the effect upon the conductivity of the semiconductor is profound. The addition of an impurity which creates a majority of electron carriers is known as a *donor* (because it donates electrons), and the extrinsic semiconductor which results is called N-type. Likewise, the addition of an impurity which creates a majority of hole carriers produces a P-type semiconductor, and is referred to as an *acceptor* impurity (because it will accept electrons).

A PN junction is a single crystal consisting of P and N types of semiconductors formed by an alloying or growing process. To facilitate an understanding of its operation, it is assumed that if the P and N materials are brought together externally the junction will function normally, although actually it will not. Each type of material is considered to be electrically neutral. When the P and N materials are brought into contact to form the PN junction, a concentration gradient exists for electrons and holes. Holes diffuse from the P material into the N material, and electrons diffuse from the N material into the P material. This process continues until the donor and acceptor sites near the junction barrier lose their compensating carriers and a potential gradient is built up which opposes the tendency for further diffusion. Eventually a condition of balance is reached where the current across the junction becomes zero. The relationships across the junction and the final charge dipole which results from the diffusion process is graphically illustrated below.

be represented by a space-charge equivalent battery (commonly called a *potentiul hill* battery). In the absence of an external field, the magnitude of the difference in potential across the space-charge equiva*lent battery* (this potential is not available for external use as a battery) is on the order of tenths of a volt.

When the negative terminal of an external battery is connected to the P material and the positive terminal is connected to the N material, the junction is said to be reverse-biased. In this condition, the external battery polarity is the same as that of the potentialhill battery as shown below. Therefore, the bias battery aids the potential-hill battery, and very little or no forward current passes across the junction. This action occurs because the holes are attracted to the negative terminal of the external battery and away from the junction. Similarly, the electrons are attracted to the positive terminal of the battery and away from the junction. Thus, the depletion area is effectively widened, and the potential across the junction is effectively increased, making it more difficult



**Electric Field Relationships** 

The region containing the uncompensated donor (negative) and acceptor (positive) ions is commonly referred to as the *depletion* region. (Since the acceptor and donor ions are freed and are charged electrically, the depletion region is sometime called the *space charge* region.) The electric field between the acceptor (positive) and donor (negative) ions is called a *barrier*, and the effect of the barrier is considered to



**Raverse Bias Conditions** 

for normal current to flow. With the majority carriers effectively blocked, the only current that can flow is that caused by the minority carriers, and it is in the opposite (or reverse current) direction. This reverse current is called *back current*, and is substantially independent of reverse-bias vrdues until a certain voltage level is reached. At this voltage the covalent bond structure begins to break down, and a sharp rise in reverse current occurs because of avalanche breakdown. The breakdown voltage is popularly called the Zener voltage, although there is some doubt as to the manner in which it occurs. Once the crystal breaks down, there is a heavy reverse (back) current flow, which, if not controlled, can overheat the crystal and cause permanent damage. If the current is kept at a safe value, the crystal will return to normal operation when the reverse bias is again reduced to the proper value. The construction of the junction determines the type of back current flow. A crystal with more N-type material than P-type material will have a back current due to electron flow; conversely, a crystal with predominantly P-type material will have a back current due to hole flow.

Back current exists solely because the depletion area, although depleted of majority carriers, is never entirely free of minority carriers, and, since they are effectively polarized opposite to the majority carriers, the external reverse-bias polarity is actually a forward bias for the minority carriers.

When the external bias battery is connected so that it is oppositely polarized to the potential-hill battery (positive to P region and negative to N region), the barrier voltage is reduced, and a heavy forward current flows; this bias condition is called *forward* bias. Forward current flow is heavy because the electrons of the N region are repelled from the negative battery terminal and driven toward the junction, and the holes in the P region are forced toward the junction by the positive terminal. Depending upon the battery potential, a number of electrons and holes cross the barrier region of the junction and combine. Simultaneously, two other actions take place. Near the positive terminal of the P material the covalent bonds of the atoms are broken, and electrons are freed, to enter the positive terminal. Each free electron which enters the positive terminal produces a new hole, and the new hole is attracted toward the N material (toward the junction). At the same time an electron enters the negative terminal of the N material and moves toward the junction, heading for the positive terminal of the P material. This action reduces the effective value of the potential hill so that it no longer prohibits the flow o'f current across the barrier, or junction, as shown by the upper portion of the illustration below. Internal current flow occurs in the P region by holes (the majority carriers) and in the N region by electrons (also majority carriers). Externally, the current consists of electron flow and is dependent upon the bias battery potential.



Forward-Bias Conditions

If the forward bias is increased, the current through the junction likewise increases, and causes a reduced barrier potential. If the forward bias were increased sufficiently to reduce the barrier potential to zero, a very heavy forward current would flow and possibly damage the junction because of heating effects. Therefore, the forward bias is usually kept at a low value. Although the initial junction barrier

#### **ELECTRONIC CIRCUITS**

potential is on the order of tenths of a volt, the material comprising the junction is a semiconductor and has resistance. Thus the applied bias must be sufficient to overcome the resistive drop in the semiconductor; as a rule, one or two volts is usually required to produce a satisfactory current flow. '

Even though the depletion region is less depleted with forward bias, the minority carriers still exist. The flow of reverse leakage current is practically negligible, however, because the forward bias is in effect a reverse bias to the minority carriers and reduces the back current practically to zero.

The dynamic transfer characteristic curve of the junction diode, illustrated below, shows how the conduction varies with the applied voltage. Observe that **as** the reverse bias is increased, a point is reached where the back current suddenly starts to increase. If the reverse bias is increased still further, avalanche breakdown occurs and a heavy reverse current flows as a result of crystal breakdown (sometimes called the *Zener effect). The* minimum breakdown voltage of the junction diode corresponds to the maximum inverse peak voltage of an electron-tube diode.



**Diode Transfer Characteristic Curve** 

#### Application.

The application of semiconductor rectifiers in the design of power supplies for electronic equipment is increasing. The characteristics which have caused this increase are: no requirement for filament (cathode) power, immediate operation without need for warmup time, low internal voltage drop substantially independent of load current, low operating temperature, and generally small physical size.

Formerly, metallic or dry-disc rectifiers, such as copper-oxide, copper-sulfide, and selenium rectifiers, were used primarily in low-voltage applications and were limited in use to the lower frequencies (25 to 800 Hz). Additional design improvements have allowed these rectifiers to be used with higher input voltages, and today they are widely used as power rectifiers. The newer silicon-type rectifier is now used in many power-supply circuits where other types were formerly used. The small physical size of semiconductor rectifiers, especially the silicon types, makes it practical to place these units in series to handle the higher input voltages.

The semiconductor rectifier is utilized as a diode in power-supply circuits in much the same manner as the electron-tube diode. A semiconductor rectifier can be substituted for each electron-tube diode in almost every basic power supply circuit given in this handbook; furthermore, many power-supply circuits which were originally designed to use tubes and were formerly considered impracticable can now be used to advantage by incorporating semiconductor rectifiers in lieu of electron-tube diodes. For example, a voltage-multiplier circuit with many stages to obtain an extremely **high-voltage** output becomes practicable when semiconductor-type rectifiers are used because the need for an independent filament-voltage source for each stage (to operate directly-heated diodes) is eliminated.

Semiconductor rectifiers are particularly welladapted for use in the power supplies of portable and small electronic equipment where weight and space are important considerations. Many of these smaller





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power supplies use very practical bridge and voltagedoubler circuits which require a transformer having only a single high-voltage secondary winding; thus, there is no requirement for a large, expensive transformer which has a center-tapped secondary winding (or an extremely high-voltage secondary winding).

Semiconductor Diode Symbol. The rectifying action of semiconductor diodes is essentially the same as that for electron-tube diodes. The accompanying illustration shows two equivalent rectifier circuits for the purpose of comparison and to establish the correct use of the semiconductor-diode symbol. (The small arrow adjacent to the load resistance indicates the direction of electron flow in the circuit.)

The terminal of the semiconductor diode (CR1), shown in part B, which corresponds to the cathode (or **filament)** of the electron-tube diode (Vi), shown in part A, is usually identified by a colored dot or band, or by a plus (+) sign, the letter "K", the schematic symbol, or other similar means of identification stenciled on the rectifier itself. The power supply circuits described in this section of the handbook and their associated schematics will use the serniconductordiode symbol in the same manner as shown in the circuit (part B) above.

**Reetifier Retings. The** use of one or a combination of several particular type semiconductor rectifiers in any given circuit is based upon the voltage and current requirements of the circuit. All semiconductor rectifiers are subject to certain voltage breakdown and current limitations; for these reasons the rectifier is usually rated in accordance with its ability to withstand a given peak-inverse voltage, its ability to conduct in terms of a maximum dc load current, or its working rnis (applied ac input) voltage.

The semiconductor rectifier has an extremely low forward resistance, and precautions are generally taken in the circuit design to ensure that the peakcurrent rating of the rectifier is not exceeded, especially if the rectifier is used with a capacitance-input filter. For this reason, a small value resistor, called a *surge resistor*, is frequently placed in series with the rectifier to limit the peak current through the rectifier; however, if there is sufficient resistance in the transformer winding (or the ac source), the series resistor is usually omitted. The series resistor, if used, can also be made to act as a fuse in the circuit. Typical values for the series resistor range from approximately 5 ohms for high-current rectifiers (200 milliamperes or greater) to approximately 50 ohms for low-current rectifiers (50 milliamperes or less). The series resistor is normally not necessary when the rectifier is used with a choke-input filter.

An ideal rectifier would have no (zero) resistance in the forward direction and infinite resistance in the reverse direction. (The electron tube approaches an ideal diode.) In commercially available semiconductor rectifiers, the forward resistance is very small and almost constant, but the reverse resistance is not as great as that of an electron-tube diode; however, the reverse resistance of the semiconductor rectifier can normally be neglected because it is generally so much greater than the associated load resistance. Under normal operating conditions, as long as the rectifier is not subjected to severe overload or otherwise abused, the rectifying action is very stable. The only effect of long use is a gradual increase in the forward resistance with age and, depending upon the rectifier type, a gradual increase in the amount of heat developed. An individual rectifier cell (or element) can withstand only a given peak-inverse voltage without breakdown or rupture of the cell; therefore, if higher peak-inverse voltages are to be sustained, a number of cells must be connected in series. Therefore, it is common practice to place many individual cells in series, or to "stack" several complete rectifier units, to obtain the desired characteristics and ratings necessary to withstand the peak-inverse voltage of the circuit without breakdown.

When rectifiers are placed in series (or stacked) to meet the voltage requirements of the circuit, the total forward resistance is increased accordingly. It is normal for this forward resistance to develop some heat; for this reason, many types of rectifiers are equipped with cooling fins or are mounted on "heat sinks" to dissipate the heat. These rectifiers are cooled by convection air currents or by forced-air. In some special applications, a large number of rectifiers may be incased in an oil-filled container to help dissipate heat. Similarly, just as rectifiers are placed in series to meet certain voltage requirements, they may also be placed in parallel to meet power (current) requirements; however, when rectifiers are operated in parallel to provide for an increased current output, precautions are usually taken to ensure that the parallel rectifiers have reasonably similar electrical characteristics.

Semiconductor Rectifier Circuit Analysis. As mentioned before, the rectifying action of a semiconductor diode is the same as that of an electron-tube

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diode; for this reason, the various power-supply circuits in this part of the handbook are described only briefly, especially where the basic circuit is the counterpart of the electron-tube circuit. Since many of the power-supply circuits are similar, much of the detailed theory of circuit operation can be omitted for the semiconductor version, because the rectifier action is identical with that given for the corresponding electron-tube circuit.

Semiconductor Rectifier Failure Analysis. Depending upon the semiconductor type, materials, and construction, a visual check of rectifier appearance may or may not reveal a defective rectifier. Since rectifier failure is not always accompanied by a change in physical appearance, an ohmmeter check or an electrical test may be necessary to determine whether the rectifier is damaged or defective. Improper rectifier operation may result from a change in the rectifier characteristics; that is, the rectifier can be open or shorted, its forward resistance can increase, or its reverse resistance can decrease.

An ohmmeter can be used to make a quick, relative check of rectifier condition. To make this check, disconnect one of the rectifier terminals from the circuit wiring, and make resistance measurements across the terminals of the rectifier. The resistance measurements obtained depend upon the test-lead polarity of the ohmmeter: therefore, two measurements must be made, with the test leads reversed at the rectifier terminals for one of the measurements. The larger resistance value is assumed to be the reverse resistance of the rectifier, and the smaller resistance value is assumed to be the forward resistance. Measurements can be made for comparison purposes using another identical-type rectifier, known to be good, as a standard. Two high-value resistance measurements indicate that the rectifier is open or has a high forward resistance; two low-value resistance measurements indicate that the rectifier is shorted or has a low reverse resistance. An apparently normal set of measurements, with one high value and one low value, does not necessarily indicate satisfactory or efficient rectifier operation, but merely shows that the rectifier is capable of rectification. The rectifier efficiency is determined by how low the forward resistance is as compared with the reverse resistance; that is, it is desirable to have as great a ratio as possible between the reverse and forward resistance measurements. However, the only valid check of rectifier condition is

a dynamic electrical test which determines the rectifier forward current (resistance) and reverse current (resistance) parameters.

#### SILICON-CONTROLLED RECTIFIERS

#### General.

The silicon-controlled rectifier is considered to be a PNPN device operating as a controlled switch. It has a low resistance in the forward direction when triggered, and **a** high resistance in the reverse direction. Once triggered, the amount of conduction is limited only by the impedance of the external circuit. In addition, it requires only a small amount of trigger current to initiate conduction. For example, a small current of 50 milliamperes, or less, can control currents from a few milliamperes up to hundreds of amperes. While the silicon-controlled rectifier is normally triggered by a current gate, it may also be turned on by exceeding the forward breakdown voltage. When the forward voltage is increased, the forward leakage current does not increase, or change, until the triggering point is reached. Once triggered, the controlled rectifier continues to conduct until the forward voltage is removed, reversed in polarity, or the holding current is reduced to a value which will no longer sustain conduction. There is also a value of reverse voltage which, when exceeded, will produce avalanche breakdown. Normally, the reverse breakdown voltage is high because of the inherent construction of the device, and is much greater than that of a conventional semiconductor diode.

Generally speaking, the silicon-controlled rectifier is the solid-state counterpart of the electron tube gasfilled thyratron rectifier. In this respect, the forward holding current corresponds to the minimum firing potential of the thyratron. It is important to note, that while the thyratron tube requires a grid firing voltage to cause conduction, the controlled rectifier requires current triggering to initiate conduction. Like most solid-state devices, the controlled rectifier is much smaller in size than a similarly rated thyratron tube.

**Controlled Rectifier Symbol.** The rectifying action of the controlled rectifier diode, when gated, is essentially the same as that discussed for the semiconductor diode discussed earlier in this section. The two equivalent rectifier circuits are shown in the accompanying illustration for the purpose of comparison, and to establish the correct use of the controlled

rectitler symbol. The **small** arrow, adjacent to the load resistance, indicates the direction of electron current flow in the circuit.



**Equivalent Rectifier Circuits** 

Siiicon-controlled rectifiers are manufactured in many sizes, from small lead-mounted types to large stud-mounted units. They may be obtained in positive or negative polarities (PNPN or NPNP). The positive type usually has the stud comected to the cathode and the braided heavy lead is connected to the anode. The negative type is connected inversely, with the stud connected to the anode, and the heavy braided lead to the cathode. The gate comection is aiways the smailer and thinner lead which protrudes from the stud. in lead-mounted types the cathode and anode pins are usually diametrically opposite, with the gate lead between them offset to the left. When installing or replacing units, comect them in accordance with the manufacturers' instruction sheets to avoid accidental reversai of connections.

Rectifier Rstings. The use of one, or a combination of severrd particular types of controlled rectifiers, in any given circuit is based upon the voltage and current requirements of the circuit. All controlled rectifiers are subject to specific voltage breakdown and current Jimitations. The rectifier is rated in accordance with its abiiity to withstand a maximum repetitive peak reverse voltage, which corresponds to the peak inverse voltage rating applied to transistors and diodes. It is also rated for maximum permissible dc load current, and for maximum working rms (appiied ac input) voltage. In addition, the controlled rectifier is also rated for a maximum value of peak forward **blocking** voltage, which will prevent the unit from conducting unless gated. The higher the bJocking voitage permitted, the higher the permissible controlled voltage. It is also necessary to exceed a certain minimum gate trigger voltage and current to make the rectifier conduct. There is a minimum holding current rating below which forward conduction ceases and blocking again occurs. It is usually necessary to apply the gating current for a short period (from approximately 5 to 15 microseconds) before conduction starts. That is, both the turn-on and turnoff operation are not instantaneous, but take finite intervals, depending upon the size and rating of the rectifier. Maximum turnoff time is approximately 50 microseconds. For example, in some types of rectifiers, without any gate appiied, the turn-off current may have ceassed for as much as 40 microseconds until the application of forward voltage again causes a flow of forward current. Once the maximum forward turn-off delay time is exceeded, a normal gate or a higher than rated forward blocking voltage is necessarv to turn on the controlled rectitler.

When the peak working voitage of the supply is greater than the rectifier rating, it is permissible to connect (stack) a number of controlled rectifiers in series, provided proper equalizing arrangements are made. The simplest arrangements are a series of equalizing resistors placed in shunt with the controlled rectifier. The more eiaborate arrangementsinclude series resistor-capacitor combinations, with the resistor shunted by a semiconductor diode. This combination eliminates transients and excessive starting current because of slight differences in ratings between similarly controlled rectifier units.. Likewise, when the current-carrying capability of a single control rectifier is insufficient, it is also possible to connect a group of controlled rectifiers in parallel. Compensation must be provided for any differences in forward resistance (or for current ratings and characteristics encountered as a result of production variations). Because of the number of current ratings available, it is seldom that more than two controlled rectifiers are paralleled. Cooling fins or heat sinks are available to ensure that the controlled rectifier is held within temperature ratings by means of convection cooiing. Use of the stud-type unit for currents above approximately 5 amperes enables the entire chassis to be used as a permanent low-cost heat sink.

**Circuit Operetion.** Operation of a PNPN semiconductor arrangement as used in the controlled rectitler is best visualized by connecting a pair of PNP and NPN transistors to form a regenerative feedback pair as shown in part B of the accompanying illustration.

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Transistor Analog of Controlled Rectifier

When a positive voltage is applied to the anode, junctions J1 and J3 (part A of the figure) are forward-biased, but since J2 is reverse-biased, current flow is blocked. Likewise, when a negative voltage is applied to the anode, junctions J1 and J3 are reversebiased, and although junction J2 is forward biased, current flow is also blocked. The biasing of J2 may be controlled by applying a positive voltage to the gate electrode. Let us assume now that a positive gate current is injected into the P2 layer shown in part A of the figure. In the two-transistor analog shown in part B of the figure, the increase in gate current causes an increase in the base current of transistor Q2. An increase in the base current of Q2 causes the emitter current of Q2 to increase. When the emitter current increases, the collector current of Q2 also increases. Since the collector of Q2 is connected to the base of Ql, an increase of collector current in Q2 causes an increase in the base current of Q1. The increased base current of O1 now increases the emitter current and also the collector current of Q1. Since the collector of Q1 is shown connected back to the base of Q2, an increase of Q1 collector current feeds back an increased base, or gate current, thus causing the base

current of Q2 to increase further. The feedback around this closed loop rapidly increases and is regenerative, so that even when the external gate is removed, both transistors are still driven rapidly into saturation. Thus, junction J2 is effectively forwardbiased by the insertion of the gate current. With all three junctions forward-biased, there is a high electron current flow from cathode to anode of the controlled rectifier and an extremely low forward resistance.

Once triggered, anode current will continue until the current falls below the holding current value. As the current falls below the holding value, the electrons and their positive counterparts called "holes" which were induced as charge carriers during the turn-on process decrease through recombination; the positive feedback ceases and the unit returns to its normally blocked state. At power frequencies, this relatively slow process is no problem. Particularly, since in ac circuits, the turnoff process is further assisted by the reverse half-cycle of voltage which helps sweep out the left-over carriers before blocking the next half-cycle. (When an SCR is used as a switch in dc circuits, for example as an inverter, some means must be provided to turn off the unit.) This is usually accomplished by reversing the voltage and causing the electrons and holes stored in the inner regions to diffuse toward J1 and J3. Thus a reverse current is produced in the external circuit. The voltage across the unit remains at about +0.7 volt until the reverse current ceases and junctions J1 and J3 enter the blocking state. Complete recovery, however, does not occur until the carriers remaining near the center junction, J2, are entirely removed by recombination; this takes a somewhat longer time. If sufficient J2 carriers are not combined, junctions J1 and J3 will conduct when forward-biased by the voltage applied during the forward blocking cycle, and cause false firing.

The accompanying figure shows the voltage and current characteristics of a typical silicon-controlled rectifier.

As shown on the figure, only a small reverse current flows over the reverse blocking region when a negative anode voltage is applied. When the reverse avalanche voltage is exceeded, a heavy reverse current flows. Over the gated region, a heavy forward current flows that is greater than the holding current. Over the forward blocking region, only a small (leakage) current flows; this does not change until the forward

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Controlled Rectifier V/I Characteristics

breakover voltage is reached, whereupon the SCR fries and a heavy forward current flows.

Failure Analysis. Since the silicon-controlled rectifier has a high resistance in both the forward and reverse directions until gated, the conventional forward-reverse-resistance diode check, usually made with an ohmmeter, will not give any indication of the condition of the controlled rectifier. Normally, the controlled rectifier will be either open or shorted. If the unit (when not gated) indicates a low forward resistance when checked with an ohmmeter, it definitely is defective. A high resistance reading in the reverse direction, preferably in the megohm region usually indicates low leakage current. However, this is only a relative test, since leakage current varies with different types of controlled rectifiers. The standard tube or diode tester cannot be used to test an SCR. However, there are a number of types of SCR testers available, ranging from precise laboratory types to practical portable types similar in size to a voltohmmeter. To determine the condition of an SCR, it is necessary to check the gate firing voltage and gate current, and to determine the anode to cathode leakage. It is also important to know the anode to gate leakage current, since excessive anode-gate leakage can cause self-triggering when the full anode to cathode voltage is applied during operation.

Although most electronic parts exhibit visible evidence of trouble, such as burned or discolored areas, the rugged construction of the silicon-controlled rectifier, to a large extent, makes the possibility of determining failure by visual inspection rather remote. In the absence of a suitable SCR tester, an oscilloscope can be used to determine that the proper firing waveform exists at the gate, and whether or not it is of sufficient amplitude. Usually the SCR will either fire normally, continuously, or erratically, or not at all. Any of these conditions maybe caused by a defective SCR, a faulty gate or gate circuit, or poor connections. Isolation of the trouble usually is reduced to making gate voltage and current measurements to determine that proper gating occurs.

## RECTIFIERS

#### General.

Rectifiers are used to convert an alternating current to a direct current to provide power required for operation of electrical and electronic equipment. Several types of rectifiers exist, and selection is based upon the requirements of the equipment it will sup ply; whether the equipment requires low or high voltage, low or high current, etc.

The dc output of a power supply can be either positive or negative, depending upon the circuit design, but it will always be a pulsating dc voltage (commonly referred to as *ripple voltage*). Filtering circuits are generally required at the rectifier output to reduce these pulsations to a pure or near-pure dc. These filter circuits are described in detail in the Filter section of this handbook. The different types of power supplies in use today are described briefly below.

#### **BASIC POWER SUPPLIES**

#### Half-Wave Rectifiers.

A half-wave rectifier power supply allows current to flow in the output only during the positive or negative half cycle of the input, as shown below:



In this example, the half-wave rectifier limits the negative half cycle of the input, as represented by the dashed lines in the output waveform.

The half-wave rectifier is the simplest in design and lowest in cost of all rectifiers. However, because of the low ripple frequency (same frequency as the input), the faltering required at the output must be of high quality. Additionally, the average output voltage is relatively low when compared to the input voltage; only half the applied power is passed to the load. This factor limits the half-wave rectifier to applications where the power required by the load is very low.

#### Full-Wave Rectifiers.

The full-wave rectifier power supply allows current to flow in the output during both the positive and negative half cycles of the input, as shown in the illustration below:



In this case, the output ripple voltage is positive; the negative half cycles of the input appear in the output as positive pulses. The output polarity can be reversed to produce negative pulsations by variations in circuit design.

Since the ripple frequency is twice the frequency of the input voltage, it is much easier to filter than the output of a half-wave rectifier. Also, since the frequency of the applied voltage is doubled, the average output voltage is much higher than the half-wave rectifier (given the same input signal) because much more of the applied power is passed to the load.

#### Full-Weve Bridge Rectifier.

**The** full-wave bridge rectifier passes the positive and negative halves of the applied voltage, just as the previously described full-wave rectifier. By utilizing the full secondary voltage of the input transformer instead of using a center tap, a full-wave bridge rectifier aquires the advantage of being able to deliver about twice the voltage of the full-wave rectifier.

#### **MULTIPHASE** POWER SUPPLIES

#### Multiphase Rectifiers.

Multiphase rectifiers are used in most applications where a power requirement of greater than 1 **killo**watt exists. The multiphase rectifier (sometimes called **polyphase**) uses a multiphase input, and rectifies each phase independently. The result is a single output voltage with a much smoother ripple (a higher ripple frequency) than the previously described rectifier circuits. The illustration below shows the input and output waveforms of a multiphase rectifier circuit.

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#### **VOLTAGE MULTIPLIER POWER SUPPLIES**

#### Voltage Multipliers.

Voltage multipliers are used to produce an output that is some multiple of the peak input line voltage. Voltage multipliers can be used for high voltage applications but the current delivering capability is very low. The voltage multiplier can produce any of a number of multiples of the input voltage; however, voltage regulation is generally poor. The greater is the multiplying factor, the poorer is the regulation, and the lower the proportion of current available to the load. The output voltage, as the previously discussed rectifier circuits requires filter circuits to smooth the pulsating dc output. These filter circuits are discussed in detail in the Filter section of this handbook.

#### **OC-TO-DC CONVERTERS**

#### General.

**The** de-to-de converter is used to convert a lowlevel dc voltage to a higher level dc voltage. They are especially useful in applications where the equipment, operates from a dc supply or a battery, or where extremely high dc voltage with low current is required. Basically, the low-level dc voltage is applied to an oscillator circuit which converts it to an ac voltage. This ac voltage is then stepped up through transformer action and applied to a rectifier or voltage multiplier circuit where it is converted back to a pulsating dc voltage that is a higher level than the input. The pulsating dc is then applied to a filtering circuit to smooth the dc pulsations to a constant dc voltage. These **filter** circuits are discussed in the Filter Section of this handbook.

#### ROTATING ELECTROMECHANICAL SYSTEMS

#### General.

The primary electrical power source in many small boats and aircraft is a 12- or 24-volt storage battery; the battery is kept in a charged condition by means of an engine-driven generator. The battery supplies the voltage for the engine ignition system, navigation lights, and other electrical loads. When cormnunications or similar electronic equipment is a part of the electrical load, an electromechanical-type power supply is frequently employed to supply high voltage for operation of the electronic equipment. In such cases, a rotating electromechanical device called a *dynamotor* is used to obtain high-voltage dc for operation of the electronic equipment, although a transistorized de-to-de converter or a vibrator-type power supply could also be used for the same purpose.

In some instances where the primary electrical power source is ac, an electromechanical device called a rotary converter is used to convert ac to dc. By definition, a rotary converter is a machine that changes electrical energy of one form to electrical energy of another form. A rotary converter can convert alternating current to direct current, or it can convert direct current to alternating current. It can also be used to change frequency and phase. In the normal sense, the rotary converter is a machine used to convert ac to dc; when it is used to convert dc to ac it is called an *inverter*, and is occasionally referred to as an *inverted converter*. When ac is available as the primary electrical power source, it is usually more efficient to use a power transformer and rectifier combination to obtain high-voltage dc than to use a rotary converter; for this reason, the application of

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rotary converters is limited. However, the rotary converter in another more common form, that of an inverter, is frequency used to convert dc to ac.

In naval aircraft, a source of alternating current is frequently required to power some of the instruments, electronic equipment, fluorescent lighting, etc. If the aircraft does not have an enginedriven ac primary power source (single-phase or polyphase), it is necessary to provide a means of changing the primary dc source to ac for use by the electrical load. In this application an inverter (one form of rotary converter) is used to change the dc to ac; the output of the inverter may be either single- or three-phase dc at a frequency which is normally 400 or 800 hertz.

From the brief discussion above, it can be seen that the dynamotor, rotary converter, and inverter are merely specialized combinations of motors and generators (or alternators). The detailed theory of operation and the construction of ac and dc motors, generators, and alternators are covered in Navy publications on basic electricity, and, therefore, will not be treated in this handbook. Ordy the basic principles will be discussed in this section of the handbook, as required, to provide a better understanding of the application and the failure anrdysis of the electromechanical devices discussed.

#### **VIBRATOR-TYPE POWER SUPPLIES**

#### General.

**The** primary electrical power source in many portable and mobile (small boats, light aircraft, and ground vehicles) electronic equipments is a storage battery. Vibrator-type power supplies are used to convert direct current from the storage battery to alternating current which can be rectified to furnish high-voltage for the operation of the equipment. Vibrator-type power supplies are designed for operation with specific input voltages; storage batteries having voltage values of 6, 12, or 24 volts are commonly used to operate this type of supply.

The main differences between a conventional power supply operating from an ac source and a vibrator power supply are the vibrating device used to convert the low dc voltage to high ac voltage and the special step-up power transformer used in conjunction with the vibrator. The vibrator itself is essentially a high-speed reversing switch that alternately opens and closes sets of contacts in the primary circuit of the power transformer. The rising and fatling magnetic field caused by the current pulses in the transformer primary induces an alternating square wave in the secondary circuit. The vibrator is designed to operate at a given frequency, usually between 60 and 250 hertz, although in some applications higher frequencies are employed.

Two basic vibrators are widely used in power supplies of this type; one is called the nonsynchronous (or *interrupter*) vibrator, and the other is called the synchronous (or self-rectifying) vibrator. The primary function of either type of vibrator is to cause the dc input current to flow in pulses through alternate halves of the transformer primary. The nonaynchronous vibrator requires the use of some form of highvoltage rectifier circuit to produce dc output from the supply. The synchronous vibrator does not require a separate rectifier circuit since, as the name synchronous (or self-rectifying) implies, the vibrator itself performs the additional function of rectifying the high-voltage ac it produces by synchronous switching of the transformer secondary winding; the resultant output voltage is essentially dc.

Occasionally, vibrator power supplies are designed to operate on more than one value of input voltage; this is accomplished by providing a number of taps on the transformer primary, and appropriate switching or terminrd points to accommodate the different battery voltages.

Several types of vibrator power supplies are capable of operation from both a low-voltage dc source and a conventional 60-hertz ac source. A"combination power supply of this type is usually equipped with a transformer having an additional primary winding for ac operation; the primary winding used for vibrator operation is tapped, and is used as the filament winding for the electron tubes when operating on ac. This type of power supply uses a non-synchronous vibrator and a separate rectifier circuit, since the same high-voltage secondary is used for both ac and dc operation.

Another combination ac and vibrator powersupply design uses two separate power transformers, with independent rectifiers in the vibrator circuit and in the ac input circuit. These two independent power-supply circuits share a common **filter** circuit to falter their respective dc outputs; either of the two input circuits is selected by a switching arrangement, depending upon whether dc input or ac input operation is desired.

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Although there are other circuit arrangements for providing operation from both ac and dc input sources, the examples given above are typical. One other combination vibrator supply which is occasionally employed makes use of two vibrator supplies operating from a common dc input but with two or more output voltages. The outputs of the combined supplies can be either positive or negative, or both, and of different voltage values. Any of the conventional electron-tube or semiconductor rectifier circuits, such as the half-wave, full-wave, bridge, and voltage doubler, can be used in nonsynchronous vibrator power supplies. The use of semiconductor rectifiers simplifies the design of nonsynchronous vibrator-type power supplies, since no **filament** voltage is required for the rectifier(s).

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### PART 2-1. BASIC POWER SUPPLY CIRCUITS

## SINGLE-PHASE, HALF-WAVE RECTIFIER (ELECTRON TUBE)

#### Application.

**The** single-phase, half-wave rectifier is used in all types of electronic equipment for applications requiring high-voltage dc at a low load current. The rectifier circuit can be arranged to furnish negative or positive high-voltage output to the load.

#### Charrrctaristics.

Input to circuit ia ac; output is pulsating dc.

Uses high-vacuum or gas-filled electron-tube diode as rectifier.

Output requires filtering; dc output ripple frequency is equal to primary line-voltage frequency.

Haa poor regulation characteristics.

Circuit provides either positive- or negative-Polarity output voltage.

#### Circuit Analysis.

**General.** '**lhe** single-phase, half-wave rectifier is one of the simplest types of rectifier circuits. The circuit consists of a rectifier (diode) in series with the alternating source and the load. Since the rectifier conducts in only one direction, electrons flow through the load and through the rectifier once during each complete cycle of the impressed voltage. Rectifier conduction occurs only during the interval of time the plate is positive with respect to the filament (cathode). Thus, the electrons flow through the load in pulses, one puke for each positive half cycle of the impressed voltage.

**Circuit Operation.** In the accompanying circuit schematic, parts A and B illustrate an electron-tube diode, VI, used in a basic single-phaae, hrdf-wave rec**tifier** circuit. The circuit given in part A uses a single transformer, TI, to step up the alternating-source voltage to a high value in the secondary. The fdament of the tube, V1, is operated from a low-voltage secondary winding located on the same core and connected to the high-voltage winding. The circuit given in part B ia shown with two separate transformers; T1 is a step-up transformer to obtain high voltage, and T2 is a stepdown transformer to obtain the correct fdament voltage for the operation of V1. Although separate transformers are shown in part B, the lowvoltage secondary of T2 could just as well be wound on the core of transformer T1. However, the highand low-voltage secondary windings must be adequately insulated from one another to allow the simultaneous application of plate and fdament voltages to the tube.

In the two circuits illustrated, either terminal of the load may be placed at ground potential, depending upon whether a positive or negative dc output is desired. The circuit illustrated in part A is commonly used as a negative high-voltage supply with the positive terminal of the load connected to ground (chassis); the circuit illustrated in part B is commonly used as a positive high-voltage supply with the negative terminal of the load connected to ground.





Basic Single-Phase, Hatf-Wave Rectifier Circuits

The operation of a half-wave rectifier circuit cars be understood from the waveforms given in the accompanying illustration.

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In part A, the  $F_{-}$ [ $I_{-1}$  characteristic curve for the rectifier is given. When high-voltage a. is applied to the rectifier circuit, electrons flow through the tube and the load whenever the plate is positive with respect to the **filament** or cathode; the amount of current is determined by the characteristic curve of the tube. Part A of the illustration shows that for each positive half cycle of the applied voltage, a current puke passes through the rectifier, the load, and the secondary winding of the transformer, TI. For each negative half cycle of the applied voltage, the plate is negative with respect to the filament or cathode and no current pulse is obtained. Thus, the electrons flow through the load circuit in pukes, to



Waveforms for Half-Wave Rectifier Circuit

produce a pulsating current waveform as shown in part A of the illustration.

In part B of the illustration, voltage waveforms for the half-wave rectifier circuit are given. The primary winding of transformer T1 is connected to an ac source, represented as waveform e<sub>ni</sub>. The transformer, TI, increases the primary voltage to a higher value in the secondary winding by step-up transformer action. The purpose of the small secondary winding of T1 (or T2) is to supply voltage to the filament of rectifier tube V1. The alternations of the ac source, e<sub>pri</sub>, are applied to the primary of the transformer and induce a voltage, esec, in the secondary winding of the transformer. The waveform illustration shows a 180degree change in phase between the primary  $(e_{pri})$  and secondary  $(e_{e_{cc}})$  voltages because of transformer action and the fact that the secondary-output voltage is an induced voltage. Since the transformer is a step-up transformer, the amplitude of the secondary voltage,  $e_{sec}$ , is greater than the applied primary voltage, epri. The induced secondary voltage, sec, is applied across the rectifier and the load. On positive half cycles of  $e_{sec}$ , current passes through the rectifier and the load resistance, producing an output voltage, e, across the load resistance. The output voltage e, has a pulsating waveform which results in an irregularly shaped ripple voltage; the frequency of the ripple voltage is the same as the frequency of the ac source. Because the output voltage and current are not continuous, the half-wave rectifier circuit requires considerable filtering to smooth out the ripple and produce a steady dc voltage.

The half-wave rectifier utilizes transformer T1 during only one half of the cycle; therefore, for a given transformer less power can be developed in the load than could be developed if the transformer were utilized for both halves of the cycle. Thus, if a considerable amount of power is to be developed in the load, the half-wave transformer must be relatively large compared with a transformer in which both halves of the cycle are utilized. This disadvantage limits the use of the transformer-type half-wave rectifier circuit to applications which require a relatively small load current. Since the dc load current passes through the secondary winding in only one direction, the laminated-iron core of the transformer tends to become magnetized. This effect is called *dc core* saturation and reduces the effective inductance of the transformer. The net effect inductance with the dc
core saturation effect present is known as *transformer incremental inductance*. Thus, transformer incremental inductance is reduced as the dc load current is increased. The resultant effect is to decrease the primary counter emf to a greater degree and thereby **increase** the load component of primary current. Therefore, the efficiency of the transformer is reduced, and the regulation of the circuit is impaired.

The half-wave rectifier, assuming half sine waves as the waveform for the output voltage,  $e_0$  (unfiltered), produces the following root-mean-square voltage:

$$E_{\rm rms} = \frac{E_{\rm max} \times 0.707}{2}$$

where:  $E_{max}$  = maximum instantaneous voltage. The corresponding average output voltage is:

$$E_{av} = 0.45 E_{ms}$$

Similarly, the root-mean-square and average output currents can be expressed as:

$$I_{\rm rms} = \frac{I_{\rm max} \times 0.707}{2}$$

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and:

The *peak inverse voltage* of a rectifier tube is defined as the maximum instantaneous voltage in the direction opposite to that in which the rectifier is &signed to pass current. The peak inverse voltage across the rectifier in a half-wave rectifier circuit **during** the period of time that the tube is nonconducting is approximately 2.83 times the rms value of the transformer second@ voltage. The peak inverse voltage can be expressed as:

$$E_{inv} = 2.83 E_{rms}$$

where:  $E_{,m}s = transformer secondary$ (or applied) voltage

The output of the rectifier circuit is connected to a suitable filter circuit, to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.)

#### Failure Amlysis.

**No Output.** In the half-wave rectifier circuit, the **no-output** condition is likely to be limited to one of three possible causes: a defective rectifier tube (open **filament**), the lack of applied ac voltage, or a shorted load circuit (including shorted filter-circuit components).

A visual check of a glass envelope rectifier tube can be made to determine whether the **filament** is lit; if the filament is not lit, it may be open or the **fila**ment voltage may not be applied. The tube **filament** should be checked for continuity; also, the presence of correct **filament** voltage at the tube socket should be determined by measurement.

The ac secondary voltage,  $\mathbf{e}_{sec}$ , should be measured at the terminals of transformer T1 to determine whether the voltage is present and of correct value. If necessary, measure the applied primary voltage,  $\mathbf{e}_{pri}$ , to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity (resistance) measurements of the primary and secondary windings should be made to determine whether one of the windings is open, since an open (discontinuity) in either winding will cause a lack of secondary voltage. Also, continuity measurements should be made between each transformer secondary terminal and the corresponding tube socket or load terminal to determine whether either one of these two leads is open.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including the filter, is shorted. If the filter circuit incorporates an electrolytic capacitor, the resistance measurements made across the output of the rectifier circuit may vary depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the circuit test points for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value. A short in the components of the filter circuit or in the load will cause an excessive load current to flow. If the rectifier tube is a high-vacuum type, the heavy load current will cause the plate to become heated and emit a reddish glow when the plate dissipation is exceeded and, if allowed to continue, may

result in permanent damage to the tube. If a gas-fflled rectifier is used in the circuit, a heavy current overload will likely result in damage to the tube, because gas-fflled rectifiers are more susceptible to damage from current overload than are high-vacuum rectifiers.

Low Output. The rectifier tube should be checked to determine whether the cause of low output is low filament emission. The load current should be checked to make sure that it is not excessive, because the half-wave rectifier circuit has relatively poor regulation and a decrease in output voltage can be caused by an increase in load current (decrease in load resistance). Also, the ac secondary voltage,  $e_{sec}$ , and the primary voltage, epri, should be measured at terminrds of transformer TI to determine whether these voltages are present and of the correct value. Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. Shorted turns are not easily detected by resistance measurement; a voltage measurement is a more reliable indication. If the transformer losses (due to shorted turns) are excessive, the transformer may also become overheated. Another check to determine whether the transformer is defective is to disconnect the secondary load(s) and measure the primary current with the transformer unloaded; excessive primary current is an indication of shorted turns. Still another check is to disconnect all primary and secondary leads from the transformer terminals and make measurements between the individual windings and the core, using an ohmmeter or a Megger (insulation tester), to determine whether any of the windings are shorted to the core or to the Faraday shield (noise-reduction shield between primary and secondary).

# SINGLE-PHASE, HALF-WAVE RECTIFIER (SEMICONDUCTOR)

#### Application.

The single-phase, half-wave rectifier is sometimes used in electronic equipment for applications requiring a dc output voltage from an ac source. It is frequently used in "transformerless" circuits where the load current is small and voltage regulation is not critical and also where small space, light weight, high efficiency, mggedness, and long life are important considerations. The circuit is often employed as the power supply in small receivers and audio amplifiers. It is also used in low-voltage battery chargers and in some equipment applications, as a bias supply. The rectifier circuit can be arranged to furnish either negative or positive dc output to the load.

### Characteristics.

**Same** characteristics as electron tube version, with following exceptions:

Uses semiconductor diode instead of electron tube.

Depending upon application, it may be used with or without a power or isolation transformer.

#### Circuit Analysis.

General. The single-phase, half-wave rectifier is the simplest type of rectifier circuit. It consists of a semiconductor rectifier (diode) in series with the alternating source and the load. Since the rectifier conducts in only one direction, electrons flow through the load and through the rectifier once during each complete cycle of the impressed voltage. Thus, the electrons flow through the load in pulses, one pulse for every other half cycle of the impressed voltage.

Circuit Operation. In the accompanying circuit schematic, parts A and B illustrate a semiconductor diode, CR1, used in two variations of a basic singlephase, half-wave rectifier circuit. These two circuit variations use a transformer, TI, as an isolation transformer or to step up the alternating-source voltage to a higher value in the secondary. The use of a transformer in this circuit permits either dc output terminal to be placed at ground (chassis) potential. The two circuit variations shown in parts C and D do not use a transformer, but operate directly from the ac source. Both circuits shown in parts C and D place one side of the ac source at a dc potential, and thus restricts the output of the supply to either a positive dc potential (part C) or a negative dc potential (part D)

In the four circuits illustrated, the function of semiconductor diode CR1 is the same for each circuit. However, because of the manner in which the diode is placed in the circuit, electrons flow through the load in the direction indicated by the arrow adjacent to the load resistance. The dc output polarity for each circuit is indicated by the signs associated with the load resistance. The triangle in the graphic symbol for diode CR1 points in the direction of current flow

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**Basic Half-Wava Rectifier Circuits** 

according to conventional (positive-to-negative) current theory; electron flow is in the opposite direction. The letter "K" assigned to one terminal of the graphic symbol for CR1 indicates that this terminal corresponds to the cathode (filament) of a electrontube diode. Therefore, the terminal represented by the solid-arrow portion of the graphic symbol corresponds to the plate of an electron-tube diode.

Each of the four circuits shows a resistor, RS, in series with the semiconductor dio&. This resistor, called the surge *resistor*, limits the peak current through the rectifier to a safe value. The value of resistor Rs is influenced by the circuit design; determination of its value includes the consideration of several other factors, such as the applied ac voltage, the resistance of the load circuit, the filter-circuit input capacitance, and the peak current rating of the semiconductor diode. If there is **sufficient resistance** in the secondary winding of transformer T1 (shown in parts A and B) or in the ac source (parts C and D), the resistor may be omitted; also, if the load circuit of the supply includes a choke-input filter, the resistor may be omitted.

The operation of the half-wave rectifier circuit can be understood from the simplified circuits, parts A and B, and the waveforms, part C, shown in the accompanying illustration.

Assume that the ac voltage applied to the input terminals of the rectifier circuit **during** the initial



Typical Half-Wave Ractifier Circuit Operation and Waveforms

half-cycle has the polarity indicated in part A of the illustration. Electrons flow in the direction indicated by the small arrows from the lower (negative) input terminal, through the load, through rectifier CR, and to the upper (positive) input terminal. Thus, during the initial half-cycle, rectifier CR passes maximum current in the forward direction, and an output voltage is developed across the load resistance. In other words, when the rectifier conducts, electrons pass through the load to develop a corresponding output-voltage pulse, as shown in part C of the illustration.

During the next half-cycle, the polarity of the applied ac input is as indicated in part B of the illustration. Except for possibily a very small value of reverse current, the rectifier does not conduct, the reverse resistance remains high, and the small current which flows can be neglected. (Normally, the reverse resistance of the rectifier is extremely high as compared with the circuit load resistance.) Thus, during the second half-cycle, no voltage is developed across

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the load resistance. In other words, because the rectifier is nonconducting and no electrons pass through the load, there is no output from the circuit.

The waveforms given in part C show that, on positive half cycles of the applied voltage, current passes through the rectifier and the load resistance, producing an output voltage across the load resistance. The output voltage has a pulsating waveform, which results in an irregularly shaped ripple voltage; the frequency of the ripple voltage is the same as the frequency of the ac source. Since the output voltage and current are not continuous, the half-wave rectifier circuit requires considerable filtering to smooth out the ripple and produce a steady dc voltage.

The peak *inverse voltage* of the semiconductor rectifier is defined as the maximum instantaneous voltage in the direction opposite to that in which the rectifier is designed to pass current. Assuming the output of the supply to be filtered, the peak inverse voltage across the rectifier in a half-wave rectifier circuit during the period of time the rectifier is nonconducting is approximately 2.83 times the rms value of the applied (or transformer secondary) voltage.

The output of the half-wave rectifier circuit is connected to a suitable falter circuit, to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.) Because of the very low forward resistance of the semiconductor rectifier and its associated low internal-voltage drop which is practically independent of load current, the half-wave power supply (including falter and load) using a semiconductor diode will have somewhat better regulation characteristics that the equivalent electron-tube circuit; however, the regulation is still considered to be relatively poor.

#### Failure Analysis.

**No Output.** In the half-wave rectifier circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of an open series resistor Rs or a defective transformer), a defective rectifier, or a shorted load circuit (including shorted falter-circuit components).

The ac supply voltage should be measured at the input of the circuit to determine whether the voltage

is present and is the correct value. If the circuit uses a step-up (or isolation) transformer, measure the voltage at the secondary terminals to determine whether it is present and is the correct value. If necessary, the primary voltage should be removed from the transformer and continuity measurements of the primary and secondary windings made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

If the circuit includes a series resistor (Rs), a resistance measurement can be made to determine whether the resistor is open. However, if the resistor is found to be open, the rectifier and load circuit should be checked further to determine whether excessive load current or a defective rectifier has caused the resistor to act as a fuse and to open.

With the ac supply voltage removed from the input of the circuit and with the load disconnected from the rectifier, resistance measurements can be made across the load to determine whether the load circuit (including falter components) is shorted.

Although physical appearance is not a positive indication of condition, the rectifier may be given a visual check for a change in physical appearance which can indicate rectifier failure. A relative check of the rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. However, failure of the rectifier may be the result of other causes; therefore, additional tests of the filter and load circuit are necessary.

Low Output. The rectifier should be checked to determine whether the low output is due to normal rectifier aging. A relative check of the rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will become excessive.

The load current should be checked to make sure that it is not excessive, because the circuit has relatively poor regulation and an appreciable increase in load current (decrease in load resistance) can cause a decrease in output voltage. **Also**, the filter circuit components should be suspected as a possible cause of low output.

# SINGLE-PHASE, FULL-WAVE RECTIFIER (ELECTRON TUBE)

#### Application.

**The** single-phase, MI-wave rectifier is commonly used in all types of electronic equipment for applications requiring high-voltage dc at a relatively high load current. The rectifier circuit can be arranged to furnish negative or positive high-voltage output to the load.

#### Characteristics.

Input to circuit is ac; output is pulsating dc.

Uses two high-vacuum or gas-filled electron-tube diodes as rectifiers, or one twindiode rectifier.

Output requires filtering; dc output ripple frequency is twice the primary line-voltage frequency.

Has good regulation characteristics.

Circuit provides either positive- or negative-polarity output voltage.

Uses power transformer with center-tapped, high-voltage secondary winding.

### Circuit Analysis.

General. The single-phase, full-wave rectifier is the most common type of rectifier circuit used in electronic equipment. The circuit consists of a highvoltage transformer with a center-tapped secondary winding. One plate of the rectifier tube (s) is connected to one end of the transformer secondary, and the other plate is connected to the other end. The load is connected between the center-tap of the secondary winding and the filament (cathode) of the rectifiers (s). Since the secondary winding is centertapped, the voltage developed in each half of the secondary winding is in series with the other half; therefore, only one rectifier plate is positive at any instant. As a result, electrons flow through one half of the secondary winding, the load, and a rectifier diode on each half cycle of the impressed voltage, with first one diode conducting then the other. Thus, the electrons flow through the load in pulses, one pulse for each half cycle of the impressed voltage.

**Circuit Operation.** In the accompanying circuit schematic, part A illustrates a "full-wave" twin-diode rectifier, VI, used in a basic single-phase, full-wave rectifier circuit. The rectifier circuit uses a single transformer, Tl, to step up the alternating-source voltage to a high value in each half of the secondary

winding. The **filament** of tube V1 is operated from a low-voltage secondary winding located on the same transformer core with the high-voltage secondary. The low-voltage secondary winding is center-tapped and is the mid-point of the filament (cathode) circuit to which the load is comected. The circuit given in part A is typical of plate-voltage and bias supplies designed to meet medium power requirements such as those found in communication receivers and transmitters, audio amplifiers, radar sets, etc.



Basic Single-Phase, Full-Wave Rectifier Circuits

The rectifier circuit given in part B is shown with two separate transformers; T1 is a step-up transformer to obtain high voltage in each half of the secondary winding, and T2 is a step-down transformer to

obtain the correct filament voltage for the operation of the two rectifiers, VI and V2. The circuit is fundamentally the same as that given in part A. The separate transformer arrangement permits the primary voltage to be applied to transformer T2 independent of, the prior to, the application of primary voltage to T1 so that the rectifier filaments may be heated to the normrd operating temperature before the plate voltage is applied. Although provision for a time delay in the application of plate voltage is not too important in the case of high-vacuum rectifiers, a time interval to permit preheating of the filament is usually necessary for gas-filled rectifiers. The circuit arrangement given in part B is typical of high-voltage, dc supplies designed for use in radar sets and communication transmitters.

In the two circuits illustrated, either terminal of the load may be placed at ground potential, depending upon whether a positive or negative dc output is desired.

The operation of a full-wave rectifier circuit can be understood from the simplified circuit schematics (parts A and B) and the waveforms (part C) given in the accompanying illustration.

This circuit requires two rectifier diodes and a transformer with a center-tapped secondary winding. Each end terminal of the secondary winding (terminals A and C) is connected to a rectifier plate, as shown in the simplified circuit schematic. Since only one half of the secondary winding is in use at any one time, the totrd secondary voltage ( $e_{sec}$ ) must be twice the voltage that would be required for use with a half-wave rectifier circuit (previously described).

The part' of the secondary winding between terminals A and B,  $(e_{pl})$  shown in the schematic of part A, may be considered a voltage source that produces a voltage of the polarity given in the illustration. This voltage is applied in series with the load resistance between the plate and cathode of the rectifier, V1. During one half cycle, time interval *a* (part C of the illustration), the plate of VI is positive with respect to its cathode; therefore, electrons flow in the direction indicated by the arrows on the schematic of part A. Thus, during the time intervrd *a*, *an* output voltage is developed across the load resistance. Also during this half cycle, the voltage produced across the part of the secondary winding between terminals B and C  $(e_{n2})$  is negative; therefore, the plate of V2 is negative with respect to its cathode, and V2 is nonconducting.



Simplified Full-Wave Rectifier Circuit and Waveforms

During the next half cycle, time interval **b** (part C  $\checkmark$  of the illustration), the polarity of the voltage is reversed. The part of the secondary between terminals B and C  $(e_{p2})$ , shown in the schematic of part B, produces a voltage of the polarity given in the illustration. This voltage is applied in series with the load resistance between the plate and cathode of the rectifier, V2. During time interval b (part C of the illustration), the plate of V2 is positive with respect to its cathode, and electrons flow in the direction indicated by the arrows on the schematic of part B. Thus, during time interval **b**, an output voltage is developed across the load resistance. Also, during this half cycle, the voltage produced across the part of the secondary winding between terminals A and B  $(e_{p1})$  is negative and, therefore V1 is nonconducting. From the waveforms given in part C, it can be seen that only one rectifier conducts at any instant of time; thus, on alternate half cycles, electrons flow through the load resistance to produce a pulsating output voltage, e.. This output voltage has a pulsating waveform which results in an irregularly shaped ripple voltage because the output voltage and current are not continuous; the frequency of the ripple voltage is twice the frequency of the ac source. The full-wave rectifier circuit requires filtering to smooth out the ripple and produce a steady dc voltage.

> The full-wave rectifier circuit utilizes the transformer (Tl) for a greater percentage of the input cycle than the half-wave rectifier, because there are two pulsations of current in the output for each complete cycle of the applied alternating voltage. Therefore, the full-wave rectifier circuit is more efficient, has less output ripple amplitude, and has better voltage regulation than the half-wave rectifier circuit. The dc load current passes through each half of the secondary winding on alternate half cycles, flowing in opposite directions in each half of the winding. Since the windings are electrically equal (ampere turns) to one another, the current passes first in one direction for one half of the secondary winding and then in the other direction for the other half; thus, there is no tendency for the transformer core to become permanently magnetized. Furthermore, since little dc core saturation occurs, the effective inductance of the transformer remains relatively high. As a result, the transformer has much higher efficiency than the transformer used in a half-wave rectifier circuit.

> The full-wave rectifier, assuming a series of half sine waves as the waveform for the output voltage e.

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(unfiltered), produces the following root-mean-square voltage:

$$E_{rms} = E_{max} \ge 0.707$$

where:  $E_{max}$  = maximum instantaneous voltage The corresponding average output voltage is:

$$E_{av} = 0.9 E_{,m}s$$

Similarly, the root-mean-square and average output currents can be expressed as:

and:  $I_{rms} = 1_{max} \ge 0.707$  $I_{av} = 0.9 I_{m},$ 

The *peak inverse voltage* across a rectifier in a fullwave rectifier circuit during the period of time the tube is nonconducting is approximately 2.83 times the rms voltage across half of the transformer secondary, or 1.41 times the rms voltage across the entire secondary. The peak inverse voltage can be expressed as:

$$E_{inv} = 2.83 E_{inv}$$

where:  $E_{rms} = rms$  voltage across half of transformer secondary

or, 
$$E_{inv} = 1.41 E_{rms}$$

where: E<sub>rms</sub> rms voltage across entire transformer secondary

The output of the full-wave rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in part D of this section.)

# Failure Analysis.

**No Output.** In the full-wave rectifier circuit the no-output condition is likely to be limited to one of three possible causes: defective rectifier tube or tubes (open filaments), the lack of applied ac voltage, or a shorted load circuit (including shorted falter-circuit components).

A visual check of glass-envelope rectifier tube (s) can be made to determine whether the filament is lit; if the filament is not lit, the filament of the tube is likely to be open or the filament voltage may not be applied. The tube filament(s) should be checked for continuity; the presence of correct filament voltage at the tube socket should be determined by measurement.

The ac secondary voltage applied to each rectifier plate should be measured between the secondary center-tap and each rectifier plate to determine whether voltage is present and of the correct value. If necessary, measure the applied primary voltage to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity (resistance) measurements of the primary winding should be made to determine whether the winding is open, since an open (discontinuity) in the primary winding will cause a lack of secondary voltage.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including filter, is shorted. If the filter circuit incorporates an electrolytic capacitor, the resistance measurements made across the output of the rectifier circuit may vary depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the circuit test points for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value. A short in the components of the fiiter circuit or in the load will cause an excessive load current to flow; if the rectifier-tube type is a high-vacuum type, the heavy load current will cause the plate to become heated and emit a reddish glow when the plate dissipation is exceeded, and, if allowed to continue, may result in permanent damage to the tube. If a gas-filled rectifier is used in the circuit, excessive load current will likely result in damage to the tube because gasfilled rectifiers are more susceptible to damage from current overload than are high-vacuum rectifiers.

Low Output. The rectifier tube(s) should be checked to determine whether the cause of low output is low filament emission. Also, since the full-wave rectifier circuit normally supplies current to the load on each half cycle, failure of either rectifier or an open in either half of the secondary winding will allow the circuit to act as a half-wave rectifier circuit, and the output voltage will be reduced accordingly. Furthermore, whenever this occurs, the ripple amplitude will also increase, and the ripple frequency will be that of the ac source (instead of twice the source frequency). In the case of two separate rectifier tubes, if one tube is lit and the other is not, the trouble is obviously associated with the tube that is not lit.

With the primary voltage removed from the circuit, resistance measurements can be made to check the continuity between the center-tap and each rectifier plate; this will determine whether one of the  $\checkmark$ windings or plate leads is open. As an alternative, the ac secondary voltage applied to each rectifier plate can be measured between the secondary center-tap and each rectifier plate to determine whether both voltages are present and are of the correct value.

The primary voltage should be measured to determine whether it is of the correct value, since a low applied primary voltage can result in a low secondary voltage. Also, shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. Shorted turns are not easily detected by resistance measurement t; a voltage measurement is a more reliable indication. If the transformer losses (due to shorted turns) are excessive, the transformer may also become overheated. Another check to determine whether the transformer is defective is to disconnect the secondary load(s) and measure the primary current with the transformer unloaded; excessive primary current is an indication of shorted turns. Still another check is to disconnect all primary and secondary leads from the transformer and make measurements between the individual windings and the core, using an ohmmeter or a Megger (insulation tester), to determine whether any of the windings are shorted to the core or to the Faraday shield (noise-reduction shield between primary and secondary).

The rectifier-output current (to the filter circuit and to the load) should be checked to make sure that it is within tolerance and is not excessive. A lowoutput condition due to a decrease in load resistance would cause an increase in load current; for example, excessive leakage in the capacitors of the filter circuit would result in increased load current.

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# SINGLE-PHASE, FULL-WAVE RECTIFIER (SEMICONDUCTOR)

### Application.

The single-phase, full-wave rectifier is commonly used in all types of electronic equipment for applications requiring high- or low-voltage dc at a relatively high load current. The rectifier circuit can be arranged to furnish negative or positive output to the load.

# Characteristics.

**Same** characteristics as electron tube version, except it uses two semiconductor rectifiers instead of electron tubes.

# Circuit Analysis.

General. The single-phase, full-wave rectifier is one of the most common types of rectifier circuits used in electronic equipment. It may be used as a low-voltage dc supply for operation of relays, motors, electrontube filaments, telephone and teletype circuits, and semiconductor circuits, or as a high-voltage dc supply for operation of electron-tube circuits. The full-wave rectifier circuit consists of a transformer with a center-tapped secondary winding. At least two semiconductor diodes are used in the circuit; one diode is connected to one end of the transformer secondary, and the other diode is connected to the other end. The load is connected between the center tap of the secondary winding and the common junction of the two semiconductor diodes. Since the secondary winding is center-tapped, the voltages developed in the two halves of the secondary winding are in series with each other; therefore, only one rectifier is conducting at any instant. As a result, electrons flow through one half of the secondary winding, the load, and a rectifier on each half cycle of the impressed voltage, with first one diode conducting and then the other. Thus, the electrons flow through the load in pukes, one puke for each half cycle of theirnpreaaed voltage.

**Circuit Operation.** In parts A and B of the accompanying circuit schematic, two semiconductor diodes, CR1 and CR2, are used in a basic single-phase, fuU-wave rectifier circuit. Although the schematic shows only two diodes in the circuit, in some instances for high-voltage operation each diode symbol represents two or more diodes in series to obtain the necessary peak-inverse characteristics.



Basic Single-Phase, Full-Wave Rectifier Circuits

The circuit uses a single transformer, T1, either to step up the alternating-source voltage to a higher value in each half of the secondary winding or to step down the voltage to a lower value. The circuit application and the values of the input and output voltages determine whether a step-up or stepdown transformer is used.

The series, or surge, resistor ( $\mathbf{R}_s$ ) is generally required only in high-voltage supplies. Its function is to limit the peak current that can flow through the semiconductor rectifiers. When power is applied to the circuit, the input capacitor (in the falter circuit) is in a **discharged** condition. Avery heavy current flows initially to establish the charge on this capacitor. The limiting action of.  $\mathbf{R}_s$  prevents any damage to the rectifiers, which would otherwise occur from the large surge of charging current. For 380-volt (peak inverse) rectifiers, the value of  $\mathbf{R}_s$  is between 1 and 50 ohms, depending on the peak current rating of the unit. The

resistor is common to both rectifiers since it is placed in the circuit between the transformer center tap and the load. A variation of this design practice uses two resistors, one resistor in series with each rectifier.

The circuit arrangement given in part A is typical of many plate- and low-voltage (positive) supplies. The circuit given in part B is typical for bias supply applications requiring a negative voltage. In the basic circuits illustrated, either terminal of the load may be placed at ground potential, depending upon whether a positive or negative dc output is desired. When the dc output terminal associated with the transformer center tap is grounded, the secondary-to-core insulation need not be as great as it **would be** if the secondary winding were above ground by the amount of the dc output voltage. For this reason, the two circuits shown in parts A and B are the commonly used circuits, and do not require that special design consideration be given to the secondary-winding insulation.

In parts A and B of the accompanying illustration, the voltage induced in each half of the secondary of transformer T1 causes each diode to conduct on alternate half-cycles of the input voltage. Two dc pulses are thus produced during each complete cycle of ac input voltage. Hence, the output has a frequency which is twice the input frequency. Because of this, the full-wave circuit is more efficient, has better voltage regulation, and has an output which is easier to falter (with a higher average value than that of the half-wave circuit).

As an example of the peak and average voltages obtained from the full-wave rectifier circuit, assume that **transformer** T1 in part A of the illustration has a step-up ratio of 1 to 6. Then, with an applied input voltage of 115 volts, 690 volts will appear across the secondary winding, and 345 volts will be applied to each diode. Since only one-half of the secondary is used at a time, the peak voltage is found by using half of the voltage across the winding, or 345 volts. From the peak voltage formula:

$$\mathbf{E_{peak}}^{=}$$
 1.414 x  $\mathbf{E_{rms}}$   
= 1.414x 345

= 488 volts (approx)

This is the peak value of the output voltage for halfwave (single-phase) rectification. Since two pukes are produced for every cycle of ac input voltage in **full**wave rectification, the average value of the dc output voltage will be greater than that for half-wave rectification; thus:

$$\mathbf{E_{av}} = \mathbf{E_{peak}} \times \frac{2}{\pi}$$
  
= 4 8 8 ° m  
= 310 volts (approx)

In a full-wave rectifier circuit designed to furnish high-voltage dc to the load, the peak-inverse voltage rating of the semiconductor rectifier is an important consideration.

The peak-inverse voltage across a semiconductor rectifier in a full-wave circuit during the period of time it is nonconducting is approximately 2.83 times the rms voltage across half of the transformer secondary  $(e_{sec})/2$ , or approximately 1.41 times the rms voltage across the entire secondary  $(e_{sec})$ . For high-voltage applications, several identical-type rectifiers may be placed in series or stacked to withstand the peak-inverse voltage and avoid the possibility of rectifier breakdown. Generally, whenever a single rectifier unit is used in the full-wave circuit, it is chosen to have a peak-inverse voltage rating which is conservative and thus provide a safety factor.

Because of the very low forward resistance of the semiconductor rectifier and its low internal-voltage drop which is practically independent of load current, the full-wave power supply using semiconductor diodes has regulation characteristics which approach or equal those of the equivalent electron-tube circuit using mercury-vapor rectifiers. Hence, its regulation characteristics are somewhat better than those of the electron-tube circuit which uses high-vacuum rectifiers.

#### Failure Analysis.

**No Output.** In the full-wave rectifier circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of a defective transformer), defective rectifiers, or a shorted load circuit (including shorted filter-circuit components).

The ac voltage applied to each rectifier should be measured between the secondary center tap and each rectifier to determine whether voltage is present and of the correct value. If the circuit includes a series resistor ( $\mathbf{R}_{s}$ ), an additional measurement should be made between the load connection at the resistor and the rectifier to determine whether the resistor is open. (With primary voltage removed from the input, a resistance measurement can be made to determine whether the resistor is open.)

If necessary, measure the applied primary voltage to determine whether it is present and of the correct vahre. With the primary voltage removed from the circuit, a continuity measurement of the **primary** winding should be made to determine whether the winding is open, since an open winding will cause lack of secondary voltage.

If the circuit includes a series (surge) resistor common to both rectifiers and the resistor is found to be open, each rectifier and the load circuit should be checked further to determine whether excessive load current or a defective rectifier(s) has caused the resistor to act as a fuse and to open. With the ac supply voltage removed from the input of the circuit and with the load disconnected from the rectifiers, resistance measurements can be made across the load to determine whether the load circuit (including filter components) is shorted.

Although physical appearance is not a positive indication of condition, the rectifier may be given a visual check for a change in physical appearance which can indicate rectifier failure. A relative check of the rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. However, failure of the rectifier(s) may be the result of other causes; therefore, additional tests of the falter and load circuit are necessary.

Low Output. Each rectifier should be checked to determine whether the low output is due to normal rectifier aging or to one or more defective rectifiers. A relative check of rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. (A comparison can be made by checking one rectifier against the other to determine whether they have similar characteristics.) If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will become excessive. Since the full-wave rectifier circuit normally sup plies current to the load on each half cycle, failure of either rectifier (or associated series resistor, if used) or an open in either half of the secondary winding will allow the circuit to act as a half-wave rectifier circuit, and the output voltage will be reduced accordingly. Furthermore, whenever this occurs, the ripple amplitude will also increase, and the ripple frequency will be that of the ac source (instead of twice the source frequency). If one rectifier of the full-wave circuit is found to be defective, rather than replace the defective rectifier only, it is good practice to replace both rectifiers at the same time and to make certain that the replacement rectifiers have like, or matched, characteristics.

With the primary voltage removed from the circuit, resistance measurements can be made to check the continuity between the center tap and each rectifier terminal; this will determine whether one of the windings is open. As an alternative, the ac secondary voltage applied to each rectifier can be measured between the center tap and each rectifier to determine whether both voltages are present and are of the correct value.

The primary voltage should be measured to determine whether it is of the correct value, since a low applied primary voltage can result in a low secondary voltage. Also, shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. (A check for shorted turns was outlined in the failure analysis described for the electron-tube full-wave rectifier circuit, given earlier in this section of the handbook).

The load current (to the falter circuit and to the load) should be checked to make sure that it is within tolerance and is not excessive. A low-output condition due to a decrease in load resistance would cause an increase in load current; for example, excessive leakage in the capacitors of the filter circuit would result in increased load current.

# SINGLE-PHASE, FULL-WAVE BRIDGE RECTIFIER (ELECTRON TUBE)

#### Application.

The single-phase, full-wave bridge rectifier is used in electronic equipment for applications requiring high-voltage dc at a high load current. The rectifier

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circuit can be arranged to furnish negative or positive high-voltage output to the load, although the circuit is commonly used as a positive high-voltage power supply in most applications.

# Characteristics.

Input to circuit is ac; output is pulsating dc.

Uses four high-vacuum or gas-filled electron-tube diodes as rectifiers, or two diodes and one twin-diode as rectifiers.

Output requires faltering; dc output ripple frequency is twice the primary line-voltage frequency.

.Has good regulation characteristics.

Circuit provides either positive- or negative-polarity output voltage.

Requires three separate filament transformers or separate **filament windings** for rectifier tubes.

Uses power transformer with single high-voltage secondary winding; modified circuit to supply two output voltages simultaneously uses transformer with center-tapped, high-voltage secondary winding.

### **Circuit** Analysis.

**General. The** single-phase, full-wave bridge rectifier circuit uses two half-wave rectifier tubes in series on each side of a single transformer high-voltage secondary winding (the transformer secondary winding does not require a center tap); a total of four rectifiers are used in the bridge circuit. During each half cycle of the impressed ac voltage, two rectifiers, one at each end of the secondary, conduct in series to produce an electron flow through the load. Thus, electrons flow through the load in pulses, one pulse for each half cycle of the impressed voltage. Since two dc output pulses are therefore produced for each complete input cycle, full-wave rectification is obtained and the output is similar to that of the conventional **full**wave rectifier circuit.

One advantage of the bridge rectifier circuit over a conventionrdl fidl-wave rectifier is that for a given transformer total-secondary voltage the bridge circuit produces an output voltage which is nearly twice that of the Ml-wave circuit. Another advantage is that the peak inverse voltage across an individual rectifier tube, during the period of time the tube is nonconducting, is approximately half the peak **inverse** voltage across a tube in a conventional full-wave rectifier circuit designed to produce the same output voltage. One disadvantage of the bridge rectifier circuit, however, is that at least three filament transformers (or three separate windings) are required for the rectifier tubes.

In many power-supply applications, it is desirable to provide two voltages simultaneously-one voltage for high-power stages and the other voltage for **low**power stages. For these applications the single-phase, full-wave bridge rectifier circuit can be **modified** to supply an additional output voltage which is equal to one half of the voltage provided by the fidl-wave bridge rectifier circuit.

**Circuit Operation.** A single-phase, full-wave bridge rectifier is shown in the accompanying circuit **sche**-matic.



Basic Single-Phase, Full-Wave Bridge Rectifier Circuit

Four identical-type electron-tube diodes, VI, V2, V3, and V4, are comected in a bridge circuit across the secondary winding of transformer T1. Each tube forms one arm of the bridge circuit; the load is connected between the junction points of the balanced arms of the bridge. Transformer T1 is a step-up transformer to provide high voltage for the bridge rectifiers. The circuit given shows three separate fdament transformers, T2, T3, and T4. A single fdament transformer may be used, provided that it incorporates three separate fdament secondary windings that are well insulated from each other and from ground (chassis). Note that the **filaments** of V1 and V2 are at the same potential with respect to each other,

whereas the **filaments** of V3 and V4 are not. The **filaments** of V3 and V4 are connected to opposite ends of the high-voltage secondary and therefore operate at the full potential difference that exists across the secondary of T1; thus, if the filaments of V3 and V4 were supplied by a single transformer winding, the common comection would place a short across the high-voltage secondary winding. The **fila**ments of V3 and V4 must, therefore, be insulated from each other and must also be well insulated from ground. In either case, whether three separate **fila**ment transformers or a single filament transformer with multiple secondary windings is used, the **fila**ment primary voltage is applied independent of, and

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prior to, the primary voltage to T1. This arrangement permits the rectifier **filaments** to be preheated to the normal operating temperature before the high voltage is applied to the bridge-rectifier circuit.

The circuit arrangement given in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired. The circuit is typical of high-voltage, dc supplies designed for use in radar sets and communication transmitters.

The operation of the fill-wave bridge rectifier circuit can be understood from the simplified circuit schematic (parts A and B) and the waveforms (part C) shown in the accompanying illustration. The basic bridge rectifier schematic, given earlier in this discussion, has been simplified and redrawn in the form of a simple bridge circuit; the rectifier tube reference designations used correspond to those assigned in the basic bridge rectifier schematic. The bridge circuit uses four identical-type rectifiers. The end terminals of the transformer high-voltage secondary winding are connected to opposite cathode-plate junction points of the rectifiers comprising the arms of the bridge circuit, as shown. The load is connected between the remaining two cathode-plate junction points of the bridge circuit.

During the first half cycle, the transformer secondary winding (terminals A and B), shown in the schematic of part A, may be considered a voltage source that produces a voltage of the polarity given in the illustration. During time interval*a*, terminal A is positive with respect to terminal B; as a result, electrons will flow in the direction indicated by the arrows through the series circuit composed of rectifier V4, the load, and rectifier VI. This electron flow produces an output pulse of the polarity indicated across the load resistance. Also, during this period (time interval a), V2 and V3 are nonconducting.

During the next half cycle, time interval **b**, a secondary voltage is produced of the polarity given in part B of the illustration. Terminal B is positive with respect to terminal A; as a result, electrons will flow in the **direction** indicated by the arrows through the series circuit composed of rectifier V3, the load, and rectifier V2. The electrons flowing in the series circuit once again produce an output of the same polarity as before across the load resistance. During this period (time interval b), V1 and V4 are nonconducting.



Simplified Full-Wave Bridge Ractifier Circuit and Wavaforms

From the waveforms given in part C, it can be seen that two rectifiers conduct at any instant of time; thus, on alternate half cycles, electrons flow through the load resistance to produce a pulsating output volt $age;e_o$ . This output voltage has a pulsating waveform, which results in an irregularly shaped ripple voltage because the output voltage and current are not continuous; the frequency of the ripple voltage is twice the frequency of the ac source. The full-wave bridge rectifier circuit requires filtering to smooth out the ripple and produce a steady dc voltage.

The full-wave bridge rectifier circuit makes continuous use of the transformer secondary; therefore, there are two pulsations of current in the output for each complete cycle of the applied ac voltage. The dc load current passes through the entire secondary winding, flowing in one direction for one half cycle of the applied voltage, and in the opposite direction for the other half cycle; thus, there is no tendency for the transformer core to become permanently magnetized. Since little dc core saturation occurs, the effective inductance of the transformer, and therefore the efficiency, is relatively high.

The full-wave bridge rectifier, assuming a series of half sine waves as the waveform for the output voltage, e. (unfiltered), produce the following rootmean-square voltage:

 $E_{\text{rms}} = E_{\max} \times 0.707$ where:  $E_{\max} = \max_{\text{voltage}}$ 

The corresponding average output voltage is:

$$E_{av} = 0.9 E_{,m}s$$

Similarly, the root-mean-square and average output currents can be expressed as:

and:

$$I_{rmmax} \times 0.707$$
$$I_{av} = 0.9 I_{rms}$$

The peak inverse voltage across an individual rectifier in a full-wave bridge rectifier circuit during the period of time the tube is nonconducting is approximately 1.41 times the ms voltage across the secondary winding. The secondary voltage,  $\mathbf{e_{sec}}$ , is applied to two rectifier tubes in series; therefore, since less peak inverse voltage (approximately one half) appears across each tube, the bridge circuit can be used to obtain a higher output voltage than can be obtained from a conventional full-wave rectifier circuit using equivalent rectifier tubes. The peak inverse voltage *per tube* can be expressed as:

where: 
$$E_{imv}$$
 (per tube) = 1.41 E, ,,  
Erms = times voltage across entire secondary

The output of the full-wave bridge rectifier is similar to that of the conventional full-wave rectifier circuit. The bridge rectifier provides twice the output voltage for the same total transformer secondary voltage and dc output **current** as does the full-wave rectifier circuit using a center-tapped secondary. The output of the bridge rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the latter part of this section.)

A variation of the full-wave bridge rectifier circuit uses a transformer with a center-tapped secondary winding to supply two output voltages simultaneously to two separate loads. The circuit is fundamentally the same as that given earlier; for this reason the accompanying circuit schematic has been simplified and redrawn to eliminate the filament transformers and associated filament circuitry. The reference designations previously assigned remain unchanged.



Simplified Full-Wave Center-Tap and Full-Wave Bridge Rectifier Circuit

# ELECTRONIC CIRCUITS

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One advantage of the circuit is that two voltages may be supplied from the same set of rectifiers. One output voltage ( $E_{av}$ ) is obtained from the output of the bridge circuit; the second output voltage ( $E_{av}$ )/2, which is equal to one half of the bridge output voltage, is obtained by using two rectifiers, V3 and V4 of the bridge, and the center tap of the secondary winding as a conventional full-wave rectifier circuit. (The operation of the full-wave rectifier circuit was previously described in this section.) Although this circuit variation can supply two output voltages simultaneously to two separate loads, there is a limitation on the total current which can be carried by the rectifiers, V3 and V4.

# Failure Analysis.

**No Output.** In the full-wave bridge rectifier circuit, the no-output condition is likely to be limited to one of several possible causes: an open filament supply circuit, defective rectifier tubes, the lack of applied ac voltage, or a shorted load circuit (including shorted filter-circuit components).

A visual check of glass+ **nvelope** rectifier tubes can be made to determine whether the **filements** are lit. If the filaments are not all lit, the primary voltage may not be applied to the **filament** transformers (T2, T3, and T4 of Basic Single-Phase, Full-Wave Bridge Rectifier Circuit). If only the **filaments** of VI and V2 are not lit, there will be no dc output from the rectifier circuit, and transformer T2 or both tubes may be defective. The tube filaments should be checked for continuity; the presence of correct filament voltage at the tube sockets (VI and V2) should be determined by measurement. If necessary, the primary and secondary voltages should be checked at the terminals of transformer T2 to determine whether the transformer is defective.

The ac secondary voltage,  $e_{sec}$ , should be measured at the terminals of transformer T1 to determine whether the voltage is present and of correct value. If necessary, measure the applied primary voltage,  $e_{pri}$ , to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity measurements of the primary and secondary windings should be made to determine whether one of the windings is open, since an open (discontinuity) in either winding will cause a lack of secondary voltage.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to

determine whether the load circuit, including filter, is shorted. A short in the components of the filter circuit or in the load will cause an excessive load current to flow. If the rectifiers are of the high-vacuum type, the heavy load current will cause the plates of the rectifiers to become heated and emit a reddish glow when" the plate dissipation is exceeded and, if allowed to continue, may result in permanent damage to the tubes. The high-voltage bridge circuit normally employs gas-filled rectifiers; an excessive load current will very likely result in permanent damage to the tubes because they are susceptible to damage from current overload. Therefore, once the difficulty in the load circuit has been located and corrected, the gasfilled rectifiers may require replacement as a result of the overload condition.

Low Output. The rectifier tubes should be checked to determine whether the filaments are lit; one or more defective rectifiers in the bridge can cause the low-output condition. Also, failure of only one rectifier in the bridge will allow the circuit to act as a half-wave rectifier with current supplied to the load on alternate half cycles only, and the output voltage will be reduced accordingly. If rectifier tube V1 or V2 is not lit, the trouble is obviously associated with the tube that is not lit; however, if V3 or V4 is not lit, then the trouble may be either the tube (V3 or V4) or its associated filament transformer (T3 or T4). The tube filament should be checked for continuity; the presence of correct filament voltage at the tube socket should be determined by measurement. If necessary, the primary, and secondary voltages should be checked at the terminals of the filament transformer (T3 or T4) to determine whether the transformer is defective.

The load current should be checked to make sure that it is not excessive, because a decrease in output voltage can be caused by an increase in load current (decrease in load resistance); for example, excessive leakage in the capacitors of the filter circuit would result in increased load current. Also, the ac secondary voltage,  $e_{sec}$ , and the primary voltage,  $e_{pri}$ , should be measured at the terminals of transformer T1 to determine whether these voltages are of the correct value. Shorted turns in either the primary of secondary windings will cause the secondary voltage to measure below normal. Shorted turns are not easily detected by resistance measurement; a voltage measurement is a more reliable indication. If the trans. former losses (due to shorted turns) are excessive, the

transformer may also become overheated. Another check to determine whether the transformer is defective is to disconnect the secondary load (s) and measure the primary current with the transformer unloaded; excessive primary current is an indication of shorted turns. Still another check is to disconnect all primary and secondary leads from the transformer and make measurements between the individual windings and the core, using an ohmmeter or a Megger (insulation tester), to determine whether any of the windings are shorted to the core or to the Faraday shield (noise-reduction shield between primary and secondary).

# SINGLE-PHASE, FULL-WAVE BRIDGE RECTIFIER (SEMICONDUCTOR)

#### Application.

The single-phase, full-wave bridge rectifier is used in electronic equipment for applications requiring high- or low-voltage dc at a relatively high load current. The circuit can be arranged to furnish negative or positive voltage to the load. A variation of the basic bridge circuit can supply two output voltages simultaneously to separate loads.

#### Characteristics.

Same characteristics as electron tube version, except that it uses four semiconductor rectifiers (single, multiple, or stacked units) instead of electron tubes.

#### Circuit Analysis.

**General.** The single-phase, full-wave bridge rectifier circuit uses two semiconductor rectifiers in series on each side of a single transformer secondary winding (the secondary winding does not require a center tap); four rectifiers are used in the bridge circuit, one in each arm of the bridge. During each half cycle of the impressed ac voltage, two rectifiers, one at each end of the secondary, conduct in series to produce an electron flow through the load. Thus, electrons flow through the load in pulses, one pulse for each half cycle of the impressed voltage. Since two dc output pulses are produced for each complete input cycle, full-wave rectification is obtained, and the output is similar to that of the conventional full-wave rectifier circuit.

One advantage of the bridge rectifier circuit over a conventional full-wave rectifier is that for a given transformer total-secondary voltage the bridge circuit produces an output voltage which is nearly twice that of the fill-wave circuit. Another advantage is that the peak-inverse voltage across an individual rectifier, during the period of time it is nonconducting, is approximately half the peak-inverse voltage across a rectifier in a conventional full-wave circuit designed to produce the same output voltage.

In many power-supply applications, it is desirable to provide two voltages simultaneously-one voltage for high-power stages and the other for low-power stages. For these applications the single-phase, **full**wave bridge rectifier circuit can be modified to supply an additional output voltage which is equal to one half of the voltage provided by the full-wave bridge rectifier circuit.

Circuit Operation. A single-phase, full-wave bridge rectifier using semiconductor diodes is shown in the accompanying circuit schematic. Four identical-type semiconductor rectifiers, CR1, CR2, CR3 and CR4, are connected in a bridge circuit across the secondary winding of transformer T1. Each rectifier forms one arm of the bridge circuit; the load is connected between the junction points of the balanced arms of the bridge. The circuit uses a single transformer, Tl, either to step up the alternating-source voltage to a higher value in the secondary winding or to step down the voltage to a low value. The circuit application and the values of the input and output voltages determine whether a step-up or step-down transformer is used. The series, or surge, resistor (Rs) is generally used only in high-voltage supplies and is not normally required in low-voltage supplies. The resistor is common to all rectifiers since it is placed in series with the load and filter circuit.

The circuit arrangement given in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired.

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Basic Single-Phase, Full-Wave Bridge Rectifier Circuit

The operation of the till-wave bridge rectifier circuit can be understood from the simplified circuit schematic (parts A and B) and the waveforms (part C) shown in the accompanying illustration and by reference to the explanation given for the equivalent electron-tube bridge circuit. The basic bridge rectifier schematic, given previously in this discussion, has been simplified and redrawn to show the action which occurs on alternate half-cycles of the applied voltage. The rectifier reference designations used correspond to these assigned in the basic bridge schematic.



Simplified Full-Wave Bridge Rectifier Circuit and Waveforms

During the first half-cycle the transformed secondary winding may be considered as a voltage source of the polarity given in part A of the illustration. As a result, electrons flow, in the direction indicated by the arrows, through the series circuit composed of rectifier CR2, resistor Rs, the load, and rectifier CR3. This electron flow produces on output pulse of the polarity indicated across the load resistance. Also, during this period, rectifiers CR1 and CR4 are nonconducting.

During the next half-cycle, a secondary voltage is produced of the polarity given in part B of the illustration. As a result, electrons flow, in the direction indicated by the arrows, through the series circuit

composed of rectifier CR1, resistor Rs, the load, and rectifier CR4. The electrons flowing in the series circuit once again produce an output of the same polarity as before across the load resistance. During this period, rectifiers CR2 and CR3 are nonconducting.

From the waveforms given in part C, it can be seen that two rectifiers in series conduct at any instant of time; thus, on alternate half-cyles, electrons flow through the load resistance to produce a pulsating output voltage, e.. This pulsating waveform results in an irregularly shaped ripple voltage because the output voltage and current are not continuous; the frequency of the ripple voltage is twice the frequency of the ac source. The output of the full-wave bridge rectifier circuit requires filtering to smooth out the ripple and produce a steady dc voltage.

The full-wave bridge rectifier circuit makes continuous use of the transformer **secondary**; therefore, there are two pulsations of current in the output for each complete cycle of the applied ac voltage. The dc load current phases through the entire secondary winding, flowing in one direction for one half-cycle of the applied voltage, and in the opposite direction for the other half-cycle; thus, there is no tendency for the transformer core to become permanently magnetized. Since little dc core saturation occurs, the effective inductance of the transformer, and therefore the efficiency, is relatively high.

The peak-inverse voltage across an individual rectifier in a full-wave bridge rectifier circuit during the period of time the rectifier is nonconducting is approximately 1.41 times the rms voltage across the secondary winding. Since the secondary voltage,  $\mathbf{e}_{sec}$ , is applied to two rectifiers in series, less peak-inverse voltage appears across each rectifier. Thus, the bridge circuit can be used to obtain a higher output voltage than can be obtained from a conventional full-wave rectifier circuit using identical rectifiers.

In bridge circuits designed to furnish high-voltage dc to the load, the peak-inverse voltage rating of the semiconductor rectifier is an important consideration. For such applications, several identical-type rectifiers may be placed in series or stacked to withstand the peak-inverse voltage and avoid the possibility of rectifier breakdown.

The output of the full-wave bridge rectifier is similar to that of the conventional full-wave rectifier circuit. For the some totrd transformer secondary voltage and dc output current, the bridge rectifier

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provides twice as much output voltage as does the full-wave rectifiers circuit using a center-tapped secondary.

The output of the bridge rectifier circuit is connected to a suitable filter circuit to smooth out the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the latter part of this handbook.)

A variation of the full-wave bridge rectifier circuit is shown below; it uses a transformer with a centertapped secondary winding to supply two output voltages simultaneously to two separate loads. The circuit is fundamentally the same as that given earlier; therefore, the reference designations previously assigned to the basic circuit remain unchanged. This modified circuit uses two series (surge) resistors which are common to both the full-wave center-tap rectifier circuit and the full-wave bridge rectifier circuit.



#### Full-Wave Center-Tap and Full-Weve Bridge Rectifier Circuit

One advantage of this circuit is that two voltages may be supplied from the same set of rectifiers. One output voltage ( $E_{av}$ ) is obtained from the output of the bridge circuit; the other output voltage ( $E_{av}$ )/2, which is equal to one half of the bridge output voltage, is obtained by using two rectifiers, CR1 and CR2 of the bridge, and the center tap of the secondary winding as a conventional full-wave rectifier circuit. Although this circuit can supply two output voltages simultaneously to two separate loads, there is a limitation on the total current which can be safely carried by rectifiers CR1 and CR2.

#### Failure Analysis.

**No Output.** In the full-wave bridge rectifier circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of a defective transformer), a shorted load circuit (including shorted filter-circuit components), or defective rectifiers.

The ac secondary voltage,  $e_{sec}$ , should be measured at the transformer terminals to determine whether the voltage is present and of the correct value. If necessary, measure the appiled primary voltage to determine whether it is present and of the correct value. With the input voltage removed from the circuit, continuity measurements of the windings can be made to determine whether one of the windings is open, since an open winding will cause a lack of secondary voltage.

If the circuit includes one or more series resistors (Rs), continuity measurements can be made to determine whether the resistors are open. When a series resistor is found to be open, the associated rectifiers and load circuit (including falter-circuit components) should be checked to determine whether excessive load current or defective rectifiers have caused the resistor to act as a **fuse** and to open.

With the ac supply voltage removed from the input of the circuit and with the load disconnected from the rectifiers, resistance measurements can be made across the load to determine whether the load circuit (including filter components) is shorted.

Although physical appearance is not a positive indication of condition, the rectifiers may be given a visual check for a change in physical appearance which can indicate rectifier failure. A relative check of the rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. However, failure of the rectifiers may be the result of other causes; for this reason, tests of the filter and load circuit are necessary.

**Low Output.** Each rectifier should be checked to determine whether the low output is due to normal rectifier aging or to one or more defective rectifiers. A relative check of rectifier condition can be made using an ohmmeter, as outlined in a previous paragraph of this section. A comparison can be made by

checking all rectifiers and noting the results obtained to determine whether the rectifiers have similar characteristics. If the forward resistance of the rectifier increases, the output voltage will decrease. **Also**, if the reverse resistance decreases, the output voltage will decrease and the amplitude of the ripple will become excessive.

Complete faihrre of only one rectifier in the bridge will allow the circuit to act as a half-wave rectifier with current supplied to the load on alternate halfcycles only, and the output voltage will be reduced accordingly. Furthermore, whenever this occurs, the ripple amplitude will also increase, and the ripple frequency will be that of the ac source (instead of twice the source frequency).

The load current should be checked to make sure that it is not excessive, because a decrease in output voltage can be caused by an increase in load current (decrease in load resistance); for example, excessive leakage in the capacitors of the filter circuit would result in increased load current. Also, the ac secondary voltage,  $e_{sec}$ , and the input (Primary) voltage should be measured at the terminals of transformer T1 to determine whether these voltages are of the correct value. Shorted terms in either the primary or secondary windings will cause the secondary voltage to measure below normal. (A check for shorted turns is outlined in the failure analysis described for the electron-tube MI-wave bridge rectifier circuit given earlier in. this section of the handbook.)

In the modified full-wave center-tap and Ml-wave bridge circuit, it is possible to have two **definite** conditions of low voltage caused by defective rectifiers: the output voltage  $(E_w)$  to load No. 1 can be low and the output voltage  $(E_{av})/2$  to load No. 2 normal, or both output voltages can be below normal. If the load currents are not excessive and the filter components have been checked as satisfactory the defective rectifiers in the first case are assumed to be CR3 and CR4 of the bridge circuit, and those in the second case are assumed to be CR1 and CR2, which are common to both the Ml-wave center-tap and the bridge circuits. In a practical full-wave center-tap and full-wave bridge circuit, the two rectifiers designated in the schematic as CR1 and CR2 may have higher current ratings than the rectifiers designated as CR3 and CR4, because CR1 and CR2 must carry the combined currents of both output loads. For this reason, rectifiers CR1 and CR2 may not be directly interchangeable with rectifiers CR3 and CR4 of the bridge circuit.

# PART 2-2. MULTI PHASE POWER SUPPLIES

THREE-PHASE HALF-WAVE (SINGLE "Y" SECONDARY) RECTIFIER (ELECTRON TUBE)

# Application.

**The** three-phase, (single "y" secondary) or "Half-Wave Star" rectifier is used in electronic equipment for applications where the primary ac source is three-phase and the dc power requirements exceed 1 kilowatt. The rectifier circuit can be arranged to furnish negative or positive high-voltage output to the load.

#### Characteristics.

Input to circuit is three-phase ac; output is dc with amplitude of ripple voltage less than that for a singlephase rectifier.

Uses three high-vacuum or gas-filled electron-tube diodes as rectifiers.

Output is relatively easy to filter; dc output ripple frequency is equal to three times the primary linevoltage frequency.

Has good regulation characteristics.

Circuit provides either positive- or negativepolarity output voltage.

Uses multiphase power transformer with star- or wye-connected secondary windings; primary windings may be either delta- or wye-connected.

#### Circuit Analysis.

**General.** The three-phase, half-wave (single "y" secondary) rectifier is the simplest type of three-phase rectifier circuit. The term three-phase refers to

the primary ac source, which is the equivalent of three singfe-phase sources, each source supplying a sine-wave voltage 120 degrees out of phase with the others. Fundamentally, this rectifier circuit resembles three single-phase, half-wave rectifier circuits, each rectifier circuit operating from one phase of a threephase source and sharing a common load. The voltages incluced in the transformer secondary windings differ in phase by 120 degrees; thus, each half-wave rectifier conducts for 120 degrees of the complete input cycle and contributes one third of the dc current supplied to the load. Electrons flow through the load in pulses, one pulse for each positive half cycle. of the impressed voltage in each of the three phases; therefore, the output voltage has a ripple frequency which is three times the frequency of the ac source.

Circuit Operation. A basic three-phase, half-wave rectifier is illustrated in the circuit schematic below. 'The circuit uses a three-phase transformer, T1, to step up the alternating source voltage to a high value in the star- or wye-connected secondaries. The primary windings of transformer T1 are shown deltaconnected, although in some instances the primary windings may be wye-connected (as for a three- or four-wire system). The plate of each rectifier tube, VI, V2, and V3, is connected to a high-voltage secondary winding. One filament transformer, T2, is used to supply the filament voltage to all three rectifiers since the filaments of the rectifiers are all at the same potential. The primary of transformer T2 is connected to one phase of the three-phase source. The load is connected between the junction point of the wye-connected secondary windings and the filament circuit of the rectifier tubes.

CHANGE 1



Basic Three-phase, Half-Wave (Single "Y" Secondary) Rectifier Circuit

CHANGE 1

In the circuit illustrated, either terminal of the load may be placed **at ground** potential, depending upon whether a positive or negative dc output is desired.

The operation of the three-phase, half-wave rectifier circuit can be understood from the circuit schematic previously given and from the waveforms shown in the accompanying illustration.



Three-Phase, Half-Wave Rectifier Waveforms

Each phase of the three-phase secondary voltage is applied across a rectifier and the common load. The secondary voltage of phase No. 1 ( $e_{sec}$ 1) is applied to rectifier VI, the secondary voltage of phase No. 2 ( $e_{sec}$ 2) is applied to rectifier V2, and the secondary voltage of phase No. 3 ( $e_{sec}$ 3) is applied to rectifier V3. The waveform given in the accompanying illustration as  $e_{sec}$  shows each of the three secondary voltages displaced 120 degrees from each other. On positive half cycles of  $e_{sec}$ 1, electrons flow through the

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load and rectifier VI; the pulse of plate current for rectifier V1 is identified in the illustration as the waveform, V1  $i_{p}$ . On positive half cycle of  $e_{sec}2$ , electrons flow through the load and rectifier V2; the pulse of plate current for V2 is identified as V2 i<sub>n</sub>. On positive half cycles of  $e_{sec}3$ , electrons flow through the load and rectifier V3; the pulse of plate current for V3 is identified as V3i<sub>p</sub>. From the three individual plate-current waveforms it can be seen that the start of a conduction period for any rectifier occurs 120 electrical degrees from the start of a conduction period for another rectifier in the circuit. The output voltage, e, across the load resistance is determined by the instantaneous currents flowing through the load; therefore, the output voltage has a pulsating waveform which never drops to zero because of the nature of the rectifier conduction periods.

If it were not for the overlapping of applied threephase secondary voltages, the rectifiers would each conduct for 180 degrees of the cycle; however, during the first 30 degrees of a half cycle, the plate of the rectifier is negative with respect to its positive filament (cathode), apd it will not conduct until the positive voltage applied to the plate exceeds the dc output voltage pulsations present across the load and at the filament circuit. Also, during the last 30 degrees of a half cycle, the plate is again negative with respect to the filament, and rectifier conduction ceases because the rectifier of another phase has started to conduct and produce a positive voltage across the load. In other words, each rectifier tube conducts for only one-third cycle, and this results in a series of dc output voltage pulsations with an irregularly shape ripple voltage; the frequency of the ripple voltage is equal to three times the frequency of the ac source. Because the ripple frequency is higher than that of a single-phase rectifier curcuit, the threephase, half-wave rectifier circuit requires less filtering to smooth out the ripple and produce a steady dc voltage.

In order to keep dc core saturation to a minimum (because of current flowing in one direction only in the secondary windings) and to keep the efficiency relatively high, it is necessary to use a single threephase transformer in this circuit, rather than three separate single-phase transformers.

The three-phase, half-wave rectifier produces across the load a pulsating (unfiltered) dc output voltage,  $E_{av}$ , as follows:

 $\begin{array}{l} E_{av} = 1.17 \ E_{rm\,s} \\ \text{where:} \quad E_{rm\,s} = rms \ \text{voltage across one} \\ \text{secondary winding of} \\ \text{three-phase transformer} \end{array}$ 

The *peak inverse voltage* across an individurd rectifier in the three-phase, half-wave rectifier circuit during the period of time the tube is nonconducting is approximately 2.45 times the rms voltage across the secondary winding of one phase. Some pulsating dc voltage is always present across the load, and this voltage is in series with the ac voltage applied to the plate; therefore, the sum of the instantaneous value of pulsating dc voltage across the load and the instantaneous peak voltage across the secondary represent the value of peak inverse voltage per *fube* can be expressed as:

where:  $E_{imv}$  (per tube)= 2.45  $E_{rms}$ where:  $E_{rms}$  = rms voltage across one secondary winding of the three-phase transformer

The output of the three-phase, half-wave rectifier circuit is connected to a suitable falter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.

#### Failure Analysis.

**No Output.** In the three-phase, half-wave rectifier circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of ac **fila**-ment supply, the lack of applied ac high voltage, of a shorted load circuit (including shorted **filter** components).

A visual check of the **glass-envelop** rectifier tubes can easily be made to determine whether all **filaments** are lit; if they are not lit, the filament voltage should be measured at the secondary terminals of transformer T2. If **necessary**, measure the applied primary voltage to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity (resistance) measurements of the primary and secondary windings should be made to determine whether one winding is open, since an open winding (primary or secondary) will cause a lack of **filament** voltage. With the primary voltage removed from the circuit, continuity (resistance) measurements should be made of the secondary and primary windings, to determine whether one or more windings are open and whether the common terminal (s) of the wyeconnected secondaries is connected to the load circuit. It necessary, the ac secondary voltage applied to the rectifier plates may be measured between the common terminal of the **wye-connected** secondaries and the plate of one or more rectifiers, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage to determine whether it is present and of the correct value.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to &termine whether the load circuit, including falter, is shorted. A short in the components of the filter circuit or in the load circuit will cause an excessive load current to flow: if the rectifier tube is of the high-vacuum type, the heavy load current will cause the plate of the rectifiers to become heated and emit a reddish glow when the plate dissipation is exceeded and, if allowed to continue, may result in permanent damage to the tubes. If gas-filled rectifiers are used in the circuit, excessive load current will result in permanent damage to the tubes because gasfilled rectifiers are very susceptible to damage from current overload. Therefore, once the difficulty in the load circuit has been located and corrected, the gasfilled rectifiers will require replacement as a result of the overload condition,

Low Output. If only one or two phases of the three-phase, half-wave rectifier circuit are operating normally the output voltage will be lower than normal. For example, if only one secondary winding and associated rectifier is in operation, the effect is the same as though it were a single-phase, half-wave rectifier circuit and, as a result, the output voltage is much lower than normal. When two phases are operating, the output voltage is somewhat higher and, when all three phases are operating, the output is normal. Thus, the low-output condition can be due to the fact that one or more secondary-phase circuits are not functioning normally.

The rectifier tubes should be checked first to determine whether all **filaments** are lit. All rectifier **filaments** are in parallel; therefore, if one **filament** is

not lit, the trouble is obviously associated with this particular tube. The tube **filament** should be checked for continuity; the presence of correct filament voltage at the tube socket should be determined by measurement.

With the three-phase primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one (or more) of the windings is open. If necessary, the ac secondary voltage applied to each rectifier plate may be measured between the common terminal of the secondary wye connection and the plate of each rectifier, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage at each of the phases, to determine whether each voltage is present and of the correct value, since a low applied primary voltage can result in a low secondary voltage.

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. Discomect all secondary leads from the transformer, TI, and measure the primary current in each leg of the three-phase primary with the transformer unloaded; excessive primary current is an indication of shorted turns. A secondary winding which is shorted to the core can cause a low-output voltage indication; all leads should be disconnected from the transformer and measurements made between the individual windings and the core, using an ohmmeter or a Megger (insulation tester), to determine whether any of the windings are shorted to the core.

The rectifier-output current (to the filter circuit and to the load) should be checked to make sure that it is within tolerance and is not excessive. A **low**output condition due to a decrease in load resistance would cause an increase in load current; for example, excessive leakage in the capacitors of the **filter** circuit would result in increased load current.

# THREE-PHASE, HALF-WAVE (SINGLE "Y" SECONOARY) RECTIFIER (SEMICONDUCTOR)

#### Application.

Same as electron tube version.

#### Characteristics.

Same characteristics as electron tube version, except it uses three semiconductor rectifiers (single, multiple, or stacked units) instead of electron tubes.

#### Circuit Analysis.

**General. The** three-phase, half-wave, (single "Y' secondary) rectifier is the simplest type of three-phase rectifier circuit. Fundamentally, this rectifier circuit is three single-phase half-wave rectifier circuits, each rectifier operating from one phase of a three-phase source and sharing a common load. The voltages induced in the transformer secondary windings differ in phase by 120 degrees; thus, each half-wave rectifier conducts for 120 degrees of the complete input cycle, and contributes one-third of the dc current supplied to the load. Electrons flow through the load in pukes, one pulse for every other half-cycle of the impressed voltage in each of the three phases; therefore, the output voltage has a ripple frequency which is three times the frequency of the ac source.

**Circuit operation.** A basic three-phase, half-wave rectifier is illustrated in the accompanying circuit schematic. The circuit uses a three-phase transformer, Tl, to step up the alternating source voltage to a high value in the wye-connected secondaries. The primary windings of transformer T1 are shown delta-connected, although in some instances the primary windings may be wye-connected (as for a three- or four-wire system). Each rectitier, CR], CR2, and CR3, is connected to a high-voltage secondary winding. The load is connected between the junction point of the wye-connected secondary windings and the common connection of the three rectifiers.



Basic Three-Phase, Half-Wave (Single "Y" secondary) Rectifier Circuit

In the circuit illustrated, either terminal of the load can be placed at ground potential, depending upon whether a positive or negative dc output is desired. However, it is good design practice for the dc output terminal associated with the junction of the wye-comected secondaries to be grounded, in this case, the secondary-to-core insulation need not be as great as it would be if the secondary windings were above ground by the amount of the dc output voltage. When a negative high-voltage dc supply is required, it is common practice to keep the junction of the wye-connected secondaries at ground (chassis) potential and to reverse the connections to the rectifiers (CR1, CR2, and CR3); in this case, the output polarity across the load will be opposite that shown on the schematic.

The semiconductor rectifiers, CR1, CR2, and CR3, are made up of several rectifiers in series to safely withstand the peak inverse voltage of the circuit and to prevent rectifier breakdown. Since each individual rectifier cell in the series-connected arrangement (multiple or stacked units) has a maximum reversevoltage rating, it is necessary for the series combination of rectifiers in any secondary leg to have a totrd reverse-voltage rating in excess of the maximum peak inverse voltage encountered in the circuit configuration. Although the voltage ratings for the commercially available silicon rectifiers are generally higher than for the selenium rectifiers, both selenium and silicon rectifiers are commonly used in highvoltage power supplies. Because a choke-input filter system is commonly employed with this circuit, series, or surge, resistors are not normally used, and for this reason are not shown in the schematic.

The operation of the three-phase, half-wave rectifier circuit can be readily understood from a study of the equivalent electron-tube circuit description and the associated waveforms given previously in this section of the handbook. For this reason, an explanation of circuit operation is not given here.

The action of the semiconductor rectifiers in this circuit is essentially the same as that described for the equivalent electron-tube circuit. The rectifier in each secondary leg conducts for only one-third cycle, and this results in a series of dc output voltage pulsations. The output voltage, e,, across **the load** resistance is determined by the instantaneous currents flowing through the load; therefore, the output voltage never drops to zero because of the overlapping of applied three-phase secondary voltages and the resulting rec-

tifier conduction **in** each **secondary** leg. Because the ripple voltage is equal to three tirries the frequency of the ac source, the circuit requires less **filtering** to smooth out the ripple and **produce** a steady dc voltage than does a single-phase rectifier circuit.

The peak inverse voltage across the rectifier (multiple or stacked units) in one secondary leg of the three-phase, half-wave circuit during the period of time the rectifier is nonconducting is approximately 2.45 time the rms voltage ( $e_{sec}$ ) across the secondary winding of one phase.

The regulation of the circuit is considered to be very good, and is better than that of a single-phase rectifier circuit having equivalent power-output rating; the semiconductor rectifier characteristics and the three-phase input contribute greatly to the improved regulation characteristic of the supply. The output of the three-phase, half-wave rectifier circuit is connected to a suitable falter circuit, to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.)

# Failure Analysis.

**No Output.** In the three-phase, half-wave rectifier circuit, the no-output condition is likely to be limited to one of three possible causes: the lack of applied ac voltage, a shorted load circuit (including shorted filter capacitors), or an open filter choke.

# NOTE

Most filter circuits used in Navy equipment employ two-section choke-input falters; thus, an open choke in either section will cause no output.

Measure the applied three-phase primary voltage to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one or more than one winding is open and whether the common terminrd(s) of the wyeconnected secondaries is connected to the load circuit. If necessary, the ac secondary voltage applied to the rectifiers may be measured between the common terminal(s) of the wye-connected secondaries and one or more rectifiers, to determine whether voltage is present and of the correct value.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifiers circuit (across load) to determine whether the load circuit, including the filter, is shorted. (As explained in the preceding note, an open choke in the filter circuit will also cause no output.) A short in the load circuit (including components in the filter circuit) will cause an excessive load current to flow and may result in permanent damage to the rectifiers. Therefore, once the difficulty in the load (including filter) circuit has been located and corrected, the rectifiers should be checked to determine whether they have been darn aged as a result of the overload condition.

Low Output. If <u>onry</u> one or two phases of the three-phase, half-wave rectifier circuit are operating normally, the output voltage will be lower than normal. For example, if only one secondary winding and associated rectifier is in operation, the effect is the same as though it were a single-phase, half-wave rectifier circuit; as a result, the output voltage is much lower than normal. When two phases are operating, the output voltage is somewhat higher, and when all three phases are operating, the output is normal. (Also, the percentage of ripple voltage will change for each of the conditions mentioned.) Thus, the low-output condition can be due to the fact that one (or more) of the secondary-phase circuits (including rectifiers) is not functioning normally.

The rectifiers should be checked to determine whether the low output is due to normal rectifier aging, or to one or more defective rectifiers. A relative check of rectifier condition can be made by using an ohmmeter, as outlined in a previous paragraph of this section. (A comparison can be made by checking one rectifier against each of the others to determine whether they have similar characteristics.) If the forward resistance of a rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will increase.

With the three-phase primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one (or more) of the windings is open. If necessary, the ac secondary voltage ( $es_{e}$ ) applied to each rectifier may be measured between the common terminal of the secondary wye connection and each rectifier, to determine whether voltage is present and of the correct vahre. Also, if necessary, measure the applied three-phase voltage at each of the phases, to determine whether each voltage is present and of the correct value, since low applied primary voltages can result in low secondary voltages.

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. (A check. for shorted turns is outlined in the failure analysis described for the electron-tube three-phase, half-wave rectifier circuit discussed earlier in this section of the handbook.)

The load current should be checked to make sure that it is not excessive, because a decrease in output voltage can be caused by an increase in load current (decrease in load resistance); for example, excessive <u>leakage</u> in the capacitors of the filter circuit will result in increased load current.

# THREE-PHASE, FULL-WAVE (SINGLE "Y" SECONDARY) RECTIFIER (ELECTRON TUBE)

# Application.

The three-phase, full-wave rectifier with single-wye secondary is used in electronic equipment for applications where the primary ac source is three-phase and the dc output requirements are relatively high. The rectifier circuit can be arranged to furnish either negative or positive high-voltage output to the load.

# Characteristics.

Input to circuit is three-phase ac; output is dc with amplitude of ripple voltage less than that for a singlephase rectifier.

Uses six high-vacuum or gas-filled electron-tube diodes as rectifiers.

Output requires very little filtering; dc output ripple frequency is equal to six times the primary line-voltage frequency.

Has good regulation characteristics.

Circuit provides either positive- or negativepolarity output voltage.

Requires separate filament transformers or separate filament windings for rectifier tubes.

Uses multiphase power transformer with wyeconnected secondary windings; primary windings may be either delta-or wye-connected.

# Circuit Analysis.

**General.** The three-phase, full wave (single-wyeconnected secondary) rectifier is extensively used where a large amount of power is required by the load, such as for large shipboard or shore electronic installations. The term *three-phase* refers to the primary ac source, which is the equivalent of three single-phase sources, each source supplying a sinewave voltage 120 degrees out of phase with the

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others. Because of the three-phase transformer secondary configuration, the circuit is sometimes referred to as *a bridge* Or *six-phase* rectifier circuit.

In man, power-supply applications, it is desirable to provide two voltages simultaneously—one voltage for high-power stages and the other voltage for lowpower stages. For these applications the three-phase, full-wave rectifier circuit can be modified to supply an additional output voltage, which is equal to one half of the voltage provided by the full-wave rectifier circuit.

Circuit Operation. The basic three-phase, full-wave rectifier circuit is illustrated in the accompanying

circuit schematic. The circuit uses a conventional three-phase power transformer, Tl, to step up the alternating source voltage to a high value in the wye-connected secondaries. The primary windings of transformer T1 are shown delta-connected, although in some instances the primary windings may be wye-connected (as for a three-Cf four-wire system). The plate of rectifier V1 and the filament (cathode) of rectifier V6 are connected to secondary terminal No. 1 of transformer Tl; the plate of rectifier V2 and the filament of rectifier V4 are connected to secon-Aayternunal No. 2, and the filament of secondary terminal No. 3.



Basic Three-Phase, Full-Wave (Single "Y" Secondary) Rectifier Circuit

One filament transformer, T2, is used to supply the filament voltage to rectifiers VI, V2, and V3, since the filaments of these rectifiers are all at the same potential. However, since the filaments of rectifiers V4, V5, and V6 have a high potential difference existing between them, three separate filament transformer (T3, T4, and T5) are used. A single filament transformer may be used for this purpose, provided that it incorporates three separate filament windings that are well insulated from each other and grounded (chassis). The primary windings of filament transformers T3, T4, and T5 are connected to different phases of the three-phase source. The ac voltage for the primaries of the filament transformers is applied independent of, and prior to, the primary voltage to the three-phase power transformer, T1. A time-delay arrangement, either manually operated or automatic, normally permits the rectifier filaments to be preheated to the normal operating temperature before the high-voltage ac can be applied to the rectifier circuit.

The circuit arrangement given in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired; however, the circuit is commonly arranged for a positive dc output, with the negative output terminal at ground (chassis). The circuit is typical of high-voltage dc supplies designed for use in radar sets, communication transmitters, or other equipment for which the dc power requirement is several kilowatts or more.

The operation of the three-phase, full-wave rectifier circuit can be understood from the simplified circuit schematics (parts A through F) and the waveforms given in the accompanying illustration. The basic three-phase, full-wave rectifier schematic, given earlier in this discussion, has been simplified to show the circuit action throughout the electrical cycle; the reference designations used correspond to those assigned in the basic circuit schematic.

The voltages developed across the secondary windings of transformer T1 are 120 degrees out of phase with relation to each other and are constantly changing in polarity. The polarities indicated for the secondary windings in the simplified circuit schematics (parts A through F) of the accompanying illustration represent the instantaneous polarity of the induced voltages in the secondary. The arrows on the schematics are used to indicate the directions of electron flow in the circuit.

The plates of rectifiers VI, V2, and V3 are connected to secondary windings No. 1, No. 2, and No. 3, respectively; the filaments (cathode) of rectifiers V6, V4, and V5, are connected to secondary windings No. 1, No. 2, and No. 3, respectively. When the plates of V1, V2, and V3 are positive with respect to their filaments, the tubes will conduct; when the filaments of V4, V5, and V6 are negative with respect to their plates, there tubes will conduct. At any given instant of time in the three-phase, full-wave rectifier circuit, a rectifier, the load, and a second rectifier are in series across two of the wye-connected transformer secondaries and, therefore, two rectifiers are conducting. Each of the six rectifiers conducts for 120 degrees of an electrical cycle; however, there is an over-lap of conduction periods, and the rectifiers conduct in a sequence which is determined by the phasing of the instantaneous secondary voltages of the power transformer. In the circuit described, two rectifiers are conducting at any instant of time, with rectifier conduction occurring in the following order: V1 and V4, V1 and V5, V2 and V5, V2 and V6, V3 and V6, V3 and V4, V1 and V4, etc.

Refer to the secondary-voltage waveform, esec, shown in the accompanying illustration. Assume that the ac voltage induced in secondary No. 1 (between 30 and 90 electrical degrees, phase No. 1) is approaching its maximum positive value (at 90 degrees); also, the voltage induced in secondary No. 2 has reached its maximum negative vahre (at 30 degrees) and is decreasing. (Secondary No. 3, although positive at 30 degrees, is decreasing to zero.) This condition is shown by the simplified schematic of part A in the accompanying illustration. The plate of rectifier VI becomes positive with respect to its filament (cathode), and the filament of rectifier V4 is negative with respect to its plate; therefore, both tubes conduct, and the electrons flow through V4, the load, and V1 for 60 degrees of the electrical cycle.



In part B, the ac voltage induced in secondary No. 1 reaches its macimum positive value (at 90 degrees) and starts to decrease during the next 60 degrees of the cycle; the voltage induced in secondary No. 3 is approaching its maximum negative value. The plate of VI remains positive with respect to its filament, and the filament of V5 becomes negative with respect to its plate; therefore, V1 continues to conduct and V5 takes over conduction from V4, with V1 and V5 conducting in series with the load. Electrons flow through V5, the load, and V1 for another 60 degrees of the cycle.

1ss part C, the ac voltage induced in secondary No. 3 reaches its macimum negative value and the positive voltage in secondary No. 2 is increasing. The filament of V5 remains negative with respect to its plate, and the plate of V2 becomes positive with respect to its filament; therefore, V5 continues to conduct and V2 takes over conduction from V1, with V2 and V5 conducting in series with the load. Electrons flow through V5, the load, and V2 for another 60 degrees of the cycle.

In part D, the ac voltage induced in secondary No. 2 reaches its maximum positive value and starts to decrease; the voltage induced in secondary No. 1 is approaching its maximum negative value. The plate of V2 remains positive with respect to its filament, and the filament of V6 becomes negative with respect to its plate; therefore, V2 continues to conduct and V6 takes over conduction from V5, with V2 and V6 conducting in series with the load. Electrons flow through V6, the load, and V2 for another 60 degrees of the cycle.

In part E, the ac voltage induced in secondary No. 3 is approaching its maximum positive value, and the negative voltage in secondary No. 1 is decreasing. The filament of V6 remains negative with respect to its plate, and the plate of V3 becomes positive with respect to its filament; therefore, V6 continues to conduct and V3 takes over conduction from V2, with V3 and V6 conducting in series with the load. Electrons flow through V6, the load, and V3 for another 60 degrees of the cycle.

In part F, the dc voltage induced in secondary No. 2 is approaching its maximum negative value, and the positive voltage in secondary No. 3 is decreasing. The plate of V3 remains positive with respect to its filament, and the filament of V4 becomes negative with respect to its plate; therefore, V3 continues to conduct and V4 takes over conduction from V6, with V3

and V4 conducting in series with the load. Electrons flow through V4, the load, and V3 for another 60 degrees of the cycle.

The cycle of operation is repeated, as shown in part A, when the dc voltage induced in secondary No. 2 reaches its maximum negative value and the positive voltage in secondary No. 1 is increasing. The filament of V4 remains negative with respect to its plate, and the plate of V1 becomes positive with respect to its filament; therefore, V4 continues to conduct and V1 takes over conduction from V3, with V1 and V4 conducting in series with the load. Electrons flow through V4, the load, and V1, to initiate another complete cycle.

Thus, from the action described above, it can be seen that each positive and negative peak in each of the three phases produces a current pulse in the load. Because of the nature of the rectifier conduction periods, each rectifier tube conducts for 120 degrees of the cycle and carries one third of the total load current. The output voltage, e, produced across the load resistance is determined by the instantaneous currents flowing through the load; therefore, the output voltage has a pulsating waveform, which results in an irregularly shaped ripple voltage, because the output current and voltage are not continuous. The frequency of the ripple voltage is six times the frequency of the ac source. Since this ripple frequency is higher than the ripple frequency of a single-phase, full-wave rectifier circuit or a three-phase, half-wave rectifier circuit, relatively little filtering is required to smooth out the ripple and produce a steady dc voltage.

The three-phase, full-wave rectifier circuit makes continuous use of the transformer secondaries, with the dc load current passing through a **secondary** winding first in one direction and then in the other; thus, there is no tendency for the transformer core to become permanently magnetized. Since little dc core saturation occurs, the effective inductance of the transformer, and therefore the effciency, is relatively high.

The three-phase, full-wave rectifier produces across the load a pulsating (unfiltered) dc output voltage,  $E_{av}$ , as follows:

where: 
$$E_{av} = 2.34 E_{rms}$$
  
 $E_{rms}$  = rms voltage across one  
secondary winding of  
three-phase transformer

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The peak inverse voltage across an individual rectitier in the three-phase, full-wave rectifier circuit during the period of time the tube is nonconducting is approximately 2.45 times the rms voltage across the secondary winding of one phase. Some pulsating dc voltage is rdways present across the load, and this voltage is in series with the applied ac secondary voltage; therefore, the sum of the instantaneous pulsation dc load voltage and the instantaneous peak secondary voltage represents the peak inverse voltage across the rectifier tube. Threpekk-inverse voltage *per 4: doe can* be expressed as:

where:  $E_{inv}$  (per tube) = 2.45  $E_{rms}$  $E_{rms}$  = rms voltage across one secondary winding of three-phase transformer

The output of the three-phase, full-wave rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the kind circuit. (Filter circuits are discussed in the Filter Section of this handbook.

A variation of the three-phase, **full-wave** rectifier circuit uses the common terminal of the wyeconnected secondaries and rectifiers V4, V5, and V6 to form a three-phase, half-wave rectifier circuit. The circuit is fundamentally the same as that given earlier; for this reason the accompanying circuit schematic has been simplified and redrawn to eliminate the filament transformers and associated filament circuity. The reference designations previously assigned remain unchanged.





# ELECTRONIC CIRCUITS

#### NAVSHIPS 0967-0000120

One advantage of the circuit is that two voltages may be supplied from the same transformer and rectifier combination. One output voltage  $(E_{out})$  is obtained from the full-wave circuit; the other voltage  $E_{out}/2$ , which is equal to one half of the full-wave output voltage, is obtained by using rectifiers V4, V5, and V6 and the common terminal of the wyeconnected secondaries as a conventional three-phase, half-wave rectifier circuit. (The operation of the three-phase, half-wave rectifier circuit was previously described in this section.) Although this circuit variation can supply two output voltages simultaneously to two separate loads, there is a limitation on the total current which can be carried by the rectifiers (V4, V5, and V6). Another variation of the three-phase, full-wave rectifier circuit uses a delta-connected secondary for T1. Each secondary winding is connected to the other in proper phase relationship so that the currents through the windings are balanced. Damage can result to the transformer windings if improperly connected; for this reason, the windings are usually connected internally in the proper phase to prevent the possibility of making wrong connections, and only the three secondary terminals are brought out of the case.

A schematic diagram showing this circuit variation is shown below.

The operation of the circuit can be easier understood from the simplified circuit schematics (parts A through F) and the waveforms given in the following illustrations.



Basic Three-Phase, Full-Wave (Delta Secondary) Rectifier Circuit

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Three-Phase, Fall-Wave Rectifier

The operation of the delta-secondary rectifier circuit is similar to that of the wye-secondary rectifier circuit (previously described); however, the ac voltage across an individual delta-connected secondary winding is  $0.742 E_{av}$ , whereas the voltage across an individual wye-connected secondary winding is 0.428  $E_{av}(E_{av})$  is the unfiltered ac output across the load). The voltages developed across the secondary windings of transformer T1 are 120 degrees out of phase with relation to each other and are constantly changing in polarity. In the delta-connected secondary, at any given instant the voltage in one phase is equal to the vector sum of the voltages in the other two phases. The polarities indicated for the secondary windings in the simplified circuit schematics (parts A through F) of the accompanying illustration represent the instantaneous polarity of the incluced voltage in the secondary. Although the instantaneous polarity shown in the schematic is given for only one secondary winding, the sum of the instantaneous voltages in the other two windings is equal to the voltage of the first winding. The arrows on the schematics are used to indicate the directions of electron flow in the circuit.

> The plates of rectifiers VI, V2, and V3 are connected to secondary terminals No. 1, No. 2, and No. 3, respectively; the filaments (cathode) of rectifiers V4, V5, and V6 are connected to secondary terminals No. 1, No. 2, and No. 3, respectively. When the plates of VI, V2, and V3 are positive with respect to their filaments, the tubes will conduct; when the filaments of V4, V5, and V6 are negative with respect to their plates, these tubes will conduct.

> At any given instant of time in the three-phase, full-wave rectifier circuit, a rectifier, the load, and a second rectifier are in series across two terminals of the **delta-connected** secondaries and, therefore, two rectifiers are conducting. Each of the six rectifiers conducts for 120 degrees of an electrical cycle; however, there is an overlap of conduction periods, and the rectifiers conduct in a sequence which is determined by the phasing of the instantaneous secondary voltages of the power transformer. In the circuit described, two rectifiers are conducting at any instant of time, with the rectifier conduction periods occurring in the following order: V1 and V6, V6 and V2, V2 and V4, V4 and V3, V3 and V5, V5 and **V1**, VI and V6, etc.

> Refer to the secondary-voltage waveform,  $e_{sec}$ , shown in the accompanying illustration. Assume that

the ac voltage induced in secondary No. 1, transformer terminals No. 1 and No. 2, is approaching its maximum positive value (at 90 degrees); also, the voltage induced in secondary No. 2, transformer secondary terminals No. 2 and No. 3, has reached its maximum negative value (at 30 degrees) and is decreasing. (The voltage induced in secondary No. 3, terminals No. 1 and No. 3, is passing through zero.) This condition is shown by the simplified schematic of part A in the accompanying illustration. The plate of rectifier V1 is positive with respect to its filament (cathode), and the filament of rectifier V5 is negative with respect to its plate; therefore, both tubes conduct, and electrons flow through V5, the load, and V1 for 60 degrees of the electrical cycle.

In part B, the ac voltage induced in secondary No. 1 has reached its maximum positive value (at 90 degrees) and starts to decrease during the next 60 degrees of the cycle; the voltage induced in secondary No. 3 is approaching its maximum negative value. The plate of V1 remains positive with respect to its filament, and the filament of V6 becomes negative with respect to its plate; therefore, V1 continues to conduct and V6 takes over conduction from V5, with V1 and V6 conducting in series with the load. Electrons flow through V6, the load, and V1 for another 60 degrees of the cycle.

In part C, the ac voltage induced in secondary No. 3 has reached its *maximum* negative value and starts to decrease; the voltage induced in secondary No. 2 is approaching its maximum positive value. The filament of V6 remains negative with respect to its plate, and the plate of V2 becomes positive with respect to its filament; therefore, V6 continues to conduct and V2 takes over conduction from V1, with V2 and V6 conducting in series with the load. Electrons flow through V6, the load, and V2 for another 60 degrees of the cycle.

In part D, the ac voltage induced in secondary No. 2 has reached its maximum positive value and starts to decrease; the voltage induced in secondary No. 1 is approaching its maximum negative value. The plate of V2 remains positive with respect to its filament, and the filament of V4 becomes negative with respect to its plate; therefore, V2 continues to conduct and V4 takes over conduction from V6, with V2 and V4 conducting in series with the load. Electrons flow through V4, the load, and V2 for **another** 60 degrees of the cycle.

In part E, the dc voltage induced in secondary No. 3 approaches its maximum positive value, and the negative voltage in secondary No. 1 is decreasing. The **filament** of V4 remains negative with respect to its plate, and the plate of V3 becomes positive with respect to its filament; therefore, V4 continues to conduct and V3 takes over conduction from V2 with V3 and V4 conducting in series with the load. Electrons flow through V4, the load, and V3 for another 60 degrees of the cycle.

In part F, the ac voltage induced in secondary No. 2 approaches its maximum negative value, and the positive voltage in secondary No. 3 is decreasing. The plate of V3 remains positive with respect to its filament, and the **filament** of V5 becomes negative with respect to its plate; therefore, V3 continues to conduct and V5 takes over conduction from V4, with V3 and V5 conducting in series with the load. Electrons flow through V5, the load, and V3 for another 60 degrees of the cycle.

The cycle of operation is represented, as shown in part A, when the ac voltage induced in secondary No. 2 has reached its maximum negative value and the positive voltage in secondary No. 1 is increasing. The filament of V5 remains negative with respect to its plate, and the plate of VI becomes positive with respect to its filament; therefore, V5 continues to conduct and V1 takes over conduction from V3, with VI and V5 conducting in series with the load. Electrons flow through V5, the load, and V1, to initiate another complete cycle. The three-phase, full-wave rectifier with delta-connected secondaries produces across the load a pulsating (unfiltered) dc output voltage,  $E_w$ , as follows:

where:

 $E_{av} = 1.35 \ E_{rms}$  $E_{rms} = rms voltage across one$ secondary winding ofthree-phase deltaconnected transformer

The *peak inverse voltage* across an individual rectifier in the three-phase, full-wave circuit during the period of time the tube is nonconducting is approximately 1.42 times the rms voltage across the secondary winding of one phase. Some pulsating dc voltage is always present across the load, and this voltage is in series with the applied ac secondary voltage; therefore, the sum of the instantaneous pulsating dc load voltage and the instantaneous peak to peak secondary voltage represents the peak inverse voltage across the rectifier tube. The peak inverse voltage *per tube can be* expressed as:

where:  $E_{inv}$  (per tube)= 1.42  $E_{rms}$  $E_{rms}$  = rms voltage across one secondary winding of three-phase delta-connected transformer

#### Failure Analysis

**No Output.** In the three-phase, full-wave rectifier circuit, the no-output condition is likely to be limited to the following possible causes: the lack of ac filament or filament-transformer primary supply voltage, the lack of applied ac high voltage, or a shorted load circuit (including shorted filter components).

A visual check of the glass-envelope rectifier tubes can easily be made to determine whether all filaments are lit. The filaments of V1, V2, and V3 should be observed first, because if these rectifiers are not lit there can be no dc output. If the filaments of V1, V2, and V3 are not lit, the filament voltage should be measured at the secondary of transformer T2 to determine whether it is present; if necessary, check the primary voltage of T2 to determine whether it is present and of the correct value. If none of the rectifier filaments are lit, the primary voltage source for the operation of transformers T2, T3, T4, and T5 should be checked for the presence of voltage.

With the primary voltage removed from the circuit, continuity (resistance) measurements should be made of the secondary and primary windings to determine whether one or more windings are open. Since the three windings of the delta-secondary circuit are sometimes connected internally and only three terminals are brought out of the case, voltage and resistance measurements are made between the terminals of the delta-connected secondaries. When making measurements (voltage or resistance) of the secondary circuit, it should be remembered that the windings form a delta configuration, with two windings in series and this combination in parallel with the winding under measurement. In other instances, the secondary windings are connected to six individual terminals, and these terminals are connected together to form a delta configuration. Thus, in this instance, the terminal connections may be removed to enable measurements to be made on individual secondary windings independent of other windings.
If necessary, the ac secondary voltage at each of the three high-voltage secondaries may be measured between the terminals of the delta-connected secondaries, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage to determine whether it is present and of the correct value.

With primary voltage removed from the rectifier circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including the filter, is shorted. A short in the components of the filter circuit or in the load circuit will cause an excessive load current to flow. If the rectifier tubes are of the high-vacuum type, the heavy load current will cause the plate of the rectifiers to become heated and emit a reddish glow when the plate dissipation is exceeded and, if allowed to continue, may result in permanent damage to the tubes. If gas-filled rectifiers are used in the circuit, excessive load current will result in permanent damage to the tubes because gasfilled rectifiers are very susceptible to damage from current overload. Therefore, once the difficulty in the load circuit has been located and corrected, the gasfilled rectifiers will require replacement as a result of the overload condition.

Low Output. The rectifier tubes should be checked to determine whether the filaments are lit. Because of the normal overlap in rectifier conduction periods and the conduction of tubes in series to obtain full-wave output, one or more defective rectifiers in the three-phase, full-wave rectifier circuit can cause the low-output condition. Failure of only one rectifier in the circuit will cause a loss of rectifier conduction and no delivery of current to the load for approximately 120 degrees of the electrical cycle, and the output voltage will be reduced accordingly. If rectifier tube VI, V2, or V3 is not lit, the trouble is obviously associated with the tube that is not lit since the filaments of these tubes are in parallel; however, if V4, V5, or V6 is not lit, then the trouble may be either the tube or its associated filament supply (T3, T4, or T5). The tube filament should be checked for continuity; the presence of correct filament voltage at the tube socket should be determined by measurement. If necessary, the primary and secondary voltages should be checked at the terminals of the tilament transformer (T3, T4, or T5) to determine whether the transformer is defective.

With the three-phase primary voltage removed from the circuit, continuity measurements should be made of the primary (and secondary) windings, to determine whether one (or more) of the windings is open. In the case of the delta-connected secondary, refer to the paragraph above explaining the "no-Output" condition for procedures to be used when making voltage and resistance measurements of the secondary windings. If necessary, the ac voltage of each secondary winding may be measured between the common terminal of the wye connection and the individual secondary terminal or the corresponding rectifier plate, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage at each of the phases, to determine whether each voltage is present and of the correct value, since a low applied primary voltage can result in a low secondary voltage.

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. Disconnect all secondary leads from the transformer, TI, and measure the current in each leg of the three-phase primary with the transformer unloaded; excessive primary current is an indication of shorted turns. A secondary winding which is shorted to the core can cause a low output voltage indication; to determine whether a winding is shorted to the core, all leads should be disconnected from the transformer and a measurement made between each individual winding and the core, using an ohmeter or a Megger (insulation tester).

Since a decrease in load resistance can cause an increase in load current and possibly result in a lowoutput condition, the rectifier-output current (to the filter circuit and to the load) should be checked to make sure that it is within tolerance and not excessive.

# THREE-PHASE, FULL-WAVE (SINGLE "Y" SECONDARY) RECTIFIER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version except that it uses six semiconductor rectifiers (multiple or stacked units) instead of electron tubes, and it does not require filament transfrrmers.

#### Circuit Analysis.

**General.** The three-phase, full-wave (single-wye secondary) rectifier is extensively used where a large amount of power is required by the load, such as for large shipboard or shore electronic installations. The rectifiers used in this circuit are generally forced-air-cooled or oil-cooled to dissipate heat developed during normal operation.

In many power-supply applications, it is desirable to provide two voltages simultaneously-one voltage for high-power stages and the other voltage for lowpower stages. For these applications the three-phase, full-wave rectifier circuit can be modified to supply an additional output voltage, which is equal to onehalf the voltage provided by the full-wave rectifier circuit.

**Circuit Operation.** The basic three-phase, full-wave rectifier circuit is illustrated in the accompanying circuit schematic. The circuit uses a conventional three-phase power transformer, T1, to step up the alternating source voltage to a high value in the wye-connected secondaries. The primary windings of T1 are shown delta-connected, although in some instances the primary windings may be wye-connected (as for a three-or four-wire system).



Basic Three-Phase, Full-Wave (Single "Y" Secondary) Rectifier Circuit

Semiconductor rectifiers CR1 and CR6 are connected to secondary terminal No. 1 of transformer T1; rectifiers CR2 and CR4 are connected to secondary terminal No. 2; rectifiers CR3 and CR5 are connected to secondary terminal No. 3. The rectifiers are identical-type semiconductor rectifiers. Although the schematic shows only six individual rectifiers in the circuit, each graphic diode symbol represents two or more diodes in series to obtain the necessary peakinverse characteristics for high-voltage operation.

The circuit arrangement shown in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired; however, the circuit is commonly arranged for a positive dc output, with the negative output terminal at ground (chassis). Aiso, a choke-input filter system is commonly used with this circuit; therefore, series, or surge, resistors are not normally used.

The operation of the three-phase, full-wave rectifier circuit can be readily understood from a study of the equivalent electron-tube circuit description and the associated waveforms given previously in this section of the handbook. The **reference** designations used for semiconductor rectifiers CR1 through CR6 correspond directly to the reference designations used in the electron-tube circuit for rectifiers V1 through V6. Since the rectifier action which takes place in both circuits is the same, an explanation of circuit operation is not given here.

The voltages developed across the secondary windings of transformer T1 are 120 degrees out of phase with relation to each other, and are constantly changing in polarity. At any given instant of time in the three-phase, full-wave rectifier circuit, a rectifier, the load, and a second rectifier are in series across two of the wye-connected transformer secondaries. Each of the six rectifiers conducts for 120 degrees of an electrical cycle; however, there is an overlap of conduction periods, and the rectifiers conduct in a sequence which is determined by the phasing of the instantaneous secondary voltages. In the circuit given here (and in the electron-tube equivalent circuit), two rectifiers are conducting at any 'instant of time, with rectifier conduction occurring in the following order: CR1 and CR4, CR1 and CR5, CR2 and CR5, CR2 and CR6, CR3 and CR6, CR3 and CR4, CR1 and CR4, etc.

Each positive and negative peak in each of the three phases produces a current pulse in the load. Because of the nature of the rectifier conduction periods, each rectifier conducts for 120 degrees of the cycle, and carries one third of the total load current. The output voltage, e., produced across the load resistance is determined by the instantaneous currents

flowing through the load; therefore, the output voltage has a pulsating waveform, which results in a ripple voltage, because the output current and voltage are not continuous. The frequency of the ripple voltage is six times the frequency of the ac source. Since this ripple frequency is higher than the ripple frequency of a single-phase, full-wave rectifier circuit or a threephase, half-wave rectifier circuit, relatively little filtering is **required** to smooth out the ripple and produce a steady dc voltage.

The peak inverse voltage across an individual rectifier (multiple or stacked units) in the three-phase, full-wave rectifier circuit during the period of time the rectifier is nonconducting is approximately 2.45 times the rms voltage across the secondary winding of one phase.

The regulation of the circuit is considered to be very good, and is better than that of a single-phase rectifier or of a three-phase, half-wave rectifier circuit having equivalent power-output rating. The output of the three-phase, full-wave rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.)



Three-Phase, Half-Wave and Three-Phase, Full-Wave Rectifier Circuit

A variation of the three-phase, full-wave rectifier circuit uses the common terminal of the wye-connected secondaries and rectifiers CR4, CR5, and CR6 to form a three-phase, half-wave rectifier circuit. The circuit is fundamentally the same as that discussed earlier; therefore, the reference designations previously assigned to the basic circuit remain unchanged.

One advantage of this circuit variation is that two voltages may be supplied from the same transformer and rectifier combination. One output voltage  $(E_{av})$  is obtained from the full-wave circuit; the other voltage  $(E_{av})/2$ , which is equal to one-half the full-wave output voltage, is obtained by using rectifiers CR4, CR5, and CR6 and the common terminal of the wye-connected secondaries as a conventional three-phase, half-wave rectifier circuit. Although this circuit can supply two output voltages simultaneously to two separate loads, there is a limitation on the total current which can be safely carried by the rectifiers (CR4, CF.5, and CR6).

Another variation of the three-phase, full-wave rectifier circuit uses a delta-connected secondary for T1. Each secondary winding is connected to the other in proper phase relationship so that the currents through the windings are balanced. Damage can result to the transformer windings if they are improperly connected; for this reason, the windings are usually connected internally in the proper phase to prevent the possibility of making wrong connections, and only three secondary terminals are brought out of the transformer case.



Basic Three-Phase, Full-Wave (Delta Secondary) Rectifier Circuit

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The primary windings of transformer T1 are shown delta-connected, although in some instances they may be wye-connected (as for a three- or fourwire system).

Semiconductor rectifiers CR1 and CR4 are connected to secondary terminal No. 1 of transformer T1; rectifiers CR2 and CR5 are connected to secondary terminal No. 2; rectifiers CR3 and CR5 are connected to secondary terminal No. 3. The rectifiers are identical-type semiconductor rectifiers. Although the schematic shows only six individual rectifiers in the circuit, each graphic symbol representa two or more diodes in series to obtain the necessary peak-inverse characteristics for high-voltage operation.

The circuit arrangement shown in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired; however, the circuit is commonly arranged for a positive dc output, with the negative output terminal at ground (chassis). Also, a choke-input filter system is commonly used with this circuit.

The operation of the three-phase, full-wave (delta secondary) rectifier circuit can be readily understood from a study of the equivalent electron-tube circuit description and the associated waveforms given previously in this section of the handbook. The reference designations used for semiconductor rectifiers CR1 through CR6 correspond directly to the reference designations used in the electron-tube circuit for rectifiers VI through V6. Since the rectifier action which takes place in both circuits is the same, an explanation of circuit operation is not given here.

The operation of the delta-secondary rectifier circuit is similar to that of the wye-secondary rectifier circuit (previously described); however, the ac voltage across an individual delta-connected secondary winding is approximately 1.73 times greater than the voltage across an individual wye-connected secondary winding for equal dc output voltages from the two circuits. The voltages developed across the secondary windings of transformer T1 are 120 degrees out of phase with relation to one another, and are constantly changing in polarity. In the delta-connected secondary, at any given instant the voltage in one phase is equal to the vector sum of the voltages in the other two phases. At any given instant of time in the three-phase, full-wave rectifier circuit, a rectifier, the load, and a second rectifier are in series across two terminals of the delta-connected secondaries. Each of the six rectifiers conducts for 120 degrees of an electrical cycle; however, there is an overlap of conduction periods, and the rectifiers conduct in a **sequence** which is determined by the phasing of the instantaneous secondary voltages of the power transformer. In the circuit given here (and in the electron-tube **equivalent** circuit), two rectifiers are conducting at any instant of time, with rectifier conduction occurring in the following order: CRI and CR6, CR6 and CR2, CR2 and CR4, CR4 and CR3, CR3 and CR5, CR5 and CR1, CR1 and CR6, etc.

Each positive and negative peak in each of the three phases produces a current pulse in the load. Because of the nature of the rectifier conduction periods, each rectifier conducts for 120 degrees of the cycle, and carries one third of the total load current. The output voltage,  $e_0$ , produced across the load resistance is determined by the instantaneous current flowing through the load; therefore, the output voltage has a pulsating waveform, which results in a ripple voltage, because the output current and voltage are not continuous. The frequency of the ripple voltage is six times the frequency of the ac source. Since this ripple frequency is higher than the ripple frequency of a single-phase, full-wave rectifier circuit or a threephase, half-wave rectifier circuit, relatively little filtering is required to smooth out the ripple and produce a steady dc voltage.

The peak inverse voltage across an individual rectifier (multiple or stacked units) in the three-phase, full-wave (delta secondary) rectifier circuit during the period of time the rectifier is nonconducting is approximately 1.42 times the rms voltage across the secondary winding of one phase.

The regulation of the circuit is considered to be very **good,and** is better than that of a single-phase rectifier or of a three-phase, half-wave rectifier circuit having equivalent power-output rating. The output of the three-phase, full-wave rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.)

#### Failure Analysis.

**No Output.** In the three-phase, full-wave rectifier circuit, the no-output condition is likely *to* be limited to one of three possible causes: the lack of applied ac voltage, a shorted load circuit (including shorted filter capacitors), or an open filter choke.

#### NOTE

Most filter circuits used in Navy equipment employ two-section choke-input filters; thus, an open choke in either section will cause no output.

Measure the applied three-phase primary voltage to determine whether it is present and of the correct value. With the primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one or more than one winding is open and whether the common terminal(s) of the wyeconnected secondaries is connected to the load circuit. If necessary, the ac secondary voltage applied to the rectifiers may be measured between the common terminal(s) of the wye-connected secondaries and one or more rectifiers to determine whether voltage is present and of the correct value.

Since the three windings of the delta-secondary circuit are sometimes connected internally and only three terminals are brought out of the case, voltage and resistance measurements are made between the terminals of the delta-connected secondaries. When making measurements (voltage or resistance) of the secondary circuit, it should be remembered that the windings form a delta configuration, with two windings in series, and this combination in parallel with the winding under measurement. In other instances, the secondary windings are connected to six individual terminals, and these terminals are connected together to form a delta configuration. Thus, in this instance, the terminal connections may be removed to enable measurements to be made on individual secondary windings, independent of other windings. If necessary, the ac voltage at each of the three highvoltage secondaries may be measured between the terminals of the delta-connected secondaries, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied threephase primary voltage to determine whether it is present and of the correct value.

With the primary voltage removed from the circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including the filter, is shorted. (An open choke in the filter circuit will also cause no output. See note above.) A short in the load circuit (including components in the filter circuit) will cause an excessive load current to flow and may result in permanent damage to the rectifiers. Therefore, once the difficulty in the load (including filter) circuit has been located and corrected, the rectifiers should be checked to determine whether they have been damaged as a result of the overload condition.

Low Output. Failure of only one rectifier to conduct will cause a loss of current delivered to the load for approximately 120 degrees of the electrical cycle, and the output voltage will be reduced accordingly. (Also, breakdown of a rectifier will cause a shorting effect upon the windings of the transformer and subject other rectifiers to overload.) Furthermore, when one rectifier fails to conduct, the ripple amplitude will increase. Therefore, each rectifier should be checked to determine whether the low output is due to normal rectifier aging, or to one or more defective rectifiers. A relative check of recitifer condition can be made by using an ohmmeter, as outlined in a previous paragraph of this section. A comparison can be made by checking one rectifier against each of the others to determine whether the rectifiers have similar characteristics. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will increase.

The load current should be checked to make sure that it is not excessive, because a decrease in output voltage can be caused by an increase in load current (decrease in load resistance); for example, excessive leakage in the capacitors of the filter circuit will result in increased load current. Also, the ac secondary voltage and the input (primary) voltage should be measured at the terminals of the transformer to determine whether these voltages are of the correct value. If necessary, and with the primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one (or more) of the windings is open. (Refer to the paragraph above for information concerning procedures to be used when making voltage and resistance measurements on delta-connected secondary windings.)

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. (A check for shorted turns is outlined in the failure analysis described for the electron-tube equivalent circuit given earlier in this section of the handbook.)

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In the modified three-phase, half-wave and threephase, full-wave rectifier circuit, it is possible to have two definite conditions of low voltage caused by one or more defective rectifiers; the output voltage  $(E_{w})$ to load No. 1 can be low and the output voltage  $(E_w)/2$  to load No. 2 normal, or both output voltages can be below normal. If the load currents are not excessive and the filter components have been checked as satisfactory, the defective rectifier(s) in the first case is assumed to be CR1, CR2, or CR3, and in the second case, CR4, CR5, or CR6. When the modified circuit is used, rectifiers CR4, CR5, and CR6 will usually have higher current ratings than the other rectifiers (CR1, CR2, and CR3) because of the requirement to handle the combined currents of both output loads.

# THREE-PHASE, HALF-WAVE (DOUBLE "Y" SECONDARY) RECTIFIER (ELECTRON TUBE)

# Application.

The three-phase, half-wave rectifier with doublewye secondary and interphase reactor is used in electronic equipment for applications where the primary ac source is three-phase and the dc output power requirements are relatively high. The rectifier circuit can be arranged to furnish either negative or positive high-voltage output to the load.

# Characteristics.

Input to circuit is three-phase ac; output is dc with amplitude of ripple voltage less than that for a singlephase rectifier.

Uses six high-vacuum or gas-filled electron-tube diodes as rectifiers.

Output requires very little filtering; dc output ripple frequency is equal to six times the primary linevoltage frequency.

Has good regulation characteristics.

Circuit provides either positive- or negative-polarity output voltage.

Requires only one filament-voltage supply.

Uses multiphase power transformer with two parallel sets of wye-comected secondaries operating 180 degrees out of phase with each other. The center points of the wye-connected secondaries are connected through an interphase reactor or balance coil to the load. The primary windings are generally delta-connected.

#### Circuit Analysis.

**General.** Fundamentally, this rectifier circuit resembles two half-wave (single-' 'y'' secondary) recti-

fiers in parallel, each rectifier circuit operating from a common delta-connected primary, and sharing a common load through an interphase reactor or balance coi. (The three-phase, half-wave rectifier circuit was previously described in this section.) The three-phase, half-wave (double-wye secondary) rectifier circuit uses a power transformer with two sets of wyeconnected secondaries, the windings of one set being connected 180 degrees out of phase with respect to the corresponding windings of the other set. For this reason, the circuit is sometimes referred to as a sixphase rectifier. The junction point of each wyeconnected secondary is, in turn, connected to a center-tapped inductance, called an interphase reactor or balance coil. The center tap of the interphase reactor is the common negative terminal for the load.

**Circuit Operation.** The three-phase, half-wave (double-wye secondary) rectifier circuit is illustrated in the accompanying circuit schematic. The circuit used a three-phase power transformer, T1, to step up the alternating source voltage to a high value in the wye-connected secondaries. The primary windings of transformer T1 are shown delta-connected; the delta primary is common to both wye-connected secondaries. The plates of rectifiers V 1, V2, and V3 are connected to one set of secondary ("A") windings at terminals 1A, 2A, and 3A, respectively. The plates of rectifiers V4, V5, and V6 are connected to the other set of secondary ("B") windings at terminals 3B, 1 B, and 2B, respectively.

One filament transformer, T2, is used to supply the filament voltage to all rectifiers, since the filament of the rectifiers are ail at the same potential. Although a single filament transformer is shown on the schematic, as many as three identical filament transformers are sometimes used as the filament supply, with each filament transformer supplying two (or more) rectifier tubes; in this case the primary of each single-phase filament tramformer is connected to a different phase of the three-phase source. Voltage is applied to the primaries of the filament transformers before it is applied to the primary of the three-phase power transformer T1. A timedelay arrangement, either manually operated or automatic, normally permits the rectifier filaments to be preheated to the normal operating temperature before the high-voltage ac can be applied to the rectifier circuit.

The center-tapped inductance, Ll, is an interphase reactor or balance coil. The common terminal of each wye-connected secondary is connected to one end of

L1; the center tap of the interphase reactor is connected to the load. Thus, the output-load current of each three-phase, half-wave rectifier circuit passes through one half of the interphase reactor, and these two currents are then combined in the load. For satisfactory operation, interphase reactor L1 must have sufficient inductance to maintain continuous current flow through each half of the coil. In effect, this reactor constitutes a choke-input filter arrangement, and exhibits the regulation characteristics of such a filter.

The circuit arrangement given in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired; however, the circuit is commonly arranged for a positive dc output, with the negative output terminal at ground (chassis). The circuit is typical of high-voltage dc supplies designed for use in large communication transmitters or other equipment for which the dc power requirement is several kilowatts or more.

The operation of the three-phase, half-wave (double-wye secondary) rectifier circuit can be understood by reference to the circuit schematic and the waveforms given in the accompanying illustration. The operation of each individual half-wave rectifier is the same as that given for the three-phase, half-wave (three-phase star) rectifier circuit previously described in this section. Although the voltages induced in the three transformer secondary windings differ in phase by 120 degrees, the voltages induced in corresponding windings of the two sets of wye-connected secondaries ("A" and "B") are 180 degrees out of phase with respect to each other.



Basic Three-Phase, Half-Wave (Double "Y" Secondary) Rectifier Circuit

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The output resulting from the conduction of rectifiers VI, V2, and V3 in conjunction with secondary "A" is shown on the accompanying illustration; the output resulting from the conduction of rectifiers V4, V5, and V6 in conjunction with secondary "B", the resulting combined dc output voltage,  $e_o$ , and the corresponding rectifier conduction periods are also given.

At any instant of time, two rectifier tubes are conducting to deliver current to the load, but their currents are not in phase and an overlap in conduction periods of the six rectifiers occurs. Each rectifier conducts for 120 degrees of the input cycle and contributes one sixth of the total dc current supplied to the load. In the circuit described, two rectifiers are conducting at any instant of time, with the rectifier conduction periods occurring in the following order: V6 and VI, VI and V4, V4 and V2, V2 and V5, V5 and V3, V3 and V6, V6 and V1, etc.



# Waveforms for Three-Phase, Half-Wave (Doubla "Y" Secondary) Rectifier Circuit

The main component of the ripple frequency present across the interphase reactor is three times the frequency of the ac source. Electrons flow through the load in pulses, one pulse for each positive half cycle of the impressed voltage in each of the three phases of the two sets of secondaries. As mentioned previously, the secondaries are 180 degrees out of phase with respect to each other; therefore, the output voltage has a ripple frequency which is six times the frequency of the ac source. Since this ripple frequency is higher than that of a single-phase, **full**wave rectifier circuit or a single three-phase, half-wave rectifier circuit, relatively little filtering is required to smooth out the ripple and produce a steady dc voltage.

In order to keep dc core saturation to a minimum (because of current flowing in one direction ordy in each secondary winding) and to keep the efficiency relatively high, it is necessary to use a single threephase transformer with multiple secondaries, rather than six individual single-phase transformers.

The three-phase, half-wave (double-wye secondary) rectifier circuit produces across the load a pulsating **(unfiltered)** dc output voltage,  $E_{av}$ , as follows:

$$E_{av} = 1.17 E_{rms}$$

where:  $E_{rms}$  = rms voltage across one secondary winding of the three-phase transformer

The *peuk inverse voltage* across an individual rectifier in the three-phase, half-wave rectifier circuit during the period of time the tube is nonconducting is approximately 2.45 times the rms voltage across the secondary winding of one phase. The peak inverse voltage per *tube* can be expressed as:

$$E_{inv}$$
 (per tube)= 2.45  $E_{rms}$ 

where:  $E_{rms}$  = rms voltage across one secondary winding of the three-phase transformer

The output of the three-phase, half-wave (doublewye secondary) rectifier is connected to a suitable filter circuit, to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the latter part of this section.)

A variation of the three-phase, half-wave (doublewye secondary) rectifier circuit omits the use of an interphase reactor or balance coil. If the interphase reactor (Ll) is not used in the circuit and the common terminal of each wye-connected secondary is connected to the negative terminal of the load, the circuit is classified as a *six-phase star*. However, the six-phase star, half-wave rectifier circuit is considered less desirable than the three-phase, half-wave (double-wye secondary) rectifier circuit, because it

requires the use of tubes with higher peak current ratings and a transformer with a higher KVA rating to obtain an equivalent dc output. Therefore, the circuit is seldom used.

# Failure Analysis.

**No Output.** In the three-phase, half-wave (doublewye secondary) rectifier circuit, the no-output condition is likely to be limited to the following possible causes: the lack of ac filament or tilament-transformer primary supply voltage, the lack of applied ac high voltage, or a shorted load circuit (including shorted filter components).

A visual check of the glass-envelope rectifier tubes can easily be made to determine whether the filaments are lit; if they are not lit, there can be no dc output. The filament voltage should be measured at the secondary terminals of transformer T2 to determine whether it is present; if necessary, check the primary voltage to T2 to determine whether it is present and of the correct value. When the circuit employs more than one filament transformer (for example, three transformers each operating from one phase of the three-phase source), if none of the rectifier filaments are lit the primary voltage source for the filament transformers should be checked for the presence of voltage.

With the primary voltage removed from the circuit, continuity (resistance) measurements should be made of the secondary and primary windings, to determine whether one or more windings are open and whether the common terminals of the wye-connected secondaries are connected to the load circuit through the interphase reactor or balance coil. If necessary, the secondary voltage may be measured at one (or more) of the high-voltage secondaries between the common terminal of the wye-connected secondaries and a secondary terminal *or* corresponding rectifier plate, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage to determine whether it is present and of the correct value.

With primary voltage removed from the rectifier circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including the filter, is shorted. A short in the components of the filter circuit or in the load circuit will cause an excessive load current to flow, and the full output voltage will be developed across each half of the interphase reactor, L1. If the rectifier tubes are of the highvacuum type, the heavy load current will cause the plates of the rectifiers to become heated and emit a reddish glow when the plate dissipation is exceeded and, if allowed to continue, may result in permanent damage to the tubes. If **gas-filled** rectifiers are used in the circuit, excessive load current will result in permanent damage to the tubes because **gas-filled** rectifiers are very susceptible to damage from current overload. Therefore, once the difficulty in the load circuit has been located and corrected, the gas-filled rectifiers will require replacement as a result of the overload condition.

Low Output. The rectifier tubes should be checked to determine whether all filaments are lit; however, because of the normal overlap in rectifier conduction periods, the failure of one or two rectifiers in the circuit will not greatly affect the output voltage but may increase the ripple amplitude. If only one rectifier is not lit, the tube filament should be checked for continuity. If the circuit employs more than one filament transformer and one or more tubes are not lit, the corresponding filament transformer(s) should be checked. Measure the secondary voltage to determine whether the correct filament voltage is present; the primary voltage should be measured at the transformer terminals, to determine whether voltage is applied and of the correct value. If necessary, continuity measurements of the transformer windings should be made to determine whether the transformer is defective.

The continuity of each half of the interphase reactor, L1, should be measured to determine whether one half of the winding is open. An open circuit in one half of this reactor will disconnect its associated three-phase, wye-connected secondary; the output voltage will decrease as a result, and the rectifier circuit will continue to operate as a three-phase, halfwave rectifier with single-wye secondary.

With the three-phase primary voltage removed from the circuit, continuity measurements should be made of the primary (and secondary) windings, to determine whether one (or more) of the windings is open. If necessary, the ac voltage of each secondary winding in each set of secondaries may be measured between the common terminal of the wye connection and the individual secondary terminal or the corresponding rectifier plate, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage at each phase, to determine whether voltage is present

and of the correct value, since a low applied primary voltage can result in a low secondary voltage.

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. Disconnect all secondary leads from the transformer, and measure the current in each leg of the three-phase primary with the transformer unloaded; excessive primary current is an indication of shorted turns. A secondary winding which is shorted to the core can also cause a low output voltage indication; to determine whether a winding is shorted to the core, all leads should be disconnected from the transformer and a measurement made between each winding and the core, using an ohmmeter or a Megger (insulation tester).

Since a decrease in load resistance can cause an increase in load current and possible result in a lowoutput condition, the rectifier-output current (to the filter circuit and to the load) should be checked, to make sure that it is within tolerance and is not excessive.

# THREE-PHASE, HALF-WAVE (DOUBLE "Y" SECONDARY) RECTIFIER (SEMICONDUCTOR)

#### Application.

Same as electron tube version.

#### Characteristics.

**Same characteristics** as electron tube version, except that it uses six semiconductor rectifiers (multiple or stacked units) instead of electron tubes, and therefore does not require a filament voltage supply.

#### Circuit Analysis.

**General.** Fundamentally, this rectifier circuit resembles two half-wave (single "Y" secondary) rectifiers in parallel, each rectifier circuit operating from a common delta-connected primary, and sharing a common load through an interphase reactor or balance coil. (The three-phase, half-wave rectifier circuit was previously described in this section.) The three-phase, half-wave (double-wye secondary) rectifier circuit uses a power transformer with two sets of wyeconnected secondaries, the winding of one set being connected 180 degrees out of phase with respect to the corresponding windings of the other set. For this reason, the circuit is sometimes referred to as a six*phase, half-wave* or a *delta-double-wye-with valance*  *coil* rectifier circuit. The junction point of each wyeconnected secondary is, in turn, connected to a center-tapped inductance, called an *Interphase reactor* or *balance coil*. The center tap of the interphase reactor is the common output terminal for the load.

Circuit **Operation**. The three-phase, half-wave (double-wye secondary) rectifier circuit is illustrated in the accompanying schematic. The circuit uses a three-phase power transformer, T1, to step up the alternating source voltage to a high value in the wye-connected secondaries. The primary windings of the transformer are shown delta-connected; the delta primary is common to both wye-connected secondaries.



# Basic Three-Phase, Half-Wave (Double "Y" Secondary) Rectifier Circuit

Semiconductor rectifiers CR1, CR2, and CR3 are connected to secondary terminals 1A, 2A, and 3A, respectively. Rectifiers CR4, CR5, and CR6 are connected to secondary terminals 3B, 1 B, and 2B, respectively. The **rectifiers** are identical-type semiconductor rectifiers. Although the schematic shows only six individual rectifiers in the circuit, each graphic symbol represents two or more diodes in series to obtain the necessary peak-inverse characteristics for high-voltage operation.

The center-tapped inductance, L1, is an interphase reactor or balance coil. The common terminal of each wye-connected secondary is connected to one end of L1; the center tap of the interphase reactor is connected to the load. Thus, the output-load current of each three-phase, half-wave rectifier circuit passes through one half of the interphase reactor, and these

two currents are then combined in the load. For satisfactory operation, interphase reactor L1 must have sufficient inductance to maintain continuous current flow through each half of the coil. In effect, this reactor constitutes a choke-input filter arrangement, and exhibits the regulation characteristics of such a filter.

The circuit arrangement shown in the illustration permits either terminal of the load to be placed at ground potential, depending upon whether a positive or negative dc output is desired; however, the circuit is commonly arranged for a positive dc output, with the negative output terminal at ground (chassis). It is good design practice for the dc output terminal associated with the center tap of the inductance. L1. to be grounded; therefore, the secondary-to-core insulation of transformer T1 need not be as great as it would be if the secondary windings were above ground by the amount of the ac output voltage. When a negative high-voltage dc supply is required, it is common practice to keep the center tap of inductor L1 at ground (chassis) potential and to reverse the rectifiers (CR1 through CR6); thus, the output polarity across the load will be opposite that shown in the schematic.

The operation of the three-phase, half-wave (double-wye secondary) rectifier circuit can be readily understood from a study of the equivalent electron-tube circuit description and the associated waveforms given previously in this section of the handbook. The reference designations **used** for semi-conductor rectifiers CR1 through CR6 correspond directly to the reference designations used in the electron-tube circuit for rectifiers VI through V6. Since the rectifier action which takes place in both circuits is the same, as explanation of circuit operation is not given here.

The operation of each half-wave rectifier circuit associated with a three-phase secondary ("A" or "B") is the same as that given for the three-phase, halfwave (single "Y" secondary) rectifier circuit previously described in this section. Although the voltages induced in the three secondary windings differ in phase by 120 degrees, the voltages induced in corresponding windings of the two sets of wye-connected secondaries ("A" and "B") are 180 degrees out of phase with respect to each other.

At any instant of time, two rectifiers are conducting to deliver current to the load, but their currents are not in phase and an overlap in conduction periods of the six rectifiers occurs. Each rectifier conducts for 120 degrees of the input cycle and contributes one sixth of the total current supplied to the load. In this circuit, two rectifiers are conducting at any instant of time, with the rectifier conduction periods occurring in the following order: CR1 and CR4, CR4 and CR2, CR2 and CR5, CR5 and CR3, CR3 and CR6, CR6 and CR1, CR1 and CR4, etc.

The main component of the ripple frequency present across the interphase reactor (Ll) is three times the frequency of the ac source. Electrons flow through the load in pulses, one pulse for each positive half-cycle of the impressed voltage in each of the three phases of the two sets of secondaries. As mentioned perviously, the secondaries are 180 degrees out of phase with respect to each other; therefore, the **output** voltage has a ripple frequency which is six times the frequency of the ac source. Since this ripple frequency is higher than that of a single-phase, fullwave rectifier circuit or a three-phase, half-wave (three-phase star) rectifier circuit, relatively little filtering is required to smooth out the ripple and produce a steady dc voltage.

The peak inverse voltage across a rectifier (multiple or stacked units) in a secondary leg of the threephase, half-wave (double-wye secondary) rectifier circuit during the period of time the rectifier is nonconducting is approximately 2.45 times the rms voltage across the secondary winding of one phase.

The regulation of the circuit is considered to be very good, and is better than that of asingle-phase rectifier or a three-phase, half-wave (single "Y" secondary) rectifier circuit having equivalent poweroutput rating. The output of the three-phase, halfwave (double-wye secondary) rectifier circuit is connected to a suitable filter circuit to smooth the pulsating direct current for use in the load circuit. (Filter circuits are discussed in the Filter Section of this handbook.)

# Failure Analysis.

**No Output.** In the three-phase, half-wave (doublewye secondary) rectifier circuit, the no-output condition is likely to be limited to one of three possible causes: the lack of applied ac voltage, a shorted load circuit (including shorted filter capacitors), or an open input choke.

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# NOTE

Most filter circuits used in Navy equipment employ two-section choke-input filters; thus, an open choke in either section will cause no output.

With the primary voltage removed from the circuit, continuity measurements should be made of the secondary and primary windings, to determine whether one or more than one winding is open, and whether the common terminals of the wye-connected secondaries are connected to the load circuit through the interphase reactor or balance coil. If necessary, the ac secondary voltage may be measured at one (or more) of the high-voltage secondaries (between the common terminal of the wye-connected secondaries and one or more rectifiers), to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage to determine whether it is present and of the correct value.

With primary voltage removed from the rectifier circuit, resistance measurements can be made at the output terminals of the rectifier circuit (across load) to determine whether the load circuit, including the filter, is shorted. A short in the components of the load circuit (including filter circuit) will cause an excessive load current to flow, and considerable output voltage will be developed across each half of the interphase reactor, L1. If an open should develop in both halves or in the center-tap lead of the interphase reactor, no output will be developed. Likewise, an open choke in the filter circuit will cause no output. (See note above.) An excessive load current caused by shorted components in the circuit may result in permanent damage to the rectifiers. Therefore, once the difficulty in the load (including filter) circuit has been located and corrected, the rectifiers should be checked to determine whether they have been damaged as a result of the overload condition.

Low Output. An open circuit in one half of the interphase reactor will disconnect its associated three-phase, wye-connected secondary; the output voltage will decrease as a result, and the rectifier circuit will continue to operate s a three-phase, halfwave rectifier with single-wye secondary. Therefore, the continuity of each half of the interphase reactor (Ll) should be checked to determine whether one half of the winding is open.

With the three-phase primary voltage removed from the circuit, continuity measurements should be made of the primary and secondary windings, to determine whether one (or more) of the windings is open. If necessary, the ac voltage of each secondary winding in each set of secondaries may be measured between the common terminal of the wye connection and the individual secondary terminal of the corresponding rectifier, to determine whether voltage is present and of the correct value. Also, if necessary, measure the applied three-phase primary voltage at each phase, to determine whether voltage is present and of the correct value, since a low applied primary voltage can result in a low secondary voltage.

Shorted turns in either the primary or secondary windings will cause the secondary voltage to measure below normal. (A check for shorted turns is outlined in the failure analysis described for the electron-tube equivalent circuit given earlier in this section of the handbook.)

The load current should be checked to make sure that it is not excessive, because a decrease in output voltage can be caused by an increase in load current (decrease in load resistance); for example, excessive leakage in the capacitors of the filter circuit will result in increased load current.

Failure of a rectifier to conduct will cause a loss of current delivered to the load, and the output voltage will be reduced accordingly. Therefore, each rectifier should be checked to determine whether the low output is due to normal rectifier aging, or to one or more defective rectifiers. A relative check of rectifier condition can be made by using an ohmmeter, as outlined in a previous paragraph of this section. A comparison can be made by checking one rectifier against each of the others to determine whether the rectifiers have similar characteristics. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease and the amplitude of the ripple voltage will also increase.  $\sim$ 

# PART 2-3. VOLTAGE MULTIPLIERS

# HALF-WAVE VOLTAGE DOUBLER (ELECTRON TUBE)

#### Application.

The half-wave voltage-doubler circuit is used to produce a higher dc output voltage than can be obtained from a conventional half-wave rectifier circuit. This voltage doubler is normally used in "transformerless" circuits where the load current is small and voltage regulation is not critical. The circuit is frequently employed as the power supply in small portable receivers and audio amplifiers and, in some transmitter applications, as a bias supply.

# Characteristics.

Input to circuit is ac; output is pulsating dc.

DC output voltage is approximately twice that obtained from equivalent half-wave rectifier circuit; output current is relatively small.

Output requires filtering; dc output ripple frequency is equal to ac source frequency.

Has poor regulation characteristics; output voltage available is a function of load current.

Depending upon circuit applications, may be used with or without a power isolation transformer.

Uses indirectly heated cathode-type rectifiers.

# **Circuit Analysis.**

**General. The** half-wave voltage doubler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term *voltage doubler* implies, the output voltage is approximately twice the input voltage. The half-wave voltage doubler derives its name from the fact that the output charging capacitor (C2) across the load receives a charge once for each complete cycle of the applied voltage. The half-wave voltage doubler is sometimes called a *cascade* voltage doubler. The voltage regulation of the circuit is poor and, therefore, its use is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation.** In the accompanying circuit schematics, parts A, B, and C illustrate basic **half**-wave voltage-doubler circuits. The circuit shown in part A uses a transformer, T1, which can be either a step-up transformer to obtain a high value of voltage in the secondary circuit, or an isolation transformer to permit either dc output terminal to be placed at

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ground (chassis) potential. The circuits shown in parts B and C do not use a transformer, and operate dirctly from the ac source. In the circuit illustrated in part A, either output terminal may be placed at ground (chassis) potential.. The circuit illustrated in part B places one side of the ac source at a negative dc potential, and thus restricts the circuit to use as a positive dc supply. The negative dc supply variation of this circuit is illustrated in part C.



Basic Half-Wave Voltage-Doubler Circuits

The rectifiers, VI and V2, are of the indirectly heated cathode type, and are identical-type diodes. Although the circuit schematic illustrates two separate rectifiers, a twin-diode is generally used in the circuit. Typical twin-diode electron tubes designed specifically for use in voltage-doubler circuits are: 25Z6, 50Y6, and 117Z6. As indicated by the tubetype numbers, these tubes require nominal filamentsupply voltages of 25, 50, and 117 volts, respectively. Because there are several possible circuit combinations, the actual filament circuits for V1 and V2 are not shown on the circuit schematics. The filament voltage for the rectifiers is usually obtained directly from the ac source if the filament is rated at the source voltage, by use of a voltage-dropping resistance in series with the rectifier filament (s) to reduce the ac source voltage to the correct value, or from a transformer secondary winding of the correct value. In some equipments, the filaments of other tubes within the equipment are connected in series (or seriesparallel), and this combination is then placed in series with the rectifier filament (s) across the ac source; when this is done, a voltage-dropping resistor may be required.

In the three circuits illustrated, the functions of rectifiers V1 and V2, and of charging capacitors Cl and C2, are the same for each of the circuits.



Typical Half-Wava Voltege-Doublar Circuit Operation and Waveforms

The operation of a half-wave voltage-doubler circuit can be understood from the simplified circuits, parts A and B, and the waveforms, part C, shown in the following illustration.

Assume that the ac input to the voltage doubler during the initial half-cycle is of the polarity indicated in part A of the illustration. Electrons flow in the direction indicated by the small arrows from the positive plate of charging capacitor Cl, through rectifier tube VI (cathode to plate), and to the dc source. The left-hand (negative) plate of capacitor Cl now, has a surplus of electrons, while the right-hand (positive) plate lacks electrons. Thus, during initial half-cycle, capacitor C 1 assumes a charge ( $E_{c1}$ ) of the polarity indicated, which is equal to approximately the peak value of the applied ac voltage.

During the next half-cycle the polarity of the applied ac input to the voltage doubler is as indicated in part B of the illustration. The charge  $(E_{c})$  existing across capacitor Cl is in series with the applied ac and will therefore add its potential to the peak value of the input voltage. Electrons flow in the direction indicated by the small arrows from the positive plate of capacitor C2, through rectifier tube V2 (cathode to plate), and to the positive plate of capacitor Cl. Thus, during the second half-cycle capacitor C2 assumes a charge  $(E_{co})$  of the polarity indicated which is equal to the peak value of the applied ac voltage plus the value of the charge  $(E_{cl})$  existing across charging capacitor Cl. Thus the value of the voltage  $(E_{c2})$  across capacitor C2 is equal to approximately twice the peak voltage of the applied ac, provided that charging capacitor Cl does not lose any initial charge.

In a practical circuit, the values of capacitors Cl and C2 are at least 16  $\mu$ f; therefore, with such a large value of capacitance in the circuit and because there is always some resistance (rectifier-tube plate resistance and ac source impedance) in the circuit, each capacitor may not immediately attain its maximum charge until several input cycles have occurred. Capacitor C2 is charged only on alternate half-cycles of the applied ac voltage, and is always attempting to discharge through the load resistance; therefore, the resulting waveform of the output voltage,  $\mathbf{e}_0$  (or  $\mathbf{E}_{c_0}$ ), varies as shown in part C of the illustration.

The output waveform contains some ripple voltage; therefore, additional filtering is required to obtain a steady dc voltage. The frequency of the main component of the ripple voltage is the same as the

frequency of the ac source, because capacitor C2 is charged only once for each complete input cycle. The regulation of the voltage-doubler circuit is relatively poor; the value of output voltage obtained is determined largely by the resistance of the load and the resulting load current, since the load (and the filter circuit, if used) is in parallel with capacitor C2.

# Failure Analysis.

**No Output.** In the half-wave voltage-doubler circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of filament voltage or an open filament in the rectifier (s), the lack of applied ac voltage, a shorted load circuit (including capacitor C2 and filter circuit components), or an open capacitor C1.

A visual check of a glass-envelope rectifier tube can be made to determine whether the filament (s) is lit; if the filament is not lit, it may be open or the filament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of voltage at the tube socket should be determined by measurement.

The ac supply voltage should be measured at the input of the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a step-up or isolation transformer (Tl) measure the voltage at the secondary terminals to determine whether it is present and is the correct value. With the primary voltage removed from the transformer, continuity measurements of the primary and secondary windings should be made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

With the ac supply voltage removed from the input to the circuit and with the load disconnected from capacitor C2, resistance measurements can be made across the terminals of capacitor C2 and at the output terminals of the circuit (across load). These measurements will determine whether the capacitor (C2) or the load circuit (including filter components) is shorted. Because capacitor C2 and the filter-circuit capacitors are usually electrolytic capacitors, the resistance measurements may vary, depending upon the test-lead polarity of the ommeter. Therefore, two measurements must be made, with the test leads reversed at the circuit test points for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value. Capacitor Cl may be checked in a similar manner.

Low Output. The rectifiers (V1 and V2) should be checked to determine whether the cause of low output is low cathode emission. The load current should be checked to make sure that it is not excessive, because the voltagedoubler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminal of each capacitor, Cl and C2, should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine the effective capacitance and leakage resistance of each capacitor. A decrease in effective capacitance or losses within either capacitor can cause the output of the voltage-doubler circuit to be below normal, since the defective capacitor will not charge to its normal operating value. If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter; the measurements are made with one terminal of the capacitor disconnected from the circuit and, using the ohmmeter procedure outlined in the previous paragraph, two measurements are made (with the test leads reversed at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohm for a satisfactory capacitor.

# HALF-WAVE VOLTAGE DOUBLER (SEMICONDUCTOR)

# Application.

Same application as electron tube version.

# Characteristics.

Same characteristics as electron tube version except that it uses two semiconductor rectifiers (single, multiple, or stacked units) instead of electron tubes.

# Circuit Analysis.

**General. The** half-wave voltage-doubler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term *voltage doubler* implies, the output voltage is approximately twice the input voltage. The half-wave voltage doubler derives its name from the fact that the output charging capacity (C2) across the load receives a

charge once for each complete cycle of the applied voltage. The hrdf-wave voltage doubler is sometimes called a *cascade* voltage doubler. The voltage regulation of the circuit is poor, and, therefore, its use is generally restricted to applications in which the load current is small and relatively constant.

Circuit Operation. In the accompanying circuit schematics, parts A, B, and C illustrate basic halfwave voltage doubler circuits. The circuit shown in part A uses a transformer, Tl, which can be either a step-up transformer to obtain a high vrdue of voltage in the secondary circuit, or an isolation transformer. The circuits shown in parts B and C do not use a transformer, and operate directly from the ac source. In the circuit illustrated in part A, the use of transformer T1 permits either output terminal to be placed at ground (chassis) potential. The circuit illustrated in part B places one side of the ac source at a negative dc potential, and thus restricts the circuit to use as a positive dc supply. A variation of this circuit is illustrated in part C; this variation provides a negative output voltage.



**Basic Half-Wave Voltage-Doubler Circuits** 

The rectifiers, CR1 and CR2, are identical-type semiconductor diodes. In the three circuits **illus**-trated, the functions of rectifiers CR1 and CR2, and of charging capacitors Cl and C2, are the same for

each of the circuits. Electrons flow through the load in the direction indicated by the arrow adjacent to the load resistance. The dc output polarity for each circuit is indicated by the signs associated with the load resistance.

The circuits shown in parts B and C have a resistor, Rs, in series with the ac source. The resistor, called the surge *resistor*, limits the peak current through each rectifier to a safe vahre. The value of resistor Rs is influenced by the circuit design; determination of its value includes the consideration of several other factors, such as the applied ac voltage, the resistance of the load circuit, the capacitance value of the charging capacitors, and the peak current rating of the semiconductor diodes. In the circuit shown in part A, the resistor has been omitted since there is normally sufficient resistance in the secondary winding of transformer T1 to limit the peak current through each rectifier; however, some circuits may include a resistor (Rs) between the charging capacitor (Cl) and the transformer secondary winding.

The operation of the half-wave voltagedouble circuit can be readily understood from a study of the equivalent electron-tube circuit description, simplified circuits, and associated waveforms given previously in this section of the handbook. The action of the semiconductor rectifiers in this voltagedoubler circuit is essentially the same as that described for the equivalent electron-tube circuit. Semiconductor rectifiers CRI and CR2 correspond directly to rectifiers V1 and V2 in the electron-tube circuit description. For these reasons, an explanation of circuit operation is not given here.

Charging capacitor C2 is charged only on alternate **half-cycles** of the applied ac voltage, and is rdways attempting to discharge through the load resistance; therefore, the output voltage, e<sub>o</sub>, contains some voltage variation, or ripple. The frequency of the ripple voltage is the same as the frequency of the ac source, because capacitor C2 is charged only once for each complete input cycle; thus, additional faltering is necessary to obtain a steady dc voltage. (Filter circuits are discussed in the Filter Section of this handbook.)

The regulation of the voltage-doubler circuit is relatively poor; the vahre of output voltage obtained is determined largely by the resistance of the load and the resulting load circuit, since the load (and the filter circuit, if used) is in parallel with capacitor C2.

#### Failure Analysis.

**No Output.** In the half-wave voltage-doubler circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of a defective transformer or an open surge resistor Rs), an open capacitor C 1, a shorted load circuit (including capacitor C2 and filter circuit capacitor), an open filter choke, or defective rectifiers.

The ac supply voltage should be measured at the input of the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a step-up or isolation transformer (T1), measure the voltage at the secondary terminals to determine whether it is present and is the correct value. With the primary voltage removed from the transformer, continuity measurements of the primary and secondary windings should be made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

If the circuit includes a surge resistor (Rs), a" resistance measurement can be made to determine whether the resistor is open. If the resistor is found to be open, the voltage-doubler and load circuit should be checked further to determine whether excessive load current, a defective rectifier, or a shorted capacitor has caused the resistor to act as a fuse and to open.

With the ac supply voltage removed from the input to the circuit and with the load disconnected from capacitor C2, resistance measurements can be made across the terminals of capacitor C2 and at the output terminals of the circuit (across the load). These measurements will determime whether capacitor C2 or the load circuit (including falter components) is shorted. Because capacitor C2 and the falter-circuit capacitors are electrolytic capacitors, the resistance measurements may vary, depending upon the testlead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the circuit test points for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value. Capacitor Cl may be checked in a similar manner.

The rectifiers should be checked to determine whether they are open or otherwise defective. A relative check of the rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. However, failure of one or both rectifiers may be the result of other causes; therefore, tests of the filter and load circuit are necessary.

Low Output. The ac supply voltage should be measured at the input of the circuit to determine whether the voltage is the currect value, since a low applied voltage can result in a IOW output voltage.

Each rectifier should be checked to determine whether the low output is due to normal rectifier aging. A relative check of rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will increase.

The load current should be checked to make sure that it is not excessive, because the voltage-doubler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminal of each charging capacitor, Cl and C2, should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine the effective capacitance and leakage resistance of each capacitor. A decrease in effective capacitance or losses within either capacitor can cause the output of the voltage-doubler circuit to be below normal, since the defective capacitor will not charge to its normal operating value. If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by use of an ohmmeter; the measurements are made with one terminal of the capacitor disconnected from the circuit. Using the ohmmeter procedure outlined in a previous paragraph for the no-output condition, two measurements are made (with the test leads reversed at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohm for a satisfactory capacitor.

# FULL-WAVE VOLTAGE DOUBLER. (ELECTRON TUBE)

#### Application.

**The** full-wave voltage-doubler circuit is used to produce a higher d-c output voltage than can be obtained from a conventional rectifier circuit utilizing the same input voltage. This voltage doubler is normally used where the load current is small and voltage

regulation is not too critical; however, the regulation of the full-wave voltage doubler is better than that of the half-wave voltage doubler. The circuit is frequently employed as the power supply in small portable receivers and audio amplifiers and, in some transmitter applications, as a bias supply.

# Characteristics.

Input to circuit is ac; output is pulsating dc.

DC output voltage is approximately twice that obtained from half-wave rectifier circuit utilizing the same input voltage; output current is relatively small.

Output requires filtering; dc output ripple frequency is equal to twice the ac source frequency.

Has relatively poor regulation characteristics; output voltage available is a function of load current.

Depending upon circuit application, may be used with or without a power or isolation transformer.

Uses indirectly heated cathode-type rectifiers.

# Circuit Analysis.

General. The full-wave voltage-doubler circuit is used either with or without a transformer to obtain a dc voltage from an ac source. As the term voltage *doubler* implies, the output voltage is approximately twice the input voltage. The full-wave voltage doubler derives its name from the fact that the charging capacitors (Cl and C2) are in series across the load, and each capacitor receives a charge on alternate half-cycles of the applied voltage; therefore, two pulses are present in the load circuit for each complete cycle of the applied voltage. Although the voltage regulation of the full-wave voltage doubler is better than that of the half-wave voltage doubler, it is nevertheless considered poor as compared with conventional rectifier circuits. Therefore, use of the circuit is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation.** A basic full-wave voltagedoubler circuit is shown in the accompanying circuit schematic. Fundamentally, the circuit consists of two half-wave rectifiers, V1 and V2, and two charging capacitors, Cl and C2, arranged so that each capacitor receives a charge on alternate half-cycles of the applied voltage. The voltage developed across one capacitor is in series with the voltage developed across the other; thus, the output voltage developed across the load resistance is approximately twice the applied voltage.

The rectifiers, VI and V2, are of the indirectly heated cathode type, and are identical-type diodes. Although the circuit schematic illustrates two separate rectifiers, a twindiode is generally used in the circuit. Typical twindiode electron tubes designed specifically for use in voltagedoubler circuits are: 25Z6, 50Y6, and 117Z6. As indicated by the tubetype numbers, these tubes require nominal filamentsupply voltages of 25,50, and 117 volts, respectively. Because there are several possible filament circuit combinations, the actual filament circuit for V1 and V2 is not shown on the circuit schematic. The filament voltage is usually obtained directly from the ac source if the filament is rated at the source voltage. by use of a voltage-dropping resistance in series with the rectifier filament (s) to reduce the ac source voltage to the correct value, or from a transformer secondary winding of the correct value. In some equipments, the filaments of other tubes within the equip ment are connected in series (or series-parallel), and this combination is then placed in series with the rectifier filament (s) across the ac source; when this is done, a voltage-dropping resistor maybe required.



**Basic Full-Wave Voltage-Doubler Circuit** 

The charging capacitors, Cl and C2, are of equal capacitance value and are usually relatively large (10 to 16 @). Equalizing resistors R1 and R2, are connected across charging capacitors C 1 and C2, respectively; they are of equal value and are generally greater than 2 megohms. Resistors R1 and R2 are not necessary for circuit operation; however, when included in the circuit, they have a dual purpose in that

they tend to equalize the voltages across the charging capacitors and also act as bleeder resistors to discharge the associated capacitors when the circuit is de-energized. When capacitors Cl and C2 are large, the peak charge current, during the period of time the rectifier conducts, may be excessive. To limit the charge current and offer protection to the rectifiers, a protective "surge" resistor is placed in series with the ac source. The value of the surge resistor is relatively small, generally 50 to 1000 ohms.

One disadvantage of the full-wave voltage-double circuit is that neither dc output terminal can be directly connected to ground or to one side of the ac



Typical Full-Wave Voltage-Doubler Circuit Operation and Waveforms

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source; however, when a stept-up or isolation transformer is used to supply the input to the voltage doubler, either output terminal may be connected to ground or to the chassis.

The operation of the full-wave voltage-doubler circuit can be understood from the simplified circuits, parts A and B, and the waveforms, part C, shown in the accompanying illustration.

Assume that the ac input to the voltage doubler during the inditial half-cycle is of the polarity indicated in part A of the illustration. C2 does not enter into circuit operation here. Electrons flow in the direction indicated by the arrows from the positive plate of charging capacitor Cl, through rectifier tube VI (cathode to plate), through the ac source, and to the negative plate of charging capacitor Cl. The upper (positive) plate of capacitor C 1 lacks electrons, while the lower (negative) plate has a surplus of electrons. Thus, during the initial half cycle, capacitor Cl assumes a charge  $(E_{c1})$  of the polarity indicated, which is equal to approximately the peak value of the applied ac voltage. The voltage  $(E_{cl})$  developed across charging capacitor Cl does not remain constant, as shown by waveform E<sub>c1</sub>, but tends to vary somewhat because of a small discharge current flowing through the parallel equalizing resistor (RI) and because there is a tendency to discharge through the series circuit consisting of the ac source, rectifier V2, and the load.

During the next half-cycle the polarity of the applied ac input to the voltage doubler is as indicated in part B of the illustration. Cl does not enter into circuit operation here. Electrons flow in the direction indicated by the arrows from the positive plate of charging capacitor C2, through the ac source, through rectifier V2, to the negative plate of charging capacitor C2. Thus, during the second half-cycle, capacitor C2 assumes a charge  $(E_{c2})$  of the polarity indicated, which is equal to approximately the peak value of the applied ac voltage. The voltage  $(E_{c2})$  developed across capacitor C2 does not remain constant, as shown by waveform  $E_{c2}$ , but tends to vary somewhat because of the small discharge current flowing through the parallel equalizing resistor (R2), and because there is a tendency to discharge through the series circuit consisting of the load, rectifier V1, and the ac source.

Charging capacitors Cl and C2 are connected in series across the load resistance, and the current delivered to the load results from the discharge of these capacitors. The instantaneous sum of the chargingcapacitor voltages,  $E_{c1}$  and  $E_{c2}$ , is equal to approximately twice the peak voltage applied to the input of the voltagedoubler circuit, and is shown by the waveform of the output voltage, e..

The output waveform contains some ripple voltage; therefore, additional filtering is required to obtain a steady dc voltage. The frequency of the main component of the ripple voltage is equal to twice the frequency of the ac source, since each charging capacitor receives a charge on alternate half-cycles of the applied voltage. The regulation of the voltagedoubler circuit is relatively poor; the value of the output voltage obtained is determined largely by' the resistance of the load and the resulting load current. If the load current is large, the voltage across capacitors C 1 and C2 is reduced accordingly.

# Failure Analysis.

**No Output.** In the full-wave voltage-double circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of filament voltage or an open filament in the rectifier (s), the lack of applied ac voltage, or a shorted load circuit (including falter circuit components).

A visual check of a glass-envelope rectifier tube can be made to determine whether the filament (s) is lit; if the filament is not lit, it may be open or the filament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of voltage at the tube socket should be determined by measurement.

The ac supply voltage should be measured at the input of the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a step-up or isolation transformer, measure the voltage at the secondary terminals to determine whether it is present and is the correct value. If necessary, the primary voltage should be removed from the transformer and continuity measurements of the primary and secondary windings made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

With the ac supply voltage removed from the input to the circuit and with the load (including filter circuit) disconnected from capacitor Cl, resistance measurements can be made across the load to determine whether the load circuit (including filter components) is shorted. Measurements should be made across the terminals of charging capacitors C 1 and C2 to determine whether one or both capacitors are shorted. (If the circuit includes equalizing resistors RI and R2, the resistance measured across a capacitor will normally measure something less the value of the equalizing resistor.) Because Cl and C2 are electrolytic capacitors, the resistance measurements may vary, depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the capacitor terminals for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value.

Low Output. The rectifiers (V1 and V2) should be checked to determine whether the cause of low output is low cathode emission. The load current should be checked to make sure that it is not excessive, because the voltage-doubler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminal of each capacitor, Cl and C2, should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine the effective capacitance and leakage resistance of each capacitor. A decrease in effective capacitance or losses within either capacitor can cause the output of the voltage-doubler circuit to be below normal, since the defective capacitor will not charge to its normal operating value. If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. The measurements are made with one terminal of the capacitor disconnected from the circuit; using the ohmmeter procedure outlined in a previous paragraph, two measurements are required (the test leads are reversed at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohrn for a satisfactory capacitor.

# FULL-WAVE VOLTAGE DOUBLER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

**Same** characteristics as electron tube version except that it uses two semiconductor rectifiers

(single, multiple, or stacked units) instead of electron tubes.

#### Circuit Analysis.

Generel. The full-wave voltage-double circuit is used either with or without a transformer to obtain a dc voltage from ac source. As the term *voltage* doubler implies, the output voltage is approximately twice the input voltage. The full-wave voltage doubler derives its name from the fact that the charging capacitors (and C2) are in series across the load, and each capacitor receives a charge nalternate halfycles of the applied voltage; therefore, two pukes are present in the load circuit for each complete cycle of the applied voltage. Although the voltage regulation of the full-wave voltage doubler is better than that of the half-wave voltage doubler, it is nevertheless considered poor as compared with conventional rectifier circuits. Therefore, use of the circuit is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation.** A bisic full-wave voltagedoubler circuit is shown in the accompanying circuit schematic. Fundamentally, the circuit consists of two half-wave rectifiers, CR1 and CR2, and two charging capacitors, Cl and C2, arranged so that each capacitor receives a charge on alternate half-cycles of the applied voltage. The voltage developed across one capacitor is in series with the voltage developed across the other; thus, the output voltage developed across the load resistance is approximately twice the applied voltage.



**Basic Full-Wave Voltage-Doubler Circuit** 

The rectifiers, CR1 and CR2, are identical-type semiconductor diodes, and the charging capacitors, Cl and C2, are of equal vahre. Equalizing resistors RI and R2 are connected across charging capacitors Cl

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and C2, respectively; they are of equal value and are generally greater than 2 megohms. Resistors RI and R2 are not necessary for circuit operation; however, when included in the circuit, they have a dual purpose in that they tend to equalize the voltages across the charging capacitors and also act as bleeder resistors to discharge the associated capacitors when the circuit is de-energized. When capacitors Cl and C2 are large, the peak charage current, during the period of time the rectifier conducts, may be excessive. To limit the charge current and offer protection to the rectifiers, a protective "surge" resistor, Rs, is placed in series with the ac source; however, if a transformer is used and if there is sufficient resistance in the secondary winding, the series resistor is usually omitted.

One disadvantage of the full-wave voltage-doubler circuit is that neither dcoutput terminal can be directly connected to ground or to one side of the ac source; however, when a step-up or isolation transformer is used to supply the input to the voltage doubler, either output terminal may be connected to ground or to the chassis.

The operation of the full-wave voltage-doubler circuit can be readily understood from a study of the equivalent electron-tube circuit description, simplified circuits, and associated waveforms given previously in this section of the handbook. The action of the semiconductor rectifiers in this voltagedoubler circuit is essentially the same as that described for the equivalent electron-tube circuit. Semiconductor rectifiers CR1 and CR2 correspond directly to rectifiers V1 and V2 in the electron-tube circuit description. For these reasons, an explanation of circuit operation is not given here.

Charging capacitors Cl and C2 are comected in series across the load resistance, and each capacitor receives a charge on alternate half-cycle of the applied voltage; therefore, the output voltage, e<sub>o</sub>, contains some voltage variations, or ripple. The frequency of the main component of the ripple voltage is equal to twice the frequency of the ac source and, therefore, additional **filtering** is required to obtain a steady dc voltage. (Filter circuits are discussed in the Filter Section of this handbook.)

The regulation of the voltagedoubler circuit is relatively poor; the value of the output voltage obtained is determined largely by the resistance of the load and the resulting load current. If the load current is large, the voltage across capacitors Cl and C2 is reduced accordingly.

# Failure Analysis.

**No Output.** In the full-wave voltage-doubler circuit, the no-output condition is likely to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of a defective transformer or an open surge resistors Rs), a shorted load circuit (including filter circuit capacitor), an open filter choke, or defective rectifiers.

The ac supply voftage should be measured at the input of the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a step-up of isolation transformer, measure the voltage at the secondary terminals to determine whether it is present and is the correct value. With the primary voltage regime d from the transformer, continuity measurements of the primary and secondary windings should be made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

If the circuit includes a surge resistor (Rs), a resistance measurement can be made to determine whether the resistor is open. If the resistor is found to be open, the voltage-doubler and load circuit should be checked further to determine whether excessive load current, a defective rectifier, or a shorted capacitor has caused the resistor to act as a fuse and to open.

Wrth the ac supply voltage removed from the input to the circuit and with the load (inchrding falter circuit) disconnected from capacitor Cl, resistance measurements can be made across the load to determine whether the load circuit (including filter components) is shorted. Measurements should be made across the terminals of charging capacitors Cl and C2 to determine whether one or both capacitors are shorted. (If the circuit includes equalizing resistors RI and R2, the resistance measured across a capacitor will normally measure something less than the value of the equalizing resistor.) Because Cl and C2 are electrolytic capacitors, the resistance measurements may vary, depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the capacitor terminals for one of the measurements, to determine the larger of the two resistance measurements. The

larger resistance value is then accepted as the measured vahre.

The rectifiers should be checked to determine whether they are open or otherwise defective. A relative check of the rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. However, faihrre of the rectifiers may be the result of other causes; therefore, tests of the filter and load circuit are necessary.

Low Output. The ac supply voltage should be measured at the input of the circuit <u>to determine</u> whether the voltage is the correct value, since a low applied voltage can result in a low output voltage.

Each rectifier should be checked to determine whether the low output is due to normal rectifier **aging**. A relative check of rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease, and the amplitude of the ripple voltage will increase.

The load current should be checked to make sure that it is not excessive, because the voltagedoubler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminrd of each charging capacitor, Cl and C2, should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine the effective capacitance and leakage resistance of each capacitor. A decrease in effective capacitance or losses within either capacitor can cause the output of the voltage-doubler circuit to be below normal, since the defective capacitor will not charge to its normal operating value. If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter; the measurements are made with one terminal of the capacitor disconnected from the circuit and, using the ohmmeter procedure outlined in a previous paragraph for the no-output condition, two measurements are made (with the test leads reversed at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohm for a satisfactory capacitor.

# VOLTAGE TRIPLER. (ELECTRON TUBE)

# Application.

**The** voltage-tripler circuit is used to produce a higher dc output voltage than can be obtained from a conventional rectifier circuit utilizing the same input voltage. It is normally used in "transformerless" circuits where the load current is small and voltage regulation is not critical.

# Characteristics.

Input to circuit is ac; output is pulsating dc.

Dc output voltage is approximately three times the voltage obtained from a half-wave rectifier circuit utilizing the same input voltage; output current is relatively small.

Output requires faltering; dc output ripple frequency is either twice or equal to ac source frequency, depending upon triple circuit arrangement.

Has poor regulation characteristics; output voltage available is a function of load current.

Depending upon circuit application, may be used with or without a power or isolation transformer.

Uses indirectly heated cathode-type rectifiers.

# Circuit Analysis.

General. The voltage-tripler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term voltage tripler implies, the output voltage is approximately three times the input voltage. The voltage regulation of the voltage tripler is relatively poor as compared with the regulation of either the half-wave or the full-wave voltage doubler circuit. Assuming that a given voltage-multiplier (doubler, tripler, or quadruple) circuit uses the same value of capacitors in each instance, the greater the voltage-multiplication factor of the circuit, the poorer is the regulation characteristics. However, the regulation characteristics can be improved somewhat by increasing the value of the individual capacitors used in the voltage-multiplier circuit. Because of the regulation characteristics of the voltage tripler, the use of the circuit is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation.** A basic voltage-tripler circuit is shown in the accompanying circuit schematic, Fundamentally, this circuit consists of a half-wave voltagedoubler circuit and a half-wave rectifier circuit arranged so that the output voltage of one circuit is in series with the output voltage of the other; thus, the total output voltage developed across the load resistance is approximately three times the applied voltages.



Basic Voltage-Triple Circuit

Rectifiers VI and V2, charging capacitors Cl and C2, and resistor RI form a half-wave voltagedoubler circuit (the operation of the voltagedoubler circuit was previously described in this section). Rectifier V3, charging capacitor C3, and resistor R2 form a simple half-wave rectifier circuit. Rectifiers V1, V2, and V3 are all identical-type diodes with indirectly heated cathodes. Because there are several possible fdament circuit arrangements, the actual fdament circuit schematic. It is usually necessary to isolate the **fila**ment (heater) voltages from independent sources because of heater-to-cathode breakdown voltage limitations imposed by the rectifier tubes themselves.

Charging capacitors Cl, C2, and C3 are of equal capacitance value and are usually rather large (10 to  $20 \,\mu$ f) for **50**- to 60-hertz ac input. Resistors R1 and R2 are connected across charging capacitors C2 and C3, respectively; they are generally greater than 2 megohms. Resistors RI and R2 are not necessary for circuit operation; however, when included in the circuit, they act as bleeder resistors to discharge the associated capacitors when the circuit is **de-energized**.

One disadvantage of the basic voltage-triple circuit illustrated is that neither dc output terminal can be directly connected to ground or to one side of the ac

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Typical Voltage-Tripler Circuit Operetion end Waveforms tripler, either output terminal may be connected to ground or to the chassis.

The operation of the basic voltage-tripler circuit can be understood from the simplifier circuits, parts A, B, and C, and the waveforms, part D, shown in the accompanying illustration.

Assume that the ac input to the voltage-tripler circuit (during the initial half-cycle) has the polarity indicated by the signs adjacent to the input terminals in part A of the illustration. Electrons flow in the direction indicated by the arrows from the right-hand (positive) plate of charging capacitor Cl, through rectifier tube V2 (cathode to plate), through the ac source, and to the left-hand (negative) plate of charging capacitor Cl. (The positive plate of capacitor Cl lacks electrons, while the negative plate has a surplus of electrons.)

While the action described above for the simplified circuit of part A is taking place, a similar action occurs (during the initial half-cycle) for the simplified half-wave circuit given in part B. (Note that in part B, the ac input has the polarity indicated by the signs adjacent to the input terminals, and, since these two circuits operate simultaneously, the input polarity is the same as that shown in part A.) Electrons flow in the direction indicated by the arrows from the upper (positive) plate of charging capacitor C3, through the ac source, through rectifier tube V3 (cathode to plate), and to the lower (negative) plate of charging capacitor C3. Thus, during the initial half-cycle, charging capacitor Cl assumes a charge  $(E_{c1})$  of the polarity indicated in part A, and this voltage is equal to approximately the peak value of the applied ac voltage; also, charging capacitor C3 assumes a charge  $(E_{c_3})$  of the polarity indicated in part B, and this voltage is equal to approximately the peak value of the applied ac voltage.

During the next half-cycle, the applied ac input to the voltage tripler has the polarity indicated by the signs adjacent to the input terminals in part C of the illustration. The charge ( $E_{cr}$ ) existing across charging capacitor Cl is in series with the applied ac and will therefore add its potential to the peak vahre of the input voltage. Electrons flow in the direction indicated by the arrows from the upper (positive) plate of capacitor C2, through rectifier tube VI (cathode to plate), through charging capacitor Cl and the ac source in series, and to the lower (negative) plate of charging capacitor C2. Thus, during the second halfcycle, charging capacitor C2 assumes a charge ( $E_{cr}$ )

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source; however, when a step-up or isolation trans. former is used to supply the input to the voltage L

of the polarity indicated which is equal to the peak value of the applied ac voltage pulse the vrdue of the charge ( $E_{el}$ ) existing across charging capacitor Cl. **As** a result, the vrdue of the voltage ( $E_{c2}$ ) across capacitor C2 is equal to approximately twice the peak voltage of the applied ac, provided that charging capacitor Cl does not lose any of its initial charge.

Charging capacitors C2 and C3 are connected in series across the load resistance; therefore, the dc voltage delivered to the load is the sum of the voltages ( $E_{c2} + E_{c3}$ ) developed across **charging** capacitors C2 and C3. The value of the dc output voltage, e<sub>o</sub>, is approximately three times the peak voltage applied to the input of the voltage-tripler circuit.

The output waveform,  $e_o$ , contains a ripple component; therefore, filtering is required to obtain a stead dc voltage. The frequency of the main component of the ripple voltage is equal to twice the frequency of the ac source because charging capacitors C2 and C3 receive charges on alternate half-cycles of the applied voltage. The vahre of the output voltage obtained from the voltage tripler is determined largely by the resistance of the load and the resulting load current. Assuming the same value for each of the charging capacitors in either rectifier circuit, the regulation of the voltage-tripler circuit is poor as compared with that of a typical voltage-doubler circuit.

Two possible arrangements for a modified voltagetripler circuit are given in the accompanying illustration; part A shows a modified triple circuit arranged for positive output with the negative output terminal common to one side of the ac source, and part B shows the circuit arranged for negative output with the positive output terminal common to one side of the ac source.

In these two circuit variations, the basic half-wave rectifier circuit, represented by V3 and C3, has a voltage-doubler circuit connected to it in such a manner that the full output voltage is developed across charging capacitor C2. The operation of either tripler circuit (part A or part B) is briefly described in the following paragraph.

During the initial half-cycle of the applied voltage, rectifier V3 conducts to charge capacitor C3. During the next half-cycle, the voltage across capacitor C3 is in a series with the applied voltage, and rectifier V2 conducts to charge capacitor C 1 to approximately twice the value of the peak input voltage. On the next half-cycle, rectifier V3 again conducts to charge

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Modified Voltage-Tripler Circuits

capacitor C3; at the same time, since the voltage across capacitor Cl is in series with the applied voltage, rectifier VI also conducts to charge capacitor C2 to approximately three times the peak value of the input voltage. Thus, the voltage developed across capacitor C2 is the dc output delivered to the load.

The output of the tripler circuits illustrated in parts A and B requires filtering to obtain a steady **dc voltage**. The frequency of the ripple voltage for either circuit arrangement is equal to the frequency of the ac source because charging capacitor C2 receives a charge only once for each complete cycle of the applied voltage. For this reason, the regulation is not as good as the regulation of the basic voltage-tripler circuit described earlier.

# Failure Analysis.

**No Output.** In the basic voltage-tripler circuit, the no-output condition is likely to be limited to one of the following possible causes: the lack of filament voltage to all rectifiers, the lack of applied ac voltage, or a shorted load circuit (including filter circuit components).

A visual check of the glass-envelope rectifier tubes can be made to determine whether the filaments are lit; if the filaments are not lit, the presence of voltage should be determined by measurement.

The ac supply voltage should be measured at the input to the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a step-up or isolation transformer, measure the voltage at the secondary terminals to determine whether it is present and is the correct value. If necessary, the primary voltage should be removed from the transformer and continuity measurements of the primary and secondary windings made to determine whether one of the windings is open, since an open circuit in either winding will cause a lack of secondary voltage.

With the ac supply voltage removed from the input to the circuit and with the load (including filter circuit) disconnected from the terminal of capacitor C2, resistance measurements can be made across the load to determine whether the load circuit (including filter components) is shorted. Measurements should be made across the terminals of charging capacitors C2 and C3 in the basic tripler circuit, or across charging capacitor C2 in the modified tripler circuit, to determine whether the no-output condition is caused by shorted capacitors. The basic tripler circuit includes resistors RI and R2; therefore, the resistance measured across capacitors C2 and C3 will normally be something less than the value of the associated bleeder resistor. Since the charging capacitors are electrolytic capacitors, the resistance measurements may vary, depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the capacitor terminals for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value.

**Low Output. The** rectifiers (Vi, V2, and V3) should be checked to determine whether the cause of

low output is low cathode emission. The load current should be checked to make sure that it is not excessive, because the voltage-tripler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminal of each charging capacitor (Cl, C2, and C3) should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance. A decrease in effective capacitance or losses within the capacitor can cause the output of the voltage-tripler circuit to be below normal, since the defective capacitor will not charge to its normal operating value. If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. First, discomect one terminal of the capacitor from the circuit; then, using the ohmmeter procedure outlined for the nooutput condition, make two measurements (reverse the test leads at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohm for a satisfactory capacitor.

# **VOLTAGE TRIPLER (SEMICONDUCTOR)**

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version except that it uses three semiconductor rectifiers (single, multipler, or stacked units) instead of electron tubes.

#### Circuit Analysis.

**General.** The voltage-tripler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term *voltage tripler* implies, the output voltage is approximately three times the input voltage. The voltage regulation of the voltage tripler is relatively poor as compared with the regulation of either the half-wave or the full-wave voltage-doubler circuit. Assuming that a given voltage-multiplier (doubler, tripler, or quadruple) circuit uses the same value of capacitors in each instance, the greater the voltage-multiplication factor of the circuit, the poorer the regulation characteristics. However, the regulation

characteristics can be improved somewhat by increasing the value of the individual capacitors used in the voltage-multipler circuit. Because of the regulation characteristics of the voltage tripler, the use of the circuit is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation.** Three voltage-tripler circuits are shown in the accompanying illustration. The schematic of part A shows a basic voltage-tripler circuit, which is fundamentally a half-wave voltage-doubler and a half-wave rectifier arranged so that the output voltage of one circuit is in series with the output voltage of the other. The schematic of part B shows a modified tripler circuit arranged for positive output, with the negative output terminal common to one side of the ac source; part C shows this same circuit



**Voltage-Tripler Circuits** 

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arranged for negative output, with the positive terminal common to one side of the ac source. In each of the voltage-tripler circuits shown in the accompanying illustration, the total output voltage developed across the load resistance is approximately three times the applied voltage.

The rectifiers, CR1, CR2, and CR3, are identicaltype semiconductor diodes in each of the three circuits illustrated. Charging capacitors Cl, C2, and C3 are of equal capacitance value in each of the three circuits; however, because of the higher voltage developed across capacitor C2, the voltage rating of C2 is always greater than the voltage rating of either Cl or C3. Resistors R1 and R2, shown in the circuit of part A, are not necessary for circuit operation; however, when they are included in the circuit, resistors R1 and R2 stabilize the voltage developed across the two series capacitors, C2 and C3, respectively, and also act as a bleeder to discharge the capacitors when the circuit is de-energized. The value of resistor R1 is generally twice the value of resistor R2.

A surge resistor, Rs, is placed in series with the ac source; however, if a transformer is used in the circuit, and if there is sufficient resistance in the secondary winding, the resistor may be omitted.

Each tripler circuit illustrated has one disadvantage in that neither dc output terminal can be directly connected to ground (chassis). (The circuits shown in parts B and C have one output terminal in common with the ac source.) If a step-up or isolation transformer is used to supply the input to a tripler circuit, either output terminal may be connected to ground or to the chassis.

The operation of the tripler circuits can be readily understood from a study of the equivalent electrontube circuit descriptions given perviously in this section of the handbook. The action of the semiconductor rectifiers in a tripler circuit is essentially the same as that described for the equivalent electrontube circuit. Semiconductor rectifiers CR1, CR2, and CR3 correspond directly to rectifiers V1, V2, and V3 in the electron-tube circuit description. For these reasons, an explanation of circuit operation is not given here.

In the circuit shown in part A, charging capacitors C2 and C3 are in series across the load resistance, and each capacitor receives a change on alternate halfcycles of the applied voltage; as a result, the output voltage contains some ripple. In this tripler circuit, the frequency of the main component of the ripple voltage is equal to twice the frequency of the ac source. In the circuits shown in parts B and C, charging capacitor C2 receives a charge on alternate halfcycles only; thus, the output voltage of these two circuits contains a ripple voltage which has a frequency equal to that of the ac source.

As stated previously, the regulation of a voltagetripler circuit is relatively poor; therefore, the value of the output voltage obtained from the voltage tripler is determined largely by the resistance of the load and the resulting load current. The output of each of the circuits illustrated requires filtering to obtain a steady dc voltage. (Filter circuits are discussed in the Filter Section of this handbook.)

# Failure Analysis.

**No Output.** In the voltage-tripler circuit, the nooutput condition is likely to be limited to be limited to one of several possible causes: the lack of applied ac voltage (including the possibility of an open surge resistor, Rs, or a defective stepup or isolation transformer), a shorted load circuit (including filter circuit components), open charging capacitors (dependent upon circuit configuration), or defective rectifiers.

The ac supply voltage should be measured at the input to the circuit to determine whether the voltage is present and is the correct value. If the circuit uses a stepup or isolation transformer, measure the voltage at the secondary terminals to determine whether is is present and is the correct value. If necessary, the primary voltage should be removed from the transformer and continuity measurements of the primary and secondary windinga made to determine whether one of the windinga is open, since an open circuit in either winding will cause a lack of secondary voltage.

If the circuit includes a surge resistor, Rs, a resistance measurement can be made to determine whether the resistor is open. If the resistor is found to be open, the voltage tripler and the load (including filter) circuit should be checked further to determine whether excessive load current, a defective rectifier, or a shorted capacitor has caused the resistor to act as a **fuse** and to open.

With the ac supply voltage removed from the output to the circuit and with the load (including filter circuit) disconnected from the load terminal of capacitor C2, resistance measurements can be made across the load to determine whether the load circuit (including falter components) is shorted. Measurements should be made across the terminals of charging capacitors C2 and C3 in the tripler circuit shown in part

A, or across charging capacitor C2 in the tripler circuit of part B or part C, to determine whether the no-output condition is caused by shorted capacitors. The tripler circuit shown in part A includes resistors RI and R2; therefore, the resistance value measured across capacitors C2 and C3 will normally be something less than the value of the associated bleeder resistor. Since the charging capacitors are electrolytic capacitors, the resistance measurements will vary, depending upon the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the capacitor terminals for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value. Capacitor Cl maybe checked in a similar manner.

The rectifiers should be checked to determine whether they are open or otherwise defective. A relative check of rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. However, failure of one or more rectifiers may be the result of other causes; therefore, tests of the falter and load circuit are necessary.

**Low Output. The** ac supply voltage should be measured at the input of the circuit to determine whether the voltage is the correct value, since a low applied voltage can result in a low output voltage.

Each rectifier (CR1, CR2, and CR3) should be checked to determine whether the low output is due to normal rectifier aging. A relative check of rectifier condition can be made by use of an ohmmeter, as outlined in a previous paragraph of this section. If the forward resistance of the rectifier increases, the output voltage will decrease. Also, if the reverse resistance decreases, the output voltage will decrease.

The load current should be checked to make sure that it is not excessive, because the voltage-tripler circuit has poor regulation and an increase in load current (decrease in load resistance) can cause a decrease in output voltage.

One terminal of each charging capacitor (Cl, C2, and C3) should be disconnected from the circuit and each capacitor checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance. A decrease in effective capacitance or losses within the capacitor can cause the output of the voltage-tripler circuit to be below normal, since the defective capacitor will not charge to its normal operating vahre. If a suitable capacitance analyzer is not available, an indication of leakage resistance can

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be obtained by use of an ohmmeter. First, disconnect one terminal of the capacitor from the circuit; then, using the ohmmeter procedure outlined for the nooutput condition, make two measurements (reverse the test leads at the capacitor terminals for one of the measurements). The larger of the two measurements should be greater than 1 megohm for a satisfactory capacitor.

# VOLTAGE QUADRUPLE (ELECTRON TUBE)

# Application.

The voltage-quadrupler circuit is used to produce a higher dc output voltage than can be obtained from a conventional rectifier circuit utilizing the same input voltage. It is normally used in "transformerless" circuits where the load current is small and voltage regulation is not critical.

### Characteristics.

Input to circuit is ac; output is pulsating dc.

DC output voltage is approximately four times the voltage obtained from a half-wave rectifier circuit utilizing the same input voltage; output current is relatively small.

Output requires filtering; dc output ripple frequency is either equal to or twice the ac source frequency, depending upon quadruple circuit arrangement.

Has poor regulation characteristics; output voltage available is a function of load current.

Depending upon circuit application, may be used with or without a power or isolation transformer.

Uses indirectly heated cathode-type rectifiers.

# Circuit Analysis.

General. The voltage-quadrupler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term voltage quadruple implies, the output voltage is approximately four times the input voltage. The voltage regulation of the voltage quadruple is very poor as compared with the regulation of either the half-wave or the full-wave voltage doubler circuit. Assuming that a given voltage-multiplier (doubler, tripler, or quadruple) circuit uses the same value of capacitors in each instance, the greater the voltage-multiplication factor of the circuit, the poorer will be the regulation characteristics. Because of the poor regulation characteristics of the voltage quadruple, the use of the circuit is generally restricted to applications in which the load current is small and relatively constant.

**Circuit Operation. Two** basic voltage-quadrupler circuits are shown in the accompanying circuit schematic. Each circuit (part A or part B of the illustration) consists of two half-wave voltage doublers arranged so that the output of one doubler circuit is in series with the output of the other; thus, the total



Basic Cascade Voltage-Quadruplar Circuits

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output voltage developed across the load resistance is approximately four times the applied voltage.

Rectifiers V3 and V4 and charging capacitors Cl and C4 form a conventional half-wave voltage-doubler circuit (the operation of the voltage-doubler circuit was previously described in this section). Rectifiers VI and V2 and charging capacitors C2 and C3 form a second half-wave voltage-doubler circuit; however, this voltagedoubler circuit operates in cascade with the first voltagedoubler circuit and obtains its input from the voltage available across the series combination of charging capacitor Cl, the applied ac input voltage, and charging capacitor C4.

Rectifiers VI, V2, V3, and V4 are identical-type diodes with indirectly heated cathodes. Because there are several possible filament circuit arrangements, the actual filament circuits are not shown on the schematic. It is necessary to isolate the rectifier filament circuits from each other because of the heater-to-cathode breakdown voltage limitation imposed by the rectifier tubes themselves; therefore, a filament transformer with separate well-insulated secondary windings, or a single transformer for each rectifier tube, is required. This requirement for an independent filament (heater) voltage source for each rectifier tube places a practical limitations on the use of electron tubes in voltage-multiplier circuits; for this reason, the voltage-quadrupler circuit and other voltage-multiplier circuits generally employ semiconductor diodes as rectifiers in lieu of electron-tube diodes.

Charging capacitors Cl, C2, C3, and C4 are of equal capacitance and are usually relatively large (10 to 20  $\mu$ f) for 50- to 60-hertz ac input; however, for some high-voltage, low-current applications, such as in the high-voltage supply for cathode-ray tube indicators, the charging capacitors may be relatively small (0.01 to 0.1  $\mu$ f), especially if the ac input frequency is much higher than the normal 50- to 60-hertz input frequency.

Resistors R1 and R2 are equalizing resistors for charging capacitors C3 and C4, respectively; they are of equal value and are generally greater than 2 megohms. Resistors R1 and R2 are not necessary for circuit operation; however, when included in the circuit, they have a dual purpose–they tend to equalize the voltage across charging capacitors C3 and C4, and

they also act as bleeder resistors to discharge the capacitors when the circuit is de-energized.

The operation of the basic voltage-quadrupler circuit can be understood from the simplified circuits, part A, B, C, and D, given in the accompanying illustration. These simplified circuits are based upon the basic voltage-quadrupler circuit schematic (part A) given earlier in this discussion. The operation of a typical half-wave voltage-doubler circuit was described earlier in this section of the handbook; therefore, the discussion which follows will ordy briefly describe the circuit operation when two voltagedoubler circuits are arranged in cascade to obtain voltage-quadrupler action.





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# **ELECTRONIC CIRCUITS**

Assume that the ac input to the voltage-quadrupler circuit (during the initial half-cycle) has the polarity indicated by the signs adjacent to the input terminals in part A of the accompanying illustration. Rectifier V4 conducts to charge capacitor Cl to the peak value of the applied ac input voltage. In part B of the illustration (during the next half-cycle) the applied voltage has the polarity indicated by the signs at the input terminals and is in series with the charge on capacitor Cl ( $E_{c1}$ ); hence, rectifier V3 conducts to charge capacitor C4 to twice the peak value of the applied voltage and thereby discharge capacitor Cl. In part C of the illustration, the applied voltage has the polarity indicated and is in series with the charge on capacitor C4 ( $E_{ci}$ ) which causes rectifier V2 to conduct. This action charges capacitor C2 to twice the peak value of the input voltage, capacitor Cl to the peak value of 'the input voltage, and discharges capacitor C4 to zero. In part D of the illustration, the applied voltage has the polarity indicated and is in series with the charge on capacitor Cl (E<sub>d</sub>) and capacitor C2 ( $E_{C2}$ ). At this time rectifier V1 conducts charging capacitors C3 and C4. Capacitors C3 and C4 are equal value capacitors and each will charge to twice the peak value of the applied voltage (ac input plus EC 1 and EC2.) Since C3 and C4 are in series, the dc voltage delivered to the load resistance is the sum of the voltage (EC<sub>3</sub> plus EC<sub>4</sub>) developed across capacitors C3 and C4. Because the voltage across each of these capacitors is equal to twice the applied voltage, the value of the dc output voltage is approximately four times the peak voltage of the ac input to the voltage-quadrupler circuit.

The dc output contains a rippler component; therefore, filtering is required to obtain a steady dc voltage. The frequency of the main component of the ripple voltage is equal to the frequency of the ac source because capacitors C3 and C4 simultaneously receive a charge, once for each complete cycle of the applied voltage. The value of the output voltage obtained from the voltage quadruple is determined largely by the resistance of the load and the resulting load current. The regulation of the circuit is very poor; for this reason, if the output voltage is to be maintained at a high level, the load current must be kept small.

The voltage-quadrupler circuit given in the accompanying circuit schematic is a variation of the basic cascade voltage-quadrupler circuits given earlier.



Two Half-Wave Voltage-Doublers Connected Back-to-Back To Form a Voltage-Quadrupler Circuit

In this circuit, two basic half-wave voltage-doubler circuits are arranged back-to-back; each doublercircuit input is connected to the common ac source, and the two output voltages,  $E_{C3}$  and  $E_{C4}$ , are in series to produce the total output voltage, e. Rectifiers V1 and V2 and charging capacitors Cl and C3 form one doubler circuit; rectifiers V3 and V4 and charging capacitors C2 and C4 form the other doubler circuit. Each doubler circuit operates to charge its associated output capacitor (C3 or C4) to a value which is twice the peak value of the applied input voltage; as a result, the voltage produced across capacitors C3 and C4, in series, is four times the value of the applied input voltage. Because charging capacitors C3 and C4 receive a charge on alternate half-cycles of the applied input voltage, the ripple frequency for this quadruple circuit is equal to twice the frequency of the ac source.

Once it is recognized that this quadruple circuit consists of two complete half-wave voltage-doublers connected back-to-back sharing a common input input source and that measurements on each doubler

circuit may be made as though they were two independent circuits, then failure analysis becomes relatively simple. The circuit operation and failure analysis for each doubler circuit is identical to that given for the basic half-wave voltage-doubler circuit described earlier in this section of the handbook and, therefore, will not be discussed here.

The operation of these quadruple circuits can be readily understood from a study of equivalent electron-tube circuit descriptions given previously in this section of the handbook. The action of the semiconductor rectifiers in the quadruple circuit is essentially the same as that described for the equivalent electron-tube circuit. For these reasons, an explanation of circuit operation is not given here.

In the circuit shown in part A, charging capacitors C3 and C4 are in series across the load resistance, and each capacitor simultaneously receives a change, once for each complete cycle of the applied voltage; as a result, the output ripple voltage has a frequency which is equal to the freqency of the ac source. In part B, charging capacitor C4 in parallel with the load resistance is charged only on alternate half-cycles of the applied ac voltage; therefore, the frequency of the ripple voltage is the same as the frequency of the ac source. In part C, charging capacitors C3 and C4 are in series across the load resistance, and the capacitors receive a charge on alternate half-cycles of the applied voltage; as a result, the output ripple voltage for this circuit has a frequency which is equal to twice the frequency of the ac source.

Since all three circuits described contain a ripple voltage, additional filtering is required to obtain a steady dc voltage. (Filter circuits are discussed in the Filter Section of this handbook.)

As stated previously, the regulation of the voltage quadruple is relatively poor; the value of the output voltage obtained is determined largely by the resistance of the load and the resulting load current. If the load current is large, the output voltage is reduced accordingly.

#### Failure Analysis.

**No Output.** In the voltage-quadrupler circuit, the no-output condition is likely to be limited to one of serveral possible causes: the lack of applied ac voltage (including the possibility of an open surge resistor, Rs, or a defective step-up or isolation transformer), a shorted load circuit (including filter circuit com-

ponents), open charging capacitors (dependent upon circuit configuration) or defective rectifiers.

The failure analysis procedures for the no-output condition, such as voltage and resistance measurements, and capacitor and rectifier checks, etc, are essentially the same as those given for the voltagetripler and voltage-doubler circuits described previously in this section of the handbook. Therefore, these procedures are not repeated here.

Low Output. The failure analysis procedures for the low-output condition consist of voltage, resistance, and load-current measurements, capacitor and rectifier checks, etc. These procedures are essentially the same as the procedures given for the voltagetripler circuit described previously, and are somewhat similar to those given for the half-wave voltagedoubler circuit described earlier in this section of the handbook.

#### Failure Analysis.

**No Outnut.** In the voltage-quadrupler circuit, the no-output condition is likely to be limited to one of the following possible causes: the lack of filament voltage or an open filament in two or more rectifiers, the lack of applied ac voltage, a shorted load circuit (including filter circuit components), or an open in one or both of the charging capacitors, Cl and C2.

The failure analysis procedures for the no-output condition are essentially the same as those given for the voltage-tripler and half-wave voltage-doubler circuits described previously in this section of the handbook.

Low Output. The failure analysis for the lowoutput condition is essentially the same as that given for the voltage-tripler circuit described previously and is somewhat similar to that given for the half-wave voltage-doubler circuit described earlier in this section of the handbook.

### VOLTAGE QUADRUPLE (SEMICONDUCTOR)

#### Application.

Same application as the electron tube version.

# Characteristics.

Same characteristics as the electron tube version except that it uses four semiconductor rectifiers

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(single, multipler, or stacked units) instead of electron tubes.

# Circuit Analysis.

General. The voltage-quadrupler circuit is used with or without a transformer to obtain a dc voltage from an ac source. As the term voltage quadruple implies, the output voltage is approximately four times the input voltage. The voltage regulation of the voltage quadruple is very poor as compared with the regulation of either the voltage-doubler or voltagetripler circuit. Assuming that a given voltagemultiplier (doubler, tripler, or quadruple) circuit uses the same value of capacitors in each instance, the greater the voltage-multiplication factor of the circuit, the poorer will be regulation characteristics. Because of the poor regulation characteristics of the voltage quadruple, the use of the circuit is generally limited to applications in which the load current is small and relatively constant.

Circuit Operation. Three voltage-quadrupler circuits are shown in the accompanying illustration. The schematic of part A shows a basic cascade voltagequadrupler circuit; fundamentally, this circuit consists of two voltage doublers whose outputs are in series. The schematic of part B shows a circuit arrangement which is a variation of that given in part A. The schematic of part C is a quadruple circuit consisting of two complete half-wave voltage-doublers connected back-to-back and sharing a common ac input. The circuits shown in parts A and B have the negative output terminal common to one side of the ac source; both of these circuits can be arranged to have the positive output terminal common to one side of the ac source by simply reversing the connections to each rectifier (CR1 through CR4) and to each charging capacitor (Cl through C4).



Voltage-Quadrupler Circuits

The rectifiers, CR1, CR2, CR3, and CR4, are identical-type semiconductor diodes in each of the three circuits illustrated. Charging capacitors Cl, C2, C3, and C4 are of equal capacitance value in each of the three circuits; however, because of the differences

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in the voltages developed across individual capacitors in a particular circuit, the voltage ratings of the capacitors will differ. In the circuit of part A, the voltage rating of capacitors C3 and C4 is the same for each capacitor; the voltage rating of capacitor C2 is less than that of C3 or C4, and the rating of capacitor Cl is less than that of C2. In part B, the voltage rating of capacitors C2 and C4 is the same for each capacitor; the rating of C3 is less than that of C2 or C4, and the rating of C1 is less than that of C3. In part C, the voltage rating of capacitors C3 and C4 is the same for each capacitor, and the rating of capacitors C1 and C2 is the same for each capacitor; however, the rating of capacitors C1 and C2 is less than that of C3 and C4.

Equalizing resistors RI and R2, shown in the circuits of parts A and C, are not necessary for circuit

operation; however, when they are included in the circuit, resistors R1 and R2 equalize the voltages developed across capacitors C3 and C4, respectively, and also act as a bleeder to discharge the capacitors when the circuit is de-energized. A surge resistor, Rs, is placed in series with the ac source *to* limit the peak current in the rectifier circuit.

One disadvantage common to all three quadruple circuits illustrated is that neither dc output terminal can be directly connected to ground or to the chassis; however, when a step-up or isolation transformer is used to supply the input to any one of these quadruple circuits, either output terminal may be connected to ground or to the chassis. Furthermore, if a transformer is used and if there is sufficient resistance in the secondary winding, the surge resistor, Rs, may be omitted.

# PART 2-4. DC-TO-DC CONVERTERS

# DC-TO-DC CONVERTER, AUDIO OSCILLATOR TYPE (ELECTRON TUBE)

# Application.

**The** audio-oscillator type de-to-de converter is used in electronic equipment for applications requiring extremely high-voltage dc at a small load current. The output circuit can be arranged to furnish negative or positive high voltage to the load. The supply is commonly used to provide the high voltage for accelerating and final anodes, ultor (element with highest voltage) and other similar electrodes of cathode-ray tubes used in indicators. It is sometimes used as a keep-alive voltage source in radar equipment.

#### Characteristics.

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Uses a self-excited oscillator circuit combined with a full-wave voltage doubler circuit.

Typical operating frequency is between 400 to 3000 Hz.

Output is high-voitage dc at low current.

Regulation is fair; may be improved by regulating oscillator dc supply voltage.

The rectifier circuit can be arranged to provide either positive- or negative-polarity output voltage.

#### **Circuit Analysis.**

General. The audio-oscillator type dc-todc conveter is a self+ xcited oscillator operation in the audiofrequency range. The oscillator generates a voltage which is either sinusoidal or square wave in form, depending upon the circuit design. The rectifier circuit used in conjunction with the oscillator circuit is commonly a half-wave rectifier or a full-wave voltage-doubler circuit and uses either electron tubes or semiconductor diodes as rectifiers. The dc output filter component values are determined by the desired output impedance of the high-voltage supply and by the frequency of the applied ac generated by the oscillator circuit. In most cases, the output impedance is given first consideration in the design of the filter circuit, rather than the reduction or elimination of the ripple-frequency component from the dc output.

The dc output of a self-excited oscillator supply under a given load, such as the load offered by a cathode-ray tube circuit, can be maintained nearly as constant as the dc source supplying the oscillator circuit. For this reason, it is desirable to provide the oscillator circuit with a regulated supply voltage which approaches  $\pm 1$  percent so that the output voltage can be maintained reasonably constant for a given load current.

**Circuit Operation. The accompanying** circuit schematic illustrates a push-pull, self-excited oscillator circuit used in conjunction with a full-wave voltagedoubler circuit to obtain high-voltage output. The operation of the self-excited, push-pul! oscillator is essentially the same as that described in the Oscillator Section of this handbook; the operation of a typical full-wave voltage-doubler circuit has already been described in this section of the handbook. For these reasons, the discussion which follows will be somewhat limited **because** the circuit is a combination of two basic circuits discussed elsewhere in this handbook.



# DC-TO-DC CONVERTER, Audi@ Oscillator Type Using Twin-Triode Tube

Electrode tube VI is a twin-triode, such as the type 5670 or 6J6? if desired, two identical-type triode tubes may be used in this circuit in lieu of the single twin-triode. Electron tubes V2 and V3 are identical diodes using directly-heated cathodes, such as the type 1B3, 1V2, or 1X2, and are specifically

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designed for high-voltage applications. The parallel combination of resistor R1 and capacitor Cl is used to obtain operating (grid-leak) bias for the selfexcited oscillator circuit. Transformer T1 is the oscillator and high-voltage transformer; in the schematic the dots adjacent to windings L1, L2, L3, and L4 are used to indicate similar winding polarities. Windings L1 and L4 are the push-pull oscillator grid windings, and windings L2 and L3 are plate windings. Capacitor C2 forms a resonant circuit with the inductance of windings L2 and L3 to determine the frequency of oscillation. Transformer windings L5 and L6 supply the fdament current to the diodes, V2 and V3, respectively. Although windings L5 and L6 are shown as part of transformer Tl, a separate filament transformer with independent, well-insulated windings is sometimes used as the fdament supply. (A fdament supply is not necessary when semiconductor diodes are used in the rectifier circuit, and windings L5 and L6 maybe omitted.) Transformer winding L7 is the high-voltage (step-up) winding and is the ac source for the rectifier circuit. Depending upon the design of the transformer and the circuit constants used, the oscillator circuit generates a sinusoidal waveform at the high-voltage winding, or, if the circuit operates in a switching mode, it generates a square wave.

Capacitor C3 and variable resistor R2 form a decoupling falter to prevent interaction between the oscillator circuit and the dc supply. Resistor R2 is also used to vary the dc potential applied to the oscillator circuit. A change in the applied voltage affects the amplitude of the voltage across winding L7 which is applied to the rectifier circuit; therefore, the setting of resistor R2 determines the high-voltage output within certain limits and may be adjusted to obtain a predetermined output voltage.

Capacitors C4 and C5 are the charging capacitors of the voltagedoubler circuit. Since the frequency of the applied voltage is in the audio range and the load current is small, the value of these capacitors is relatively small. Resistors R3, R4, and R5 in series form a bleeder and a voltage-divider resistance for the output of the doubler circuit. The tap at the junction of **resistors** R3 and R4 enables a lower voltage to be supplied to a low-current load, **such as the** lowervoltage electrodes of a cathode-ray tube. In actual practice, resistors R3 and R4 are made up of a number of resistors in series to obtain the desired value of total resistance for each portion of the bleeder (R3 and R4). To prevent failure, the voltage drop across each resistor must be less than the maximum terminal-voltage rating of the resistor.

Resistor R5 is used for test metering purposes, to permit measurement of the high-voltage dc output without the requirement for a special voltmeter or high-voltage probe. A precalculated voltage drop across R5, when read with a high-resistance voltmeter, will indicate the presence of the correct value of high voltage.

In general, the output-voltage regulation of this supply is sufficient for most cathode-ray-tube circuit applications since the stability of the output voltage can be held to  $\pm 1$  percent by regulating the dc supply voltage applied to the oscillator circuit.

The oscillator circuit using a twin-triode tube offers several advantages; its efficiency is relatively high and it requires fewer parts than does a comparable circuit which uses a single pentode. Furthermore, the reliability of the twin-triode oscillator circuit is better than that of a comparable pentode circuit, because it has the ability to oscillate even after failure of one triode section of the tube. If a failure of this nature should occur at a time when continued operation isvital to the mission, sufficient voltage will normally be available to sustain emergency operation with reduced efficiency until corrective maintenance can be performed.

The accompanying circuit schematic illustrates a single pentode used in a self-excited oscillator circuit to produce a sinusoidrd voltage. The oscillator is fundamentally a series-fed Hartley oscillator with grid stabilization; the operation of this circuit is similar to that of the conventional Hartley oscillator described elsewhere in this handbook. The rectifier circuit commonly used with the pentode oscillator is a fidl-wave voltage doubler and employs neither electron tubes or semiconductor diodes as rectifiers; however, the schematic does not show the associated rectifier circuit because it can be the same as that illustrated for the twin-triode oscillator given earlier in this discussion.




DC-to-DC Converter, Audio-oscillator Type Using Pentode Tube

Electron tube VI is a pentode such as the type 5763. The parallel combination of resistor R1 and capacitor Cl is used to obtain operating bias for the self-excited oscillator circuit. Transformer T1 is the oscillator and high-voltage transformer. In this transformer, winding L1 is tapped for the series-fed oscillator circuit and is in parallel with capacitor C4 to determine the resonant frequency of the oscillator. Winding L2 is the high-voltage winding and is the ac source for the rectifier circuit. (The pentode oscillator circuit generates a sinusoidal waveform.) Although not shown, if electron-tube diodes are used in the rectifier circuit, additional windings may be required to supply the rectifier filament current. Capacitor C3 couples the grid of V1 to the gridwinding portion of L1 and also acts as a dc blocking capacitor. Capacitor C2 is the screen bypass, and resistor R2 is the screen-dropping resistor. Capacitor C5 and resistor R3 forma decoupling filter; capacitor C5 also returns the tap of winding L1 to signal ground (cathode) potential.

The pentode oscillator circuit found in various equipments may differ somewhat from the circuit given in the accompanying schematic. Several typical variations are as follows: A small capacitor **may** be connected between the control gird and the plate of VI to increase the **grid-to-plate** capacitance and thus provide additional feedback to sustain oscillator; a resistance may be placed in series with capacitor C3 to help stabilize the circuit and limit the amplitude of oscillations; and a variable resistor may be **placed** in series with either screen-dropping resistor R2 or decoupling resistor R3 to **permit adjustment** of the screen voltage or both the plate and screen voltages. A change in the applied oscillator voltage(s) will affect the output amplitude of the oscillator and will therefore affect the high-voltage output of the supply.

#### Failure Analysis.

Ganaral. T'he audio-oscillator type de-to-de converter consists of two basic circuits-an oscillator and a rectifier. It must be determined initially whether the oscillator or the rectifier portion of the powersupply circuit is at fault. Tests must be made to determine whether the oscillator is performing satisfactorily; if it is, the trouble is then assumed to be located within the associated rectifier circuit. The failure analysis outlined in the following paragraphs is somewhat brief because the subject of electron-tube oscillators is discussed in another section of this handbook; furthermore, the particular high-voltage rectifier circuit may be the same as one of the rectifier circuits described earlier in this section. Since the audio-oscillator type de-to-de converter is a combination of two basic circuits, information concerning failure analysis for either portion of the high-voltage supply can be obtained by reference to the applicable basic circuit given elsewhere in this handbook.

No Output. When the oscillator is in a nonoscillating condition, negative grid voltage will not be developed across RIC1, and the measured plate (and screen) voltage of oscillator tube V1 will be below normal. The applied filament and plate (and screen) voltages should be measured to determine whether these voltages are present and of the correct value. The oscillator tube V1 should be checked to determine if it is defective. Excessive losses in the L-C resonant circuit formed by the transformer and its associated capacitor will prevent sustained oscillation; the transformer windings should be checked for continuity, and the associated capacitor should be checked to determine whether it is open or shorted. Shorted capacitor in the circuit will prevent oscillation; therefore, all capacitors should be checked with a suitable capacitance analyzer to determine whether they are satisfactory. An open transformer winding

would normally prevent sustained oscillations, however, in the twin triode oscillator circuit, there is a possibility that one coil could resonate with stray capacity and oscillate (at a higher frequency) and produce *a low* output.

If the oscillator circuit is found to be functioning normally, then it must be assumed that the trouble is associated with the rectifier circuit or its load, and a check of the rectifier circuit must be made in accordance with the procedures outlined earlier in this section for the applicable rectifier circuit.

Low Output. A relative indication of oscillator output can be obtained by measuring the amount of bias voltage developed across **R1C1**. A value of bias which is below normal is an indication of low oscillator output. Also, if the applied plate (and screen) voltage *is* below normal, *a* reduction in output will occur. The applied filament and plate (also screen) voltages should be measured to determine whether they are within tolerance; a 10-percent variation in applied filament voltage will not appreciably affect the output of the supply, but a small change in applied plate voltage **will** produce a noticeable change in output.

In the twin-triode oscillator circuit, trouble in one triode section (such as low cathode emission, Iow transconductance, or an open tube element) or an open winding in transformer T1 will cause a reduction in output. Continuity measurements of the windings of transformer T1 can be made to determine whether any of the windings are open. In the pentode oscillator circuit a leaky screen bypass (C2) will form a voltage divider with the screen-dropping resistor (R2) and a result in a decreased screen voltage; thus, the output of the supply will be low.

If the oscillator is found to be operating normally, a defect within the rectifier circuit or associated load must be suspected as the cause of low output. For example, because of the relatively high-impedance rectifier and **filter** circuits, an excessive load current can cause the output voltage to be low. Failure analysis procedures for typical rectifier circuits used in high-voltage supplies are outlined earlier in this section.

# DC-TO-DC CONVERTER, SQUARE-WAVE (AUDIO) OSCILLATOR TYPE (SEMICON-DUCTOR)

# Application.

**Same** application as electron tube audio oscillator type.

# Characteristics.

Same characteristics as electron tube audio oscillator type, except that typical operating frequency is between 400 and 2000 Hz.

#### Circuit Analysis.

General. The square-wave oscillator type de-to-de converter includes a self-excited oscillator which has an operating frequency in the range between 400 and 2000 Hertz. The oscillator circuit operates most efficiently as a square-wave generator with the transistors functioning as high-speed switching elements. The transistors provide a form of astable, or freerunning, multivibrator circuit; the action can be compared to the switching action which occurs with a mechanical vibrator in a nonsynchronous vibrator supply. The oscillator circuit is frequently referred to as a saturable core square-wave oscillator. The square-wave output from the oscillator circuit may be stepped u, or down and rectified to provide a dc voltage higher or lower than the input voltage. The circuit described here is used in conjunction with a full-wave voltage-doubler circuit to obtain high-voltage dc. Because of the square-wave output and the relatively high frequency of oscillation, very little filtering is required to eliminate the ripple voltage from the output; this is especially true when a full-wave rectifier circuit is used.

**Circuit Operation. The** accompanying circuit schematic illustrates a push-pull, self excited oscillator circuit used in conjunction with a full-wave voltagedoubler circuit to obtain a high-voltage output. The discussion which follows is limited to the oscillator circuit, since the operation of a typical **full-wave** voltage-doubler circuit has been described earlier in this section of the handbook.



DC-to-DC Converter, Square-Wave Oscillator Type Using PNP Power Transistors

Transistors QI and Q2 are identical PNP, alloyjunction type, power transistors. The power transistors used in this common-emitter circuit **configura**tion normally have the collector connected to the case or shell of the transistor; thus, the circuit shown here permits the collectors to be in physical and electrical contact with a metal chassis or a grounded heat sink. Rectifiers CR1 and CR2 are identical semiconductor diodes; although the schematic shows only two rectifiers in the voltage-doubler circuit, each **graphic** diode symbol represents two or more diodes in series to obtain the necessary peak-inverse characteristics for high-voltage operation in the voltagedoubler circuit.

Transformer T1 provides the necessary regenerative feedback coupling from the emitter to the base of the power transistors, Q1 and Q2, and is also the source of high voltage for the rectifier circuit. Transformer windings L2 and L3 are emitter windings; L1 and L4 are the feedback, or base, windings. The load for the transistors is formed by windings L2 and L3 connected between the emitters and the voltage source. Transformer winding L5 is the highvoltage (step-up) winding, and is the ac source for the voltage-doubler circuit. In the schematic, the dots adjacent to the transformer windings are used to indicate similar winding polarities.

Resistors R1 and R2 form a voltage divider to provide forward-bias voltage for the base of transistor Ql, in like reamer, resistors R3 and R4 establish the bias for the base of **transistor** Q2. Separate voltage dividers are used in this push-pull circuit to provide an independent base-voltage source for each transistor and thereby increase the reliability of the circuit. In the event of failure of one transistor, such as an open circuit in one of the transistor junctions, the independent base-biasing arrangement enables the remaining tansistor of the oscillator circuit to continue operation at reduced efficiency, and the dc output of the power supply is reduced accordingly.

Capacitors Cl and C2 are the charging capacitors of the voltage-doubler circuit. Since the frequency of the applied voltage is generally between 400 and 2000 Hz, the vahre of these capacitors is relatively small, usually between 5600 pf and 0.02  $\mu$ f. Resistors R5, R6, and R7 in series form a bleeder and voltage-divider resistance for the output of the doubler circuit. The tap at the function of resistors R5 and R6 enables a low voltage to be supplied to a low-current load, such as the lower-voltage electrodes of a cathode-ray tube. In actual practice, resistors R5 and R6 are made up of a number of resistors in series to obtain the desired value of total resistance for each portion of the bleeder (R5 and R6). To prevent failure, the voltage drop across each resistor must be less than the maximum terminal-voltage rating of the resistor.

Resistor R7 is used as a shunt resistor for test metering purposes, to permit measurement of the high-voltage dc output without the requirement for a special voltmeter or high-voltage probe. The test points located at each end of R7 permit a lowresistance microammeter to be connected across the resistor; in this case the bleeder resistance (R5 and R6) is used as a series multiplier for the test microammeter. When this test circuit is employed, the highvoltage output can be calculated by using Ohm's law, once the bleeder current is determined by measurement and the total resistance of R5 and R6 is known. As an alternative, an electronic voltmeter can be connected to the test points, to measure the voltage drop

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across R7; the output voltage can then be calculated by taking into account the voltage division provided by the bleeder resistance. In other cases, a predetermined (calculated) voltage drop across R7, when measured by use of a high-resistance voltmeter, will indicate the presence of the correct value of highvoltage output.

The operation of transistors functioning as highspeed switching elements can be understood by reference to the accompanying illustration below for a fundamental switching circuit. The reference designations used for the windings of transformer T1 in the illustration correspond to those used in the schematic given earlier in this discussion.



# Fundamental Switching Circuit and Rasulting Output Waveform

The switching action, such as occurs with a **mechanical** vibrator, is represented in the simplified schematic by ganged switches SW1 and SW2, mechanically linked together so that when one switch is

closed, the other switch is opened. When switch SW1 is open (transistor Q1 cut off), switch SW2 is closed (transistor Q2 conducting heavily), as shown in part A of the illustration, and heavy current flows in transformer winding L3. When the switches are reversed, as shown in part B, switch SW1 is closed (Ql conducting heavily) and switch SW2 is open (q2 cut off); thus, heavy current flows in winding L2. The polarities of the voltages produced across the primary and secondary windings are as indicated in parts A and B of the illustration. Assuming a rapid rate of switching, the resulting output voltage developed across secondary winding L5 is essentially a square waveform, as shown in part C.

Bias and stabilization techniques employed for a transistor oscillator are essentially the same as those employed for a transistor amplifier. The grounded-collector, common-emitter configuration illustrated earlier in the discussion utilizes a single-battery power source; as mentioned previously, this dc source produces the required bias voltages through the voltage-divider action of resistors RI and R2, and resistors R3 and R4. Since the connector is at negative (ground) potential and the emitter is at a positive potential, each pair of resistors form a voltage divider to place the base of the associated transistor as a negative potential with respect to its emitter; the required forward bias for the PNP transistor is thereby established.

The square-wave oscillator can be compared to an amplifier with feedback of the proper phase and amplitude. In the PNP transistor schematic given earlier, feedback is obtained by transformer coupling from the emitter to the base in order to sustain oscillations; the feedback signal must be in phase with the emitter signal. If NPN transistors are used in the oscillator circuit, the polarity of the supply voltage must be opposite to that indicated in the schematic; however, for either type of transistor the feedback signal must be in phase with the emitter signai.

When dc power is first applied to the circuit, the current which flows through each primary winding, L2 and L3, is initially determined by the effective resistance offered by transistors Q1 and Q2, and their associated bias **resistors** RI and R2 and resistors R3 and R4. The push-pull circuit **appears** to be balanced, since each half of the circuit is identical to the other; however, there will always be minor differences in circuit resistance and within the transistors themselves. As a result of this inherent unbalance, the

initial current in one primary winding of transformer T1 does not exactly equal the initial current in the other. It is this unequed current flow in primary windings L2 and L3 which starts the oscillation in a manner which is typical of free-running miltivibrators or relaxation oscillator

In order to compare the action of the square-wave oscillator with the action of the fundamental switching circuit, assume that more current flows through primary winding L3 than flows through primary winding L2 because of the circuit unbalance mentioned previously. As emitter-current flow increases through winding L3, a voltage is induced in the feedback (or base) winding, L4. This voltage is in phase with the voltage produced across winding L3. The induced voltage across L4 effectively increases the forward bias, and transistor Q2 rapidly approaches saturation. As this regenerative process continues, core saturation is eventually reached; at this time no further increase in the emitter current through L3 can occur, and the effective inductance of the transformer windings decreases. The flux in the core of transformer T1 during this period has changed from point O to point A on the hysteresis curve, as shown in the accompanying illustration.



Core Hysteresis Curve

During the interval the transistor Q2 is approaching saturation, voltage is induced in winding L1 by the resultant field of L2 and L3. This induced voltage is in opposition to the initial voltage developed when the dc supply voltage was first applied to the circuit. As a result of the action occurring in the circuit associated with transistor Q2, the voltage across winding L1 causes the base of transistor Q1 to approach a condition of reverse bias. The emitter current of transistor Q1 decreases rapidly, and Q1 reaches cutoff because the feedback from winding L1 has driven the base of Q1 to a condition of reverse bias. Since no further increase or change in current through L3 occurs, the base of transistor Q2 is no longer driven by a voltage from L4, and it starts to return to the normal (forward) bias condition. Also, the magnetic flux developed in the core of T1 starts to decrease to point B on the hysteresis curve. Consequently, the voltage induced in L4 starts to drive the base of Q2 to a reverse bias condition. The emitter current of transistor Q2 decreases rapidly and Q2 finally reaches cutoff. As a result of this regenerative process, the magnetic flux developed in the core rapidly changes from point B on the hysteresis curve. At the same time, transistor Q1 receives a signal from L1 and its base is driven toward the forward bias condition. Q1 conducts heavily, causing the flux in the core to reach point C. During the interval when transistor Q1 is at saturation, no further change in the current through winding L2 occurs; thus, the base of transistor Q1 is no longer driven by a voltage from Ll, and it starts to return to the normal (forward) bias condition. Also, the magnetic flux developed in the core of T1 starts to decrease to point D on the hysteresis curve. Consequently, the voltage induced in LI starts to drive the base of Q1 to a reverse bias condition.

The emitter current of transistor **Q1** decreases rapidly, and **Q1 finally** reaches cutoff. As a result of this regenerative process, the flux developed in the core rapidly changes from point D on the hysteresis curve. At the same time, transistor Q2 receives a signal from winding L4, and its base is driven into the forward bias condition. Q2 conducts heavily, causing the flux in the core to reach point A once again. At this time, transistor Q2 is at saturation (point A on the hysteresis curve) and transistor Q1 is cut off; the cycle is now complete and ready to be repeated.

The output frequency and secondary voltage are determined by the turns ratio of the transformer windings and by the saturation flux of the core. The core laminations of transformer T1 are usually made of nickel-iron or other material exhibiting similar magnetic characteristics. The nickel-iron material has a high permeability and a square-loop hysteresis curve, which is ideal for use with transistors operating in a switching mode. The transistors, functioning as high-speed switches, operate alternately from cutoff to saturation; when this action is combined with the flux characteristics of the transformer core, the output voltage produced is essentially a square wave. This is because the core flux changes rapidly at a relatively constant rate from point B to point C and from point D to point A on the hysteresis curve.

The output-voltage regulation of this high-voltage supply is sufficient for most cathode-ray-tube circuit applications without additional circuitry, especially if the dc input supply voltage is regulated. The outputvoltage stability could be improved somewhat by the use of a regulator in the collector circuit of the transistors, but the added regulator circuit would become rather complex if stability better than that already provided by the circuit were to be obtained.

The transistorized push-pull oscillator circuit offers several advantages; its efficiency is relatively high, the physical size of the supply is small and much of the circuit can be encapsulated, and the grounded-collector configuration simplifies the method used to dissipate heat developed by the transistors. Furthermore, the circuit has the ability to continue to operate, but with reduced output, even though an open circuit develops in one of the transistors. If a faihrre of this nature occurs at a time when continued operation is vital to the mission, sufficient output voltage will normally be available to sustain emergency operation until corrective maintenance can be performed. With such a failure, the cathode-ray-tube indicator brilliance is likely to decrease somewhat, and an increase in deflection may be noticed.

# Failura Analysis.

**General. The** square-wave oscillator type de-to-de converter consists of two basic circuits - a push-pull oscillator and a voltage doubler. It must be determined initially whether the oscillator or the voltage-doubler portion of the power-supply circuit is at fault. Tests must be made to determine whether the

oscillator is performing satisfactorily, if it is, the trouble is then assumed to be located within the associated voltage-doubler circuit. The failure analysis outlined in the following paragraphs is somewhat brief because the subject of oscillators is discussed in another section of this handbook; furthermore, the voltage-doubler circuit is described earlier in this section. Since the square-wave oscillator type highvoltage supply is a combination of two basic circuits, additional information concerning failure analysis for either portion of the high-voltage supply can be obtained by reference to the applicable basic circuit given elsewhere in this handbook.

No Output. The dc input voltage, Vcc, should be measured to determine whether it is present and of the correct value.

The push-pull oscillator can be quickly checked to determine whether it is oscillating by using an oscilloscope to observe the emitter-to-collector waveform at each transistor. When the push-pull oscillator is functioning normally, the emitter-to-collector waveform is essentially a square wave having a peak-to-peak amplitude which is approximately equal to twice the value of the dc input voltage, Vcc.

Each biasing resistor should be disconnected and, using an ohmmeter, the value of each resistor should be measured to determine whether the resistor is within tolerance. If the vahres of the biasing resistors (Rl through R4) change appreciably, it is likely that the forward bias will change for the associated transistor: if the forward bias increases, such a condition may cause thermal runaway, with eventual damage to the transistor(s) and failure of the circuit to oscillate. Thus, with one transistor conducting heavily or with a shorted junction within the transistor, the resulting current flow in the windings of transformer T1 will cause the effective inductance to be decreased; the core may reach saturation, in which case the circuit will not oscillate because of the loading on the circuit caused by the defective transistor.

Any defect in transformer T1, such as an open base or emitter winding, or shorted turns in any of the windings, will prevent the circuit from operating properly, since oscillations in each half of the circuit depend upon regenerative feedback from the transformer.

A shorted secondary circuit, reflected to the emitter and base windings, may cause excessive losses which will prevent sustained oscillations. Also, if the -

high-voltage winding, L5, should open, the circuit will continue to oscillate; however, no output will be obtained from winding L5 for the input to the voltage-doubler circuit.

If the oscillator circuit is found to be functioning normally, then it must be assumed that the trouble is in the voltage-doubler circuit or its associated load, and a check of the rectifier circuit must be made in accordance with the procedures outlined earlier in this section for the applicable rectifier circuit.

Low Output. The dc input voltage, Vcc, should be measured to determine whether it is of the correct value.

If one transistor should develop an open circuit in one of its junctions, the high-voltage output will decrease (for a given load current), and the peak-topeak amplitude of the ripple voltage will increase. Because of the independent base-biasing arrangement, the remaining good transistor will continue to oscillate. Under these conditions the transformer core may not reach saturation. In this case there will be a reduction in the efficiency of the circuit, together with an accompanying decrease in the output voltage; furthermore, the oscillator frequency will increase to two or three times the normal operating frequency when only one transistor is operating. A calibrated oscilloscope can be used to observe the emitter-tocollector waveform at each transistor. If the oscillator is functioning normally, the emitter-to-collector waveform is essentially a square wave having a peak-to-peak amplitude which is approximately equal to twice the value of the dc input voltage, Vcc. However, if only one transistor is functioning and the other transistor has an open circuit in one of its junctions, the emitter-to-collector waveform will not resemble a square wave on both halves of the cycle; instead it will resemble a square wave for one half-cycle and a trapezoid for the other half-cycle. As mentioned previously, the frequency of oscillation wiU be higher than normal under these conditions.

If the oscillator circuit is found to be operating normally, a defect within the voltage-doubler circuit or associated load must be suspected as the cause of low output. For example, because of the relatively high-impedance rectifier and falter circuits, an excessive load current can cause the output voltage to be low. Faihrre analysis procedures for typical rectifier circuits used in high-voltage supplies are outlined earlier in this section.

# DC-TO-DC CONVERTER, R-F OSCILLATOR TYPE (ELECTRON TUBE)

# Application.

**The** r-f oscillator type high-voltage supply is used in electronic equipment for applications requiring extremely high-voltage dc at a small load current. The output circuit can be arranged to furnish negative or positive high voltage to the load. The supply is commonly used to provide the high voltage for the accelerating and final anodes, the ultor (element with highest voltage), and other similar electrodes of cathode-ray tubes used in video indicators.

#### Characteristics.

Uses a self-excited r-f oscillator circuit combined with a voltage doubler circuit.

Typical operating frequency is between 40 and 600kilohertz.

Output is high-voltage dc at low current.

Regulation is poor; maybe improved considerably by additional circuitry to control the oscillator output.

The rectifier circuit can be arranged to provide either positive- or negative-polarity output voltage.

Circuit may require shielding to prevent undesirable radiation from interfering with other equipments.

# Circuit Analysis.

**Generel. The** r-f oscillator type high-voltage supply is a self-excited oscillator operating in the low- and medium-frequency range. The oscillator generates a sinusoidal output which is coupled through the air-core step-up transformer to the high-voltage rectifier circuit. Sometimes two identicrd oscillator tubes are connected in parallel to increase the current output capability of the supply over that obtainable with single-tube operation. The rectifier circuit used in conjunction with the oscillator circuit is commonly a half-wave rectifier or a voltage-doubler circuit. The rectifier circuit may employ either electron-tubes or semiconductor diodes as rectifiers.

The dc output from the r-f oscillator high-voltage supply is subject to considerable variation with a change in load current, and, therefore, because of its poor regulation characteristics, the use of this circuit is usually limited to applications where the load is

constant. Although the regulation characteristics of the supply can be improved considerably by the addition of regulator circuits to control the **oscillator** output, the additional circuitry required in some causes makes it impracticable to do so because of the added space, weight, number of components, etc.

**Circuit Operation. The** accompanying circuit schematic illustrates a self-excited pentode power oscillator used in conjunction with a full-wave voltagedoubler circuit to obtain high-voltage dc output. The oscillator is fundamentally a series-fed tuned-plate, untuned-grid (tickler) oscillator circuit. The operation of the oscillator is essentially the same as the Tuned-Plate Armstrong Oscillator circuit' described in the **Ocillator** Section of this handbook; the operation of a typical full-wave voltage-doubler circuit has rdready been described in this section of the handbook. For these reasons, the discussion which follows will be somewhat limited.



DCto-DC Converter, R-F Oscillator Type

Electron tube VI is a pentode tube, such as type 6V6 or 6Y6. Electron tubes V2 and V3 are identical directly-heated diodes, such as type 1B3, IV2, or

1X2. The parallel combination of resistor RI and capacitor Cl is used to obtain operating (grid-leak) bias for the self-excited oscillator circuit. The air-core transformer, Tl, is the oscillator tank circuit and high-voltage transformer. Winding L1 is the primary winding of the transformer, and is resonated by tuning capacitor C4 to determine the frequency of oscillation. Winding L2 is the untuned-grid (tickler) coil, which supplies the necessary feedback to the grid of V1 to sustain oscillations. (The ratio of the relative reactance of L1 and L2 determines the exciting voltage for the oscillator grid.) Windings L3 and L4 supply the filament current to the rectifier diodes, V2 and V3, respectively. Winding L5 is the high-voltage (step-up) winding, and is the ac source for the rectifier circuit.

Capacitor C2 is the screen bypass capacitor, and resistor R2 is the screen dropping resistor. Bypass capacitor C3 returns the series-fed primary winding, L1, to r-f ground potential, and the r-f choke (RFC) prevents any radio-frequency currents from entering the plate-voltage source,  $E_{bb}$ .

Capacitors C5 and C6 are the charging capacitors of the voltage-doubler circuit. Since the frequency of the applied voltage is between 40 and 600 kilohertz, and the load current is a low value, the value of these capacitors is relatively small, generally about 1000  $\mu\mu f$ . Furthermore, because the ripple-frequency component is also in the radio-frequency range, there is little need for large-value filter components. **Resistors** R3, R4, and R5 in series form a bleeder and voltage-divider resistance for the output of the doubler circuit.

As previously mentioned, primary winding L1 is tuned to resonance by capacitor C4. The resonant frequency of the high-voltage winding, L5, is determined primarily by the shunting capacitances of rectifier V3 and capacitor C6 in series, as well as stray circuit capacitance resulting from wiring and the physical placement of other circuit components. The r-f oscillator power supply is normally designed so that the maximum output voltage obtainable is greater than the output voltage required to be delivered to the load. Maximum output voltage is developed when the oscillator frequency is equal to the natural resonant frequency of L5 is parallel with its shunting capacitance; therefore, the desired value of output voltage is obtained by adjusting tuning capacitor C4 to set the oscillator frequency near the natural

resonant frequency of L5 and its shunting capacitance. The voltage produced across winding L5 is applied to the voltage-doubler circuit, and since the dc output voltage contains a ripple-frequency component which is twice the frequency of the applied ac voltage, the output requires very little filtering.

The use of grid-leak bias (RIC1) tends to make the oscillator self-regulating with respect to its power output, because the oscillator operates as a Class C stage, the efficiency is fairly high. The regulation of the supply is considered adequate for most cathode-raytube circuit applications where the load current is always constant; however, any change in the voltages applied to the oscillator circuit, a change in the oscillator frequency, or a change in the load current will affect the output voltage and thus cause poor regulation. Therefore, if good regulation is required, a voltage regulator circuit must be added. Another disadvantage of the r-f oscillator power supply is that it must be well shielded to prevent the oscillator fundamental frequency or its harmonics from being radiated as an undesired signal, causing interference within the associated equipment or perhaps affecting nearby electronic equipments.

#### **Failure Analysis**

**Genaral.** The r-f oscillator type high-voltage supply consists of two basic circuits-an oscillator and a rectifier. It must be determined initially whether the oscillator or the rectifier portion of the power-supply circuit is at fault. Tests must be made to determine whether the oscillator is performing satisfactorily; if it is, the trouble is then assumed to be located within the associated rectifier circuit or its load circuit. The failure analysis outlined in the following paragraphs is somewhat brief because the subject of electron-tube oscillators is discussed in another section of this handbook; furthermore, the particular high-voltagerectifier circuit may be the same as one of the rectifier circuits described earlier in this section. Since the r-f oscillator high-voltage supply is a combination of two basic circuits, information concerning failure analysis for either portion of the high-voltage supply can be obtained by reference to the applicable basic circuit given elsewhere in this handbook.

No **Output.** When the oscillator is in a nonoscillating condition, negative grid voltage will not be developed across RIC1, and the measured plate and screen voltages of oscillator tube VI will be below normal. The applied filament, plate, and screen volt-

ages should be measured to determine whether these voltages are present and are of the correct value. The oscillator tube VI should be tested to determine if it is defective.

Excessive losses in the air-core transformer, T1, or shorted capacitor Cl, C2, C3, or C4 will prevent the oscillator from operating. Also, defective components in the rectifier circuit associated with the high-voltage winding, L5; may introduce losses into the oscillator circuit which will prevent oscillator operation. With all voltages removed from the circuit, disconnect one lead from winding L5, or remove rectifiers V2 and V3 from their sockets; then reapply the voltages and again perform tests on the oscillator to determine whether the oscillator will operate under no-load conditions.

If the oscillator circuit is found to be functioning normally, it must be assumed that the trouble is associated with the rectifier circuit or its load, and a check of the rectifier circuit must be made in accordance with the procedures outlined in this section for the applicable rectifier circuit.

Low Output. A relative indication of oscillator output can be obtained by measuring the amount of bias voltage developed across RIC1. A value of bias which is below normal is an indication of low oscillator output. Also, if the applied plate and screen voltages are below normal, a reduction in output will occur. A leaky screen bypass capacitor, C2, will form a voltage divider with screen dropping resistor R2 and result in a decreased screen voltage; thus, the output of the supply will be low. Oscillator tube V1 should be checked to determine if it is the cause of the low output. Where the oscillator circuit employs two tubes in parallel, one or both tubes maybe suspected as causing low output.

It is possible that the low output condition may be caused by a change in oscillator frequency away from the resonant frequency of the high-voltage winding L5. (A change in the oscillator frequency toward the resonant frequency of L5 will ordinarily cause a higher than normal output.) An adjustment of tuning capacitor C4 can be made in this case in an attempt to obtain the normal output voltage.

If the oscillator is found to be operating normally, a defect within the rectifier circuit or the associated load must be suspected as the cause of low output. For example, because of the relatively highimpedance rectifier and filter circuits and the generally poor regulation characteristics of this type of

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supply, an excessive load current can cause the output voltage to be low. Failure analysis procedures for typical rectifier circuits used in high-voltage supplies are outlined earlier in this section.

# **DOSIMETER** CHARGER (DC-TO-DC CONVERTER) (SEMICONDUCTOR)

### Application.

The dosimeter charger is one typical application of the de-to-de converter circuit. The dosimeter charger is a self- contained, portable, battery-operated, transistorized power supply which is used to generate a dc output (charging) voltage at a small load current. The circuit can be arranged to furnish either a negative or a positive **high-voltage** out-put. The dosimeter charger is commonly used to provide a high-voltage charge for radiation detectors employed for personnel monitoring. The dc output voltage developed by the charger is transmitted, through an appropriate connection or receptacle, to the dosimeter being charged.

## Characteristics.

Uses single transistor self-excited oscillator circuit combined with a half-wave rectifier circuit.

Typical operating frequency is between 400 and 2000 Hz.

Output is high-voltage dc at low current.

Regulation is poor; however, for the application the regulation is not important.

Rectifier circuit can be arranged to provide either positive- or negative-polarity output voltage; rectifier is semiconductor diode.

# Circuit Analysis.

**General.** The dosimeter charger consists of a tickler-coil (Armstrong) audio-frequency oscillator operating in conjunction with a rectifier to convert a low dc voltage to a high dc voltage. The oscillator described here operates in the range between 400 and 2000 Hz as a sine-wave generator, although with slight modification the circuit can operate as a blocking oscillator to produce a square-wave. The high-voltage ac output from the oscillator is rectified to provide a dc output voltage which is then filtered to remove ripple, and applied to the electroscope assembly of the dosimeter (or radiacmeter).

A brief description of a small, direct-reading pocket dosirneter, used to measure X and gamma radiation, is in order at this time so that the application of the charger maybe better understood.

The pocket dosimeter is one of several radiation monitoring instruments utilizing the ability to radiation to produce ionization in gases. The dosimeter is approximately the size of a fountain pen, and consists of a hermetically sealed metal tube, or barrel, with an inner ionization chamber electrically connected to the metal tube. An electroscope assembly, consisting of a stiff support wire mounted in a clear plastic insulator and a freely moving quartz fiber supported by the wire, is mounted within the ionization chamber. The support wire is connected to a charging contract which is insulated from, and mounted in, the sealed end of the metal tube. A sealed optical system, consisting of an eyepiece lens, a calibrated scale, and an objective lens, is mounted axially in the other end of the metal tube.

Before the dosimeter can be used to detect radiation, it must be charged. This is accomplished by applying a dc voltage between the metal tube and the charging contact located on the end of the tube. The charging voltage causes a mutual repulsion between the support wire and the quartz fiber, and a mutual attraction between the ionization chamber wall (tube) and the quartz fiber. As a result, the quartz fiber is deflected away from the support wire toward the chamber wall. The amount of deflection is a direct function of the charging voltage; the greater the voltage, the greater the deflection. The dosimeter is charged prior to use by looking into the eyepiece and adjusting the voltage output of the charger until the quartz fiber indicates "O" on the internal calibrated scale of the optical system.

As radiation passes through the dosimeter, the gas within the chamber ionizes. The ionized gas is capable of electrical conduction, and thus partially neutralizes the charge existing on the quartz fiber. As a result, the fiber moves toward the support wire a distance equivalent to the amount of radiation received. The amount of total radiation exposure can be read directly from the calibrated scale by viewing it through the eyepiece.

**Circuit Operation-** The accompanying circuit schematic illustrates a self-excited, tickler-coil (**Arm**strong) audio-frequency oscillator used in conjunction with a half-wave rectifier circuit. The discussion which follows is limited to a brief discussion of the oscillator circuit, since the operation of the Single Phase Half-Wave Rectifier Circuit using a semiconductor diode has been described earlier in this section of the handbook.



#### **Typical Dosimeter Charger Circuit**

Transistor Q1 is a PNP transistor, either a pointcontract or a diffused-junction type, used in a common-emitter circuit configuration. Since the power output required of the charger is extremely small, the transistor need not be a power transistor as was the case in other DC-to-DC Converter Circuits described previously in this section. Rectifier CR1 is a semiconductor diode used in a conventional half-wave rectifier circuit. Because the dc output voltage is usually limited to approximately **400 volts**, dc, a single rectifier having the necessary peak-inverse voltage characteristics is normally employed.

Transformer 11 provides the necessary regenerative feedback coupling from the collector to the base of the transistor, and is also the source of high voltage for the half-wave rectifier circuit. Transformer winding L1 is the collector winding, winding L2 is the feedback (tickler coil), or base, winding, and winding L3 is the high-voltage secondary (step-up) winding. In the schematic, the dots adjacent to the transformer windings are used to indicate similar winding polarities.

Potentiometer RI is used as a voltage divider to provide forward bias for the base of the transistor.

Once R1 has been set to establish forward bias for proper operation of the transistor, it normally does not require further readjustment unless the transistor is replaced or a change is transistor characteristics occurs.

Capacitor Cl is an audio bypass capacitor provided to return the end of feedback winding L2 to the emitter of transistor Q1. Capacitor C2 is the filter capacitor of the half-wave rectifier circuit. Since the frequency of the oscillator is relatively high (400 to 2000 Hz), the value of capacitor C2 need not be very large (usually 0.01 to 0.02  $\mu$ f) in order to effectively remove any trace of ripple voltage; furthermore, since the load is an extremely high impedance and the load current is small, the capacitor charges to the peak value of the applied ac.

Potentiometer R2 and resistor R3 form a voltage divider across the output of the rectifier circuit. The value of R2 is usually several times greater than the value of R3, and the total series resistance is usually 15 to 20 megohms; thus, the voltage available at the output terminals of the supply can be varied between approximately 125 and 425 volts, dc. Potentiometer R2 is controlled by a front panel knob, and permits the dc output voltage of the charger, which is applied to the dosimeter electroscope assembly, to be adjusted and thus calibrate the instrument prior to use.

The common-emitter configuration illustrated earlier in this discussion utilizes a single-battery power source; as mentioned previously, this dc source produces the required base-bias voltage through the voltage-divider action of potentiometer R1. Since the collector of Q1 is at a negative potential and the emitter is at a positive potential, the base is effectively placed at a negative potential with respect to its emitter; thus, forward bias is established for the PNP transistor.

The oscillator circuit can be compared to an amplifier with feedback of the proper phase and amplitude. The oscillator may be operated Class A if a linear waveform is required, or Class C if the output waveform is not very important. In the PNP transistor schematic given earlier, feedback is obtained by transformer coupling from the collector to the base in order to sustain oscillations. If an NPN transistor is used in the circuit, the polarity of the supply voltage must be opposite to that shown on the schematic; however, for either type of transistor, the feedback signal must be 180 degrees out of phase with the collector signal. Although the transistor can also be

arranged in a common-base or a common-collector circuit, the common-emitter circuit is most commonly used because greatest gain is achieved with this configuration. The oscillator circuit shown in the schematic is essentially a transformer-coupled, feedback oscillator; its operation is similar to that of the common-emitter circuit described for the Tickler Coil (Armstrong) Oscillator Circuit in the Oscillator Section of this handbook. Although the circuits described are L-C oscillators, the operation of the audio-frequency oscillator discussed here is essentially the same; the frequency of oscillation is determined primarily by the inductance of collector winding Ll, stray circuit capacitance, and the collector-to-emitter capacitance of the transistor itself. When voltage is first applied to the oscillator, the initial rush of current through L1 and L2 induces a feedback voltage in the windings. The feedback is regenerative and causes emitter and collector current to increase rapidly until the collector is saturated and no further change of current occurs. At this time the magnetic field around the windings of T1 collapses, and causes a reversed feedback voltage. This feedback is now in a direction which causes a reduction of collector and emitter current. Thus the collector is quickly driven to cutoff, and once again the collapsing magnetic field (at cutoff) causes a reversal of current flow through the induced feedback voltage. As the current through L1 alternately flows back and forth at the oscillation period, it induces a similar but higher alternating voltage in winding L3, the high-voltage winding.

The voltage produced across the high-voltage secondary winding, L3, may be either a sine wave or essentially a square wave, depending upon the class of transistor operation. This voltage is rectified by semiconductor diode CR1, is filtered by capacitor C2, and is applied across R2 and R3. A dc output voltage which is determined by the setting of potentiometer R2 is applied to the dosimeter charging contact for calibration of the radiation monitoring instrument.

#### Failure Analysis.

**General. The** dosimeter charger is self-contained, battery-operated power supply. The unit is usually very small and operates from a self-contained, 1.5 volt-battery power source. It must be determined initially whether the battery, the oscillator, or the rectifier portion of the power supply is at fault. Since the most common failure for a battery-powered device is the battery itself, a quick check can be made by substituting a known good battery in the power supply and checking the operation once again to determine whether the battery is at fault. If the operation is not satisfactory after battery substitution, tests must then be made to determine whether the oscillator or the rectifier circuit is at fault.

As stated before, the dosimeter charger is a combination of two basic circuits, an oscillator and a half-wave rectifier using a semiconductor diode. Therefore, the failure analysis outined in the following paragraphs is somewhat brief since oscillators are completely discussed in the Oscillator Section of this handbook, and the Half-Wave Semiconductor Diode Rectifier is discussed earlier in this section of the handbook.

No **Output. The battery** power source (VCC) should be measured to determine whether it is present and of the correct value.

The oscillator can be quickly checked to determine whether or not it is oscillating by using an oscilloscope to observe the **collector-to-emitter** waveform.

If potentiometer R1 should change value (or is misadjusted), the forward bias will change accordingly. If the forward bias decreases the collector current also decreases, and, conversely, if the forward bias increases the collector current increases. At either extreme of these two conditions, oscillations will cease.

Any defect in transfornwr Tl, such as on open feedback or collector winding, or shorted turns in any of the windings, will prevent the circuit from oscillating. A shorted secondary circuit, reflected to the collector and feedback windings, will cause excessive losses in the circuit and prevent sustained oscillations. If the high-voltage winding, L3, should open, the circuit will oscillate; however, no output will be obtained from winding L3 for the rectifier circuit.

A shorted junction or an open junction in the transistor, Q1, will cause the circuit to stop oscillating.

If the oscillator circuit is found to be functioning normally, then it must be assumed that the trouble is in the associated rectifier circuit.

Low Output. The battery power source (VCC) should be measured to determine whether it is present and of the correct value.

In the common-emitter configuration, a relatively small change in base current produces a relatively large change in collector current. Therefore, the value of the forward-bias voltage applied to the base of the )

transistor is rather critical, since the bias voltage has a direct effect upon collector current and thus upon the oscillator power output. While reduced output can result from a loss of gain in the transistor, this condition is not very common; therefore, it is more logical to measure the supply and bias voltages before deciding to replace the transistor.

A change in the resistance ratio of potentiometer RI, an open or short in a portion of potentiometer RI, or leakage in bypass capacitor Cl will affect the output, since any of these conditions 'will cause a change in bias; however, a change in bias is easily detected by measuring the operating bias with a high-resistance voltmeter, or preferably an electronic voltmeter. For example, if the positive end of R1 should open, the base of QI is returned to -Vcc through the remaining portion of RI; in this case, since the base remains in a forward-bias condition, the circuit will continue to oscillate. However, the oscillator output will no longer remain a sine wave, and the oscillator may start to puke in a manner similar to that of a blocking oscillator. On the other hand, if the negative

end of RI should open, the base of Q1 is returned to +Vcc, and oscillations will cease. Either of these two conditions can be detected by a measurement of the bias voltage.

If resistance measurements are to be made on potentiometer RI, at least two of the terminals should be disconnected from the circuit, or the transistor removed from the circuit, in order to obtain valid resistance measurements (that is, measurements that are unaffected by the junctions of the transistor).

If the oscillator circuit is found to be operating normally, a defect within the rectifier circuit must be suspected as the cause of low output. Since the rectifier circuit is a high-impedance circuit, an excessive load current **caused** by a decrease in the value of R2 or R3, or by a leaky bypass cpacitor (C2), can result in reduced output. Also, a defective semiconductor diode **(CR1)** can cause decreased output. Failure analysis procedures for the Half-Wave Semiconductor Diode Circuit are given earlier in this section of the handbook.

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# PART 2-5. SILICON-CONTROLLED RECTIFIERS

# SINGLE-PHASE FULL-WAVE SCR

### Application.

The single-phase full-wave silicon-controlled rectifier is usually used where a high dc current output is required from the power supply. It is used as a power supply in electronic equipments such as transmitters and computers, or industrially in battery charges, in welders, and as a control device.

#### Characteristics.

Input is alternating current and output is pulsating direct current.

Uses a center-tapped transformer.

DC output ripple frequency is twice the primary line voltage frequency.

Uses two silicon-controlled rectifiers.

May be connected to supply either positive or negative output voltage.

#### Circuit Analysis.

**General.** Except that it is controlled by a gate, the silicon-controlled rectifier operates in a manner similar to the conventional semiconductor diode rectifier. For full-wave operation two diodes are required; one for each half of the cycle.

In the ordinary diode, conduction occurs in a forward direction as soon as the anode becomes more positive than the cathode. In the silicon-controlled diode, conduction does not occur until the unit is turned on by a positive current gate (or until the forward breakdown voltage is exceeded). Once triggered, conduction continues for the remainder of the ac half-cycle until the reducing forward voltage causes the forward current to fall below the holding current value, whereupon conduction ceases. At the same time, the polarity of the ac input changes, and a reverse voltage is applied to the diode. During the second half-cycle, the other controlled rectifier diode is gated and conducts in a similar manner. By controlling the gate tiring time, the output voltage and current may be controlled over any desired portion of the operating cycle.

**Circuit Operation.** The schematic of a typical fullwave controlled rectifier circuit is shown in the accompanying illustration.





Transformer T1 is the supply voltage transformer with a center-tapped secondary. The secondary voltage may be any value within the rating of the controlled rectifier diodes. Diodes CR1 and CR2 are similar types of silicon-controlled rectifiers. The gate firing network for CR1 consists of current-limiting resistors R1 and R2, with semiconductor diode CR3. The gating network for CR2 consists of currentlimiting resistors R3 and R4 with semiconductor diode CR4.

When primary voltage is applied to T1, one end of the secondary becomes positive with respect to the center tap, while the other end is negative with respect to the center tap.

Assume that the anode of CR1 is driven positive while the anode of CR2 is driven negative. Since a negative voltage is applied to CR2, only reverse leakage current flows through the diode. Meanwhile, since CR1 is not triggered and the forward voltage is below the firing level, CR1 will not conduct. As the positive half-cycle increases from zero toward maximum, a positive voltage is also applied to gate-control diode CR3 which conducts and produces a positive voltage drop across R2. The positive voltage applied to the gate electrode of CR1 forward-biases CR1 and permits a flow of electron current from cathode to anode of the silicon-controlled rectifier. The current flow path is from the center tap of T1 through load  $R_L$ , and through diode CR1 to the top of the secondary winding. Conduction through CR1 continues until the secondary voltage drops to zero, and reverses during the next half-cycle. At the same time, the anode of gate-control diode CR3 is also driven negative and does not conduct. Hence, with no gate voltage, and a negative anode voltage, CR1 ceases conduction for the negative half-cycle.

The anode of controlled rectifier CR2 is now driven positive, but CR2 remains blocked until gated. The positive half- cycle also drives the anode of gatecontrol diode CR4 positive, and current flow through resistor R4 eventually provides a positive gating voltage. When CR2 is gated, electrons flow from cathode to anode until the next half-cycle occurs, and the polarity is reversed. Current flow is from the center tap of T1 through load resistor  $R_{I}$  and controlled rectifier CR2 to the bottom of the secondary winding. Since current flows through the load in the same direction when either rectifier is conducting, a positive dc voitage is obtained at the output of the power supply. Thus, for each half cycle of ac, a positive output pulse is produced, creating a ripple frequency of twice the input frequency. This ripple component is eliminated by using a low-pass filter, as required.

The use of a simple resistor-diode type of gating is shown and described for simplicity and ease of discussion. Usually a more complicated firing circuit is used, and the output is controlled over the entire halfcycle of operation, as desired. With the resistor-diode control circuit, control is limited to a maximum of 90 electrical degrees of the half-cycle of operation, as determined by the values of resistors RI, R2, R3, and R4. Increasing the resistance value delays the firing time, while decreasing the resistance value lengthens the firing time. Delaying the firing time also changes the pulse shape from a sinusoidal waveform toward a square waveform, since the leading edge is straightened. Hence, in control circuits which tire only over a small portion of the ac half cycle, an almost pure square-wave output voltage is produced. Thus, the silicon-controlled rectifier tends to be more difficult to filter than the conventional semiconductor or electron tube power supply, since it contains more harmonic output.

For high currents at standard line voltages, the center-tapped transformer may be dispensed with, and the controlled rectifiers are connected across the line in series with the load. In addition, surge voltage suppressors and transient elimination circuits are required to stabilize the line voltage. Since circuits of this type are usually used on industrial equipment such as spot welders, they are beyond the scope of this handbook; the interested reader is referred to standard commercial design data and manufacturers' handbooks.

#### Failure Analysis.

**No Output.** Lack of output may be caused by loss of line voltage, a defective supply transformer, a defective controlled rectifier, or a defective gate control circuit. Check the line voltage with a voltmeter to determine that primary voltage is available and that a defective supply or blown power fuse is not at fault.

With the proper primary voltage available, check the secondary voltage with an ac voltmeter to determine that T1 is not defective. If voltage exists across the primary of T1 but does not appear across the secondary, remove the power and check both primary and secondary windings with an ohmmeter for continuity. Lack of continuity indicates an open winding. A shorted winding will usually blow the primary fuse or open the circuit breaker. Use an oscilloscope to check the gating waveform and amplitude. Presence of the proper firing pulse and no output usually indicates that the controlled rectifier diode is defective.

If the gating waveform is incorrect, or does not appear, check the firing circuit (Rl, R2, R3 and R4) with an ohmmeter. Check the forward and reverse resistance of CR3 and CR4. Normally, the reverse resistance should be high and the forward resistance low. If a **low** reading is obtained in both directions, the diode is shorted; if a high resistance is obtained in both directions, the diode is open. If the components are checked and found to be normai, but there is still no output, check the output resistance and load. Where a ripple filter is used, it is possible for the input capacitor to be shorted. Usually such a condition will create a load sufficient to blow the fuse or open the primary circuit breaker.

Low Output. Low line voltage, a defective controlled rectifier, or a defective firing circuit can cause a low output. Use an accurate ac voltmeter to measure the line voltage. To determine if the controlled rectifier is defective, use an SCR tester. It is also possible to have only one controlled rectifier operative, so that instead of functioning as a full-wave rectifier, it

operates only as a half-wave rectifier. Hence, it is necessary to make similar measurements on both sides of the circuit., Equal secondary voltages must exist between the center tap and each side of the secondary of T1 to ensure that equal outputs are obtained at the cathode. Likewise, both firing gates must be **equal** in waveshape and amplitude to fire over the same range. If one diode fires sooner or later than the other, so that conduction occurs for different periods of time, a lower than normal output can be obtained.

When checking the firing circuits, the values of RI and R3 should perferably be the same; differences in the resistance values of these resistors have a greater effect on the firing time than do the differences between R2 and R4. For best results, gating diodes CR3 and CR4 should be matched also. Where a large value of input capacitance is used on the ripple filter following the rectifier, a greater mismatch between firing components can be allowed, since the long charge and discharge time constant of the filter averages out the changes between half-cycles of operation.

**Erratic Firing.** In the simple resistance-diode firing circuit described in this full-wave rectifier circuit, the trigger pulse is obtained from line voltage. Therefore, it is possible for line transients of sufficient amplitude to cause false triggering. These transients can be observed on an oscilloscope connected across the line. It may be necessary to employ surge suppressors or a line regulator to prevent such erratic operation. When encountering trouble of this sort, it is important not to neglect the location and dressing of input and output cabling, particularly where the transients are being induced by unnecessary inductive coupling between the rectifier and the line or device causing the trouble.

## THREE-PHASE FULL-WAVE SCR

## Application.

The three-phase full-wave silicon-controlled rectifier is generally used in high voltage and high current three-phase power supplies for electronic and industrial equipments.

#### Characteristics.

Input to circuit is three-phase ac; output is dc with amplitude of ripple voltage less than that for a singlephase rectifier.

Uses six controlled rectifiers.

Output requires very little filtering; dc output ripple frequency is equired to six times the primary linevoltage frequency.

Circuit has good regulation characteristics.

Can be connected for either positive or negative output voltage.

Uses multi-phase transformer with wye-connected secondary. Primary may be comected either delta or wye.

#### **Circuit** Analysis.

**General.** The three-phase silicon< ontrolled fullwave rectifier is similar in operation to the conventional semiconductor rectifier, except for its gating circuitry. Usually the primary is connected in delta and the secondary in wye to obtain a step-up of voltage. A delta-to-delta connection will produce a lower output voltage in comparison with the delta-to-wye connection. Usually the gating circuit is of the variable-phase control type, allowing full control over each phase to provide a uniforfn balance, maximum voltage, and better efficiency.

**Circuit Operation.** A typical three-phase, full-wave silicon-controlled rectifier schematic is shown in the accompanying illustration. The gate tiring control circuitry is not shown since there is no single basic firing circuit, but each manufacturer has his own proprietary claims for his own devices. In the discussion of circuit operation, an adequate firing pulse will be presumed to occur at the desired instant and of sufficient amplitude, duration, polarity, and value to produce forward conduction in the controlled rectifier.



**Three-Phase Full-Wave Controlled Rectifier** 

In the schematic, T1 is a three-phase transformer with the primary delta connected and the secondary wye connected. Silicon-controlled rectifiers CRI, CR2, and CR3 operate on one-half of the ac cycle, while CR4, CR5, and CR6 operate on the other halfcycle since they are connected in reverse (these connections are similar to those used for electron tube and conventional semiconductor diodes also).

The secondary voltages between terminals A, B, and C ( $e_{sec}$  1, es. 2 and  $e_{sec}$  3, respectively) are 120 electrical degrees out of phase, producing three separate single-phase ac voltages over a complete 360degree cycle. Thus, a positive or a negative peak of voltage occurs every 60 electrical degrees. With three rectifiers connected to operate on each half-cycle, six conduction periods occur during one 360-degree period of operation. The individual circuits are shown for each conduction period in the accompanying illustration. The arrows show the direction of electron flow through the circuit. Since the path through the load is always in the same direction, a dc output voltage and current are produced. Since the output ripple frequency is six times that of the line frequency, the output is much easier to filter than the conventional single-phase supply.

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**Rectifier Circuits and Waveforms** 

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When voltage is applied, the diodes do not conduct since they are not gated and the normal forward voltage is insufficient to cause them to fire. At time to, assume that phase A (terminal A on the secondary) is at zero and voltage  $e_{sec 1}$  is increasing in a positive direction. At this time, phase B (terminal B) is negative 60 degrees and increasing toward its maximum negative potential at -90 degrees. Phase C has reached and passed its maximum positive peak and is becoming less positive (approaching zero) during its final 60 degrees of positive half-cycle. Since half of the rectifiers conduct during the positive hrdf-cycle, and half during the negative half-cycle of operation, there are rdways two rectifiers conducting. Thus, over a 360-degree period of operation, each rectifier conducts for 120 degrees and is off for 60 degrees. If we assume that the controlled rectifier gate is arranged to trigger each rectifier when the voltage reaches 60 degrees amplitude (positive or negative), then the rectifier will continue to conduct for 120 degrees until the applied voltage reaches zero at the 180-degree point where the polarity reverses during the following half-cycle. The accompanying waveform illustration shows the ac secondary voltage relationships.

Starting at to, voltage CB reaches its 60-degree positive position while voltage BC reaches its 60degree negative position. Controlled rectifiers CR2 f and CR5 are gated and forward conduction occurs in each. During period CB, electron flow is from terminal B through CR5, through the load, and CR2, back to terminal C. During the interval of voltage from C to B, terminal C voltage is falling toward zero while terminal B is increasing negatively. Meanwhile, the voltage at terminal A is increasing from zero in a positive direction. When voltage A reaches the 60degree point, CR1 is gated by a positive firing pulse and CR1 conducts. Simultaneously, terminal C voltage reaches zero and CR2 ceases conduction. Since CR5 is still negatively biased and conducting, the cur-

rent path for period AB is from terminal B through CR5, through the load, and CR1, to terminal A. Thus the same current direction is maintained and the output voltage remains positive. During the period AB, terminal B voltage declines from a maximum negative value to zero, turning off CR5 when terminal B becomes zero, and starts increasing in a positive direction. Simultaneously, the voltage at terminal C is increasing negatively from zero and reaches the 60-degree firing point as CR5 turns off, and transfers conduction to CR4. Thus, during the period AC, elec-

tron flow is from terminal C, through CR4, through the load and CR1, back to terminal A. At the end of period AC, the positive voltage on terminal A has reduced to zero, turning off CR1. Meanwhile, terminal B voltage is increasing in a positive direction, and reaches the firing point 60 degrees later when period AC ends and BC begins, and turns on CR3. Conduction now occurs from terminal C through CR4, the load and CR3 to terminal B. Since the current flow is stiU in the same direction through the load, the output voltage is still positive.

During the period BC, terminal A voltage increases from zero toward a maximum negative value, and at the end of period BC reaches the firing value for CR6. Meanwhile, voltage C has reached zero and turns off CR4 as CR6 is turned on. During period BC, voltage BA is increasing from zero toward a positive maximum, so that CR3 still conducts for the period BA. Meanwhile, the voltage at terminal C increases from zero in a positive direction, and at the end of period BA tires CR2. The conduction path for period CA is now from A, through CR6 and the load, and through CR2 back to C.

At the end of period CA, voltage A has declined from a maximum negative value to zero and turns off CR6. Meanwhile, voltage B has increased negatively to the firing point and turned on CR5. Thus, conduction continues for period CB from terminal B through CR5, the load and CR2 to terminal C. The sequence of **on-and-off** gating just described for the 360-degree period of operation now continues in the same manner, producing a continuous dc output voltage.

Although the firing time has arbitrarily been chosen at the 60-degree point for ease of discussion, it is usually possible to control operation over any desired portion of the cycle. In those cases where it is desired to turn off the rectifier before the end of the half cycle, it is necessary to include in the control circuit some form of turn-off voltage.

# Failure Analysis.

**No Output.** A no-output condition can be caused by lack of supply voltage, or a blown line fuse, by a defective firing circuit, or by a defective controlled rectifier. Use a voltmeter to determine if line voltage is present. If line voltage is not present, check for a blown line fuse or a defective transformer. If line voltage is present in the primary but no secondary voltage exists, remove the power and check the secondary windings for continuity. Since there are three

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separate windings involved in three-phase circuits, each must be checked individually. Usually only one phase opens at a time, so that no-output conditions are usually caused by short circuits across the output, which are usually indicated by continuous blowing of fuses. The more probable event is a defective firing circuit which prevents any of the rectifiers from operating. Use an oscilloscope to observe the ftig waveform and amplitude. If firing waveforms are present and no output is obtained, the rectifier is defective.

Low Output. Low output voltage can be caused by low line voltage, improper transformer comections, or a defective transformer or controlled rectifier. Check the line voltage with a voltmeter, and in addition check for poor or loose primary comections. Check the transformer comections to make certain that the secondary is wye-connected, since a delta connection will automatically produce a lower output voltage. Check the transformer for equal voltages across each winding. If unequal voltages are measured, remove the power and check the resistance between each terminal and ground, since a partially shorted or grounded secondary can exist. If equal secondary resistances exist with equrd primary and secondary voltages, but the output voltages are different, the low reading controlled rectifier is probably defective.

A firing circuit adjusted for short conduction periods, or with defective components which can cause a shorter than normal conduction period, will also provide a low output. If a slight readjustment of the firing circuit control will return the output voltage to normal, the trouble is probably a change in component values in the firing circuit. Voltage and resistance checks of the ftig circuit will usually determine the part at fault. Increased resistance in the circuit usually causes delayed ftig, while decreased **resistance** values lengthen the firing time. Where an output filter is used, it is possible for a faulty falter to produce a lower than normal voltage.

#### **BRIDGE-CONNECTED SCR**

# Application.

**The** bridge-connected SCR is used to supply high voltage at relatively high current in electronic and industrial equipments. Low-voltage applications are also possible.

## characteristics.

Does not require a center-tapped transformer; full potential of winding is available.

Ordy requires two controlled rectifiers and two semiconductor diodes.

Input circuit is ac, output is pulsating dc.

Polarity of output may be either positive or negative, as desired.

Output frequency is twice the input frequency and requires ripple faltering.

#### Circuit Analysis.

General. The bridge rectifier uses a minimum of two controlled rectifiers firing on each half-cycle of input voltage, in conjunction with two semiconductor diodes, to provide a full-wave rectifier circuit. Since one diode and one controlled rectifier are always connected across the line in series with the load, gating the controlled rectifier also controls diode operation. Since the full secondary winding of the high voltage transformer is used, twice the voltage of a centertapped secondary is available. For special applications, it is also possible to use four controlled rectifiers in the bridge by substituting controlled rectifiers for the two diodes. The increased complexity of the tiring circuit, plus the cost of the extra controlled rectifiers, makes the two controlled rectifier bridges a more preferred circuit for general use.

**Circuit Operation.** The accompanying schematic illustrates a typical controlled rectifier bridge using two controlled rectifiers and two semiconductor diodes.



**Controlled Bridge Rectifier** 

As shown in the schematic, firing of the controlled **rectifiers** is accomplished by a resistance-diode network. Transformer T1 supplies the secondary voltage across which the bridge, consisting of diode CR5 and controlled rectifier CR2 on one arm, and diode CR6 and controlled rectifier CR4 on the other arm, are connected. Resistors R1 and R2 are current-limiting firing resistors, and diodes CR1 and CR3 are gating diodes. Diode CR1 controls the firing of controlled rectifier CR4.

At the instant when power is first applied, both controlled rectifiers are in a nonconducting condition, since they are not gated and the forward voltage is not sufficient to cause self-firing. Assume for the moment that the top of the secondary winding of T1 is positive, while the bottom of the winding is negative. For this half-cycle the cathode of diode CR6 is biased negatively, permitting a forward flow of current. However, with controlled rectifier CR2 blocked open, the current path across the secondary is open, and current will not flow until CR2 is gated. Since the top of the secondary is positive, a positive potential is placed on the anode of control diode CRI, forward biasing the diode. Thus, as the secondary voltage of T1 increases, the positive gate voltage on CR2 also increases. When the gate voltage reaches an amplitude which causes sufficient gate current to flow, CR2 becomes forward-biased, closing the circuit path across the secondary. Current now flows from the bottom of the secondary through diode CR6, through load  $\mathbf{R}_{\mathbf{I}}$  and controlled rectifier CR2 to the top of the secondary, and a positive output voltage is produced. Conduction now occurs for the remainder of the positive half-cycle, and ceases as the anode voltage drops to zero and is unable to sustain sufficient holding current through CR2. At this time, the secondary voltage also reverses polarity, reversebiasing control diode CR1 and controlled rectifier CR2, and forward-biasing diode CR5. When the top of the secondary of T1 is made negative, the bottom of the secondary becomes positive, and a positive gate voltage is applied to the anode of gating diode CR3 through R2. Although 'the mode of controlled rectifier CR4 is also made positive, the forward voltage is insufficient to cause firing. No current flows through the circuit until the positive gate voltage increases to the firing level and produces forward conduction in CR4. When CR4 conducts, current flows from the top of the secondary winding through diode CR5, the load, and controlled rectifier CR4, back to the bottom of the secondary, and a dc output voltage is produced across the load.

Since the current flows through the load in the same direction for both half-cycles of operation, the current flows continuously in one direction and the ac input is changed to a dc output. Controlled rectifier CR4 continues to conduct until the anode voltage drops to zero at the end of the half-cycle and reverses polarity. Once again, the top of the secondary winding becomes positive and eventually CR2 is gated, and the cycle repeats. Since conduction in the rectifiers does not occur until they are gated and varies with the applied voltage amplitude, the output voltage is pulsating direct current with a ripple frequency twice that of the input. Therefore, an output falter is required for those applications requiring pure direct current. Filter circuits are discusses in the Filter Section of this handbook.

When the two controlled rectifier bridge circuit is used, it is necessary that the associated diodes are capable of handling the same current and voltage as the controlled rectifiers. The gating diodes, however,

need only be rated sufficiently to carry the gating current and voltage. The time of firing is mainly controlled by the vahres of firing resistors RI and R2.

## Failure Analysis.

No Output. Loss of line voltage or a defective transformer are the most likely causes for a no-output condition. While it is also possible that a defective firing circuit or faulty rectifiers can also cause lack of output, it is necessary that both rectifiers, both diodes, or both firing circuits be simultaneously defective to cause a complete loss of output. Failure of one half of the circuit will cause a low output, rather than none at all. Check the primary line voltage with an ac voltmeter; if no voltage is present, a fuse or circuit breaker is most likely at fault. If primary voltage exista, check the secondary voltage. If no secondary voltage exists, check transformer T1 for continuity with an ohmmeter. Usually a shortcircuited secondary will continue to blow the primary firse. If secondary voltage is present but there is still no output voltage, check each firing circuit with an oscilloscope to see if a firing waveform exists. Check the value of RI and R2 with an ohmmeter, and check the forward and reverse resistance of gating diodes CR1 and CR3. If the gating diodes are defective they will indicate the same resistance in both directions. Also check diodes CR5 and CR6. If a firing gate is present on CR2 and CR4, and diodes CR5 and CR6 are satisfactory, controlled rectifiers CR2 and CR4 are probably defective. Where a falter is used at the output, it is possible for the falter to be shorted, but usually such a condition results in continuous blowing of the primary or line fuse.

Low Output. Low output voltage can be caused by low line voltage, a defective transformer, a faulty circuit, or a faulty rectifier. Check the primary and secondary voltages with a voltmeter to make certain they are normal. Use an oscilloscope to check that both firing circuits operate. Check the value of both RI and R2 with an ohmmeter. A reduced firing time, caused by either **R1** or R2 increasing in vahre, can produce a lower output than normal. A similar condition could also be caused by either CR1 or CR3 being defective.

# SCR INVERTER (DC to AC)

# Application.

The SCR inverter is used to change a dc input voltage to an ac output voltage for power-supply use aboard ship, small craft, aircraft, and mobile equipment, which primarily have only a source of direct current available.

#### Characteristics.

Input to inverter is dc, output is ac.

Oscillator frequency determines output frequency. Two SCR'S are used (one for each half-cycle).

Conversion efficiency is high (85 to 90 per cent).

Output waveform may vary between that of a square wave and a sine wave (usually a filter is required to produce a sine wave).

# Circuit Analysis.

Ganaral. The inverter changes a dc input to an ac output. The output of a square-wave multiviirator, puke generator, or oscillator, is used to gate a siliconcontrolled rectifier (SCR) and produce a flow of current in one direction through a transformer primary for one **half-cycle** of operation. A means of applying a reverse voltage is used to block and turn off the first controlled rectifier at the time that a second 8(7R is triggered during the next **half-cycle**, or the phase between the output current and voltage is controlled so that the current drops to zero or below the minimum holding value to stop the SCR from conducting at the end of the half-cycle. During the second halfcycle of operation, the other SCR is gated and causes current to flow in the opposite direction through the transformer primary. Thus, the output in the secondary of the transformer is an alternating current and the voltage is at a frequency which is half that of the primary oscillator. Normally, the output frequency is fairly stable, but does tend to vary somewhat with the load. Therefore, in the more expensive inverters, provisions are usually made to insert a synchronizing voltage to make the output frequency constant. In the basic inverter, the output voltage also varies somewhat with the load, so that for precise voltage applications voltage regulator circuits are also included.

**Circuit Operation.** The schematic of a simple basic single-phase inverter using **silicon-controlled** rectifiers is shown in the accompanying illustration.





supply lead through the center tap, as shown in the

#### **Typical SCR Parallel Irrverter**

In the schematic, the pulse generator is shown in block diagram form, since it may be any one of a number of types of oscillators or multivibrators described in the Oscillators or Multivibrators Sections of this handbook. It is ordy necessary that it produce an output sufficient in amplitude and duration to gate the controlled rectifiers. Resistors R1 and R2 are current-limiting resistors used to hold the dc firing current, rectified by diodes CR2 and CR3, to a safe vahre. Capacitor C is used to provide a turn-off voltage for the controlled rectifiers. Transformer T1 is the output and ac supply transformer, and inductor L provides an increase in efficiency, permitting each SCR to fire for a complete half-cycle of operation. CRI and CR4 are silicon-controlled rectifiers, employed as polarity reversing switches for the transformer primary.

Assume for the moment that controlled rectifier CRI is conducting; hence, electron current flows from the negative dc supply lead through choke L, controlled rectifier CR1, and the top half of the primary of transformer T1, and returns to the positive

Primary Current Flow

As the dc current through the primary of T1 increases, it develops an output voltage in the transformer secondary. At the same time, capacitor C is negatively charged through controlled rectifier CRI, since the opposite plate is connected to the positive supply through T1. The inductance of choke L causes the leading edge of the output waveform to taper slightly, and as the current flow reaches its peak vahre, the resistance of the choke produces a small voltage drop for the duration of current flow through T1. This voltage drop causes the normally flat top of the output waveform to taper off slightly toward zero. By this time, the driving oscillator waveform reverses polarity, and applies a negative pulse to the anode of CR2 through R1, which stops the CR1 gate from conducting, but controlled rectifier CR1 remains forward-biased and continues to conduct. As the oscillator reverses polarity, a positive pulse is applied to gating diode CR3 through R2, and a positive gating voltage is produced as the diode rectifies the positive portion of the oscillator pulse. Thus, controlled rectifier CR4 is forward-biased and conducts. The instant CR4 conducts, capacitor C is connected

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across both CR1 and CR4, and the full negative voltage of the capacitor is applied to the anode of CR1 and blocks forward current flow. Hence current flow through the top half of the primary of T1 drops to zero, developing the trailing edge of the ac output waveform in the secondary. Controlled rectifier CR1 now remains in the turned-off condition until the driving oscillator again changes polarity. Meanwhile, current flows through the primary of T1 in the opposite direction, as shown in the figure. Electron flow is now from the negative terminal of the dc input supply, through CR4 and the bottom half of the primary of Tl, and out of the center tap to the positive lead. Since current flow in the primary is reversed, the voltage induced in the secondary is also reversed, and is polarized oppositely to the output produced by CR1 operation. Thus, dc current flow through the primary of T1 produces an ac output in the secondary.

When CR1 stops conducting and CR4 conducts, capacitor C is quickly discharged through CR4 (it is only required to hold its charge long enough to turn off CR1) and is recharged in the opposite direction, since the bottom plate is connected to the negative dc supply, while the top plate of the capacitor is connected to the positive lead through T1. As current flows through CR4 and the bottom half of the primary of T1, the leading edge of the output waveform is developed. The inductance of choke L causes the leading edge of the output waveform to taper off slightly, and as the current flow reaches its peak value, the resistance of the choke produces a small voltage drop for the duration of current flow through T1. This voltage drop causes the normally flat top of the output waveform to taper off slightly toward zero. When the oscillator again reverses polarity, a negative pulse is applied to gating diode CR3, stopping the gate, while a positive pulse is applied to gating diode CR2 through R1 and forward-biases controlled rectifier CR1, which again conducts. The instant CRI conducts, capacitor C is again connected across both CR4 and CR1, and this time the full negative voltage of the capacitor is applied to the anode of CR4, blocking forward current flow. Current flow through the bottom half of the primary of T1 now drops to zero, and develops the trailing edge of the positive waveform in the secondary. Controlled rectifier CR4 now remains in the turned-off condition until the driving oscillator again changes polarity. Meanwhile, current flows through the top half of the

primary of T1 in the opposite direction as shown in the figure, and the initial condition of operation is resumed. As the oscillator changes polarity, the current through the primary of **T1** is switched in synchronism, first in one direction and then in the other direction, producing an ac output in the secondary from a dc input in the primary of T1. The large inductance of L1 prevents any sudden current surges from interfering with the turning off of one SCR as the other is switched on, giving the blocking SCR sufficient time to recover its forward blocking characteristic.

Although the output of the inverter without a filter normally resembles a square wave, this is not necessarily a detriment, since it has been found that many ac devices such as motors and power supplies can be efficiently operated from these waveforms. It should be noted, however, that because of the change in waveform, the rms and average values do not have the same numerical relationships as for sine waves. Usually, a larger amplitude output is required when no fiiter is used. Although only single-phase inverters have been discussed herein, three-phase inverters may also be obtained. Operation is similar and can be considered as three single-phase inverters operating with a 120degree phase separation.

# Failure Analysis.

No Output. An open inductor, L, a shorted capacitor, C, or a defective transformer, Tl, as well as a defective pulse generator, firing circuit, or controlled rectifier can cause a no-output condition. Check the input voltage with a dc voltmeter to make certain that the dc source is available, and check both L and the primary and secondary of T1 for continuity with an ohmmeter. Also check Tl and capacitor C for shorts. Check the outputs of the puke generator with an oscilloscope to determine that both output pulses are present. If the firing output pulses are present, check the values of RI and R2 with an ohmmeter, and the forward and reverse resistance of firing diodes CR2 and CR3. Normally, to cause a loss of output it is necessary for both firing circuits and both controlled rectifiers to be defective simultaneously. If only one rectifier and one firing circuit operate, there will be a partird output rather than none at all. If there is no output from the firing circuit, both controlled rectifiers will remain blocked, and no ac output will be obtained. If dc firing gates are present but

neither CR1 or CR4 fires, both controlled rectifiers are probably defective. Firing of the controlled rectifiers may be checked by measuring the potential between anode and cathode with a dc voltmeter. If **full** supply voltage indication is obtained, the rectifier is not firing. If no voltage or ordy a few volts indication is obtained, the rectifier is conducting, since the forward **resistance** of the SCR is only a few ohms at most.

Low Output. Low dc supply voltage, a high resistance in controlled rectifiers CR1, CR4, or both, a leaky capacitor, C, or a defective transformer, Tl, as well as erratic firing can cause a low output voltage. Check the dc supply voltage with a dc voltmeter, and measure the dc resistance of inductor L with an ohmmeter. Check capacitor C for leakage with a capacitance checker. Check the primary and secondary of TI with an ohmmeter for a higher or lower resistance than normal.

Erratic firing can be caused by a change in the constants of the firing circuit, or a change in the gating characteristics of the controlled rectifier. Observe the tiring circuit and the output with an oscilloscope. If the firing pulses occur at the same instant from the start of operation, but the controlled rectifiers fire at different times, it is most probable that the SCR characteristic has changed and the value of the firing pulse appears normal and the parts in the gating circuit check normal, the fault must be a defective controlled rectifier. When the firing pulses are erratic or occur at different times in each cycle, each part in the pulse generator must be checked to determine where the lack of symmetry occurs.

## SCR REGULATOR

# Application.

**The** silicon< **ontrolled** rectifier regulator is generally used as a combined rectifier and regulator for high-current, high-voltage power supplies, particularly for transistorized equipments.

## Characteristics.

Operates both as a rectifier and a regulator.

Controls on and off time of rectifier to regulate voltage and power output.

**Uses** a unijunction transistor **as** a relaxation oscillator to develop the firing puke.

Uaes bridge rectification with a transformer.

## Circuit Analysis.

Generel. The silicon-controlled rectifier regulator uses a phase< ontrolled or time-controlled arrangement of rectifiers. Under normal load, the output is maintained by conduction over a portion of the ac cycle. When a load change produces a tendency for the output voltage to rise, the conduction cycle is reduced, providing a reduction in output voltage. When the load increases and the output voltage tends to fall, the conduction cycle is increased, providing an increase in output voltage. Thus, by controlling the conduction time of the rectifiers, the output is automatically regulated. Since there is no series resistance used to produce a controlled voltage drop, as in other types of regulators, the controlled rectifier circuit is usually more efficient. Normally, the circuit operates directly from the line and does not require a voltage transformer. Where higher voltages than line voltages are required, a transformer maybe used to supply the

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desired high voltage, provided that the proper voltage ratings are observed when selecting the semiconductor rectifiers.

**Circuit Operation.** The schematic of a typical silicon-controlled rectifier regulator is shown in the accompanying illustration.



Silicon-controlled Rectifier Regulator

Transistor Q1 is the NPN control amplifier with base bias supplied by R4 and emitter voltage by breakdown diode CR2. Resistors R8 and R9 form a voltage divider across the output to provide a sensing voltage, with C2 used as a stabilizing capacitor. Resistor RI and breakdown (Zener) diode CR1 provide a constant supply voltage to the control circuit from the secondary diode bridge rectifier consisting of CR3, CR4, CR6, and CR7. Silicon-controlled rectifiers Q3 and Q4 also form a primary bridge rectifier with diodes CR6 and CR7. Resistors R2 and R3 are current-limiting resistors for the firing circuit, which uses unijunction transistor Q2 to supply the firing pulse. The firing pulse is developed across the base B1 resistor R7, with R6 supplying the base voltage to B2; **R5** is the emitter resistor of O2 and also the collector resistor of Q1, while capacitor Cl is the charging capacitor. Inductor L1 and capacitor C3 are conventional power-supply falter elements for smoothing the dc output. Diode CR5 is a protective and stabilizing

element which discharges inductor L1 through the load when the controlled rectifiers are not conducting; it also eliminates any inductive transients generated by the rapid on-off switching of the rectifiers.

Normally, controlled rectifiers Q3 and Q4 are in a nonconducting condition until gated by a firing puke. During this period, the secondary bridge circuit consisting of diodes CR3, CR7 and CR4, CR6 alternately conducts and produces a dc output for operation of the control circuit. This output is applied to current-limiting resistor RI and breakdown diode CRI, which furnishes a relatively constant voltage to base-2 of unijunction transistor Q2 through R6, and charging current through R5 for capacitor C1. The **secondary** bridge circuit also supplies emmiter voltage to Q2 and collector voltage to control transistor Q1. The circuit, consisting of R5, R6, R7, C1 and Q2, comprises a relaxation type oscillator. Normally, Q2 is biased practically to cutoff, and capacitor Cl

charges at a rate determined by the RC value of R5 and Cl. When Cl charges to a value sufficient to overcome the bias, heavy emitter current flows, and Cl is discharged through base-1 and R7. A positive puke is developed across R7 by the heavy flow of current. When Cl is sufficiently discharged, the bias again cuts off current flow until Cl again reaches a peak tiring charge. The pulse developed across R7 is used as a tiring pulse for controlled rectifiers Q3 and Q4. Since Q3 and Q4have their outputs connected in parallel, each rectifier will conduct when a positive anode voltage is applied coincident with a positive firing pulse, and since the anodes are connected across opposite sides of the line, one anode will be positive while the other is negative. Thus, a controlled rectifier tires for each half-cycle of applied ac. Current-limiting resistors R2 and R3 prevent excessive current flow in the trigger circuit. Once a rectifier fires, it continues to conduct until the ac polarity reverses, whereupon the reverse voltage applied to the cathode stops conduction; both rectifiers remain nonconducting until the next trigger pulse fires the other rectifier during the next half-cycle of operation. The length of the conduction period determines the output voltage and current delivered. Without filter L1 and C3, the dc output would be a series of pulses, but the filter, following conventional power supply filter action, smooths the output and provides a steady continuous voltage and current. To ensure this continuous current flow, CR5 conducts during the time that both Q3 and Q4 are inoperative because of the reverse voltage developed by the discharge of choke L1. Thus current continues to flow through the load as L1 discharges. The value of L1 (and C3)is very large to ensure a practically constant current supply.

Control amplifier Q1 uses a shunt form of control circuit operating on unijunction transistor Q2 to maintain a practically constant output voltage. Regulation is accomplished by using an NPN transistor and biasing the base in a forward direction. The base of Q1 is returned through R4 to the positive output voltage bus, and the emitter is biased with a fixed reference voltage through breakdown diode CR2, which is returned to voltage divider R8 and R9 connected across the power supply. Resistor R8 is adjustable, to permit setting the bias on Q1 for the desired operating voltage. Bypass capacitor C2 is a large value which helps stabilize the emitter voltage by breakdown

diode CR2, any chsnge of base voltage changes the conduction of Q1. When the base voltage of Q1 increases with an increase in output voltage, Q1 draws a larger emitter current and effectively shunts relaxation capacitor Cl. Hence, Cl takes a longer time to charge and fire Q2, and controlled rectifiers Q3 and Q4 conduct for a smaller period of time, reducing the output voltage. When the output voltage tends to drop, the base bias on Q1 is reduced, and capacitor Cl charges more quickly as the shunting effect of Q1 emitter current is reduced. Hence Q3 and Q4 fire earlier in the cycle and produce a larger output voltage.

The accompanying waveform charts show two typical forms of operation, one for a low voltage output and the other for a high voltage output.



**Typical Waveforms** 



The ac input is a typical sine wave for both conditions. For the low-voltage output, 11, which is the current passed by Q3, occurs during the latter part of the positive half-cycle of input, while 12, the current passed by Q4, occurs for a corresponding period during the negative half-cycle. For each of these conduction periods, a dc output puke is produced as shown by VI. During the nonconducting period, 13 flows through CR5, discharging inductance L1. The smoothing filter averages out the dc puke to a constant value at the output, shown as V2. For the high voltage output, 11 and 12 occur earlier in the ac cycle and last for a longer period of time, producing a larger dc pulse output, as shown by VI. Because of the longer periods of controlled rectifier conduction, L1 discharges for a smaller period, shown by 13. With less discharge of L1 and a larger dc pulse output, the smoothing tilter averages out a higher dc output voltage.

# Failure Analysis.

**Genaral. When making voltage checks, use a vacuum-tube** voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be **careful** also to observe proper polarity when checking continuity, since a forward bias through any of the transistor or diode junctions will cause a false low-resistance reading.

No Output. Lack of line voltage, defective controlled rectifiers Q3 and Q4, lack of a liring pulse, a defective control circuit, or an open filter circuit can cause loss of output. Measure the line voltage to make certain that a blown primruy fuse is not at fault. An oscilloscope will determine that there is a firing puke at the gates of Q3 and Q4. If the firing puke is present, both Q3 and Q4 are defective. If no firing puke is present, the control circuit is at fault, or R2, R3 and R7 may be open; check them for proper value. If the resistors are satisfactory, measure the voltage across CR1. If no voltage is present, either CR3 or CR4 is defective, R1 is open, or CR1 maybe shorted. Measure the value of R1 and check the diodes. Check that voltage is present at Cl and at base-2 of Q2. If no voltage is present on base-2, check R6 for continuity and resistance. If no voltage is present at Cl, check R5 for continuity and resistance, and check capacitor Cl for a short. If voltage is present at Cl, there is still the possibility that either Q1 or Q2 is defective. The remaining circuit components, if defective, should not cause a no-output condition, but most probably a low output. If in doubt, check the value of R4, R8 and R9, and capacitor C2, and diode CR2. An open **filter** choke L1, or shorted output filter capacitor C3, may also be at fault; check L1 for resistance and continuity, and check C3 for a short with a capacitor checker.

Low Output. A low output can be caused by low line voltage; check the line voltage to make certain that the supply is not at fault. If the line voltage is normal but the output is constantly low, either the control circuit is defective, or controlled rectifiers Q3 and Q4, or diodes CR6 and CR7, maybe defective. If low voltage persists, adjust R8 first in one direction, and then in the other direction and observe with a voltmeter whether the output can be returned to normal. If normal output can be obtained by readjustment of R8, the values of the parts in the control circuit may have changed; check the values of resistors R4, R5, R6, R7, R8, and R9. It is also possible for the value of Cl to change, or for it to be leaky, or for Ql, Q2, or CR2 to be defective. If the control circuit appears satisfactory, it is also possible for CR5 or falter capacitor C3 to be defective. Should the low voltage condition still persist, the possibility exists that choke L1 has developed a high resistance. Check the dc resistance.

**High Output. A constant high output is** most probably caused by too long a firing time resulting from a defective control circuit. First try readjusting R8 to determine if the voltage can be reduced to normal. If it cannot, transistor Q1 is probably being biased off, so that it has little shunting effect on the charging of C1. Measure the value of resistors R4, R5, R8, and R9, and check C2 for a short. If the high voltage still persists, measure the voltage acrosa CR2 to be certain that it is operating. There also remains the possibility of C1 changing value and producing a smaller time constant and faster charge, or that Q1 is defective.

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# PART 2-6. ELECTROMECHANICAL POWER SUPPLIES

# DYNAMOTOR

# Application.

A dynamotor performs the dual functions of motor and generator to change the relatively low voltage of a dc power source into a much higher value for use in electronic equipments which employ electron tubes. The dynamotor may be contained within"the electronic equipment, or it may be a separate unit external to the equipment. The dynamotor is frequently used in aircraft, small-craft, and portableequipment applications where the primary source of power is dc.

#### Characteristics.

Input to dynamotor is dc; output is dc (or ac).

Dc output requires **filtering** to remove commutation ripple.

Requires filtering of input and output leads, and shielding of complete assembly to eliminate radiated interference.

A rotating machine; field poles are common to both motor and generator windings.

Has fair regulation characteristics.

Efficiency as high as 45 percent can be obtained.

# Circuit Analysis.

**Ganeral. The** dynamotor is a rotating electromechanical device used to change one value of dc voltage to a different value of dc voltage. By definition, a dynamotor is a combination electric motor and a generator having two (or more) separate rotor windings and a common set of field poles; one winding receives direct current from a primary power source and operates as a motor to produce rotation of the armature assembly, while the remaining winding(s) operates as a generator to produce a dc output voltage.

**Circuit Operation.** A simplified schematic for a typical dynamotor is shown in part A of the accompanying illustration, and a functional diagram is shown in part B of the illustration.

Capacitor Cl is an input filter capacitor provided to remove variations in the input dc voltage, caused by sparking of the brushes at the motor commutator; the capacitor also reduces interference which can be

radiated to other equipments connected to the same power source. Capacitor C2, r-f choke RFC, and capacitor C3 form a filter network at the output of the dynamotor to remove the effects of sparking at the generator commutator. Depending upon the design of the dynamotor, inductance-capacitance falters may be installed at both the input and the output to prevent undesirable voltage transients (hash), caused by commutation, from being radiated or coupled through the input and output leads to other electronic equipments. Also, in many dynamotor output circuits, because the generator commutation ripple frequency is relatively high, an iron-core choke and a capacitor (4  $\mu$ f or larger) are used to falter the dc output and remove the ripple-voltage component.

The single, rotating armature assembly carries both the motor winding and the generator winding. Each winding terminates in a separate commutator; the commutators are usually located at opposite ends of the armature assembly. The two windings occupy the same set of slots in the armature, and terminate in their respective commutators. Since the motor and



Simplified Sohemetic and Functionel Diagram of Typical Dynemotor

generator windings are both on the same rotor assembly, the field is common to both the motor and the generator. Because the field winding is connected in parallel with the motor winding, the motor is called a *shunt-connected*, or *shunt-wound*, motor. One of the desirable characteristic of this type of motor is that the speed of armature rotation remains relatively constant, regardless of the changes in load placed upon the motor; as a result, the output voltage is also held relatively constant.

When a dc voltage is applied to the low-voltage motor commutator (input terminals) of the dynamotor, current flows in the motor winding of the armature. At the same time, the applied voltage appeara across the field coils and a current flows in them to produce a strong magnetic field. The flux produced by the field reacts with the flux produced by the motor winding; this results in torque, which causes the armature assembly to ratate. Because the generator winding is wound on the same assembly, it also rotates in the same magnetic field produced by the field coils. Therefore, since the generator winding cuts the magnetic field as it rotates, this action induces a voltage in the generator winding. The dc output voltage is taken from the generator commutator of the dynamotor, is filtered if necessary, and is applied to the load.

Since the motor and generator share a common magnetic field, the relationship of input voltage to output voltage &penda on the ratio of the number of turns in the motor winding to the number of turns in the generator winding. For example, if the number of turns in the generator winding is increased (with respect to a given motor winding), the output voltage will increase accordingly; whereas, if the number of turns in the generator windirrg is decreased, the output voltage will decrease. In like manner, changing the number of turns in the motor winding (for a given generator winding) will affect the output voltage and also the speed of armature rotation. Changing the strength of the magnetic field will not appreciably affect the voltage ratio of the dynamotor. If the field strength is increased, the armature is slowed down, but the induced voltage in the generator winding remains unchanged; on the other hand, if the field strength is decreased, the armature speed increases, but the induced voltage remains the same. This is true because the field strength and the speed of rotation are inversely proportional to each other. For example, when the magnetic flux is increased in the

field, the armature speed decreases and the generator winding cuts more lines of flux at a lower speed; conversely, when the magnetic flux is decreased, the armature speed increases and the generator winding cuts fewer lines of flux at a higher speed. In either case, the induced voltage in the generator winding remains essentially the same.

The inverse relationship between armature speed and field strength is a basic principle of dc motors, and exists because of the counter emf which is generated by the armature cutting flux as it rotates through the magnetic field. The current induced by the counter emf flows in a direction opposite to that of the applied current. If the field strength of a motor is reduced, the value of the counter emf, which is dependent upon the strength of the field flux, is also reduced. A drop in counter emf allows a greater current to flow in the armature and this causes the motor speed to increase. The speed increases because the effect of the increase in armature current far exceeds that of the decrease in field flux. When the field strength is increased, the reverse action takes place. The increase in field current, and thus field strength, causes the counter emf to increase. This action decreases the applied current and thus reduces the motor speed.

One disadvantage of the dynamotor is that the output voltage cannot be adjusted to different values without changing the input to the motor and field windings. For this reason, the dynamotor must be designed for a given output voltage and load current.

Dynamotors operating from a dc source corm monly have an input voltage rating of 6, 12, or 24 volts, and, depending upon the design and output requirements, can deliver 1200 volts or more to the load. A dynamotor is not necessarily restricted to only one generator winding-more than one winding is sometimes placed on the armature to provide for additional outputs, as required. For example, a lowvoltage winding for the operation of electron-tube **filaments** maybe incorporated in the armature assembly. In this case a separate commutator for dc output (or separate slip rings for ac output) and associated brushes are required for comection to the lowvoltage winding.

One variation of this motor has, in addition to the shunt-comected field coils, another set of field coils connected in series with the motor winding. See the accompanying illustration. This type of motor is called a *compensated, compound,* or *stabilized shunt* 

motor; the flux components developed in the shunt and series field coils are combined within the dynamotor to produce a strong magnetic field. Still another variation in design utilizes a permanent magnet to furnish the magnetic field; this variation is satisfactory for many applications, and is somewhat more efficient than an equivalent dynamotor with field coils, because less input current is required for operation.



**Diagram of Compound Motor** 

#### Failure Analysis.

**General.** Dynamotors are built to high standards and are characterized by long life and relatively trouble-free operation. If normal preventive maintenance is carried out at regular intervals as recommended by the equipment maintenance handbook, few failures will result. However, many dynamotors are subject to operation under conditions which are less than ideal, and, as a result, failures do occur.

The dynamotor can best be thought of as two separate machines combined in a single frame and sharing a common magnetic field. The relationship between motor and generator is purely mechanical. There is no electrical comection between the motor and generator windings. Since the currents in the two windings flow in opposite directions, their resultant magnetic effect is zero, which effectively isolates one winding from the other. In failure analysis procedures for the dynamotor, the two windings are treated separately; that is, the input circuit is treated as a conventional dc motor, and the output circuit is treated as a conventional dc generator.

In testing the dynamotor, the procedures are the same as those given in Navy publications for similar dc machinery (dc motors and generators). It must be first established whether the trouble is of an electrical or a mechanical nature, or both; therefore, several of the more common dynamotor troubles are given in the paragraphs which follow, to help the technician recognize typical faihrres.

No Output. If the dynamotor fails to start, the input circuit and fuse should be checked to make certain that the applied input voltage is present and of the correct vahre. If necessary, the associated primary power source control or relay circuit should be checked to make certain that it is functioning normally. Also, a low applied input voltage or an open field circuit can prevent the motor from starting. If the dynamotor is operating but there is no output, the load should be disconnected and checks made to determine whether the load is shorted: after the load is disconnected, a voltage measurement can be made at the output terminals of the dynamotor to determine whether voltage is present. As a further check, a voltage measurement can be made at the high-voltage brush terminals to determine whether voltage is present at the output of the generator winding. If falter capacitor C2 or C3 should become shorted, there will be no output from the dynamotor; if capacitor C3 should become shorted, it is likely to result in the opening of the filter choke, RFC. If voltage is found to be present at the high-voltage brush terminals, the falter circuit used to remove the ripple voltage from the dc output should be checked for a shorted capacitor or an open filter choke in a manner similar to the procedures used for any other type of dc power supply.

Low Output. The primary power source is normally connected to the input of the dynamotor, using relatively short and heavy leads. Since a low applied voltage can cause a low output condition, the input to the dynamotor should be measured to determine whether the voltage is of the correct value.

A low-output condition can be the result of one or a combination of causes, and may be accompanied by a temperature rise or mechanical noise, or both. Opens or shorts in the armature windings, excessive sparking at either commutator, poor commutation because of the presence of dirt or oil, worn brushes, and brushes improperly seated are all typical troubles which contribute to a low-output condition.

If the load current is excessive, the output voltage may be below normal; therefore, the load current shor.dd be checked to determine whether it is within tolerance. As mentioned previously, this condition is

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likely to be accompanied by a temperature rise in the machine and by sparking at the commutator. A leaky bypass capacitor (C2 or c3) or a leaky filter circuit capacitor, used to remove the ripple voltage from the dc output, may cause additional load and drop the output voltage accordingly.

**Mechanical Noise.** Excessive mechanical noise in a dynamotor is another indication of impending trouble. Although the dynamotor itself (or the unit in which the dynamotor is located) is usually mounted on some form of shock-mount support, to reduce mechanical vibration and noise resulting from armature rotation, various abnormal mechanical noises can still be heard, identified, and traced to the source. High mica, an out-of-round or eccentric commutator, high or low commutator segments, and worn bearings are all typical causes of abnormal operating noise.

Broken or chipped brushes, or brushes which are not seating properly, develop a characteristic highfrequency whine, while worn or dirty **bearings** generally cause a low-frequency (or grinding) sound. Bearing failure is frequently the result of wear caused by lack of proper lubrication; badly worn bearings may allow the rotating armature assembly to strike the field poles and create additional noise.

**Commutator Sparking. Excessive sparking at the commutator is** generally an indication of brush or commutator trouble, Sparking brushes may also be an indication of excessive load current; therefore, the load current should be measured to determine whether it is excessive. As mentioned previously, this condition will likely be accompanied by a rise in the temperature of the dynamotor.

Worn brushes, lack of brush pressure, and brushes not seating properly are common causes of brush sparking; open coils in the armature assembly will also cause brush sparking. Typical commutator troubles are high or low segments, an out-of-round or eccentric commutator surface, and a high mica condition. The high-mica condition occurs when the commutator segments have worn down below the insulating mica separator strips between the copper segments. If any one of the three commutator conditions mentioned is found to exist in the dynamotor, the machine will require disassembly and repair (by the electrical shop), since it will be necessary to turn down the commutator in a lathe and then undercut the mica to a level which is below the surface of the commutator segments.

Temperature Rise. An excessive temperature rise is one of the first indications of trouble. Dynarnotors are designed for either continuous or intermittent duty, and are rated accordingly. Occasionally, a dynamotor which is rated for intermittent duty is run continuously; in this case the dynamotor is not being operated in accordance with its design rating, and a temperature rise may be expected.

An overload condition is a common cause for overheating; therefore, the load current should be checked to determine whether it is excessive. Poor ventilation resulting from restricted cooling vents or **clogged** internal air passages can cause a temperature rise because of the lack of adequate cooling-air circulation. Shorts in the commutator segments, shorted turns in the armature or field windings themselves, or winding shorts to metal parts of the armature or frame are all typical causes of dynamotor heating. Also, worn brushes or high mica on the commutator, or both, can contribute to an abnormal temperature rise. In any event, excessive heating of a dynamotor should always be considered an effect rather than a cause of trouble.

# INVERTER

#### Application.

An inverter is one form of rotary converter, and is used to change the relatively low voltage of a dc power source to ac for use by the electrical load. Depending upon the design of the inverter, the output can be either single-phase or polyphase (multiphase) ac; the frequency of the output voltage is generally 60, 400, or 800 Hz. The inverter is frequently used in aircraft, shipboard, and small-craft applications where the primary source of power is dc.

# Characteristics.

**Input** to inverter is dc; output is ac.

Requires faltering of input leads to eliminate possible interference resulting from commutation.

A rotating machine; commonly uses two sets of rotors and stators, one set (rotor and stator) functioning as a motor and the other as a generator.

AC output commonly obtained by either of two methods: a stationary field with output taken from a rotating armature, using slip rings and brushes, or a rotating field (rotor) with output taken from one or more stationary armature (stator) windings.

Frequency of output controlled by speed of rotation.

Has fair regulation characteristics; output varies with dc input.

Maximum efficiency obtained when power factor of load is near unity.

# Circuit Analysis.

**General. The** inverter is a rotating electromechanical device for converting direct current into alternating current. The inverter is a combination electric motor and alternator; the motor is the prime mover which produces the necessary rotation of an armature, field, or rotor assembly. By definition, the winding in which the output voltage is generated is called an *armature windrng*, and the winding through which dc is passed to produce an electromagnetic field is called the *field winding*.

Inverters fall into three general classes, depending upon the ac generator design. These classes are called the *rotating-* or *revolving-arrnature*, *the rotating-* or *revolving-field*, and the *inductor-type alternator*.

In the rotating-or revolving-armature ac generator, the stator provides a stationary electromagnetic field. **The** rotor, acting as the armature, revolves in the magnetic field, cutting the lines of force, and produces the desired output voltage. The armature ac output is taken through slip Mgs and bmshes. One limitation of this type of generator is that the output is taken through sliding contacts (slip rings and brushes); therefore, this type of machine is usually limited to low-power, low-voltage applications.

The rotating- or revolving-field ac generator is most widely used. In this type of machine, current from a dc source is passed through slip rings and brushes to field coils wound on a rotor. Thus, a magnetic field is produced in the rotor of fixed polarity, and, since the rotor is driven by the motor, a rotating magnetic field is created. The rotating magnetic field extends outward and cuts the stationary armature (stator) windings; as the rotor turns, ac is produced in the stationary windings. The output is taken from the stationary windings, either single-phase or polyphase, through the output terminals to the load without the need for slip rings and brushes.

In the inductor-type alternator, a field (exciter) winding and an armature winding are both contained within the same stator frame. The rotor, including its pole pieces, is made of soft-iron laminations. DC is supplied to the field (exciter) winding, thus estab

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Iishing a magnetic field in the stator. As the rotor revolves, the poles of the rotor become aligned with the poles of the stator, and maximum flux density is produced. As the poles move out of alignment, the flux decreases. The sinusoidal increase and decrease in magnetic flux in the rotor and stator as the rotor rotates induces an alternating voltage in the stationary armature windings. The ac output is taken from the stationary armature windings without the need for slip Mgs and brushes. This type of machine is frequently used to generate single-phase, highfrequency ac.

The frequency of the ac generator voltage depends upon the speed of rotation of the rotor and the number of pairs of poles in the machine. That is:

$$\mathbf{F} = \frac{Px rpm}{60}$$

where P is the number of pairs of poles, and rpm is the revolutions of the rotor per minute. The following **examples** are provided to illustrate the use of the formula in solving for rpm, F, and P.

Alternators are generally designed with a multipole rotor and a multipole stator; however, for simplicity, the first example will consider a basic alternator having only a two-pole rotor and a two-pole stator. In this machine one complete cycle of ac voltage will be induced in the armature winding for each complete revolution of the rotor as it passes under the two (north and south) poles of the stator. When the rotor of this simple machine rotates at a rate of 3600 rpm, the frequency (in Hz) of the ac output voltage is easily found by using the basic formula. Thus:

$$\mathbf{F} = \frac{\mathbf{P} \times \mathbf{rpm}}{60}$$
$$= \frac{1 \times 3600}{60}$$
$$= 60 \text{ Hz}$$

If six poles are provided on the rotor and on the stator of an ac generator, then during each revolution each pair of rotor poles passes under three pairs of stator poles, and thus generates three complete cycles of ac output. Since there are three pairs of poles provided on the rotor, it follows that three times as many cycles will be generated during one rotor **revo**lution as will be for a single pair, or a total of nine

hertz. Assuming again that the output frequency is 60 Hz, the required rpm of the rotor may be found by transposing the basic formula to solve for rpm. **Thus**:

$$rpm \cdot \frac{60 \text{ F}}{\text{P}}$$
$$= \frac{60 \text{ X 60}}{3}$$
$$= \frac{3600}{3}$$
$$= 1200 \text{ rpm}$$

This example clearly illustrates the inverse relationship existing between the speed of rotor rotation and the number of pairs of poles of the alternator. For the same output frequency as in the first example (60 Hz), when the number of pairs of poles was increased by a factor of three, the required rpm of the rotor was decreased by one third, that is, from 3600 to 1200 rpm.

When the speed of rotor rotation and the output frequency of the alternator are known, the number of pole pairs is easily found. For example, if F = 400 Hz and the rotor rotation is 3000 rpm, then the number of pairs of poles is found as follows:

$$\mathbf{P} = \frac{60 \text{ F}}{\text{rpm}}$$

$$.60 \text{ X } 400$$

$$3000$$

$$.24000$$

$$3000$$

= 8 pairs of poles

When the load on a generator is changed, the terminal voltage varies with load. The amount of variation depends on the design of the generator and the power factor of the load. Unless the load is fixed and constant, some form of voltage regulation is necessary to maintain the output voltage relatively constant under conditions of varying load. In practice, once a machine is designed and built, the output voltage is controlled by varying the dc excitation voltage ap plied to the field winding. When an ac generator is equipped with a voltage regulator, the regulator uses the ac output voltage which is **to** be regulated as a sensing voltage to control the amount of current used to excite the field.

The operation of a typical regulation system can be briefly explained as follows: a drop in output voltage sensed by the regulator causes the regulator to increase the field current, and an increase in field current causes a corresponding increase in output voltage to compensate for the original drop in output voltage. Stated conversely, if the output voltage should rise, the regulator decreases the field current, causing a corresponding decrease in output voltage to compensate for the original rise in voltage. Thus, the regulator senses a change in output voltage and compensates for this change by altering the field (exciting) current accordingly. A detailed description of the construction and operation of various voltage regulators can be found in Navy publications covering basic electricity, or in course materials for EM and AE ratings.

Several typical inverters will be discussed briefly in the paragraphs that follow.

Inverter with **Permanent-Magnet** Rotor. One of the simplest inverters is the permanent-magnet-type inverter shown in the accompanying schematic. This rotating-field-type inverter is designed to supply single-phase ac at a frequency of either 400 or 800 Hz to a constant and relatively light load.

The inverter consists of a dc motor and a permanent-magnet-type ac generator assembly combined within a single housing. The dc motor is a shunt-connected, or shunt-wound, motor with armature and commutator mounted on a single shaft, and rotating within the stationary field (stator) windings. **The** motor armature rotates within the stationary field, and the commutator rotates between a pair of spring-loaded brushes. The motor brushes are



Simple Inverter with Permanent-Magnet Rotor; Single-Phase Output

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mounted in holders that are placed on opposite sides of the motor housing; the construction is such that the brushes may be easily removed for inspection and replacement.

The ac generator portion of the inverter consists of a stationary armature and a rotating permanentmagnet field. The permanent-magnet rotor is mounted on the same shaft as the motor armature and commutator. The rotating magnetic field is produced by a six-pole, permanent-magnet rotor, with alternate poles around the circumference magnetized alike. The stationary armature (stator) is a six-pole, six-slot, laminated stator with the single-phase output winding mounted in the slots of the stator. A magnetic field exists about the poles of the permanentmagnet rotor, and as the rotor revolves the poles of the rotor align with the poles of the stator to produce maximum Iux density in the stator. As the poles move out of alignment, the flux decreases in the stator to a minimum, and the flux polarity reverses as the rotor poles move into alignment with the stator once again. The sinusoidal changing of flux polarity as the rotor poles move past the stator poles induces an alternating current in the armature windings located in the slots of the stator. 'I'he ac output is taken from the stationary armature windings, without the need for slip rings and brushes. Since this inverter is designed for use with a constant load, no provision is made for either voltage or speed regulation.

The permanent-magnet-type inverter can also be made to furnish three-phase output. The three-phase inverter, shown in the accompanying schematic, is essentially the same size and weight as the singlephase inverter described above. The dc motor is essentially the same as that described for the single-phase machine. Also, the sixpole, permanent-magnet rotor of the generator is placed on the same shaft and rotates with the motor armature, as described for the single-phase machine. **The** three-phase stationary armature consists of a nine-pole laminated stator. In this generator nine sep arate coils are wound in the stator slots; each set of three coils, located 120 degrees apart on the stator, are connected in series to form an output winding for each phase. The three sets of series coils produce output voltages which differ in phase by 120 electrical degrees; the stator windings are shown on the schematic as a three-phase wye, or star, connection.

As in the single-phase machine, a magnetic field exists about the six poles of the permanent-magnet rotor. When three of the rotor poles spaced 120 degrees apart are in alignment with three of the stator poles of the same winding phase, the remaining three rotor poles are positioned between the remaining six stator poles. Thus, when maximum flux is produced in one set of stator poles, one of the remaining two sets of stator poles is increasing in flux density, while the other set is decreasing in flux density. The flux polarity in any stator pole reverses as alternate rotor poles have past the individual stator poles; as a result, the changing flux induces an alternating current in each of the three armature windings which is 120 degrees out-of-phase with the current produced in either of the other two armature windings. The three-phase ac output is taken from the three stationary armature windings without the need for slip rings and brushes. Since this inverter is designed for use with a constant load, no provision is made for either voltage or speed regulation.

Inverter with Rotating Armature. The inverter shown in the accompanying schematic is typical of many inverters with separate dc fields for the motor and generator sections. This type of inverter has a stationary field, and the armature windings rotate within the magnetic field produced by the field. Although the schematic shows an inverter with threephase output, the same principles discussed here apply to an inverter with single-phase output.



Simple Inverter with Permanent-Magnet Rotor; Three-Phase Output

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Inverter With Rotating Armature

The dc motor shown in the accompanying schematic has a compounded field consisting of both a series and a shunt winding. This type of motor provides better speed regulation under conditions of varying load; as a result, the output frequency can be held relatively constant. To further improve the frequency stability of the inverter, a speed governor is incorporated in series with the shunt winding to control the shunt-field current and, therefore, the magnetic flux developed by the shunt field. The governor is a centrifugal type, mounted on the armature shaft of the motor. Electrical connection to the governor contracts is accomplished by two slip rings, located at the commutator end of the armature; brushes are used to contact the slip rings and complete the circuit to the speed regulating resistor, RI. The governor controls the speed of the motor by placing resistor RI into and out of the shunt-field circuit. For example, when the motor attempts to increase speed, the governor contacts close to shunt the resistor, RI. (The governor contacts open and close by centrifugal action.) As a result, the current through the shuntfield winding increases, the magnetic flux developed by the field increases, and the motor speed is reduced accordingly. Conversely, when the motor attempts to decrease speed, the governor contacts open and resistor R1 is placed in series with the shunt-field winding. In this case, the current through the shunttield winding decreases the magnetic flux developed

also decreases, and the motor speed is increased accordingly. By controlling the motor speed, the centrifugal governor thus controls the resulting frequency of the ac output.

The generator portion of the inverter consists of a stationary four-pole field and a three-phase, wye- or star- connected rotating armature. The armature windings are distributed and mounted in the slots of the laminated rotor core, and are brought out to three slip rings which are mounted on the rotor shaft; bmshes contact the slip rings to complete the circuit.

The stationary field, consisting of four seriescomected coils (each placed on a pole piece), is supplied direct current from the dc input to the motor. The strength of the magnetic flux developed by the field is determined by the current which passes through the field windings; consequently, this current also determines the amplitude of the output voltage produced in the armature windings. Resistor R2 is placed in series with the field windings to adjust the value of current through the windings and thus control the amplitude of the ac output voltage in all three phases.

If the electrical load on the inverter is relatively constant, the output voltage is likely to remain relatively constant; thus, resistor R2 is usually adjusted under conditions of normal load to obtain the desired output voltage. However, when the electrical load is subject to considerable variation, a system of voltage regulation must be employed. As mentioned in a previous paragraph, voltage regulation can be achieved by sensing the ac output voltage and then controlling the magnetic field to compensate for the original output-voltage variation. A typical system for output-voltage regulation uses dc voltage rectifier from one of the phases to control a carbon-pile voltage regulator. The regulator, in turn, substitutes for resistor R2 in the field circuit and varies the current through the field windings; thus, the magnetic flux of the field is varied. As a result, the ac output voltage amplitude is controlled by action of the carbon-pile regulator to compensate for changes occurring in the output voltage. (A detailed description of generator and alternator voltage regulation is found in Navy publications covering basic electricity and, therefore, is not given in this handbook.)

In the inverter described here, the output can be set to a given value by adjustment of resistor R2, or the output can be automatically regulated by a regulating system which substitutes for resistor R2. The

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governor assembly, together with resistor RI, on the dc motor controls the speed of rotation and thus the frequency of the ac output. One disadvantage of this inverter is that all current delivered to the load must pass through the slip rings and brushes of the armature assembly. Therefore, the use of this type of inverter is usually limited to low-power, constant-load applications, where the use of slip rings and brushes will not seriously affect operating efficiency.

Inverter with Rotating Field. The inverter shown in the accompanying schematic has a rotating field and stationary armature windings; the machine is similar to the inverter using a permanent-magnet rotor, described earlier, except in this instance a dc rotor field is used. Although the schematic shows an inverter with three-phase output, the same principles discussed here apply to an inverter with single-phase output.

The dc motor shown in the accompanying schematic has a compounded field consisting of both a series winding and a shunt winding. The motor is identical with the motor just described for the inverter with a rotating armature. The motor is equipped with a centrifugal governor, which controls the motor speed by shunting resistor RI into and out of the shunt-field circuit. (The speed-regulating action of the governor assembly and its effect upon output frequency was described in a preceding paragraph.)



#### **Inverter With Rotating Field**

The generator portion of the inverter consists of a rotating field assembly and stationary armature

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windings. DC exciting coils for the rotating field are wound on the six-pole rotor, and are brought out to two slip rings which are mounted on the rotor shaft; brushes contact the slip rings to complete the dc circuit to the rotating field. The direct current for the rotating field is obtained from the dc input to the motor. The strength of the magnetic flux developed by the rotating field is determined by the current which passes through the field windings; consequently, this current rdso determines the amplitude of the output voltage produced in the stationary armature windings. Resistor R2 is placed in series with the field windings to adjust the value of current through them, and thus controls the amplitude of the ac output voltage in all three phases.

The three-phase stationary armature consists of a nine-pole, laminated stator, similar to the armature described previously for the three-phase inverter using a permanent-magnet rotor. The nine separate coils of the stator are connected to form three sets of three series coils each; the three sets of series coils produce output voltages which differ in phase by 120 electrical degrees. The armature (stator) windings are shown on the schematic as a three-phase wye or star connection.

If the electrical load on the inverter is relatively constant, the output voltage is likely to remain relatively constant; thus, resistor R2 is usurdly adjusted under conditions of normal load to obtain the desired output voltage. However, when the electrical load is subject to considerable variation, a system of voltage regulation must be employed. The voltage and output-frequency regulation principles for this inverter are identical with those given in previous paragraphs for the inverter with rotating armature.

One advantage of this type of inverter is that the three-phase ac output is taken directly from the stationary armature windings without the need for slip rings and brushes; for this reason the inverter is cornmordy used for high-power applications, because the load current is not required to pass through the resistance offered by moving contacts (slip Mgs and brushes).

Inductor-Type Alternator. The inverter shown in the accompanying schematic is typical of inverters which operate on an induction principle and employ stationary field and armature windings located sideby-side in a common frame; the stator windings and their associated poles share a common rotor assembly. The dc motor shown in the accompanying schematic has a compounded field consisting of both a series winding and a shunt winding. The motor is identical with the motor previously described for the inverter with a rotating armature. **The** motor is equipped with a centrifugal governor which controls the motor speed by shunting resistor RI into and out of the shunt-field circuit. (The speed-regulating action of the governor assembly and its effect upon output frequency were described in the discussion on Interter with Rotating Armature.)

The generator portion of the inverter consists of a six-pole, laminated rotor mounted on the end of the dc motor shaft, and a stator assembly with two dualpole pieces on which the stator windings are mounted. The two dc field (exciting) coils, connected in series, are mounted around both dual-pole pieces, which are opposite each other in the stator assembly; the four ac armature coils, connected in series, are mounted around the individual poles of the two dualpole pieces.



Inverter With Inductor-Type Alternator; Single-Phase Output

Direct current is supplied to the dc field (exciting) coils of the stator from the dc input to the motor. The field coils establish a magnetic field in each of the two **dual-pole** pieces that make up the stator as-

sembly, as shown in the illustration below. The current passing through the field determines the strength of the magnetic flux developed by the dc field winding, and thus the amplitude of the output voltage. Resistor R2 is placed in series with the field winding to adjust the value of field current, in order to control the amplitude of the ac output voltage.



Basic Inductor-Type Alternator

For a given value of current in the dc field winding (as determined by the adjustment of resistor R2), the strength of the field flux linking the ac armature coils on the stator will vary as the reluctance of the magnetic circuit is varied. Because of the high permeaility (as compared with air) of the soft iron laminations of the rotor, the reluctance is varied as the poles of the revolving rotor continuously move in and out of alignment with the poles of the stator. As the rotor revolves and varies the reluctance of the magnetic circuit, the strength of the magnetic field and. consequently, the amount of induction coupling to the ac coils will also vary. The periodic variation in induction coupling, which is sinusoidal in nature, induces an alternating current in the ac armature coils. This current achieves a maximum value at a time when the poles of the rotor and stator are in alignment, and reaches a minimum value when the

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rotor and stator poles are farthest out of alignment. One cycle of generated voltage occurs in the armature winding as the rotor rotates through an angle equal to the angle of separation for adjacent rotor poles. Since it is relatively easy to build a machine with a large number of rotor poles, the inductor-type design is readily **adaptable** to the generation of high frequencies. For a given number of rotor and stator poles, the induced voltage in the armature **windings** alternates at a frequency determined by the speed of the rotor assembly.

If the electrical load on the inverter is relatively constant, the output voltage is likely to remain relatively constant, and, as for the other inverters previously described, resistor R2 is usually adjusted under conditions of normal load to obtain the desired output voltage. However, when the electrical load is subject to considerable variation, a system of voltage regulation must be employed. The voltage and output-frequency regulation principles for the inductor-type alternator are identical with those given in previous paragraphs for the inverter with rotating armature.

The inductor-type alternator is frequently used in applications where high-frequency output at a moderate power level is required. One advantage of this type of inverter is that no slip rings or brushes are used for the alternator portion of the inverter, the output being taken directly from the armature windings.

# Failure Analysis.

**General.** Inverters generally provide trouble-free operation as long as normal preventive maintenance is performed in accordance with the procedures recommended by the equipment maintenance handbooks. However, the technician must be aware of possible failures and be able to recognize such failures when they occur.

The inverter can best be thought of as two separate machines combined in a single housing and sharing a common rotating shaft. The relationship between the dc motor and ac generator (or alternator) is essentially a mechanical one; therefore, in failure-analysis procedures for an inverter, the dc motor and ac generator are usually treated as separate machines mechanically coupled to each other. In testing inverters, the procedures are the same as those given in Navy publications for similar dc motors and ac generators. It must be first established whether the trouble is of an electrical or a mechanical nature, or both; therefore, several of the more common dc motor and ac generator troubles are given in the paragraphs which follow to help the technician recognize typical failures.

**Temperature Rise. As stated** previously for the dynamotor, an excessive temperature rise in an inverter is one of the first indications of trouble. Excessive heating of an inverter should always be considered as an effect rather than a cause of trouble.

An overload condition is a common cause for overheating; therefore, the load current should be checked to determine whether it is excessive. The three-phase inverter offers a problem in distributing the electrical load equally between the three phases. For this reason, it is possible that one phase may become overloaded and cause overheating of the machine because of the load unbalance; therefore, the load current in each phase should be checked to determine whether it is excessive and whether the load is balanced for each phase.

Poor ventilation, resulting from restricted cooling vents or clogged internal air passages, can cause a temperature rise because of the lack of adequate coolingair circulation. Shorts in the dc motor commutator segments or shorted turns in the motor armature **windings**, shorted turns in the **motor** field windings themselves, or windings shorted to metal parts of the armature or frame are all typical causes of motor heating. Worn brushes or high mica on the commutator, or both, can also contribute to an abnormal temperature rise in the motor. Shorted turns in the windings of the ac **generator** (alternator) rotor or stator can also contribute to a temperature rise in the machine.

**Mechanical Noise.** Excessive mechanical noise in an inverter is another indication of impending trouble. Although the inverter itself (or the unit in which the inverter is located) is usually mounted on some form of shock-mount support, to reduce mechanical vibration and noise resulting from the rotating parts of the machine, various abnormal mechanical noises can still be heard, identified, and traced to the source. High mica, an out-of-round or eccentric motor commutator, high or low motor commutator segments, and dry or worn bearings are all typical causes of abnormal operating noise.

Broken or chipped motor brushes, or brushes which are not seating on the commutator properly, develop a characteristic whine; however, this noise

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**may** not be readily heard because loose rotor Or stator laminations in the ac generator portion of the machine may develop a high-frequency sound which masks the commutation noise. Worn or dirty bearings generally cause a **low-frequency** (or grinding) sound, and may also result in the generation of additional heat. Bearing failure is **frequently** the result of wear caused by lack of proper lubrication; badly worn bearings may allow the rotor assembly to strike the stator **and** create additional noise. Furthermore, a rotor which is not centered in the stator because of worn bearings, although it may not strike the stator, is likely to cause some localized heating in the stator.

Motor Commutator Sparking. Excessive sparking at the motor commutator is generally an indication of brush or commutator troubles. Sparking brushes may also be an indication of open or shorted coils in the armature winding, or an indication of a grounded, open, or shorted field winding. As mentioned previously, this condition will likely be accompanied by a rise in temperature of the machine. Worn brushes, lack of brush pressure, brushes sticking in their holders, or brushes not seating properly are also causes for sparking.

Typical dc motor commutator troubles are high or low segments, an out-of-round or eccentric commutator surface, or a high mica condition. (The high mica condition occurs when the commutator segments have worn down below the insulating mica separator strips between the copper segments.) If any one of the three conditions mentioned is found to exist in the motor commutator, the machine will require disassembly and repair (by the electrical shop), since it will be necessary to turn down the commutator in a lathe and then undercut the mica to a level which is below the surface of the commutator segments.

No **Output.** If the inverter fails to start, the input circuit should be checked to make certain that the applied dc voltage is present and of the correct value. If necessary, the associated primary power source control or relay circuit should be checked to make certain that it is functioning normally. A low applied input voltage or an open field circuit can also prevent the motor from starting.

If the inverter is running but there is no output, the load should be disconnected and checks made to determine whether the load is shorted; a voltage measurement can be made at the output terminals of the ac generator after the load is disconnected to determine whether voltage is present. In the case of the three-phase inverter, measurements should be made on each of the three phases. With the inverter disconnected from its input and output circuits, continuity measurements can be made in accordance with the **equipment** maintenance handbook instructions to determine whether any of the windings are open.

Low Output. A low-output condition can be the result of one or a combination of causes, and may be accompanied by a temperature rise or mechanical noise, or both. Low input dc to the exciter coils, poor slip ring contact because of the presence of dirt or oil, worn brushes, and improper brush tension are typical troubles which contribute to a low-output condition.

Shorted windings can cause low output, and this condition is nearly always accompanied by a temperature rise in the inverter. If the load current is excessive, the output voltage may be below normal; therefore, the load current should be checked to determine whether it is within tolerance. For the three-phase generator or alternator, the load current for each phase should be checked to determine whether it is within tolerance and whether the load is balanced for each phase. As mentioned previously, an unbalance in the load of the three-phase machine is likely to cause a temperature rise in the machine.

A low-output condition can also be caused by a decrease in the current through the exciting field; as a result, the magnetic flux in the field decreases and the output voltage decreases accordingly. If the dc (exciting) field current is controlled by a voltage regulating system, it is possible that the system is faulty. If the field current is established by means of an adjustable resistor (resistor R2), it is possible that the value of the resistor is too high. In the case of the inverter with rotating field, the slip Mgs and brushes may cause this condition because of excessive contact resistance.

**High Output A high-output** condition is usually caused by an excessive current in the exciting field; as a result, the magnetic flux in the field increases and the output voltage increases accordingly. If the dc (exciting) field current is controlled by a voltage regulating system, it is possible that the system is faulty. If the field current is established by means of an adjustable resistor (resistor R2), it is possible that the value of the resistor is too low.

Unsteady Output Voltage. The cause of unsteady or fluctuating output voltage, sometimes called voltage hunting, varies, depending on the design of the inverter and the method incorporated in the machine to regulate the vrdue of the output voltage. If the output voltage fluctuates (assuming the speed of rotation to be relatively constant), this condition maybe caused by fluctuations of the current in the exciting field; as a result, the magnetic flux in the field will also fluctuate. This condition may also be caused by a defective voltage-regulating system (mentioned previously under the high-output and low-output conditions discussed above), or, if the inverter has a rotating field, the slip rings and brushes may not be in good contact with each other.

Unsteady or Incorract Output Frequency. The cause of unsteady output frequency, sometimes called *frequency hunting*, or simply *hunting*, and the cause of incorrect output frequency varies, depending on the design of the inverter and the method incorporated in the machine to regulate the speed of rotation. If the sped of rotation fluctuates, the output frequency will also fluctuate, since the speed of the rotor determines the frequency of the alternations in the armature windings. Thus, if the rotor speed is below normal, the output frequency will also be below normal, and, conversely, if the rotor speed is above normal, the output frequency will also be above normal. If the dc motor has a centrifugalgovemor assembly, the governor contacts, slip rings, and brushes should be inspected for possible defects. Instability in the motor speed may also be evidenced by mechanical noises, temperature rise, brush sparking, etc, mentioned earlier in this discussion.

#### NONSYNCHRONOUS VIBRATOR SUPPLY

#### Application.

The nonsynchronous vibrator supply is commonly employed in many portable and mobile equipments where the primary power source is a storage battery. This supply produces a relatively high value of dc voltage at a moderate load current from a low-voltage dc source. The supply is commonly used to provide high voltage for the operation of small receivers, transmitters, and public-address systems, although in many recent equipments the transistorized dc-todc converter, described earlier in this section of the handbook, is used in lieu of the vibrator supply.

## Characteristics.

Input is low-voltage dc; output is high-voltage dc. Input voltage is usually 6, 12, or 24 volts; **special** vibrators for other input voltages are available.

Typical vibrator operating frequency is between 60 and 250 Hz.

Output high-voltage dc is normally between 180 and 300 volts; load current is normally between 60 and 200 milliamperes.

Output circuit can be arranged to furnish negative or positive high voltage to the load.

Output dc requires filtering; ripple-voltage frequency is relatively high, and is determined by the vibrator frequency and the rectifier circuit used.

Electron-tube or semiconductor diodes are used in the rectifier circuit; rectifier circuit may be half-wave, full-wave, bridge, or voltage-doubler.

Regulation is fair; output voltage regulation may be employed.

Vibrator must be shielded and leads filtered to prevent r-f radiation and interference to other circuits.

## Circuit Analysis.

General. A nonsynchronous vibrator supply converts direct current from a low-voltage power source into alternating current that can be rectified and used to obtain a higher dc output voltage for use as the plate and screen voltages in the operating equipment. The supply offers the advantages of light weight, small physical size, and good efficiency; its main disadvantages are the limitation in output current and the tendency to produce interference to other circuits. Therefore, the vibrator must be well-filtered and shielded. Another disadvantage is that, although the vibrator itself is relatively inexpensive, its useful life is shorter than that of a dynamotor or of the transistors in a dc-todc converter. However, when this type of power supply is used within its rating, it will furnish reliable power for low-power communications and public address equipment.

Nonsynchronous Vibrator Types. A vibrator is an electromechanical mechanism, sometimes called an *interrupter*, which acts as a **high-speed** reversing switch to control (or interrupt) the current in each half of a tapped primary winding in a special step-up power transformer. The operation of a simple vibrator as a high-speed switching device can be understood by reference to the accompanying illustration of a fundamental vibrator circuit.

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Fundamental Vibrator Circuit and Output Voltage Waveform

In part A of the illustration, when switch S is closed, current flows from the battery, through the vibrator coil, and the lower half of the transformer primary. The magnetic field created by current flow through the vibrator coil attracts the armature and pulls it down against the lower contact. This places a short circuit across the vibrator coil, which causes it to de-energize and release the armature. Spring action draws the armature away from the coil, carries it through the neutral position, and drives it against the upper contact. Since the short circuit is now removed from the vibrator coil, a magnetic field again exists, which draws the armature down until it again touches the lower contact. This action continues at a rate dependent on the natural frequency of the vibrator (typically about 100 Hz).

During the time when the armature is against the lower contact, the lower portion of the transformer

primary is m me circuit. Ine airection or current flow in this half of the primary is such that the bottom of the primary winding is negative with respect to the center tap. The voltage induced in the secondary, as a result of this current, will be of like polarity, that is, positive-going with respect to the bottom of the secondary winding. This condition is indicated at time t. in part B of the illustration. When the armature switches to the upper contact, the upper portion of the transformer primary is placed in the circuit. Since the current through this half of the primary winding flows in a direction opposite to that in the lower half of the winding, a voltage pulse of opposite polarity will be induced in the secondary. This is shown at time  $t_1$ . The start of another complete cycle of operation, which is identical in every respect to the cycle just described, is shown at time  $t_2$ .

The closing of the lower and upper contacts (in succession) corresponds to one complete cycle of the vibrator frequency, and two pulses of current in alternate directions through the two halves of the transformer primary. The magnetic field created by these current pulses induces a voltage in the transformer secondary which is essentially a square wave, as shown in part B of the illustration. The output voltage does not achieve the shape of an ideal square wave because of the inductance of the transformer. As the current is continuously interrupted in the primary circuit, the alternate build-up and decay of the magnetic field both require a certain finite time. This results from the inductive reactance of the windings, which opposes both the build-up and the decay of the field. Because of this action, and of the high-voltage inductive effect (overshoot), the shape of the output voltage waveform will be as shown in the illustration. Because the vibrator switching action produces a current flow in opposite directions in the two halves of the primary during one complete mechanical cycle of the vibrating reed, the vibrator is sometimes called a full-wave nonsynchronous vibrator.

As shown in the accompanying diagram, a nonsynchronous vibrator consists of five basic parts: a heavy frame, an electromagnetic driving coil and core or pole piece, a flexible reed and armature, one or more contacts attached to each side of the reed, and one or more stationary contacts mounted on each side of the reed and armature assembly. There are two basic electrical variations in full-wave nonsynchronous vibrators; the first type is called a *shunt-drive* vibrator and the second is called a *series-drive*, (or *separate-drive*)

vibrator. These names are derived from the manner in which the electromagnetic driving coil receives its excitation. Refer to the accompanying illustration of two typical nonsynchronous vibrators; part A shows the construction of a shunt-drive vibrator together with its graphic symbol, and part B shows the construction of series-drive vibrator and its graphic symbol.



Nonsynchronous Vibrator Types

The electromagnetic driving coil is mounted on one end of the frame, as shown in the illustration, and the reed is rigidly **clamped** in insulating spacers and fixed to the opposite end of the frame. The sta-

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tionary contacts are similarly clamped at the end of the frame, on each side of the reed. Electrical connections to the vibrator are also made at this point on the frame. The vibrator assembly is usually mounted in a sound-absorbing and cushioning material, such as foam or sponge rubber, which, in turn, is sealed within a metal can. The material placed around the vibrator reduces the amount of mechanical noise created by the vibrating reed, and the metal can acts as an r-f shield to reduce direct radiation of electrical noise. The connecting leads from the vibrator are brought out to metal prongs at the base of the can, and the complete unit is plugged into a special socket in the same manner that an electron tube is installed in a tube socket; the socket also grounds the can to the chassis to completely shield the vibrator. Since the vibrator may require replacement at intervals throughout the useful life of the power supply, the plug-in method of electrical connection insures convenient and easy replacement of a defective vibrator unit.

The shunt-drive vibrator, shown in part A of the illustration, has one end of the driving-coil winding connected to the vibrating reed, which is normally connected to ground. The other end of the winding is connected to an insulated stationary contact on the electromagnetic *pull* (or power) side of the reed; this contact is connected to the top of the primary winding. As shown by the graphic symbol in Part A of the illustration, both sets of contacts are open when the vibrator is at rest; however, when voltage is applied to the vibrator circuit, current flows through the driving coil, which magnetizes the core and causes the reed armature to be pulled toward the pole piece. As this occurs, the pull (or power) contacts close to shunt or short out the driving coil as well as to complete one half of the primary circuit. (Refer to the accompanying illustration below showing typical nonsynchronous vibrator supplies.) This shunting action of the pull contacts causes the driving coil to lose its magnetic attraction for the reed armature and, as a result of the spring action stored in the reed, causes the reed to swing back away from the pull contacts to interrupt the primary circuit. The inertia of the reed carries it back across the neutral (at rest) position to the other set of contacts, called the inertia contacts, closing these contacts to complete the other half of the primary circuit. While the inertia contacts are closed, current once again flows through the driving coil and causes a high magnetic attraction to be

imparted to the reed armature. As the reed moves away from the inertia contacts, these contacts open to interrupt the primary circuit. The cycle is then repeated as the reed is carried across the neutral (at rest) position to close the pull contacts and once again shunt the driving coil. It should be noted at this time that the peak voltage applied to the driving coil, during the time the inertia contacts are closed, is approximately twice the value of the normal dc input voltage to the supply; this is because the voltage induced by autotransformer action in the half of the primary winding which is connected to the stationary pull contact is in series with the dc input voltage.





**Typical Nonsynchronus Vibrator Supplies** 

By referring to the diagram of the shunt-drive vibrator, it will be seen that when the armature is in

the neutral position (all contacts open), a complete series circuit exists from the negative side of the input source, through the driving coil and pull winding, to the positive side of the dc source. For a given value of current, as determined by the total resistance in the circuit, the portion of the input voltage that will be dropped across each of the two circuit elements will be in direct proportion to the resistance present in each element. Since the transformer primary winding offers only negligible resistance to the comparatively small and steady dc current which flows under the conditions stated, no appreciable voltage will be developed across the pull winding.

When the inertia contacts are closed, the series circuit through the driving coil and pull winding remains completed. The voltage existing across the pull winding and the voltage developed in the inertia winding have opposite polarities. Through the autotransformer action which takes place across the tapped primary, the rapidly changing magnetic field around the inertia winding induces a voltage in the pull winding; this voltage has the same polarity as that of the inertia winding. As a result, the voltage now present across the pull winding will be the difference between the induced voltage and the existing voltage. Since the induced voltage has the greater value, the polarity of the difference voltage will be the same as that of the induced voltage. Thus, not only is the counteracting effect of an opposing voltage neutralized, the the voltage in the inertia winding is effectively aided.

The series-drive (or separate-drive) vibrator, shown in part B of both illustrations (the Nonsynchronous Vibrator Types and the Typical Nonsynchronous Vibrator Supplies), differs from the shunt-drive vibrator just described in that is has an extra pair of contacts. These contacts, called starting contacts, are normally closed when the vibrator is at rest. The moving contact of this pair is mounted on the armature reed, which is normally connected to ground. The stationary starting contact is wired to one end of the driving coil. The other end of the coil is connected to the high side of the dc input voltage source, through a terminal in the base of the vibrator provided for this purpose. As shown in part B of both illustrations, both the inertia contacts and pull contacts are open when the vibrator is at rest. However, when voltage is applied to the vibrator circuit, current flows through the driving coil and causes the reed

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armature to be attracted to the pole piece (magnetized core); thus, the moving pull contact is drawn against the stationary pull contact. The closing of these contacts completes a circuit through one half of the transformer primary. The armature, in moving twoard the pole piece, opens the starter contacts, which prevents any further current flow in the driving coil; this results in the collapse of the magnetic field. The reed, now no longer attracted by the pole piece, swings back from the driving coil; this opens the pull contacts and interrupts the primary circuit. The inertia of the reed carries it back across the neutral (at rest) position to the inertia contacts, closing these contacts to complete the other half of the primary circuit. At the same time, the starting contacts close and current once again flows through the driving coil to produce a magnetic attraction for the reed armature. As the reed moves away from the inertia contacts, these contacts open to interrupt the primary circuit; at the same time the starting contacts open to interrupt the circuit to the driving coil. The cycle is then repeated as the reed is carried across the neutral (at rest) position to close the pull contacts and once again complete the primary circuit. It should be noted at this time that if the series-drive vibrator is connected in the circuit so that the driving coil receives voltage directly from the input source (through a separate contact in the vibrator base), the vibrator will continue to vibrate mechanically, even though the transformer center tap and end leads are open. This will not occur with the shunt-drive vibrator since the current to energize the driving coil must pass through one half of the primary winding.

In both the shunt-drive vibrator and the seriesdrive vibrator the current is alternately switched through each half of the transformer primary, and, as a result of these alternate pulses and the magnetic field they produce in transformer Tl, a stepped-up voltage is induced in the transformer secondary. The resulting secondary voltage is essentially square in waveform, and is applied to the full-wave rectifier circuit. In the circuits illustrated by the diagrams of typical nonsynchronous vibrator supplies, transformer T1 has a center-tapped secondary winding; each end terminal of the secondary is connected to a plate of the electron tube, V1. On alternate halfcycles of the secondary voltage, alternate diodes of the full-wave rectifier conduct and produce an output voltage across the load resistance. Since only one diode conducts at any instant of time, electrons flow

through the load resistance in pulses to produce a pulsating output voltage. The output of the rectifier circuit is connected to a suitable filter circuit to smooth out the dc for use in the load circuit; because a square-wave voltage is applied to the rectifier circuit, and because the frequency of vibrator switching is farily high (uaually 100 to 120 Hz), very little filtering is required to obtain a dc output voltage which is free from voltage transients and relatively free from ripple.

In practice, the nonsynchronous vibrator is normally constructed with a four-prong base, and the socket into which the vibrator is plugged is wired to accept either a shunt-drive or a series-drive vibrator; therefore, the two vibrator types may be used interchangeably in a large number of vibrator-type supplies.

**Circuit Operation. Both** supplies shown in the Nonsynchronous Vibrator Supplies illustration utilize a full-wave rectifier **circuit** to obtain high-voltage output. The discussion which follows is concerned primarily with the vibrator and its associated transformer, since the operation of a full-wave rectifier circuit has been described previously in this section of the handbook. Furthermore, the nonsynchronous vibrator-type power supply is not necessarily restricted to the use of a full-wave rectifier circuit and, in many instances, the rectifier circuit is likely to be a bridge or voltage-doubler circuit employing either electron-tube or semiconductor diodes as rectifiers.

Vibrator G1 in the circuit of part A is a shuntdrive vibrator; vibrator Cl in the circuit of part B is a series-drive vibrator. Transformer T1, in both circuits, is a special power transformer with a center-tapped primary and center-tapped secondary; however, if a bridge or voltage-doubler rectifier circuit is used instead of a full-wave rectifier shown, the transformer secondary need not be center-tapped. Electron tube V1 is a twin-diode rectifier, and may be either an indirectly heated cathode rectifier or a gas-filled, cold-cathode rectifier. Bypass capacitor Cl and r-f choke RFC1 serve as a filter to eliminate or reduce impulse electrical noise (or "hash"), originated by arcing vibrator contacts, from being radiated by the dc input leads and coupled into other circuits of the equipment. Resistors RI and R2 are connected across the interrupter contacts of the vibrator to reduce interference and sparking and also to increase the life of the vibrator contacts; the value of R1 and R2 is usually between 47 and 220 ohms, depending upon

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the dc input voltage and circuit design. Resistors R1 and R2 also help to reduce the peak amplitude of any transient voltages which might occur in the primary circuit because of vibrator switching action. Capacitor C2, commonly called the buffer capacitor, and occasionally referred to as the surge or timing capacitor, is connected across the transformer secondary to effectively absorb the high transient voltages produced by the inductive reactance when the primary current is interrupted by the opening of the vibrator contacts. Because of the magnitude of these voltages, it is necessary that the buffer capacitor have a rating in working volts of from 6 to 8 times the voltage delivered by the power supply. For example, for a supply which deliverrs 250 volts, the capacitor should be rated between 1500 and 2000 working volts. A resistor of approximately 5000 ohms is sometimes connected in series with the buffer capacitor to limit the secondary current in case the buffer capacitor becomes shorted. The value of a buffer capacitor depends upon the circuit design (transformer turns ratio and effective inductance, vibrator frequency, etc), but is usually between .001 and .047  $\mu$ f. Capacitors used in this application generally have a breakdown voltage of 1000 to 2000 volts. In some circuits a buffer capacitor is connected across the transformer primary. Another circuit variation uses two buffer capacitors of equal value; a capacitor is connected at each end of the secondary to ground or to the secondary center tap. Bypass capacitor C3 and r-f choke RFC2 form an additional filter to prevent noise (or "hash") from being coupled to other circuits through the high-voltage, dc output lead.

When dc input power is applied to the circuit, the driving **coil** of vibrator G1 is energized to start the reed vibrating at its own natural frequency. (The operation of shunt-drive and series-d"rive vibrators was described in considerable detail in previous paragraphs; therefore, a description of vibrator switching action will not be repeated here.)

# Failure Analysis.

**General.** A quick check to determine whether the vibrator is operating is to listen for the characteristic mechanical buzzing noise which is made by the vibrating action of the reed assembly; although the reed assembly is enclosed in a sealed can and is cushioned to deaden the sound, an audible indication can usually be detected. However, this simple check is not a

positive indication of correct vibrator operation; for example, the series-drive vibrator will often continue to operate even when there are discontinuities in the transformer primary circuit.

The most frequent trouble which develops in a vibrator-type supply is caused by a defective vibrator or a defective buffer capacitor. The power transformer and the rectifier-circuit components generally have a useful life which is comparable to the life of the components in a conventional power supply designed for ac input.

Although certain waveform measurements can be made with an oscilloscope to check for correct operation of the vibrator supply, this technique will not always immediately reveal troubles within the supply, since mechanical defects which may be of short duration sometimes occur only after the vibrator reaches a certain operating temperature.

An indication of vibrator operation can be quickly obtained by using an oscilloscope to observe the voltage waveform at the primary of the power transformer. If measurements are made at each end of the primary to chassis (ground), the peak-to-peak amplitude of the square wave will be approximately equal to twice the value of the dc input voltage; however, if the oscilloscope vertical input is connected across the entire primary winding, the peak-to-peak amplitude of the square wave will be approximately equal to four times the value of the dc input voltage. When the vibrator circuit is operating normally, a square wave will be observed with relatively smooth transition occurring after the contacts break and during the voltage reversal when another set of contacts make to produce the next half-cycle of the waveform. The flat portion of the square wave should be relatively smooth; if radical transients appear on the flat portion of the square wave, this is an indication of poor electrical contact, caused by chattering or bouncing of the contacts, and is a good reason to suspect that the vibrator is defective. Minor roughness, or "ripple", on the flat portion of the square wave is not usually sufficient cause to reject the vibrator, since this indication merely represents some small variation in contact resistance during the time the vibrator contacts are closed. The smoothness of the transition from one flat-topped portion of the square wave is controlled by the value of the buffer (timing) capacitor, the inductive reactance of the transformer, the natural frequency of the vibrator reed assembly, and the elapsed time between contact closures.

When the symptoms and checks indicate that the vibrator is definitely at fault, it is important that the replacement vibrator be the same, or an equivalent, **type**. There are many variations in vibrator terminal connections and operating characteristics; therefore, the replacement vibrator should be the same type as the original, or at least a vibrator which is recommended by the manufacturer as the correct replacement for the original.

No **Output. The** nonsynchronous vibrator supply consists of a vibrator and associated transformer, and a rectifier and falter circuit. Therefore, when checking the vibrator supply for a possible defect, tests must be made to determine whether the trouble **is** due to a defective vibrator and associated transformer, or to a defect within the rectifier circuit.

The dc input voltage should be checked to determine whether it is present and of the correct value.

The operation of the vibrator can be checked by an ac voltage measurement made at the secondary terminals of the transformer, or by use of an oscilloscope connected to the primary circuit to observe the switching-action waveform. If the vibrator and associated transformer are found to be functioning normally, as indicated by a secondary-voltage measurement or an oscilloscope check, it must be assumed that the trouble is in the rectifier circuit or the associated load. A check of the rectifier circuit can be made in accordance with the procedures outlined previously in this section for the applicable rectifier circuit; in the case of this particular vibrator-supply circuit, reference should be made to the Single-Phase Full-Wave rectifier circuit. When burned or pitted vibrator contacts stick together, a heavy current flows in the associated primary winding, and this current should be made with an ammeter to determine whether this current is within tolerance, or whether it is excessive. With the vibrator removed from its socket, continuity measurements of the transformer primary circuit may be made to determine whether the primary winding is open, shorted, or grounded.

A shorted buffer capacitor C2 can be detected by a higher than normal input current to the supply and a very low ac voltage at the secondary terminals of the transformer. The replacement buffer capacitor should be the same value as the original capacitor and of equal or greater voltage rating. A leaky or shorted falter capacitor Cl will also cause the input current to the supply to be above normal. As a general role, any time the vibrator is replaced the buffer capacitor should also be replaced.

The indirectly heated cathode rectifier, V1, is frequently subject to heater-to-cathode leakage, and, since the heater is normally at ground potential, this leakage will cause an abnormal load on the rectifier output; a complete short will result in no dc output from the supply. Also, a short in filter capacitor C3 or an open r-f choke RFC2 will result in no output from the **power** supply.

Low **Output**. A low-output condition in a nonsynchronous vibrator-type power supply usually results from a defective vibrator, a leaky buffer capacitor, low input voltage, or a defective component in the rectifier or falter circuit.

A voltage drop in the primary leads to the supply can result in low output; therefore, the input voltage should be checked at the transformer or vibrator terminals to determine whether the input voltage is present and of the correct value.

The ac secondary voltage may be measured at the transformer to determine whether it is approximately the value specified for normal operation of the sup ply. The test procedures described for the no-output condition and in previous paragraphs can be used to determine whether the vibrator is at fault. A defective vibrator with only one set of properly making contacts results in reduced output from the supply. A vibrator in which "frequency hunting" occurs may be detected by an uneven or irregular buzzing noise, which indicates that the armature is vibrating erratically and at frequencies other than its normal frequency of vibration. This unstable condition of the vibrator causes the stepped-up voltage induced in the secondary of the transformer to also be erratic, and the output voltage to be below its normal value. This trouble is usually caused by excessive load current, and is an indication of impending vibrator failure. Frequency hunting can also be caused by burned or pitted vibrator contacts which are sticking; this usually results in a higher than normal input current and reduced output from the supply. A check of the input current should be made with an ammeter to determine whether the current is within tolerance; also, an oscilloscope check of the waveform at the primary of the transformer should be made to determine whether the vibrator is faulty. Shorts, leakage, or excessive current drain in the filter circuit or in the high-voltage load circuit external to the supply will cause a heavy load on the vibrator contacts, and may

cause early failure of the vibrator. The output load current should be measured after installation of a replacement vibrator to determine whether the load current is within tolerance; if the load current is excessive, the replacement vibrator may be damaged unless the cause for the excessive load current is found and corrected.

Continuity measurements of the primary and secondary windings of transformer T1 should be made, since an open circuit in either of the windings will cause a reduction in output.

The rectifier, Vl, maybe weak and cause low output. The tube is usually an indirectly heated cathode type, such as a type 6X5, 6X4, or 12X4, or a gaseous rectifier, such as a type OZ4. In an emergency, when the vibrator is urgently needed and no replacement is available, the vibrator may be opened and the contacts burnished as an interim corrective measure. The indirectly heated cathode rectifier is frequently subject to heater-to-cathode leakage, and, since the heater is normally at ground potential, this leakage will cause a load on the rectifier output; a complete short will result in no dc output from the supply.

The power supply output current should be checked to make sure that it is within tolerance. A low-output condition due to a decrease in load resistance will cause an increase in load current; for example, excessive leakage in the capacitors of the output filter circuit will result in increased load current.

# SYNCHRONOUS VIBRATOR SUPPLY

#### Application.

The synchronous vibrator supply is commonly employed in many portable and mobile equipments where the primary power source is a storage battery. This supply produces a relatively high value of dc voltage at a moderate load current from a low-voltage dc source. The supply is commonly used to provide high voltage for the operation of small receivers, transmitters, and public-address systems, although in many equipments the transistorized de-to-de converter described previously in this section is used in lieu of the vibrator supply.

# Characteristics.

Input is low-voltage dc; output is high-voltage dc. Input voltage is usually 6, 12, or 24 volts; special vibrators for other input voltages are available. Typical vibrator operating frequency is between 60 and 250 Hz.

Output high-voltage dc is normally between 180 and 300 volts; load current is normally between 60 and 200 milliamperes.

Output circuit can be arranged to furnish negative or positive high voltage to the load.

Output dc requires filtering; ripple-voltage frequency is relatively high, and is determined by the vibrator frequency.

Synchronous vibrator is self-rectifying; electrontube or semiconductor rectifier circuit is not required.

Regulation is fair; output voltage regulation may be employed.

Vibrator must be shielded and leads faltered to prevent r-f radiation and interference to other circuits. **Circuit Analysis.** 

General. A synchronous vibrator supply converts direct current from a low-voltage power source into high-voltage dc that can be filtered for use as the plate and screen voltages in the operating equipment. A separate rectifier is not required with this circuit because rectification is accomplished by means of an extra set of contacts on the vibrator. The supply offers the advantages of light weight, small physical size, and good efficiency; its main disadvantages are the limitation in output current and tendency to produce interference to other circuits. Therefore, the vibrator must be well-filtered and shielded. Another disadvantage is that, although the vibrator itself is relatively inexpensive, its useful life is shorter than that of a dynamotor or of the transistors in a dc-todc converter. However, when this type of power supply is used within its rating, it will furnish reliable power for low-power communications and public address equipment.

**Synchronous Vibrator Typas.** A vibrator is an electromechanical mechanism, **sometimes** called an *interrupter*, which acts as a high-speed reversing switch to control (or interrupt) the current in each half of a tapped primary winding in a special stepup power **transformer**; in addition, the synchronous vibrator is equipped with two additional sets of contacts, operating in synchronism with the primary circuit interrupter contacts, to provide rectification of the transformer secondary voltage. The operation of a simple vibrator as a high-speed switching device and its rectifying action can be understood by reference to the accompanying illustration.



Fundamental Switching Circuit, Using Synchronous Vibrator, and Rasulting Output Waveform

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In this illustration, a vibrating reed is equipped with two sets of interrupter contacts arranged so that when one set of contacts is closed to complete one primary circuit, the other set of contacts is open to interrupt the other primary circuit. Two additional sets of contacts, called the rectifier contacts, operate in synchronism with the primary interrupter contacts. The action of the rectifier contacts is identical with the action of the primary contacts; that is, when one set of rectifier contacts is closed to complete one hrdf of the secondary circuit, the other set of rectifier contacts is open to interrupt the other half of the secondary circuit. Thus, as shown in part A of the illustration, when the upper sets of contacts are open, the lower sets of contacts are closed, and heavy current flows in the lower primary winding of the transformer. Also at this time, the lower half of the secondary, marked "A", is grounded through the lower set of vibrator contacts to complete the secondary circuit and produce a voltage at the output terminals. The polarities of the voltages produced across the primary and secondary windings of the transformer, which are so wound that no phase reversal occurs, are as indicated in part A of the illustration.

When the vibrating reed reverses its position, as shown in part B, the upper sets of contacts are closed, and heavy current flows in the upper primary winding of the transformer. Also at this time, the upper half of the secondary, marked "B", is grounded through the upper set of rectifier contacts to complete the secondary circuit and produce a voltage at the output terminals. The polarities of the voltages produced across the primary and secondary windings of the transformer are as indicated in part B of the illustration.

Assuming a rapid rate of primary switching, the voltage developed across the entire secondary is essentially a square **waveform**, as shown in part C. The voltage produced **in** each half of the secondary on alternate half-cycles, when combined, results in an output voltage which is essentially pulsating dc voltage. Small transients occur in the output voltage during the time the vibrator reed is transferring from one set of contacts to the other; however, these transients are easily removed by a **filter** circuit comected to the output of the vibrator supply.

A synchronous vibrator consists of five basic parts: a heavy frame, an electromagnetic driving coil and core or pole piece, a flexible reed and armature, two contacts attached to each side of the reed, and two (or more) stationary contacts mounted on each side of the reed and armature assembly. There are two basic electrical variations in synchronous vibrators; the first type is called a *shuntdrive* vibrator, and the second is called a *senesdrive* (or *separatednve*) vibrator. These names are derived from the manner in which the electromagnetic driving coil receives its excitation. The two types of synchronous vibrators are shown in the illustration below; part A shows the construction of a shunt-drive vibrator and its graphic symbol, and part B shows the construction of a series-drive vibrator and its graphic symbol.

The electromagnetic driving coil is mounted on one end of the frame, as shown in the illustration,



Synchronous Vibrator Types

and the reed is rigidly clamped in insulating spacers and fixed to the opposite end of the frame. The movable contacts are mounted on the sides of the reed. The stationary contacts are similarly clamped at the end of the frame, on each side of the reed. Electrical connections to the vibrator are also made at this point on the frame. The vibrator assembly is usually mounted within a sound-absorbing and cushioning material, such as foam or sponge rubber, which, in turn, is sealed within a metal can. The material placed around the vibrator reduces the amount of mechanical noise created by the vibrating reed, and the metal can acts as an r-f shield to reduce direct radiation of electrical noise. The connecting leads from the vibrator are brought out to metal prongs at the base of the can, and the complete unit is plugged into a special socket in the same manner that an electron tube is installed in a tube socket; the socket also grounds the can to the chassis to completely shield the vibrator. Since the vibrator may require replacement at intervals throughout the useful life of the power supply, the plug-in method of electrical connection insures convenient and easy replacement of a defective vibrator unit.

The shunt-drive vibrator, shown in part A, has one end of the driving-coil winding connected to the vibrating reed (normally connected to ground); the other end of the winding is connected to one of the insulated stationary primary contacts on the electromagnetic *pull* (or *power*) side of the reed. As shown in part A of the illustration, all contacts are open when the vibrator is at rest; however, when voltage is applied to the vibrator circuit through the power transformer primary, current flows through the driving coil and causes the reed armature to be pulled toward the pole piece. As this occurs, one set of primary contacts, called the *pull* or *power* contacts, close to shunt or short out the driving coil and also complete one half of the primary circuit. (An additional set of pull contacts, called the rectifier contacts, close to complete one half of the secondary circuit at this time.) The shunting action of the primary pull contacts causes the driving coil to lose its magnetic attraction for the reed armature and, as a result of the mechanical energy stored in the reed, causes the reed to swing back away from the pull contacts to interrupt the primary circuit and also break the secondary circuit. The inertia of the reed carries it back across the neutral (at rest) position to the other set of primary contacts, called the *inertia* 

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contacts, closing these contacts to complete the other half of the primary circuit. (An additional set of inertia contacts, called the *rectifier* contacts, close to complete the other half of the secondary circuit at this time.) While the inertia contacts are closed, current once again flows through the driving coil and causes a high magnetic attraction to be imparted to the reed armature. As the reed moves away from the inertia contacts, these contacts open to interrupt the primary circuit and also break the secondary circuit. The cycle is then repeated as the reed is carried across the neutral (at rest) position to close the primary pull contacts, thus shunting the driving coil, and also closing the rectifier pull contacts to complete the secondary circuit. It should be noted at this time that the peak voltage applied to the driving coil, during the time the inertia contacts are closed, is approximately twice the vahre of the normal dc input voltage to the supply; this is because the voltage induced by autotransformer action in the half of the primary winding which is connected to the stationary pull contact is in series with the dc input voltage.

By referring to the diagram of the shunt-drive vibrator, it will be seen that when the armature is in the neutral position (all contacts open), a complete series circuit exists from the negative side of the input source, through the driving coil and pull winding, to the positive side of the dc source. For a given value of current, as determined by the total resistance in the circuit, the portion of the input voltage that will be dropped across each of the two circuit elements will be in direct proportion to the resistance present in each element. Since the transformer primary winding offers only negligible resistance to the comparatively small and steady dc current which flows under the conditions stated, no appreciable voltage will be developed across the pull winding.

When the inertia contacts are closed, the series circuit through the driving coil and pull winding remains completed. The voltage existing across the pull winding and the voltage developed in the inertia winding have opposite polarities. Through the autotransformer action which takes place across the tapped primary, the rapidly changing magnetic field around the inertia winding induces a voltage in the pull winding; this voltage has the same polarity as that of the inertia winding. As a result, the voltage now present across the pull winding will be the difference between the induced voltage has the greater value, the polarity of the difference voltage will be the same **as** that of the induced voltage. Thus, not only is the counteracting effect of an opposing voltage neutralized, but the voltage in the inertia winding is effectively aided.

The series-drive (or separatedrive), vibrator, shown in part B, differs from the shuntdrive vibrator just described in that it has an extra pair of contacts which are normally closed when the vibrator is at rest. These contacts, called *starting* contacts, are in series with the ground connection to one end of the driving coil, while the other end of the driving coil is connected to the dc input voltage, either through a separate terminal in the vibrator base or to one of the stationary primary contacts. As shown in the illustration (part B), all pull and inertia contacts are open when the vibrator is at rest; however, when voltage is applied to the vibrator coil circuit, either through a stationary primary-pull contact or through the driving coil and causes the reed armature to be pulled toward the pole piece. The reed continues to move toward the pull contacts and, as the pull contacts close to complete one half of the primary and secondary circuits, the starting contacts are opened, causing the driving coil to lose its magnetic attraction for the reed armature. The reed now swings back away from the pull contacts, because the driving coil has lost its magnetic attraction for the reed armature, and the pull contacts open to interrupt the primary and secondary circuits. The inertia of the reed carries it back across the neutral (at rest) position to the inertia contacts, closing both the primary and rectifier contacts to complete the other half of the primary and secondary circuits. At the same time, the starting contacts close and current once again flows through the driving coil to produce a magnetic attraction for the reed armature. As the reed moves away from the inertia contacts, the primary and rectifier inertia contacts open to interrupt both circuits; at the same time the starting contacts open to interrupt the circuit to the driving coil. The cycle is then repeated as the reed is carried across the neutral (at rest) position to close the pull contacts and once again complete the primary and secondary circuits. It should be noted at this time that if the series-drive vibrator is comected in the circuit so that the driving coil receives voltage directly from the input source (through a separate contact in the vibrator base), the vibrator will continue to vibrate mechanically, even though the transformer primary center-tap and end leads are open.

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This will not occur with the shunt-drive vibrator, since the current to energize the driving coil must pass through one half of the primary winding.

The output polarity of a synchronous vibrator power supply depends upon the polarity of the dc input voltage. For this reason, means are often provided for reversing the dc output polarity. In practice, the synchronous vibrator is normally constructed with a special five-prong base, and the special sevenprong socket into which the vibrator is plugged accepts the vibrator in either of two positions. When installed in one position a positive output is obtained, and when installed in the other position a negative output is obtained. In other vibrator installations, a reversing switch (or flexible jumpers on a terminal board) is used to reverse the secondary-winding (or the primary-winding) comections to the power transformer.

**Circuit Oparation.** The accompanying illustration shows a typical synchronous vibrator supply using a shunt-drive vibrator. (Except for the manner in which connections are made to the driving coil, the operation of a seriesdrive vibrator is essentially the same.)



# Typical Synchronous Vibrator Supply Using a Shunt-Driva Vibrator

Vibrator **G1** is a shunt-drive vibrator; transformer T1 is a special power transformer with a centertapped primary and center-tapped secondary. Bypass capacitor Cl and r-f choke RFC1 serve as a falter to reduce or eliminate impulse electrical noise (or "hash"), originated by arcing vibrator contacts, from

being radiated by the dc input leads and coupled into other circuits of the equipment. Resistors RI and R2 and connected across the primary interrupter contacts of the vibrator to reduce interference and sparking and also to increase the life of the vibrator contacts; the value of R1 and R2 is usually between 47 and 220 ohms, depending upon the dc input voltage and circuit design. Resistors R1 and R2 also help to reduce the peak amplitude of any transient voltages which might occur in the primary circuit because of vibrator switching action. Capacitor C2, commonly called the *buffer* capacitor, and occasionally referred to as the surge or *timing* capacitor, is connected across the transformer secondary to effectively absorb the high transient voltages produced by the inductive reactance when the primary current is interrupted by the opening of the vibrator contacts. A resistor of approximately 5000 ohms is sometimes connected in series with the buffer capacitor to limit the secondary current in case the buffer capacitor becomes shorted. The value of a buffer capacitor depends upon the circuit design (transformer turns ratio and effective inductance, vibrator frequency, etc), but is usually between .001 and .047 µf. Capacitors used in this application generally have a breakdown voltage of from 1000 to 2000 volts. In some circuits a buffer capacitor is connected across the transformer primary. Another circuit variation, commonly used with the synchronous vibrator, uses two buffer capacitors of equal value; a capacitor is connected at each end of the secondary winding to ground (chassis). Bypass capacitor C3 and r-f choke RFC2 form an additional filter to prevent noise (or "hash") from being coupled to other circuits through the high-voltage, dc output lead.

When dc input power is applied to the circuit, the driving coil of vibrator Cl is energized to start the reed vibrating at its own natural frequency. (The operation of shunt-drive and seriesdrive vibrators was described in **considerable** detail in previous paragraphs; therefore, a description of vibrator switching action will not be repeated here.) The current is alternately switched through each half of the transformer primary, and, as a result of these alternate pulses and the magnetic field they **produce** in transformer Tl, a stepped-up voltage is induced in the transformer secondary. The resulting voltage in each half of the secondary is essentially square in waveform During the time that a square wave is being produced in the secondary winding, one set of rectifier contacts close in

the vibrator to connect the proper secondary winding to ground, and current flows through the load resistance. The rectifier contacts operate in synchronism with the primary interrupter contacts and alternately connect opposite ends of the secondary to ground; this action causes each half of the secondary to supply current to the load resistance on alternate halfcycles. Since only one half of the secondary is connected to the load circuit at any instant, electrons flow through the load resistance in pulses to produce a pulsating output voltage. (The action is similar to that of a full-wave rectifier circuit.) The output of the synchronous vibrator supply is connected to a suitable filter circuit to smooth out the dc for use in the load circuit. Because a square-wave voltage is switched in synchronism with the switching of the primary circuit, and because the frequency of the switching is fairly high (usually 100 to 120 Hz) very little filtering is required to obtain a dc output voltage which is free from voltage transients and relatively free from ripple.

## Failure Analysis.

**General.** A quick check to determine whether the vibrator is operating is to listen for the characteristic mechanical buzzing noise which is made by the vibrating action of the reed assembly; although the reed assembly is enclosed in a sealed can and is cushioned to deaden the sound, an audible indication can usually be detected. However, this simple check is not a positive indication of correct vibrator action, but merely indicates that mechanical action is taking place.

The most frequent trouble which develops in a vibrator-type supply is caused by a defective vibrator or a defective buffer capacitor(s). The power transformer and the associated circuit components generally have a useful life which is comparable to the life of the components in a conventional power supply designed for ac input.

Although certain waveform measurements can be made with an oscilloscope to check for correct operation of the vibrator supply, this technique will not always immediately reveal troubles within the supply, since mechanical defects which may be of short duration sometimes occur only after the vibrator reaches a certain operating temperature.

An indication of vibrator operation can be quickly obtained by using an oscilloscope to observe the volt-

age waveform at the primary of the power transformer. If measurements are made at each end of the primary to chassis (ground), the peak-to-peak amplitude of the square wave will be approximately equal to twice the value of the dc input voltage; however, if the oscilloscope vertical input is connected across the entire primary winding, the peak-to-peak amplitude of the square wave will be approximately equal to four times the value of the dc input voltage. When the vibrator circuit is operating normally, a square wave will be observed with relatively smooth transition occurring after the contacts break and during the voltage reversal when another set of contacts make to produce the next half-cycle of the waveform. The flat portion of the square wave should be relatively smooth; if radical transients appear on the flat portion of the square wave, this is an indication of poor electrical contact caused by chattering or bouncing of the contacts, and is a good reason to suspect that the vibrator is defective. Minor roughness, or "ripple", on the ilat **portion** of the square wave is not usually sufficient cause to reject the vibrator, since this indication merely represents some small variation in contact resistance during the time the vibrator contacts are closed. The smoothness of the transition from one flat-topped portion of the square wave, through the voltage reversal (contacts open), to the other voltage extreme of the square wave is controlled by the value of the buffer (timing) capacitor, the inductive reactance of the transformer, the natural frequency of the vibrator reed assembly, and the elapsed time between contact closures.

When the symptoms and checks indicate that the vibrator is definitely at fault, it is important that the replacement vibrator be the same, or an equivalent type. There are many variations in vibrator terminal connections and operating characteristics; therefore, the replacement vibrator should be the same type as the original, or at least a vibrator which is recommended by the manufacturer as the correct replacement for the original.

No **Output. The** synchronous vibrator supply consists of a vibrator, transformer, and associated filter circuit. It must be determined initially whether the vibrator is operating; if it is, tests must be made to determine whether the trouble is due to a defective vibrator or transformer, or to a defect located within the filter circuit.

The dc input voltage should be checked to determine whether it is present and of the correct value.

POWER SUPPLIES

The operation of the vibrator can be checked by an ac voltage measurement made at the secondary terminals of the transformer, or by use of an oscilloscope connected to the primary circuit **to** observe the switching-action waveform. If the vibrator and associated transformer are found to be functioning normally, as indicated by a secondary-voltage measurement or an oscilloscope check, it must be assumed that the trouble is in the filter circuit or the associated load.

If the vibrator-type power supply blows its dc input fuse each time the supply is energized, the vibrator should be removed from its socket, and, with a new fuse installed, the input power applied once again to determine whether a defective vibrator is the cause of excessive input current. When burned or pitted vibrator contacts stick together, a heavy current flows in the associated primary winding; this current is likely to blow the **fuse** because of the low dc resistance of the winding. A check of the input current should be made with an ammeter to determine whether this current is within tolerance, or whether it is excessive. With the vibrator removed from its socket, continuity measurements of the transformer primary circuit may be made to determine whether the primary winding is open, shorted, or grounded.

A shorted buffer capacitor C2 can be detected by a higher than normal input current to the supply and a very low ac voltage at the secondary terminals of the transformer. The replacement buffer capacitor should be the same value as the original capacitor and of equal or greater voltage rating. A leaky or shorted filter capacitor Cl will also cause the input current to the supply to be above normal. Also, a short in filter capacitor C3 or an open r-f choke RFC2 will result in no output from the power supply.

Low Output. A low-output condition in a synchronous vibrator-type power supply usually results from a defective vibrator, a leaky buffer capacitor, low input voltage, or a defective component in the falter circuit.

A voltage drop in the primary leads to the supply, due to the high resistance of a defective terminal or connector, can result in low output; therefore, the input voltage should be checked at the transformer or vibrator terminals to determine whether the input voltage is present and of the correct value.

The ac voltage may be measured between the center tap and each end of the secondary to deter-

mine whether the two measurements are equal and approximately the values specified for normal operation of the supply. The test procedures described for the no-output condition and in previous paragraphs can be used to determine whether the vibrator is at fault. A defective vibrator with only one set of prop erly making contacts results in reduced output from the supply and poor filtering. A vibrator in which "frequency hunting" occurs may be detected by an uneven or irregular buzzing noise; this trouble is usually caused by an excessive load current, and is an indication of impending vibrator failure. Frequency hunting can also be caused by burned or pitted vibrator contacts which are sticking; this usually results in a higher than normal input current and reduced output from the supply. A check of the input current should be made with an ammeter to determine whether the current is within tolerance; also, an oscilloscope check of the waveform at the primary of the transformer should be made to determine whether the vibrator is faulty; an additional check should also be made at the secondary center tap to determine whether the rectifier contacts are operating correctly. Shorts, leakage, or excessive current drain in the filter circuit or in the high-voltage load circuit external to the supply will cause a heavy load on the vibrator contacts, and may cause early failure of the vibrator. The output load current should be measured after installation of a replacement vibrator to determine whether the load current is within tolerance; if the load current is excessive, the replacement vibrator may be damaged unless the cause for the excessive load current is found and corrected.

In one circuit variation of a synchronous vibrator supply, buffer capacitor C2 is actually two capacitors; one capacitor is connected at each end of the transformer secondary to ground (chassis). If one of these buffer capacitors becomes shorted, the output voltage will be reduced accordingly.

Continuity measurements of the primary and secondary windings of transformer T1 should be made, since an open circuit in either of the windings will cause a reduction in output.

The power supply output current should be checked to make sure that it is within tolerance. A low-output condition due to a decrease in load resistance will cause an increase in load current; for example, excessive le\*age in the capacitors of the output falter circuit will result in increased load current.

# SECTION 3 VOLTAGE REGULATORS

# **PART 3-O. INTRODUCTION**

# **VOLTAGE REGULATION CIRCUITS**

# General.

Most electronic equipment can operate satisfactorily with a certain amount of variation in the supply voltage without affecting equipment performance. However, the operation of certain circuits is very sensitive to alight changes in supply voltage; thus, the use of a voltage regulator is required.

A voltage regulator is a device connected in the output of a supply to maintain the output voltage at a specified value. The regulator circuit reacts automatically within its design limits to compensate for any change in the output voltage, due either to a change in the supply voltage or to a change in the load current.

Voltage regulation can be provided by any of several means, depending upon the type of supply and the type of regulation required. The three basic classifications of voltage regulators discussed in this section are the electronic voltage regulatora, electromechanicrd voltage regulators, and electromagnetic voltage regulators. General discussions of these three classifications are given below.

# **ELECTRONIC REGULATORS**

#### General.

**The** electronic voltage regulator can be compared to a variable resistance,  $\mathbf{R}_{s}$ , in series (series type) or in parallel (shunt type) with a load resistance,  $\mathbf{R}_{L}$ , at the output of the power supply. The shunt type is commonly used where input voltage variations are small and the load remains relatively constant. The series is a more efficient regulator and is used in power supply applications where the load resistance and input voltage variations are large, or where a constant current rather than a constant voltage is the primary requirement.

#### Sarias Regulator.

A simple series type voltage regulator is shown in the illustration below.



Simple Series-Type Voltage-Ragtslator Circuit

Variable resistance  $\mathbf{R}_{s}$  and load resistance  $\mathbf{R}_{\perp}$  form a voltage divider. If the supply voltage increases, resistance  $\mathbf{R}_{s}$  is increased, again maintaining a constant voltage across the load. Similar variations in  $\mathbf{R}_{s}$  occur for any variations in the load. If the load resistance increases, with a decrease in load current,  $\mathbf{R}_{s}$  is made smaller; thus the voltage dropped across it is less, and the voltage across the load is maintained constant. With a decrease in the load resistance and a corresponding increase in the load current, the resistance of  $\mathbf{R}_{s}$  is made larger, causing a greater drop across it; again the constant voltage across the load is maintained.

Thus, it is seen that the voltage regulator is essentially a voltage-divider circuit, with the voltage drop across the series resistor absorbing any changes in the supply voltage or the load current, so that the voltage across the load is held constant. '

## Shunt-Type Regulator.

**The** shunt-type regulator, while one of the simplest regulators, is usually the least efficient. It may

be used to provide a regulated output where the load is relatively constant, the voltage low to medium, and the output current high. The shunt regulator utilizes the voltage-divider principle to obtain regulation of the output voltage.

The accompanying illustration shows the shunttype regulator reduced to its fundamental form. The fixed resistor,  $\mathbf{R}_{\mathbf{S}}$ , is in series with the parallel combination of the load resistance,  $\mathbf{R}_{\text{L}}$ , and the variable resistor,  $\mathbf{R}_{\mathbf{v}}$ , and forms a voltage divider across the input circuit.





All current that flows in the complete circuit passes through the series resistance,  $\mathbf{R}_{\mathbf{S}}$ . The magnitude of this current, and thus the value of the voltage drop across  $\mathbf{R}_{\mathbf{S}}$ , is controlled by variable resistance  $\mathbf{R}_v$ . The voltage across  $\mathbf{R}_{\mathbf{S}}$  is equal to the difference between the larger voltage of the dc source and the output voltage across load resistance  $\mathbf{R}_v$ . The difference voltage across  $\mathbf{R}_{\mathbf{S}}$  is varied by action of resistance  $\mathbf{R}_v$ , as required, to compensate for circuit changes and maintain the output voltage to the load, constant, at the desired value.

If the input voltage to the regulator circuit decreases, the voltage across load resistance  $R_{\perp}$  and the variable resistance,  $R_{\downarrow}$ , tends to decrease. To counteract this decrease, the resistance of  $R_v$  is increased; this reduces the total current flow through  $R_s$  and thereby the voltage drop across it. Thus, by decreasing the difference voltage of  $R_s$  to compensate for the decrease in the input voltage, the output voltage remains constant at its nominal value. Conversely, if the input voltage increases, the voltage across  $R_{\perp}$  and  $R_v$  tends to increase. To counteract the increase, the resistance of  $R_s$  and thus an increase in the voltage

drop across it. The increase in the difference voltage compensates for the increase in the input voltage, and again, the output voltage remains constant at the regulated vahre.

The shunt regulator must be capable of withstanding the entire output voltage of the dc source; however, it does not have to carry the full load current unless it is required to regulate from the no-load to the MI-10ad condition. Since series dropping resistor  $\mathbf{R}_{\mathbf{S}}$ , used with the shunt regulator, has relatively high power dissipation, the over-all efficiency of this type of regulator may be less than that of other types. One advantage of the shunt-type regulator is the inherent overload and short-circuit protection offered. This is because the series resistance,  $\mathbf{R}_{\mathbf{S}}$ , is between the dc source and the load; thus, a short circuit or overload merely decreases the output voltage from the regulator circuit. Note that under no-Ioad conditions, however, the shunt regulating device must dissipate the full output; therefore, the shunttype regulator is most often used in constant-load applications.

In the simple voltage-regulator circuit illustrated above, it is assumed that variable resistance  $R_v$  is varied manually to **keep** the voltage across the load constant. In an actual regulated power supply, the control action required to vary the series resistance, and, consequently, to produce a corresponding variable voltage drop, is completely automatic. This basic principle of voltage regulation can be accomplished by **use** of either a gas-tube regulator or by an electron tube regulator, both of which **are** described in this section of the handbook.

# Gas Tube Ragdator.

The gas-tube regulator is the simplest type of automatic voltage regulator, as illustrated below. A characteristic of the gas-tube is that within the operating range of the tube, as the voltage across the tube increases, the resistance of the tube decreases and the current through the tube therefore increases. The tube thus acts as a variable resistance. This increase in current through the tube causes the current through **Rs** to increase and the voltage drop across it to increase. Thus the voltage increase is developed across **Rs**, and the voltage drop across VI (and across **R**<sub>L</sub> which is in parallel with VI) returns to normal. A decrease in the input voltage operates in the reverse manner. A more detailed discussion of the gas-tube regulator is given later in this section.



Simple Voltaga Regulator Using Gas-Tuba

# Electron Tube Regulator.

An electron tube may also be considered as a variable resistance. Although the tube is conducting, its effective resistance is the plate-to-cathode voltage divided by the plate current. This calculated value of resistance is called the *de plate resistance*, or  $\mathbf{R_p}$ , of the tube. For a given applied plate voltage, the value of  $\mathbf{R_p}$  depends on the current through the tube, which, in turn, depends on the grid bias of the tube. Therefore, varying the grid bias applied to the tube controls the amount of current through the tube and causes the dc plate resistance,  $\mathbf{R_p}$ , to vary accordingly.

The accompanying illustration shows a triode used as a variable resistance in a simple voltage-regulator circuit.



# Simple Voltage-Regulator Circuit Using Trioda Elaatron Tuba

The dc plate resistance,  $\mathbf{R}_{n}$  of the series regulator tube, VI, is established by  $\mathbf{te}$  grid bias of the tube. The actual grid bias,  $\mathbf{e}_{g}$ , is the grid-to-cathode voltage; it equals  $\mathbf{E}_{2}$ -  $\mathbf{E}_{1}$ . Potentiometer R2 is placed across  $\mathbf{E}_{c}$  to provide a variable source of grid voltage. It is

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adjusted until the grid bias is the value that will allow VI to conduct the exact value of load current required to produce the desired value of voltage E, across the load resistance R<sub>L</sub>. Thus, adjustment of the bias alters the R<sub>p</sub> of VI to control the current through the tube, the voltage drop across the tube, and, therefore, the voltage across the load. Consider the condition where voltage E tries to increase, due either to an increase in the supply voltage, or to an increase in the load resistance. As E<sub>1</sub>goes more positive,  $\mathbf{e}_{\mathbf{g}}$  is made more negative ( $\mathbf{e}_{g} = \mathbf{E}_{2}$ - El), the conduction of the tube is reduced, the voltage drop across the tube is increased, and the voltage across the load is kept constant. Conversely, if voltage El tends to decrease, due either to a decrease in the supply voltage or to a decrease in the load resistance,  $\mathbf{e}_{\mathbf{g}}$ becomes less negative. This causes an increase in the conductivity of the tube, a decrease in its  $\mathbf{R}_{\mathbf{p}}$ , a corresponding decrease in the voltage drop across the tube; again the voltage across the load is maintained constant. In a properly designed regulator circuit, the voltage change which occurs across the series regulator tube is approximately equal to the voltage change which appears across the combined resistance of the regulator tube and the load; thus the voltage across the load remains constant.

Since the series regulator may not be sufficiently sensitive to small voltage changes, the output voltage of the simple voltage regulator may not be held absolutely constant, Therefore, where the regulation must be held to a small percentage, additional amplification must be used to increase the sensitivity of the regulator circuit.

# Regulated Power Supplies.

A complete regulated power supply consists of a power source, a transformer, rectifier, and filter circuit, and a dc regulator circuit. The dc regulator circuit may, in turn, be subdivided into four parts: series regulator electron tube(s), dc amplifier, voltagecomparison circuit, and reference-voltage circuit. The dc amplifier, the **voltage-comparison** circuit, and the reference-voltage circuit are considered as one complete functional circuit, generally referred to as the *regulator-amplifier* circuit of the electronic voltageregulated power supply. The design of the regulatoramplifier circuit depends primarily upon the degree of voltage regulation desired, and is relatively independent of the load current to be supplied. The majority of regulated power supplies which are used to provide plate and screen potentials for electronic equipments provide an output voltage of 150,250, or 300 volts, dc, with either a positive-output or a negative-output polarity. A typical electronic voltage-regulated power supply is shown in the accompanying block diagram.



Block Diagram of Electronic Voltage-Re@ated Power Supply

The series regulator tube, sometimes called the series control tube, used in the electronic voltage regulator is generally one of three possible circuit configurations: a **triode-connected** beam power tube, such as the type 6L6 or 6Y6; a low-mu, high-conduction triode tube, such as the type 6AS7 or 6080; or a beam power tube, such as the type 6L6, operated with a separate screen supply. The first two configurations mentioned are in common use. The third configuration has the disadvantage of requiring a separate power supply for the screen potential; for this reason its use is somewhat limited.

The triode-connected beam power tube used as a series regulator tube has a higher gain characteristic and provides a greater useful percentage of rated capacity over the other circuit configurations. Additionally, the **triode-connected** beam power tube requires a lower plate-voltage swing of the associated dc amplifier. The low-mu, high-conduction triode offers the advantage of a low dc plate resistance, and is frequently used where minimum power loss in the regulator circuit is an important consideration. The beam power tube operated with a separate screen supply has the advantages of a high gain **characteristic**, **a** low plate resistance, and a generally higher plate dissipation than the first two configurations mentioned above, but it does have a disadvantage in that a separate screen-voltage supply is required.

Regulator-amplifier circuits generally fall into one of several circuit configurations: single pentode, twin-triode cascode, twin-triode cascade, twin-triode and pentode with balanced input, and pentode and twin-triode with balanced output. For each of these regulator-amplifier circuit configurations, there are basic circuit variations which result. 'I'here is different reference-voltage polarities, different comection points for the amplifier plate-load resistor(s), various methods used to obtain voltage comparison, and in the case of a pentode dc amplifier, various connection points for the screen-dropping resistor. These and other typical circuit variations will be discussed in connection with the various types of electronic voltage-regulator circuits described in this section of the handbook.

# ELECTROMECHANICAL REGULATORS

## General.

Electromechanical regulators are automatic devices which are mechanical rather than electronic in nature and affect the power source itself; these regulators hold the output of a dc generator, ac generator (alternator), or other source of primary power at a predetermined value, or vary the output according to a predetermined plan. Because the power source always has some internal resistance or reactance, the output voltage changes when the load is varied; the amount of output-voltage variation depends upon the design of the dc or ac generator. In the case of an ac generator (alternator), the power factor of the load also influences the amount of variation. Under conditions of varying load, some form of voltage regulation is necessary to maintain the output voltage relatively constant; thus, the primary purpose of the regulator is to automatically compensate for any changes in output voltage.

Electromechanical voltage **regulators** control the generator or alternator output by controlling the current flow through the field (or exciter) winding of the machine. In most cases, control is accomplished by changing the resistance of the field circuit, which controls the field current, thus controlling the output voltage.

The operation of a typical regulation system can be briefly explained as follows: a drop in output voltage sensed by the regulator causes the regulator to increase the field current, and an increase in field current causes a corresponding increase in output voltage to compensate for the original drop in output voltage.

If the output voltage should rise, the regulator decreases the field current, causing a corresponding decrease in output voltage to compensate for the original rise in voltage. Thus, the regulator senses a change in output voltage and compensates for this change by altering the field current accordingly. The major difference between voltage-regulator systems, concerns the method used to control the field current.

The accompanying illustration shows a simplified circuit for controlling the output of a generator.



Simplified Circuit for Control of Generator Output

In this simplified circuit, variable resistor  $\mathbf{R}_{\mathbf{v}}$  is connected in series with the shunt field circuit of the generator. The purpose of this resistor is to control the current flow through the field winding and thus affect the strength of the magnetic flux developed by the field. (As the magnetic flux is either increased or decreased, the output voltage is either raised or lowered.) If the resistance of  $\mathbf{R}_{\mathbf{v}}$  is increased, less current flows through the shunt field, the magnetic flux developed by the field winding is decreased, and the voltage output developed across load resistance R<sub>1</sub> is decreased. Conversely, if the resistance of R is decreased, more current flows through the shunt field, the magnetic flux developed by the field winding is increased, and the voltage output developed across load resistance R<sub>1</sub> is increased. This principle of output-voltage control was briefly described in connection with rotating electromechanical power sources (generator and inverter), discussed in the Electromechanical Power Supplies.

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There are three common types of electromechanical regulators in general use: the vibrating-contact reg. ulator, the carbon-pile regulator, and the multitapped resistor regulator using a finger-type contactor or similar mechanical device. A brief description of the construction, operation, and application of the three types of voltage regulators is given in the following paragraphs.

## VibratingContact Ragulator.

The vibrating-contact regulator is commonly used to control the output of **battery-charging** generators in automotive, small-boat, and some aircraft applications where the speed of generator rotation varies with engine speed. The vibrating-contact regulator operates on the principle that an intermittent short circuit applied across a resistor which is in series with the shunt field winding causes the output voltage of the generator to fluctuate within narrow voltage limits; such a regulator will maintain an average value of output voltage which is independent of load changes. The accompanying illustration shows a simplified circuit for a vibrating-contact regulator.



Simplified Circuit for Vibrating-Contact Regulator

In this simplified circuit, a vibrating-contact relay, Kl, is used as a voltage regulator. Resistor RI is a voltage-dropping resistor in series with a solenoid, called the *potential coil*, which is part of relay K1. Resistor R2 is in series with the shunt field winding of the generator. The value of resistor R2 is chosen so that if the vibrating contacts of the relay were not in the circuit (held open), the value of output voltage would be approximately 60 percent of the desired value of output voltage when the generator is running

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at normal speed. If the contacts of the relay are held closed, resistor R2 is shorted by the contacts and maximum current flows through the shunt field winding; thus, the output voltage of the generator is maximum. Thus, it can be seen that in actual practice when the contacts open and close rapidly to intermittently short out resistor R2, the output voltage will reach a value which is greater than 60 percent of the desired value and less than the maximum value. For example, when the output voltage of the generator rises above a critical value, the voltage developed across the potential coil of the relay develops sufficient magnetic flux to attract the armature (or reed), and contacts 1 and 2 of the relay momentarily open to place resistor R2 in series with the shunt field winding. Thus, the current through the field is momentarily reduced and the output voltage of the generator is also momentarily reduced. Then, when the output voltage of the generator drops below a critical value (after the opening of contacts 1 and 2), the voltage developed across the potential coil decreases so that there is no longer sufficient magnetic flux to attract the armature, and contacts 1 and 2 of the relay close to short out resistor R2. Thus, the current through the field winding is maximum and the output voltage of the generator is momentarily increased.

The cycle described above is repeated when the potential coil again develops sufficient magnetic flux to attract the armature and open the contacts of the relay; the action described is rapid, and continues at a rate of approximately 60 to 240 times a second, so that an average voltage is maintained regardless of changes in load. If the load is increased and the output voltage tends to fall, the momentary voltage decrease is reflected by a decrease in voltage applied to the potential coil; thus, the armature vibrates more slowly, permitting an increased average current flow in the field winding. As a result, the output voltage is returned to the normal vahre. On the other hand, if the load is decreased and the output voltage tends to rise, the momentary voltage increase, when reflected to the potential coil, causes the armature to vibrate more rapidly and thus decrease the average current flow in the field winding. As a result, the output voltage is returned to the normal value.

In a practical application of this type of **regula**tion, means must be provided for adjusting the regulator to obtain the desired vrdue of output voltage. This is accomplished by one or both of the following methods: resistor **R1** or resistor R2 is made adjustable to change the value of resistance in the circuit, or the armature (reed) tension is made adjustable to change the amount of magnetic flux required to attract the armature to the solenoid.

The vibrating-contact regulator is sometimes used to control the output of a multiphase ac generator (alternator). When this is the case, the potential coil receives its operating current from a rectifier connected to one phase of the ac output, and the regulation action is the same as that described for the dc generator.

From the brief discussion given here, it can be seen that the vibrating-contact regulator acts as an automatic variable resistance in the field circuit of the generator, to hold the output voltage at a steady value for any change in load which occurs within the no-load to full-load operating conditions of the generator.

# Carbon-Pile Reguletor.

The carbon-pile regulator is commonly used to control the output of generators, alternators, and **inverters** used in automotive, shipboard, and aircraft applications. The carbon-pile regulator operates on the principle of a variable resistance (in the form of a stack of carbon disks) in series with the shunt field winding, to control the current through the field **and** thus the output voltage of the generator. The accompanying illustration shows a simplified *circuit* for a carbon-pile regulator.



Simplified Circuit for Carbon-Pile Regulator

In this simplified circuit, resistor RI is a voltagedropping resistor in series with a solenoid (electromagnet), called the *potential coil*; the resistor determines the current flow through the solenoid, and thus affects the magnetic flux developed by the solenoid. A resistance in the form of a stack of carbon disks, called the *pile*, is placed in series with the shunt field winding, to act as a variable resistance which can be controlled automatically. The resistance of the carbon pile depends upon the mechanical pressure applied to the pile by a spring which presses a movable iron armature against the end of the pile. The greater the mechanical pressure applied to compress the carbon disks, the smaller will be the resistance of the pile; if the mechanical pressure is decreased, the resistance of the pile increases. A change in mechanical pressure is accomplished by placement of the solenoid in proximity to the iron armature so that the magnetic flux developed by the solenoid acts to pull (attract) the iron armature away from the carbon pile. In a steady-state condition, the magnetic force attracting the iron armature is opposed by the mechanical force of the spring against the iron armature.

For example, assume that the output voltage of the generator rises above a critical vrdue. The voltage developed across the potential coif increases to develop a stronger magnetic field. Thus, the potential coil offers greater attraction to the iron armature and relieves the mechanical pressure exerted on the carbon disks; as a result, the resistance of the pile increases, the current through the shunt field winding decreases, and the output voltage returns to its former value. Conversely, when the output voltage fafls below a critical value, the voltage developed across the potential coil decreases, and the strength of the magnetic field developed by the potential coil also decreases. Thus, the potential coil offers less attraction to the iron armature, and the spring places a greater mechanical pressure on the carbon disks; as a result, the resistance of the pile decreases, the current through the shunt field winding increases, and the output voltage returns to its former vahre.

The operation of the carbon-pile regulator maybe briefly summarized as follows: when the output voltage rises, the spring pressure applied to the carbon pile decreases, causing an increase in pile resistance and a decrease in shunt field current; when the output voltage falls, the spring pressure applied to the carbon pile increases, causing decrease in pile resistance and an increase in shunt field current. The resultant decrease or increase in shunt field current lowers or raises the generator output, accordingly.

In a practical application of this type of regulator, means must be provided to adjust the regulator in order to obtain the desired value of output voltage. This is normally accomplished by an initial adjustment of the mechanical spring pressure (with resistor R1 set at mid-range), to obtain a steady-state condition whereby the magnetic force and the mechanical force are in balance; minor variations in voltage characteristics during normal operation are compensated for by an adjustment of resistor R1, which controls the current through the potential coil, to set the generator output voltage to the desired value.

The discussion in the preceding paragraphs has been primarily concerned with the operation of the carbon-pile regulator in conjunction with a dc generator; however, this type of regulator can be used equally well in an ac generating system. In practice, the output voltage of a multiphase ac generator (alternator) is controlled by varying the dc excitation current applied to the field winding of the machine. In this case, the carbon-pile regulator obtains a dc voltage for operation of the potential coil from a rectifier which is connected to one phase of the ac output, and the regulation action is the same as that described for the dc generator.

From the brief discussion given here, it can be seen that the carbon-pile regulator acts as an automatic variable resistance in the field circuit of a dc generator or in the field (exciter) circuit of an ac generator (alternator), to hold the output voltage at a specified value of voltage regardless of changes in load.

# Multitapped-Resistor Regulator.

The multitapped-resistor regulator is commonly used to control the output of generators, alternators, and inverters used in shipboard and shore-based applications. The multitapped-resistor regulator operates on the principle of a stepped, variable resistance connected in series with the generator field winding to control the current through the field, and thus the output of the generator. Basically, the multitappedresistor regulator consists of a single multitapped resistor (or several resistors connected in series), the terminals of which are either selected or shorted out automatically to obtain the desired resistance value. The name given to a particular regulator **configura**tion is derived from the manner in which the over-all series resistance is determined. For example, the

name *finger-type* regulator, *tilted-plate* regulator, or *rocking-disk* regulator, merely signifies the electromechanical method used to achieve physical contact and thus obtain a variable-resistance action within the regulating device. The accompanying illustration shows a simplified circuit for a typical multitappedresistor regulator.



### Simplified Circuit for Multitapped-Resistor Regulator

In this simplified circuit, resistor RI is a voltagedropping resistor in series with a solenoid, called the potential coil; the resistor determines the current flow through the solenoid, and thus affects the magnetic flux developed by the solenoid. Resistor R2 is the series resistor in the shunt-field circuit; R2 is a multitapped resistor, with the taps on the resistor connected to leaf springs (fingers) which are insulated from each other and are stacked one above the other. Electrical contacts are located at one end of each leaf spring. These contacts are arranged so that as mechanical pressure is increased at one end (lower end) of the stack, the number of electrical contacts that close is increased to short out sections of resistor R2. Thus, the greater the mechanical pressure applied to the stack of leaf springs, the smaller the effective series resistance of R2. If the mechanical pressure is decreased, the effective series resistance of R2 will be increased. A change in mechanical pressure is accomplished by placement of the solenoid in proximity to the iron armature, which is spring-loaded and linked mechanically through a lever system to the stack of leaf springs. In a steady-state condition, the magnetic force attracting the iron armature is opposed by the mechanical force of the armature **spring** pulling against the iron armature, and nly a few contacts are closed on the stack of leaf springs to provide some intermediate value of resistance.

When a change in generator output voltage occurs, the voltage developed across the potential coil changes; thus, the magnetic flux developed by the potential coil also changes. As a result, the mechanical force exerted on the stack of leaf spMgs is altered to change the number of contacts which are closed. This, in turn, changes the value of resistance (R2) in series with the shunt field winding and compensates for the change in output voltage. For example, assume that the output voltage of the generator rises above the critical value. The voltage developed across the potential coil increases to develop a stronger magnetic field. Thus, the potential coil offers greater attraction to the iron armature and decreases the mechanical pressure exerted on the stack of leaf spMgs (through the lever system); as a result, the value of resistance (R2) in series with the shunt field winding increases, the current through the shunt field winding decreases, and the output voltage returns to its former value. Conversely, when the output voltage falls below a critical value, the voltage developed across the potential coil decreases, and the strength of the magnetic field developed by the potential coil also decreases. Thus, the potential coil offers less attraction to the iron armature, and the armature spring places a greater mechanical pressure on the stack of leaf springs; as a result, the value of resistance (R2) decreases, the current through the shunt field winding increases, and the output voltage returns to its former value.

In a practical application of the muhitappedresistor regulator, regardless of the mechanical configuration employed to change the value of resistance, means must be provided for adjusting the regulator to the desired value of output voltage. This is normally accomplished by an initial adjustment of the mechanical spring tension which acts upon the armature and lever system (with resistor RI set at mid-range), to obtain a steady-state condition whereby the magnetic force and the mechanical force are in balance. Minor variations in voltage characteristics during normal operation are compensated for by an adjustment of resistor R1, which controls the current through the

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potential coil, to set the generator output voltage to the desired value.

The discussion in the preceding paragraphs has been primarily concerned with the operation of the multitapped-resistor regulator in conjunction with a dc generator; however, this type of regulator is frequently used in an ac generating system. When the multitapped-resistor regulator is used to control the output of a multiphase ac generator (alternator), the regulator obtains a dc voltage for operation of the potential coil from a rectifier connected to one phase of the ac output voltage, and the regulation action is the same as that described for the dc generator.

In conclusion, it can be seen that the multitappedresistor regulator acts as an automatic variable resistance in the field circuit of a dc generator or in the field (esciter) circuit of an ac generator (alternator), to hold the output voltage at a specified value of voltage regardless of changes in load.

From the brief descriptions of voltage regulators given in the preceding paragraphs, it can be seen that the vibrating-contact regulator, the carbon-pale regulator, and the multitapped-resistor regulator are merely controlled, automatic variable resistors. The detailed theory of operation and the construction of electromechanical regulators are covered in Navy publications on basic electricity (or in course materials for EM and AE ratings), and, therefore, will not be treated m this handbook. Only the basic principles will be discussed in this section of the handbook, as required, to provide a better understanding of the application and the failure analysis of the electromechanical regulators discussed.

## ELECTROMAGNETIC REGULATORS

#### General.

Electromagnetic regulators are automatic devices which are magnetic rather than electronic or mechanical in nature. These regulators are of two basic types: the induction regulator, which employs a variableinductor transformer, and the saturable-core-reactor regulator. An application of the induction regulator is its use iri an ac power regulator and distribution system wherein the unregulated power from the generating source is converted into a form required by the electronic systems or equipment at a particular facility or installation. The saturable-core-reactor regulator is used in such applications as the regulation of

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the ac voltage input to an electronic equipment or the equipment's power supply, or the regulation of the dc voltage output from the power supply in a given electronic equipment. Each of the two types of electromagnetic regulators will be discussed in the following paragraphs.

# Induction Regulator.

An example of an induction regulator used in an ac regulation and distribution system is illustrated in the accompanying block diagram. The input power (in this case, three-phase, 60 Hz ac) is applied through a transfer switch that automatically connects to an emergency power source when the normal source voltage between any phase and the neutral line falls below a predetermined level. When the normal source voltage returns to the proper level, the transfer switch again connects to the normal source.



# AC Regulation end Distribution System Using Induction Regulator

After passing through the transfer switch, the input power is applied through the system main circuit breaker to a three-phase reactor. The purpose of the three-phase reactor is to limit any short-circuit currents within the system to a preselected value of the regulator full-load current for any one phase. The reactor opposes large, rapid changes of current until a circuit breaker trips and opens the circuit; in this manner the system is protected and the effects of short circuits are localized. The output from the three-phase reactor is applied to the induction regulator and its associated control circuits. The regulated ac output is then fed through a circuit-breaker panel to the applicable equipment. Voltage and current meters monitor the load voltages and currents at the output of the induction regulator.

A simplified diagram of a three-phase induction regulator and its control circuits is given in the accompanying figure. The voltage-regulating component of this regulator is a variable-inductor transformer which is split into a rotating section and a stationary section. The rotating section, or rotor, for each phase is connected across the input line; hence, it is in parallel with the load ( $R_1$ ) for that phase. The stationary section, or stator, for each is connected in series with the input line; hence, it is **in** series with the load for that phase. A variation in the output (load) voltage is obtained by rotating the rotor inside the stator to change their flux linkage in both magnitude and direction. Thus, depending upon their relative angular positions, the rotor induces in the stator a voltage that either aids or opposes the line voltage. When the stator voltage aids the rotor voltage, the load voltage is greater than the input voltage. That is, the load voltage will be maximum when both the flux linkage between rotor and stator and the voltage induced in the stator are maximum, and the stator voltage is in phase with the rotor voltage. When the rotor is turned 180 degrees, both the flux linkage between rotor and stator and the voltage induced in the stator will again be maximum, but the voltage induced in the stator will be maximum, but the voltage induced in the stator will be out of phase with the rotor voltage. Hence, at this time the stator voltage opposes the rotor voltage and the load voltage is minimum. For relative angular positions of rotor and stator between the extremes noted, the load voltage likewise will be a value between the maximum and minimum extremes.



# Thraa-Phasa Induction **Regulator,** Simplified Diagram

The rotation of the rotor is accomplished by a reversible motor, which, in turn, is controlled by the action of two relays; this arrangement is illustrated schematically in the accompanying diagram. In a typical application of an induction regulator, a variable-inductor transformer and its associated control cir-

cuits are placed in each phase line of the distribution system. In this case, however, only the control circuits for phase 1 **will** be analyzed; the phase 2 and phase 3 control circuits are identical to those of phase 1, and thus will not be considered in this discussion.

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The output voltage of the selected-phase variableinductor transformer is sensed by a voltage-regulating relay, K1, which causes a motor-control relay, K2, to operate a reversible motor. The motor, BI, drives the

rotor of the applicable variable-inductor transformer in the direction necessary to compensate for the output-voltage variation.



Circuit for Phasa 1

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The sensing element of voltage-regulating relay K1 is an iron-core solenoid, which is suspended on a compensating spring. (The solenoid core and compensating spring are shown dotted in the illustration.) The solenoid current is made proportional to the output voltage by inserting limiting resistors R1 and R2 in series with the solenoid coil. In this manner, the solenoid current is maintained constant for a given voltage, and yet it can still change with the voltage to be regulated. A holding coil is wound in the opposite direction over the solenoid coil of K1; the holding coil, HC, is excited through the tapped sections of the K2 motor-control relay coils. The purpose of the holding coil is twofold: to modify the "pull" of the KI solenoid, and to hold the contacts of K1 closed until the control motor has caused the variableinductor transformer to correct the output voltage. When voltage-regulating relay K1 is in operation for a normal output voltage, the pull of its solenoid, which varies with the current through the coil, and the tension of the compensating spring are balanced against the weight of the solenoid core. The solenoid core operates a set of single-pole, double-throw contacts mounted on opposite ends of a pivoted beam and separated by equal distances from the stationary contacts; one normally open contact of the set closes when the output voltage increases, and the other normally open contact of the set closes when the output voltage decreases. This action causes voltageregulating relay K1 to operate motor-control relay K2, which, in turn, causes control motor B1 to turn and thus rotate the rotor of the variable-inductor transformer to correct the output voltage when this voltage is higher or lower than normal. In the accompanying diagram, the symbols (L) and (R) denote the components that produce the action necessary to "lower" and "raise" the output voltage, respectively.

Consider, now, the operation of the induction regulator when the output voltage of phase 1 increases above the level determined by the setting of voltagelevel potentiometer R2. To energize the control circuits, including the control motor, control-power switch S1 and motor-power switch S2 must be set to the "ON" position, and auto-manual switch S3 must be set to the "AUTO" position. Since the output voltage is higher than normal, the control motor must rotate the rotor of the variable-inductor transformer in the direction which will lower the voltage; this is accomplished in the manner described below. The

higher-than-normal output voltage of phase 1 causes an increase in the current through the solenoid coil of voltage-regulating relay K1. The stronger magnetic field resulting from the increased current exerts a greater pull and draws the solenoid core farther into the coil, thus relaxing the tension on the compensating spring. When the tension on this spring is relaxed sufficiently, the normally open contacts on the K1 (L) section of the voltage-regulating relay close. When this occurs, the "lower" (L) coil of motor-control relay K2 energizes and closes the normally open (N.O.) contacts on the K2 (L) section of this relay. Closing the K2 (L) contacts of the motor-control relay applies a voltage to the control motor, B 1, thus energizing the motor and causing it to turn to the "lower" direction. The control motor is mechanically coupled to the rotor of the phase 1 variable-inductor transformer. Therefore, when the motor turns, it also turns the rotor of the variable-inductor transformer in the direction which will cause less flux linkage between the rotor (primary) nad the stator (secondary). As a result, there will be less voltage induced in the stator; that is, since the stator, or output, voltage varies with the flux linkage between the rotor and the stator, reducing the flux linkage causes a reduction in the output voltage.

The control motor turns the rotor of the variableinductor transformer until the output voltage again becomes normal. As this point is approached, the current through the solenoid coil of voltage-regulating relay K1 decreases, since this current is proportional to the output voltage. Thus, at the predetermined level of output voltage, sensed by the current through the coil of Kl, the weaker magnetic field resulting from the decreased current exerts a lesser pull on the solenoid core of Kl, so that the weight of the core and the tension of the compensating spring are again in balance. When this occurs, the (K1(L) contacts of the voltage-regulating relay open, thereby causing the "lower" (L) coil of K2 to de-energize and, in turn, to open the K2(L) contacts of the motor-control relay, Opening the K2(L) contacts of the motor control relay removes the energizing voltage from control motor B1, and the motor stops turning. When the motor stops turning, the rotor of the variableinductor transformer also stops turning, and remains stationary at the normal output-voltage level until a further variation from normal occurs.

Assume that the output voltage of phase 1 now decreases below the predetermined level established by the setting of potentiometer R2. Since the output voltage is lower than normal, the control motor must turn the rotor of the variable-inductor transformer in the direction which will raise the voltage; this is accomplished in the manner described below. The lower-than-normal output voltage of phase 1 causes a decrease in the current through the solenoid coil of voltage-regulating relay K1. The weaker magnetic field resulting from the decreased current exerts a lesser pull on the solenoid core and thereby releases the core from the coil; the additional weight of the core now increases the tension on the compensating spring. When the solenoid core is released sufficiently, its weight causes the normally open contacts on the K1(R) section of the voltage-regulating relay to close. When this occurs, the "raise" (R) coil of motorcontrol relay K2 energizes and closes the normally open (N. O.) contacts on the K2(R) section of this relay. Closing the K2(R) contacts of the motorcontrol relay applies a voltage to the control motor, B1, thus energizing the motor and causing it to turn in the "raise" direction. The control motor is mechanically coupled to the rotor of the phase 1 variable-inductor transformer. Therefore, when the motor turns, it also turns the rotor of the variableinductor transformer in the direction which will cause more flux linkage between the rotor (primary) and the stator (secondary). As a result, there will be more voltage induced in the stator; that is, since the stator, or output, voltage varies with the flux linkage between the rotor and the stator, increasing the flux

The control motor turns the rotor of the variableirrductor transformer until the output voltage again becomes normal. As this point is approached, the current through the solenoid coil of voltage-regulating relay KI increases, since this current is proportional to the output voltage. Thus, at the predetermined level of output voltage, as sensed by the current through the coil of Kl, the stronger magnetic field resulting from the increased current exerts a greater pull on the solenoid core of Kl, so that the weight of the core and the tension of the compensating spring are again in balance. When this occurs, the K1(R)contacts of the voltage-regulating relay open, thereby causing the "raise" (R) coil of K2 to de-enregize and, in turn, to open the K2(R) contacts of the motorcontrol relay. Opening the K2(R) contacts of the

linkage causes an increase in the output voltage.

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motor-control relay removes the energizing voltage from control motor Bl, and the motor stops turning. When the motor stops turning, the rotor of the variable-inductor transformer also stops turning, and remains stationary at the normal output-voltage level until a further variation from normal occurs.

As previously explained, the voltage-regulating component of the induction regulator is the variableinductor transformer, and the voltage-sensing element is the voltage-regulating relay, K1. The setting of voltage-level potentiometer R2, which is in series with the coil of relay Kl, determines the desired normaloutput-voltage level by establishing the initial magnitude of current to determine the amount of pull on the solenoid core of K1 required to just balance the tension of the compensating spring. Thus, the current through the coil of K1 will remain constant as long as the output voltage is normal; when the output voltage changes (increases or decreases), the magnitude of the current will change proportionally and cause the induction regulator to compensate for the change in voltage. By establishing the magnitude of current through the holding coil of relay Kl, the setting of holding-effect potentiometer R3 determines the modified pull of the solenoid core and the length of time that the K1 contacts are held closed. In this manner, the holding coil helps the regulator control circuit to rapidly stop the rotor of the variable-inductor transformer when the output voltage reaches the predetermined normal level. The resistor-capacitor networks, R4-C1 and R5-C2, in the "lower" and "raise" sections, respectively, of motor-control relay K2 are used for arc suppression. Switches **S4(L)** and S5(R) are limiting switches in the "lower" and "raise" power-input lines to the control motor; these switches cut off power to the control motor and thereby prevent mechanical damage by preventing the motor from exceeding the desired maximum rotation in the respective directions.

# Saturable-Core-Reactor Regulator.

An example of a saturable-core-reactor regulator used in the regulation of an ac voltage is illustrated in the accompanying simplified diagram. In this application, the saturable-core reactor is used to regulate the ac voltage applied to an electronic equipment or to the power supply within an equipment. The degree of saturation of the reactor core is controlled by a two-stage dc amplifier, the bias of which is provided by a full-wave rectifier that receives its input voltage from the regulated output. Before the discussion of the saturable-core-reactor regulator is continued, a brief review of the operation of a saturable-core reactor will be presented.



A saturable-core reactor (or simply "saturable reactor") is a device consisting of one or more coils of wire, or windings, placed on an iron core which has special magnetic properties. Thus, a saturable reactor resembles a transformer in that it has windings on an iron core. However, it differs from a transformer in that the reactor operates in the region of core maturation during part of each ac input cycle. The basic operating principle of a saturable reactor is selfinduction, or that electromagnetic characteristic whereby a counter electromotive force is produced in a winding by a magnetic field which changes with the changes in current through the winding. The magnetic field concentrates in the iron core, and the flux density in the core varies directly with the current through the winding up to the point of core saturation. That is, when the current in a winding is increased from zero, the magnetic field surrounding each turn of the winding expands and cuts the other turns. As a result, a voltage is induced in the winding; this voltage opposes the applied voltage and tends to keep the current in the wire at a low value. While the current through the winding is less than the saturation current, the opposition (inductive reactance) of the winding is high and permits little current to flow. When the current is increased to the point where the core is saturated, the reactance becomes zero because the rate of change of flux density is zero. Thus, when the core becomes saturated, an increase in current in

the winding will no longer increase the flux density in the core; at this time, since the reactance is zero, ordy the dc resistance of the wire limits the current through the winding. When the current through the winding is decreased from a maximum value, the magnetic field begins to collapse and cut the turns of the winding. Again a voltage is induced in the coil. This voltage is opposite in direction to that which was induced by the rising current and the expanding magnetic field. Consequently, the voltage induced by the collapsing field tends to keep the current in the wire at a high value, even though it is decreasing toward zero.

A practical saturable reactor is different from an ordinary iron-core coil (just described) in that there are two windings associated with the core, as shown by the SRI component in the accompanying figure. One of the windings is called the control winding, and the other is called the load winding. The control winding is in the plate circuit of the output stage of the two-stage dc amplifier, and the load winding is in the input circuit of the ac voltage applied from the source. Thus, the variation in impedance of the input circuit, of which the saturable reactor load winding is a part, can be used to regulate voltages in a manner similar to the use of the variable resistance characteristic of an electron tube.

The components in the circuit of the accompanying figure may be grouped into three sections: input, rectification, and sensing-control. The input ac is applied across autotransformer Tl, which is in series with the load winding of saturable reactor SRI. Capacitor Cl, which is across the load winding, forms a tuned circuit with the load winding. The resonant frequency to which the parallel circuit of capacitor Cl and the load winding is tuned is slightly lower than the input line frequency; that is, it is on the inductive slope of the line frequency impedance curve. This resonant frequency is selected so that the input circuit always appears inductive, even when the input-circuit impedance, which includes autotransformer Tl. is shifted to increase or decrease the amount of apparent inductance in the circuit. Therefore, the input line voltage will be divided proportionally between autotransformer T1 and saturable reactor SRI, as determined by their impedance ratio.

The circuit operates in the manner described below. The unregulated ac input voltage, Ein, is applied across autotransformer T1 and the load winding of saturable reactor SR1 connected in series. The

autotransformer feeds power transformer T2, which is part of a conventional full-wave rectifier circuit. The dc output of the rectifier is developed across a voltage divider consisting of resistors RI, R2, and R3; the voltage divider provides the bias voltage for the input stage of the two-stage dc amplifier. The bias voltage, as selected by the setting of variable resistor R2, controls the conduction of the dc amplifiers, and thereby controls the resultant current through the control winding of saturable reactor SRI. Adjustment of autotransformer T1 and variable resistor R2, therefore, determines the value at which the ac output voltage, E<sub>aut</sub>, is regulated; any variations from the desired value of output voltage will be automatically compensated for by the action of the regulating circuit.

Assume, first, that there is an increase in the ac output voltage, E<sub>out</sub>. The increased ac voltage coupled to the secondary of power transformer T2 results in a greater dc voltage across the voltage divider in the output of the rectifier. Thus, a higher positive voltage is sensed at the wiper arm of variable resistor R2, thereby causing a decrease in the bias of the input dc amplifier. This decrease in bias causes an increase in the conduction of the input dc amplitler which, in turn develops a bias on the output dc amplifier and decreases the conduction of the output stage. As a result, the current through the control winding of saturable reactor SRI is reduced, thereby decreasing the degree of saturation of the reactor core. The saturable reactor now presents a greater impedance to the ac input voltage, thus permitting a greater voltage to be dropped across the reactor, and, consequently, lowering the voltage applied to autotransformer T1. With less voltage coupled from the autotransfonner, the output voltage decreases; thus, the ac output voltage is returned to the initially desired value.

Consider, now, the analysis of the circuit operation for the condition of a decrease in the ac output voltage,  $E_{out}$ . The decreased ac voltage coupled to the secondary of power transformer T2 results in a lower dc voltage across the voltage divider in the output of the rectifier. Thus, a lower positive voltage is sensed at the wiper arm of variable resistor R2, thereby causing an increase in the bias of the input dc amplifier. This increase in bias causes a decrease in the conduction of the input dc amplifier, which, in turn, decreases the bias on the output dc amplifier and increases the conduction of the output stage. As

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a result, the current through the control winding of saturable reactor SRI is increased, thereby increasing the degree of saturation of the reactor core. The saturable reactor now presents a lower impedance to the ac input voltage, thus permitting less voltage to be dropped across the reactor, and, consequently, raising the voltage applied to autotransformer T1. With a greater voltage coupled from the autotransformer, the output voltage increases; thus, the ac output voltage is returned to the vahse desired initially.

The circuit will also compensate for variations in the unregulated ac input voltage, Ein. For an increase in the input voltage, the circuit operation is the same as previously described for an increase in the output voltage; also, for a decrease in the input voltage, the circuit operation is the same as previously described for a decrease in the output voltage. Although the configuration of the circuitry of the dc amplifiers may vary in the regulator circuit, the purpose of this section is always to sense the variation in the voltage coupled to the rectifier, and then to control the degree of core saturation of the saturable reactor to compensate for the variation in voltage.

With slight modifications the **saturable-core** reactor regulator circuit just described can be used for regulating the dc voltage output of an equipment's power supply; such a modified circuit is illustrated in the accompanying figure. Note that the full-wave rectifier of the previous circuit is omitted, and the output of the power supply is used in its place to furnish the bias voltage for the input stage dc **amplifier**. Thus, the dc output voltage of the power supply controls the ac input voltage to the power supply, to provide regulation. Otherwise, the circuit function and operation in all respects are the same as described previously under this heading.



Regulation of DC Voltage with Saturable-Core Reactor

# PART 3-1. ELECTRONIC VOLTAGE REGULATORS

# GAS-TUBE REGULATOR

# Application.

The gas-tube regulator circuit is used in certain electronic equipment power supply circuits to obtain nearly constant output voltage(s).

# Characteristics.

Regr.dated output voltage to load is nearly constant; voltage drop across regulator tube remains nearly constant for considerable range of tube currents.

Voltage-divider principle employed, using fixed resistance and variable resistance (gaseous regulator tube) in series; regulated load is taken from across regulator tube.

Variation in basic circuit permits positive (plate and screen) or negative (bias) supply voltages to be regulated.

# Circuit Analysis.

**General. The** gas-tube regulator is one of the simplest types of voltage regulators. The regulator circuit consists of a fixed resistor in series with a cold-cathode, **gas-filled** regulator tube. The regulated output voltage is developed across the regulator tube; therefore, it is across this tube that the load is connected.

The regulator circuit develops a definite output voltage which is dependent upon the type of gas tube used in the circuit, provided that the variation in load current is within the operating range of the tube type employed. Gas tubes are rated according to the voltage appearing across the tube during normal operation and according to the maximum permissible current through the tube. Typical approximate operating voltage ratings for cold-cathode gas-filled tubes are 75, 90, 105, and 150 volts dc; typical maximum current ratings are 30,40, and 50 milliamperes.

Circuit Operation. In the accompanying circuit schematic, parts A and B illustrate a gas tube used in a basic voltage regulator circuit. Resistor  $\mathbf{R}_{s}$  is the series resistor; electron tube V1 is the gas-filled regulator tube. The circuit given in part A provides regulation of a positive input voltage, while the circuit given in part B provides regulation of a negative input voltage. Several regulator tubes may be connected in a series combination, if desired, to obtain a higher regulated output voltage. In the accompanying circuit schematic, parts C and D illustrate two regulator tubes in series. The circuit given in part C provides regulation of a positive input voltage, while the circuit given in part D provides regulation of a negative input voltage. Intermediate regulated voltages can be obtained from the junction of the regulator tubes in the latter two circuits (or from the junction of any series combination of regulator tubes), provided that the current drain of the associated load is kept low.





The cold-cathode **gas-filled** regulator tube is a two-electrode tube with a cathode and plate. The evacuated tube contains a small amount of gas, such as neon, which is sealed inside the tube. When sufficient voltage is applied to the tube, ionization of the gas molecules occurs and is responsible for the current passing through the tube during operation. If a gas tube is connected directly across a source of voltage which is high enough to ionize the gas, the current will immediately increase to such proportions that the tube may be darnaged. The use of a series resistance is essential, therefore, to limit the current through the tube.

There are two separate voltages to be considered in discussing the conditions under which the regulator tube will ionize and operate; these voltages are the breakdown, or firing, voltage and the operating voltage. The breakdown (or firing) voltage is that voltage at which the gas becomes ionized and begins to pass current. Mow this starting voltage the gas will not ionize and current will not pass through the tube. The operating voltage is the voltage at which the tube will remain ionized after having started. There is a considerable difference between the supply voltage and the voltage at which the regulator operates. This difference is compensated for by the series resistor,  $\mathbf{R_s}$ , which also serves to stabilize the load.

The value of the series resistor depends upon the maximum dc voltage input to the regulator circuit, the regulated dc output voltage, and the combined currents of the regulator tube and the load. The resistor is generally chosen to be of sufficient resistance to limit the current through the regulator tube to a value which is always less than the rated maximum operating current. The current through the regulator tube at the instant of ionization and before the load current has risen to its normal value may initially exceed the maximum value; however, as soon as the load

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current rises to its normal value, the regulator tube current drops to a value which is within operating limits because of the series resistance in the circuit.

The ionization of the gas within the tube changes, depending upon the applied voltage; as a result, the internal resistance of the regulator tube changes. When the applied voltage increases, the ionization of the gas increases to lower the tube resistance, and a larger current is passed. Conversely, when the applied voltage decreases, the ionization of the gas decreases to increase the tube resistance, and a smaller current is passed.

From the accompanying circuit schematic, note that the load current and the regulator tube current both pass through the series resistor,  $R_s$ . If the dc input voltage to the regulator circuit drops, the voltage across the regulator tube also drops momentarily, at which time the gas within the tube deionizes slightly and less current passes through the regulator tube. Therefore, the current through the series resistor decreases by the amount of the decrease in the regulator tube. Since the current through the series resistor decreases, the voltage drop across this resistor also decreases, and the output voltage delivered to the load increases to return to its original value. In a similar manner, if the input voltage to the regulator circuit increases, the voltage across the regulator circuit increases, the voltage across the regulator also increases momentarily, at which time the gas within the tube is further ionized and more current passes through the regulator tube. Thus, the current through the series resistor is increased. Since the current through the series resistor increases, the voltage drop across the resistor also increases, and the output voltage delivered to the load decreases to return to its original value. When the value of the series resistance is the correct value for the load to be regulated, the output voltage is held nearly constant by the action of the regulator tube. As just described, this action depends upon the fact that changes in the ionization of the gas within the tube varies the amount of current that the tube conducts.

The discussion above assumed that a change occurred in the dc input voltage applied to the regulator circuit. However, the regulator circuit also compensates for changes occurring in the load current. If the load requirement causes the current to increase, the voltage drop across the series resistor,  $R_s$ , will

immediately increase. As a result, the voltage across the regulator tube decreases momentarily, at which time the gas within the tube deionizes slightly and less current passes through the regulator tube. Therefore, the current through the series resistor decreases by the amount of the decrease in the regulator tube. Since the current through the series resistor decreases, the voltage drop across the resistor also decreases, and the output voltage delivered to the load increases, returning to its original value. In a similar manner, if the load current should decrease, the voltage drop across the series resistor will immediately decrease. As a result, the voltage across the regulator tube increases momentarily, at which time the gas within the tube is further ionized and more current passes through the regulator tube. Thus, the current through the series resistor is increased. Since the current through the series resistor increases, the voltage drop across the resistor also increases, and the output voltage delivered to the load decreases, returning to its original value. From the discussion given here, it is seen that the output voltage is held nearly constant by action of the regulator tube when changes occur in the load current.

The dc input voltage required to cause ionization of the regulator tube when the circuit is first energized is approximately 30 percent greater than the operating voltage specified for the regr.dater tube. The output voltage of the regulator circuit quickly drops to the operating value of the regulator tube as soon as the tube ionizes and begins to conduct, causing a voltage drop to appear across the series resistance, R<sub>s</sub>. In order to obtain stable operation, the regulator tube must be operated so that it is ionized at all times, and its operating current must fall within specified maximum and minimum current ratings. If, for some reason, the operating current exceeds the specified maximum current rating or if the voltage across the tube is excessive, the tube will become highly ionized, will lose its ability to regulate, and maybe permanently damaged. Conversely, if the operating current drops below the specified minimum current rating (approximately 5 milliamperes), the tube will become deionized and will no longer regulate the output. Also, if the voltage across the regulator tube drops below the specified operating voltage to a value which is approximately 70 percent of the breakdown (or firing) voltage, the tube will become deionized.
The value of the series resistor,  $\mathbf{R}_{\mathbf{s}}$ , can be approximated using the following formula:

where:

Ebb = unregulated dc input (supply voltage)

E.= regulated output voltage (to load)

**I**<sub>p</sub><sup>⁼</sup>regulator-tube current

 $I_{load} = load current$ 

When operation of the regulator tube is desired at the midpoint of its rated current range, the value of tube current used in the above formula is given as:

$$\mathbf{I_p} = \frac{(\max )^{-1} \min \mathbf{n}}{2}$$

where:

 $I_{max}$  = rated maximum tube current

 $I_{min}$  = rated minimum tube current

In applications where a regulated voltage greater than the voltage rating of a single regulator tube is required, several regulator tubes may be comected in series to obtain regulation of the desired voltage. Furthermore, if the current drain of the load is kept low, an intermediate regulated voltage can be obtained at the junction of any two regulator tubes of the series. Parts C and D of the accompanying circuit schematic illustrate two regulator tubes connected in series. This circuit configuration permits a lower regulated voltage (E<sub>o</sub>No. 2) to be taken from the dc supply. Note that the current through regulator tube V2 and the load current of the lower regulated voltage ( $E_0$  No. 2) must pass through regulator tube V1; therefore, the load current of the lower voltage must be relatively small to prevent the combined currents from exceeding the maximum current rating of regulator tube VI.

#### Faihrra Analysis.

**General.** Initially, some indication of the trouble associated with a gas-tube regulator circuit can be obtained by visual inspection to determine the presence of the characteristic glow from the ionized gas within the tube. When current through the tube is near its maximum rating, the tube is highly ionized; when the current is near its minimum rating, the tube is lightly ionized; therefore, the intensity of the gaseous discharge within the tube is not ionized, however, this does not necessarily mean that the tube is defective, since the same indication (lack of characteristic glow) may possibly occur if the series resistor ( $\mathbf{R}_{s}$ ) increases in

value, if the dc input voltage (Ebb) is below normal, or if the load current is excessive. It is therefore necessary to make dc voltage measurements at the input and output terminals of the voltage regulator circuit to determine whether the fault lies within the regulator circuit or whether it is external to the regulator circuit.

The value of the series resistor,  $\mathbf{R}_{s}$ , can be checked by ohmmeter measurements to determine whether any change in resistance has occurred. If the maximum current rating of the regulator tube is exceeded for a considerable length of time, the tube may be damaged and lose its regulation characteristics; therefore, the regulator tube itself can be suspected as a possible source of trouble. Furthermore, a regulator tube which is subjected to a very strong r-f field may be unable to regulate while the field is present, because the r-f field may ionize the gas within the tube independent of the normal dc conduction current.

# BREAKDOWN DIODE SHUNT-TYPE REGULATOR

#### Application.

The breakdown-diode shunt-type regulator is similar in operation to gas-tube regulators previously discussed in this section. It is used as a voltage regulator where the load is relatively constant. This circuit is frequently used in more complex regulator circuits as a reference-voltage source and as a preregulator in transistorized series-type regulators.

#### Characteristics.

Uses a breakdown, or Zener, diode as shunt regulating device.

Regulated output voltage to load is nearly constant, even though changes in input voltage or changes in load current occur.

Voltage-divider principle employed, using fixed resistance and breakdown diode in series; regulated load is taken from across diode.

Variation in basic circuit permits positive or negative voltages to be regulated.

#### Circuit Analysis.

**General. The** breakdown-diode regulator is the simplest form of shunt-type regulator. The regulator circuit consists of a **fixed** resistor in series with a breakdown, or Zener, diode. The regulated output voltage is developed across the diode; therefore, the

load is connected across the diode. The regulator circuit develops a definite output voltage which is dependent upon the characteristics of the particular breakdown diode; breakdown diodes are presently available with voltage ratings between 2 and 20 volts, in 5-, 10-, and 20-percent tolerances, and with power dissipation ratings as high as 50 watts.

The breakdown, or Zener, diode is a PN junction which has been modified during its manufacture to produce a specific breakdown voltage level; it operates with a relatively close voltage tolerance over a considerable range of reverse current. The breakdown diode is subject to a variation in resistance with a change in temperature of the diode; a circuit which compensates for this change in resistance is discussed later. The basic theory for the breakdown diode is discussed in the Introduction Section of Power Supplies in this handbook.

**Circuit Operation.** In the accompanying circuit schematics, parts A and B illustrate a breakdown diode used in a basic voltage-regulator circuit. The two parts are identical in configuration to the electron-tube, gaseous-type voltage regulators discussed earlier in this section of the handbook. Resistor R1 is the series resistor; semiconductor CR1 is a breakdown, or Zener, diode. The circuit in part A provides regulation of a positive input voltage, while the circuit in part B provides regulation of a negative input voltage.



Simple Breakdown-Diode Regulator Circuit

The design of the breakdown-diode regulator differs from that of the gas-tube regulator circuit in that no "firing", or "ionizing", potential must be considered when the value of the series resistance is determined. It is likely that both the input voltage and the load current for the regulator will be subject to variation; therefore, the breakdown-diode regulator is designed to operate within the extremes to be encountered. The series resistor, RI, needs only to stabilize the load; it compensates for any difference between the diode operating voltage and the unregulated input voltage. The value of the series resistor depends upon the combined currents of the breakdown diode and the load. The series resistor is generally chosen with the following factors in mind: the minimum value of input voltage (unregulated), the maximum value of load current, the minimum value of breakdown-diode current, and, knowing the diode characteristics, the value of the highest voltage to be developed across the breakdown diode and its parallel load resistance. Once the value of series resistor RI is determined, the maximum power dissipation in the diode can be arrived at by considering the maximum value of input voltage (unregulated), the minimum value of load current, and the minimum value of voltage developed across the diode (using the value of series resistance established for RI). In order to obtain stable operation, the breakdown diode must be operated so that its reverse current fails within its minimum and maximum ratings for the specified voltage. It is important to note that under no-load conditions, the breakdown diode must dissipate the full output power; therefore, this regulator circuit is never used in applications where a no-load condition is likely to exist. Instead, the breakdown-diode regulator is most often used in applications where the output voltage is fixed and the load current is relatively constant.

If the input voltage to the regulator circuit decreases, the voltage decrease appears across the breakdown diode, CR1, and immediately the current through the diode decreases; thus, the total current through series resistor R1 decreases, and the voltage drop across RI decreases proportionately, so that for ail practical purposes the output voltage across the load resistance (and breakdown diode) remains the same. Conversely, if the input voltage to the regulator circuit increases, the voltage increase appears across the breakdown diode, and immediately the current through the diode increases; thus, the total current

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# **ELECTRONIC CIRCUITS**

through series resistor RI increases, and the voltage drop across R1 increases proportionately, so that for all practical purposes the output voltage across the load resistance (and diode) remains the same.

If the current drawn by the load resistance decreases, the total current drawn from the input source does not change; instead, a corresponding increase in current through the breakdown diode occurs and the current drawn from the source remains constant, **so** that the output voltage across the load resistance (and diode) remains constant. Conversely, if the current drawn by the load resistance increases, the total current drawn from the input source does not change; instead, a corresponding decrease in current through the breakdown diode 'occurs and the current drawn from the source remains constant, so that the voltage across the load resistance (and diode) remains constant.

Environmental temperature extremes, as well as junction temperature changes, may result in variations of the internal impedance of the breakdown diode, which, in turn, results in changes of the output voltage. Thus, in practical circuits, provisions must be made to compensate for any variation of the impedance of the breakdown diode. The temperature coefficient of resistance of the breakdown diode is normally several times larger than the negative temperature coefficient of resistance of either the forward-biased or reverse-biased junction diode. To obtain a zero coefficient of resistance over a wide range of temperatures, one commonly used method of temperature compensation uses negativetemperature devices, such as forward-biased diodes or thermistors, in series with the breakdown diode. This method is illustrated in the accompanying diagram.



**Temparature-Compensated Voltage-Regulator Circuits** 

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The negative temperature coefficient of resistance of diodes CR2 and CR3 in series equals the positive temperature coefficient of resistance of the breakdown diode, CR1. By using forward biasing for diodes CR2 and CR3, the voltage drop across them will be kept to a minimum and, consequently, will have negligible effect on the value of the output voltage.

When the voltage-regulator circuit is temperaturecompensated as described above, the total resistance of CR1, CR2, and CR3, in series, remains constant over a wide range of temperatures; the end result is a constant voltage output, even though temperature, applied input voltage, or load current may change during operation.

Silicon breakdown diodes are generally used as the reference-voltage source in the more complex transistorized regulators because the breakdown voltage of a silicon breakdown diode is relatively constant over a wide range or reverse current.

#### Failure Analysis.

General. The shunt-type voltage-regulator circuit should never be operated without a load, since the no-load condition causes the breakdown diode to conduct heavily and it must dissipate power which is normally dissipated by the load resistance. In this case, if the maximum power dissipation or maximum reverse current rating of the breakdown diode is exceeded for any length of time, the diode may be damaged; thus, breakdown diode CR1 may be suspected as a possible source of trouble. Therefore, the load circuit should be carefully checked to determine that a load is presented to the regulator circuit at all times. It is also necessary to make dc voltage measurements at the input terminals of the regulator circuit to determine whether voltage is applied and whether it is within tolerance.

The operation of the shunt-type regulator is based upon the voltage-divider principle; therefore, voltage measurements made across the output terminals of the regulator circuit and across series resistor R1 (observing correct voltmeter polarity) are necessary to determine whether the output voltage is within tolerance and whether the drop across series resistor R1 is excessive. If the load is shorted, there will be no output from the regulator circuit, and the full output voltage will be measured across series resistor R1. Also, if series resistor RI should become open, there will be no output from the circuit, and the full output voltage will be measured across the resistor. The value of series resistor RI can be checked by ohmmeter measurement to determine whether any change in resistance has occurred; disconnect one terminal of RI from the circuit when making the measurement.

If breakdown diode CR1, or diode CR2 or CR3, should become open, the output voltage will be higher than normal; if breakdown diode CR1 should fail and become shorted, the voltage will be lower than normal, and diodes CR2 and CR2 will become overloaded. If diodes CR2 and CR3 should fail and become shorted, the output voltage will be subject to changes with temperature variations, since the temperature coefficient of resistance for the series diode combination will be changed. In general, if the output voltage is above normal, this is an indication that either an open circuit or an increase in impedance has occurred in the shunt elements (CR1, CR2, and CR3) or in the load of the regulator circuit. If the output voltage is below normal, this indicates that either series resistor R1 has increased in value, the input voltage is below normal, or the load current is excessive because of a decrease in load resistance (excessive leakage or shorted components in the load circuit).

# SHUNT TRANSISTOR REGULATOR

#### Application.

**The shunt** transistor regulator is used as a voltage regulator in electronic equipment where the load is farily constant and relatively light, and where it cannot be adequately handled by a simple breakdown diode regulator.

#### Characteristics.

Capable of handling a larger load than the diode regulator.

Is smaller, weighs less, and provides better reliability and performance than the electron tube regulator.

Efficiency is relatively low, because it uses a series-dropping resistor which dissipates considerable power.

Requires a reference voltage source for control purposes.

Transistor cannot be damaged by an external overload or short circuit. Circuit Analysis.

General. The shunt transistor regulator uses a series voltage-dropping resistor, whose voltage drop is controlled by the current drawn by a transistor connected across the output, to provide the desired change in output voltage. It is necessary that the series resistor be capable of carrying the load current and maximum transistor current; the transistor must be rated to handle the highest output voltage developed, since it is connected across the line. A source of reference voltage is required to bias the transistor. In addition, at no load, the transistor must be able to dissipate the full-load current. Under conditions of extreme load variation, the shunt regulator may be stabilized by adding a control amplifier stage. The shunt regulator is used to best advantage for fixedload, fixed-voltage applications.

**Circuit Operation. The** schematic diagram of a typical basic shunt transistor voltage regulator is shown in the accompanying illustration,



#### Shunt Transistor Regulator

Resistor R1 and Zener diode CR1 form a voltage divider across the supply which furnishes a fixed reference voltage across CR1. This is applied to the base of transistor Q1, biasing it at about midcurrent operating range. Meanwhile, the supply voltage is kept from dropping to the breakdown voltage of CR1 by resistor R1. Resistor R2 is the series voltage-dropping resistor through which the load voltage is regulated by the current drawn through shunt resistor Q1. The load resistance is represented by  $\mathbf{R_1}$ .

With a fixed load and normal voltage applied, breakdown diode CR1 holds the base bias of Q1 at a fixed value. Hence, transistor Q1 draws a fixed value of current from the line. The sum of the transistor

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current and the load current is such that the desired voltage drop is produced across R2. This voltage drop is the difference between the supply and the desired line voltage. With no change in load or transistor current drain, the difference voltage remains the same, and the line voltage remains constant. Assume for the instant that the load decreases slightly, reducing the difference voltage dropped across R2 and thereby increasing the line output voltage. This places a higher positive potential on the emitter of Ql, and, since the base is fixed by CR1, causes an increase of collector current through the transistor. The increase in collector current flowing through dropping resistor R2 produces a higher difference voltage and reduces the line output voltage back to normal.

When the load current increases again to the original value, a higher difference voltage is produced by the increased voltage drop across R2, and the line voltage is reduced below normal. The emitter-to-base voltage is now reduced below normal so that less forward bias is applied, and less collector current flows. The reduced voltage drop across R2, produced by the reduction of transistor current flow, reduces the difference voltage and the output line voltage increases back to normal value. To produce effective regulation, the change in transistor current must equal the change in load current. For large load changes power transistors are required.

# Faihrra Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional voltohmmeters. Be careful also to observe the proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No **Output**. If the load is short-circuited, Q1 is defective, or if R2 is open, no output voltage will be obtained. Check the input voltage. If the input voltage is normal, and there is no output voltage, measure the voltage drop across R2. If the output is shorted, full voltage will be indicated across R2 and the output will measure zero resistance with the power removed. Check the forward and reverse resistance of Q1. The reverse resistance low; if shorted, Q1 will indicate a low resistance in both directions.

**High Output Voltage.** If R1 is open or CR1 is defective, no reference voltage will be observed be-

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tween base and collector, transistor Q1 will be inoperative, and a higher than normal voltage will be obtained (with normal load). Make certain also that the resistance of R2 is not lowered by checking for proper value with an ohmmeter with the power off. It is also possible that Q1 is inoperative.

Low Output Voltage. If the resistance of R2 increases, a lower than normal output will be obtained. Check R2 for proper vrdue. If diode CR1 is defective or if R1 changes value, improper biasing of the Q1 base may cause higher than normal transistor current flow and create a continuous low output. Check RI for proper value. There is also a possibility that transistor Q1 may be defective and drawing a heavier than normal current.

**Erratic Operation. In the event that the output** voltage appears occasionally to vary below normal and does not become higher than normal, check the voltage across R2, since the range of the regulator may be exceeded on heavy loads.

# SERIES TRANSISTOR REGULATOR

### Application.

**The** series transistor regulator is used as a voltage regulator in electronic equipment where small-load variations permit the increased efficiency of this circuit to be used advantageously.

#### Characteristics.

Is smaller, weighs less, and provides better reliability and performance than the electron tube regulator.

Efficiency is higher than the shunt-type regulator. Requires a reference voltage source for control purposes.

Transistor must be capable of carrying the **full**-load current.

Transistor is subject to damage from a heavy overload or short circuit, except where protective provisions are included in the circuit.

# Circuit Analysis.

**General. The series** transistor voltage regulator uses a transistor connected in series with the load and voltage supply to act as a variable voltage-dropping resistor. The effective resistance of the transistor is controlled with respect to a reference voltage. When the regulated output voltage tends to charge, a correction voltage biases the transistor in the opposite direction. Thus, as the output voltage tends to rise, conduction through the transistor is reduced and the internal effective resistance tends to increase, automatically dropping the output voltage back to its original value. When the output voltage falls, conduction is increased, effectively reducing the transistor resistance and automatically increasing the output voltage back to normal. This action may be controlled by **am**plifiers to extend the range where large voltage swings are encountered, or to increase the sensitivity where only small ripple voltages are encountered, as desired.

**Circuit Operation. The** schematic diagram of a basic series voltage regulator is shown in the **accom**panying illustration.



Series Transistor Regulator

Capacitors Cl and C2 are conventional filter capacitors connected at the input and output, respectively. They tend to stabilize any small voltage variations and to eliminate any excess ripple present from the power supply. Breakdown diode CR1 and resistor R1 form a voltage divider across the supply, and are used to supply a constant base bias to regulator transistor Q1. Transistor Q1 is connected in series with the negative supply lead and operates as a voltagedropping resistor.

Under normal operating conditions, the base-toemitter bias is determined by breakdown diode CRI and resistor RI which form a voltage divider across the supply voltage. The base bias is fixed at a value which will produce the desired output voltage with a normal load. If the load is reduced, the output voltage will tend to rise. Since the base voltage is **fixed** by breakdown diode CR1, the emitter voltage will become more negative and reduce the effective baseemitter bias, causing the forward collector current to decrease. A decrease in collector current will increase the effective internal resistance of the transistor. Since the entire load current flows through the transistor, the voltage drop across Q1 will increase and reduce the output voltage back toward its original value.

Conversely, when the external load increases, the voltage across the load tends to drop. Thus, the emitter of Q1 will become less negative and the baseemitter forward bias will be increased, causing a heavier flow of forward current through Q1. The increased current flow through transistor Q1 will effectively reduce ther internal resistance of the transistor. Therefore, the load current flowing through the transistor will produce a smaller voltage drop across QI, and the output voltage will increase toward the supply voltage, returning the output voltage back to normal.

When the load current is too large for a single transistor, it is possible to parallel similar transistors to obtain sufficient current-carrying capacity. In some instances, because of production differences causing different characteristics, it may be necessary to compensate for the difference between high and low tolerance units by inserting small emitter resistors in the off-tolerance units. The object is to divide the current equally, so that each transistor carries an equal portion of the load, or to use matched pairs of transistors. Operation basically remains the same, with the current varying equally between transistors.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional ohmmeters. Be careful also to observe the properly polarity when checking continuity since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** If capacitors Cl or C2 are shorted, or if breakdown diode CR1 or transistor QI is open, there will be no output. Measure the input and output voltages. If there is no output voltage, check for a blown line fuse, and check capacitor Cl for a short. If input voltage exists but there is no output voltage, check capacitor C2 for a short. If C2 is satisfactory, measure the voltage across breakdown diode CR1. If the proper breakdown voltage is not obtained, check R1 for value and check breakdown diode CR1. If the

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proper breakdown voltage exists, and still no output is obtained, transistor Q1 may be at fault.

Low Output Voltage. If the line voltage is low, capacitors Cl and C2 are leaky; if improper bias exists, or if QI is defective, a constant low output voltage can be obtained. Check the line voltage, and check Cl and C2 for leakage and value. Check the base bias, and if normal, but the output voltage still remains low, transistor Q1 is probably defective. If the base bias is lower than normal, R1 may have changed in value, or breakdown diode CR1 may have changed its characteristics.

**High Output Voltage.** If the output voltage is constantly higher than normal, transistor Q1 is probably conducting heavier than normal because of a short, or because of high forward bias. Check diode CR1 and check the value of R1. If both parts are satisfactory, Q1 maybe defective.

# DC REGULATOR USING PENTODE AMPLIFIER

#### Application.

**The** dc regulator with series tube, pentode arm plifier, and gas tube voltage reference is used in certain electronic equipment power supply circuits to obtain nearly constant output voltage(s).

# Characteristics.

Regulated output voltage to load is nearly constant, even though changes in input voltage or changes in load current occur.

Voltage-divider principle employed, using variable resistance (electron tube) in series with load resistance; series electron tube may be a triode, a triode-connected pentode or a pentode with separate screen-voltage supply.

Uses pentode amplifier circuit to control series electron tube.

Uses gas gas-tube regulator circuit as reference-voltage source.

Variation in basic circuit permits positive (plate and screen) or negative (bias) supply voltages to be regulated.

# **Circuit Analysis.**

**General. The** dc regulator with triode series tube, single-pentode amplifier, and gas-tube voltage reference is capable of providing very stable outputvoltage regulation. The high amplification obtained from the pentode amplifier stage enables the circuit to have good sensitivity to small output-voltage variations. In this type of voltage regulator, regulation is accomplished by allowing the cathode-to-plate resistance of an electron tube, in series with the output of a power supply, to function as a variable resistance, and thus provide the voltage drop necessary to compensate for any change in output voltage. Voltage regulation which is better than 1 percent can be obtained with this type of regulator, depending upon circuit design.

Typical regulated output voltages obtained with this regulator circuit are 150, 250, and 300 volts, dc.

Circuit Operation. A typical voltage regulator circuit using a pentode amplifier and gas-tube voltage reference is illustrated in the accompanying circuit schematic. Electron tube VI is a twin triode used as the series regulator tube; V2 is a pentode used as a dc amplifier; V3 is a cold-cathode, gas-fdled regulator tube used to provide a reference voltage for operation of the regulator-amplifier circuit. Resistors R1 are voltagedropping resistors comected in series with regulator tube V3 across the input circuit. In addition, they function as a voltage divider to provide dc potential for the screen grid of V2. Cl, connected in parallel with regulator tube V3, is a bypass capacitor which provides a low-impedance path at the power supply ripple frequency (usually 120 Hz) to reduce the possibility of degeneration in the cathode circuit of V2.



Typical Voltage Regulator Circuit Using Pentode Amplifier and Gas-Tube Voltage Reference

The value of capacitor Cl is usually a compromise between a value which offers low impedance to the power supply ripple frequency (usually 120 Hz) and a value which is not so large as to affect normal operation of the regulator tube, V3. Capacitor C2 couples the full value of ripple voltage from the output of the regulator circuit; if C2 were not used, only a portion of the ripple voltage would be applied to the grid of V2, as determined by the voltage-divider action of R9, R10, and RI 1. The value of this capacitor is chosen to be just large enough to provide satisfactory ripple suppression. If the value of C2 is made too large, the response time of the regulator circuit to normal dc output-voltage variations will be affected; a value of from 0.01 to 0.1  $\mu$ f is typical in most regular-amplifier circuits. Capacitor C3 is connected across the output terminals to lower the output impedance of the regulator circuit; the value of this capacitor depends upon circuit design, but is usually  $2 \,\mu f$  or larger. Resistor R3 is the plate-load resistor for the pentode amplifier, V2. Resistors R4 and R5, in the grid circuits of V1, are parasitic oscillation suppressors; they are of equal value, generally between 270 and 1000 ohms. Resistors R6 and R7, in the cathode circuits of V1, are included for the purpose of equalizing the current flow in the parallel triode sections; these equalizing resistors are of equal value, generally between 10 and 47 ohms, depending upon circuit design. Resistor R8, in the control-grid circuit of V2, is a parastic oscillation suppressor. Resistors R9, R1O, and R11 form a voltage divider across the output of the regulator circuit, and are in parallel with the resistance of the load; resistor R1O is adjustable, and is used to set the output voltage to the desired value the circuit is to maintain.

Electron tubes V1 and V2 are indirectly heated, cathode-type tubes; V1 normally has a high heaterto-cathode voltage rating, while V2 has a heater-tocathode voltage rating which is typical for receivingtype tubes. Because of the heater-to-cathode breakdown voltage limitations imposed by the tubes themselves, it is usually necessary to isolate the filament circuits from each other and to supply the filament (heater) voltages from independent sources.

When the unregulated voltage,  $E_{in}$  is first applied to the input of the regulator circuit, voltage is applied to regulator tube V3 through resistors R1 and R2, in series; V3 ionizes and begins to conduct, thus establishing a reference voltage at the cathode of V2. The action which occurs is the same as that previously described under *Gas-Tube Regulator Circuit*, in this section of the handbook. The voltage divider formed by resistors R1 and R2 establishes the voltage applied to the screen grid of V2. Regardless of the value of dc voltage applied to the input of the regulator circuit, the voltage at the cathode of V2 will be held constant by the action of V3 for use as a reference voltage; however, the voltage at the screen grid of V2 is subject to change if the input voltage changes. This screen-circuit configuration increases the gain of the amplifier stage and also the regulator-amplifier sensitivity to either input or output voltage changes.

As previously mentioned, this regulator circuit is based upon the voltage-driver principle of using a variable resistance in the form of electron tube V1 in series with the load resistance. The regulated output voltage, E<sub>out</sub>, appears across the voltage divider formed by series resistors R9, R1O, and R11, which are connected across the output of the regulator circuit and in parallel with the load. The total resistance of these series in parallel with the load resistance constitutes one part of the resistance in the series voltage-divider arrangement, the other part being the variable cathode-to-plate resistance of VI. When the cathode-to-plate resistance of V1 is controlled to vary the voltage drop across VI, the output voltage developed across the load can be regulated and maintained at a constant value.

The voltage appearing at the plate of V2 is dropped from the input to the regulator circuit through plate-load resistor R3 and is applied to the control grids of V1. The amount of current through R3 and the resulting value of voltage at the plate of V2 are control grid of V2. The voltage applied to the grid of V2 is obtained from the voltage divider circuit composed of R9, R1O, and R1 1; the exact value of voltage applied to the grid of V2 is determined by the setting of R1O. Since the potential at the cathode of V2 is maintained at a constant positive value by the action of regulator tube V3, adjustable resistor R1O is set to the point where the bias applied to the grid of V2 permits a predetermined value of current to be drawn by V2. When V2 is conducting, the voltage drop through plate-load resistor R3 develops a voltage at the grid of V1 which is less than either the plate or cathode voltage of VI; the difference in voltage between the cathode of VI and the plate of V2 is the operating bias for V1. Thuse, the setting of resistor R1O determines the current through V2, establishes the bias for V1, and initially determines the effective

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internal resistance of VI to obtain the desired output voltage from the regulator circuit.

Assume that the regulated output voltage,  $E_{out}$ , attempts to increase, either because of an increase in the input voltage to the regulator circuit or because of a decrease in the load requirement. Through the voltage-divider action of resistors R9, R1 O, and R11, a slightly higher positive voltage now appears across R1O and R11. This results in an increase in the positive voltage applied to the grid of V2 and a corresponding decrease in the bias voltage between the cathode and grid. (The cathode voltage of V2 remains constant because of the action of regulator tube V3.) As a result of the decreased bias, V2 now conducts more current, and this additional current flow through plate-load resistor R3 results in a greater voltage drop across R3; thus, the voltage at the plate of V2 decreases and causes the difference in voltage between the cathode of V1 and the plate of V2 to increase. This difference in voltage between the cathode of V1 and the plate of V2 is the operating bias for VI; thus, as a result of this voltage increase, the effective internal resistance of VI increases. When the internal resistance of V1 increases, less load current flows through V1, the voltage drop across V1 increases, and the output voltage of the regulator circuit decreases to its original value.

An action similar to that just described occurs when the regulated output voltage,  $E_{out}$ , attempts to decrease. Through the voltagedivider action of resistors R9, R1O, and R11, the bias voltage between the cathode and grid of V2 is increased, since a slightly low positive potential now exists across RIO and R11. As a result of the increased bias, V2 now conducts less current, and this decreased current flow through plate-load resistor R3 causes a smaller voltage drop to occur across R3; thus, the voltage at the plate of V2 increases and causes the difference in voltage between the cathode of V1 and the plate of V2 to decrease. The difference in voltage between the cathode of V1 and the plate of V2 is the operating bias for V1; thus, as a result of this voltage decrease, the effective internal resistance of VI decreases. When the internal resistance of V1 decreases, more load current flows through VI, the voltage drop across V1 decreases, and the output voltage of the regulator circuit increases to its original value.

The actions described in the preceding paragraphs are practically instantaneous; consequently, the output voltage  $(E_{out})$  remains practically constant.

Since all of the load current must pass through the series regulator tube, V1, the tube(s) must be capable of passing considerable current. In some circuit applications where the load current requirements exceed the capabilities of a single tube, two or more identical tubes are connected in parallel (as the sections of twin-triode V1 have been paralleled) in order to obtain suitable regulation characteristics and current-handling capability.

The output of the regulator circuit is coupled to the grid of the pentode amplifier tube, V2, through coupling capacitor C2. Any ripple component present in the output voltage is amplified by V2, and, since the circuit is basically a negative feedback circuit, the ripple component is suppressed. Also, since the screen-grid voltage for V2 is obtained from the unregulated input voltage to the regulator circuit, the sensitivity of the amplifier to voltage changes is increased. As a result, the regulator circuit is sensitive to any voltage changes and is very effective in removing any fundamental ripple-frequency component which is present in the unregulated voltage supplied to the input of the regulator circuit.

'As previously mentioned in this section, there are several circuit variations possible for the series regulator tube, V1. These variations in the series regulator circuit include the use of a triode (a twintriode is shown in the schematic), a triode-connected pentode, and a pentode with separate screen-voltage supply.

Also, there are several variations in the regulatoramplifier circuit which are commonly employed in electronic regulators (see illustrations below). For example, the screen-grid voltage for V2 may be obtained through a separate screen dropping resistor from the cathode circuit of VI, or from a tap placed on the bleeder resistance formed by resistors R9, R1O, and R11; this is shown in part A of the accompanying illustration. In some cases the screen voltage is obtained from a separate regulated-voltage source. Another circuit variation, shown in part B of the illustration, is connection of the plate-load resistor, R3, to the cathode circuit of VI instead of to the plate circuit as shown in part A; in this case, the voltage drop developed across plate-load resistor R3 is the bias voltage for V1. Still another circuit variation is obtaining the voltage for operation of regulator tube V3 through a separate series resistor comected to the cathode circuit of V1. An alternative method of obtaining the reference voltage (See part C) is to ground

the cathode of V2 and connect resistor RI 1 of the voltage divider (R9, R1O, and R1 1) to a regulated negative-voltage source. Although there are many minor variations in the regulator-amplifier circuit configuration, the function of the regulator circuit remains the same, that is, to supply a regulated output voltage to the load which is independent of variations in input voltage or changes in load current.



# Typical Regulator-Amplifier Circuits (Showing Variations)

#### Failure Analysis.

**General.** The voltage-regulator circuit includes several parts which are rather critical and directly affect operation of the regulator circuit. For this reason, resistors R9, R1O, and R1 1, and perhaps resistors R1 and R2, are normally close-tolerance resistors with good temperature stability characteristics. If for any reason these particular resistors should change in value, the operation of the circuit will be impaired.

Since the regulator circuit attemps to hold the output voltage constant, it is usually good partice to determine whether the load current is within tolerance between suspecting trouble within the regulator circuit. A load-current measurement may be made by inserting a milliammeter (having a suitable range) in series with the output of the regulator circuit. Also, a voltage measurement should be made at the input to the regulator circuit to determine whether the unregulated voltage output from the power supply (and filter circuit) is within tolerance.

No **Output**. In the voltage-regulator circuit using a pentode amplifier, the no-output condition is likely to be limited to one of the following possible causes: the lack of filament voltage applied to series regulator tube VI, the lack of applied dc voltage (from the associated power supply and filter circuit), or a shorted load circuit (including output capacitor C3).

A visual check of the glass-envelope seriesregulator tube, V1, should be made to determine whether the filament(s) is lit; if the filament is not lit, it may be open or the filament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of voltage at the tube socket should be determined by measurement.

The dc voltage applied to the regulator circuit should be measured at the input (plate of VI) to determine whether it is present and of the correct value, since the lack of input voltage from the associated power supply and filter circuit causes a lack of output voltage.

With the dc voltage removed from the input to the circuit, resistance measurements can be made across the load (resistors R9, R1O, and R11) to determine whether the load circuit, including capacitor C3, is shorted. (The resistance measured across the load circuit will normally measure something less than the total value of series resistors R9, R1O, and R11, depending upon the load circuit design.)

**High Output.** The high-output condition is usually caused by a descrease in operating bias for the series regulator tube, V1, which, in turn, causes the tube to decrease its internal resistance and permits the regulator output voltage to rise above normal; therefore, any defects in the regulator-amplifier circuit which can cause a decrease in the operating bias for V1 are to be suspected. Voltage measurements should be

made at the socket of VI to determine whether bias (cathode-to-grid) is present.

A visual check of the gas-fried regulator tube, V3, which provides a reference voltage for operation of the regulator-amplifier circuit, should be made to determine whether the tube is conducting. A voltage measurement made between the plate and cathode of V3 will determine whether sufficient voltage is present at the tube to cause conduction. If the voltage is above normal, the tube may be defective. If the voltage measure across V3 is below normal, it is likely that resistor R1 or R2 is open or possibly the dc amplifier tube, V2, is not conducting.

A visual check of amplifier tube V2 should be made to determine whether the filament is lit; if the filament is not lit, it may be open or the filament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of voltage at the tube socket should be determined by measurement. The grid voltage applied to V2 should be measured to determine whether the tube is improperly biased and causing the operating bias on VI to decrease. Assuming that V3 is conducting normally to provide a reference voltage, if the voltage at the grid of V2 is below normal, is is possible that resistors R9 and RI 1 have changed in value or that resistor R1O is not set properly; however, if no voltage is present at the grid of V2, the tube will be biased to cutoff and V1 will conduct heavily as a result of decreased operating bias. In this case, it is likely that either resistor R9 or a portion of R1O (connected to R9) is open. If amplifier tube V2 has low emission, the voltage drop across plate-load resistor R3 will be below normal.

Low Output. The low-output condition is usually caused by an increase in operating bias for the series regulator tube, VI, which, in turn, causes the tube to increase its internal resistance and permits the regulator output voltage to fall below normal; therefore? any defects in the regulator-amplifier circuit which can cause an increase in the operating bias for V1 are to be suspected.

In the twin-triode series regulator tube, trouble in one section (such as low cathode emission or an open tube element) will cause a reduction in output. Voltage measurements should be made at the socket of VI to determine whether the bias (cathode-to-grid) is excessive. The equalizing resistors, R6 and R7, in the cathode circuits of V1 should be measured to determine that neither one is open, that they have not increased in value, and that they are of equal resistance.

A visual check of the gas-filled regulator tube, V3, which provide a reference voltage for operation of the regulator-amplifier circuit, should be made to determine that the tube is conducting. A voltage measurement made between the plate and cathode of V3 will determine whether sufficient voltage is present at the tube to cause conduction. If the voltage measured across V3 is below normal, or if no voltage is present, it is likely that capacitor Cl is either leaky or shorted.

The grid voltage applied to V2 should be measured to determine whether the tube is improperly biased, thus causing the operating bias on V1 to increase. Assuming that V3 is conducting normally to provide a reference voltage, if the voltage at the grid of V2 is above normal, it is possible that resistors R9 and R11 have changed in value or that resistor R1O is not set properly; however, if a high voltage is present at the grid of V2, the tube will conduct heavily and V1 will conduct less as a result of an increase in operating bias. In this case, it is likely that coupling capacitor C2 is either leaky or shorted, or that either resistor R11 or a portion of R1O (connected to RI 1) is open. Also, if amplifier tube V2 is shorted and conducting heavily, the voltage drop across plate-load resistor R3 will be excessive; therefore, a known good tube should be substituted and operation of the circuit observed to determine whether V2 is the cause of trouble.

As mentioned previously, excessive load current can cause the output voltage to be low, especially if the load current exceeds the maximum rating of series regulator tube V1 (resulting in excessive voltage drop across V1) or if the load current exceeds the rating of the power supply (resulting in a decrease in the applied voltage). For these reasons, output capacitor C3 should be checked to determine whether it is satisfactory; a leaky output capacitor could result in reduced output voltage, although the regulatoramplifier circuit may be functioning normally but is unable to compensate for the decrease in output.

**Poor Regulation Characteristics.** Voltage instability, slow response, etc, are frequently caused by weak or unbalanced triode sections in series regulator V1, unbalanced cathode resistors R6 and R7, or a defective dc amplifier, V2. The gain of the dc amplifier stage is determined primarily by amplifier tube V2 and its applied voltages; therefore, the condition of V2 and its applied voltages are important factors

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governing satisfactory operation of the regulator circuit.

# DC REGULATOR USING **CASCODE** TWIN-TRIODE AMPLIFIER

# Application.

**The** dc regulator using a cascode twin-triode amplifier is employed in certain electronic equipment power supply circuits to obtain nearly constant output voltage (or voltages) despite variations of input voltage or output load current.

# Characteristics.

Same characteristics as DC Regulator using Pentode Amplifier, except that it uses a cascode twintriode dc amplifier **circuit** to control series electron tube.

# Circuit Analysis.

**Genaral. The** dc regulator with twin-triode series regulator tube, cascode twin-triode amplifier, and gas-filled voltage reference tube is capable of providing very stable output voltage regulation. The term "regulation" as used here means the maintenance of a nearly constant output voltage despite changes in the input voltage or the load current. The variation in output voltage that normally result from component aging, changes in operational environment, etc, are usually considered in the design of the circuit, and are compensated for by using close-tolerance (on the order of 1,2, or 5 percent) components whose values do no deviate from the nominal by more than the strict limits specified.

In this type of voltage regulator, regulation is accomplished by allowing the cathode-to-plate conduction resistance of an electron tube, in series with the output of a power supply, to function as a variable resistance, and thus provide the voltage drop necessary to compensate for any change in output voltage. That is, the change in output voltage is compared and amplified in the regulator-amplifier circuit, and applied as a bias voltage to the grid of the series regulator tube, thereby varying the conduction resistance of this tube. The varying conduction resistance of the regulator tube, in turn, varies and load current drawn by the series curcuit and the voltage drop across the regulator tube; in so doing, the regulator tube absorbs the change in the output voltage. Voltage regulation of approximately 1 percent can be obtained with this type of electronic dc regulator, depending on the circuit design.

Circuit Operation. A typical dc regulator using a cascode twin-triode amplifier is illustrated in the accompanying circuit schematic. Electron tube VI is a parallel-connected twin-triode used as the series regulator tube. (In applications where the current drain exceeds the current-handling capability of a single series regulator tube, two or more tubes of the same type may be comected in parallel.) Electron tube V2 is another twin-triode, in a cascode dc amplifier circuit conf@rration, used as the regulator amplifier. Tube V3 is a cold-cathode, gas filled tube used to provide a reference voltage for operation of the regulator-amplifier circuit. The use of the gas-filled regulator tube in this application is satisfactory as a reliable reference since there are no excessive currents in that branch of the circuit. Electron tubes V1 and V2 are indirectly heated, cathode-type tubes; V1 normally has a high heater-to-cathode voltage rating, while V2 has a heater-to-cathode voltage rating which is typical for receiving-type tubes. Because of the heater-to-cathode breakdown voltage limitations imposed by the tubes themselves, it is usually necessary to isolate the filament circuits from each other and to supply the filament (heater) voltages from independent sources.

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DC Regulator Using CaseOde Twin-Triode Amplifier

Resistors R2 and R3, in the grid circuits of VI, are parasitic oscillation suppressors; they are of equal value general between 170 and 1000 ohms. Resistors R4 and R5, in the cathode circuits of Vl, are included for the purpose of equalizing the current flow in the parallel-connected triode sections; these resistors are of equal value, generally between 10 and 47 ohms, depending upon the circuit design. Resistor R6, connected in series with reference tube V3 across the output circuit, serves to apply the full output voltage of the regulator to V3, to ensure a satisfactory striking potential and also to act as a current-limiting resistor once the tube is ionized. Capacitor Cl, connected in parallel with reference tube V3, is a bypass capacitor which provides a low-impedance path at the power supply ripple frequency (usually 120 Hz), to reduce the possibility of degeneration in the cathode circuit of V2B. The value of capacitor Cl is usually a

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compromise between a value which offers low impedance to the power supply ripple frequency and a value wihch is not so large as to affect the normal op eration of the reference tube, V3.

Capacitor C2 couples the full value of ripple voltage from the output of the regulator circuit to the grid of V2B; if capacitor C2 were not used, only a portion of the ripple voltage would be applied to the grid of V2B, as determined by the voltagedivider action of R8, R9, R1O, and R11. The value of capacitor C2 is chosen so that it is just large enough to provide satisfactory ripple suppression. If the value of capacitor C2 were made too large, the response time of the regulator circuit to normal dc outputvoltage variations would be affected; a value of from 0.01 to 0.1 microfarad is typical in most regulatoramplifier circuits. Resistor R7 helps provide the bias for the grid of V2B. Capacitor C3 is connected across the output terminals to lower the output inpedance of the regulator circuit; the value of this capacitor depends upon the circuit design, but is usually 2 microfarads or larger. Resistors R8, R9, R1O, and RI 1 form a voltage divider across the output of the regulator circuit, and are in parallel with the resistance of the load. Resistor R9 is adjustable, and is used to set the output voltage to the desired value the circuit is to maintain.

The cascode configuration of the regulatoramplifier circuit, V2, can be considered as two triode amplifiers directly connected (direct-coupled) in series. The action of this circuit is similar to that of a pentode in that the isolating effect of the screen grid on the plate is achieved, with the advantage that no screen-voltage supply is required. The cascode circuit is used when the gain required of the regulator amplifier is too high for a single triode, yet it is desired to eliminate the pentode screen-voltage supply. However, in order to achieve adequate gain, the cascode circuit requires a large-value plate-load resistor (Rl, on the order of 2.2 megohms); this requirement causes the frequency response to be reduced and thereby restricts the area of application of the circuit. The effects of poor frequency response can be reduced somewhat by using a relatively large-value capacitor (about 5 microfarads) for C3.

The two triodes of the cascode twin-triode regulator amplifier are the input section, which is the right-hand tube (V2B), and the output section, which is the left-hand tube (V2A). The cathode of the input section is at a positive potential determined by the

reference tube, V3. The control grid of the input section is returned through resistor R7 to the voltage divider at the junction of resistors R1O and R11. The voltage at the top of resistor RI 1 is slightly less positive than the operating potential of reference tube V3; hence, a bias voltage of only a few volts is established between the control grid and cathode of V2B. The plate of V2B is directly connected to the cathode of the output section, V2A. The control grid of V2A is returned to the wiper arm of voltage-divider variable resistor R9. The value of grid voltage of V2A, as determined by the setting of resistor R9, is of sufficient amplitude to keep the grid of V2A from drawing appreciable grid current. The operating range of V2A plate. voltage, which is applied though plate-load resistor R1, is far enough above its grid voltage so that the current in the grid circuit of V2A does not approach or become comparable with the V2A plate current.

As previously mentioned, the operation of this regulator circuit is based upon the voltagedivider principle of using a variable resistance in the form of electron tube V1 irr series with the load resistance. The regulated output voltage,  $E_{out}$ , appears across the voltage divider formed by resistors R8, R9, R1O, and R11, which are connected across the output of the regulator circuit and in parallel with the load. The total resistance of these voltagedivider resistors in parallel with the load resistance constitutes one part of the resistance in the regulator series voltage-divider arrangement, which includes the variable cathode-toplate resistance of series regulator tube V1. The currents which pass through the parallel branches (voltage-divider resistors and load resistance) combine, 'and this total current passes through series regulator tube V1. When the cathode-to-plate reference of VI is controlled to vary the voltage drop across this tube, the output voltage developed across the load can be regulated and maintained at a constant value.

In order to understand how the dc regulator circuit operates under varying-load conditions, it is necessary to examine first the static voltage distribution under normal-load conditions. The cathode of series regulator tube V1 is held positive with respect to ground by the output voltage,  $E_{out}$ , while the grid is held somewhat less positive by the action of regulator amplifier V2. The difference between these two voltages is the bias voltage for V1, which now is at the proper value for series regulator tube VI to have the required amount of cathode-to-plate **resistance** to produce the correct output voltage. The output voltage is applied to reference tube V3 through resistor R6, causing V3 to ionize and conduct, thereby establishing a reference voltage at the cathode of the input section, V2B, of the cascode regulator amplifier. (The action of the **gas-filled** reference tube, V3, is the same as that previously described under Gas-Tube Regulator Circuit earlier in this section of the handbook.) Regardless of the value of dc voltage applied to the input,  $E_m$  of the regulator circuit, the voltage at the cathode of V2B will be held constant (by the action of V3) for use as reference voltage.

Cascode regulator-amplifier V2, in essence a twostage series-connected triode amplifier, uses the plate load of the input section, V2B, as the cathode input impedance of the output section, V2A. Thus, the signal to the input stage is applied between the control grid and ground, while the output of this same stage is the input to the direct-coupled output stage, and is applied between the cathode and ground. The output section, V2A, has a fixed voltage on its grid, obtained from adjustable resistor R9 of the voltagedivider network. This bias voltage limits the excursions of the V2A cathode voltage, which is also the plate voltage of the input section, V2B. The grid voltage for V2B is obtained from voltage-divider resistors R11 and R7. Since the potential at the cathode of V2B is maintained at a constant positive value by the action of reference tube V3, the bias on V2B and V2A, as determined by voltagedivider resistors RI l/R7 and R9, respectively, is such that it permits a predetermined value of current to be drawn by V2. The plate voltage of V2A is obtained from the unregulated input, Ein, and applied to the regulator amplifier through plate-load resistor R1. When V2 is conducting, the voltage drop across plate-load resistor R1 develops a voltage at the plate of V2A; this voltage is coupled to the grids of V1. The voltage at the grids of VI is less than the voltage at the cathodes of V1; hence, the operating bias for VI is established. The setting of resistor R9, therefore, determines the current through V2A, establishes the bias for Vl, and initially determines the effective internal resistance of V1 to obtain the desired output voltage,  $E_{out}$ , from the regulator circuit.

Assume, now, that the regulated output voltage, Eout> attemPts to Increase, either because of an in. crease in the input voltage,  $E_{in}$ , to the regulator circuit or because of a decrease in the load requirement. Through the voltage-divider action of resistors R8, R9, R1O, and R11, a slightly higher positive voltage now appears across resistors R9, R1O, and RI 1. This results in an increase in the positive voltage applied to the grids of V2A and V2B, and a corresponding decrease in the bias voltage of this stape. (The cathode voltage of V2B remains constant because of the action of reference tube V3.) As a result of the decreased bias, V2 now conducts more current, and this additional current flow through plate-load resistor R1 results in a greater voltage drop across resistor R1. Thus the voltage at the plate of V2A, which is coupled to the grids of V1, decreases and causes the difference in voltage between the grids and cathodes of V1 to increase. This difference in voltage between the grids and cathodes of V1 is the operating bias for VI. As a result of the bias voltage increase, the effective internal resistance of V1 increases. When the internal resistance of V1 increases, less load current flows through VI, the voltage drop across VI increases, and the output voltage, E<sub>out</sub>, of the regulator circuit decreases to its original value.

An action similar to that just described occurs when the regulated output voltage, E<sub>out</sub>, attempts to decrease. Through the voltage-divider action of resistors R8, R9, R1O, and R11, the bias voltage on the grids of V2A and V2B is increased, since a slightly lower positive potential now exists across resistors R9, R10, and R11. As a result of the increased bias, V2 now conducts less current, and this decreased current flow through plate-load resistor R 1 causes a smaller voltage drop to occur across resistor R1. Thus, the voltage at the plate of V2A (and the grids of Vl) increases and causes the difference in voltage between the grids and cathodes of V1 to decrease. This difference in voltage between the grids and cathodes of V1 is the operating bias for V1. As a result of the bias voltage decrease, the effective internal resistance of V1 decreases. When the internal resistance of V1 decreases, more load current flows through VI, the voltage drop across V1 decreases, and the output voltage of the regulator circuit increases to its original value.

The actions described in the preceding paragraphs are practically instantaneous; consequently, the output voltage,  $E_{out}$ , remains practicably constant. Since aff of the load current must pass through the series control tube, V1, the tube must be capable of passing considerable current. In some circuit applications where the load current requirements exceed the capabilities of a single tube, two or more identical tubes are connected in **paralled** (as the sections of twin-triode V1 have been paralleled) in order to obtain suitable regulation characteristics and current handling capability.

The output of the regulator circuit is coupled to the grid of the input section of the cascode twintriode regulator-amplifier tube, V2B, through coupling capacitor C2. Any ripple component present in the output voltage is amplified in the regulator amplifier, and, since the circuit is basically a negative-feedback circuit, the ripple component is suppressed. As a result, the regulator circuit is sensitive to any voltage changes and is very effective in removing any fundamental ripple-frequency component which is present in the regulated voltage output. Although there are many minor variations in the regulator-amplifier circuit configuration, the function of the regulator circuit remains the same, that is, to supply a regulated output voltage to the load which is independent of variations in input voltage or changes in load current.

#### Failure Analysis.

Due to the similarity between the DC Regulator using Cascode Twin-Triode Amplifier and the DC Regulator using a Pentode Amplifier (discussed previously in this section), the discussion will not be repeated here. The only differences in Failure Analysis will be some component reference designations. For example: in the Pentode Amplifier, voltage divider resistors R9, R10, and R11 are close tolerance resistors; in this circuit, the c1ow tolerance voltage divider resistors are R6, R8, R9, RIO, and R11. The procedures are presented so that, with slight differences, they are applicable to both circuits.

# DC REGULATOR USING CASCADE TWIN-T RI ODE AMPLIFIER

#### Application.

**Same application** as DC Regulator Using Cascode Twin-Triode Amplifier.

#### Characteristics.

Same characteristics as DC Regulator Using Cascode Twin-Triode Amplifier

# Circuit Analysis.

**General.** The-de regulator with twin-triode series regulator tube, cascade twin-triode amplifier, and gas-filled voltage reference tube is capable of providing very stable output voltage regulation. In this discussion the term "regulation" means the maintenance of a nearly constant output voltage, regardless of changes in the input voltage or the load current. The variations in output voltage that normally result from component aging, changes in operational environment, etc, are usually considered in the design of the circuit, and are compensated for by using close-tolerance (on the order of 1, 2, or 5 percent) components whose values do not deviate from the nominal by more than the strict limits specified.

In this type of voltage regulator, regulation is accomplished by allowing the cathode-to-plate conduction resistance of an electron tube, in series with the output of a power supply, to function as a variable resistance, and thus provide the voltage drop necessary to compensate for any change in output voltage. That is, the change in output voltage is compared and amplified in the cascade twin-triode amplifier circuit, and applied as a bias voltage to the grid of the series regulator tube, thereby varying the conduction resistance of this tube. The varying conduction resistance of the regulator tube, in turn, varies the load current drawn by the series circuit and the voltage drop across the series regulator tube; in so doing, the series regulator tube absorbs the change in the output voltage. Voltage regulation on the order of 1 percent can be obtained with this type of dc regulator, depending on the circuit design.

Circuit Operation. A typical dc regulator circuit using a cascade twin-triode amplifier is illustrated in the accompanying circuit schematic. Electron tube VI is a parallel-connected twin triode used as the series regulator tube. (In applications where the current drain exceeds the current-handling capability of a single series regulator tube, two or more tubes of the same type may be connected in parallel.) Electron tube V2 is another twin triode, in a cascade dc amplifier circuit configuration, used as the regulator amplifier. Tube V3 is a cold-cathode, gas-filled regulator tube used to provide a reference voltage for operation of the regulator-amplifier circuit. The use of the gas-filled regulator tube in this application is satisfactory as a reliable reference since there are no excessive currents in that branch of the circuit. Electron tubes V1 and V2 are indirectly heated, cathodetype tubes; VI normally has a high heater-to-cathode voltage rating, while V2 has a heater-to-cathode voltage rating which is typical for receiving-type tubes. Because of the heater-to-cathode breakdown voltage limitations imposed by the tubes themselves, it is usually necessary to isolate the filament circuits from each other and to supply the filament (heater) voltages from independent sources.



#### DC Regulator Using Cascade Twin-Triode Amplifier

Resistors R2 and R3, in the grid circuits of VI, are parasitic oscillation suppressors; they are of equal value, generally between 270 and 1000 ohms. Resistors R4 and R5, in the cathode circuits of VI, are included for the purpose of equalizing the current flow in the parallel-connected triode sections; these resistors are of equal value, generally between 10 and 47 ohms, depending upon the circuit design. Resistor R1O, connected in series with reference tube V3 across the output circuit, serves to apply the full output voltage of the regulator to V3, to ensure a satisfactory striking potential and also to act as a currentlimiting resistor once the tube is ionized. The choice

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of current is a compromise between shortened tube life at high currents, and higher noise level at low currents. Resistor R9 returns and grid of V2B to the positive reference voltage; also, resistor R9, in conjunction with capacitor Cl, forms a series RC filter across V3 to suppress the transient noise generated by the gas tube and thereby present these undesirable signals from appearing on the grid of V2B. The value of capacitor C 1 is usually a compromise between a value which offers low impedance to the transient noise and a value which is not so large as to affect the normal operation of reference tube V3.

Capacitor C2 couples the full value of the power supply ripple voltage (usually 120 Hz) appearing in the output of the regulator to the cathode of V2B. If capacitor C2 were not used, only a portion of the ripple voltage would be applied to the cathode of V2B, as determined by the voltage-divider action of resistors R1 1, RI 2, and R13. The value of capacitor C2 is clown so that it is just large enough to provide satisfactory ripple suppression. If the value of capacitor C2 were made too large, the response time of the regulator circuit to normal dc output voltage variations would be affected; a value of from 0.01 to 0.1 microfarad is typical in most regulator-amplifier circuits, although values to 2 microfarads may occasionally be used. Capacitor C3 is connected across the output terminals to lower the output impedance of the regulator circuits; the value of this capacitor depends upon the circuit design, but is usually 2 microfarads or larger. Resistors **R1**1, R12, and R13 form a voltage divider across the output of the regulator circuit, and are in parallel with the resistance of the load. Resistor R12 is adjustable, and is used to set the output voltage to the desired value that the circuit is to maintain.

The cascade configuration of the regulatoramplifier circuit, V2, can be considered as two triode amplifiers that use direct coupling. In a directcoupled (de) amplifier, operating plate voltage and current are usually established by the circuit design, and the grid bias is then adjusted to compensate for tube tolerance. Since, in order to function, to plate of a tube must have a positive voltage with respect to its cathode, and the grid of the next tube must have a negative voltage with respect to its cathode, the voltage-divider arrangements indicated in the diagram are required to obtain the necessary operating voltages for the cascade twin-triode direct-coupled amplifier, V2.

The two triodes of the cascade twin-triode amplifier are the input stage, which is the right-hand tube (V2B), and the output stage, which is the left-hand tube (V2A). The control grid of the input stage is at a positive potential determined by the reference tube, V3. The cathode of the input stage is returned to the wiper arm of voltage-divider variable resister RI 2. The cathode voltage of V2B, as determined by the setting of resistor R12, is slightly more positive than the operating potentird of reference tube V3; hence, a bias voltage of only a few volts is established between the control grid and cathode of V2B. Resistor R8 is the plate-load resistor for the input stage, V2B; since direct coupling is used from the plate of V2B to the grid of V2A, resistor R8 also serves as the grid-return resistor for the control grid circuit of the output stage, V2A. Thus, the plate voltage of V2B is also the grid voltage of V2A. The cathode of V2A is returned to the junction of resistors R6 and R7, which forma voltage divider across the regulator output, E out. The V2A cathode voltage, which is the voltage developed across resistor R7, is slightly more positive than the voltage at the grid of V2A; hence, a bias voltage of only a few volts is established between the control grid and cathode of V2A. Plate voltage for V2A is obtained from the unregulated voltage input,  $E_{in}$ , through plate-load resistor R1.

As previously mentioned, the operation of this regulator circuit is based upon the voltage-divider principle of using a variable resistance in the form of electron tube VI is series with the load resistance. The regulated output voltage, E<sub>out</sub>, appears across the voltage dividers formed by resistors R11, R12, and R13, and resistors R6 and R7, which are connected across the output of the regulator circuit and in parallel with the load. The total resistance of these voltage-divider resistors in parallel with the load resistance constitutes one part of the resistance in the regulator series voltage-divider arrangement, which includes the variable cathode-to-plate resistance of series regulator tube V1. The currents which pass through the parallel branches (voltage-divider resistors and load resistance) combine, and this total current passes through series regulator tube V1. When the cathode-to-plate resistance of VI is controlled to vary the voltage drop across this tube, the output voltage developed across the load can be regulated and maintained at a constant value.

In order to understand how the dc regulator circuit operates under varying-load conditions, it is

necessary to examine first the static voltage distribution under normal-load conditions. The cathode of series regulator tube VI is held positive with respect to ground by the output voltage,  $E_{\mbox{\tiny Out}},$  while the grid is held somewhat less positive by the action of regulator amplifier V2. The difference between these two voltages is the bias voltage for V1, which is at the proper value for series regulator tube VI to have the required amount of cathode-to-plate resistance to produce the correct output voltage. The output voltage is applied to reference tube V3 through resistor R1O, causing V3 to ionize and conduct, thereby establishing a reference voltage at the grid of the input stage, V2B, of the cascade regulator amplifier. (The action of the gas-filled reference tube, V3, is the same as that previously described under Gas-Tube Regulator Circuit earlier in this section.) Regardless of the value of the dc voltage applied to the input,  $\mathbf{E}_{in}$ , of the regulator circuit, the voltage at the grid of V2B will be held constant (by the action of V3) for use as a reference voltage.

Cascade regulator amplifier V2, in essence a twostage series-connected triode amplifier, uses the plate load of the input stage, V2B, as the grid input impedance of the output stage, V2A. Thus, the signal to the imput stage is applied between the cathode and ground; the output of this same stage, which is developed across resistor R8, is the input to the directcoupled output stage, and is applied between the control grid and ground. The grid of V2B is connected through resistor R9 to the positive reference voltage established by V3, and the cathode of the same tube is at a potential slightly more positive than the reference voltage, since it is returned to the wiper arm of voltage-divider variable resistor R12; this arrangement establishes the operating bias for V2B. The plate of V2B is connected to the full voltage of the regulated output through resistor R8; because the plate of V2B is more positive than its cathode, and the proper bias is established, tube V2B conducts. When V2B plate current flows through resistor R8, a voltage is dropped across this resistor; this voltage is also the grid voltage of V2A, and is at a relatively high value.

A two-stage direct-coupled amplifier is usually designed so that approximately one-half of the available voltage of the regulated output,  $E_{out}$ , is used for the input stage. The plate of the output stage, V2A, of the two-stage configuration is connected through a suitable load resistor to the most positive point of the

available voltage, which, in this regulator circuit, is through resistor R1 to the unregulated input,  $E_{in}$ . The cathode of the output step, V2A, must be connected to a positive voltage point suitable for providing the proper biasing voltage and the proper plateoperating voltage. This point is determined by the proper selection of voltage-divider resistors R6 and R7 so that the voltage developed across resistor R7, which is the cathode-bias voltage of V2A, is slightly more positive than the voltage at the grid (which is determined by the voltage drop across resistor R8).

Although the cascade twin-triode regulatoramplifier circuit is a rather complex resistance network which must be adjusted carefully to obtain the proper plate, grid, and cathode voltages for both stages, it provides a rather high gain and good frequency response; therefore, it serves very well as the dc amplifier in an electronic voltage regulator. That is, when regulator amplifier V2 is conducting, the voltage drop across V2A plate-load resistor RI provides a voltage for the grids of series regulator tube VI; this voltage is less than either the plate or cathode voltage of VI. The difference in voltage between the cathodes and grids of V1 is the operating bias for VI. Thus, the setting of resistor R12 determines the current through V2B, which, in turn, determines the bias of V2A. This bias controls the conduction of V2A hence the voltage drop across resistor R1, which establishes the bias for V1. It is this bias level that initially determines the effective internal resistance of VI to obtain the desired output voltage, E<sub>out</sub>, from the regulator circuit.

Assume, now, that the regulated output voltage, E<sub>out</sub> attempts to decrease, either because of a decrease in the input voltage to the regulator circuit or because of an increase in the load requirement. Through the voltage-divider action of resistors R11, R12, and R13, a slightly lower positive voltage now appears across R12, and RI 3. This results in a decrease in the positive voltage applied to the cathode of V2B and a corresponding decrease in the bias voltage between this cathode and the grid of V2B. (The grid voltage of V2B remains constant because of the action of reference tube V3.) As a result of the decreased bias, V2B now conducts more current, and this additional current flow through plate-load resistor R8 results in a greater voltage drop across R8; thus, the voltage at the plate of V2B decrease. Since the voltage at the plate of V2B is also the grid voltage of V2A, the bias on V2A now increases; this results

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from the fact that a negative-going grid signal in conjunction with a fixed voltage on the cathode causes the difference in potential between these two electrodes to become greater. The increased bias of V2A reduces the conduction through this tube and causes a decrease of plate current through plate-load resistor Rl, thereby producing a smaller voltage drop across this resistor to cause a rise in V2A plate voltage. This positive-going voltage at the plate of V2A is coupled to the grids of VI and causes the difference in potential between the grids and cathodes of VI to decrease. This difference in voltage between the grids and cathodes of VI is the operating bias for VI. Thus, as a result of this bias voltage decrease, the effective internal resistance of V1 decreases. When the internal resistance of V1 decreases, more load current flows through VI, the voltage drop across V1 decreases, and the output voltage of the regulator circuit increases to its original value.

> An action similar to that just described occurs , when the regulated output voltage,  $E_{uu}$ , attempts to increase. Through the voltage-divide action of resistors R11, R12, and R13, the bias voltage between the cathode and grid of V2B is increased, since a slightly higher positive potential now exists across R12 and R13. As a result of the increased bias, V2B now conducts less current, and this decreased current flow through plate-load resistor R8 causes a smaller voltage drop to occur across R8; thus, the voltage at the plate of V2B increases, and this positive-going voltage causes the bias of V2A to decrease. With a decreased bias, V2A conducts more heavily and the increased plate current through plate-load resistor R1 produces a negative-going voltage at the plate of V2A. This negative-going signal is coupled to the grids of Vl, causing the difference in potential between the grids and cathodes of VI to increase. This difference in voltage between the grids and cathodes of **V1** is the operating bias for VI. Thus, as a result of this bias voltage increase, the effective internal resistance of VI increases. When the internal resistance of V1 increases, less load current flows through VI, the volt-: age drop across V1 increases, and the output voltage of the regulator circuit decreases to its original value.

The actions described in the preceding paragraphs are practically instantaneous; consequently, the output voltage,  $E_{out}$ , remains practically constant. Since all the load current must pass through the series regulator tube, V1, the tube must be capable of passing considerable current. In some circuit applications

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where the load current **requirements** exceed the capabilities of a single tube, two or more identical tubes are connected in parallel (as the sections of twin-triode V1 have been paralleled) in order to obtain suitable regulation characteristics and current-handling capability.

The output of the regulator circuit is coupled to the cathode of the input stage of the cascade twintriode amplifier tube, V2, through coupling capacitor C2. Any ripple component present in the output voltage is amplified by V2, and, since the circuit is basically a negative feedback circuit, the ripple component is suppressed. As a result, the regulator circuit is sensitive to any voltage changes and it is very effective in removing any fundamental ripple-frequency component which is present in the regulated voltage output. Although there are many minor variations in the regulator-amplifier circuit configuration, the function of the regulator circuit remains the same, that is, to supply a regulated output voltage to the load which is independent of variations in input voltage or changes in load current.

# Failure Analysis.

**Due** to the similarity between the DC Regulator using a Cascade Twin-Triode Amplifier to previous circuits discussed in this section (namely, the DC Regulator using a Pentode Amplifier and the DC Regulator using a Cascode Twin-Triode Amplifier), the discussion will not be repeated here. With minor changes in component designations, the same failure analysis is applicable.

# DC REGULATOR USING TWIN-TRIODE AND PENTODE (BALANCED INPUT)

#### Application.

**Same application** as DC Regulator using a Pentode Amplifier.

# Characteristics.

Same characteristics as DC Regulator using a Pentode Amplifier, with following exceptions:

Uses twin-triode differential amplifier and pentode amplifier circuit to control the series electron tube; the pentode amplifier uses a separate external screenvoltage supply.

The gas-tube regulators are fed from an external regulated negative-voltage supply.

### Circuit Analysis.

**Generel. The** dc regulator using a twin-triode differential amplifier and pentode amplifier is capable of providing very stable output voltage regulation. In this discussion the term "regulation" means the maintenance of a nearly constant output voltage regardless of changes in the input voltage or the load current. The variations in output voltage that normally result from component aging, changes in operational environment, etc, are usually considered in the design of the circuit, and are compensated for by using close-tolerance (on the order of 1, 2, or 5 percent) components whose values do not deviate from the nominal by more than the strict limits specified.

In this type of voltage regulator, regulation is accomplished by allowing the cathode-to-plate conduction resistance of an electron tube, in series with the output of a power supply, to fuction as a variable resistance, and thus provide the voltage drop necessary to compensate for any change in output voltage. That is, the change in output voltage is compared and amplified in the twin-triode and pentode regulatoramplifier circuit, and applied as a bias voltage to the grid of the series regulator tube, thereby varying the conduction resistance of this tube. The varying conduction resistance of the regulator tube, in turn, varies the load current drawn by the series circuit and the voltage drop across the series regulator tube; in so doing, the series regulator tube absorbs the change in the output voltage. Voltage regulation on the order of 1 percent can be obtained with this type of voltage regulator, depending on the circuit design.

Circuit Operation. A typical dc regulator circuit using a twin-triode differential amplifier and pentode amplifier is illustrated in the accompanying circuit schematic. Electron tube, V1 is a parallel-connected twin-triode used as the series regulator tube. (In applacations where the current drain exceeds the current-handling capability of a single series regulator tube, two or more tubes of the same type may be connected in parallel.) Electron tube V2 is a high-gain pentode, and electron tube V3 is a high-gain twintriode; V3 functions as a cathode-coupled differential amplifier and is the input stage of the regulatoramplifier circuit, whereas pentode amplifier V2 is the output stage of the same circuit. The high amplification obtain from differential amplifier V3 and pentode amplifier V2 enables the circuit to have good



DC Regulator Using Twin-Triode and Pentode (8alancad Input)

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sensitivity to small-voltage variations. Tubes V4 and V5 are cold-cathode, gas filled tubes used to provide reference voltages for operation of the regulatoramplifier circuit. The use of the gas-filled regulator tubes in this application is satisfactory as reliable references sinces there are no excessive currents in those branches of the circuit. Electron tubes V1, V2, and V3 are indirectly heated, cathode-type tubes; VI normally has a high heater-to-cathode voltage rating, while V2 and V3 have a heater-to-cathode voltage rating which is typical for receiving-type tubes. Because of the heater-to-cathode breakdown voltage limitations imposed by the tubes themselves, it is usually necessary to isolate the filament circuits from each other and to supply the filament (heater) voltages from independent sources.

Resistors R1 and R2, in the grid circuits of VI, are parasitic oscillation suppressors; they are of equal value, generally between 270 and 1000 ohms. Resistors R3 and R4, in the cathode circuits VI, are included for the purpose of equalizing the current flow of the parallel-connected triode sections; these resistors are of equal value, generally between 10 and 47 ohms, depending upon circuit design. Resistors R5 and R6 are connected in parallel with series regulator tube VI to reduce its plate dissipation. The value of these resistors is selected so that their current flow under all operating conditions is less than the minimum load current; this will ensure a current flow through series regulator tube V1 and thereby permit the regulator to function.

Gas-fdled regulator tubes V4 and V5 provide reference voltage for the grid circuits of V2 and V3B, respectively. Parallel-connected resistors R18 and R19 apply to the cathode of V4 a negative potential which is sufficiently high to ensure satisfactory ionization; these resistors also limit the current through V4 once the gas in the tube is ionized. Because tube V5 provides a reference voltage less negative than of V4, its cathode potential is accordingly made less negative by the voltage drop across resistor R20, which also serves as a current-limiting resistor once tube V5 is ionized. In a typical dc regulator circuit, V4 may be a type OA2 gas tube to provide a reference voltage of -150 volts, and V5 may be a type 5651 gas tube to provide a reference voltage in the range of -82 to -92 volts. By supplying the reference tubes from an external regulator negative-voltage source rather than connecting the tubes in the cathode circuit of the regulator-amplifier stage (as is

done in some dc regulator circuits), several advantages are obtained. First, the cathodes of the regulatoramplifier stages are at ground rather than at a high positive potential, thereby allowing a larger plate swing of the stages; second, the reference tube is in a grid circuit rather than in a cathode circuit, and thus operates under constant-current conditions; and third, the regulator-amplifier stage gain is greater with this comection because cathode degeneration caused by gas-tube impedance is not present. The choice current for the respective gas-fdled tubes, as determined by resistors R18, R19, and R20, is a compromise between shortened tube life a high currents and higher noise level at low currents. Capacitors C4 and C5, connected across V4 and V5, respectively, are bypass capacitors to supress the transient noise generated by the gas tubes. The value of these capacitors is usually the largest value recommended by the tube manufacturer.

The regulator-amplifier circuit consists of cathodecoupled differential amplifer V3, used as a balanced input stage, cascaded with pentode amplifier V2, used as a single-ended output stage. The left-hand section of the differential amplifier, V3A, functions as a triode amplifier, and the right-hand section, V3B, functions as a cathode follower. The balanced-input configuration of twin-triode V3 reduces the effects of tube aging and heater voltage variations.

If an input signal is applied to the grid of the cathode follower (V3B) and the output signal is taken from the plate of the triode amplifier (V3A), the cathode-coupled differential amplifier will have a high input impedance and provide high amplification without signal inversion between the input and output. Resistors R15, R16, and R17 from a voltage divider across the regulator output and the regulated negative input to gas-filled reference tube V5. This voltage divider provides the operating bias for the grid of V3B; the value of bias voltage is selected by setting variable resistor R16. Resistor R14 is the common cathode resistor that provides the cathode coupling from cathode follower V3B to triode amplifier V3A. Resistors R12 and R13 also form a voltage divider, but this one is across the regulator output and ground. The voltage developed across resistor R13 provides the operating bias for the grid of triode amplifier V3A. Plate voltage for V3A is obtained from the regulator output through resistor R9; this resistor, along with resistors R1O and R1 1, is in a voltage divider across the regulator output and the

regulated negative input to **gas-filled** reference tube V4.

In addition to providing the plate voltage for V3A, voltage divider R9, R1O, and R1 1 provides the operating bias for the girl of output pentode amplifier V2; this bias voltage is obtained from the junction of resistors R1O and RI1. Resistors R1O provides direct coupling from the plate of V3A to the grid of V2. The RC combination of resistor RIO and capacitor Cl is a phase-lead network in the coupling circuit; the purpose of this network is to provide stabilization and thereby prevent oscillation within the regulator amplifier. The suppressor grid of pentod V2 is connected internally to the cathode, and the cathode is returned directly to ground. The pentode screen grid receives its operating voltage from an external regulated positive-voltage source. Plate voltage for output pentode amplifier V2 is obtained from the regulator output through parallel-connected, equal-value resistors R7 and R8; this arrangement lowers the effective plate-load resistance, but permits the pentode to handle higher plate currents. The decreased plate-load resistance improves the frequency response of the circuit.

Capacitor C2 couples the full value of the power supply ripple voltage (usually 120 Hz) appearing in the output of the regulator to the grid of V3B. If capacitor C2 were not used, a portion of the ripple voltage would be applied to the grid of V3B, as determined by the voltagedivider action of resistors R15, R16, and R17. The value of capacitor C2 is chosen so that it is just large enough to provide satisfactory ripple suppression. If the value of capacitor C2 were made too large, the response time of the regulator circuit to normal dc output-voltage variations would be affected; a value of from 0.01 to 0.1 microfarad is typical in most regulator-amplifier circuits, although values up to 2 microfarad may, occasionally be used. Capacitor C3 is connected across the output terminals to lower the output impedance of the regulator circuit; the value of this capacitor depends upon the circuit design, ranging from 0.5 microfarad to 2 microfarads. The voltage dividers formed by the series-connected combinations of resistors R9, R1O, and R11, resistors R12 and R13, and resistors R15, R16, and R17 are all across the output of the regulator circuit and are thereby in parallel with the load. Any resistance measurement across the output must take into consideration these parallel circuits. Voltagedivider resistor R16, in the grid circuit of V3B,. is adjustable and is used to set the output voltage to the desired value that the circuit is to maintain.

The cathode-coupled differential amplifier configuration of V3 provides a single-ended output signal having high amplification but no signal inversion from input to output. The single-ended output makes the circuit sensitive to power-supply voltage changes, and the common-cathode arrangement causes the cathodes to mutually offset the drift due to heatervoltage variations. The gain of the differential amplifier is a combination of the gains of the cathodefollower section, V3B, and the triode-amplifier section, V3A. The output impedance of the cathode follower acts as an impedance in series with the cathode input to the triode amplifier. To avoid an excessively large bias produced by a large-value cathode resistor (R14), the cathodes of the differential amplifier are returned to ground and the grids are returned to the regulator output. The sum of the plate currents of V3A and V3B is equal to the current through cathode resistor R14. This value of current is essentially constant; that is, an increase in cathode follower V3B plate current causes an almost equal decrease in triode amplifier V3A plate current. In this manner the current through resistor R14 is kept essentially constant.

As previously mentioned, the operation of this regulator circuit is based upon the voltagedivider principle of using a variable resistance in the form of electron tube V1 in series with the load resistance. The regulated output voltage, **E**<sub>out</sub>, appears across the voltage dividers (previously pointed out) which are in parallel with the load. The total resistance of these voltage-divider resistors in parallel with the load resistance constitutes one part of the resistance in the regulator series "voltagedivider arrangement, which includes the variable cathode-to-plate resistance of " series regulator tube V1. The currents which pass through the parallel branches (voltage-divider resistors and load resistance) combine, and this total current passes through series regulator tube VI (and parallelconnected resistors R5 and R6). When the cathodeto-plate resistance of V1 is controlled to vary the voltage drop across this tube, the output voltage developed across the load can be regulated and maintained at a constant value.

In order to understand how the dc regulator circuit operates under varying-load conditions, it is necessary to examine first the static voltage distribution under normal-load conditions. The cathode of

series regulator tube VI is held positive with respect to ground by the output voltage,  $E_{out}$ , while the grid is held somewhat less positive by the action of the regulator amplifier (pentode amplifier V2 and differential amplifier V3). The difference between these two voltages is the bias voltage for V1, which is at the proper value for series regulator tube V1 to have the required cathode-to-plate resistance to produce the correct output voltage.

A negative voltage is fed from an external regulated source to the cathode of reference tube V4 through parallel-connected resistors R18 and R19, and to the cathode of reference tube V5 through resistor R20. Since the plate of each reference tube is at ground potential, the negative voltage at the cathode causes the gas to ionize and the tube to conduct. In this manner negative reference voltage are established for the voltage dividers feeding the grid of pentode amplifier V2 and the grid of the cathodefollower section, V3B, of the differential amplifier. (The action of the gas-filled reference tubes is the same as that previously described, under Gas-Tube Regulator Circuit, in this Section of the Handbook.) Regardless of the value of dc voltage applied to the input, E<sub>in</sub>, of the regulator circuit, the negativevoltage references in the grid circuits of V2 and V3B will be held constant by the action of V4 and V5, respectively.

The regulator-amplifier circuit, which consists of pentode amplifier V2 and cathode-coupled differential amplifier V3, uses the cathode load impedance of cathode follower V3B as the cathode input impedance of triode amplifier V3A. Thus, the signal of the cathode follower is applied between the control grid and ground, while the output of this same stage is the input to the triode amplifier, and is applied between the cathode and ground. The grid voltage for the cathode follower is determined by the setting of voltage-divider resistor R16. The triode amplifier has a freed voltage on its grid, obtained from the junction of voltage-divider resistors R12 and R13. The plate voltage of V3A and V3B is obtained from the regulated output,  $E_{out}$ ; the plate of V3B is returned directly to the regulator output, whereas the plate of V3A is returned to this potential through plate-load resistor R9, which is part of the voltagedivider network consisting of resistors R9, R1O, and R11. Thus, the operating potentials at the electrodes of V3A and V3B are such that, under normal-load conditions, they permit a predetermined value of

current to be drawn by V3 and develop an output signal across plate-load resistor R9.

The output signal of V3A developed across resistor R9 is direct-coupled through resistor R1O to the grid of pentode amplifier V2. This signal, then, acts to control the conduction through V2. When V2 is conducting, the current through partdlel-coducted plateload resistors R7 and R8 develops a voltage at the plate of V2; this voltage is coupled to the grids of V]. The voltage at the grids of VI is less than the voltage at the cathodes of this tube; hence, the normal-load operating bias for VI is established. The setting of variable resistor RI 6, therefore, determines the current through V3, which, in turn, controls the current through V2 and thereby establishes the bias for V1. This bias voltage of V1 initially determines the effective normal-load internal resistance of VI to obtain the desired output voltage, E<sub>out</sub>, from the regulator circuit.

Assume, now, that the regulated output voltage, Eout, attempts to increase, either because of an increase in the input voltage, E<sub>in</sub>, to the regulator circuit-or because of a decrease in the load requirement. Through the voltage-divider action of resistors R15, R16, and R17, a slightly higher positive voltage now appears across resistors R16 and R17. This results in an increase in the voltage applied to the grid of V3B, and a corresponding decrease in the bias of this stage. As a result of the decreased bias, V3B now conducts more current, and this additional current flow through cathode-load resistor R14 results in a greater voltage drop across this resistor. The voltage at the cathode of V3, in going more positive, increases the bias on V3A and thereby reduces conduction through this stage. The reduced plate current of V3A causes a small voltage drop across a plate-load resistor R9, which, in effect, is a positive-going signal at the plate of V3A. The differential amplifier, therefore, amplifies but does not invert the positive going signal applied to the grid of V3B.

The positive-going signal at the plate of V3A is direct-coupled through resistor RIO to the grid of pentod amplifier V2, where it reduces the bias and causes an increase in the conduction of this stage. When the conduction of V2 is increased, the additional plate current through plate-load resistors R7 and R8 produces a greater voltage drop across these resistors, and thereby develops a negative-going signal at the plate of V2. This negative-going is coupled to the grids of VI, where it causes the difference in

voltage between the grids and cathodes of VI to increase. The difference in voltage between the grids and cathodes of VI is the operating bias for VI. As a result of the bias voltage increase, the effective internal resistance of VI increases. When the internal resistance of VI increases, Iess load current flows through V1, the voltage drop across VI increases, and the output voltage E **out**, of the regulator circuit decreases to its original value.

An action similar to that just described occurs when the regulated output voltage,  $E_{out}$ , attempts to decrease. Through the voltagedivider action of resistors R15, R16, and R17, the bias voltage on the grid of V3B is increased, since a slightly lower positive potential now exists across resistors R16 and R17. As a result of the increased bias, V3B now conducts less current, and the decreased current flow through cathode-load resistor R14 causes a smaller voltage drop to occur across this resistor. The voltage at the cathode of V3, in going negative, decreases the bias on V3A and thereby increases conduction through this stage. The increased plate current of V3A causes a greater voltage drop across plate-load resistor R9, which, in effect, is a negative-going signal at the plate of V3A. This negative-going signal is direct-coupled through resistor R1O to the grid of pentode amplifier V2, where it increases the bias and causes a decrease in the conduction of V2. When V2 conduction decreases, less plate current flows through plate-load resistors R7 and R8, thereby producing a smaller voltage drop across these resistors. Thus, the voltage at the plate of V2 (and the grids of Vl) increases and causes the difference in voltage between the grids and cathodes of VI to decrease. This difference in voltage between the grids and cathodes of VI is the operating bias for V1. As a result of the bias voltage decrease, the effective internal resistance of V1 decreases. When the internal resistance of V1 decreases, more load current flows through V1, the voltage drop across V1 decreases, and the output voltage of the regulator circuit increases to its original value.

The actions described in the preceding paragraphs are practically instantaneous; consequently, the output voltage,  $E_{out}$ , remains practicality constant. Since most of the load current must pass through series regulator tube VI, the tube must be capable of passing considerable current. In some circuit applications where the load current requirements exceed the capabilities of a single tube, two or more identical tubes are connected in parallel (as the sections of twin-triode V1 have been paralleled) in order to obtain suitable regulation characteristics and currenthandling capability. Also, in order to reduce the plate dissipation of series regulator tube V1, **resistors** can be connected in parallel with the tube (as resistors R5 and R6 have been connected in this regulator circuit).

The output of the regulator circuit is coupled to the grid of the cathode-follow section, V3B, of the differential amplifier through coupling capacitor C2. Any ripple component present in the output voltage is amplified in the regulator amplifier, and since the circuit is basically a negative-feedback circuit, the ripple component is suppressed. As a result, the regulater circuit is sensitive to any voltage changes and is very effective in removing any fundamental ripplefrequency component which is present in the regu-1 ted **voltage** output. Although there are many variations in the regulator-amplifier circuit configuration, the function of the regulator circuit remains the same, that is, to supply a regulated output voltage to the load which is independent of variations in input voltage or changes in load current.

# Failure Analysis.

General. The dc regulator using a twin-triode and pentode regulator amplifier includes several components which are rather critical and thus directly affect the operation of the regulator circuit. For this reason, the resistors in the regulator-amplifier circuit are normally close-tolerance (on the order of 1, 2, or 5 percent) resistors with good temperature-stability characteristics. The operation of the circuit will be impaired if these resistors should change in value for any reason. Since the regulator circuit attempts to hold the output voltage constant, it is usually good practice to determine whether the load current is within tolerance before supecting trouble within the " regulator circuit proper. A load-current measurement may be made by inserting a milliammenter (having a suitable range) in series with the output of the regulator circuit. Also, a voltage measurement should be made at the input to the regulator circuit to determine whether the unregulated voltage output from the power supply (and filter circuit) is within tolerance.

No **Output**. In this dc regulator circuit, the nooutput condition is likely to be limited to one of the following possible causes: the lack of filament voltage applied to series regulator tube V1, the lack of applied dc voltage (from the associated power supply

and filter circuit), or a short-circuited load (including output capacitor C3). A visurd check of the glassenvelope series regulator tube, VI, should be made to determine whether the fdament is lit; if the fdament is not lit, it may be open or the filament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of **filament** voltage at the tube socket should be determined by measurement. The dc voltage applied to the regulator circuit should be measured at the input (plate of VI) to determine whether it is present and of the correct value, since the lack of input voltage from the associated power supply and filter circuit will cause a lack of output voltage. With the dc voltage removed from the input to the circuit, resistance measurements can be made across the load to determine whether the load circuit, including capacitor C3, is shorted. (The resistance measured across the load circuit will normally be something less than the total value of the voltage-divider resistors, depending upon the load circuit design.)

If pentode amplifier V2 has low emission, the voltage drop across plate-load **resistors** R7 and R8 will be below normal; therefore, the bias of V1 will be decreased and a high output from the regulator will result. Under this circumstance, a tube known to be good should be substituted at V2 and operation of the circuit observed to determine whether tube V2 is the cause of the trouble.

**High Output. The** high-output condition is usually caused by a decrease in operating bias for the series regulator tube, VI, which, in turn, causes the tube to decrease its internal resistance and permit the regulator output voltage to rise above normal. Therefore, any defects in the electronic regulator circuit which can cause a decrease in the operating bias for V1 should be suspected. Voltage measurements should be made at the socket of V1 to determine whether bias (cathode-to-grid) voltage is present.

A visual check of gas-filled regulator tube V5, which provides a reference voltage for the operation of the cathode-follower section (V3B) of the differential amplifier circuit, should be made to determine whether the tube is conducting. A voltage measurement made between the cathode and plate of V5 will determine whether sufficient negative voltage is present at the tube to cause conduction. If the voltage is more negative than normal, the tube may be defective. If the voltage measured across V5 is less negative than normal, it is likely that resistor R20 has changed in value.

A visual check of regulator-amplifier tubes V2 and V3 should be made to determine whether their filaments are lit; if the filaments are not lit, they may be open or the filament voltage may not be applied. The tube **filaments** should be checked for continuity; also, the presence of filament voltage at the tube sockets should be determined by measurement.

The bias voltages applied to V2 and V3 should be measured to determine whether these tubes are improperly biased, causing the operating bias on V1 to decrease. Assuming that V4 and V5 are conducting normally to provide the proper reference voltages, if the voltage at the grid of V2 or V2B is below normal, there will be an increase in the bias on the respective tube. In this case it is possible that the resistor R9, R1O, or R11 has changed in value to increase the bias of V2, or that resistor R15 or R16 has changed m value to increase the bias of V3B; in addition, an improper setting of variable resistor R16 will affect the bias voltage at the grid of V3B. A high output from the regulator also will result when the voltage at the grid of V3A is above normal, and thereby causes a bias decrease on this stage; a change in the value of resistor R12 or R13 will produce this effect. If V2 or V3B is biased to cutoff, or if V3A is conducting heavily as a result of a high positive voltage at its grid, V1 will be made to conduct heavily as a result of a decreased operating bias. In this case, it is likely that resistor R9 or R1O is open to cut off V2, that resistor R15 or the top portion of resistor R16 is open to cut off V3B, or that resistor R13 is open to cause the heavy conduction of V3A.

Low Output. The low-output condition of the regulator is usually caused by an increase in operating bias for the series regulator tube, Vl, which, in turn, causes the tube to increase its internal resistance and permit the regulator output voltage to fall below normal. Therefore, any defects in the electronic regulator circuit which can cause an increase in the operating bias for V1 should be suspected. Trouble in one section of V1 (such as low cathode emission or an open tube element) will cause a reduction in the output. Voltage measurements should be made at the socket of V1 to determine whether the bias (cathode-to-grid) voltage is excessive. The equalizing resistors, R3 and R4, in the cathode circuits of V1 should be measured to determine that neither one is open, that they have

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not increased in value, and that they are of equal resistance.

A visual check of gas-tilled regulator tube V4, which provides a reference voltage for the operation of pentode amplifier V2, should be made to determine that the tube is conducting. A voltage measurement made between the cathode and plate of V4 will determine whether sufficient voltage is present at the tube to cause conduction. If the voltage is more negative than normal, the tube may be defective. If the voltage measured across V4 is less negative than normal, it is likely that resistor R18 or R19 is open, thereby providing a voltage which is not sufficiently negative to cause gas tube V4 to ionize.

The bias voltages applied to V2 and V3 should be measured to determine whether these tubes are improperly biased, causing the operating bias on V1 to increase. Assuming that V4 and V5 are conducting normally to provide the reference voltages, if the voltage at the grid of V2 or V3B is above normal, there will be a decrease in the bias on the respective tube. In this case, it is possible that resistor R9, R10, or Rll has changed in value to decrease the bias of V2, or that resistor R15 or R16 has changed in value to decrease the bias of V3B; in addition, an improper setting of variable resistor R16 will affect the bias voltage at the grid of V3B. A low output from the regulator also will result when the voltage at the grid of V3A is below normal, and thereby cause a bias increase on this stage; a change in the value of resistor R12 or R13 will produce this effect. If V2 orV3B is biased by a high positive voltage on its grid so that either tube conducts heavily, or if V3A is biased to cutoff, VI will be made to conduct less as a result of an increased operating bias. In this case, it is likely that resistor R11 is open or capacitor C1 is leaky or shorted, thus placing a high positive voltage on the grid of V2. A high positive voltage will be placed on the grid of V3B if the bottom portion of resistor R16 or resistor R17 is open, or if capacitor C2 is leaky or shorted. A bias sufficient to cut off V3A will result if resistor R12 is open; also, an open cathode resistor, R14, in the differential amplifier will cut off V3A.

It is possible for the symptom of a high positive voltage at the **grid** of V2 or V3B to be caused by a defect in the voltage reference circuits. For example, if capacitor C4 or C5 (paralleling reference tubes V4

and V5, respectively) is leaky or shorted, the grids **of** pentode amplifier V2 and cathode follower V3B will be returned to ground instead of to their respective negative voltage reference. As a result, the voltage distribution across the respective voltage dividers will be such that the voltage at the grid of V2 or V3B is made more positive. Separately, the voltage at the grid of V2 will be more positive if **reference** tube V4 is defective, and a similar condition will be noted for the grid of V3B is resistor R20 is open. The result of each of the foregoing defects will be an increase in the bias on series regulator tube V1, and a decrease m the regulator output voltage.

If plate-load resistor R7 or R8 (for pentode **ampli**ier V2) is open, the bias voltage applied to the grids of VI will be made larger, causing a decrease in the regulator output. Also, if tube V2 is shorted and conducting heavily, the voltage drop across plate-load resistors R7 and R8 will be excessive. If differential amplifier tube V3 has low emission, the voltage drop across its plate-load resistor (R9) will be below normal; therefore, the bias of V2 will be decreased, and in turn, cause an increase in the bias of V1 and a decrease in the output of the regulator.

As mentioned previously, excessive load current can cause the output voltage to be low, especially if the load current exceeds the maximum rating of series regulator tube V1 (resulting in excessive voltage drop across V1) or if the load current exceeds the rating of the power supply (resulting in a decrease in the applied voltage). For these reasons, output capacitor C3 should be checked to determine whether it is satisfactory. A leaky output capacitor could result in reduced output voltage, although the **regulator**amplifier circuit (V2 and V3) may be **functioning** normally but still be unable to compensate for the decrease in output.

**Poor Regulation Charactaristies.** Voltage instability, slow response, etc, are frequently caused by weak or unbalanced triode sections in series regulator tube VI, unbalanced cathode resistors R3 and R4, or defective regulator amplifier tubes V2 and V3. The gain of the regulator-amplifier stage is determined primarily by tubes V2 and V3 and their applied voltages; therefore, the condition of V2 and V3 and the applied voltages are important factors governing satisfactory operation of the regulator circuit.

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# DC REGULATOR USING PENTODE AND TWIN-TRIODE (BALANCED OUTPUT)

#### Application.

Same application as DC regulator using Pentode and Twin-Triode (Balanced Input).

# Characteristics.

Same characteristics as DC Regulator using Pentode and Twin-Triode (Balanced Input).

# **Circuit** Analysis.

**General.** The dc regulator using a pentode amplifier and a twin-triode differential amplifier is capable of providing very stable output voltage regulation. In this discussion the term "regulation" means the maintenance of a nearly constant output voltage, regardless of changes in the input voltage or the load current. The variations in output voltage that normally result from component aging, changes in operational environment, etc, are usually considered in the design of the circuit, and are compensated for by using close-tolerance (on the order of 1, 2, or 5 percent) components whose values do not deviate from the nominal by more than the strict limits specified.

In this type of voltage regulator, regulation is accomplished by allowing the cathode-to-plate conduction resistance of an electron tube, in series with the output of a power supply, to function as a variable resistance and thus provide the voltage drop necessary to compensate for any change in output voltage. That is, the change in output voltage is compared and amplified in the pentode and twin-triode regulatoramplifier circuit, and applied as a bias voltage to the grid of the series regulator tube, thereby varying the conduction resistance of this tube. The varying conduction resistance of the regulator tube, in turn, varies the load current drawn by the series circuit and the voltage drop across the series regulator tube; in so doing, the series regulator tube absorbs the change in the output voltage. Voltage regulation of approximately 1 percent can be obtained with this type of electronic dc regulator, depending on the circuit design.

Circuit Operation. A typical dc regulator circuit using a pentode amplifier and twin-triode differential amplifier is illustrated in the accompanying circuit schematic. Electron tube V1 is a parallel-connected twin-triode used as the series regulator tube. (In applications where the current drain exceeds the currenthandling capability of a single series regulator tube, two or more tubes of the same type may be connected in parallel). Electron tube V2 is another twintriode, and is used as a cathode-coupled differential amplifier stage. Electron tube V3 is a high-gain pentode amplifier. Together, tubes V2 and V3 function as the regulator-amplifier circuit; pentode V3 is the input stage, and twin-triode V2 is the output stage. Tubes V4 and V5 are cold-cathode, gas-filled tubes used to provide reference voltages for operation of the regulator-amplifier circuit. The gas-filled regulator tubes in this application are satisfactory as reliable references since there are no excessive currents in those branches of the circuit. Electron tubes VI, V2, and V3 are indirectly heated, cathode-type tubes; VI normally has a high **heater-to-cathode** voltage rating, while V2 and V3 have a heater-to-cathode voltage rating which is typical for receiving-type tubes. Because of the heater-to-cathode breakdown voltage limitations imposed by the tubes themselves, it is usually necessary to isolate the filament circuits from each other and to supply the filament (heater) voltages from independent sources.

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DC Regulator Using Pentoda and Twin-Trioda (Balancad Output)

Resistors R2 and R3, in the grid circuits of series regulator tube VI, are parasitic oscillation suppressors; they are of equal value, generally between 270 and 1000 ohms. **Resistors** R4 and R5, in the cathode circuits of VI, are included for the purpose of equalizing the current flow in the parallel-connected triode sections; these resistors are of equal value, generally between 10 and 47 ohms, depending upon the circuit design.

The regulator-amplifier circuit consists of pentode amplifier V3, used as a single-ended input stage, cascaded with cathode-coupled differential amplifier V2, used as a balanced output stage. The left-hand section of the differential amplifier, V2A, functions as a triode amplifier, and the right-hand section, V2B, functions as a cathode follower. The balanced configuration of twin-triode V2 reduces the effects of tube aging and heater voltage variations. If an input signal is applied to the grid of the cathode follower and the output signal is taken from the plate of the triode amplifier, the cathode+ **oupled** differential amplifier will have a high input impedance and provide high amplification without signal inversion between the input and the output. Resistor Rl, connected to the source of unregulated input voltage, Ein, provides plate voltage for triode amplifier V2A. Control grid voltage for this same stage is obtained from voltage-divider resistors R6 and R7, connected across the regulated output voltage, Eout. Resistor R8 is a common resistor for triode **amplifier** V2A and cathode follower V2B,

**Gas-filled** regulator tubes V4 and V5 furnish reference voltages for pentode amplifier V3; V4 is in the cathode circuit, and V5 is in the control grid circuit. Resistors R1O and R11, connected in series with reference tube V4 across the output circuit, serve to

apply the full output voltage of the regulator to V4, to ensure a satisfactory striking potential and also to act as current-limiting resistors once the tube is ionized. In addition, resistors RIO and RI 1 function as a voltage divider to provide the dc operating potential for the screen grid of pentode amplifier V3. Plate voltage for the pentode amplifier is furnished by the regulated output through plate-load resistor R9. Capacitor Cl, comected in parallel with reference. tube V4, is a bypass capacitor which provides a lowimpedance path at the power supply ripple frequency (usually 120 Hz), to reduce the possibility of degeneration in the cathode circuit of V3. The vrdue of capacitor Cl is usually a compromise between a value which offers low impedance to the power supply ripple frequency and a value which is not so large as to affect the normal operation of the reference tube, V4.

Gas tube V5 is in series with voltage-divider resistors R12, R13, and R14 across the regulated output, Eout. Because this arrangement permits a larger. percentage of the output-voltage variations to be coupled to the control grid of the pentode amplifier, the over-all gain of the regulator amplifier is made greater. In some dc regulators, two or more gas tubes may be used in series with the voltage-divider resistors. The number and type of gas tubes used in this manner depends upon the voltage drop required between the output and the grid of pentode amplifier V3; it is usually desirable that the largest postion of the required voltage drop be obtained across the gas tube(s). With a gas tube placed in a grid circuit, such as V5 is in this dc regulator, an additional advantage is realized in that there is a constant current through the gas tube, and its dynamic resistance is of little consequence. Therefore, the gas tube is selected solely on the merits of its ability to regulate at the same voltage each time the power supply (equipment) is turned on and the degree to which the voltage is regulated at a constant value so long as the equipment is in operation. Capacitor C3, connected in parallel with V5, is used to suppress the transient noise generated by the gas tube, and thereby prevent these undesirable signals from appearing on the grid of pentode amplifier V3. The value of capacitor C3, which is usually the largest value recommended by the tube manufacturer, is a compromise between a value which eliminates the transient noise and a value which is not so large as to affect the normal operation of reference tube V5.

Capacitor C2 couples the full value of ripple voltage from the output of the regulator circuit to the grid of V3; if capacitor C2 were not used, ordy a portion of the ripple voltage would be applied to the grid of V3, as determined by the action of V5 and voltage-divider resistors R12, R13, and R14. The value of capacitor C2 is chosen so that it is just large enough to provide satisfactory ripple suppression. If the value of capacitor C2 were made too large, the response time of the regulator circuit to normal dc output-voltage variations would be affected. A value of from 0.01 to 0.1 microfarad is typical in most regulator-amplifier circuits. Capacitor C4 is connected across the output terminals to lower the output impedance of the regulator circuit; the value of this capacitor depends upon the circuit design, but is usually 2 microfarads or larger. Resistors R12, R13, and R14, which forma voltage divider in series with reference tube V5 across the output of the regulator circuit, are in parallel with the resistance of the load. Resistor R13 is adjustable, and is used to set the output voltage to the desired value the circuit is to maintain.

The cathode-coupled differential amplifier configuration of V2 provides a single-ended output signal having high amplit3cation but no signal inversion from input to output. The single-ended output makes the circuit sensitive to power-supply voltage changes, and the common cathode arrangement causes the cathodes to mutually offset the drift due to heater-voltage variations. The gain of the differential amplifier is a combination of the gains of the cathode-follower section, V2B, and the triode-amplifier section, V2A. The output impedance of the cathode follower acts as an impedance in series with the cathode input to the triode amplifier. The sum of the plate currents of V2A and V2B is equal to the current through cathode resistor R8. This value of current is essentially constant; that is, an increase in the plate current of cathode follower V2B causes an almost equal decrease in the plate current of triode amplifier V2A. In this manner, the current through resistor R8 is kept essentially constant.

As previously mentioned, the operation of this regulator circuit is based upon the voltage-divider principle of using a variable resistance in the form of electron tube V1 in series with the load resistance. The regulated output voltage, Eout, appears across the voltage dividers formed by gas tube V5 and resistors R12, R13, and R14, and resistors R6 and R7, which

are **connected** across the output of the regulator circuit and in parallel with the load. The total resistance of these voltage-divider resistors in parallel with the load resistance constitutes one part of the resistance in the regulator series voltage-divider arrangement, which includes the variable cathode-to-plate resistance of series regulator tube V1. The currents which pass **thr.ugh** the parallel branches (voltage-divider resistors and load resistance) combine, and this total current passes through series regulator tube VI. When the cathode-to-plate resistance of V1 is controlled to vary the voltage drop across this tube, the output voltage developed across the load can be regulated and maintained at a constant value.

In order to understand how the dc regulator circuit operates under varying-load conditions, it is necessary to examine first the static voltage distribution under normal-load conditions. The cathode of series regulator tube V1 is held positive with respect to ground by the output voltage, Eout, while the grid is held somewhat less positive by the action of the regulator-amplifier circuit. The difference between these two voltages is the bias voltage for Vl, which is at the proper value for series regulator tube VI to have the required amount of cathode-to-plate resistance to produce the correct output voltage. The output voltage is applied to reference tube V4 through resistors R1O and R1 1;-causing V4 to ionize and conduct, thereby establishing a reference voltage at the cathode of pentode amplifier V3. In a like manner, gas tube V5 also ionizes and conducts to produce a constant voltage drop in the voltage-divider circuit consisting of that tube as well as resistors R12, R13, and R14. (The action of the gas-filled reference tubes, V4 and V5, is the same as that previously described under Gas-Tube Regulator Circuit earlier in this Section of the handbook.) Regardless of the value of the dc voltage applied to the input, Ein, of the regulator circuit, the voltage at the cathode of V3 will be held constant (by the action of V4) for use as a reference voltage. Likewise, the voltage at the top of resistor R12 will be held constant by the action of gas tube V5.

The input to the regulator-amplifier circuit, as determined by the setting of resistor R13, is applied to the grid of pentode amplifier V3. The output signal of this stage, developed across plate-load resistor R9, is direct-coupled to the grid of V2B-the cathode follower input section of cathode-coupled differential amplifier V2. The cathode load impedance of cathode

follower V2B is used as the cathode input impedance of triode amplifier V2A. Thus, the signal to the cathode follower is applied between the control grid and ground, while the output of this same stage is the input to the triode amplifier, and is applied between the cathode and ground. The grid voltage for the cathode follower is determined by the voltage drop across the pentode plate-load resistor, R9. The triode amplifier, V2A, has a fixed voltage on its grid, obtained from the junction of voltage-divider resistors R6 and R7. The plate voltage of V2A is obtained from the unregulated input, Ein, through plate-load resistor RI; the plate of V2B is returned directly to the regulator output. Thus, the operating potentials at the electrodes of V2A and V2B are such that, under normal-load conditions, they permit a predetermined value of current to be drawn by V2 and develop as output signal across plate-load resistor RI.

The output signal of V2A developed across resistor R1 is direct-coupled through resistors R2 and R3 to the grids of series regulator tube V1. This signal, then, acts to control the conduction through VI. That is, when differential amplifier V2 is conducting, the voltage drop across V2A plate-load resistor RI provides a voltage for the grids of series regulator tube VI; this voltage is less than either the plate or cathode voltage of V1. The difference in voltage between the cathodes and grids of VI is the operating bias for V1. Thus, the setting of resistor R13 determines the current through V3, which, in turn, determines the conduction of V2, and thus the voltage drop across resistor R1, which establishes the bias for V1. It is this bias level that initially determines the effective internal resistance of VI to obtain the desired output voltage, Eout, from the regulator circuit.

Assume, now, that the regulated output voltage, Eout, attempts to decrease, either because of a decrease in the input voltage to the regulator circuit or because of an increase in the load requirement. Through the voltage-divider action of resistors R12, R13, and R14, a slightly lower positive voltage now appears across R13 and R14. This results in a decrease in the positive voltage applied to the grid of pentode amplifier V3 and a corresponding increase in the bias voltage between the cathode and the grid of V3. (The cathode voltage of V3 remains constant because of the action of reference tube V4.) As a result of the increased bias, V3 now conducts less current, and this reduced current flow through plateload resistor R9 results in a smaller voltage drop

across R9; thus, the voltage at the plate of V3 increases. Since the voltage at the plate of V3 is also the grid voltage of cathode follower V2B, the bias on V2B now decreases. As a result of the decreased bias, V2B conducts more current, and this additional current flow through cathode-load resistor R8 results m a greater voltage drop across this resistor. The voltage at the cathode of V2, in going more positive, increases the bias on triode amplifier V2A, and thereby reduced conduction through this stage. The reduced plate current of V2A causes a smrdler voltage drop across plate-load resistor R1, which, in effect, is a positive-going signal at the plate of V2A. The differential amplifier, therefore, amplities but does not invert the positive-going signal applied to the grid of V2B. The positive-going voltage at the plate of V2A is coupled to the grids of VI and causes the difference m potential between the grids and cathodes of **V1** to decrease. This difference in voltage between the grids and cathodes of VI is the operating bias for V1. Thus, as a result of this bias voltage decrease, the effective internal resistance of VI decreases. When the internal resistance of V1 decreases, more load current flows through VI, the voltage drop across V1 decreases, and the output voltage of the regulator circuit increases to its original value.

An action similar to that just described occurs when the regulated output voltage, Eout, attempts to increase. Through the voltage-divider action of resistors R12, R13, and R14, the bias voltage between the cathode and grid of V3 is decreased, since a slightly higher positive potential now exists across R13 and R14. As a result of the decreased bias, V3 now conducta more current, and this increased current flow through plate-load resistor R9 causes a larger voltage drop to occur across R9; thus, the voltage at the plate of V3 decreases, and this negative-going voltage causes the bias of V2B to increase. As a result of the increased bias, V2B now conducts less current, and the decreased current flow through cathode-load resistor R8 causes a smaller voltage drop to occur across this resistor. The voltage at the cathode of V2, in going negative, decreases the bias on triode amplifier V2A, and thereby increases the conduction through this stage. The increased plate current of V2A causes a greater voltage drop across plate-load resistor Rl, which, in effect, is a negative going voltage at the plate of V2A. This negative-going signal is coupled to the grids of Vl, causing the difference in potential between the grids and cathodes of V1 to

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increase. This difference in voltage between the grids and cathodes of V1 is the operating bias for V1. Thus, as a result of this bias voltage increase, the effective internal resistance of V1 increases. When the internal resistance of V1 increases less load current flows through V1, the voltage drop across V1 increases, and the output voltage of the regulator circuit decreases to its original value.

The actions described in the preceding paragraphs are practically instantaneous; consequently, the output voltage, Eout, remains practicality constant. Since all the load current must pass through the series regulator tube, VI, the tube must be capable of passing considerable current. In some circuit applications where the load current requirements exceed the capabilities of a single tube, two or more identical tubes are connected in parallel (as the sections of **twin**triode V1 have been paralleled) in order to obtain suitable regulation characteristics and currenthandling capability.

The output of the regulator circuit is coupled to the grid of pentode amplifier V3 through coupling capacitor C2. Any ripple component present in the output voltage is amplified in the regulator amplifier, and, since the circuit is basically a negative-feedback circuit, the ripple component is suppressed. As a result, the dc regulator circuit is sensitive to any voltage changes and is very effective in removing any fundamental ripple-frequency component which is present in the regulated voltage output. Although there are many variations in the regulator-amplifier circuit configuration, the function of the dc regulator circuit remains the same, that is, to supply a regulated output voltage to the load which is independent of variations in the input voltage or changes in the load current.

# Failure **Analysis**,

**General.** The dc regulator using a pentode and a twin-tnode regulator amplifier includes several components which are rather critical and directly affect the operation of the regulator circuit. For this reason, the **resistors** in the **regulator-amplifier** circuit are normally close-tolerance (on the order of 1, 2, or 5 percent) resistors with good temperature stability characteristics. The operation of the circuit will be impaired if these resistors should change in value for any reason. Since the regulator circuit attempts to hold the output voltage constant, it is usually good practice to determine whether the load current is within

tolerance before suspecting trouble within the regulator circuit proper. A load-current measurement may be made by inserting a milliammeter (having a suitable range) in series with the output of the regulator circuit. Also, a voltage measurement should be made at the input to the regulator circuit to determine whether the unregulated voltage output from the power supply (and falter circuit) is within tolerance.

No Output. In this dc regulator circuit, the nooutput condition is likely to be limited to one of the following possible causes: the lack of filament voltage applied to series regulator tube VI, the lack of applied dc voltage (from the associated power supply and filter circuit), or a short-circuited load (including output capacitor C4). A visual check of the glassenvelope series regulator tube, V1, should be made to deteirnine whether the filament is lit; if the filament is not lit, it maybe open or fdament voltage may not be applied. The tube filament should be checked for continuity; also, the presence of filament voltage at the tube socket should be determined by measurement. The dc voltage applied to the regulator circuit should be measured at the input (plate of Vl) to determine whether it is present and of the correct value, since the lack of input voltage from the associated power supply and lilter circuit will cause a lack of output voltage. With the dc voltage removed from the input to the circuit, resistance measurements can be made across the load to determine whether the load circuit, including capacitor C3, is shorted. (The resistance measured across the load circuit will normally measure something less than the total value of the voltage-divider resistors, depending upon the load circuit design.)

**High Output.** The high-output condition is usually caused by a decrease in operating bias for the series regulator tube, V1, which, in turn, causes the tube to decrease its internal resistance and permits the regulator output voltage to rise above normal. Therefore, any defects in the **electronic** regulator circuit which can cause a decrease in the operating bias for VI should be suspected. Voltage measurements should be made at the socket of V1 to determine whether bias (cathode-to-grid) voltage is present.

A visual check of the gas-filled regulator tubes, V4 and V5, which provide the reference voltages for the operation of pentode amplifier V3, should be made to determine whether the tubes are conducting. A voltage measurement made between the plate and cathode of V4 or V5 will determine whether sufficient voltage is present at the tube to cause conduction. If the voltage is above normal, the tube maybe defective. If the voltage measured across V4 is below normal, it is likely that resistor R10 or RI 1 is open. A below-normal voltage measurement across V5 will indicate that resistor R12, R13, or R14 is probably open.

A visual check of regulator-amplifier tubes V2 and V3 should be made to determine whether their **fila**ments are lit; if the **filaments** are not lit, they may be open or the filament voltage may not be applied. The tube filaments should be checked for continuity; also, the presence of fdament voltage at the tube sockets should be determined by measurement.

The bias voltages applied to V2 and V3 should be measured to determine whether these tubes are improperly biased, causing the operating bias on V1 to decrease. Assuming that V4 and V5 are conducting normally to provide the proper reference voltages, if the voltage at the grid of V2A or V3 is below normal, there will be an increase in the bias on the respective tube. In this case it is possible that resistor R6 or R7 has changed in value to increase the bias of V2A, or that resistor R12, R13, or R14 has changed in value to increase the bias of V3; in addition, an improper setting of variable resistor R13 will affect the bias voltage at the grid of V3. If V2A or V3 is biased to cutoff, VI will be made to conduct heavily as a result of the decreased operating bias. In this case, it is likely that resistor R6 is open to cut off V2A, or that resistor R12 or the top portion of resistor R13 is open to cut off V3.

A high output from the regulator will also result when the voltage at the grid of V2B is above normal, thereby causing a bias decrease on this stage. This condition will result when pentode amplifier V3 is in cutoff because of a floating control grid or open cathode circuit. In" the case of a floating control grid, it is likely that the bottom portion of resistor R13 or resistor R14 is open; and open cathode circuit of tube V3 will result if resistor RIO or RI 1 is open.

If the differential amplifier tube, V2, has low emission, the voltage drop across V2A plate-load resistor RI will be below normal; therefore, the bias of VI will be decreased and a high output from the regulator will result. An open cathode resistor, R8, will produce the same effects as a defective differential amplifier tube.

Low **Output. The** low-output condition of the reg- — ulator is usually caused by an increase in operating

bias for the series regulator tube, VI, which, in turn, causes the tube to increase its internal resistance and permits the regulator output voltage to fall below normal. Therefore, any defects in the electronic regulator circuit which can cause an increase in the operating bias for V1 should be suspected. Trouble in one section of V1 (such as low cathode emission or an open tube element) will cause a reduction in the output. Voltage measurements should be made at the socket of V1 to determine whether the bias (cathode-to-grid) voltage is excessive. The equalizing resistors, R4 and R5, in the cathode circuits of V1 should **be** measured to determine that neither one is open, that they have not increased in value, and that they are of equal resistance.

A visual check of the gas-filled regulator tubes, V4 and V5, which provide the reference voltages for the operation of the pentode amplifier circuit, should be made to determine that the tube is conducting. A voltage measurement made between the plate and cathode of V4, and also between the plate and cathode of V5, will determine whether sufficient voltage is present at the tube to cause conduction. If the voltage measured across V4 is below normal, or if no voltage is present, it is likely that capacitor C1 is either leaky or shorted. A below-normal voltage measurement across V5 will indicate that capacitor C2 or C3 is probably either leaky or shorted.

The bias voltages applied to V2 and V3 should be measured to determine whether these tubes are improperly biased, causing the operating bias on VI to increase. Assuming that V4 and V5 are conducting normally to provide the reference voltages, if the voltage at the grid of V2A or V3 is above normal, there will be a decrease in the bias on the respective tube. In this case, it is possible that resistor R6 or R7 has changed in value to decrease the bias of V2A, or that resistor R12, R13, or R14 has changed in value to decrease the bias of V3; in addition, an improper setting of variable resistor R13 will affect the bias voltage at the grid of V3. If V2A or V3 is biased by a high positive voltage on its grid 'so that either tube conducts heavily, VI will be made to conduct less as a result of an increased operating bias. In this case, it is likely that capacitor C2 is leaky or shorted, thus placing a high positive voltage on the grid of V3. A high positive voltage will be placed on the grid of V2A if resistor R7 is open.

If plate-load resistor R1 (for differential amplifier V2) is open, the bias voltage applied to the grids of

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VI will be made larger, causing a decrease in the regulator output. Also, if tube V2 is shorted and conducting heavily, the voltage drop across plate-load resistor RI w-ill be excessive. If pentode amplifier tube V3 has high emission, the voltage drop across its plate-load resistor, R9, will be above normal; therefore, the bias of V2B will be increased, thus causing an increase in the bias of VI and a decrease in the output of the regulator. If resistor R9 is open, the cathode follower (V2B) control grid will be floating; this will cause the cathode follower to cut off. As a result, the regulator output will decrease.

As mentioned previously, excessive load current can cause the output voltage to be low, especially if the load current exceeds the maximum rating of series regulator tube V1 (resulting in excessive voltage drop across V1) or if the load **current** exceeds the rating of the power supply (resulting in a decrease m the applied voltage). For these reasons, output capacitor C4 should be checked to determine whether it is satisfactory. A leaky output capacitor could result in reduced output voltage, although the **regulator**amplifier circuit (V2 and V3) may be finctioning normally but still be unable to compensate for the decrease in output.

**Poor Regulation Characteristics. Voltage instabil**ity, slow response, etc, are frequently caused by weak or unbalanced triode sections in series regulator tube VI, unbalanced cathode resistors R4 and R5, or defective regulator amplifier tubes V2 and V3. The gain of the regulator-amplifier stage is determined primarily by tubes V2 and V3 and their applied voltages; therefore, the condition of V2 and V3 and the applied voltages are important factors governing satisfactory operation of the regulator circuit.

# BASE-CONTROLLEII REGULATOR (SEMICONDUCTOR)

## Application.

**The** base-controlled transistor regulator is used as a voltage regulator in electronic equipment where more precise voltage control is required.

# Characteristics.

Is smaller, weights less, and provides better reliability and **performance** than the electron tube regulator.

Efficiency is higher than the shunt-type regulator. Requires a reference voltage source for control purposes. Control amplifier provides more precise regulation. Series transistor is subject to damage by heavy overload or short circuit, except where protective provisions are included with the circuit.

# Circuit Analysis.

**General. The** base-controlled regulator uses a dc amplifier to control the conductivity of a seriesconnected transistor regulator. The dc control amplifier is controlled by base bias variations which, in turn, vary the base bias of the series regulator accordingly. Use of the control amplifier improves the sensitivity of the regulator and helps to stabilize output voltage variations. The control transistor must be large enough to carry only the base current, but the series transistor must be rated for full-load capability.

**Circuit Operation.** The schematic of a typical base-controlled regulator is shown in the accompanying illustration.



**Base-Controlled Regulator** 

Breakdown diode CR1, together with currentlimiting resistor R4, supplies a constant voltage reference source to the emitter of Q1. Transistor Q1 is the regulator control **amplifier** whose base is biased by a fixed voltage divider, consisting of RI and R3, connected across the output. Resistor R2 functions as the collector resistor for control transistor Q1, across which the bias for the base of series regulator transistor Q2 is developed.

During normal operation, resistor R4 provides a resistance low enough to keep breakdown diode CR1 conducting sufficiently to develop its rated breakdown voltage. Thus, the emitter of transistor Q1 is held at a fixed positive bias voltage. The resistive voltage divider, composed of R1 and R3, provides a nega-

tive (forward) base bias to control transistor Ql, which causes sufficient conduction to keep the current flow through Q2 at a value which produces the desired nominal regulated output voltage.

Assume for the moment that the output voltage tends to rise; an increasing negative voltage will appear across R1 and bias Q1 further in a forward direction to cause the collector current of QI to increase. Electron flow wiU develop a positive voltage across collector resistor R2 and reduce the base bias of Q2. When the base bias of series regulator transistor O2 is reduced, less emitter current flows and the effective internal resistance of O2 is increased. Thus, the load current flowing through Q2 produces a larger voltage drop between the emitter and collector, and causes the output voltage to decrease and return to its original value. Conversely, when the output voltage tends to drop, the base bias on Q1 is reduced, and causes the collector current of Q1 to decrease. A decreased flow of current through collector resistor R2 allows the collector voltage of Q1 to increase in a negative direction toward the supply value. Hence, the base of series regulator transistor Q2 is biased more negative and causes the emitter current of Q2 to increase. The increased current flow from collector to emitter of Q2 effectively reduces the internal resistance offered between collector and emitter and reduces the voltage drop across the transistor caused by load current. Thus, the output voltage rises back toward its normal value.

By connecting breakdown diode CR1 and resistor R4 across the regulated output voltage, instead of the supply voltage, a more stable reference voltage is obtained, and more precide control is achieved. If the amplification of control transistor Q1 is sufficient, ripple voltage variations, as well as ordinary load variations, will be compensated for, providing more precise regulation. If necessary more than one control amplifier may be used by connecting them in tandem.

### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe the proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output**. Lack of line voltage, an open transistor Q2, or a defective control amplifier circuit can cause loss of output. Check the line voltage to make certain that a blown primary fuse is not at fault. Measure the voltage across CR1 to determine whether the breakdown diode is operational, and measure the resistance of RI, "R2, R3, and R4. If control amplifier **Q1** is shorted, the base bias on Q2 will probably be sufficient to bias off Q2 and prevent an output voltage. If Q1 is satisfactory, and no output appears, Q2 is probably defective.

Low Output. A constant low output voltage can result from low line voltage, a defective series transistor Q2, or a defective control circuit. Check the line voltage. If the output voltage is still low, check the breakdown voltage across CR1 and the base bias of Q1 and Q2. If the breakdown voltage of CR1 is normal, but the base bias of QI is higher than normal, measure the values of R1 and R3. If CRI voltage is other than normal, measure the value of R4 and check CR1. If the base bias on Q1 is normal, measure the base bias of Q2. If this bias is lower than normal, measure the value of R2. If resistor R2 is satisfactory, then Q1 is drawing less than normal current, and with fixed emitter bias and normal base bias, indicates a change of characteristics in Q1. If all parts check satisfactory but a low output still exists, the regulator is probably overloaded. Series transistor Q2 will become overheated and eventually fail.

**High Output.** If the output voltage is continuously higher than normal, it indicates that series transistor Q2 is conducting heavily and offering little resistance. Such a condition can be caused by a high forward base bias or a shorted transistor. If the base bias of Q2 is higher than normal, the trouble is in the control circuit. If the base bias of Q2 is normal or lower than normal, the transistor may be defective. With a higher than normal base bias on Q2 check the value of R2 to make certain it has not decreased. If R2 is satisfactory, low collector current in Q1 is indicated. Either RI or R3 has increased in value or Q1 is defective. Measure the values of R1 and R3. If the resistors check normal, **Q1** is probably defective.

# EMITTER-FOLLOWER REGULATOR (SEMICONDUCTOR)

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# Application.

**The** emitter-follower regulator is commonly used as a voltage regulator in electronic equipments.

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## Characteristics.

**Is** smaller, weighs less, and provides better reliability and performance than the electron tube regulator.

Efficiency is high.

Requires a reference voltage source.

Transistor must be capable of carrying full-load current.

Transistor may be easily darnaged by an overload or short circuit.

May be used with a control amplifier for more precise regulation.

#### Circuit Analysis.

**General. The** emitter-follower regulator may be controlled by a Zener or breakdown diode, or by a dc control amplifier. The control **amplifier** may be basecontrolled, or emitter-controlled. It is always connected as a series regulator; units may be paralleled for high current-carrying capacity. The base voltage or current is used to drive the unit into heavy conduction when a low series resistance and higher output voltage is desired, or to reduce conduction to produce a high series resistance and lower the output voltage. Normally, it operates at the middle of its **range** to produce the nominal output voltage.

**Circuit Operation. The** schematic of a typical emitter-follower regulator is shown in the accompanying illustration.



Emitter-Follovver Regulator

As shown in the schematic, resistor R1 and breakdown diode CR1 form a voltage divider across the input which determines the base-emitter bias of transistor Q1. Transistor Q1 is comected as an emitterfollower to drive the base of series regulator transistor Q2, which is also connected as an emitter-follower. Resistor R2 stabilizes the emitter bias of transistor QI, while R3 ensures that a minimum emitter current in Q2 will always flow, even though the load current may drop to zero.

In normal operation, breakdown diode CR1 is isolated from regulator transistor Q2 by emitter-follower control stage Q1. Resistor RI is chosen to have a value which permits breakdown diode CRI to operate constantly, and maintains the base of O1 at a fixed reference voltage. Emitter resistor R2 maintains an essentially constant minimum current through Q1 and stabilizes the base bias for regulator transistor O2. When the emitter output voltage of O1 increases, the bias voltage between base and emitter is reduced, less current flows through Ql, and the voltage drop across QI is increased, lowering the emitter output voltage. Similarly, when the emitter voltage of Q1 becomes lower than normal, the base-emitter bias increases and produces a greater flow of emitter current. Hence, the internal effective resistance between collector and emitter is decreased, the voltage drop across the transistor is less, and the emitter output voltage increases. Thus, the base bias voltage to transistor Q2 is stabilized with respect to the reference voltage produced by breakdown diode CRI, and transistor Q1 need only supply the base current for regulator transistor Q2.

Normally, the base bias on Q2 produces sufficient emitter current flow to produce an effective internal collector-emitter resistance sufficient to drop the source voltage at the collector to the nominal output voltage value. When the output voltage tends to increase because of a reduction in load, the emitter voltage of Q2 increases; the value of the base-emitter bias is lowered (since the base voltage is fixed), producing a reduced flow of emitter current through Q2. In this manner, the internal collector-toanitter effective resistance is increased, producing a greater voltage drop across the transistor. The output voltage is reduced accordingly. Conversely, when the output voltage decreases, the forward base-to-emitter bias is increased and causes a greater forward flow of current. Hence, the effective collector-toenitter internal resistance is decreased, the voltage drop across the transistor is reduced, and the output voltage is increased accordingly. Emitter resistor R3 is in parallel with the load and determines minimum emitter current flow at no-load. The major function of resistors

R2 and R3 are to determine minimum emitter current flow, and hence limit the minimum output voltage to the desired value.

Actually, these resistors are not absolutely required for operation of the regulator, since the two transistors will operate in tandem in a super-alpha connection without them. When these resistors are used, slightly better regulation is obtained.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful rdso to observe the proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. If RI opens, breakdown diode CR] is shorted and transistor Q1 or Q2 is defective; or if R2 or R3 is shorted, no output will occur. Measure the input voltage to determine that a blown line fuse is not at fault. In addition, measure the voltage across R1 and CR1. If no voltage is measured across  $R_1$ , either CR1 or R1 is open. Check the resistance of RI, and check CR1. With normal base voltage applied to Q1, check the voltage across R2. If no voltage exists, either Q1 is defective, or R2 is shorted, and no output will be obtained from Q2. Measure the value of R2, and check the forward and reverse resistance of Ql, If the forward and reverse resistance both are high, Q1 is probably defective. With normal base voltage on Q2 and no output, either Q2 is defective or R3 is shorted. Measure the value of R3, and check the forward and reverse resistance of Q2. If both the forward and reverse resistance of Q2 is high, Q2 is probably defective. Where a regulator is connected to a power supply filter, do not neglect the fact that the input capacitor of the filter can be shorted, and make R3 appear to be shorted.

Low Output **Voltage**. If the input voltage is low, or the base-emitter bias of Q1 or Q2 is reduced, a low output voltage can exist. Check diode CR1 and measure the value of R1. Measure the value of R2 and R3 and check transistors Q1 and Q2 for a higher than normal forward resistance. Do not neglect to check the load current, since it is possible that the range of the regulator is being exceeded. This will usually be indicated by the operation of Q2 at a higher than
normal temperature. If prolonged, this will lead to damage or burnout of the transistor.

**High Output Voltage.** If the output voltage is continuously higher than normal, it indicates that the voltage drop across Q2 is lower than normal because of excessive current flow, producing a lower effective internal resistance. If Q1 is defective, a larger than normal forward bias may be applied to Q2. Likewise, if Q2 is defective, a greater than normal emitter current can flow. If resistor R3 increases in value or opens, the minimum voltage may change, but the output voltage will not increase to a higher value. On the other hand, if R3 decreases in value, it will tend to increase the output voltage.

# CONSTANT-CURRENT REGULATOR (SEMICONDUCTOR)

#### Application.

**The** constant-current regulator is used in electronic equipment to supply a constant current from a voltage source, regardless of load or voltage changes.

## Characteristics.

Utilizes the **constant-current** characteristics of a triode transistor biased by a fixed base current.

Current regulator is connected in series with the load.

Voltage changes across a resistor are used to sense the proper control action against a reference voltage source.

Circuit is designed to produce a relatively constant high-output impedance.

## Circuit Analysis.

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**General.** In a voltage regulator, the attempt is made to reduce the output impedance to produce the smallest possible voltage variation, while the current regulator uses exactly the opposite approach. It is constructed to produce the highest possible output impedance, so that only fractional current changes are produced by large voltage variations. Instead of sensing the output voltage changes, the regulated current is passed through a series resistor and the voltage developed across the resistor is compared with a reference voltage source. Any voltage difference is amplified and applied to a series-regulating transistor which completes the regulated feedback connection by controlling the regulated current flow. The simpler types of current regulator use the series transistor itself to supply the amplified error voltage, while the more complicated types use a separate control amplifier to control more precisely the output of the regulating transistor.

**Circuit Operation.** The schematic of a typical series current regulator is shown in the accompanying illustration.



Series Current Regulator

Breakdown diode CR1 provides a source of reference voltage against which any current changes are compared. Resistor R2 limits the current through CR1 to a reasonable value which produces a constant voltage across the diode. Resistor RI acts as the current-sensing resistor which develops the comparison voltage.

Since resistor R1 is connected in series with the emitter of Q1, current flow produces a voltage drop across RI which varies directly with the amount of current drawn by the load. Normally, breakdown diode CRI provides a constant voltage which holds the base of **Q1** at a fixed bias value. The absolute value of bias is determined by the difference between the fixed base bias and the voltage developed across emitter resistor R1 by current flow. With a constant current flow, a constant bias is developed. Should the emitter current tend to increase, a larger voltage drop occurs across R1 and reduces the forward bias. Consequently, less current flows and the output current is returned to its normal value. Should the current tend to decrease, the voltage drop across R1 is decreased and the forward bias is increased, causing a greater flow of current and returning it back to normal. Although the current is held to a relatively constant value, the voltage may vary widely. Where better performance is required, or where only very small current changes occur, a dc control amplifier may be

added. In this type of regulator, the error voltage produced by the difference between the voltage drop across the sensing resistor and the reference source is amplified and applied to control the base of the regulator.

## Failure Analysis.

**General. When** making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe the proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output. If RI, or R2, or Q1 are open, no** current can flow. First measure the line voltage to make certain that a blown fuse is not at fault. Then measure the resistance of RI and R2. If both resistors are satisfactory, check for normal voltage across CRI. If no voltage appears across CR1 and R2 is of the proper value, CR1 is probably defective. If R1 is of the proper resistance and the voltage across CR1 is normal, but there is still no output, transistor Q1 is probably defective.

**Improper Output.** If the value of R1 changes, or if diode CR1 or transistor Q1 changes characteristics, an improper output will result, If the change produces a lower than normal bias, the output will be reduced. If a higher than normal bias is produced, the output will be increased.

# CURRENT-LIMITED SERIES VOLTAGE REGULATOR (SEMICONDUCTOR)

#### Application.

**The** current-limited series voltage regulator is used as a regulated voltage supply for electronic equipments; it has a maximum current output limitation. This circuit is used to provide overload protection.

#### Characteristics.

Circuit output drops when a maximum output level is reached.

Voltage is constant up to the current limit.

Provides protection from current overload.

Base bias of **regulator** transistor is used to control output.

#### Circuit Analysis.

General. The current-limited series regulator operates as a conventional series constant-voltage regulator up to a specific current level, after which it operates effectively as a constant-current generator. Since the series voltage regulator is subject to instant damage in case of a short circuit or severe overload, the current-limiting feature automatically provides overload protection. Because circuit opening overload devices can cause voltage spikes or transients which can easily damage transistors, the current-limiting regulator circuit offers a more suitable arrangement for transistorized power supplies and regulators. Current limiting is usually accomplished by developing a control voltage which operates a diode and control transistor that reduce base current to the regulator diode and thus reduce the output.

**Circuit Operation.** The schematic of a simple current-limited voltage regulator is shown in the accompanying illustration.



#### Currant-Limited Saries Voltage Regulator

Examination of the schematic shows that the series regulator circuit is identical with the circuit described as the Base-Controlled Regulator, discussed earlier in this section of the handbook, except that a protective circuit involving transistor Q3, sensing resistor  $\mathbf{R}_s$ , and switching diode CR2 has been added. Transistor Q1 is the series-regulating transistor, and Q2 is the control amplifier, with R2 as its collector resistor. Resistors RI and R3 form the base bias voltage divider for control amplifier Q2, while breakdown diode CR1, together with current-limiting resistor R4, hold the emitter of Q1 at a fixed reference potential.

In normal operation, the base bias of control amplifier Q2 is varied above or below its normal value when the output voltage across R1 and R3 varies correspondingly. When the base bias of Q2 is increased, a larger collector current flows and develops a positive base bias across R2, which is applied to regulate Q1. A positive base bias on Q1 reduces current flow and increases the internal resistance between the emitter and collector of Q1, and the output voltage is reduced accordingly. Conversely, when the base bias increases, O1 conducts heavier and a lower resistance between emitter and collector occurs, permitting the output voltage to increase. This is the normal operation of the voltage regulator, discussed in more detail in the Base-Controlled Voltage Regulator circuit description which appears earlier in this section of the Handbook. In this regulator circuit there is no protective arrangement, so that an overload or short circuit on the output will cause low output voltage, cause the base bias of Q1 to be increased to provide heavier current, and reduce the effective series resistance of the regulator. Hence, Q1 may be easily overloaded and burnt out.

It is at this **point** that the protective circuit consisting of Q3, CR2, and sensing resistor R<sub>e</sub> begins to operate. Normally, switching diode CR2 is backbiased by leakage current through transistor Q3, and as the current through sensing resistor  $\mathbf{R}_{s}$  increases, a positive voltage drop is produced across the resistor. At a **definite** current value, the voltage on the anode of CR2 becomes greater than the voltage applied to the cathode and forward-biases the diode into conduction. The emitter of Q3 is thus switched to a positive potential with respect to its base, produced by the voltage developed across  $\mathbf{R}_{\mathbf{s}}$ . The greater the emitter bias, the larger is the flow of collector current in Q3. Since the collector voltage of Q3 is supplied through R2, a positive base bias is developed on Q1 and automatically reduces cument flow through Q1. Reducing the base bias of Q1 produces a higher effective collector-to-emitter resistance in Ql, and thus effectively places more resistance in series with the output. Hence, current flow through Q1 and  $\mathbf{R}_{s}$  is restricted to a definite maximum value.

Actually, R2 is not essential to the operation of this circuit, since a flow of collector current through Q3 can also be obtained by reducing the collector current of Q2 and the base current of Q1 (if R2 is not used). A reduction of base current in Q1 means a reduction of drive, with a consequent reduction of emitter current. When the overload is removed from Ql, the voltage on the anode of diode CR2 drops as the voltage across  $\mathbf{R}_{s}$  decreases, until CR2 is again back-biased and effectively switched off. As a result, Q3 ceases conducting and returns the base bias of Q1 back to normal. Once again, Q2 resumes control of Q1 and regulates the output voltage. The current-limiting circuit operates only in one direction because of the switching action of diode CR2; Q3 remains inoperative until CR2 is forward-biased by excess current flow through Rs. Although the voltage drop across the series resistor will reduce the output voltage, it is usually on the order of a volt or two at maximum value, so that it has little effect on the total amount of output voltage.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube **voltmeter** to avoid the low values of shunting resistance employed on the low-voltage **ranges** of conventional voltmeters. Be careful also to observe the proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** Lack of line voltage, an open transistor Q2 or series resistor Rs, a defective transistor Q3, or a defective control **amplifier** can cause loss of output. Check the line voltage to make certain that a blown primary fuse is not at fault. Measure the voltage across CR1 to determine whether the breakdown diode is operative; measure the resistance of R1, R2, R3, R4, and  $\mathbf{R_s}$ . If control amplifier Q2 is shorted, the base bias on Q1 will probably be sufficient to bias off Q1 and prevent an output voltage. Transistor Q3 may also be defective and biasing off Q1.

Low **Output.** A constant low output can result from low line voltage, a defective series transistor Q1, a defective control circuit, or a defective protective circuit. Check the line voltage. If the output voltage remains low, check the breakdown voltage across diode CR1 and check the base bias of Q1 and Q2. If the breakdown voltage of CR1 is normal but the bias of Q2 is higher than normal, measure the value of RI and R3. If the **voltage** of CR1 is other than normal, measure the value of R4 and check CR1. If the base bias is normal on Q2, measure the base bias on Q1. If this bias is lower than normal, measure the value of R2. If resistor R2 is satisfactory, the protective circuit may be faulty. If CR2 is excessively leaky or shorted, it will cause Q3 to operate and automatically

reduce the output. If the output still remains low, there is the possibility that control **amplifier** Q2 is defective.

**High Output.** Ordinarily, a defective control circuit or a defective series transistor Q1 can cause a high output. Such action is dependent upon heavier than normal conduction of Q1 to create a lower effective internal resistance from the emitter to the collector. With a current-limiting protective circuit, however, such a condition cannot happen except for currents which are lower than the limiting value, or unless the current-limiting circuit is inoperative. Q1 may be defective, or resistors RI, R2, R3 and R4, and diode CR1, or transistor Q2, may also be faulty.

# HIGH-VOLTAGE SERIES STACK REGULATOR (SEMICONDUCTOR)

## Application.

**The high-voltage** series stack type voltage regulator is used to regulate high voltage which exceeds the rated value for a single transistor. It is utilized in all types of semiconductor equipment using high-voltage power supplies.

## Characteristics.

Each series stack transistor is of the same type, with equal voltage breakdown and **current** ratings.

A voltage divider is used to distribute the voltage equally across each transistor.

Only one stack transistor is directly controlled by the regulator circuit.

Uses a breakdown diode to ensure equal voltage distribution across each stack transistor.

Series regulator may use any type of control circuit.

# Circuit Analysis.

General. When a high voltage which exceeds the transistor voltage rating is to be regulated, voltage breakdown may be prevented by using a number of series-connected transistors, in a stack arrangement, to reduce the voltage across each transistor to a value within the rating. A conventional **base-controlled** (or other type) series regulator is used to provide the voltage regulation, while the series stack of transistors is used to divide the high voltage equally across them. The simpler types use a resistive voltage divider to help equalize the voltage across each transistor of the

series stack. The more complicated circuits may use additional transistors to produce equal voltage distribution, and in addition, to provide temperaturecompensating circuits.

**Circuit Operation.** A schematic of a typical highvoltage series stack regulator is shown in the accompanying illustration.



High-Voltage Series Stack Voltaga Regulator

The high voltage transistor stack consists of transistors QI, Q2, Q3, and Q4. Resistors RI, R2, R3, and R4, together with breakdown diode CRI, form a group of equalizing resistors connected as a series voltage divider. Resistor R5 is the collector resistor for control transistor Q5. Resistors R6 and R7 forma base bias voltage divider across the regulated output for control amplifier Q5. Resistor R8 is a currentlimiting resistor for breakdown diode CR2, which holds the emitter bias of Q5 at a fixed value.

In normal operation, the base bias on transistor Q5 varies in accordance with the output voltage; when the output voltage increases the forward base bias also increases, and when the output voltage drops the forward bias decreases. As the forward bias increases, the collector current of Q5 also increases, and produces a positive voltage drop across R5. Thus a reverse bias is placed on the base of Q4. Since the base of Q4 is directly connected to the collector of Q5, an increase in collector current is obtained both through R5 and by reducing the base current of Q4. Reducing the base current of Q4 reduces the drive and has the same effect as reducing the base bias. — Therefore, increasing the collector current of the Q5

 control transistor reduces the base voltage and drive current of the Q4 regulator and reduces conduction. The reduced flow of emitter and collector current through Q4 effectively increases the internal ernitterto-collector resistance and **produces** a greater voltage drop across the transistor, reducing the output voltage.

> When the output voltage drops, the forward bias applied to the base of Q5 from voltage divider R6 and R7 also reduces, and causes a reduction in collector current. The collector voltage of Q5 increases negatively, rising toward the supply voltage as the current flow through R5 decreases. Consequently, an increasing negative bias is applied to the base of regulator transistor Q4. The increased forward bias on Q4 causes an increased emitter current flow which reduces the effective internal resistance between the emitter and collector of Q4. Hence, less voltage drop occurs across the transistor, and the output voltage increases back to normal, Since all transistors in the stack are connected in series, the same current flows through each transistor. Therefore, it is only necessary to control directly one transistor (Q4) to control current flow through the stack.

Resistors RI, R2, end R3 are of equal value and are series-connected with R4 and breakdown diode CR1; therefore, a current determined by the total voltage drop across the stack (difference between input and output voltages) will flow through each resistor, With equal resistances and the same series current flow, equal voltage drops appear across each resistor. Thus, the bases of Ol, O2, and O3 have equal voltages applied, and R4 is chosen in conjunction with CR1 also to have an equal drop. Breakdown diode CR1 keeps the emitter of Q4 at a freed voltage with respect to the base of Q3. Thus, when the output voltage increases, the voltage across the stack increases, and the collector-to-base voltage across each of the stack transistors increases. Since equal voltages appear across resistors Rl, R2, and R3, equal voltages appear across transistors Q1, Q2, and Q3. Likewise, since R4 and CR1 are chosen to produce an equal voltage drop, the same drop appears across Q4, less the amount of breakdown voltage of CR1. Thus, the collector of Q4 and the emitter of Q3 are held at a small voltage difference from the emitter of Q4; it is this difference which provides the collector voltage for the regulator action of Q4. Consequently, the voltage drops across the four transistors are practically identical. When the control amplifier operates to

lower the base bias of Q4 and reduce the output voltage, the voltage across the stack is automatically reduced. With a lower collector-to-base voltage appJied to Q1, Q2, and Q3, the base bias on these transistors is also reduced, and equal reduced current flow through each stack transistor produces approximately equal voltage distribution across each of the transistors.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional **volt-ohmmeters**. Be careful also to observe proper polarity when checking continuity since a forward bias through any of the transistor **junctions** will cause a false low-resistance reading.

No Output. An open-circuited series stack, defective transistors, breakdown diodes, or regulator control circuit can cause loss of output. If any of the series stack transistors is defective, the series circwt will be open and the only output will be the small output across breakdown diode CR1. Measure the line voltage **first** to be certain that a blown supply fuse is not at fault. Measure resistors Rl, R2, R3, and R4 to determine if they are within tolerance. If there is input voltage present at the emitters of Q1, Q2, and Q3, but not at Q4, the control circuit is probably at fault, causing Q4 to be cut off. Transistor Q5 is most probably shorted.

Low Output. If transistors Ql, Q2, Q3, or Q4 are open, only the small breakdown voltage across CR1 will be obtained at the output. Check the line voltage to make certain the input is normal and that the power supply is not at fault. If either Rl, R2, R3, or R4 is open the voltage will be below normal; check the resistance of each resistor for proper value. If diode CR2 is open, the bias on Q5 maybe sufflcient to reduce the output of Q4. Check diode CR2 and check the value of resistor R8. If R6 or R7 changes in value, the base bias of Q5 may be changed and cause a low output. Measure the values of R6 and R7; if they are satisfactory, regulator control transistor Q5 may be defective. Also check the value of collector resistor R5, as it may be open; in which case, Q5 can operate only by reducing the drive on the base of Q4.

**High Output.** A high output can be caused by one of the stack transistors shorting and producing less than the normal voltage drop. Measure the voltage from the emitter of each stack transistor to the posi-

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tive terminal to determine where the high voltage exists. Check the base bias of Q5 to make certain that it has not decreased because of a change in resistors R6 and R7. If the base bias is low, resistors R6 and R7, or transistor Q5, maybe at fault. Also, check the value of R8 and the operation of diode CR2.

# SECTION 4 FILTERS

## PART 4-1. POWER SUPPLY

# **POWER-SUPPLY FILTERS**

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While the output of most types of rectifiers is a pulsating direct current, most electronic circuits require a substantially pure direct current for operation. To provide this type of output, single- or multiple-section filter circuits (which effectively eliminate any alternating or ripple-voltage components by smoothing out the dc pulsations) are placed between the output of the rectifier and the load.

Filtering is accomplished with various combinations of resistors, inductors, and/or capacitors, usually arranged as a low pass falter. Inductor, as series impedances, oppose the flow of alternating (pulsating dc) current, while capacitors, as shunt elements, by-pass the alternating components that succeed in passing through the series impedances. (Resistors are used in the place of inductors for very low-current outputs.) The four basic types of falter circuits are the shunt-capacitor filter, the R-C capacitor-input falter, the L-C capacitor-input filter, and the LC chokeinput filter. A fifth type of **filter**, the resonant falter, employs one of the basic falter configurations in conjunction with a series-resonant, or parallel-resonant circuit.

#### Shunt-Capacitor Filters.

**The** shunt-capacitor filter (which is discussed more thoroughly later in this section) is the simplest type of falter. As shown in part A of the accompanying illustration, it consists of only a single filter element, capacitor C, connected **across** the rectifier in parallel with the load. In order to obtain good smoothing action when using this filter, the R-C time constant of the circuit should be large. Hence, both the capacitance and the load resistance should be large. Better filtering also results when the ripple frequency is high.



Shunt-Capacitor Filter and Associated Waveforms

Part B of the illustration shows the input and output waveforms of the shunt-capacitor filter, using a medium to large value of capacitance in a full-wave rectifier circuit. Capacitor C initially charges up to the peak value of the applied voltage and discharges through the load  $(\mathbf{R_L})$  between the rectified pulses. The charge and discharge of C is indicated in part A of the illustration as is the polarity of the voltage developed across the capacitor and the load.

The chief disadvantage of the shunt-capacitor falter is poor regulation, which precludes its use in most power supply applications. However, the advantages of simplicity and effectiveness recommend its use in some high-voltage applications in preference to more elaborate filters. It finds wide use in power supplies that furnish high-voltage anode potentials to cathode-ray and similar tubes where the current drain is insignificant.

## **R-C Capacitor-Input Filters.**

**The** addition of a series resistor and a second shunt capacitor to the shunt-capacitor filter results in the basic R-C capacitor-input falter, as shown in the accompanying illustration. Because of its resemblance

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to the Greek letter Pi (n), it is known as a Pisectwn falter. The input to the filter is the output voltage from the rectifier developed across input capacitor Cl. Typical waveforms of these voltages are included in the illustration.



R-C Capacitor-Input Filter and Associated Waveforms

Both the ac and dc components of the rectified current flow through series resistor R1. Because the **reactance** of C2 is small at the frequency of pulsation, most of the ac component flows through this capacitor and is bypassed to ground around the load resistor. The dc component flows through load resistor R2. The charging and discharging of C2, due to the passage of the pulsating component, results in a smoothing out of the ripple fluctuations, and a relatively pure direct current is delivered to the load, as is indicated by the output waveform.

The reduction in output voltage due to the excessive voltage drop across the series filter resistor when load current is high makes the R-C falter impracticable for most applications requiring even a moderate amount of current. This type of falter is used effectively in high-voltage, low-current applications. It is also cornmordy used as a decoupling network in multistage amplifier circuits.

# L-C Capecitor-input Filters.

**The basic L-C capacitor-input** filter has an identical configuration, and is similar in every respect to the R-C capacitor-input filter with one exception—a choke coil (iron-core inductor) replaces the series resistor in the Pi-section network, as shown in the accompanying iUustration. The LC capacitor-input filter is probably used to a greater extent than any other type of falter in power supply applications. The input to the falter section comprising L and C2 is the output voltage of the rectifier, developed across capacitor Cl. Typicrd rectifier output and capacitor Cl input voltage waveforms are included in the illustration. Inductor L and capacitor C2, working together, materially reduce the ac component remaining in the voltage across Cl, and thus supply a substantially pure dc output voltage to the load.



L-C Capacitor-input Filter and Associated Waveforms

As in the case of the shunt-capacitor falter, and also the R-C capacitor-input falter, the poor regulation of the LC capacitor-input filter is a major disadvantage. In fact, assuming equal values of C, the regulation of a power supply using an LC capacitorinput falter is actually worse than that of a power supply using a shunt-capacitor falter. An advantage of the capacitor-input filter is the provision of a much higher output voltage than can be obtained from a comparable falter of the choke-input type.

#### L-C Choka-input Filters.

With the elimination of capacitor- Cl, the L-C capacitor-input falter becomes an LC choke-input falter. This type of filter, together with the associated waveforms, is illustrated below,



L-C Choke-Input Filter and Associated Waveforms

When rectified pulses are applied to the choke coil (series inductor L), the inductance opposes any change in current through the coil. Thus, the inductance of the coil acts to oppose any increase in current during the rapid positive excursion of the pulses, as well as any decrease in current during the equally rapid negative excursion of the pulses. This action tends to keep a constant current flowing to the load throughout the cycle. Because of this, the pulsating voltage (resulting from the **inductance** effect) which is developed across capacitor C is maintained relatively constant at a value which approaches the average value of the input voltage. The low reactance presented by capacitor C to the pulsating component functions to decrease the ripple amplitude in the output and thereby to increase the average de output voltage.

> One disadvantage of the choke-input falter is the significantly lower output voltage of this type of falter as compared with the higher voltage provided by a comparable filter of the capacitor-input type. Another disadvantage, concerned with economics, is that for equivalent faltering, the choke-input filter must employ higher-value components than are required in the capacitor-input filter.

However, the advantage of lower peak currents in the choke-input system, which effects important savings in tube and transformer costs, somewhat offsets the second disadvantage mentioned in the preceding paragraph. Two additional advantages of the choke-input arrangement, in comparison with the capacitor input arrangement, are a greater power capability and much better de voltage regulation.

#### **Multiple-Section Filters.**

To further enhance the filtering action and provide a smoother rectified output voltage (beyond that possible with the simple falter circuits discussed in the preceding paragraphs), one or more additional sections may be added to the basic falter circuit. The accompanying circuits illustrate two multiple-section filters. The capacitor-input type is shown in part A, and the choke-input type is shown in part B. Representative waveforms indicating the approximate shape of the voltage at several different points in each type of multi-section falter are included in the illustration.



Multiple-Section capacitor-input and Choke-input Filters

Multiple-section filters are effective in those applications where only a minimum ripple content can be tolerated in the rectified output voltage to the load. If the ripple attenuation ratio of one LC section is 100 to 1, then an over-all 10,000 **-tg-l** attenuation ratio will be obtained with two such sections, and a 1,000,000-to-l attenuation ratio with three L-C sections. While additional filter sections do reduce the ripple component in the output to a minimum, they also result unfortunately, in reduced regulation. With additional sections, more resistance is placed in series with the power supply, which causes greater variations in the output voltage with variations in the load current. Most multiple-section filters consist of a combination of identical LC sections. However,

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multiple-section falters are not restricted to this type of design; combinations of LC and R-C sections may be used effectively to satisfy specific filtering requirements in certain applications.

## **Resonant Filters.**

Resonant falters are incorporated in the design of some power supply circuits. This type of filter is usually made up of two basic types of circuits. One common type of resonant falter uses a series-resonant (or a parallel-resonant) circuit in conjunction with one of more L-C falter sections. Another type employs a parallel-resonant circuit with shunt capacitors in a Pi-section **filter** arrangement. This **type** of resonant falter is shown in the accompanying illustration.



#### Resonant Filter

**The** parallel-resonant circuit, consisting of L and C, is tuned to the fundamental ripple frequency, and is connected in series with the output of the rectifier. Since this type of circuit presents an extremely high **impedance** at resonance, the **fundamental-ripple**-frequency component will therefore be greatly attenuated in the output voltage to the load.

Two serious disadvantages which knit the use of the resonant filter are as follows: (1) A change in the inductance of L with a change in load cirrent results in detuning of the circuit, and thus a loss in its effectiveness. (2) Harmonics see a much lower impedance than the **fundamental** ripple frequency (since the circuit is tuned to the **fundamental**), and are therefore less effectively attenuated. A conventional LC **filter** section is sometimes added to the resonant filter shown in the illustration to offset the latter disadvantage.

## Filter Output-Voltage Considerations.

**The** unfdtered output from a rectifier can be considered as a pulsating (ac) voltage superimposed on a dc voltage. The pulsating component of the rectified voltage is commonly referred to as *n"pple. l‰e* frequency components of the ripple and their amplitudes are the major factors which determine the amount of filtering required.

The accompanying illustration shows four typical rectifier output waveforms (part B, C, D, and E). For contrast, part A shows the smooth dc output of a battery. The frequency of voltage pulsation, or ripple frequency, is different for each of the rectifier output waveforms. The output of a single-phase, hrdf-wave rectifier, shown in part B, produces pulsations at the frequency of the applied ac voltage. If the applied ac voltage has a frequency of 60 Hz, the frequency of the ripple component will also be 60 Hz. The output of a single-phase, full-wave rectifier, shown in part C, produces pulsations at twice the frequency of the applied ac voltage because both alternations of the input voltage are rectified. The output of a threephase, half-wave rectifier, shown in part D, produces pulsations at three times the frequency of the applied voltage; the output of a three-phase, Ml-wave rectifier, shown in part E, produces pulsations at six times the frequency of the applied voltage. From a comparison of the four typical output waveforms, it can be seen that for an applied ac voltage of a given frequency, each of the rectifier circuits produces a different ripple frequency. Also, it will be noted that when the output pulses overlap (as shown in parts D and E), an increase in ripple frequency results in a decrease in ripple amplitude. As the ripple frequency is increased and the ripple amplitude is decreased, the rectifier output becomes easier to filter.





It is desirable to furnish a voltage to the load which is free from any ripple component; however, there are several practical limitations (over-all regulation characteristics of the power supply; size, weight, and design of filter components; cost of components; etc) which influence the extent of faltering which is possible. Furthermore, the equipment design may tolerate a small percentage of ripple without any adverse effects upon equipment performance. As a result, the faltered output from the rectifier circuit may contain a small amount of residual ripple voltage which is applied to the load circuit.

Part A of the accompanying illustratio, shows a typical single-phase, full-wave rectifier system using a choke-input filter to provide dc voltage to a resistance load. The idealized curves of part B of the illustration show the shape of the output voltage from the rectifier, together with that of the voltage across the load. Since the output voltage of the rectifier can be considered as consisting of a dc component upon which is superimposed an ac ripple voltage, it can be shown that (by 'means of a Fourier analysis) the dc component of the **output** wave is 2/rr times the peak value



Single-phase Full-wave Rectifiar System and Associated Output Voltage Waveform

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of **the** ac **input** wave. The lowest frequency component of ripple in the output is twice the input frequency and two-thirds the magnitude of the dc component of the output voltage. The remaining ripple components are harmonics of this lowest-frequency component, and rapidly diminish in amplitude as the order of harmonics is increased. This is graphically illustrated in the **accompanying** tabulation, which provides pertinent characteristics of three of the four rectifiers considered in this discussion.

## Characteristics of Three Typical Rectifier Circuits Having Choke-input Filter Systems

Note: Relative voltage amplitudes are with reference to the dc component of output voltage, takan as 1.0.	Rectifier Circuit		
	Single- Phese, Full- Wave (Center- tapped)	Three- Phase, Half- Wave	Three- Phase, Full- Wave
a. RMS value of trans- former secondary			
voltage (one-half)	1.11	0.855	0.428
b. Maximum inverse			
voltage	3.14	2.09	1.05
c. Lowest frequency in rectifier outPut (F = frequency of applied ssc voltage)	2F	3F	6F
<ul> <li>d. Peak value of first three ec components of rectifier outPut (ripple frequency):</li> </ul>			
Fundamental	0.667	0.250	0.057
Second harmonic	0.133	0.057	0.014
Third harmonic	0.057	0.025	0.008
e. Ripple peaks with reference to dc axis:			
Positive peak	0.363	0.209	0.0472
Negative peak	0.637	0.395	0.0930

In addition to the ripple frequencies present and their respective magnitude, another very important factor which must also be considered is the amount factor which must also be considered is the amount (percentage) of residual ripple that can be tolerated by the equipment which uses the faltered voltage from the rectifier system. The effectiveness of the filter circuit in this respect is determined from the ratio of the rms value of the ripple voltage to the average value of the output voltage. This ratio is expressed as percentage of ripple, as follows:

Percentage of ripple= 
$$\frac{E_r}{E_{av}} \times 100$$

where: 
$$\mathbf{E}_{\mathbf{r}}$$
 = effective (rms) value of ripple  
voltage  
 $\mathbf{E}_{av}^{-}$  average value of output voltage

As a sine wave, the effective (rms) value of ripple voltage can be expressed by the following equation:

$$E_r = 0.354 \ (e_{max} - e_{min})$$

(Refer to preceding tabulation of rectifier voltage relations for percentage values of  $e_{max}$  and  $e_{min}$ .) An alternate way of stating the percentage of ripple, which may be found preferable in some instances, is (for a single-section filter) as follows:

Percentage of ripple= 
$$\frac{mX_C}{(X_L + X_C)}$$

where:  $\mathbf{X}_{\mathbf{C}}$  = falter capacitance reactance  $X_{L}$  = filter inductive reactance c =filter capacitance in microfarads L =falter inductance in henries

The factor m equals 70 for a single-phase, full-wave rectifier, 24 for a three-phase, half-wave rectifier, and 5 for a three-phase, full-wave rectifier.

For a double-section filter, the expression becomes:

Percentage of ripple= 
$$\frac{mX_C^2}{(X_L X_c)^2}$$

In a filter system, as the frequency of the applied voltage is increased (in this case a ripple voltage), the reactance of a shunt capacitor decreases and the reactance of a series inductance increases. The means that the faltering effectiveness of any **filter** made up of shunt capacitance and series inductance is increased as the frequency of the applied voltage is increased; thus, at the higher ripple frequencies, filter components of smaller size and lighter weight can be

used to provide the same degree of **filtering** as can be obtained at lower ripple frequencies with filter components of larger size and heavier weights.

#### Voltage Regulation.

**The** output voltage of a power supply decreases as the load current increases because of losses occurring in the various resistances in the rectifier and filter circuit. The accompanying illustration compares the voltage output for varying load currents from a rectifier for a simple capacitor-input filter and for a choke-iiput filter. In each case, the same type of tube and transformer are used in a center-tapped full-wave circuit to supply power to an identical resistance load. It is immediately apparent, when comparing the two curves on the graph, that while the output voltage for each value of load current is higher for the capacitor-input arrangement, the regulation of the power supply is far greater for the choke-input filter.

Further study of the curves reveals that in the case of the capacitor input, a change in load current from around 25 milliampers to 250 milliampere results in a drop in output voltage from 600 to 425 volts, or a total drop of 175 volts. For the same change in load current in the case of the choke input, the dc output voltage drops from 400 volts to 350 volts, or a total of only 50 volts (as compared with the 175 volts for the capacitor input).



Comparison of Voltage-Regulation Characteristics for Capacitor-Input and choke-input Filters

Voltage regulation is a measure of the degree to which a power supply maintains its output-voltage stability under varying load conditions. **The** amount of change in the output voltage between the no-load and full-load conditions is usually expressed in terms of the percentage of voltage regulation. The percentage of voltage regulation is defined as the ratio of the difference between the no-load and full-load output voltages to the full-load output voltage, times 100. This can be expressed as follows:

Percentage of voltage regulation= 
$$\frac{(E_1^{+}\%_{+})_{\times}}{E_2}$$
 100

where:  $\mathbf{E}_1$  = no-load output voltage  $E_2$  = full-load output voltage

An ideal power supply would have zero internal resistance (impedance), and the percentage of regulation would be zero because there would be no difference between the output voltage for the no-load and full-load' conditions. However, since this is not practicable, then the lower the percentage of regulation the better the power supply and the nearer the supply approaches an ideal supply. Well-designed power supplies generally have a regulation of 10 percent or less.

The regulation of the choke-input **filter** is always better than that of the capacitor-input falter, provided that some minimum value of load current flows through the choke at all times. Under this condition, the output voltage changes only slightly with small changes in load current. However, if the load current is reduced to approach a no-load condition, the choke cannot prevent the associated filter capacitor from charging to the peak value of the applied voltage; thus, the output voltage rises to its maximum value. If the load current is normally a low value, or if the load current varies between zero and a low value, the regulation will be poor as compared with the same circuit operating with a slightly greater load current. When this is the case, an additional load in the form of a resistor, called a *bleeder resistor*, is placed across the output of the falter to improve the regulation and establish a minimum value of load current for the supply. This minimum value of current, which flows

through the filter choke, improves the regulation of the power supply. The vahre of the current drawn by the bleeder resistor is usually 10 to 15 percent of the total current available from the supply.

The bleeder resistor across the output terminals of the power supply not only assists in maintaining good voltage regulation, but also prevents the capacitors in the filter system from charging up to the peak value of the applied voltage. In addition, the bleeder reduces the possibility of electrical shock to personnel, because the capacitors will discharge through the bleeder resistor after the power supply has been turned off. In many power supplies the bleeder resistor takes the form of a voltage divider, either a tapped resistor or a number of series resistors selected so that several values of output voltage can be supplied to various loads having different voltage and current requirements.

# Filter Capacitors.

A common type of capacitor used as a filter element in many receiver-type power-supply circuits is the dc electrolytic capacitor. Within the container of the electrolytic capacitor, rolled aluminum-foil plates are immersed in an electrolyte which is commordy an aqueous solution of **boric** acid and sodium borate. The actual dielectric in this type of capacitor is the thin oxide **film** which forms on one set of plates in the presence of a dc polarizing voltage. The aluminum foil acts as the anode (positive terminal), and the electrolyte acts as the cathode (negative terminal) of the electrolytic capacitor.

The are two general types of electrolytic capacitors-the wet type and the dry type. The physical characteristics of the electrolyte used determines the particular type of capacitor. The wet type uses an aqueous electrolyte in a metal container; the dry type uses a viscous or paste electrolyte, and is available in either a paper (cardboard) or metal container.

The most common working voltages for electrolytic capacitors (both types) run between 6 and 600 volts. Practical values of capacitance run anywhere from 1 or 2 microfarads to as high as 2000 microfarads, the particular value depending on the requirements of a given application.

In keeping with the necessity for a wide range of working voltage and capacitance values, electrolytic capacitors are available in a variety of physical sizes. Generally speaking, the higher the voltage and the greater the capacitance. the larger the physical size. For low-voltage applications, much greater capacitance is provided in units of smaller size than paper-type capacitors (which provide only about one ten-thousandth as much capacitance).

Multiple-section electrolytic capacitors, which have two or more capacitor units housed in a single container, are extensively used in receiver powersupply circuits. For example, a Pi-section filter circuit may use a dual-section electrolytic capacitor having two 8-micro farad sections, one connected on each side of the series falter element. However, the capacitance of the different sections need not be the same. In a typical three-section capacitor, for instance, each section may have a different capacitance, or two sections may have the same value and the third section of different value. Any number of combinations are possible, and standardization is the exception rather than the rule.

In addition to the electrolytic capacitor many other nonpolarized types of capacitors are in use; for example: paper-foil, wax-impregnated or oilimpregnated, oxide film, mica, and ceramic. For high-voltage applications such as transmitter power supplies, the individual units are larger and have insulated bushing-type terminals. The higher the voltage, the larger the unit for a given capacitance. Paperfoil types are generally used at voltages from 750 to 2500 volts. Oil-impregnated types are used for voltages of 1500 to 3500 volts (up to 30 kv for large commercial installations). Mica and ceramic capacitors are generally used as blocking capacitors or in tuned falters, since their size is usually limited to values less than 0.25 microfarad. Small, hand-portable equipments sometimes use series-comected receiving or low-voltage-type electrolytic capacitors for economy (the price of two low-voltage units is considerably lower than on high-voltage unit). Since the introduction of transistors, extremely low-voltage (2, 4, 6, and 12-volt) capacitors of very small physical size, with capacitance values on the order of 50, 100, and 150 microfarads or more, are in common use to supply high currents at the low voltages employed. These capacitors are used in power supplies which eliminate the necessity for, and expense of, battery replacement.

# SHUNT-CAPACITOR FILTER

# Application.

**'he shunt-capacitor** falter, as previously stated, is the simplest type of filter. The application of this falter is very limited; it is sometimes used in extremely high-voltage, low-current power supplies for cathode-ray and similar electron tubes which require very little load current from the supply. This filter is also used in applications where the power-supply ripple frequency is relatively high, e.g., to falter the output of a dynarnotor.

## Characteristics.

Capacitance and load-resistance values must be high (large R-C time constant required).

Load current must be relatively small if falter is to **have good** regulation.

Filtering efficiency increases as ripple frequency is increased.

Regulation of rectifier-type power supply is poor with this type of falter; voltage regulation depends mainly on value of capacitor.

#### Circuit Analysis.

General. The rectifier circuits previously described in this section of the handbook provide a rectitled output voltage, across the load resistance, which has a pulsating waveform. The accompanying illustration shows a simple shunt-capacitor **filter** and the waveforms obtained when the imput to the falter is obtained from either a half-wave or a full-wave (singlephase) rectifier circuit.



Shunt-Capacitor Filter end Waveforms

The waveforms given in part A of the illustration represent the **unfiltered** output (without capacitor C) from the rectifier circuit when current pulses flow through the load resistance,  $\mathbf{R}_{\mathbf{L}}$  each time the rectifier conducts. Note that the dashed line indicating the average value of output voltage,  $\mathbf{E}_{av}$  for the **half**-wave rectifier is less than half (approx 0.318) the amplitude of the voltage peaks; the average value of output voltage,  $\mathbf{E}_{av}$ , for the full-wave rectifier is greater than half (approx 0.637), but is still much less than the maximum peak amplitude of the applied waveform. With no capacitor connected across the output of the rectifier circuit, the waveform has a large value of pulsating component as compared with the average (or dc) component.

When a capacitor is comected across the output of the rectifier (across load resistor  $R_1$ ), the average value of output voltage, E<sub>w</sub>, will be increased because of the filtering action of the capacitor. In part B of the illustration a capacitor of medium value is placed in shunt (parallel) with the load resistance,  $R_1$ . The value of the capacitor is fairly large; it thus presents a relatively low reactance to the pulsating current and stores a substantial charge. The rate of charge for the capacitor is limited only by the impedance of the ac source (transformer) and the internal resistance of the rectifier, both of which are relatively low; therefore; the R-C charge time for the circuit is relatively short. As a result, when the **pul**sating voltage is first applied to the shunt-capacitor filter, the capacitor charges rapidly and almost reaches the peak voltage within the first few cycles. The charge on the capacitor approximates the peak value of the rectified voltage when the rectifier is conducting, and tends to retain its charge when the rectifier output falls to zero (since the capacitor cannot discharge immediately). The capacitor slowly discharges through the load resistance, R<sub>1</sub>, during the time the rectifier is nonconducting.

The rate of discharge for the capacitor is determined by the load resistance; if the capacitor and load-resistance values are large, the R-C discharge time for the circuit is relatively long. From the waveforms shown in part B of the illustration, it can be seen that the addition of capacitor C to the circuit results in an increase in the average value of output voltage,  $E_{av}$ , and a reduction in the ripple component,  $E_{r}$ , present across the load resistance.

As previously stated, the capacitor partially discharges through the load, dropping the output voltage until the next positive pulse occurs; when the amplitude of this pulse exceeds the value of voltage of the capacitor, the capacitor once again starts charging to the peak value.

If the value of the capacitor used in the falter circuit is increased, the average value of the output volt**age**,  $E_{av}$ , is **also** increased. In part C of the **illustra**tion, the effect of increasing the value of capacitor C (over that used in part B) is shown. The time constant of the charging circuit is still relatively short, but the time constant of the discharging circuit is considerably greater. Because of the increased discharge time constant, the large valve capacitor does not discharge as rapidly as the medium-value cap acitor; therefore, the average voltage is higher and the amplitude of the ripple component,  $E_{t}$ , is decreased.

Compare the increased filtering action shown in the waveform of part C with that of part B. 'theoretically, the shunt-capacitor filter cari provide any desired degree of filtering; the larger the value of capacitor C, the better the **filtering** action, because of the lowered impedance (XC) offered to the pulsating component and the ability of the capacitor to retain a charge longer because of the increased R-C discharge time constant. However, there is a practical limitation to the maximum value of the capacitor used in the falter. If the **peak-current** rating of the rectifier is exceeded during the charging time for the capacitor, the rectifier will be damaged; thus, a compromise in the value of the capacitor is necessary in order to keep the maximum charging current within the peakcurrent rating of the rectifier.

The load resistance is also an important consideration. If the load resistance is made small, the load current increases and the average value of output volt**age** ( $\mathbf{E}_{av}$ ) decreases. The R-C discharge time constant is a direct function of the value of the load resistance; therefore, the rate of capacitor voltage discharge is a direct function of the current through the load. The greater the load current, the more rapid the discharge of the capacitor, and the lower the average value of output voltage. For this reason, the shunt-capacitor falter is seldom used with rectifier circuits that must supply a relatively large load current.

The pulsations across capacitor C and load resistance  $R_L$ , no matter how small in amplitude, are in effect a form of distortion. **Although** these pulsations represent a fundamental frequency, many other frequency components are also present in the output. In the majority of equipment applications, the presence

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of' a ripple-voltage component is not desirable; therefore, for most equipment application it is impracticable to use a simple shunt-capacitor falter; additional filtering (or another type of falter) is necessary to reduce the ripple amplitude to an acceptable minimum.

**Circuit Operation.** Consider now a complete cycle of operation, using a single-phase, half-wave rectifier operating with shunt capacitor C and load resistance  $R_L$ , shown in the preceding illustration. Capacitor C is assumed to be large enough to insure small reactance to the pulsating rectified current. The resistance of  $R_L$  is assumed to be much greater than the reactance of C at the input frequency.

When the circuit is energized, the rectifier conducts on the positive half of the cycle, and current flows into and charges capacitor C to approximately the peak value of the input vohage. The charge is less than the peak value of voltage by the amount of the voltage drop across the rectifier tube. The charge on C is indicated by the heavy lines on the waveforms in parts B and C of the illustration.

On the negative half-cycle the rectifier cannot conduct, since the plate is negative with respect to the cathode. During this interval, capacitor C discharges through load resistance R<sub>1</sub>. The discharge of C produces the downward slope of the heavy lines in parts B and C of the illustration. In contrast to the abrupt fafl of the applied ac voltage from peak value to zero (shown in dotted lines), the voltage across C (and thus across  $R_1$ ) during the discharge period decreases at a gradual rate until the time of the next half-cycle of rectifier operation. For a given value of load current, the value of C determines the rate at which the discharge voltage decreases. This rate of voltage decline and the value, of C are inversely related. Thus the rate is greater for smaller values of C and less for greater values of C. This indicates that for the same load current, if C (or  $R_1$ ) is increased, the ripple component in the output to the load is decreased. (A longer time constant requires a longer time to charge and discharge.)

Since practical values of C and  $R_L$  insure a more or less graduaf decrease of the discharge voltage, a substantial charge remains on the capacitor at the time of the next half-cycle of operation. As a result, no current can flow the rectifier untif the rising ac input voltage on the rectifier plate exceeds the voltage of the

charge remaining on C, because this charge voltage is the cathode-to-ground potential of the rectifier tube. When the plate voltage exceeds the charge voltage across C, the rectifier again conducts, and again charges C to approximately the peak value of the applied voltage. Shortly after the charge on the capacitor reaches its peak value, the tube stops conducting. Because the fall of the ac input voltage on the plate is considerably more rapid than the decrease in the capacitor voltage, the cathode quickly becomes more positive than the plate, and the rectifier ceases to conduct. During the charging period, capacitor C is connected across the output of the rectifier, and the charge time is determined by the effective series resistance, which is onfy that of the tube plate-tocathode (forward) resistance and the transformer impedance, plus that of the leads to the tube and capacitor. Hence, the resistance is low and C charges very quickly. During the nonconducting period, the discharge path is through  $R_1$ , which is relatively large, so that the time constant is long. Thus capacitor C does not discharge appreciably before the conduction cycle again begins.

The repeated charge and discharge of capacitor C (as described above) with the respective rise and **fall** of the input voltage constitutes the basic filtering action of this circuit. To reduce the ripple amplitude and increase the dc component in the output voltage, capacitor C charges up and stores energy when the tube is conducting and discharges to furnish current to the load when the tube is nonconducting.

Using ohms law, 
$$R = \frac{E}{I}$$
, it is evident that a heavy

current drain, for the same output voltage, represents a lower load resistance. Therefore, with a heavy load and lower  $R_t$ , capacitor C discharges more quickly. Since the output voltage represents the average charge retained in the capacitor, it can be seen that with heavy loads the capacitor will discharge further between the periods of tube conduction. Hence, the output voltage will also be lower. This is why the single-capacitor filter is used only for very light current drains. Since the output voltage for heavy loads is lower and the output ripple voltage component is also higher, the effective filtering is good only for light loads.

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# Failure Analysis.

**General.** With the supply voltage removed from the input to the **filter** circuit, one terminal of the falter capacitor can be disconnected from the circuit. **The** capacitor should be checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance. During these checks it is very important, when the capacitor is electrolytic, that correct polarity be observed. A decrease in effective capacitance or losses within the capacitor can cause the output to be below normal and also cause excessive ripple amplitude.

If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. Resistance measurements can be made across the terminals of the capacitor to determine whether it is shorted, leaky, or open. When testing electrolytic capacitors, set the ohmmeter to the high range and connect the test prods across the capacitor, being careful to observe polarity. This is important because current flows with less opposition through an electrolytic capacitor in one direction than in the other. If the current polarity is not observed, an incorrect reading will result. When the test prods are first connected, a large deflection of the meter takes place, and then the pointer returns slowly toward the infinite-ohms position as the capacitor charges. For a good capacitor with a rated working voltage of 450 volts, dc, the final reading on the ohmmeter should be over 500,000 ohms. (A rough rule of thumb for high-voltage capacitors is at least 1000 ohms per volt.) Low-voltage electrolytic capacitors (below 100 volts rating) should indicate on the nrder of 100.000 ohms.

If no deflection is obtained in the ohmmeter when making the resistance check explained above, an open-circuited capacitor is indicated.

A steady full-scale deflection of the pointer at zero ohms indicates that the capacitor being tested is short-circuited.

An indication of a leaky capacitor is a steady reading on the scale somewhat between zero and the minimum acceptable value. (Be certain this reading is not caused by an in-circuit shunting part.) To be vrdid, these capacitor checks should be made with the capacitor completely disconnected from the circuit in which it operates.

In high-voltage filter capacitor applications, paper and oil-filled capacitors are used, as also are mica and ceramic capacitors (for low-capacitance values). In this case, polarity is of no importance unless the capacitor terminals are marked + or –. It is, however, good maintenance practice to use the output polarity of the circuit as a guide, connecting positive to positive and negative to negative. **Thus** any effects of polarity on circuit tests are minimized and the possibility of damage to components or test equipment is avoided. **Remember-** an undischarged capacitor retains its polarity and holds its charge for long periods of time. To be safe, discharge the capacitor to be tested with the **power** OFF before connecting test equipment or disconnecting the capacitor.

# **R-C CAPACITOR-INPUT FILTER**

## Application.

**The** R-C capacitor-input falter is limited to applications in which the load current is small. This type of falter is used in power supplies where the load current is constant and voltage regulation is not necessary, such as in the high-voltage power supply for a cathode-ray tube or as part of a de-coupling network for multistage amplifiers.

#### Characteristics.

Filter is composed of shunt input capacitor, series resistor, and shunt output capacitor.

Filtering efficiency increases as ripple frequency is increased.

Output current is much less than that obtained corresponding falter which uses a choke instead of a resistor.

Regulation of rectifier-type power supply is poor with this type of filter; requires relatively constant load current.

Rectifier peak current is high with this circuit because of input capacitance.

## Circuit Analysis.

**General. The** rectifier circuits previously described in this section of the handbook provide a rectified output voltage (across the load resistance) which has a pulsating waveform. The accompanying illustration shows an R-C capacitor-input filter and the waveforms obtain from either a half-wave or a fuU-wave (single-phase) rectifier circuit.



**R-C Cepecitor-input Filter and Waveforms** 

The waveforms shown in part A represent the **unfiltered** output from a typical rectifier circuit when current pulses flow through the load resistance each time the rectifier conducts. Note that the dashed line indicating the average value of output voltage,  $E_{av}$ , for the half-way rectifier is less than half the amplitude of the voltage peaks (approx 0.318). The average value of output voltage,  $E_{av}$ , for the full-wave rectifier is greater than half (approx 0.637), but is still much less than the peak amplitude of the rectifieroutput waveform. With no filter circuit **(unfiltered)**, the waveform has a large value of pulsating component as compared with the average (or dc) **com**ponent.

The RC filter shown in the schematic of the **illus**stration consists of an input **filter** capacitor, Cl, a series resistor, R1, and an output falter capacitor, C2. This filter is called an *R-C capacitor-input filter*, and is sometimes referred to as an *R-C Pi-section jilter* because the configuration of the schematic resembles the Greek letter  $\pi$ .

Capacitor Cl is placed at the input to the filter, and is in shunt with the output of the rectifier circuit; capacitor Cl has the same faltering action in this circuit that the capacitor does in the Shunt-Capacitor Filter, described earlier in this section of the handbook. In the capacitor-input filter, the major portion of the faltering action is accomplished by the input capacitor, C 1. The average value of voltage across capacitor Cl is shown in part B of the illustration for half-wave and full-wave rectifier circuits. Note that the average value of voltage across capacitor C 1 is greater than the average value of voltage for the unfiltered output of the rectifier, shown in part A. The value of the input capacitor is relatively large in order to present a low reactance  $(X_C)$  to the pulsating current, and to store a substantial charge. The rate of charge for the input capacitor is limited only by the impedance of the ac source (transformer) and the internal (or forward) resistance of the rectifier, both of which are relatively low; therefore, the R-C charge time constant for the input circuit is relatively short. As a result, when the pulsating voltage is first applied to the capacitor-input filter, capacitor Cl charges rapidly and reaches the peak voltage within the first few cycles. The charge on capacitor Cl approximates the peek value of the pulsating voltage when the rectifier is conducting, but when the rectifier output falls to zero, the capacitor partially discharges through the series resistor, Rl, and the load resistor,  $R_L$  during the time the rectifier is nonconducting. The larger the value of the input capacitor, Cl, the better the filterring action; however, there is a practical limitation to maximum value of the capacitor. If the peakcurrent rating of the rectifier is exceeded during the charging time for the capacitor, the rectifier will be damaged; for this reason, a compromise in the value of the input capacitor is necessary in order to keep the maximum charging current within the peak-current rating of the rectifier.

The R-C capacitor-input filter is similar to the L-C Chunt-Capacitor Filter, described later in this section, except that a resistor is used in place of the series inductor. Although the series resistor affords faltering action, a resistor can never be as effective as an inductor unless a considerable dc voltage drop can be

tolerated. However, the RC capacitor-input falter circuit is an improvement over the shunt-capacitor filter, described earlier in this section, because additional faltering results from the added reactance of resistor R1 and capacitor C2.

The pulsating output from the rectifier circuit, which is applied to the input of the filter, can be considered as being composed of two components: an ac component, represented by pulsations, and a dc component, represented by the average value of voltage  $(E_{av})$ . Because these pulsations occur at a relatively low frequency (which is the input frequency for a half-wave rectifier, or a multiple of the input frequency for full-wave and other types of rectifiers), the value of the shunt capacitors, Cl and C2, is purposely made large so that their reactance are very low at the pulsating (ripple) frequency. Both the ac and dc components of the rectifier output (present at the input to the filter) flow through the filter resistor, R1; therefore, a voltage drop occurs across Rl, which results from the voltagedivider action of resistor R1 in series with the parallel combination of capacitor C2 and load resistance R<sub>1</sub>. Since the reactance of C2 is very low at the ripple frequency, most of the ac component bypasses the load resistance, R, and the dc component flows through the load resistance. The efficiency of the filter depends, to a great extent, upon keeping the reactance of capacitor C2 very small as compared with the load resistance,  $R_1$ . The charging and discharging of capacitor C2 tends to smooth out the voltage fluctuations and reduce the ripple amplitude (E) applied to the load. The final result is the waveform shown in part C of the illustration. The average value of voltage developed across capacitor C2 and load resistance R<sub>1</sub> is rdways less than the average value of voltage across capacitor Cl, because of the voltage drop occurring across the filter resistor, RI. When the load current is even moderate, an R-C filter is not normally used, because the voltage drop across the series resistor, RI, becomes excessive for most applications.

The output from a Pi-section R-C falter may contain an amount of ripple which is considered excessive for the equipment application. By adding another series falter resistor, R2, and a shunt capacitor, C3, to the basic capacitor-input filter, the ripple component across the load resistance can be further attenuated. However, the addition of series resistors increases the voltage drop within the **filter**, resulting in poorer regulation and a decrease in output voltage. For these reasons, the number of sections that may be added, as well as the size of the resistors, is limited. As shown in the accompanying illustrations, the added R-C filter components, R2 and C3, resemble an inverted letter L. For this reason it is referred to as an L-Section filter.



Capecitor-input Filter with L-Seetion Added

#### Failure Analysis.

**General. The** shunt capacitors are subject to open circuits, short circuits, and excessive leakage; the series falter resistors are subject to changes in value and, occasionally, to open circuits. Any of these troubles can be easily detected.

The input capacitor has the greatest pulsating voltage applied to it, is the most susceptible to voltage surges, and has a higher average voltage applied; as a result, the input capacitor is frequently subject to voltage breakdown and shorting. The remaining shunt capacitor(s) in the falter circuit is not subject to voltage surges because of the protection offered by the series falter resistor(s); however, a shunt capacitor can become open, leaky, or shorted.

Shorted capacitors or an open falter resistor will result in a no-output indication. An open falter resistor will result in an abnormally high dc voltage at the input to the filter and no voltage at the output of the falter. Leaky capacitors or filter resistors that have increased in value will result in a low dc output voltage. Open capacitors, capacitors which have lost their effectiveness, or falter resistors that have decreased in value will result in an excessive ripple amplitude in the output of the supply.

With the supply voltage removed from the input to the **filter** circuit, one terminal of each capacitor can be discomected from the circuit. Each capacitor should be checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance. It is important, when the capacitor is electrolytic, that correct polarity be observed at all times. NAVSHIPS 0967-0000120

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A decrease in effective capacitance or losses within the capacitor can cause the output to be below normal and also cause excessive ripple amplitude. The value of resistors can be checked by using an **ohm**meter.

If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. Resistance measurements can be made across the terminals of the capacitor to determine whether it is shorted, open, or leaky. When testing electrolytic capacitors, set the ohmmeter to the high range and connect the test prods across the capacitor, being careful to observe polarity. This is important because current flows with less opposition through an electrolytic capacitor in one direction than in the other. If the correct polarity is not observed, an incorrect reading will result. When the test prods are first connected, a large deflection of the meter takes place, and then the pointer returns slowly toward the infinite-ohms position as the capacitor charges. For a good capacitor with a rated working voltage of 450 volts, dc, the final reading on the ohmmeter should be over 500,0@ ohms. (A rough rule of thumb for high-voltage capacitors is at least 1000 ohms per volt.) Low-voltage electrolytic capacitors (below 100 volts rating) should indicate on the order of 100.000 ohms.

If no deflection is obtained on the ohmmeter when making the resistance check explained above, an **open-circuited** capacitor is indicated.

A steady full-scale deflection of the pointer at zero ohms indicates that the capacitor being tested is short-circuited.

An indication of a leaky capacitor is a steady reading on the scale somewhere between zero and the minimum acceptable value. (Be certain this reading is not caused by an in-circuit shunting part.) To be valid, these capacitor checks should be made with the capacitor completely disconnected from the circuit in which it operates.

In high-voltage falter capacitor applications, paper and **oil-filled** capacitors are used, as also are mica and ceramic capacitors (for low-capacitance values), in this case, polarity is of no importance unless the capacitor terminals are marked + or -. It is, however, good maintenance practice to use the output polarity of the circuit as a guide, connecting positive to positive and negative to negative. Thus any effects of polarity on circuit tests are minimized and the possibility of damage to components or test equipment is avoided. Remember-an undischarged capacitor retains its polarity and holds its charge for long periods of time. To be safe, discharge the capacitor to be tested with the *power* OFF before connecting test equipment or disconnecting the capacitor.

# L-C CAPACITOR-INPUT FILTER

#### Application.

**The** L-C capacitor-input falter is one of the most commonly used falters. This type of filter is used primarily in radio receiver and small audio amplifier power supplies, and in any type of power supply where the output current is low and the load current is relatively constant.

#### Characteristics.

Filter is composed of shunt input capacitor, series inductor, and shunt output capacitor.

Filtering efficiency increases as ripple frequency is increased.

Output voltage is greater than that of choke-input falter; output current is less than that of choke-input falter.

Regulation of rectifier-type power supply is only fair with this type of filter; requires relatively constant load current.

Rectifier peak current is high with this circuit because of input capacitance..

#### Circuit Analysis.

General. The accompanying illustration shows an L-C capacitor-input falter and the waveforms obtained from either a half-wave or a full-wave (single-phase) rectifier circuit.

The waveforms shown in part A represent the unfdtered output from a typical rectifier circuit when current pulses flow through the load resistance each time the rectifier conducts. Note that the average value of output voltage,  $E_{av}$  (indicated by the dashed line), for the hrdf-wave rectifier is less than half the amplitude of the voltage peaks; the average value of output voltage,  $E_{av}$ , for the full-wave rectifier is greater than half, but is still much less than the peak amplitude of the rectifier-output waveform. With no falter circuit connected across the output of the rectifier circuit **(unfiltered)**, the waveform has a large value of pulsating component as compared with the average (or dc) component.



L-C Capacitor-Input Filter and Waveforms

The falter shown in the schematic of the illustration consists of an input filter capacitor, Cl, a series inductor, L, and an output filter capacitor, C2. It is called a *capacitor-input jilter*, and is often referred to as a *Pr*<sup>\*\*</sup>-section filter because the configuration of the schematic resembles the Greek letter  $\pi$ .

Capacitor Cl is placed at the input to the filter, and is in shunt with the output of the rectifier circuit; capacitor Cl exhibits the same filtering action in this circuit that Cl does in the R-C Capacitor-Input Filter, described earlier in this section of the handbook. In the capacitor-input falter, the major **portion** of the faltering action is accomplished by the input capacitor, Cl. The average value of voltage across the input capacitor, Cl, is shown in part B of the illustration for the half-wave and full-wave rectifier circuits. Note that the average value of voltage across capacitor Cl is greater than the average value of voltage for the unfiltered output of the rectifier, shown in part A. The value of the input capacitor is relatively large in order to present a low reactance (XC) to the pulsating current and to store a substantial charge. The rate of charge for the capacitor is limited only by the impedance of the ac source (transformer) and the internal resistance of the rectifier, both of which are relatively low; therefore, the R-C charge time constant for the input circuit is relatively short. As a result, when the pulsating voltage is first applied to the capacitor-input filter, capacitor C1 charges rapidly and reaches the peak voltage within the first few cycles. The charge on capacitor Cl approximates the peak value of the pulsating voltage when the rectifier is conducting, but when the rectifier output falls to zero, the capacitor partially discharges through the series inductor, L, and the load resistance, R<sub>1</sub>, during the time the rectifier is nonconducting. The larger the value of the input capacitor, Cl, the better the filtering action; however, there is a practical limitation to the maximum value of the capacitor. If the peak-current rating of the rectifier is exceeded during the charging time for the capacitor, the rectifier will be damaged; for this reason, a compromise in the value of the capacitor is necessary in order to keep the maximum charging current within the peak-current rating of the rectifier.

The inductor (or falter choke), L, serves to maintain the current flow to the falter output (capacitor C2 and load resistance  $R_1$ ) at a nearly constant level during the charge and discharge periods of input capacitor Cl. The rate of discharge for capacitor Cl is determined by the dc resistance of the falter choke, L, and the load resistance,  $R_1$ , in series. The average value of voltage developed across capacitor C2 and load resistance  $R_L$  is somewhat less than the average voltage developed across capacitor Cl. As the load current is increased, the voltage drop across inductor L increases because of the internal dc resistance of the inductor. Also, there is a decrease in the discharge time constant for capacitor Cl which, in turn, results in a decrease in the average value of voltage across Cl because of the greater discharge between rectifier pulses; thus, the average voltage across output capacitor C2 is also reduced.

Series inductor L and capacitor C2 from a voltage divider across capacitor Cl. As far as the ripple **com**onent is concerned, the inductor offers a high impedance and capacitor C2 offers a low impedance

to the ripple component; as a result, the ripple cornponent, E<sub>1</sub>, appearing across the load resistance is greatly attenuated. Since the inductance of the filter choke opposes changes in the value of the current flowing through it, the average value of the voltage produced across the output capacitor, C2, contains a much smaller value of ripple component,  $E_r$ , as compared with the value of ripple produced across the input capacitor, Cl. Since inductor L operates in conjunction with capacitor C2, if either filter element is decreased in value, the other must be increased accordingly to maintain the same degree of faltering. The pulsations across capacitor C2, which are present in spite of the action of capacitor Cl and inductor L, cause C2 to charge and discharge in the same manner as Cl. The final result is the waveform shown in part C of the illustration.

Some electronic equipments require a high degree of faltering, while other equipments are not critical in this respect. The output from a single shunt-capacitor falter, or from an R-C or L-C capacitor-input (single Pi-section) filter, may contain an amount of ripple which is considered excessive for the equipment application. When this is the case, it is necessary to use additional faltering to further attenuate the ripple component and reduce the ripple content to a minimum. By adding another series inductor (L2) and shunt capacitor (C3) to the basic capacitor-input falter, the ripple component across the load resistance can be further attenuated. As shown in the accompanying illustration, the added falter components, L2 and C3, are called an *L-section filter* because the schematic configuration resembles an inverted letter L.



Capacitor-Input Filter with L-Section Added

In a partical fiher circuit, the reactance of the additional shunt capacitor (C3) is much less than the reactance of the additional series inductor, L2, and of the load resistance, R<sub>1</sub>. Therefore, each Lsection filter which is added to the basic falter further reduces the output ripple amplitude. When using a multiplesection filter, the operating voltage may be taken from each separate filter section. However, when the L-section (L2 and C3) is added to the basic filter circuit, the regulation of the supply suffers, because adding resistance in series with the load causes greater variation of the output voltage when changes in load current occur. The voltage regulation of a power supply using a capacitor-input falter circuit is relatively poor (as compared with a choke-input filter); for this reason, the use of a capacitor-input falter is usually restricted to low-current applications such as receivers, amplifiers, and the like, where the load current is relatively constant.

**Circuit Operation.** Consider now a complete cycle of operations, using a single-phase, full-wave rectifier circuit to supply the input voltage to the filter. The rectifier voltage is developed across capacitor Cl. The ripple voltage in the output of the falter is the alternating component of the input voltage reduced in amplitude by falter action, as shown in the preceding illustration.

Each time the plate of the rectifier goes positive with respect to the cathode, the tube conducts and Cl charges to the peak value of the voltage less the internal voltage drop in the tube. Conduction occurs twice during each cycle for a full-wave rectifier; for a 60-Hz supply this produces a 120-Hz ripple voltage. Although each tube alternates (first one conducts while the other is nonconducting, and then the other conducts while the first one is nonconducting), the falter input voltage is not steady. As the positive conducting plate voltage increases (on the positive half of the cycle), capacitor Cl charges rapidly, the charge being limited only by the transformer secondary impedance and the tube forward (cathode-to-plate) resistance. During the nonconducting interval (when the plate voltage drops below the capacitor charge voltage), Cl discharges through choke L and load resistance  $R_1$ . The discharge path is an R-L longtime constant path; thus Cl discharges much more

ORIGINAL 491-044 0 -73 -16 slowly than it charges, as indicated by the waveforms in the illustration above. In this respect, the action of Cl is similar to that of the shunt-capacitor filter described previously in this section, with one exception. This exception is the effect of choke L.

Choke L is usually chosen to **bea** large value, on the order of 10 to 20 henries, and offers a large inductive reactance to the 120-Hz ripple component produced by the rectifier. Thus each time Cl starts to discharge, the inertia of the choke inductance effectively opposes a change in the ripple current through L. As far as the d-c component of this voltage is concerned, it is affected only by the time constant consisting of the dc resistance of L and RI in series with Cl.

The effect of L on the charging of capacitor C2 must not be considered. Since C2 is connected in parallel with Cl through coke L, any charge on Cl will also tend to change C2. However, both the impedance and resistance of L are in series with C2, and a voltage division of both the ripple (ac) voltage and dc output voltage occurs. The greater the impedance of the choke to the ripple frequency, the less the ripple voltage appearing across C2 and the output. The dc output voltage is freed mainly by the dc resistance of the choke. For each specific value of current there is a voltage drop across the choke. Thus the dc voltage across C2 is always less than that across C1 (the higher the output current, the lower the voltage across C2). Since C2 is simplied from Cl, which has maximum and minimum voltages produced by the charge and discharge action (the ripple voltage), C2 also follows this charge and discharge pattern. The difference is that the C2 action is smoothed out by the longer time constant. While the peaks and valleys exist, the values are lower. As can be seen from the waveform in part C of the illustration above, the over-all effect is to provide a purer direction current (less ripple).

# Failure Analysis.

**General. Shunt capacitors are subject to open cir**cuits, short circuits, and excessive leakage; series inductors are subject to open windings and occasionally shorted turns or a short circuit to the core.

The input capacitor has the greatest pulsating voltage applied to it, is the most susceptible to voltage surges, and has a generally higher average voltage applied; as a result, the input capacitor is frequently subject to voltage breakdown and shorting. The output capacitor is not as susceptible to voltage surges because of the protection offered by the series inductor, but the capacitor can become open, leaky, or shorted.

A shorted capacitor, an open falter choke, or a choke winding which is shorted to the core results in a no-output indication. A shorted capacitor, depending on the magnitude of the short, may cause a shorted rectifier, transformer, or filter choke. When proper precautions are taken, it may only blow a protective fuse. An open falter choke results in an abnormally high dc voltage at the input to the filter and no voltage at the output of the falter. A leaky or open capacitor in the falter circuit results in a low dc output voltage; this condition is generally accompanied by an excessive ripple amplitude. Shorted turns in the winding of a filter choke reduce the effective inductance of the choke and decrease its filterring efficiency; as a result, the ripple amplitude increases.

When the supply voltage removed from the input to the filter circuit, one terminal of each capacitor can be disconnected from the circuit. Each capacitor should be checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance, being careful always to observe correct polarity. A decrease in effective capacitance or losses within the capacitor can cause the output to be below normal and also cause excessive ripple amplitude.

If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. Resistance measurements can be made across the terminals of the capacitor to determine whether it is shorted or leaky. If the capacitor is of the electrolytic type, the resistance measurement may vary, depending on the test-lead polarity of the ohmmeter. Therefore, two measurements must be made, with the test leads reversed at the capacitor terminals for one of the measurements, to determine the larger of the two resistance measurements. The larger resistance value is then accepted as the measured value.

# L-C CHOKE4NPUT FILTER

# Application.

**The L-C** choke-input **filter** is used primarily in - power supplies where voltage regulation is important

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and where the output current is relatively high and subject to varying load conditions. The filter is used in high-power applications such as those found in the power supply circuits of radar and communication transmitters.

#### Characteristics.

Filter is composed of series input inductor and shunt output capacitor.

Filtering efficiency increases as ripple frequency is increased.

Output voltage is less than that of capacitor-input filter; output voltage from filter approaches average **value** of voltage from rectifier at **filter** input.

Regulation of rectifier-type power supply is good with this type of falter; further improvement in regulation characteristics can be realized with swingingchoke input inductor.

Rectifier output current approaches **maximum** rated current; output current is generally greater than that of capacitor-input falter.

## Circuit Analysis.

**General. The** accompanying illustration shows an **L-C** choke-input **filter** and the waveforms obtained from a single-phase, full-wave rectifier circuit.



L-C Choke-Input Filter and Waveforms

The output from a single-phase, half-wave rectifier circuit is not illustrated because the choke-input **filter** is seldom used with this circuit. The **unfiltered** output obtained from three-phase, half-wave and full-wave rectifier circuits produces a higher average voltage and ripple frequency; however, the principle of falter action is essentially the same as that illustrated for the single-phase, full-wave rectifier; therefore, these waveforms are not illustrated.

The waveform given in part A represents the unfiltered output from a typical single-phase, full-wave rectifier circuit when current pulses flow through the load resistance each time the rectifier conducts. Note that the dashed line indicating the average value of output voltage,  $\mathbf{E}_{av}$ , is slightly greater (0.637) than half the amplitude of the voltage peaks. With no falter circuit connected across the output of the rectifier circuit (unfiltered), the waveform has a large value of pulsating component as compared with the average (de) component.

The falter shown in the schematic of the illustration consists of an input inductor or falter choke, L, and an output falter capacitor, C, The falter illustrated is called a *choke-input jilter*, and is often referred to as an *L-sectwn filter* because the schematic configuration resembles an inverted letter L.

Inductor L is placed at the input to the falter and is in series with the output of the rectifier circuit. Since the action of an inductor is to oppose any change in current flow, the inductor tends to keep a constant current flowing to the load throughout the complete cycle of the applied voltage. As a result, the output voltage never reaches the peak value of the applied voltage; instead, the output voltage approximates the average value of the input to the falter. Also, the reactance of the inductor (XL) reduces the amplitude of ripple voltage without reducing the dc output voltage an appreciable amount.

The shunt capacitor, C, charges and discharges at the ripple frequency, but the amplitude of the ripple voltage,  $\mathbf{E}_{\mathbf{r}}$ , is relatively smaU because the inductor, L, tends to keep a constant current flowing from the rectifier circuit to the load. The reactance of the shunt capacitor (&-J presents a low impedance to the ripple component existing at the output of the **filter**, and the capacitor attempts to hold the output voltage relatively constant at the average value of the voltage. Since the reactance of the series inductor ( $S_{\mathbf{L}}$ ) is

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greater than the reactance of the shunt capacitor  $(X_C)$ , and the reactance of the shunt capacitor (XC) is less than the load resistance,  $R_L$ , the amplitude of the ripple frequency at the output of the falter is considerably reduced from that present at the input to the falter circuit. The output waveform is shown in part B of the accompanying illustration; assuming a single-phase, full-wave rectifier circuit, note that the frequency of the ripple voltage,  $E_r$ , is twice the frequency of the applied voltage.

Both the output voltage from the falter and the peak current of the rectifier depend upon the inductance of the choke and the resistance of the load. The minimum value of inductance necessary to keep the output voltage from increasing above the average value of rectified ac is called the *critical value* of inductance. If the inductance of the input filter choke is less than the critical value for the circuit, the filter acts more like a capacitor-inPut falter and the output voltage will rise above the average value.

**The** critical **value** of inductanc<sup>e</sup> "@'en b<sub>y</sub> 'he expression:

$$\mathbf{L_h} = \frac{\mathbf{E}_{\_out}}{\mathbf{I}_{out}}$$

where:  $L_{h}^{-}$  critical inductance in henries  $E_{out}^{-}$  = output of power supPlY in volts  $I_{out}^{-}$  = current drawn from power supply milliamperes

An increase in the value of choke **inductance** above the critical value will decrease the ratio of **peak-to**average rectifier current and maintain a more uniform **current** flow through the inductor. Increasing the value of inductance above a cretain value, **called the** *optimum value* of inductance, does not provide any appreciable improvement in **performance** or filtering efficiency. In **practice**, **ductance** for a given set of conditions is considered to be twice the critical value of inductance.

**The** value of inductance required for the **filter** varies directly with the effective load resistance,  $R_{L}$ . Since the **inductance** of a filter choke varies **inversely** with the current flowing through it, an increase in the load resistance causes the ratio of peak-to-average current to decrease; conversely, a decrease in the load resistance causes the ratio of peak-to-average current **to increase**.

The regulation characteristics of a power supplY using a choke-inPut falter can be improved by the use of a swinging choke as the input inductor. A swinging

choke is a choke whose inductance varies inversely with respect to the current flowing through it over the specified **operating** range. It is designed to have slightly more than the critical value of inductance at full load and an optimum value of **inductance** at no **load**. 'f'his **characteristic** maintains the peak-to-average current ratio within certain limits over a considerable **range of** changing load currents, and results **in** improved regulation for the **supply**.

The choke-input filter is widely used in electronic equipments where the power supply is required to deliver relatively high values of current to the load with good regulation characteristics. In some cases the equipment requires a high degree of filtering, while in other cases the equipment is not critical in this respect. The output from a single choke-inPut falter (single L-section) may contain an amount of ripple which is considered excessive for the equiPment application- When this is the case, it is necessary to use additional filtering to further attenuate the ripple component. By adding another series inductor, L2, and a shunt capacitor, C2, to the basic chokeinput falter, the ripple component across the load resistance can be further attenuated. As shown in the accompanying illustration, the added falter comfilter ponents, L2 and C2, ar<sup>e ca</sup>\* <sup>ed</sup> an '-section because the schematic conflation resembles an inverted letter L.



Choke-Input Filter with L-Section Added

 $I_n$ **a** Practical **filter** circuit, the reactance of the shunt capacitor (C2) is much less than the reactance of the series inductor (L2) and of the load **resistance**,  $R_L$ . Therefore, each Lsection falter which is added to the basic falter further reduces the outPut **ripple** 

amplitude. However, when the L-section, L2 and C2, is added to the basic falter circuit, the regulation of the supply suffers somewhat because the added resistance of inductor L2 is in series with the load and thus causes a variation of the output voltage when changes in load current occur. Although the voltage regulation of a power supply using a choke-input falter circuit is good (as **compared** with the capacitor-input falter), the regulation can be further improved if inductor L1 is a swinging choke. In fact, the circuit may be designed to over-regulate, in which case the rise in average voltage across capacitor Cl **com**pensates for the additional voltage drop occurring across inductor L2; as a result, the output voltage tends to remain constant.

The inductance of any iron core inductor shows a marked decrease as magnetic saturation is reached. The core of ordimry inductors is designed so that saturation occurs at a value just above the maximum current rating. Swinging chokes are generally designed to have one or more air gaps in the laminated core. The accompanying diagram illustrates a swinging choke which has two air gaps-one large and one small. (The sizes of the gaps are exaggerated in the illustration.)



#### Swinging Choke with Two Air Gaps

The purpose of the large gap is to provide effective inductance at the largest currents, while that of the small gap is to assure high inductance at the smallest currents. Saturation of the core starts at some specified current; at full rated current, saturation is almost complete. Swinging chokes are rated to indicate the variations of inductance with variations of current through the coil. A rating of 15 to 3 henries at 25 to 250 ma, for example, means that the value of inductance is 15 henries at 25 ma, and reduces to only 3 henries at 250 ma. When handling small currents, the swinging choke functions as a

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conventional choke-input falter. For larger currents, where the output voltage tends to drop, the inductance decreases and the falter starts to approach the characteristics of a capacitor-input falter. Because the decrease in inductance permits the capacitor to charge more nearly to the peak value instead of the average value, the loss of voltage in the dc resistance of choke L2 is thereby compensated for, and the output voltage tends to remain constant. As a result, regulation is greatly improved.

The output voltage available from a power supply using a choke-input falter circuit is much less than that obtained with a capacitor-input filter. However, since the input choke opposes a rapid build-up of current, there are no abrupt **peak-rectifier** currents with the choke-input falter, as there are with capacitor-input filter. Therefore, the rectifier can deliver a higher continuous current to the load without exceeding its maximum safe ratings.

**Detailed Circuit Oparation.** Consider now one cycle of operation of the basic choke-input falter, as illustrated previously with waveforms.

The input to the falter circuit is t!!e output of the single-phase, full-wave rectifier. **The** rectified pulses applied to the **filter** are as shown in part A of the illustration. During the rising portion of the input voltage, choke L produces a back emf which opposes the constantly increasing input voltage. The net result is to effectively present the rapid charging of falter capacitor C. Thus, instead of reaching the peak value of the input voltage, capacitor C is charged only to the average value of input voltage. After the input voltage reaches its peak and decreases, the back emf tends to keep the current flowing in the same direction, in effect broadening the peak.

During the rising portion of the pulse, the current flow through L is reduced, and during the **falling** portion of the pulse, the current continues to **ise**. The pulse, as it approaches zero, becomes insufficient to maintain the current, which then commences to decrease.

When the next puke starts, the back emf is still opposing an increase in current, and the current continues to decrease. (The choke, in effect, shifts the ripple peaks almost 90 degrees with respect to the rectifier output.) When the rectified puke nears the peak value, the rate of change and the inductive effect decrease, and once again the current through L starts to rise. This cycle of operation is continuously repeated during the time the circuit is energized and rectified pulses are applied to choke L. The fluctuating voltage which results from the action of choke L appears across capacitor C and load resistor  $R_L$  in parallel. The low reactance of the capacitor to this ripple voltage effectively bypasses the ripple voltage to ground, so that the amplitude of the ripple voltage in the falter output is significantly reduced.

The voltage across C is the dc component or output voltage, and is produced by the charging of C through L. Essentially, the charging of C is controlled by the value of the time constant, consisting of the dc choke resistance in series with C. Such a typical time constant is on the order of tenths of a second or seconds rather than micro-seconds or milliseconds. Thus it takes many cycles of operation to charge C. The discharging of C through the load is usually slower than the charge time, since the load resistance is normally greater than that of the choke. Therefore, the output voltage tends to remain fairly constant. The choke-input falter is effective in reducing the ripple voltage because choke L and capacitor C act as an ac voltage divider for ripple voltage. With the impedance of L high and the impedance of C low, any ripple voltage appearing across C is small, because of the large voltage drop across L, and is effectively bypassed around the load by the low value of  $X_{C}$ .

## Failure Analysis.

**General. The shunt capacitors** are subject to open circuits, short circuits, and excessive leakage; the series inductors are subject to open windings and, occasionally, shorted turns or a short circuit to the core.

Shorted turns in the input choke may reduce the value of inductance below the critical value of inductance; this will result in excessive peak-rectifier current, accompanied by an abnormally high output voltage, excessive ripple amplitude, and poor voltage regulation. Shorted turns in the smoothing choke (in the case of a **multisection** falter) will reduce the effective value of inductance; this will result in less **fil**lering efficiency, with an attendant increase in the output ripple amplitude. An open falter choke, or a choke winding which is shorted to the core, will result in a **no-output** condition. A choke winding which is shorted to the core may cause overheating of the tubes, blown fuses, etc.

The shunt capacitor(s) in the choke-input falter is not subjected to extreme voltage surges because of the protection offered by the input inductor; however, the capacitor can become open, leaky, or shorted. An open capacitor results in excessive ripple amplitude in the output voltage; a leaky capacitor results in a lower-than-normal output voltage, and a shorted capacitor results in a no-output condition.

With the supply voltage removed from the input to the filter circuit, one terminal of the capacitor can be disconnected from the circuit. The capacitor should be checked, using a capacitance analyzer, to determine its effective capacitance and leakage resistance. It is important when the capacitor is electrolytic, that correct polarity be observed at all times. A decrease in effective capacitance or losses within the capacitor can cause the filtering efficiency to decrease and produce excessive ripple amplitude.

If a suitable capacitance analyzer is not available, an indication of leakage resistance can be obtained by using an ohmmeter. Resistance measurements can be made across the terminals of the capacitor to determine whether it is shorted, open, or leaky. When testing electrolytic capacitors, set the ohmmeter to the high range and connect the test prods across the capacitor, being careful to observe polarity. This is important because current flows with less opposition through an electrolytic capacitor in one direction than in the other. If the correct polarity is not observed, an incorrect reading will result. When the test prods are first connected, a large deflection of the meter takes place, and then the pointer returns slowly toward the infinite-ohms position as the capacitor charges. For a good capacitor with a rated working voltage of 450 volts, dc, the final reading on the ohmmeter should be over 500,000 ohms. (A rough rule of thumb for high-voltage capacitors is at least 1000 ohms per volt.) Low-voltage electrolytic capacitors (below 100 volts rating) should indicate on the order of 100,000 ohms.

If no deflection is obtained on the ohmmeter when making the resistance check explained above, an open-circuited capacitor is indicated.

A steady full-scale deflection of the pointer at zero ohms indicates that the capacitor being tested is short-circuited.

An indication of a leaky capacitor is a steady reading on the scale somewhere between zero and the minimum acceptable value. (Be certain this reading is not caused by an in-circuit shunting part.) To be valid, these capacitor checks should be made with the capacitor completely disconnected from the circuit in which it operates.

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In high-voltage filter capacitor applications, paper and **oil-filled** capacitors are used, as are also mica and ceramic capacitors (for low-capacitance. values). In this case, polarity is of no importance unless the capacitor terminals are marked + or -. It is, however, good maintenance practice to use the output polarity of the circuit as a guide, connecting positive to positive and negative to negative. Thus any effects of polarity on circuit tests are minimized and the possibility of damage to components or test equipment is avoided. Remember-an undischarged capacitor retains its polarity and holds its charge for long periods of time. To be safe, discharge the capacitor to be tested with the **power OFF** before connecting test equipment or discomecting the capacitor.

## **RESONANT FILTER**

#### Application.

The resonant filter is quite limited in its application to **power-supply** falter systems. It is normally used in conjunction with Ltype or Pi-type fflter sections, rather than by itself, since it is designed to offer maximum attenuation only to the fundamental ripple frequency.

#### Characteristics.

Parallel-resonant falter is composed of an inductor and a capacitor in parallel; series-resonant falter is composed of an inductor and a capacitor in series.

Filter is resonant at fundamental frequency of ripple voltage.

Parallel-resonant fflter offers maximum impedance at resonance; series-resonant filter offers minimum impedance at resonance.

Parallel-resonant filter requires constant load current.

## Circuit Analysis.

**General.** For special applications where maximum attenuation of the ripple frequency is desired, a resonant **filter** is sometimes used in power-supply circuits. This **filter** may be either the parallel-resonant or the series-resonant type, and is **alwyas** tuned to the fundamental ripple frequency. Since the **filter** is tuned only to the fundamental ripple frequency are attenuated very little, if at all. For this reason, the resonant falter is seldom used by itself; it is normally used in conjunc-

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tion with other faltering sections. A disadvantage of the parallel-resonant filter is that the inductance is subject to change when the load current is changed. Since the load current must flow through the inductor of the parallel-resonant falter, this current determines the value of inductance and, consequently, affects the resonant frequency of the tuned circuit.

**Perallel-Resonant Filter.** The accompanying illustration shows a parallel-resonant filter, sometimes called a *parallel-resonant trap*, used in two typical power-supply falter circuits.



# Typical Power-Suppty-Filter Circuits Using a Perallel-Resonant Filter

The circuit in part A shows a parallel-resonant filter, L1 and Cl, used with an Lsection fflter, L2 and C2; the circuit in part B shows a parallel-resonant fflter, L1 and Cl, used in conjunction with a shunt input capacitor, C2, and a shunt output capacitor, C3. Note that in both filter circuits the load current must flow through inductor L1 of the **parallel**resonant fflter.

The parallel-tuned circuit, L1 and Cl, is made resonant at the fundamental ripple frequency. When this is done, the fun&mental ripple-frequency component is greatly attenuated because of the extremely high impedance offered by the parallel-resonant circuit. In a practical falter circuit, the inductor is **fixed** in value and one or more **specific-value** capacitors are selected and placed in parallel with the inductor to obtain exact resonance at the ripple frequency. In a few special cases, and also when the ripple frequency is relatively high, the capacitor is fixed in value and the inductor is made variable. In either case, however, if the load current through the inductor should change from the design value of current, the inductance of L1 will change and the circuit will no longer be resonant at the ripple frequency. The circuit loses its **effectiveness** rapidly as the load current is changed from the design value and the circuit is detuned from resonance. At resonance, the **filter** offers maximum impedance to the ripple-frequency component. The filter provides less attenuation at other frequencies; it has a progressively lower impedance, both above and below the resonant frequency, the farther the frequency is from resonance. Therefore, the parallelresonant falter is nearly always used with additional falters to overcome this disadvantage and effectively attenuate harmonic frequencies.

In the circuit shown in part A, the parallelresonant falter, L1 and Cl, is connected in series with the output of the rectifier circuit and ahead of an Lsection falter, L2 and C2. The L-section falter circuit has the general characteristics previously described for the L-C Choke Input Filter, in this section of the handbook. The ripple-frequency component from the rectifier output is attenuated by the high impedance offered to the ripple frequency by L1 and Cl, and the remaining fluctuations in the form of harmonic frequencies of the fundamental ripple frequency are attenuated by the L-section filter, L2 and C2. The upper waveform in part A of the accompanying illustration shows the shape of the output voltage obtained from a single-phase, half-wave rectifier. The frequency of the ac input voltage is assumed to be 60 Hz. When the rectifier output is applied directly to the input of the parallel-resonant falter, the fundamental ripple component is highly attenuated in the output of the filter. This is shown by the lower waveform in part A.

In the circuit shown in part B, the **parallel**resonant filter, L1 and Cl, is located between two shunt capacitors, C2 and C3. This filter circuit has the general characteristics previously described for the LC Capacitor-Input Filter, in this section of the handbook. The ripple-frequency component which remains after being reduced in amplitude by the action of shunt capacitor C2 is further attenuated by the impe&nce offered by the parallel-resonant **filter** and any remaining fluctuations are smoothed by shunt capacitor C3. The upper waveform in part B of the illustration shows the shape of the output voltage of a single-phase, half-wave rectifier, developed across C2. The frequency of the ac input voltage is assumed to be 60 Hz. When the voltage developed across C2 is applied to the input of the parallel-resonant filter, the fundamental ripple component is greatly attenuated and appears in the filter output as shown by the lower waveform in part B.



# Typical Output Waveforms for Two Different Typas of Input to the Parallel-Resonant Filtar

The circuits shown in parts A and B of the illustration above have one important disadvantage, mentioned previously; that is, changes in load current affect the faltering efficiency of the parallel-resonant falter by changing the inductance and thus detuning the circuit from resonance. In a practical falter circuit, this effect can be tolerated for small changes in load current by making inductor L1 small as compared with capacitor Cl, so that the detuning will be minimized.

Series-Resonant Filter. The accompanying illustration shows a series-resonant falter, sometimes called a *series-resonant shunt jilter*, used in a typical power supply filter circuit.



The series-resonant filter is composed of L1 and Cl in series. The filter is used in conjunction with an input inductor, L2, and an L-section filter, L3 and C2. Note that the circuit is essentially a choke-input filter with two L-sections; the first L-section includes the series-resonant falter used as a shunt element instead of a shunt capacitor. The series-tuned circuit, L1 and Cl, which is made resonant at the fundamental ripple frequency, offers extremely low impedance to the ripple frequency at resonance. The bypassing action of the resonant filter to the fundamental ripple-frequency component is, therefore, much better than that obtained with a shunt capacitor alone, since the capacitive reactance (XC) of a shunt capacitor rdone will normally be greater than the impedance of the series-resonant falter. The filter circuit illustrated has the same general characteristics previously described for the L-C Choke-Input Filter, in this section of the handbook. The ripple-frequency component which remains after passing through inductor L2 is bypassed by the resonant filter, L1 and Cl; the remaining fluctuations are further smoothed by the L-section filter, L3 and C2.

The series-resonant filter must **alwyas** be used with an input inductor (L2) in series with the rectifier output. If the series-resonant filter were shunted directly across the rectifier output, the filter would act as a short circuit (low impedance to the fundamental ripple frequency) and cause extremely high rectifier peak currents to flow; these currents, in turn, would damage the rectifier. In a practical filter circuit, the inductor (Ll) is fixed in value, and one or more specific-value capacitors (Cl) are paralleled and placed in series with the inductor to obtain exact resonance at the ripple frequency. At resonance, the falter offers extremely low impedance to the ripplefrequency component, but the filter provides very little bypassing action at other frequencies; it has a progressively higher impedance, both above and below the resonant frequency, the farther the frequency is from resonance. Therefore, the **series**resonant filter is always used with additional **filter** sections to overcome this disadvantage and effectively attenuate harmonic frequencies.

## Failure Analysis.

**General.** When analyzing the failure of a resonant falter to perform satisfactorily, it should be remembered that resonance of the falter is most important, and that any change in the inductance, capacitance, load current, or applied ripple **frequency** will directly affect the filtering efficiency. The inductors used in a resonant filter can be checked for the proper value of inductance (no dc) by using an impedance bridge; the capacitors can be checked by using a capacitance analyzer.

As previously mentioned, the inductance of the inductor (Ll) employed in a parallel-resonant falter depends on the load current which flows through it; therefore, the load current must be measured to determine that the current is within tolerance in order that the parallel-resonant filter operate effectively and remain tuned to the fundamental ripple frequency.

Because a resonant falter offers little attenuation to **higher-order** ripple frequencies (harmonics), it is normally employed in conjunction with other falter sections, such as choke-input or capacitor-input falter sections. Therefore, the failure analysis procedures for a power supply filter system which contains a resonant filter are essentially the same as those given earlier in this section of the handbook for the applicable choke-input or capacitor-input filter circuit.

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# PART 4-2. SIGNAL

# **HIGH-PASS FILTERS**

## Application.

High-pass falters are universally used in circuits where it is desired to pass the higher frequencies and to attenuate the lower frequencies below a selected cutoff frequency ( $F_o$ ).

## Characteristics.

**Resistance-capacitance-type** filters are used only for audio frequencies, whereas **inductance**capacitance-type falters are used for both audio and radio frequencies, and wherever sharp cutoff is required.

The bigher the frequency above cutoff, the lower the attenuation; below the cutoff frequency the attenuation increases as the frequency decreases.

May be half-section, single-section, or multiplesection, with the multiple-section (ladder) type providing the greatest attenuation and sharpest cutoff.

May be of either the "constant K" or "mderived" form, or combinations thereof.

#### Circuit Analysis.

General. A filter consists of a circuit containing a number of impedances grouped together in such a manner that it has a definite frequency response characteristic. It is designed to permit the passage (transmit) signals freely over a certain desired range of frequencies, and to attenuate (transmit poorly) over another range of frequencies. The frequency range over which the passage occurs freely is called the pass band, (or transmission band) and the range over which attenuation (poor transmission) occurs is called the *attenuation band*. The frequency at which the attenuation of the signal starts to increase rapidly is known as the *cutoff* frequency. The basic configurations into which the high-pass filter elements can be assembled or arranged are the *L* or *half-section*, the T-section, and the Pi-section. The L-section consists of one series capacitive element and one parallel (shunt) element of either resistance or inductance, forming an inverted L (since two L-sections may be connected together to form a symmetrical T or Pinetwork it is referred to as a half-section). The T-

section consists of two series capacitive arms and one shunt arm, resembling the letter T. The Pi-section consists of one series capacitive arm with two shunt arms, resembling the Greek letter  $\pi$ . Several sections (or half-sections) of the same circuit configuration can be joined to improve the filter attenuation or transmission characteristic. When several sections are cascaded together, they form a *rirdder* type of falter. When a falter is inserted into a circuit, it is usually terminated (matched) by a resistance of the same value at the input ends. The value of the terminating resistance is usually determined by the circuit with which the filter is used and the type of filter circuit employed. In some instances, circuit parts may be arranged basically in the form of a simple falter, even though it is not desired to provide such falter action initially. For example, the simple R-C coupling network in an audio amplifier grid circuit provides a high-pass falter effect with low-frequency cutoff, and creates a design problem because equal amplification of both the low and high frequencies is usually desired. The cutoff frequency of a filter is determined by the circuit configuration, type of falter (constant kor mderived), and the values of the capacitors and resistors (or inductors) in the filter circuit. When the cutoff frequency is known, the values of the parts required to produce this response and the desired attenuation may be calculated mathematically by use of the proper formulas. This handbook will not be concerned with design data, but will show the circuit configurations, explain the circuit action, and provide information with which the technician can determine or recognize the type of filter and determine the cutoff frequency, if needed.

**Circuit Operation.** A typical half-section R-C highpass filter is shown in the accompanying illustration.



Half-Section R-C High-Pass Filter

The simple high-pass filter shown in the figure is equivalent to an R42 coupling network placed in the grid of an amplifier stage. Note that the output voltage is taken across the resistor, and the capacitor is series-connected. The circuit is basically that of a voltage divider in which C forms the reactive arm and R the resistive arm. If the value is selected so that the capacitive reactance is equal to the resistance of resistor R at frequency  $f_1$ , then the output voltage of the network will be attenuated approximately 3 dB with respect to the input voltage. This frequency is called the theoretical cutoff frequency, and its value is given by:  $\mathbf{f_1} = 1/(27rR \text{ C})$  in Hz. The values of R and C are in ohms and farads (or in megohms and rnicrofarads), and RC is the *time constant* in seconds. Thus, if the low-frequency response of an R-C-coupled amplifier is specified as having a time constant of, for example, 2000 microseconds (which is sometimes done),  $f_1$ equals 80 Hz (apply the values in the formula above and calculate). In the example, the theoretical cutoff frequency is approximately 80 Hz, and since only a simple half-section falter is used the cutoff is not sharp, but varies directly with the capacitive reactance of C. However, with a sufficient number of cascaded filters of the proper value, it could be made reasonably sharp.

Consider now a T-section filter as illustrated in the accompanying figure.



**T-Section R-C High-Pass Filtar** 

This circuit arrangement forms a full-section which can be considered as two half-sections (L-sections) placed back to back with resistor R common to both. Note that in this circuit arrangement the two capacitors are connected in series; consequently, the design value of C is doubled. Likewise, the design value of R is also doubled since the two resistors are paralleled, thereby making the effective value of R that of the single L-section. The T arrangement provides a

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symmetrical input and output with the same time constant as the single section L-type falter. A typical Pi-section falter network is shown in the accompanying figure.



**Pi-Section R-C High-Pass Filtar** 

In this full-section arrangement the value of the resistive arms is, likewise, chosen to be double that of the half-section arrangement, and C is equal to **the** total value of the two series capacitors of the T-section arrangement. Development of the Pi-section from two inverted L-section filters is illustrated in the following diagram.



**Development of Pi-Section Filtar** 

The values used are those of the basic half-section **L-filter.** Note that in any of the three previously shown falter arrangenymts the actual time constant values are identical. Therefore, " the response and attenuation of each are also identical. Lsections are used where only a simple unbalanced input and output is needed. The T- and Pi-sections are used where balanced arrangements are required. Multiple-section falters are used to obtain greater phase shift and more attenuation, Thus, a two-section falter using identical

values of parts will multiply the phase shift and attenuation by a factor of two. For complete design data refer to a standard text.

In any of the filter arrangements previously discussed, the attenuation is assumed to be zero immediately above the cutoff frequency,  $f_o$ , and very **large** for frequencies below  $f_o$ , **as** shown **in** the **following** response graph.



Phasa and Amplitude Response Characteristics for High-Pass R-C Filter (f. = 1730 Hz)

However, as can be seen from the chart, the attenuation (for a single-section filter) becomes relatively constant at about 12 dB/octave (20 dB per decade) at frequencies considerably below the cutoff frequency. The phase shift range from zero at the higher frequencies above f. to 45 degrees at  $f_o$ . **Below** the cutoff frequency the phase shift soon becomes constant at 90 degrees. The dotted line indicates how this typical Bode plot is rounded off to simulate practical conditions. As a result, a 3dB difference exists between the actual and theoretical response at the cutoff frequency.

The effect of a high-pass filter on the response of a rectangular pulse is indicative of the action produced by this type of filter. Since the output voltage of the high-pass filter is taken from across the resistor which is in series with the capacitor and the input circuit, it is evident that before the puke is applied, there is no charge in the capacitor and no current in the circuit. Therefore, no voltage output is obtained. Upon application of the rectangular pulse, the initial current is equal to E/R. Since the output voltage is equal to the current times the resistance, the output voltage also

rises instantaneously to E. Thus the rise time in this circuit is maintained without any change. However, as the capacitor charges, the current through the resistance decreases; hence, the output voltage decreases. Eventually, the capacitor charges to the input voltage and the output voltage drops to zero.

The following figure shows the over-all response of a high-pass falter to a rectangular puke of 15 microseconds duration with different time constant values (R times C). From the previous paragraph it is clear that the rise time is unaffected, as shown in the figure. When the time constant is long with respect to the pulse duration, little effect on the pulse shape is obtained. For example, with a time constant of 150 microseconds in the filter, and a pulse of 15 microseconds time duration applied to the falter input, the output voltage will drop to only 0.9 of the input voltage, as shown by the dotted line in the figure (for an RC/t ratio of 10). On the other hand, when the pulse duration is equal to the time constant, the capacitor charges to approximately 63% of its full value and the current flow through the resistor is such as to produce an output voltage of only 0.37 that of the input ( $\mathbf{RC}/\mathbf{t} = 1$  in the figure).



## Typical Pulse Rasponse Variation with Time Constant or Pulse Width Changes

When the input voltage drops to zero at the end of the pulse duration period, the output voltage of the falter is equal to the voltage across the capacitor. For instance, in the previous example of the large time constant ratio of 10, the output voltage dropped to only 0.9 of the input. Therefore, a charge of O.IE must exist on the capacitor at the end of the pulse.

The capacitor voltage is negative with respect to the input voltage since it opposes the input voltage. Therefore, when the input voltage drops to zero, the output voltage drops to -0.1E, and the capacitor then discharges to zero volts. It is evident, then, that the greater the voltage drop across the capacitor at the end of the duration period of the pluse, the greater will be the negative voltage at the output of the circuit when the input pulse falls to zero.

Since R.C falters respond to the time constant of the circuit, it is evident that while **filters** of many sections can be used, the simple equivalent time constant of the entire network will basically determine the filter characteristics, and that really sharp cutoff cannot be obtained. With the use of L-C falter circuits, however, it is possible to produce the desired pass band with a much sharper cutoff and attenuation characteristics. Since both inductance and capacitance are used, a single-section L-C falter is capable of a **180-degree** phase shift.

High-pass falter circuits using inductance and capacitance follow the same type of circuit **configura**tion as do R.C filters, as shown in the following figure.



Hi@-Pass L-C Filter Circuits

Basic filter theory stipulates that where reactance of the same sign (either all capacitance or all inductance) are used, the characteristic impedance presented by the falter to the input or output circuit is a reactance. On the other hand, where reactance of opposite sign are used (such as capacitance and inductance), the characteristic impedance becomes resistive over one range and reactive over another range. Thus the design and matching of filters becomes an engineering problem, and is treated on an ideal theoretical basis. This means that while a falter may be considered to have infinite rejection beyond a

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particular cutoff frequency, in practice the result may not be as great as predicted. Likewise, the cut-off frequency may not be as critical or as sharp as the design figures indicate.

All the previously discussed filter arrangements are of the *constant k* type, which has gradual rather than a sharp cutoff frequency. In this simple type of filter the series **filter** arm **impedance**, 21, and the shunt falter arm impedance, 22, are so related that their product is a constant at all frequencies (21 x 22 =  $k^2$ ). Therefore, it derives its name from this relationship. This constant, in turn, is also equal to R<sup>2</sup>, since Z1 and Z2 are reciprocal reactance ( $X_c$  and XL, respectively), and R<sup>2</sup> = L/C. Thus, the formula for determining the cutoff frequency becomes; f. =  $1/4\pi\sqrt{LC}$ , where L and C are in henrys and farads, respectively.

A more complex form of high-pass falter circuit is the *mderived* type. In this type the cutoff frequency is sharper and the total attenuation of the unwanted frequencies is greater. Typical circuits of the seriescomected, mderived type are shown in the following illustration.



#### Series m-Derived High-pass Filters

As can be seen from the illustration, a seriesconnected L-C network (L2C2) is placed across the output or across the mid-termination of the filter circuit. As designed, this network is made seriesresonant at a frequency below the usual cutoff frequency. For the high-pass falter this resonant frequency, called the *frequency of infinite attenuation*  $(f_{\infty})$ , is selected at a value of about 0.8  $f_{\circ}$ . Since  $f_{\infty}$  is resonant and is **series-connected** across the input or output, it represents a short circuit across the **filter**  for the resonant frequency (with a pass band determined by the Q and resistance of the circuits). Therefore, the normally sloping attenuation characteristic which approximates 12 dB/octave for the constant kfalter is "notched" off. In effect, the rnderived filter is sharply separated from the frequencies below  $f_{\infty}$ , and thereby provides sharper and better cutoff of the lower frequencies. The action described can be visualized clearly when the attenuation (response) characteristics for the two types of filters are compared, as shown in the following figure.



**Comparison of Filter Attenuation Characteristics** 

While a constant attenuation is shown for the constant k type, with a reduced value of attenuation below  $\mathbf{f}_{\infty}$  for the mderived type, the sharpness of the mderived cutoff at  $\mathbf{f}_{\infty}$  (assuming zero circuit resistance at resonance) provides better high-pass performance, as illustrated below.



**Comparison of Transmission Characteristics** 

The shunt-connected type of mderived filter is shown in the following figure.



Shunt m-Derived High-Pass Filters

In the shunt-type falter, the high-pass action occurs by passage of the signal through the filter via capacitor Cl for those frequencies above  $f_{\infty}$ , and by attenuation of the signal due to the action of the parallel resonant circuit of LIC1 at the infinite attenuation frequency,  $f_{\infty}$ . In addition, since the inductive reactance of L2 increases with frequency, the lower frequencies below f. are shunted across the output and lost. Since the parallel-resonant circuit of LIC1 represents a high impedance at resonance, frequencies around  $f_{\infty}$  (depending upon the circuit Q) are greatly attenuated and are prevented from passing through the filter. This type of operation is mostly used for the band-rejection type of filter, to be discussed later in this section.

In the mderived filter, m is a design constant from which the falter gets its name. This constant basically represents a coupling factor, and appears in all the design formulas. It is some value less than 1, usually 0.6. Thus, the frequency of infinite attenuation **18**:
$\mathbf{f}_{\infty} = \mathbf{f}_0 \sqrt{1 - m^2}$ , which for a cutoff frequency of 7000 kHz and an *m* of 0.6 is, by substituting values, 7000 x  $\sqrt{1 - 0.36} = 7000 \text{ x}$  0.8, or 56000 kHz. The cutoff frequency for the ?nderived high-pass filter is:  $\mathbf{f}_0 = 1 / (@)$ .

In this case the value of m determines the final values of L and C. When the cutoff frequency and the frequency of intlnite attenuation are known, m can be determined from the formula:

$$=\sqrt{1-\frac{f_m^2}{f_0}}$$

If the frequency values in the example above are substituted in this formula, it will **be** seen that *m* is **0.6**, **as** selected above. When *m* is equal to 1, the *m*derived falter and the constant *k* filter are identical. Values of m smaller than 0.6 move  $\mathbf{f}_{\infty}$  closer to f. (sharpen the cutoff), and values greater than 0.6 move  $\mathbf{f}_{\infty}$  farther from f. (broaden the cutoff).

In the schematic illustrations of the filter sections shown previously, various values of L and C are indicated. These indicators merely show that the design values of L and C as chosen are either that of the original value, or are multiplied by (or divided by) 2 to produce the proper total value for use in the configuration illustrated. This change of value is necessitated by the requirermmts for proper matching, and for the connection of cascaded falter sections to produce the desired performance. For example, when connecting two Pi-sections together, the input and output inductors parallel the output and input inductors, respectively, of the next or preceding section. Since inductors in parallel have half the value of the original inductance, these networks normally use a value of 2L where more than a single section is to be connected in a ladder-type network. For further information, the interested reader is referred to standard textbooks on falter design.

## Failure Analysis.

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Generally speaking, either the falter performs as designed or it does not. Any open or short-circuited condition of the individual parts can lead to one of three possibilities: the open part may cause a nooutput condition; the short-circuited part may cause a **no-output** or a reduced-output condition; or the defective part may be located in a position in the circuit that markedly affects the falter cutoff fre-

quency, pass band, or attenuation characteristics. Usually, all three of these last mentioned conditions are affected to some extent. Therefore, it becomes rather difficult to determine whether the falter is faulty and to spot the defective part with simple servicing techniques. In most instances, a check for continuity with an ohmmeter will indicate any opencircuited parts. In the case of the capacitors in the network, they can be checked with an in-circuit type of capacitance tester for the proper capacitance. Any short-circuited capacitor should be found during the resistance and continuity check. Where a lowfrequency inductor is under suspicion, the resistance may be used as a guide; but when the resistance is so low that it is less than an ohm (as in high-frequency coils), the suspected coil must be disconnected and checked in an inductance bridge.

If a falter is suspected of operating improperly and the cutoff frequency is known (if not, it can be calculated approximately by using the formulas referenced in the preceding discussion of circuit operation), a pass band check can be made with an oscilloscope (and an r-f probe) and a signal generator. With the signal generator. modulated and simulating the input signal, the output of the filter is observed on the oscilloscope (use the vertical height of the modulaion supplied by the r-f probe as an indication of relative amplitude). For a high-pass filter, the height of the pattern should decrease rapidly as the cutoff frequency is passed (while reducing frequency), and the pattern should stay at approximately the same height for frequencies above cutoff. If such indications are obtained, the filter is probably operative, and some other portion of the associated circuit is at fault. If these indications are not obtained, the falter is definitely at fault, and each part must be individually checked for the proper value.

# LOW-PASS FILTERS

#### Application.

Low-pass falters are used in circuits where it is desired to pass only the lower frequencies and to attenuate any frequencies above a selected cut-off frequency.

### Characteristics.

Resistance-capacitance (RC) type filters are generally used for audio frequency applications, whereas

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inductance-capacitance (IX) types of falters are used for both audio and radio frequencies, particularly for wherever sharp cutoff is required.

The lower the frequency below cut off, the'lower is the attenuation; above the cut-off frequency the attenuation increases as the frequency increases.

May consist of half-sections, single sections, or multiple sections, with the multiple+ection type providing the greatest attenuation and the sharpest cutoff.

May be of either the constant k or mderived form, or any combination thereof.

# **Circuit Analysis**

General. The low-pass filter circuit consists of resistance or inductance together with capacitance combined and connected in such a manner that they have a definite frequency response characteristic. The low-pass filter is designed to permit the passage of low frequency signals over a desired range of frequencies, and to attenuate the higher frequencies above this range. The frequency range over which the passage occurs is called the *pass band*, the range over which attenuation or poor transmission occurs is called the attenuation band. The frequency at which the attenuation of a signal starts to increase rapidly is known as the *cutoff frequency*. The basic configurations into which the low-pass filter elements can be assembled or arranged are the "L" or half-section, the "T" or full section, and the Pi type.

The L-section filter consists of one series resistor or inductor, and one parallel component of either resistance or capacitance. The T-type filter consists of two series inductors and one shunt resistance or capacitance, The Pi-type consists of one series inductor and two resistive or capacitive shunts, resembling the Greek letter  $\pi$  (Pi) from whence it takes its name. Several sections (or half sections) of the same circuit configuration can be joined to improve the attenuation or transmission characteristics of the falter. When several sections are cascaded together, they form a ladder type of falter. When a filter is inserted into a circuit it is usually terminated (matched) by a resistance or impedance of the same value at the input end. The value of the terminating resistance or impedance is usually determined by the circuit with which the

falter is used and the type of filter circuit employed.

The cutoff frequency of a filter is determined by the circuit configuration, type of falter (constant k or mderived), and the values of the inductors and resistors (or capacitors) in the filter circuit. When the cutoff frequency is known, the value of the parts necessary to produce this response and the desired attenuation may be calculated mathematically by the use of the proper formulas. This handbook will not be concerned with design data, but will show the circuit configuration, explain circuit action, and provide information with which the technician can determine or recognize the type of filter and determine the cutoff frequency, if needed.

**Circuit Oparation. A** typical half-section R-C lowpass **filter** is shown in the accompanying illustration.



Half-Saction R-C Low Pass Filtar

Note that the output is taken across the capacitor and the resistor is connected in series. The circuit is basically that of a voltage divider in which C forms the reactive part, and R the resistive arm. If the values are selected so that the capacitive reactance of C is equal to the resistance of R at frequency f, then the output voltage of the voltage divider network will be attenuated approximately 3 dB with respect to that of the input voltage. This frequency is called the theoretical *cutoff frequency*, and its value is given by: f. =  $1/2\pi RC$  in Hertz. The values of R and C are in ohms and farads (or in megohms and microfarads), and RC is the time constant in seconds. A similar half-section low-pass filter arrangement using inductance and resistance (R-L) is shown in the accompanying illustration.



Note that in this instance the output is taken across the resistor and that the reactance is connected

in series. The circuit also is a voltage divider in which L forms the reactive arm, and R the resistive arm. If the values are selected so that the inductive reactance

of L is equal to the resistance of R at  $f_{\scriptscriptstyle o},$  then the output voltage of the voltage divider will be attenu-

ated approximately 3 dB with respect to the input

voltage. The theoretical frequency in this instance is

found by the formula: f. = 2  $\pi$  RL, in Hertz, with R

and L in ohms and farads, and RL is the time con-

accompanying figure. This circuit arrangement forms

a full section which can be considered as two half-

sections (L sections) placed back to back.

Consider now a T-section **filter** as illustrated in the

making the effective capacitance equal to the value of a single half section. The T-arrangement provides a symmetrical input and output with the same time constant as the single-section L-type figure. A typicrd T network using RL components is 'shown **in** the accompanying illustration.



**T-Section R-L Low-Pass Filter** 

In this instance, since the inductors are in series, only half the inductance is used in each and, since the resistors are effectively in parallel, the half-section resistance value is multiplied by 2. The T-section supplies a symmetrical input and output with a time constant equal to that of the single half-section.

A typical Pi-section falter network is shown in the accompanying diagram.



**T-Section R-C Low-Pass Filter** 

Note that in this circuit arrangement the two resistors are connected in series; consequently the design value of R is halved. Likewise, the design value of C is halved, since the two capacitors are paralleled thereby



Pi-Section R-C Low Pass Filter

In this full section arrangement the vrdue of the resistive arm is equal to the value of two half sections, while the value of the capacitor is half the total value. Note that in any of the previously discussed falter arrangements the actual time constant values are identical. Therefore, the response and attenuation of each

stant in seconds.

are also identical. L-sections are used where only a simple unbalanced input and output is needed. The Tand Pi-sections are used where balanced arrangements are required. **Multiple** section **filters** are used to obtain greater phase shift and more attenuation. Thus, a two-section filter using identical values of parts **will** multiply the phase shift and attenuation by a factor of two. For complete design data refer to a standard text.

In any of the filter arrangements previously discussed the attenuation is assumed to be zero immediately below the cutoff frequency,  $f_0$ , and very large for frequencies above  $f_o$ , as **shown in** the **following** response graph.



# Phase and Amplitude Response Characteristics for Low Pass Fifter (f. = 1,000 Hz)

However, as can be seen from the chart, the attenuation (for a single-section filter) becomes relatively constant at 12 dB/octave (20 dB per decade) at frequencies considerably above cutoff. The phase shift ranges from zero at the lower frequencies below cutoff to 45 degrees at f.. Above the cutoff frequency the phase shift soon becomes constant at 90 degrees. The dotted fine indicates how this typical Bode plot is rounded off to simulate practical conditions. As a result, a 3 dB difference exists between the actuaf and theoretical response at the cutoff frequency.

The effect of a low-pass filter on the response of-a rectangular pulse is indicative of the action produced by this type of falter. Since the output voltage is taken from across the capacitor, which is in series with the resistor and the input circuit, it is evident before the pulse is applied, there is no charge in the capacitor and no current in the circuit. Therefore, no voltage output is obtained. Upon application of the rectangular pulse the initial current is equal to E/R.

Since the capacitor cannot change its charge instantly, the high charging current drops the voltage across the resistance and the output voltage rises exponentially as the capacitor charges. Thus, as the capacitor charges the current through the resistor decreases, while the voltage across the capacitor increases correspondingly. Eventually the capacitor charges to the full input voltage and the output voltage is at a maximum. The output voltage stays at this vafue for the remainder of the pufse. At the end of the pulse the capacitor discharges, also exponentially, and the output voltage eventually decreases to zero.

The following figure shows the overaff response of a low-pass **filter** to a rectangular pulse of 15 microseconds duration with different time constant values (R times C). From the previous explanation, it is clear that both the rise and fafl times of the pulse are greatly affected. The effect is least for a small time constant. For example, consider the response of an **RC** circuit with a time constant of 1 microsecond to a rectangular pulse of 15 microseconds duration,



Typical Pulse Response Variation with Time Constant or Pulsa Width Changes

Since the rise time is taken between the 10% and 90% amplitude limits of the pulse, we see from a universaf time constant table that the leading edge reaches its maximum of 9070 amplitude in 2.2 microseconds and remains approximately at this value for the remaining 12.7 microseconds (7 time constants are required to reach full amplitude). When the pulse ends, the decay time follows the same curve and the

capacitor is 90% discharged in 2.2 microseconds, and completely discharged before the beginning of the next pulse. Consider now the response curve for a 5 microsecond time constant. In this case the leading edge of the pulse rises to 90% of maximum in two time constants, the pulse is terminated and decays to zero in the next two time constants. Because of the increase of time constant the capacitor charges to only 90% of the maximum and the output voltage is **10%** less than for the 1 microsecond condition. For the extremely long time constant of 10 microseconds it takes the entire pulse duration of 15 microseconds for the pulse to reach approximately 78% amplitude. Thus the longer the time constant the lower is the output amplitude and the more distorted is the pulse.

Since RC filters respond to the time constant of the circuit, it is evident that while falters of many sections can be used, the simple equivalent time constant of the circuit basically determines the filter characteristics, and that really sharp cutoff cannot be obtained. With the use of L-C falter circuits however, it is possible to produce the desired pass band with much sharper cutoff and attenuation characteristics. Since both inductance and capacitance are used, a single-section **L-C** falter is capable of a 180 degree phase shift.

Low pass filter circuits using inductance and capacitance follow the same type of circuit configuration as do **R-C** falters as shown in the accompanying figure.



Low-Pass L-C Filtar Circuits

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In the L-type low-pass filter using L-C components the high frequencies applied to the input are offered a relatively high inductive reactance by series inductor L, and a low capacitive reactance through the shunt path to ground provided by capacitor C. Therefore, the high frequency signals are attenuated by L and effectively shunted to ground by C if they pass the inductor. On the other hand, the low frequencies are offered little opposition by L and high opposition by C. Therefore, the lower frequencies pass from input to output with little attenuation. The T-type tNter operates identically with the half section falter, but provides a symmetrical input and output configuration with the same time constant as a single section L-type filter. The Pi-type filter is actually formed from two inverted L-type falters and provides slightly better cutoff and attenuation. In this case the high frequencies are first offered a low impedance path to ground by the first filter capacitor with higb attenuation offered by the series inductor. Any remaining high frequency signals are then effectively shunted to ground by the low impedance of the second (output) capacitor. The basic Ltype falter is used where only a simple unbalanced input and output are required. The T- and Pi-types of filter are used where balanced arrangements are necessary.

Basic falter theory stipulates that where reactance of the same sign (either all capacitance or all inductance) are used, the characteristic falter impedance presented by the filter to the input or the output circuit is a reactance. On the other hand, where reactance of opposite sign are used (such as capacitance and inductance), the characteristic impedance becomes resistive over one range and reactive over another range. Thus the design and matching of filters becomes an engineering problem, and is treated on an ideal theoretical basis. This means that while a filter may be considered to **have** infinite rejection beyond a particular cutoff frequency, in practice the result may not be great as predicted. Likewise, the critical cutoff frequency may not be as sharp or as critical as the design figures indicate.

AU the previously discussed filter arrangements are of the constant k type, which has a gradual rather than a sharp cutoff frequency. In this simple type of falter the series falter arm impedance, Z1 and the shunt falter arm impedance, 22, are so related that their product is a constant at all frequencies (ZI x Z2 =  $k^2$ ). Therefore, it derives its name from this **rela**tionship. This constant, in turn, is also equal to R<sup>2</sup>,

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since Z1 and Z2 are reciprocal reactance ( $X_L$  and  $X_c$ , respectively), and  $R^2 = L/C$ . Thus the formula for determining g the cutoff frequency becomes: f. = 1/4  $\pi\sqrt{LC}$ , where L and C are in henrys and farads, respectively.

A more complex form of low-pass **filter** circuit is the *mderived* type. In this type of falter the cutoff frequency is sharper, and the total attenuation of the unwanted frequencies is greater. Typical circuits of the **series-connected** mderived type are shown in the accompanying illustration.



Sarias m-Derived Low-Pass Filters

As can be seen from the illustration, a seriescormected **L-C** network (L2C2) is placed across the input/output or across the mid-termination of the **fil**lter network. As designed, this network is made series-resonant at a frequency above the usual cutoff frequency. For the low-pass **filter** this resonant frequency, called the *frequency of infinite attenuation*  $(\mathbf{f}_{\infty})$  is selected at a value of about 1.25 f<sub>o</sub>. Since  $\mathbf{f}_{\infty}$ is resonnt and is series connected across the input or the output it represents a short circuit across the **fil**lter for the resonant frequency (with a pass band determined by the Q and resistance of the circuits). Therefore, the normally sloping attenuation **charac**teristic which approximates 12 dB/octave for the constant **k** filter is "notched" off. In effect, the mderived falter is sharply separated from the frequencies above  $\mathbf{f}_{\infty}$  and therefore, provides sharper and better cutoff of the higher frequencies. The action described can be visualized more clearly when the **attenu**ation (response) characteristics for the two types of falters are compared as shown in the following figure.



comparison of Filtar Attenuation Characteristics

While a constant attenuation is shown for the constant k type, with a reduced value of attenuation below  $\mathbf{f}_{\infty}$  for the *m*-derived type, the sharpness of mderived cutoff at  $\mathbf{f}_{\infty}$  (assuming zero circuit resistance at resonance) provides better low-pass performance, as illustrated below.



**Comparison of Transmission Characteristics** 

**The** shunt-connected type of nrderived filter is shown in the following figure.



Shunt m-Derived High Pess Filters

In the shunt-type filter the low-pass action occurs by the shunting of the high frequencies to ground via capacitor C2 for those frequencies above  $f_{\infty}$ , and by attenuation of the signal due to the action of the parallel resonant circuit of L1-C1 at the infinite attenuation frequency  $f_{\infty}$ . Since the capacitive reactance of C2 decreases with frequency the higher frequencies above f. are shunted to ground and lost. Since the parallel-resonant circuit of LIC1 represents a high impedance at resonance, frequencies around  $f_{e}$ (depending upon the circuit Q) are greatly attenuated and are prevented from passing through the falter. This type of action is mostly used for the band rejection type of falter to be discussed later in this section.

In the mderived filter, *m* is a design constant from which the filter gets its mme. This constant basically represents a coupling factor, and appears in all the design formulas. It is some value less than 1, usually 0.6. Thus the frequency of attenuation if  $f_{\infty} = f_0/\sqrt{1-m^2}$ , which for a cutoff frequency of 1000 Hz and an m of 0.6, is by substituting values,  $1000/\sqrt{1-0.36} = 1000/.8$ , or 1250 Hz. The cutoff frequency for the m-derived filter is f. =  $1/(\pi\sqrt{LC})$ .

If the frequency values in the example above **are** substituted in this formula, it will be seen that m is equal to 0.6 as selected bove. When m is equal to 1, both the constant k and the mderived falters are iden-

tical. Values of *m* smaller than 0.6 move  $f_{\infty}$  closer to  $f_0$  (sharpen the cutoff), while values greater than 0.6 move  $f_{\infty}$  farther from f. (broaden the cutoff).

In the schematic illustrations of the filters shown previously, various values of L and C are indicated. These indicators merely show that the design values of L and C are shown to be multiplied or divided by 2 to produce the proper value for the configuration illustrated. This change of value is necessitated by the requirements for proper matching, and for the connection of cascaded filter sections to produce the desired performance. For example, when comected two Pi-sections together the input and output capacitors parallel the input and output capacitors, respectively of the next or preceding section. Since capacitors in parallel have twice the value of the original capacitance, these networks normally use a value of C/2 where more than a single section is to be connected in a ladder type network, For further information, the interested reader is referred to standard textbooks on falter design.

### Failure Analysis.

Generally speaking, either the falter performs as designed or it does not. Any open or short circuited condition of the individual parts can lead to one of three possibilities: the open part may cause a nooutput condition; the short-circuited part may cause either a no-output or a reduced-output condition; or the part may be located in a portion of the circuit that markedly affects the falter cutoff frequency, pass band, or attenuation characteristics. Usually all three of these last mentioned conditions are affected to some extent. Therefore, it becomes rather difficult to determine whether the filter is faulty and to spot the defective part with simple servicing techniques. In most instances, a check for continuity with an ohmmeter will indicate any open-circuited parts. In the case of the capacitors in the network, they can be checked with an in-circuit type of capacitance tester for the proper capacitance. Any short-circuited capacitor should be found during the resistance and continuity check. Where a low frequency inductor is under suspicion, the dc resistance may be used as a guide; but where the resistance is so low that it is less than one ohm (as in high frequency coils) the suspected coil must be disconnected and checked with an inductance bridge.

If a falter is suspected of operating improperly and the cutoff frequency is known (if not, it can be calculated approximately by using the formulas referenced in the preceding discussion of circuit operation), and a band-pass check can be made with an oscilloscope and a signal generator. With the signal generator modulated and simulating the input signal, the output of the falter is observed on the oscilloscope. For a low pass falter the height of the pattern should decrease rapidly as the cutoff frequency is passed (while increasing the frequency), and the pattern should stay at approximately the same height for frequencies below cutoff. If such indications are obtained the fillter is most probably operative, and some other portion of the associated circuit is at fault. If these indications are not obtained, the falter is definitely at fault, and each part must be checked individually for proper value.

## **BAND-PASS FILTERS**

### Application.

Band-pass filter circuits are used to allow frequencies within a certain frequency band to be passed or transmitted with minimum attenuation and to block all frequencies above and below this frequency band.

### Characteristics.

### Uses **L-C type** falters.

Frequencies between lower and upper cutoff frequencies are passed with little attenuation; frequencies above and below these values are attenuated.

Series and parallel resonant circuits combined with a series or shunting inductance or capacitor are used to develop each configuration.

Attenuation and cutoff varies with the number of elements used (the greater the number of elements, the greater is the attenuation and the sharper the **cutoff)**.

### Circuit Analysis.

**General. The** band-pass falter circuit consists of inductive and capacitive components combined and connected in such a manner that they have definite frequency response characteristics. The band-pass **fil**ler is designed to permit the passage of frequencies within a desired range or band width, and to attenuate any frequencies not in this range. The range of frequencies which is capable of being passed is re-

ferred to as **pass-band**, the range of frequencies above and below the pass band, where attenuation or poor transmission occurs is called the **attenuation band**. **The** frequency at which the attenuation of a signal starts to increase rapidly is knwon as the **cutoff frequency**. **The** basic **configurations** into which the band-pass falter elements can be assembled or arranged are the "L" or **half-section**. the "T" or full-Sech"on, and the **Pi** section.

The L-section falter consists of one inductive component, capacitive component, or one combination of inductive and capacitive components in series with the input and output, together with one inductive component, capacitive components, or combination of inductive and capacitive components shunting the input and output. The T-type filter consists of two series (inductive and/or capacitive) component groups separated by one wmponent group shunting the input and output. The Pi-type consists of one series component group between two component groups shunting the input and output. Several sections or half-sections can be joined to improve the attenuation or transmission characteristics of the filter. When several sections are cascaded together, they form a *hider* type of filter. When a filter is inserted into a circuit it is usually terminated (matched) by a resistance or impedance of the same value at the input end. The value of the terminating resistance or impedance is usually determined by the circuit with which the falter is used and the type of filter *circuit* employed.

The cutoff frequency of a falter is determined by the circuit configuration, type of filter (*constant k or m derived*), and the values of the inductors and capacitors in the falter circwt. When the cutoff frequency is known, the value of the parts necessary to produce this response and the desired attenuation may be calculated mathematically by the use of the proper formulas. This handbook will not be concerned with design data, but will show the circuit configuration, explain circuit action, and provide information with which the technician can determine or recognize the type of filter and "in most cases, determine the cutoff frequencies if needed.

Circuit **Operation.** A typical half-section band-pass falter is shown in the accompanying illustration. This is a *constant k* type band-pass falter. The band-pass of frequencies is offered a low impedance by the series resonant circuit, and a high impedance by the parallel resonant circuit which shunts the input and output. The resonant circuits are tuned to frequencies within

the band-pass. All frequencies on either side of the band-pass are offered a high impedance by the series resonant circuit and a decreased impedance by the shunting resonant circuit; therefore, the frequencies outside of the band-pass are transferred with little or no attenuation. The T-type filter operates identically to the half-section or L-section falter, but provides a symmetrical input and output configuration. The Pitype filter is actually formed from two series connected inverted L-type half-section filters and provides slightly better cutoff and attenuation than the single half-section. In this case, the attenuation-band of frequencies is offered a low impedance path to ground by the first shunting parallel resonant circuit and a high impedance by the series resonant circuit. Any remaining attenuation-band frequency signals are shunted to ground by the low impedance of the second parallel resonant circuit. The basic L halfsection falter is used where only a simple unbalanced input and output are required. The T- and Pi-section filters are used where balanced arrangements are necessary,



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**Constant k Band-Pass Filters** 

The design and matching of **filters** becomes an engineering problem, and is treated on an ideal theoretical basis. This means that while a filter may be considered to have infinite rejection beyond a particular cutoff frequency, in practice the result may not be as great as predicted. Likewise, the critical cutoff frequency may not be as sharp or as critical as the design figures indicate.

All of the previously discussed falter arrangements are of the *constant k type*, which has fairly sharp cutoff frequencies, even in its simplest form. In *constant k* type falters the product of the impedance in series with the input and output, and the impedance shunting the input and output is constant regardless of the frequency (Z series  $\circ$  Z shunt = k<sup>2</sup>). Therefore, it derives its name from this relationship. This constant, in turn, is also equal to R<sup>2</sup> (R is the value of the terminating resistance). To determine the bandwidth of the pass-band of an Lsection *k* type falter, the formula f<sub>2</sub> – f<sub>1</sub> = R/L1 may be used. To determine the value of the center frequency of the band**pass** (f<sub>c</sub>), the formula f<sub>c</sub> = C1 R<sup>2</sup>/L2 may be used.

A more complex form of band-pass filter circuit is the *m*-derived type. An *m*-derived type of falter may be composed of various numbers of inductive and capacitive components in series or parallel connection within a section of the falter. An L-section *mden-ved* falter for example, may contain three, four, five, or six elements within two possible series **configurations** and two possible shunt configurations. In order to obtain the same degree of sharpness in attenuation at both upper and lower cutoff frequencies as is obtained in a *constant k* type falter an *m*-derived falter of at least 5 elements would be required. Typical circuits of one series connected m-derived type **5**element, band-pass falter are shown in the accompanying illustration.



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lower frequencies. The action described can be visualized more clearly when attenuation (response) curves for the *constant k* and the *m*-*derived* falters are corn pared as shown in the accompanying diagrams. The response of the 5 element shunt arrangement *m*-*derived* falter is the same as the 5 element series arrangement *m*-*derived* filter if the fifth element of the shunt arrangement is an'inductance and the fifth element of the series arrangement is a capacitor.



**Comparison of Filter Attenuation Characteristics** 

Series m-Derived, 5-Element Band-Pess Filter

These *m*-derived type of filters offer low series impedance, and high shunt impedance to the band-pass frequencies, since the series and shunt resonant circuits are tuned to the frequencies within the band-pass. All frequencies on either side of the band-pass are offered a greater impedance by the series resonant circuit and a decreased impedance by the shunting resonant circuit. Capacitor C3 is of such a value that frequencies below the band-pass are attenuated to a greater degree. Thus frequencies outside the band-pass are attenuated and the frequencies within the band-pass are not attenuated.

In the band-pass filter  $f_{1\infty}$  represents the *lower* frequency of *infinite attenuation* and  $f_1$  represents the *higher frequency of infinite attenuation*. At  $f_1$  and  $f_2$  the filter effectively appears as a short circuit across the output. The 5 element series arrangement of *mderived* falter (the 5th element is a capacitor) has a low frequency minimum response notch at  $f_{1\infty}$ , and therefore, provides sharper and better cutoff of the

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The constant k type filter shows equal attenuation above  $f_1$  and below  $f_1$  (the cutoff frequencies). A steep increase in attenuation is apparent between frequencies  $f_2$  to  $f_2$  + and to  $f_1$ -, however, once frequencies  $f_2$  + and  $f_1$  - are reached, the attenuation cuwe becomes more gradual until  $f_{1\infty}$  and  $f_{2\infty}$  are reached. In this case frequencies  $f_{1\infty}$  and  $f_{2\infty}$  exist at the lowest possible and highest possible frequencies. A similar attenuation slope occurs between f, and higher frequencies of the five element, *m-derived*, band-pass filter. A different slope, with a sharp minimum notch however, exists between frequency  $f_1$ and the lower frequencies in the *mderived* filter. Frequency  $f_{1}$  does not occur at the lowest possible frequency, but at some intermediate frequency above zero. Thus, the slope between  $f_{_1} \text{and} \; f_{1_{\, \varpi}}$  produces a much steeper attenuation curve than the *constant* kfilter for the lower frequencies, even though there is still a gradual widening of the slope between  $f_1$  - and  $f_{1\,\varpi},$  Between  $f_{1\,\varpi}$  and the lowest possible frequency the attenuation decreases slightly.

The shunt-connected type of five element *m*-*derived* band-pass filter is shown in the accompanying

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illustration. This shunt connected filter uses three capacitors and two inductors to comprise the five necessary components as does the series< **onnected** *m*-*derived* filter just described.





#### Shunt m-Derivad Bend-pass Filter

In this **5** element shunt *in-derived* band-pass filter L1 and Cl form a series resonant circuit at the band-pass frequencies and L2-C2 form a parallel resonant circuit. The series resonant circuit is aided by capacitor C3 in offering a low series impedance to the band-pass, and the parallel resonant circuit offers a high impedance to the band-pass. This shunt arrangement has an attenuation curve just opposite to that of the series arrangement previously discussed, where  $f_{2\infty}$  is a frequency less than a maximum frequency and  $f_{1\infty}$  is at the lowest possible frequency. By using a series arrangement with three inductive components and two capacitive components the same attenuation curve is obtained.

In the *mderived* falter, m is a design constant from which the falter gets its name. This constant basically represents a coupling factor, and appears in all of the design formulas. In the case of the band-pass falter

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there are two *m* factors. These *m* factors have a value of 1, or less and are assigned designations ml and m2. The values of *m*1 and *m*2 can be computed by complex formulas based on the quantities of the lower cutoff angular frequency  $(f_1)$ , the upper cutoff angular frequency  $(f_2)$ , and the upper and lower frequencies of peak attenuation  $(f_{2\infty} \text{ and } f_{1\infty})$ . These design formulas are beyond the scope of this book.

### Failure Analysis.

**The failure** analysis of the band-pass falters is essentially the same as that of the previously described low-pass falters. For this reason a **failure** analysis will not be repeated here. The reader is instructed to refer to the low-pass filter circuits discussion in this section of the handbook for detailed failure analysis.

## **BAND-REJECTION FILTERS**

#### Application.

Band-rejection, or band-stop, falters are used in circuits where it is desired to reject or block a band of frequencies from being passed, and to allow all frequencies above and below this band to be passed with little or no attenuation.

#### Characteristics.

Uses L-C type falters for sharp cutoff.

Frequencies between lower and upper cutoff frequencies are attenuated; frequencies lower and greater than these values are passed with little attenuation.

May be either *constant k* or *m-derived* types.

Attenuation and cutoff varies with the number of elements used (the greater the number of elements, the greater is the attenuation and the sharper the **cutoff)**.

### Circuit Analysis.

**Generel.** The band-stop filter circuit consists of inductive and capacitive networks combined and connected in such a manner that they have a definite frequency response characteristic. The band-stop filter is designed to attenuate a specific frequency band and permit the passage of all frequencies not w-ithin this specific band. The frequency range over which attenuation or poor transmission occurs is called the *attenuation band*; the frequency range over which the

passage of signal readily occurs is called the **band**pass. The lowest frequency at which the attenuation of a signal starts to increase rapidly is known as the lower **cutoff frequency** ( $f_i$ ); and the **highest** frequency at which the attenuation of a signal starts to increase rapidly is known as the upper **cutoff frequency** ( $f_2$ ). The basic configurations into which the band-elimination falter elements can be arranged or assembled are the L or half-section, the T-section, and the Pi-section.

The L-section falter consists of one parallel combination of inductance and capacitance in series with the input and one series combination of inductance and capacitance shunting the input. The T-type falter consists of two parallel combinations of inductance and capacitance in series with the input separated by one shunting combination of inductance and capacitance. The Pi-type filter consists of two series combinations of inductance and capacitance shunting the input and output separated by one parallel combination of inductance and capacitance connected in series with the input. Several sections (or half sections) of the same circuit configuration can be joined to improve the attenuation or transmission characteristics of the filter. When several sections are cascaded together, they form a ladder type of filter. When a filter is inserted into a circuit it is usually terminated (matched) by a resistance or impedance of the same value at the input end. The value of the terminating resistance or impedance is usually determined by the circuit with which the filter is used and the type of filter circuit employed.

The cutoff frequencies of a filter are determined by the circuit configuration, type of filter (*constant k* or *mderived*), and the values of the inductors and capacitors in the filter circuit. When the cutoff frequencies are known, the value of the parts necessary to produce this response and desired attenuation may be calculated mathematically by the use of the proper formulas. This handbook will not be concerned with design data, but will show the circuit configuration, *explain* circuit action, **and** provide information with which the technician can determine or recognize the type of falter and determine the cutoff frequencies, if needed.

**Circuit Operation. Band-elimination** filter circuits are shown in the accompanying illustration in L-section, T-section, and Pi-section arrangements.



Band-Rejection k-Typa Filter

In the L-section band-rejection filter any frequencies not within a selected band are offered low series impedance by L1 and Cl and offered a high shunting impedance by L2 and C2. For this reason those frequencies not within the band are easily passed from input to output with little or no attenuation. Those frequencies within the selected band are those frequencies to which L1 and Cl are resonant and L2 and C2 are resonant. The parallel resonant circuit of L1 and Cl offers a large series impedance to the frequencies within the rejection band and thus tends to block passage of these frequencies through the filter. The series resonant circuit of L2 and C2 offers almost no impedance to the frequencies within the rejection band, thus any signals in the rejection-band which may have passed through L1 and C1 are shunted across the output. Therefore, those frequencies within this band are greatly attenuated. The T-section series resonant circuits offer minimum impedance because at resonance the inductive reactance (XL) -

equals the capacitive reactance  $(X_C)$ ; and in a series circuit the impedance (Z) is equal to  $\sqrt{R^2 + (X_L - X_C)}$ . The impedance then, is simply equal to  $\sqrt{R^2}$  or R, the dc resistance of the coil. A parallel circuit offers maximum impedance at resonance. The impedance in a parallel resonant circuit can be expressed as  $Z = X_C^2/R = X_L^2/R$ , (X<sub>C</sub> being equal to  $X_L$  at resonance). By using  $Z = X_L^2/R$  the formula  $Z = X_LQ$ can be derived, since Q = XL/R. The Q of any circuit is maximum at resonance; therefore, the impedance of a parallel resonant circuit is maximum at resonance. The T-section falter operates identically to the L-section filter, but provides a symmetrical input and output configuration with approximately the same cut off and attenuation as a single L-section filter. The Pi-section falter is actually formed from two inverted L-section filters and provides slightly better cutoff and attenuation. In this case, frequencies within the rejection-band are first offered a low impedance by the first series resonant circuit shunting the input. Any remaining signal within the rejectionband that is not shunted across the input is then attenuated by the remainder of the filter in the same manner that an L-section filter attenuates the undesired frequency band. The basic L-section falter is used where only a simple unbalanced input and output are required. The T- and Pi-sections are used where balanced arrangements are necessary,

All the previously discussed falter arrangements are of the *constant k* type. In this simple type of filter the series impedance arm, Zl, and the shunt filter arm impedance, Z2, are so related that their product is a constant at all frequencies (ZI X  $22 = k^2$ ). Therefore, it derives its name from this relationship. This constant, in turn, is also equal to  $R^2$  the squared value of the terminating resistance. In these series constant k type band-rejection falters the center frequency, fc, is equal to  $1/\sqrt{LC}$ . Once the center frequency is obtained the bandwidth can be computed by the formula  $f_2 - f_1 = fc/Q$ , where Q represents the amount of selectivity of a circuit. This value of Q equals the inductive reactance of L1 divided by the value of the dc resistance of the inductor (Q =XII/R).

A more complex form of band-rejection falter circuit is the *m*-derived type. In this type of falter the cutoff frequencies ( $f_1$  and  $f_2$ ) are much sharper, and the total attenuation of the unwanted frequencies is greater. Typical circuits of the series-connected *m*- *derived* filters are shown in the accompanying illustration.



Series m-Derived Band-Stop Filters

These m-derived type of filters offer high series impedance, and low shunt impedance to the rejection-band frequencies, since the series and shunt resonant circuits are tuned to the frequencies within this band. All frequencies on either side of the rejection band are offered less impedance by the parallel circuit (Ll and Cl) in series with the input and output and greater impedance by the series circuit shunting the input and output. Inductance L2 and capacitance C2 form a parallel circuit, which is in series with L3 and C3. The values of L2 and C2 are chosen such that at some frequency, which corresponds to the lower frequency of infinite attenuation  $(f_{1})$ , their combined reactance will form a series resonant circuit with the reactance of L3 and C3. Another series resonant circuit will be formed from

these same components at the *higher frequency of infinite attenrurh*"on  $(f_{2\infty})$ . At the frequencies where these resonant points occur the attenuation curve indicates sharp peaks or notches. These resonant points are not as broad as the band-width to which L1 and Cl are tuned to resonance. Therefore, the frequencies between  $f_{1\infty}$  and  $f_{2\infty}$ , although being attenuated, are attenuated *less* than  $f_{1\infty}$  and  $f_{2\infty}$ . The action described can be visualized more clearly when attenuation (response) curves for the *constant k* and *mderived* falters are compared as shown in the accompanying illustration. attenuation decreases nonlinearly toward the center frequency. This *mderived* attenuation curve is representative of both series *m-derived* and shunt *m-derived* band-rejection filters.

The shunt *mderived* band-rejection falter is shown in the accompanying illustration. It is composed of a parallel series network in series with the input and output, and a series network shunting the input and output.





**Comparison of Filter Attenuation Cheracteristies** 

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**The constant** k attenuation curve shows gradual attenuation of signal from frequencies  $f_1$  and  $f_2$  to the center frequency fc. The attenuation on both sides is equal, causing the resulting attenuation curve to look like an inverted cone. The frequencies of **infinite** attenuation intersect at fc, and thus occur at a single frequency.

The *mderived* attenuation curve shows a much steeper and sharper attenuation at frequencies  $f_1$  and  $f_2$ . Furthermore, the attenuation slopm from  $f_1$  and  $f_2$  do not intersect at the center frequency, but reach frequencies of infiiite attenuation on both sides of the center frequency represented by  $f_{1\infty}$  and  $f_{2\infty}$ . From these frequencies of infinite attenuation the

Shunt m-Derived Band-Elimination Filter

In the shunt *mderived* band-stop filter inductor L2 and capacitor C2 are added to a *constant k* configuration band-stop filter. L2 and C2 are of such a value that they in conjunction with LI and Cl forma parallel resonant circuit at frequencies  $f_{1\infty}$  and  $f_{2\infty}$ . This causes the attenuation to increase above the normal attenuation between the cutoff frequencies  $f_1$  and  $f_2$  caused by the parallel resonant circuit C3 and L3. After  $f_{1\infty}$  and  $f_{2=}$  the attenuation decreases toward the center frequency, since L2 and C2 in conjunction with L1 and Cl are tuned very sharply to and the two frequencies  $f_{1\infty}$  and  $f_{2\infty}$ .

In the *m*-derived falter, m is a design constant from which the filter gets its name. This constant basically represents a coupling factor, and appears in all design formulas. The *m* factor has a value of 1 or less. The value of *m* can be found by the following formula: m  $=\sqrt{1-(f_{2\infty}-f_{1\infty})^2/(f_2-f_1)^2}$ .

## Failure Analysis.

The failure analysis of the band-rejection falters is essentially the same as that of the previously described low-pass filters and band-pass falters. For this reason, a failure analysis will not be repeated here. The reader is instructed to refer to the low-pass filter circuits discussion in this section of the handbook for detailed failure analysis.

# SECTION 5 AMPLIFIERS

# PART 5-0. INTRODUCTION

# **BIASING METHOOS (ELECTRON TUBE)**

### General.

An electron tube is normally biased through the application of a negative dc potential (grid bias) between the grid and cathode elements. Grid bias is either obtained from a separate voltage supply source set for a specific fixed voltage, or developed by the flow of cathode or control grid current in the tube; bias developed by tube current is referred to as "self-bias". The grid bias determines the static (quiescent) operating current for the applied plate voltage and thus sets the operating point. When an input signal is applied to the grid, it adds to or subtracts from the initial bias in accordance with instantaneous signrd variations and correspondingly varies the plate current and voltage to produce the desired output signal.

Usually bias may be obtained by any of a number of methods; the basic circuits are discussed in the following paragraphs. For ease of explanation, triode type electron tubes are used, but biasing methods are applicable to other types of electron tubes if the currents and voltages taken by the additional electrodes are properly considered.

### Cathode Bias.

When the cathode of an electron tube is biased positively with respect to the grid, the electron tube operates exactly as though an equivalent negative bias is applied to the grid. A tube using cathode bias is shown in the accompanying illustration. Since current flow within an electron tube is from cathode to plate, cathode resistor  $R_k$  can be inserted between cathode and B- to produce a voltage drop (cathode bias) as long as the plate current flows continuously. Since cathode current always flows in the same direction, the voltage drop remains more positive at the cathode. Thus plate current flow within the electron tube itself produces a positive cathode bias. The amount of bias obtained depends upon the total tube current and the **size** of the cathode **resistor** (ilk.Rk).



Cathode Bias

This type of bias is restricted in use to amplifiers in which plate current flows for more than half of each cycle of operation, because plate current flow cannot be cut off, or the developed bias will be lost. But it can be used in combination with a **fixed** minimum bias to limit maximum plate excursions or as a potective bias which limits plate current to a safe value when grid drive is removed. An inherent disadvantage of this circuit is that the developed bias voltage is subtracted from the plate voltage applied to the electron tube. This if 30 volts cathode bias is needed with a 250-volt plate supply, the power supply must be able to furnish 280 volts, as shown in the accompanying illustration.



**Bias Voltage Divider Network** 

Its greatest advantage is that it is simple to use and economical of parts. When used in audio, video, or radio-frequency circuits, the cathode resistor must always be adequately bypassed to prevent a constant change of bias with signal. If the cathode is not bypassed, any change in plate current will produce a corresponding change in cathode bias voltage. The change in cathode voltage will be in such a direction as to oppose the effects of the input signal, and therefore will have the same effect as degenerative feedback. While a controlled amount of degenerative feedback can be beneficial in extending the over-all frequency response and in reducing distortion, a large amount of degenerative feedback will result in a serious loss of amplification. When the cathode bias resistor is adequately bypassed, the fluctuating ac plate current caused by the input signal is effectively shunted around the cathode bias resistor, through a much lower reactance path offered by the bypass capacitor. Thus only the dc component of plate current flows through the bias resistor, and the total cathode current remains constant at the initial static (de) value of no-signal current, and is unchanged by the varying input signal. For satisfactory bypassing, the bypass reactance should be about 10% of the dc bias resistance at the lowest frequencies used. Cathode bias is usually used in audio-frequency or video-frequency amplifiers and in low power r-f amplifiers and test equipment. In some applications, such as high fidelity audio amplifiers or video i-f amplifiers, a relatively small value of unbypassed cathode resistance may be used. The degenerative action of this resistance increases the fidelity (frequency response) of the stage and reduces the possibility of overloading from strong signals.

# Grid-Leak Bias.

Grid-leak bias, sometimes called *signal bias*, is obtained by allowing grid current flow, produced by the ac input signal, to charge an R-C network in the **grid**cathode circuit. Two basic circuits are used to develop this form of bias–the shunt type and the series type. These two types are shown in the accompanying illustration. The methods of developing grid voltage in these circuits are similar, but the physical connections of the network components are different.







series Grid-laak Bias

The grid-cathode circuit is used as a diode rectifier to develop a dc voltage that is proportional to the positive peak input (driving) signal amplitude. Gridleak capacitor  $C_c$  operates as a coupling capacitor to apply the input (driving) signal to the grid. On the positive input signal excursions the grid is driven positive causing grid current to flow between grid and cathode and through grid-leak resistor  $\mathbf{R_g}$ . The result is to produce a dc voltage across  $\mathbf{R_g}$  which is polarized negatively at the grid. The grid-leak capacitor, CC, is effectively connected in series with the applied input signal, as shown by the equivalent charging circuit shown in part A of the accompanying illustration.

As long as the input signal remains positive, the <sup>-</sup> coupling capacitor charges. When the input signal

becomes negative (part B of the illustration), grid capacitor C<sub>c</sub> begins discharging through the grid leak; during the discharge period the grid is held negative by the charge remaining in the capacitor plus the negative input signal, and no grid current flows. The grid-leak time constant is made long with respect to the signal frequency (usually seven times the period for one input cycle) so that the discharge is relatively slow. The charge time is much faster than the discharge time because the grid leak is effectively shunted by the flow of grid current and offers a low resistance of about 500" ohms (rgk, part A) in comparison with the large resistance of  $\mathbf{R}_{\mathbf{g}}$ . When the signal begins its next positive excursion, C again starts to charge while still retaining a certain amount of residual charge. The cycle resumes and the action is repeated. After only a few more cycles, the grid bias stabilizes, since only a small portion of each charge leaks of before the application of the next positive half of the input signal. The residual charge on the coupling capacitor will not permit the next positive portion of the input signal to drive the grid as far positive as the positive portion did in the first half cycle. Thus the additional charge placed on C is not as great as it was for the first half cycle, but when added to the residual charge that remained, it causes the total bias to increase. This process of rapid charging and slow discharging of C<sub>c</sub>leads to the steady state condition of operation, in which the

amount of charge deposited on each positive half cycle exactly equals the amount of charge lost through discharge on each negative half cycle.



Simplified Charga and Discharga Circuits

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The amount of bias developed in this manner depends upon the amplitude and frequency of the applied input signal and the time constant of the grid network. The greater the amplitude of the input (grid-driving) signal. the greater the amount of bias that will be developed. Also, the longer the time constant of the grid circuit with respect to the input frequency, the greater the amount of bias that will be developed. However, there are practical limitations to the length of time constant which maybe employed. Too long a time constant will prevent the bias voltage from changing enough during a cycle, or group of cycles, to bring the stage out of cutoff. Therefore, the stage must wait until the bias has been reduced enough to allow it to come out of cutoff; as a result, the stage will operate intermittently (motorboat). When functioning properly, a grid-leak bias network should **produce** a dc voltage that is approximately 90% of the applied positive peak voltage. Under these conditions grid current will flow for only a small portion of the positive peak of the input cycle. Plate current, however, may flow for the entire cycle or for only part of the cycle, depending upon the amplitude of the input signal and the cutoff voltage of the electron tube.

Since the amplitude of the developed grid-leak bias is determined by the driving-signal amplitude, it is evident that Class A, B or C operation may be achieved with grid-leak bias merely by increasing the amount of drive (and by selecting the proper RC value). The limiting factor in this application is the amount of distortion that may be tolerated, because the plate current will be distored for the portion of the cycle during which grid current flows. It is important to remember that grid-leak bias is developed by the rectification of the input (driving) signal and that loss of the input signal will result in a complete loss of this form of bias. In power amplifier circuits where loss of bias means excessive tube currents and possible damage, a second method of biasing (either freed or cathode bias) is usually employed as a protective feature.

The shunt type of grid-leak circuit is also used to develop contact bias, which also derives its bias from the flow of grid current, but does not require an input or driving signal to produce it. Since the heated cathode is placed very close to the metal structure of the control grid, a small potential difference called contact potential is generated between the cathode and the control grid. Random electron collisions with the grid structure, aided initially by the electrically neutral character of the grid, are the major contributors to contact potential. In diodes a contact potential exists between plate and cathode. The contact potential may be on the order of 0.5 to 1 volt depending upon the structure of the tube, emission characteristics, etc. The 6AT6 and the 6SQ7 are typical examples of the tube types frequently operated with contact bias. The distinguishing feature of contact bias is the extremely high value of grid resistance used. This high value is required because of the minute currents and small potentials involved (with 10 megohms of grid resistance only one microampere of current will produce 1 volt of grid bias). Capacitor C<sub>c</sub>(see preceding illustration of shunt gridlead bias) isolates the grid from the preceding circuit as far as the dc bias is comected, but permits the application of an ac signal to the grid. Contact bias is usually limited to circuits which operate over very small grid swings, say one volt peak to peak, such as an audio preamplitier, or a driven oscillator in which it is desired not to have dc flow through the tuned circuits. Circuits employing contact bias are sensitive to overloading, because any grid current flow due to excessive signal swing will block the tube with a "signal bias" which requires considerable time to leak off through the very long time constant grid network, R<sub>e</sub>C<sub>c</sub>.

The series grid-leak circuit employs a parallel  $R_g C_g$ combination in series between grid and cathode (see preceding illustration of series grid-leak bias). Usually grid resistor  $\mathbf{R}_{\mathbf{p}}$  is in the range of thousands of ohms (rather than megohms). This type of circuit is almost universally employed in the self-excited type of oscillator because of its self-regulating and self-starting action. Once the operating point is fixed by the value of  $\mathbf{R}_{\mathbf{g}}$  and  $\mathbf{C}_{\mathbf{g}}$  employed, the tube continues to oscillate about the grid operating point whether it be Class A, B, or C. If the amplitude of oscillations in the grid tank tends to increase, an increase in positive grid drive will occur causing the grid to draw more current. The increase in grid current will develop an increased bias and a consequent decrease of plate current which tends to reduce the plate current pukes back to their original amplitude. A similar sequence of events occurs if the grid drive tends to decrease, but in this event less bias is developed, so that the plate current pulses are increased, returning them toward their original amplitude. Bias is initally developed by the contact potential method during the first few oscillations, allowing the circuit to be selfstarting. Then as the grid swings become greater, the capacitor is charged and discharged at the repetition rate of the tuned circuit, and the grid bias is determined by the time constant of the grid circuit and the value of the grid-voltage swing at that instant, averaged over a number of cycles of oscillation. Thus, if the grid capacitor is increased in value, the grid-leak resistance must be reduced to retain the desired charge and discharge rates. When the grid capacitor is sufficiently large and the grid leak resistance is adequate, quite a large voltage can be produced, and if the discharge rate is slow enough, plate current cutoff can be obtained to produce Class B or C operation. Thus this bias method is ideal for oscillators which are self-excited (produce their own feedback). In separately driven oscillators (buffer amplifiers), the shunt (signal) bias methods is used, and the bias voltage required is obtained by supplying sufficient grid current drive from the preceding stage.

# Fixed Bias.

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There are a number of methods of obtaining **fixed** bias. The most obvious of these methods is the use of a separate C-battery or a separate negative power (C-) supply. Two other widely used, but not so obvious, methods are shown in the following illustrations. The advantage of these methods is that they both use the

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equipment power supply to produce the fixed bias, so that no separate supply is necessary.



Fixed (Voltage-Divider) Bias

The freed-bias circuit utilizes potentiometer R2 connected in series with resistors RI and R3 to form a voltage divider between B+ and B-. The cathode of the tube (s) being biased is comected to the moving contact of R2, and the grid is returned through  $\mathbf{R_g}$  to B-. Resistors RI and R3 determine the voltage range over which potentiomenter R2 operates. Thus for cutoff bias a positive cathode bias is produced by the voltage divider. For a bias less than cutoff the cathode current passing through R3 and the active portion of R2 determine the operating bias. Bypass capactor  $\mathbf{C_k}$  shunts the portion of the resistance affected by cathode current to present bias changes with signal current variations, as explained in the previous discussion of cathode bias.

The back-bias circuit uses the entire current flow of the power supply to develop a fixed "back-bias". The term *back-bias* refers to a combination of self (cathode) bias and fixed bias from another source. In this instance the self-bias is obtained from the cathode current of the tube being biased. The freed bias is obtained from the total power supply current and the fixed bias resistor connected in series with the negative supply lead and chassis. There are two variations to this circuit, one using resistor R1 alone and the other using the dc resistance of the loudspeaker field coil L (or a separate choke coil) to act as R1. Use of the latter variation results in an economy of parts since the field coil also provides the bias. The backbias circuit produces its result by virtue of the connection of the negative B supply lead to the chassis through field or choke coil L and resistor RI, when used. Since all of the tubes on the chassis have their cathodes grounded, the entire chassis current passes through the choke (and resistor) to B-. The voltage

drop across the choke coil (and Rl) is the bias. If more bias is required, more current is returned through the chassis, or resistor R1 is added to produce the required voltage drop. It is usually necessary to use a decoupling falter (R2, C4 part B to prevent power supply ripple voltage from appearing on the grid. When more than one stage uses back bias  $(E_{cc})$  a decoupling **filter** at the grid of each stage is necessary to prevent signal voltage fluctuations on the grid of one stage from affecting operation of the other stages through common impedance coupling. Where more than one value of fixed bias is necessary to suit the requirements of the individual stages a voltage divider arrangement may be used. In the case of equipments requiring large negative bias voltages a separate negative power supply is usually used to obtain the bias.



BACK BIAS CIRCUIT



Back-Bias Circuit

# **BIASING METHODS (SEMICONDUCTOR)**

### Generel.

Basically, a transistor consistor consists of two junction diodes placed back-to-back with the center element being common to both junctions. Connecting the common elements of two junctions together externally will not produce proper results, but when manufactured as one piece, the PNP junction transistor can be considered as such for ease of understanding. The diode junctions of the transistor are biased with dc potentials, emitter to base in a forward direction, and collector to base in a reverse direction.



Forward- and Reversa-Biasad Junctions

Transistors are made of NPN materials, as well as PNP materials. Current flow in one type is in exactly the opposite direction to that in the other type, and biasing polarities are reversed. Otherwise, they operate identically except that the internal current flow in the transistor is considered to be the result of hole conduction for the PNP type and electron conduction for the NPN type. AU external flow in a transistor circuit is electron flow as in the electron tube. A more detailed discussion of transistor action follows below.

# TRIODE COMMON-BASE CIRCUITS

In the common-base circuit, the input signal is injected into the emitter-base circuit, and the output signal is taken from the collector-base circuit, with L

the base element being common to both. The common-base circuit is equivalent to the electron tube grounded grid circuit. It has a low input resistance (30 to 160 ohms) and a high output resistance (250K to 550K), and is mostly used to match a lowimpedance circuit to a high-impedance circuit. It has a maximum voltage gain of about 1500 and a current gain of less than 1, with a power gain of 20 to 30 dB. There is no phase reversal between input and output signals; both signals are in-phase and of the same polarity. (That is both the input and output voltages move in the same direction, starting from zero at approximately the same time, throughout the complete positive and negative alternations. When the input signal is positive, so is the output signal, and vice versa.)

It is common practice to speak of a change of phase between an input and an output signal in both electron tube and semiconductor discussions when what actually occurs is only a change of polarity. Actually, in the semi-conductor, when a long transit time occurs (with respect *to* the frequencies being amplified), the output signal is delayed in starting because of the finite time taken for the input signal to reach the output terminal. This delay (transit time) produces an actual phase (time) difference between the input and output signals even through the polarities may be identical, or even opposite.

The common-base connections for PNP and NPN transistors are shown in the accompanying figures, together with polarities and external current paths. Emitter-base bias and collector-base bias are obtained from separate sources so that two voltage sources are required. With this type of connection, it is possible to ground the base directly for both ac and dc, if desired. The circuit for a single voltage source will be discussed later.



**PNP Common Base Circuit** 



NPN Common Basa Circuit

The semiconductor device symbol is used in the figures rather than the graphical transistor symbol for ease of presentation and understanding, since it better indicates the functioning and construction of the device. Both the PNP and NPN circuits are shown together so their operation can be more easily compared. Both circuits are forward-biased from emitter to base, and reverse-biased from collector to base. The polarities of the two circuits are opposite because the transistors are of opposite composition, and the currents in the external circuit flow in opposite directions. Note that in the PNP circuit the external current (electron) flows from emitter to collector, while in the NPN circuit it flows from collector to emitter. Internally, however, the flow is always from emitter to collector through the base region. (Current theory explains the internal flow through the medium of "holes" for PNP transistor and "electrons" for the NPN transistor.) There is one current from emitter to base and another from collector to base: in some instances these currents combine and in other instances they oppose each other, depending upon circuit configuration, biasing, and applied signal voltages. The emitter current is always greater than the collector current, and the algebraic difference between the two is the base current. The base current will be discussed when it is relevant to circuit action; otherwise, it will be ignored since it is a very small portion of the total current involved. In the junction type transistor, about 95 percent of the emitter current always reaches the collector. Transistor action is dependent entirely upon the fact that the signal applied to the low-impedance input (emitter) circuit causes a current flow change which, when transferred to the high-impedance output (collector) circuit, produces a voltage gain. The current gain (a) of the commonbase circuit is defined as

$$\alpha = \frac{\Delta I_{\rm C}}{\Delta I_{\rm E}}$$

or the ratio of a small change in emitter current to a small change in collector current produced by the emitter current change. It is always less than one.

A brief discussion of the basic current flow in a transistor is included at this point because the flow of current, both internally and externally, are important to a complete understanding of circuit action. The following figure illustrates the current flow in each junction separately and in the complete transistor.



**Transistor Current Flow** 

In part A, current flow is shown for the emitterbase junction with forward bias applied and the collector open-circuited. The flow externally is by electrons from the emitter to the base. Internally the flow is from emitter to base through the majority hole carriers and from base to emitter through the minority carriers. Assuming a value of 1 milliampere for the emitter current,  $I_E$ , the base current,  $I_B$ , is approximately the same because the collector is open (neglecting any external or internal leakage currents). The hole current predominates, there being on the order of 200 hole carriers to 1 electron carrier because of the P-doping effect. Since one milliampere of current amounts to 6.28 x 10<sup>15</sup> carriers per second, it can be said that the internal emitter current flow consists of 6.24 x 10<sup>13</sup> holes per second plus  $3.14 \times 10^{13}$  electrons per second, and the external flow is 6.28x 10<sup>15</sup> electrons per second.

In part B, the emitter is open-circuited and the collector-base junction is reverse-biased. Since reverse bias reduces current flow to a minimum, the collector current,  $I_C$ , is actually  $I_{CO}$ , the reverse leakage curcurrent from collector to base, plus any surface leakage effects, which are neglected in this discussion. Internally, there is a hole current from base to collector (minority carrier) plus an electron flow from collector to base (also a minority carrier). The minority carriers are the cause of current flow because of the reverse bias; the actual current flow is very small, being on the order of 20 microampere (or less) for a typical transistor. Since the emitter is open, there is no flow from emitter to collector, and the base current,  $I_B$ , is approximately the same as  $I_{co}$ .

In part C, both the emitter and collector circuits are completed, forward bias is applied to the emitter, calling for strong current flow, and reverse bias is applied to the collector, calling for minimum current flow (considering junction biasing only). However, because of the reverse bias on the collector, the col- lector is connected to the negative supply source. Therefore, the potential hill across the collector junctions is reduced, providing an attraction for the hole current diffusing through the base from the emitter. Thus, an easy flow of hole current is permitted and it accounts for most of the emitter current transfer from emitter to collector. As a result of base injection, however, there is an electron current flow from the base to emitter which cannot be collected through the collector because the collector junction barrier polarity opposes conduction of negative charges. There is also a recombination current which consists of holes that flow into the base; these holes

combine with electrons before reaching the collector and thereby cause an electron flow in the base lead and into the base. This current represents a loss, and reduces the amount of emitter current that can reach the collector. The current through the collector junction consists of the emitter current which is permitted to reach the collector, plus the reverse leakage current,  $I_{co}$ . Assuming that 95 percent of the emitter current reaches the collector, the total current can be represented mathematically by a coefficient  $\boldsymbol{\alpha}$ (alpha) times  $I_{\mathbf{E}}$  plus the saturation current  $I_{co}$ ; that is,

$$\mathbf{I}_{\mathbf{C}} = \boldsymbol{\alpha} \mathbf{I}_{\mathbf{E}} + \mathbf{I}_{co} \tag{1}$$

The base current is the difference between the portion of the emitter hole current that does not reach the collector (the group of holes which recombine with electrons in the base) and the saturation current. Therefore the expression for base current is:

$$\mathbf{I}_{\mathbf{B}} = (\mathbf{I}_{\mathbf{E}} - \alpha \mathbf{I}_{\mathbf{E}}) - \mathbf{I}_{\mathbf{CO}} \text{ or } \mathbf{I}_{\mathbf{B}} = \mathbf{I}_{\mathbf{E}} (\mathbf{1} - \alpha) - \mathbf{I}_{\mathbf{CO}}.$$
(2)

Using the values of base current (20  $\mu\alpha$ ), emitter current (1000  $\mu\alpha$ ), and alpha (.95) assumed previously, and substituting them into formula (1) gives the following result:

$$I_c = .95 (1000) + 20 = 950 + 20 = 970 \mu \alpha$$

Using formula (2) for base current and substituting:

$$I_{\mathbf{R}} = 1000 \ (1^{-}.95)^{-}20 = 50 \ '20 = 30 \ @$$

It can be seen from the numerical example that the value of the recombination current is 50  $\mu\alpha$ , that the base current is the difference between the recombination current and  $I_{co}$ , that the collector current is the sum of  $I_{co}$  and  $\alpha I_E$  and that the various internal currents can be made equal to the external currents. In the example above, the external current is that indicated in the figure, and is an electron flow from emitter to collector with a small amount also flowing into the base. The discussion has assumed srnaU-signal conditions and the use of a PNP transistor in the common-base connection. When other configurations such as common-emitter and common-collector circuits are used, the values of current change somewhat because of the differences in input and output connections and the current paths between them. When

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the NPN transistor is employed, operation is the inverse of that for the PNP transistor, with electrons acting as majority carriers and holes as minority carriers. For large-signal conditions, operation is slightly different and will be discussed at the appropriate point in the circuit discussions in other sections of this handbook.

The PNP Common-Base Circuit (shown previously) shows a small input signal (Veb) applied to the emitter-base junction of the PNP transistor. The circuit is considered to be biased so that it operates over the linear portion of its dynamic transfer characteristic, and is resting in a quiescent state in accordance with the dc potentials applied (similar to electron tube class A operation). Assuming a sine-wave input, it is apparent that as Veb increases to its maximum positive value the forward-bias between emitter and base is increased, causing the emitter-base junction to produce an increased current flow, which passes through the external circuit and eventually through collector load resistor  $\mathbf{R}_{\mathbf{C}}$  The increase of current through  $\mathbf{R}_{\mathbf{C}}$  causes an increased voltage drop in the positive direction, so that as the input signal reaches its positive maximum so does the output signal. Therefore, both signals are always in phase and of the same polarity.

On the negative swing of the input signal, as the negative signal voltage is added to the positive forward bias, the result is a reduction of the bias and less emitter current flows. [n turn, a reduced collector current flow through  $R_C$  results in a decreased voltage drop across  $R_C$  and produces  $\alpha$  reduced output voltage; the negative going output signal remains effectively in phase with the same polarity as the input signal.

The NPN circuit (shown previously) functions similarly but inversely to the PNP circuit, that is, on the positive swing of the input voltage, the collector current is reduced, and the drop across  $\mathbf{R}_{\mathbf{C}}$  is less negative (or more positive). On the negative input cycle forward bias is increased, and the collector current produces a greater negative drop across  $\mathbf{R}_{\mathbf{C}}$ ; thus the output voltage also follows the input voltage in phase and polarity.

### Bias (Common Base).

Transistors are normally biased by placing a forward voltage on the emitter-base junction (increasing the bias voltage causes increased emitter and collector current flow), and a reverse polarity voltage on the collector junction. The operating (or bias) point is determined by specifying the dc, no-signal (quiescent) vahres of collector voltage and emitter current. Biasing circuits and arrangements are varied; separate supplies such as batteries are commonly used, as well as so called self-bias arrangements, voltage dividers across the collector supply, and other transistors or diodes.

The common-base circuit is usually restricted to the use of separate bias for the emitter-base junction or to a voltage-divider arrangement using a single voltage supply which serves as the collector-base supply also. The following illustration is a typical singlesupply type of arrangement. Resistors RI and R2 form a voltage divider across the collector supply, with the base connected at their junction and the emitter connected to the high side of the supply. Thus the emitter is always at the highest potential, the base is at a lower potential because of the voltage drop across RI due to the current from the supply source flowing through the voltage divider, and the collector is at the lowest potential. The difference in potential between the emitter and base represents the forward bias applied to the emitter-base junction. For a PNP transistor, as shown, forward bias is achieved by making the emitter positive with respect to the base; for an NPN transistor, the polarity of the source is reversed, and the emitter is negative with respect to the base. Although the value of RI is normally low, it may be necessary in some cases for R1 to be bypassed with a very-low reactance capacitor, to assure that the base is well grounded for ac.



Single-Source, CB Fixed-Bias Circuit

The common-base configuration offers almost ideal thermal compensation, since the input resistance  $(\mathbf{R}_{\mathbf{F}})$  in the emitter circuit acts as a swamping

resistor, and changes in collector current with temperature are minimized by low base-to-emitter resistance. See the paragraph on Diode Circuits later in this section for a discussion of diode circuits used for stabilization of bias; refer to the discussion below on Triode Common-Emitter Circuits for a discussion of emitter swamping resistors.

# TRIODE COMMON-EMITTER CIRCUITS

In the common-emitter circuit, the input signal is injected into the base-emitter circuit and the output signal is taken from the collector-emitter circuit, with the emitter element being common to both. The common emitter is equivalent to the electron tube grounded-cathode (conventional) amplifier circuit. It has a somewhat low input resistance (500 to 1500 ohms) and a moderately high output resistance (30 K to 50 K or more), and is the most commonly used transistor circuit configuration. It is widely used for a number of reasons. Because the input signal is applied to the base rather than the emitter, a considerably higher input impedance is obtained than in the common-base circuit. High power gains are obtainable (25 or 40 dB), and an actual current gain is possible (from 25 to 60 or better). The actual voltage gain is slightly less than that of the common-base circuit because of the higher input impedance, but this is partially off-set by the current gain; in practice, vohage gain values of 300 to 1000 (or better) are obtained. Because the signal is applied to the base, a polarity reversal takes place, making the output signal of opposite polarity to the input signal, as in the conventional electron tube amplifier.

The common-emitter connection for PNP and NPN transistors is shown respectively in the following figures, together with polarities and *external* current paths. Base emitter bias is obtained from a separate supply than that of the collector-base junction so that two voltage sources are required. With this type of supply comection it is possible to directly ground the emitter both for ac and dc, if desired. Single voltage supply circuits will be discussed later. The PNP and NPN circuits are shown together for ease of comparison of operation. Both circuits are forward-biased from emitter to base and reverse-biased from collector to emitter. Current flow and polarities in both circuits are **opposite** because of the difference in material from which the transistors are manufactured.



**PNP Common-Emitter Circuit** 



### **NPN Common-Emitter Circuit**

Current flow is from the emitter to the collector through the base region as in the common-base connection, and, likewise, only a small amount of current is diverted in the base-to -emitter circuit. Transistor action also depends on the fact that a small change of current in the low-resistance input circuit produces a voltage gain when applied to the high-impedance output circuit. But unlike the common-base circuit, the current gain is not based on the emitter-to-collector current ratio alpha ( $\alpha$ ); instead it is based on the **base-to-collector** current ratio beta ( $\beta$ ) because the signal is injected into the base, not the emitter. Therefore, since a small change of base current controls a large change in collector current, it is possible to obtain considerable current gain (a value of 60 is not unusual). Since the collector load resistance,  $\mathbf{R}_{\mathbf{C}}$  is less than the load resistance of the BC circuit, less voltage gain might be expected. However, the increased current in the collector produced by current gain off-sets the loss of output resistance, so that the voltage gain is nearly comparable to that of the CB circuit. By manipulation of circuit constants and selection of transistors, the voltage gain can be made to exceed that of the **CB** circuit.

Beta is defined as

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

with  $V_{\rm c}\, \text{constant},$  and is related to alpha of the CB circuit by

$$\beta = \frac{\alpha}{1 - a}$$

thus the closer  $\boldsymbol{\alpha}$  is to 1, the large is  $\boldsymbol{\beta}$ ; as  $\boldsymbol{\alpha}$  approaches 1,  $\boldsymbol{\beta}$  approaches infinity.

A small input signrd is applied to the base of the PNP transistor. The circuit is biased to operate over the linear portion of its dynamic transfer characteristic, and rests in a quiescent state determined by the static dc potentials applied (similar to electron tube class A operation). Assuming a sine-wave input, it is apparent that, as veb increases to its maximum positive value, the forward bias is reduced, less current flows in the emitter and collector circuits, and the drop across the collector output resistor  $(\mathbf{R}_{\mathbf{C}})$  becomes less, producing a negative-going voltage. Conversely, as the input signal swings negative, the forward bias is increased and more emitter and collector current flows. The increased voltage drop across  $\mathbf{R}_{\mathbf{C}}$  is in a positive-going direction, and the output signal reaches a positive maximum. It is evident that, since the output signal is at a positive maximum when the input signal is at a negative maximum and vice versa, the input and output polarities are exactly opposite. Therefore, the common emitter circuit is similar to the vacuum-tube common-cathode circuit, producing a polarity reversal of the input signal (although not strictly accurate, this polarity reversal is commonly spoken of as a phase difference).

The NPN circuit shown functions similarly but inversely to the PNP circuit. That is, when the input signal is positive, the forward bias is increased, and the collector current increases and produces a negative-going output across  $R_c$ . On the negative input cycle, the collector output is positive; therefore, this circuit also produces an out-of-phase signal of opposite polarity. It is evident, then, that the *common-emitter circuit always produces a polarity reversal of the input signal*.

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# Bias Circuits (Common-Emitter).

**Because** the common-emitter circuit is more frequently used, it has a greater variety of biasing schemes than the other configurations. The basic principles though remain the same; that is, the emitter-bias junction must be forward-biased while the collector-base junction is reverse-biased, and the dc no-signal values of base current and collector voltage specify the operating point.

The following illustration is a method of using to supply sources to produce a PNP emitter-base bias arrangement which series-aids the collector supply. It is evident that the emitter-base bias voltage is the vohage of the emitter-connected source, while the collector-emitter voltage is the total voltage between emitter and collector, 'or both sources in series. For an NPN transistor the polarities are reversed.



Series-Aiding Bias Circuit, PNP

The connections for a single voltage supply source biasing arrangement are shown in the accompanying illustrations.



Voltage-Divider (Fixed) Bias, CE Circuit



PNP Intarnal Self-Bias CE Circuit

The first figure is a voltage divider **fixed-bias** arrangement, with RI and R2 connected across the collector supply, and the base connected at their common connection. Thus the base is kept at a lower positive potential than the emitter and is therefore negative with respect to the emitter.

The second figure is a self-biasing arrangement which involves the internal resistance inherent in the transistor junctions; it is similar to the contact bias of the electron tube. The emitter is at the higher positive potential, and the collector is at the lowest negative potential, so the emitter-collector relationships are correct. Since the base is sandwiched between these elements and floating, it is at some intermediate value, determined by the internal resistance parameters and the internal current flow. The potential between the emitter and base must be kept to a small vahre compared to that between the collector and base. This is achieved internally by the high-resistance action of collector-base junction and the lowresistance action of the emitter-base junction, which provide the desired voltage relationship The supply voltage polarity is reversed for NPN transistors. By placing resistor R<sub>B</sub> (shown dotted) from base to emitter, the base is effectively biased off and less base current  $(I_B)$  flows. The collector current is reduced bv

$$\frac{1}{1-\alpha}$$

for each  $I_B$  microampere, and more economical operation is achieved by reducing the battery drain. A variation of the self-bias arrangement using

external resistors is shown in the following illustration. Here the bias supply is connected in series with the emitter, and the voltage divider made up of  $R_{a}$  in series with the internal emitter-base resistance, determines the proper bias potentials. The voltage across  $R_{a}$  is subtracted from that of **the** bias supply to determine the actual input bias. Collector resistor **R**<sub>C</sub> is chosen to produce the desired operating collector voltage. The polarity of the supply voltage is reversed for NPN transistors.



**PNP External Self-Bias CE Circuit** 

## **Bias Stabilization.**

The discussion of the diode stabilization circuits paragraph, together with the discussion in this paragraph, covers basic thermal stabilization circuits. Since a number of variations of the circuits discussed below are possible, any other special circuits will be discussed in the sections of this manual as they appear. Stabilization as discussed here will be confined to thermal considerations; voltage stabilization is discussed later in this section in the paragraph titled **Dwde Voltage Stabilizatwn**.

The no-signal, dc values of collector voltage and emitter current are determined by the applied bias, which sets the operating point of the transistor. Under ideal conditions temperature would not affect the bias and the circuit would be thermally stable. Actually, however, a temperature increase causes an increase in the flow of reverse-bias collector (saturation) current  $(I_{CBO})$ , and the increase in  $I_{CBO}$  causes the temperature of the collector-base junction to increase with a consequent increase in saturation current. As this action continues, distortion occurs, and the transistor is rendered inoperative or it destroys itself. To reduce thermal instability (runaway), low values of resistance, rather than high values, must be employed in the base circuit. For a discussion of a reverse-biased diode which decreases its resistance with an increase in temperature, refer to the para-

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graph titled **Reverse-Biased Dwde Stabilizatwn**, later in this section.

Another consideration is that the **emitter-base** junction of a transistor (or a diode) has a negative temperature coefficient. That is, as the temperature increases the emitter-base resistance decreases, causing a larger flow of collector current in addition to the flow of saturation current discussed above. To correct this condition  $R_{\rm E}$ , a large-value resistor (swamping resistor), is placed in the emitter circuit, where it produces a resistance stabilizing effect (see accompanying figure). Actually, in this case, the variation of emitter-base resistance with temperature is such a small portion of the over-all emitter series resistance that it exerts little effect on the over-all operation of the circuit.



**Emitter Swamping Circuit** 

in the following figure, resistors  $R_1$  and  $R_8$  operate as a voltage divider across the collector voltage supply source to supply negative (forward) bias to the base-emitter circuit. This arrangement allows a single voltage supply to be used for both and collector voltages. When the value of  $R_1$  together with  $R_8$  in parallel is less than  $R_8$ , the effects of voltagedivider voltage stabilization and the thermal compensation provided by the swamping effect of  $R_8$  combine to offer a more stable bias circuit. Unless the proper ratio is maintained, no compensation is schieved. The stabilization is improved as the following quantity approaches zero:

$$\frac{\mathbf{R}_{\mathrm{B}} \cdot \mathbf{R}_{1}}{\mathbf{B} + \mathbf{R}_{\mathrm{I}}} / \mathbf{R}_{\mathrm{E}}$$

Capacitor Cl bypasses  $R_E$  for signal variations; otherwise, degeneration would be produced by the swamping resistor. The capacitor is chosen to have a reactance about one-tenth that of the swamping resistor at the lowest frequency to be passed.



Voltage-Divider Bias and Emitter Swamping Stabilization

The following illustration is a variation of the previous circuit; it uses only voltage-divider stabilization, the emitter swamping resistor being omitted. In this circuit, R1 and R2 from a voltage divider across the collector supply, and the effective bias is essentially the voltage existing at the junction of R1 and R2. A large resistor,  $R_{\rm B}$ , is connected from the divider **junc**tion point to the base to provide a higher input resistance and avoid the shunting effect of R2 (R2 is small in value because the base-to-emitter bias is only a fraction of a volt). The stabilizing action in this circuit is provided by the voltage divider alone, since the divider is less affected by variations in element currents or voltages than are self-bias arrangements. The disad-



**Voltage-Divider Bias** 

vantage of this circuit is that it consumes more dc power because of the voltage divider; the previously discussed circuit with both voltage divider bias and emitter swamping stabilization is preferable because of its increased stability.

Another method of compensating for emitter-base resistance change with temperature is to feed back an opposing voltage which is proportional to the temperature change per degree. An equivalent method is to correspondingly reduced the forward bias applied the circuit.

In the following figure, the circuit of part A **repre**-sents both ac and dc feedback. When resistor  $R_F$  is divided into two parts and bypassed by capacitor C as shown in part B, the feedback loop is shunted, and only dc bias variations affect operation.



## Negative Feedback Bias Circuit

Compensation is achieved as follows: When the **collector** current (I<sub>o</sub>) increases because of a temperature increase, the collector becomes less negative because of the larger positive voltage drop in resistor  $\mathbf{R}_{\mathbf{C}}$ . Since the drop across  $\mathbf{R}_{\mathbf{C}}$  opposes the initial bias, ' less forward bias is applied to the base through feedback resistor  $\mathbf{R}_{\rm F}$ , and the collector current automatically decreases to the original value (provided that the proper feedback ratio is maintained). There are two other types of compensation for the circuit in part A of the figure; voltage-divider stabilization through  $\mathbf{R}_{\mathbf{R}}$  and emitter current feedback through  $\mathbf{R}_{\mathbf{F}}$ .

Three variations of the voltage feedback circuit are shown in the accompanying illustrations. The circuit of part A represents voltage feedback alone. Actually for dc biasing conditions,  $\mathbf{R}_{\mathbf{F}}$  and  $\mathbf{R}_{\mathbf{C}}$  can be considered as one resistor having a value equal to that of

the external self-bias resistor,  $\mathbf{R}_{\mathbf{B}}$  (see previously discussed figures showing PNP External Self-Bias CE Circuit). It is seen that any change of current through  $\mathbf{R}_{\mathbf{C}}$ , therefore, will either increase or decrease the bias applied through  $\mathbf{R}_{\mathbf{F}}$ .



**Voltege Feedbeck Circuits** 

In part B of the figure, the addition of resistor  $R_{\text{B}}$  produces a voltage divider across the bias supply so that in addition to voltage feedback, the effect of voltage-divider stability is offered. In part C, current feedback through emitter resistor  $R_E$  is added, and when the resistor  $R_{\text{B}}$  shown in dotted is also added, a combination of voltage and current feedback together with voltage-divider stabilization is obtained, and the circuit is identical to the previously discussed *Nega*-tive *Feedback Bias Circuit*.

In the above discussion of stabilization, it has been assumed that only the dc, no-signal operation is of interest, as all circuits are considered to be properly bypassed so that signal operation does not materially affect the bias.

A voltagedivider base-bias arrangement using a thermistor to compensate for emitter current changes with temperature, is shown in the following illustration. When the emitter current tends to rise with temperature, the thermistor, having a negative temperature coefficient of resistance, reduces in value as the temperature increases. This reduction in resistance increases the current **flow** from the **V**<sub>cc</sub> supply and causes an increased voltage drop across R1. The base bias is reduced correspondingly, lowering the emitter current and compensating for the temperature change. Since the thermistor is constructed of a material different from that of the transistor, it does not

change resistance in exact proportion to the emitter current change; therefore, "tracking" is not very good and true compensating occurs at only a few points over the operable range. In this respect, semiconductor diodes provide much more ideal compensation. This method of stabilization is identical in concept to that described in the paragraph covering Forward-Biased Diode Stabilization, later in this section of the handbook.



**Thermistor Base-Bias Compensating Circuit** 

A number of thermistor compensation circuits have been developed, but they all use the same principle of changing bias inversely with temperature to compensate for the change. The accompanying illustration is an emitter bias compensator, in which the base bias is provided by a voltage divider consisting of RI and R2, and compensating emitter bias is provided by R3 and the thermistor. The drop across R3 applies a reverse bias to the emitter as the temperature increases, reducing the emitter current correspondingly.



Thermistor Emitter-Bias Compensating Circuit

Normally ideal thermal compensation, as well as a reduction of the number of parts required, can be achieved by the use of crossconnected transistors arranged so that the element voltages or currents of one transistor compensate for thermal variations by producing correction voltage or currents in the other, while both transistors operate as amplifiers. For example, it is possible to use the variations of the emitter-base junction resistance with temperature of one transistor to control the emitter-base bias of a second transistor, or to stabilize the emitter-collector current of one transistor with the stabilized emittercollector current of another transistor. Since these circuit arrangements become rather involved, they will be discussed as special circuits at appropriate points in other sections of this handbook. However, since thermal compensation is an important part of the dc amplifier, its use in a two-stage stabilized unit is discussed below.

In the following circuit, an increase in collector current produced by a temperature rise in transistor O1 reduces the forward bias of transistor O2. Transistor Q1 is connected as a CB amplifier, which basically has an ideal stability factor. Nevertheless, a very slight variation of collector current will occur with temperature variation. This slight temperature variation is the result of reverse leakage current (ICBO) caused by the internal flow of minority carriers (electrons from collector to base. The reverse leakage current is substantially independent of collector voltage and mainly dependent upon temperature, being constant for a specific temperature, and increasing with temperature. The effects of temperature-caused variations of the base-emitter resistance of Q1 are minimized by the relatively large swamping resistance offered by R<sub>E</sub>, and will not have any appreciable effect on the collector current, I. Thus, while the emitter junction is essentially stabilized, the collector junction is not. Although the collector junction is reverse-biased for normal forward current, this bias is actually a forward bias for reverse current. Therefore, the reverse current flow can reach values as high as 5 milliamperes. Although this high reverse current does not lead to thermal runaway, it does change the parameters, causing a change in the operating poir.t and resulting in improper circuit operation. In addition, since the two transistors are direct-coupled, current changes in Q1 will be amplified by Q2, causing a much greater shift. While the total base current, <sup>1</sup>B, is the net result of I CBO plus the base-emitter current,

the current of interest is the very small (incremental) changes of reverse leakage current,  $AI_{CBO}$ , with temperature; for this explanation then, the absolute values of base current may be disregarded.



**Tempemture-Stabilized O-C Amptifier** 

Referring again to the previous figure, the main current path for  $I_{CRO}$  is through  $R_{C1}$ , the collector-base junction of Ql, and V<sub>cc</sub>. An additional current path which is also the path of  $I_{\rm {\tiny CB02}}$ , is provided through  $R_{C2}$ , the collector-base junction of Q2,  $R_{\rm B}$ , the collector base junction of QI, and  $V_{cc}$ . Any Incremental change of I<sub>CB01</sub> and of ICB02+ ICB01 will produce an incremental change in the voltage drops across  $R_{C1}$  and  $R_{B}$ , respectively. The change in voltage across Rc1 will be in a direction to decrease the forward bias of Q2 (see polarity indicated in figure), while the change in voltage **across**  $R_{\mu}$  will be in a direction which increases the forward bias of Q2. If the values of  $\mathbf{R}_{C1}$  and  $\mathbf{R}_{B}$  are chosen so that the incremental change of voltage across R<sub>c1</sub> is slightly greater than the incremental change across  $R_{B}$ , then a thermally caused increase of collector current will be compensated for by a reduction of the forward bias of transistor O2.

The previous discussion considers only the very small changes in current produced by temperature variation in the collector junction of Q1; it does not consider the static operating conditions nor signal variations. Normally, Q1 operates as a conventional CB amplifier thermally stabilized by series emitter swamping resistor  $R_{e}$ , and biased by **supply**  $V_{ee}$ . The input signal is applied across  $R_{e}$  and **amplified** by Q1, appearing across  $R_{C1}$  as a direct-coupled input to the base of Q2, a conventional CE amplifier.

The output of the two stages is developed across collector load resistor  $\mathbf{R}_{C2}$ . The collector supply for both stages is taken from the single  $V_{cc}$  source. For a complete discussion of dc amplifiers, see DC Amplifier Circuits, in another part of this section of the handbook.

# TRIODE COMMON-COLLECTOR CIRCUITS

In the common-collector circuit, the input signal is injected into the base, and the output signal is taken from the emitter, with the collector being common to both circuits. The common-collector circuit is equivalent to the electron tube cathode-follower circuit. It has a high input resistance (2K to 500K) and a low output resistance (50 to 1500 ohms). It has a current gain similar to that of the common-emitter circuit, but a lower power gain than either the CB or CE circuits (10 to20dB). The output signal is in phase and of the same polarity as the input signal, and the voltage gain is always less than unity. This circuit is used mostly for impedance-matching and isolation of output stages; thus its function is similar to that of the electron tube cathode follower. It has the ability to pass signals in either direction (bilateral operation), a feature which is particularly useful in switching circuitry.

The PNP and NPN common-collector connections are shown in the following figures, together with polarities and external current paths. Base-emitter bias and collector-base junction voltages are obtained from separate supplies and thus two voltage sources are required. Single voltage supply circuits are discussed later, under the paragraph titled **Bias** (Common-Collector).



**PNP Common-Collector Circuit** 

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**NPN Common-Collector Circuit** 

As in the CE and CB discussions, the PNP and NPN circuits are shown together for ease of comparison of operation. Both circuits are forward-biased from emitter to base and reverse-biased from collector to emitter. The currents and polarities in both circuits are opposite because of the different types of germanium used.

The current flow and transistor action of the CC circuit are as explained for the common-base connection, but the current gain is not based on the emitter-to-collector current ratio, alpha (a) Instead, it is based on the emitter-to-base current ratio, gamma (T), because the output is taken from the emitter circuit. Since a small change in base current controls a large change in emitter (and collector) current, it is still possible to obtain considerable current gain. However, since the emitter current gain is offset by the low output resistance, the voltage gain is always less than unity, exactly as in the electron tube cathodefollower circuit.

Common-collector current gain, gamma (7), is defined as

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

with collector voltage constant, and is related to collector-to-emitter current gain, alpha (*a*), of the CB circuit by the formula:

$$\gamma = \frac{1}{1-a}$$

In the PNP circuit, a small input signal (v bc) is shown applied between base and collector of the transistor. The circuit is biased to operate over the linear

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portion of its dynamic transfer characteristic, and rests in a quiescent state determined by the static dc potentials applied (similar to electron tube class A operation). Assuming a sine-wave input, it is apparent that as  $v_{bc}$  increases to its maximum positive value the forward bias is reduced. Thus, the emitter and collector currents are reduced, producing a decreased voltage drop across the emitter output resistor, R<sub>E</sub>, and producing a positive-going output voltage. Conversely, as the input signal swings negative the forward bias is increased and more emitter-collector current flows. The increased voltage drop across R<sub>E</sub> is in the negative-going direction, and the output signal reaches a negative maximum. Since the output signal varies in the same direction as the input voltage, both reaching their positive and negative maximums simultaneously, it is evident that these signals are in phase. Therefore, the output of the common< oliector circuit is of the same phase and polarity as the input signal and no phase reversal is produced, just as in common-base operation.

The functioning of the NPN circuit previously shown is similar to, but the inverse of, the functioning of the PNP circuit. When the input signal is positive, the forward bias is increased (its polarity is opposite to that of the PNP circuit bias), and the emitter current increases and produces a positive-going output across  $\mathbf{R}_{\mathbf{E}}$ . On the negative input cycle, the emitter output across  $\mathbf{R}_{\mathbf{E}}$ . On the negative input cycle, the emitter output is negative; therefore, the output of this circuit is also of the same phase and polarity as the input signal. Thus, *the common-collector circuit always produces an in-phase output signal, 'regardless of the type of transistor used.* 

### Bias (Common-Collactor).

Common-collector biasing schemes are similar to those of the CB and CE configurations, and the basic principles are the same. That is, the base-emitter junction is forward-biased, the base-collector junction is reverse-biased, and the dc, no signal **values** of base current and collector voltage **specify** the operating point.

The accompanying figure shows a series-sidingbias arrangement in which two voltage supplies are used. This arrangement is similar to that for the Series-Aiding Bias Circuit, PNP, previously discussed under the heading *Bias Circuits (Common-Emitter)*, and the operation is also similar.



Series-Aiding Bias Circuit

In the following figure, a single voltage source bias arrangement is shown. Note that the flow of current through  $R_{\rm E}$  is in a direction which produces a voltage drop that opposes the applied bias and collector voltage. The actual bias is the algebraic sum of the two voltages. Polarities and current flow are opposite for NPN circuits.



Self-Bias Circuit

### Hybrid Parameters.

**The** hybrid parameters, or h-parameters, of the transistor are mostly of use to the circuit designer. However, manufacturers have found them convenient for use in defining the performance of their products. Therefore, a working knowledge of the use and meaning of h-parameters is essential to the technician.

The h-parameters appear in two forms which are interchangeable; one form employs letter subscripts, and the other numerical subscripts. At present, the numerical subscripts are commonly used for general circuit analysis, and the letter subscripts are used for specifying characteristics of transistors. Industry standardization accepts both forms, but the present

#### **ELECTRONIC CIRCUITS**

trend in usage indicates that the numerical subscripts may be preferred. In addition, there are other systems of parameters, such as "a", "b", "y", "g", "r", and "z" parameters, which have somewhat more specialized uses. All of these systems, which may seem confusing to anyone other than a trained engineer, represent different methods of mathematically defining transistor action, as well as the parameters limiting that action, for design purposes. Although the triode transistor is a 3-terminal device, it may be treated as a "black box" with two input and two output connections (a basic 4-terminal network). By utilizing the electrical characteristics (h-parameters) of this black box, it is possible to calculate performance of various circuits when various input signals are applied and various loads are connected. Basically, these h-parameters are limited to frequencies sufficiently low (270-100 Hz) that the capacitive and inductive effects of the transistor can be neglected. The h-parameters for common-base connection are usually shown in specification sheets because the emitter current and collector voltage can be maintained more precisely than for other configurations. Because of the trend toward the use of common-emitter circuits and the relative ease of measurement, some CE h-parameters will also be observed. In any event, formulas are available for conversion from one configuration to the other in most text books (and transistor manuals), so only the common-base connection will be discussed in here.

The simple common-base configuration shown in part A of the accompanying figure can be represented by the four-terminal h-parameter equivalent circuit shown in part **B**. In using the h-parameters, it is customary to ignore the bias and consider only the instantaneous ac values involved. Thus, the h-parameters represent operating conditions for a small signal close to the operating point. Therefore, the equivalent circuits do not show bias supplies and polarities. Conventional currents (not electron flow) and voltage polarities are assumed, and if erroneously assigned, will result in a negative answer when the problem is solved. Since the circuit is essentially a four-terminal network (two input and two output terminals), it can be described by two simultaneous equations in which the h-parameters are the coefficients, namely:

$$\mathbf{E_1} = \mathbf{h_{11}} \mathbf{i_1} + \mathbf{h_{12}} \mathbf{E_2}$$
  
1. =  $\mathbf{h_{21}} \mathbf{i_1} + \mathbf{h_{22}} \mathbf{E_2}$ 

To conform with Kirchhoff's law,  $h_{11}$  in part B of the figure must be an impedance and  $h_{22}$  an admittance, while  $h_{12}$  and  $h_{21}$  are essentially dimensionless ratios. For low frequencies  $h_{11}$  and  $h_{22}$  are resistive. Since these parameters involve two oppositesimpedance and admittance-the term *hybrid* is used to describe them.



## Transistor and Four-Terminal Network **Equivalent** Circuits

If the output terminals are short-circuited for ac **(by** a large capacitor), the output voltage **(E<sub>2</sub>)** is zero, and the following simple formulas (like Ohm's law) show the relationships between input voltage and current and between input current and output current.

$$h_{11} = \frac{E_1}{I_1}$$
$$h_{21} = \frac{i_2}{i_1}$$

If the ac input circuit is opened by the insertion of a large inductance in series with the bias, thereby reducing  $i_i$  to zero, the following additional formulas will be obtained:

$$h_{12} = \frac{E_1}{E_2}$$
 and  $h_{22} = \frac{i_2}{E_2}$ 

ORIGINAL 491-044 0- 73 -19 Thus,  $h_{11}$  is effectively the transistor input impedance (with the output short-circuited), and  $h_{22}$  is the output admittance (with the input open-circuited). Similarly,  $h_{12}$  is the voltage feedback ratio **with** the input open-circuited (this represents the internal feedback due to reverse-current effects and common impedance coupling within the transistor). Parameter  $h_{21}$  is the forward current amplification ratio with the output short-circuited.

The functioning of the equivalent circuit and the meaning of the h-parameters can perhaps be more clearly understood by considering the following intuitive reasoning. Consider part B of the figure, and for the moment neglect the voltage produced by the voltage generator  $(V_{GEN})$  in the input circuit. When the input signal voltage (El) is applied to the input terminais, current i flows through resistor  $h_1$  1 and causes Current  $h_{21}$  i<sub>1</sub> to flow in the output current source (current generator  $I_{GEN}$  in the figure). Thus,  $h_{21}$  is the current gain of the equivalent circuit. Current  $h_{2}$ **i**<sub>1</sub> divides between the output resistor, which is equal to  $1/h_{22}$  (h<sub>22</sub> is an admittance), and the external circuitry comected across the transistor output terminals. The voltage developed across the output as a result of this current is the output voltage  $(E_2)$ . When voltage E, appears across the output it causes an internal feedback voltage to be fed back to the input; this voltage is h<sub>12</sub>, E<sub>2</sub>, represented by voltage generator  $V_{GEN}$  at the source. This feedback voltage opposes the initial signal input (El) and effectively subtracts from it.

The following figure shows the hybrid equivalent circuits for the three basic transistor configurations. Note that the circuits are all the same because the defining equations must be satisfied. The parameter notation, however, is different for each configuration; it consists of the general parameter designations  $h_i$ ,  $h_r$ ,  $h_f$ , and h. with the additional subscript b, e, or c added to represent the common base, emitter, or collector configuration, respectively. The letter and numerical forms of the parameters are related as fol-10ws:  $h_1$  is  $h_{1,1}$ ,  $h_r$  is  $h_{1,2}$ ,  $h_r$  is  $h_{2,1}$ , and  $h_o$  is  $h_{22}$ .



**Basic-Hybrid Parameter Equivalent Circuits** 

From the preceding discussion, it is obvious that with a few external measurements the h-parameters of the typical "black box" can be determined, and that substitution of these values in the proper formulas will allow circuit performance to be approximated so that the proper matching values of external circuitry can be chosen by the designer.

# DIODE STABILIZATION CIRCUITS

#### Forward-Biased Diode Stabilization.

The accompanying circuit employs junction diode CR1 as a forward-biased diode to compensate for
transistor emitter-base resistance variations with temperature. This type of circuit compensation is effective over a range of from IO to 50 degrees Centigrade (usually no compensation is needed below 10 degrees). Higher temperature ranges require additional compensation (see discussions on Reverse-Biased Stabilization and Double-Diode Stabilization, later in this section).



Forward-Biased Diode Stabilization, CE Circuit

Under static conditions, the emitter of transistor Q1 is biased positive with respect to the base (forward biased), and current flows through RI and external diode CR1 connected across the cource voltage, V<sub>CC</sub>. In this condition, CR1 is forward-biased also, and the polarities around the circuit are as shown in the figure. Current flow is light (on the order of 100µa or less), and junction diode CR1 can be considered as a resistor (r about 25000 ohms). Thus the transistor emitter-base junction bias consists of the voltage drop across diode CR1. Since every junction diode has a negative temperature coefficient of resistance, an increase in temperature causes the transistor emitter-base junction resistance to decrease, and would normally produce an increased collector current in the transistor. However, the resistivity of junction diode CR1 also decreases with an increase of temperature, the diode voltage drop is lower, and increased diode current flow causes a larger voltage drop across R1 (which opposes the diode-developed bias); therefore, less actual bias is developed. The net effect is to reduce the total forward bias on the transistor and thus lower the coUector current sufficiently

to compensate for the increase of collector current with temperature.

The dc secondary resistance of T1 does not offset the operation since the transistor base current flow is negligible. However, considering the collector-to-base reverse-bias (saturation) current,  $I_{CBO}$ , which flows from the base through T1, CR1,  $V_{ee}$ , and  $R_e$  to the collector, we find no compensation is provided by this circuit. The normal current through forwardbiased diode CR1 is so heavy that it effectively swamps the small  $I_{CBO}$  current (on the order of 2 or  $3\mu a$  as compared to 75–200  $\mu a$  for the normal current). As far as signal variations are concerned, capacitor Cl effectively bypasses diode CR1 and the output voltage developed across  $R_e$  is applied to the next stage, through coupling capacitor CCC, in the conventional manner.

**Reverse-Biased Diode Stabilization.** The circuit shown in the following figure employs external junction diode CR1 as a reverse-biased diode to compensate for transistor collector-base saturation current variations with temperature. This type of circuit is effective over a wide range of temperatures when the diode is selected to have the same reverse-bias (saturation) current as the transistor. The reverse-bias diode provides a high input resistance, which is particularly advantageous when the preceding stage is resistancecapacitance coupled.



Reverse-Biased Diode Stabilization, CE Circuit

Two current paths are provided in the circuit shown. The base-emitter current  $(I_{BE})$  flows internally from the base to the emitter, then externally through  $R_E$  and  $V_{ee}$ , and through resistor RI back to the base, and is not materially affected by diode

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CR1 because of its large resistance in the reverse direction. The other path provides for the saturation current from collector to base, through CR1, V<sub>BB</sub>, and V<sub>ee</sub>, and through collector load resistor Rc to the collector. Temperature variations in the emitterbase junction resistance are compensated for in the first path by swamping resistor R<sub>n</sub>. Refer to the previo us discussions in this section of Transistor Common-Base and Common-Emitter circuits. Variations of saturation current with temperature are compensated for by the second path, using diode CR]. When a temperature increase causes the transistor junction saturation current to rise, the diode saturation current also increases, so that there is no chance for the I<sub>CBO</sub> current carriers in the junction to pile up, increase the transistor forward bias, and cause a consequent rise in emitter current. As a result, although the saturation current may increase, the emitter current does not, and there is only a negligible change in the total collector current. In effect, diode CR1 operates similarly to a variable grid-leak in an electron tube circuit. The reverse bias permits only a few microampere of current to flow in the base-toemitter circuit, and maintains a high input resistance, while simultaneously compensating for changes in I<sub>CBO</sub> with temperature.

#### Double-Diode Stabilization.

The following circuit utilizes two junction diodes in a back-to-back arrangement. Junction diode CR1 is forward-biased and compensates for emitter-base junction resistance changes with temperature below



Double-Died@ Stabilization, CE Circuit

50 degrees Centigrade, as described in the previous paragraph. Diode CR2 is reverse-biased and compensated for higher temperatures as discussed below.

Forward-biased ciode CR1 operates in the same manner as in the previous discussion on Forward-Biased Diode Stabilization, and all comparable parts are labelled exactly as in the previous discussion.

Reversed-biased diode CR2 can be considered inoperative at room temperatures and below. When the junction temperature reaches the point where saturation current flows, CR2 conducts and current  $(I_1)$ . flows through R2, producing a voltage drop with the polarity as shown. This voltage drop is in the proper direction to reduce the forward bias set up by diode CR1 and RI; its net effect is to reduce the total \_ collector current, to compensate for the increase in transistor  $I_{CBO}$  due to temperature increase.

The reverse-biased diode is selected to have a larger saturation current (1,.) than the transistor it stabilizes, since  $l_s$  consists of the transistor Saturation current plus the current through R2 0,  $= l_{CBO} + l_{I}$ ). Thus the diode saturation current controls the transistor at all times, effectively reducing the forward bias as the temperature increases and stabilizing the collector current. Capacitor C 1 bypasses both diodes for ac so the bias circuit is not affected by signal variations. **Diode Voltage Stabilization**.

If a junction diode is reverse-biased, current flow does not entirely cease, but continues at a low rate (a few microarnperes), until the bias is increased to the point where it reaches the breakdown voltage. If the reverse-bias is increased beyond the breakdown point, the diode reverse-saturation current suddenly increases, because of the avalanche effect, and the applied voltage remains practically constant. In most cases this will destroy the diode because of overheating (except in the special case of the Zener diode). Reduction of the bias below the breakdown voltage level returns the junction to its normal operation again (provided that no damage has occurred). Application of the avalanche phenomenon has resulted in the development of a voltage-stabilizing diode known as the "breakdown diode, often called a Zener diode.

The breakdown, or Zener, diode is a PN junction . modified in the manufacturing process to produce a breakdown voltage level which is closely controlled over a range of from 2.5 to 200 volts or more. Each Zener diode has a specific breakdown voltage (and operates over a small voltage range), depending upon

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## **ELECTRONIC CIRCUITS**

#### NAVSHIPS 0967-0000120

its design characteristics, and must be selected for the desired operating voltage.

Because of its unique properties, this diode has many uses other than the basic voltage-regulating application. For example, it may be used for surge protection, as an arc reducer (across contact points), as a dc coupler in an amplifier, as a reverse polarity gate, or as a biasing element. Its basic properties will be discussed in the following paragraphs for proper understanding, and special applications will be treated as the need arises in other part of this handbook.

A typical dc voltage-regulating circuit of the most elementary type is shown in the accompanying illustration. Resistor R1 is selected to produce the proper breakdown voltage to maintain diode CR1 at the correct operating point. When the input voltage rises, current through the diode increases, and the drop across R1 becomes greater so that the output voltage remains the same. Conversely, when the input voltage decreases, current through the diode decreases. and the drop across RI becomes less so that the output voltage again remains the same. Should the load resistance decrease, and more current be required, the current is divided between the load and the diode to ground path, so that no more current is drawn through R1 and the voltage across CRI remains the same. When the load resistance increases so that less current is required, the additional current is absorbed in the diode current flow to ground, again dividing so that no additional or reduced current passes through Rl, and the voltage across the diode remains the same. Thus through the avalanche effect, the breakdown diode operates similarly to the electron tube type of glow discharge voltage regulator.



Breakdown Diode Voltage Regulator

#### Temperature Compensation.

Forward'biased junction diodes have a negative temperature coefficient of resistance, and so do

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reverse-biased junctions until the breakdown voltage is reached. Once the diode is operating in the avalanche-effect region, the temperature coefficient becomes positive and of a larger value. An uncompensated diode can vary as much as 5 percent (of the maximum rated voltage); with temperature compensation, however, it is possible to reduce this figure to .0005 percent (a few millivolts) or better.

Because a forward-biased junction diode changes resistance with temperature in exactly the opposite direction from the breakdown diode, it is possible to use one or more forward-biased diodes for temperature compensation. Following is a basic compensation circuit, in which CR1 is a forward-biased diode and CR2 is the breakdown diode.



Breekdown Diode Temperature Compansation

The CRI diode is selected to have a temperature characteristic which is the exact inverse of the breakdown diode's temperature characteristic (if necessary more than one diode is used in series, but usually not more than three). Thus the combined resistance of both diodes (CR1 and CR2) in series remains constant over a wide range of temperatures and voltages to produce the desired compensation. The compensating diode must be able to pass the current taken by the breakdown diode, and should not introduce any appreciable voltage drop in circuit (across the diode itself). Fortunately, the use of forward bias produces only a very small voltage drop, depending on the material forming the junction (about 0.6 to 1.5 volts for silicon, and units with adequate current ratings are available

to produce the desired regulation. A particular advantage "of the breakdown diode over the electron tube tupe of voltage regulator is that breakdown voltages are easily manufacturable over a wide range of approximately 2.5 to 200 volts, whereas the lowest tube voltage available is about 70 volts. Adequate voltage stabilization for quite a wide range of circuit operations and temperatures is therefore available. Unique applications of the preceding principles will be discussed in comection with applicable circuits in other sections of this handbook.

#### Shunt-Limiting Diode.

The following circuit utilizes a junction diode connected in shunt between the base and emitter of the transistor as a protective peak limiter for transient voltages.



**Basic Shunt-Limiting Diode Circuit** 

Under normal circuit conditions diode CR1 is inoperative, being reverse-biased by the potential across resistors RI and R2, and the transistor is forwardbiaaed by the drip across R1. When an oppositely polarized input signal (or noise transient) exceeds the bias voltage across R1, diode CR1 becomes forwardbiased and conducts, effectively shunting the transistor base and emitter terminals. Thus the baseemitter junction of the transistor is prevented from becoming reverse-biased by excessive signal swing.

This peak limiting action is particularly applicable to transformer-coupled transistor stages because they develop transient voltages when the collector current is suddenly cut off by bias reversal. The resulting high collectorenitter voltage with **base-emitter** circuit reversed-biased can then produce stron internal oscillations and cause excessive power dissipation, which could destroy the transistor. In this circuit Cl is a low-resistance bypass capacitor to shunt Rl; it is not used to resonate with the secondary of T1.

# CLASSES OF AMPLIFIER OPERATION (ELECTRON **TUBE**)

Amplifier operation is divided into three general classes: Class A, Class B, and Class C. The classes are determined by the operating bias applied, the amplitude of the input signal, and the amount of time during the operating cycle that plate current is allowed to flow.

These general classes of operation cover a large range of operation; since it is possible to operate an amplifier partially within one class and partially within another, additional designations are added to indicate whether or not grid current flows. When gn"d current does not jlow at all during the entire cycle of opemtion, the suffix (or subscript) 1 is added to the class letter; when grid current flows, for even a portion of the cycle, the number 2 is added Thus Class AB1 operation indicates that the circuit is biased to operate somewhere between the limits of Class A and Class B operation and that no grid current flows during the operating cycle. Similarly, Class AB2 operation indicates that the circuit is biased to operate somewhere between the limits of Class A and Class B operation, and that the input signal exceeds the bias sufficiently to produce grid current flow over a portion of the cycle.

Class A operation produces the lowest power conversion efficiency and the least amount of distortion, while Class C produces the greatest possible power efficiency with the most distortion, with Class **B being** intermediate between the two values. When no grid — current is drawn during the operating cycle, there is no power loss in the grid circuit, and a minimum of driving power is required. When grid current is drawn, a power loss occurs in the grid circuit, and the driver stage must be able to supply power at the required maximum drive voltage.

## Class A Operation.

In normal Class A operation, the electron tube is operated on the linear portion of the grid-plate transfer characteristic curve, and plate current flows continuously over the entire input cycie. Because operation is on the linear portion of the curve, distortion is low (on the order of 2 to 3 percent maximum) and voltage gain is high. Because of plate current flow over the entire cycle, plate efficiency is extremely low (on the order of 20 to 30 percent) and power output is low.

Class A operation is usually employed where voltage amplification rather than power output is desired, or where low power output is desired with a minimum of distortion. Thus it is used in the r-f and i-f stages of receivers, in low-power test equipment, in the oscillator and driver stages of low-power **trans**mitters, in video amplifiers, and in audio-amplifier applacations where voltage gain with good fidelity is desired.



#### **Class** A Oparation

Normally, no grid current flows during any part of the cycle and pure Class A operation is defined as  $A_1$ . However, in common usage the symbol stands alone, the subscript is dropped, and it is understood that unless otherwise indicated no grid current flows. When the input signal amplitude exceeds the bias voltage and grid current does flow over a portion of the cycle, the subscript 2 is used, e.g.,  $A_2$ . When grid current flows, a larger input signal is required to drive the tube to the same output, and distortion increases; but at the same time, plate current flow reduces during the **grid-current** portion of the cycle and **the** overall plate efficiency is increased



Class A<sub>2</sub>Operation

## **Class B Operation.**

Biasing of Class B amplifiers is such that, with no grid input signal, the plate current is biased to cutoff; consequently, no plate current flows for approximately half the operating cycle (1800), and grid drive is sufficient to cause grid current flow. Since plate current flows for only half the cycle, it is necessary to use two tubes in a push-pull arrangement to reproduce the full positive and negative input swings, and to **minimize** distortion. An exception to this rule is in an r-f amplifier where the missing half of the signal is supplied by the tank circuit, and the distortion can be tolerated.

Class B operation is normally characterized by moderate efficiency (40 to 60%) in the plate region, with low driving power, and somewhat greater output distortion (4 to 6%). Typical Class B operation for a single tube is illustrated in the following figure.



**Class B Oparstion** 

Class B amplifiers are used extensively for audio output stages where high-power outputs are required; they are also used as the driver and power amplifier stages of transmitters and as audio modulators.

Special tubes have been developed, particularly for Class B operation, which normally rest at plate current cutoff without bias applied. These tubes, together with improved transformer design, make it possible at the present state of the art to design Class B stages which compare favorably in performance with Class A stages, and yet provide the increased power output and efficiency of Class B operation.

### Class AB Operation.

In this type of operation, the bias is set between Class A and Class B so that the amplifier operates Class A for small input signals and Class B (really Class  $AB_1$ ) for large input signals. Plate current flows for more than half the operating cycle, but not for the entire cycle. In addition, the input signal, although just about equal to the bias, is not great enough to produce grid current flow.

This type of operation is used where good fidelity and increased efficiency are desired but without sufficient drive to produce **full** Class B operation or excessive distortion.

As can be seen from the following illustration, the bias for Class AB operation is about halfway between the values for Class A and cutoff. The power output and efficiency are higher than with Class A operation, but at the expense of more distortion. To reduce the effective distortion, Class AB audio amplifiers are operated push-pull, in which case the efficiency is much greater than that of Class A operation with about equal distortion.



#### **Class AB Oparation**

Class  $AB_2$  amplifiers require low-impedance grid drive sources because' of grid-current flow and, therefore, are often transformer-coupled to power drivers. This class of operation provides power output and efficiency ratings more nearly equal to those of Class B operation.

## **Class C** Operation.

In Class C operation, the bias is adjusted to twice the cutoff value or more (usually does not exceed four times cutoff value). Plate current flows only on the peaks of the driving signal, the grid is always driven positive, and extremely high efficiency isproduced, -(70 to 85%). Because of the high distortion produced, Class C has not been found useful for audio-frequency amplifier operation. But it has proven excellent for use in r-f amplifiers, where tank circuits provide the missing portion of the signal, and extremely high powers can be conveniently and efficiently handled. The fly-wheel effect of the tuned tank circuit serves to smooth the intermittent pulses of plate current into sine-wave oscillations in the tank circuit.

Since grid current always flows, this type of operation should be designated as Class  $C_2$  but, being generally understood, this notation is usually never used. The following figure **illustrates** Class C operation.





**Class C Oparation** 

# CLASSES OF AMPLIFIER OPERATION (SEMICONDUCTOR)

Since transistors are analogous to vacuum tubes, the same general classes of amplification, input and output parameters, distortion, and efficiency are applicable. Thus the transistor can be operated as a Class A, Class B, Class AB, or Class C amplifier. Operating conditions and results for the iderd case are used in the following discussion to define the differences and relationships between the classes of operation.

## Class A.

The Class A amplifier is biased so that it operates on the linear portion of the collector characteristic, providing for equal swings above and below the bias point. Collector current flows continuously (with or without signal) for 360 degrees of the operating cycle, and the transistor is operated so that the maximum collector dissipation is never exceeded (other classes momentarily exceed this rating).

The Class A amplifier is basically a small-signal amplifier, although it can be used as a large-signal amplifier provided that the quiescent current does not exceed the maximum transistor ratings. Usurdly, large-signal amplifiers of the power type are operated as Class B amplifiers. Class A amplifiers may be operated in push-pull or as single-ended stages.

While the efficiency of a vacuum-tube amplifier operated Class A averages around 30 percent, the efficiency of a transistor operated Class A varies considerably, depending upon the circuit configuration and the parameters used. Considering the ideai case, it can be demonstrated mathematically that the directcoupled Class A amplifier produces a theoretical maximum of 25 percent in either the CB or CE circuits. On the other hand, a resistance-coupled circuit will produce a maximum collector efficiency of 17 percent. The highest possible efficiency, 50 percent, is obtained with transformer-coupled configuration (assuming a perfect transformer, with no losses), or by use of a shunt collector feed.

For Class A operation, the transistor must be capable of dissipating more than the desired power output.

Typical Class A operation for CB and CE configurations are shown in the following illustrations. Note that operation does not extend into the saturation region since the knee of the curve makes operation here very nonlinear. Likewise, operation in the cutoff region is not permitted, because current would flow for less than the entire cycle. Comparing the graphs of these two figures it is seen that the CB circuit is inherently more linear since the constant-current curves are more equally spaced than those of the CE circuit. Therefore, the distortion is lower in the CB circuit than in the CE circuit. Other parameters which affect the distortion produced are: the amplitude of the input signal (if too large, it will be clipped), the value and linearity of the input resistance, and appreciable variation of the bias with temperature. To minimize distortion and produce maximum gain, the CB circuit uses an input resistance of about two times the source impedance, while the CE circuit uses an input resistance one to three times the source impedance, to minimize the over-all imput resistance variations. Although the CB circuit produces less distortion and more power output for the same percentage distortion as the CE circuit, the CE circuit is usually preferred for all around use because it is easily cascaded and has a high power gain.



**CB Class A Graphical Oparation** 



CE Class A Graphical Oparation

#### Class B.

Class B amplifier operation is obtained when the collector current flows for one half of the operating cycle, and is entirely cutoff during the other half. The bias is set at the cutoff point (zero bias), and during the positive input signal swing on NPN transistor will amplify in a normal fashion; on the negative swing the transistor is cut off and does not operate. A PNP transistor will conduct during the negative half cycle of the input signal and remain cut off during the positive swing. To produce the full input signal, two

transistors must be employed, operating back-to-back in a push-pull arrangement. On one half of the cycle one unit operates, on the other half cycle the other unit operates, and the halves are combined and added in the load. Thus each transistor operates for only half the operating period.

A graph of Class B operation is shown in the accompanying illustration with the input and output signals projected from the transfer characteristic. Note that while collector cutoff is assumed there is a small flow of reverse leakage current, ICEO, which reduces the total efficiency of the circuit. Ideal efficiency is 78 percent, which is quite an improvement over Class A operation. Distortion components are the same as for Class A plus an additional type, known as crossover distortion. Since two transistors are employed, even though operating only half the time, the distortion is greater than for Class A depending on the circuit design. At the present state of the art, no general figures to indicate the possible range of values of distortion are available, since to obtain the necessary gain or output it may be necessary to accept more distortion with one transistor and design than with another.

Figure A-209



## **Typical Class B Operation**

Because each transistor operates for only half the time and the power conversion efficiency is high, the

Class B operated transistor is required to dissipate only about 35 percent of the total output power desired. Hence, much greater power output is possible with lower rated transistors for the Class B amplifier. Since the ideal case is usually not obtained, the percentage to be dissipated should be calculated in each instance, but the value given above is a rough approximation for comparison purposes.

Class B operation is usually used for audio power amplifier stages, but is seldom employed single-ended. However, single-ended operation is applicable to transmitters using tank circuits to fill in the missing half of the output signal, as in vacuum-tube operation.

Crossover distortion is caused basically by the nonlinearity of the transistor characteristics. At small input voltages the current change is small and varies exponentially, but at higher input voltages the transistor conduction is heavier and heavier. This action produces an inward belly, as shown in the following figure, and increased distortion. Compensation for crossover distortion is usually achieved by placing a slight forward bias on the base of the transistor, to move the bias point to a more linear portion of the transfer characteristic. While feedback can be used or the source resistance can be increased to minimize crossover effects, circuit design complications, together with the loss in the increased source resistance, make these types of compensation gneerally unsatisfactory for general use. Actually, the biasing-off type of compensation places the amplifier in the Class AB range of operation.



#### Crossover Distortion

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Class AB.

Operation in the Class AB region is obtained by biasing to the point where collector current flows for more than a half cycle, but not for the entire cycle as in Class A operation. By arranging the bias properly, efficiencies between 50 and 78 percent are obtainable, with an average of 65 percent representing typical Class AB operation.

A graph of typical Class AB operation is shown in the accompanying illustration. Distortion is less than that of Class B and more than that of Class A. The circuit arrangement is usually **pushpull**. However, for those applications which can tolerate the increased distortion, it is possible to use single-ended operation with an increase of output over Class A operation. For push-pull operation, Class AB represents greater power output and slightly more distortion than Class A, but less power output and slightly less distortion than Class B.



Typical Class AB Push-Pull Operation

class c.

Class C operation is obtained by biasing to the point where collector current flows for less than a half cycle, with the transistor remaining in the cutoff condition and with a slight cutoff (reverse) current flowing during the inoperative portion of the cycle. Class C operation is not used for audio amplification because of the severe distortion it produces. It is used for. tank circuit applications where the distortion is smoothed out and minimized by the flywheel effect, as in vacuum-tube operation; also, it is used in singleended or push-pull configurations. Switching circuits are usually operated as Class C amplifiers.

To achieve Class C operation with a bias "point considerably below cutoff, it is necessary to reversebias the emitter (assuming a common-emitter circuit), as opposed to forward-bias for normal operation in the other classes.

The Class C amplifier can be considered to operate as a pulsed oscillator for r-f energy, where the input pulses cause conduction for a small portion of the operating cycle, and the transistor rests with a small steady current during the remainder of the cycle, in a cutoff condition, with the r-f oscillations being sustained by the parallel resonant tank circuit. Assuming an input sine wave, it is only necessary to supply the losses in the tuned inductor by transistor conduction, and obtain an amplified sine wave output produced by the voltage gain factor. Naturally this type of operation is restricted to essentially sine-wave oscillations produced at the frequency to which the tuned load circuit is resonant. A typical Class C amplifier circuit with input and output waveforms is shown in the foUowing illustration.



**Class C Amplifier, CE Circuit** 

## COUPLING METHODS (ELECTRON TUBE)

Usually more than one amplifier, operated in cascade, is needed to increase the amplitude of the feeble input signal to the required output value. Cascaded amplifier stages are connected (coupled) together by resistance-capacitance networks, impedance-capacitance networks, transformers, or direct coupling as described in the following paragraphs. While all coupling networks are frequencyresponsive, some coupling methods provide better response than others, and their basic principles of operation remain the same, regardless of whether or not they are employed singly as input or output coupling devices, or in cascade. Discussion in this section will be limited to the actual types of coupling and important considerations involved in the various functional classes on a relative or comparative basis. Circuit discussions in other sections will fully cover the limiting parameters for the specific circuit arrangement.

## R-C Coupling.

Although R-C coupling involves the use of two resistors and a capacitor, as shown in the following figure, it is usually referred to as resistance coupling. Because of the rather wide frequency response offered by this form of coupling, plus small size and economy, the resistance coupler finds almost universal use where voltage amplification is required with little or no power output. Basically the resistance coupler is a Pi-type, hi-pass network, with plate resistor  $R_{L}$  and grid resistor  $R_{g}$  forming the legs of the Pi and capacitor C<sub>c</sub> the body. Since the plate and grid resistors are not frequency-responsive, it can be seen that basically over-all frequency response is limited by the capacitive reactance of C<sub>c</sub> between the plate and grid circuits, plus the effect of shunt wiring and electrode-to-ground capacitances across the network. At dc or zero frequency the coupling capacitor separates, or blocks the plate voltage of the driving stage from the grid bias of the driven stage, so that bias and plate or element voltages are not affected between stages.



In the conventional R-C amplifier signal voltage variations on the grid produce plate current variations through plate load resistor  $R_L$ , and the resulting voltage developed across  $R_L$  represents **an** amplified replica of the input signal but 180 degrees out of phase. The amplified signal is coupled through capacitor CC, and applied to the grid of the next stage across grid load resistor  $R_g$ . The same cycle of operation is repeated for each stage of the cascaded amplifier.

Since load resistor  $R_{L}$  is in **parallel** with the internal tube plate resistance,  $r_{p}$ , the load resistor of a triode is never made less than twice  $r_{p}$ . Usually the maximum undistorted output for a triode is obtained with a value of  $R_{L}$  that is 5 to 10 times the plate resistance of the tube. With pentodes the extremely high  $r_{p}$  makes this impractical; best results are **usually** obtained with a load resistor of 1/4 to 1/10 the value of  $r_{p}$ , or with a value that is as high as is practical for the plate voltage and current needed without requiring excessive supply voltage.

At low frequencies (below 100 Hz), the reactance of CC, plus  $\mathbf{R}_{\mathbf{g}}$  in series, parallels the load resistor. But the reactance of C<sub>s</sub> is in series between the plate and grid, and produces a large voltage drop (or loss of gain), while  $\mathbf{R}_{\mathbf{g}}$  shunts the grid and has the least voltage developed across it. Therefore, the interstage grid resistance has less over-all effect on the gain than the reactance of CC, and the distributed circuit and electrode capacitance to ground is not effective and may be neglected. Low-frequency response, therefore, is controlled by the size of the coupling capacitor. Simplified equivalent circuits of R-C coupling (constant current generator form) are shown in the following illustration. Part A is a simplified equivalent lowfrequency circuit. Only those circuit elements which are of significance at low frequencies are shown. When the coupling capacitor is excessively large,

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distortion is caused by excessive phase shift, and motorboating may occur. Motorboating is cuased by regenerative feedback at low frequencies through impedance coupling in multiple cascaded R-C stages with a common power supply.





Over the mid-frequency range (100 to 20,000 Hz), amplification is relatively constant, and the coupling capacitor reactance is much lower than the resistance of grid resistor  $\mathbf{R}_{\mathbf{g}}$ . Therefore, the reactance of coupling capacitor C<sub>c</sub> may be neglected as in the simplified equivalent mid-frequency circuit of part B. To insure that the plate resistor is not shunted excessively by the grid resistance of the following stage and to maintain a high input resistance, 1\$ is made two to four times  $R_{L}$  and never less than  $R_{L}$ . Usually in low-level stages the grid resistor is in the megohm range (from 1 to 5 megohms), with its value for grid leak bias ranging from 5 to 10 megohms; whereas in power amplifier stages the grid resistor is on the order of 0.5 megohm end usually never more than 1 megohm. High values of grid resistance tend to cause adverse effects due to the possibility of grid current flow caused by imperfect evacuation, grid emission, and leakage effects in the electron tube.

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In the high-frequency range (over 20,000 Hz), the coupling capacitor reactance is neglected entirely and shunt capacitive effects become the limiting parameters. The shunt capacitance consists of the plate-to-ground (tube output) capacitance, the grid-to-ground (input) capacitance, plus the distributed wiring and network capacitance to ground. The effects of these individual capacitances are cumulative and may be lumped together, as shown by  $C_d$  in part C. The overall effect of this capacitance is to shunt the signal to ground and reduce the response.

In high-fidelity amplifier circuits, increased lowfrequency response is usually desired and is achieved by bass compensating networks. Likewise, in video amplifiers both low- and high-frequency response must be increased, and is achieved through the use of shunt and series peaking circuits. For a discussion of R-C and R-L compensation considerations, refer to the discussion of time constants later in this section of the handbook.

Because of the low amount of gain available with R-C coupling at radio frequencies, it is seldom used in r-f amplifiers, but it may be encountered in special cases, particularly in test equipment.

## Impedence Coupling.

When an impedance is substituted for the plate load resistor in a resistance-coupled circuit, the impedance coupling circuit results. Actually, an original circuit derivation also involved a substitution of an impedance for the grid resistor. By making the grid inductor series resonant with the coupling capacitor, bass response was improved. However, the grid impedance offered more of a disadvantage because of high-frequency shunt losses, so the LC-R circuit as **shown** in the following figure became the standard impedance coupler. The impedance coupler operates in the same manner as the resistance coupler as far as  $C_{c}$  and  $R_{g}$  are concerned; the basic difference is in effect of the plate impedance. By using an impedance in the plate circuit, less voltage "drop occurs for a given voltage supply. Therefore, a lower supply source will provide the same effective plate voltage, there is less  $1^{2}$ R (power) loss, and a better over-all efficiency results. Low-frequency response is dependent upon obtaining a high inductive reactance in

the plate circuit, and requires a large number of turns for good low-frequency response. The distributed capacitance associated with a winding of many turns produces a large shunting capacitive reactance with a consequent drop in high-frequency response. Since the impedance of plate reactor varies with frequency, the response is not as uniform as that of the resistance coupler.



Impedance Coupling

The impedance coupling circuit is used where a limited response over a relatively narrow band of frequencies is required. As a result, impedance coupling is mostly **emploved** in tuned or untuned amplifier applications such as i-f or r-f stages, and its use in audio applications has generally been discontinued in favor of the R-C or transformer-coupled circuit, except for special designs.

As in the resistance-coupled amplifier, series and shunt peeking compensating networks may also be employed to extend frequency response. Baaa boost circuits in particular can be advantageously used. However, as frequency compensation is increased, the circuitry becomes complex and its use is restricted to a particular application, so that the basic type of coupling circuit is no longer of much significance.

## Transformer Coupling.

When the primary of a transformer is connected as the plate load, and the secondary provides the output signal, either to the next stage or an output device, we have what is known as transformer coupling; see accompanying figure.



Transformer Coupling

With transformer coupling, response gain, and output considerations become more difficult to predict, because they depend primarily on the transformer design. Basically, the use of transformer coupling provides additional gain, achieved through the use of a step-up turns ratio of primary to **secondary**, but this gain usually does not exceed 2 or 3 to 1. Since there is no physical dc connection between stages, plate and bias voltages are kept separate, and the ac signal is coupled from the plate of one stage to the grid of the following stage by the mutual inductive coupling between primary and secondary windings.

Low-frequency-response is primarily dependent on the inductive reactance of the primary, dropping off approximately 3 dB at the frequency where the inductive reactance is equal to the plate resistance plus the primary resistance  $(2\pi fL = R_p + R_{pri})$ .

Gain at the mid frequency is the highest and is essentially equal to the amplification factor of the electron tube multiplied by the transformer turns ratio. Response is considered to be relatively flat over a range of frequencies above and below the mid frequency, but such results are usually achieved only in the ideal case. In practice, the response curve is a continually changing curve, dropping off on either side of the mid frequency, with possible humps produced by circuit and transformer resonances.

Since the secondary contains more turns than the primary, a larger shunt capacitance to ground is produced and, together with the primary and secondary leakage reactance, limits the high-frequency response.

Transformer coupling is generally used for interstate applications with electron tubes having plate resistances of 5 to 10 thousand ohms maximum, since higher plate resistances require excessively large transformer primary inductances. For output stages, lower plate resistances are used, and the transformer is carefully designed to handle larger plate currents. Generally speaking, a lower plate resistance improves bass response, while a higher amplification factor provides greater gain, and lower plate current produces less dc core saturation effects.

Since the impedance transformation in a transformer varies as the square of the turns ratio between primary and secondary, output and input matching is possible and is extensively employed. For interstage applications, matching is not always used, because power output is not required; in this case, more attention is given to the step-up ratio to provide a higher voltage gain.

The limitations of frequency response generally restrict the use of transformer coupling to audio circuits which do not require an exceptionally wide bandpass or frequency response, but do require voltage or power outputs. Wide use is found for transformer coupling in the radio and intermediate frequency ranges where selective, high-Q bandpass falters and tuned transformers are universally used. See Tuned InterStage IF Amplifiers Circuit in another part of this section of the handbook for a discussion of tuned transformer coupling.

#### Direct Coupling.

Direct coupling is characterized by the direct connection of tube elements; that is, the plate of the driver stage is physically connected to the grid of the driven stage, and the coupling network is eliminated. A basic two-stage dc amplifier is shown in the following figure.



**Direct-Coupled Amplifier Circuit** 

Since the plate and bias circuits are not isolated by a transformer or coupling capacitor the directcoupling circuitry is slightly complicated by the arrangement necessary to produce an effective negative bias. Usually a voltage-divider bias arrangement similar to that shown is used.

The cathode of V1 is biased by  $R_{\kappa_1}$  between points A and B on the divider, while the plate is connected through  $R_{L1}$  to point C, which is at a potential equal to approximately half the supply voltage. Plate current through load resistor  $R_1$  (which is also the grid resistor for V2) provides a negative voltage drop and bias on V2. The cathode of V2 is tapped back at point D on the divider, and produces a voltage in opposition to the drop across  $R_1 \cdot$  When RK2 is correctly adjusted, the voltage on the cathode of V2 is always more positive than the plate of VI (and the grid of V2), producing an effective negative bias on V2 of the desired value. Voltages must be chosen so that the grid of V2 is not driven positive by the input signaL Since the plate of V2 is at the highest positive point, it is more positive than the cathode and conduction occurs. Thus the plates are maintained positive and the grids negative, to provide the conditions required for operation.

Because there is no coupling network inserted between the output of one-tube and the input of the following tube, there is no phase distortion, time delay, or loss of frequency response. Since the plate and grid of the tubes are directly comected, the lowfrequency response is extended down to dc (zero frequency). The high-frequency response is limited only by the tube interelectrode-to-ground capacitance, plus the circuit distributed wiring capacitance. By appropriate matching (or mismatching) of tubes, high values of amplification and power output may be obtained.

Since the use of more than two stages requires plate voltages two or more times the normal value for one tube, plate supply considerations limit dc coupling to a few stages. Any change in the supply voltage affects the bias of all the tubes and is cumulative; therefore, special voltage supply regulation circuits are necessary. Noise and thermal effects in tubes produce circuit instability and drift that limit the use of this type of coupling in audio or r-f amplifiers.

Because of its ability to amplify direct current or zero frequency, dc coupled circuitry is often used in computer circuits, and in the output circuits of video amplifiers. Because response is practically instantaneous and no time delay occurs, it is especially valuable for pulse circuits. See Direct Coupled (DC) Amplifier circuit in another part of this section of the handbook for a more detailed discussion.

## COUPLING METHODS (SEMICONDUCTOR)

The transistor, like the vacuum tube, is usually connected in cascaded stages to amplify the low input signal to the large output value needed. Coupling is accomplished by using resistance-capacitance networks, impedance networks, or transformers, or directly, by connecting the output element to the input element of the succeeding stage, as described in the following paragraphs. The discussion in this section will be limited to the basic circuit and important considerations involved for audio or relatively lowfrequency circuits. When special combinations or design considerations are required to achieve a particular result (for example, r-f or i-f coupling), they will be discussed in the proper section with the special circuit with which they are used. Since all coupling networks are frequency responsive to a certain extent, some coupling methods afford better results than others for a particular circuit configuration. Generally speaking, resistance coupling affords a wide frequency response with economy of parts and full transistor gain capabilities, impedance and transformer coupling provide a more efficient power matching capability with moderate frequency response, while direct coupling provides the maximum economy of parts with excellent low-frequency response and dc amplification.

#### **R-C Coupling.**

The R-C coupler utilizes two resistors and a capacitor to form an interstage coupling device which provides a broad frequency response, with high gain, an economy of parts, and small physical size. It is used extensively in audio. amplifiers, particularly in the low-level stages. Because of its poor input-output power conversion efficiency (17 percent for the ideal case), it is seldom used in power output stages.

A typical resistance coupler is shown in the accompanying illustration. Resistor  $R_L$  is the collector load resistor for the first stage, capacitor CCC is the dc voltage-blocking and ac signal-coupling capacitor, and  $R_B$  is the input-load and de-return resistor for the base-emitter junction of the second stage.



**Resistance Coupling** 

Since the input resistance of the second stage is low (on the order of 1000 ohms for a CE circuit) and the reactance of the coupling capacitor is in series with the base-emitter internal input resistance, Ccc must have a low reactance to minimize low-frequency attenuation due to a large signal drop across the coupling capacitor. This is achieved by using a high value of capacitance; thus, for low audio frequencies, values of 10 to 100 microfarads or more are employed (compare this with the vacuum-tube coupling capacitance of less than 1 microfarad).

To prevent shunting the input signal around the low base-emitter input resistance, the base dc return resistor,  $R_{B}$ , is made as large as practical with respect to the transistor input resistance. Since increasing the base series resistance deteriorates the temperature stability of the base junction (see discussion of bias stabilization); the value selected for the input resistor is a compromise between reducing the effective shunting of the input resistance and maintaining sufficient thermal stability over the desired temperature range of operation.

The high-frequency response is normally limited by the stray circuit capacitance plus the input and output capacitance; hence, the transistor itself is usually the limiting factor. The low-frequency response is normally limited by the time constant of the coupling capacitor,  $C_{CC}$ , and the base return (input) resistance,  $R_{\rm B}$ . For good low-frequency response, the time constant must be long in comparison to the lowest frequency to be amplified.

Like the vacuum-tube coupling networks, transistor coupling networks may also be compensated to increase frequency response. Shown below are the basic equivalent circuits for three types of compensation: (A) shunt peaking; (B) series peaking, and (C) combined shunt-series peaking. Insertion of series inductor L1(A) produces a parallel resonant effect with output capacitance  $C_{oe}$  and input capacitance Cie and improves the high-frequency response about 50 percent. Insertion of inductor L2(B) in series with Ccc produces a series resonant circuit with input capacitance C<sub>ie</sub> and further increases the highfrequency response about 50 percent over that of shunt peaking. Using both series- and shunt-peaking effects (C) provides a gain about 80 percent greater than that of the series-peaking circuit alone.



Shunt, Series, and Combined Peeking Circuits

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Since the response to low frequencies is limited only by the coupling network, low-frequency compensation can be provided as in vacuum-tube circuits. The following figure shows a typical low-frequency compensation circuit. With resistor R1 inserted in series with R<sub>1</sub>, the collector load is increased at those frequencies for which the resistance of RI is effective. Since capacitor Cl parallels or shunts RI, it is evident that the higher frequencies are bypassed around it, but, since the capacitive reactance of Cl increases with a decrease of frequency, the low frequencies paas through R1. Thus, the load resistance for low frequencies is increased and so is the output at these frequencies. The combination of Cl and R1 is chosen to provide the desired frequency compensation. This type of compensation also corrects for phase distortion, which is usually more prevalent at the lower frequencies.



Low-Frequency Compensation Circuit

## Impedance Coupling.

The impedance coupler is used extensively in the transistor field. Here the increased power-handling (and matching) capabilities of the inductor provides more output than the load resistor. While the overall frequency response of impedance coupling is not as good as that of resistance coupling, it is much better than that of transformer coupling, because there are no leakage reactance effects to deteriorate the high-frequency response.

Part A of the following **figure** shows the basic impedance-coupling circuit, and Part B shows a typical variation. The high-frequency response of the impedance coupler is limited mainly by the collector output capacitance, and the low-frequency response is limited by the shunt reactance of the inductor, L1.

**The** efficiency of the impedance coupler is approximately the same as that of the transformer-coupled circuit (50 percent for the ideal case).



Impedance-Coupling Circuit2

## Transformer Coupling.

Transformer coupling is used extensively in cascaded transistor stages and power output stages. It provides good frequency response and proper matching of input and output resistances with good power conversion efficiency. It is relatively much more costly and occupies more space than the simple R-C circuit components, but it compares favorably in these respects with the impedance coupler. Its frequency response is less than that of the resistance- or impedance-coupled circuit.

A typical transformer coupler is shown in the following illustration. Coupling between stages is achieved through the mutual inductive coupling of primary and secondary windings. Since these windings are separated physically, the input and output circuits are isolated for dc biasing, yet coupled for ac signal transfer. The **primary** winding presents a low dc resistance, minimizing collector current losses and allowing a lower applied collector voltage for the same gain as other coupling methods, and it presents an ac load impedance which includes the reflected input (base-emitter) impedance of the following stage. The secondary winding also completes the base dc return path and provides better thermal stability because of the low dc (winding) resistance. Since the transistor input and output impedance can be matched by using the proper turns ratio, maximum available gain can be obtained from the transistor.



**Transformer Coupling** 

As in the impedance coupler, the shunt reactance of the transformer windings causes the low-frequency response to drop off, while high-frequency response is limited by the leakage reactance between the primary and secondary windings, in addition to the effect of collector capacitance. Because of the low dc resistance in the primary winding, no excess power is dissipated, and the power efficiency approaches the maximum theoretical value of 50 percent.

## Direct Coupling.

Direct coupling is used for amplification of dc and very low frequencies. As in vacuum-tube circuits, this method of coupling is limited to a few stages since all signals are amplified, including noise, and it is extremely susceptible to instability because of shift of operating point, cumulative dc drift, and thermal changes. Its use in power output stages is limited because of the low conversion efficiency (about 25 percent). It does offer an economy of parts, and it lends itself to the use of complementary-symmetry circuitry.

The following figure shows a base dc **amplifier** utilizing two PNP transistors and two power sources. When a signal is applied to the base of Q1, the amplified output is directly applied to the base of Q2 from the collector of Q1. The output is taken from load resister  $R_{L}$  of Q2. Since the base bias of Q2 is applied through  $R_{B2}$ , the amplified signal on the collector of Q1 must not drive the base of Q2 positive; that is, it must not exceed the negative bias.



DC Amplifier

The following figure shows a basic connection not possible with electron-tube amplifiers. The grounded-base circuit of Q1 is **direct-connected** to the **grounded-emitter** circuit of Q2. Thus the input circuit of Q2 is the load for Ql, and collector bias for Q1 is obtained through the collector-to-base junction of Q2. Since Q2 biases Ql, only one power source is needed.



**CB to CE DC Amplifier** 

A typical complementary-symmetry circuit using an NPN and a PNP transistor is shown in the following figure. Since the currents flow in opposite directions, thermal effecta oppose and stabilize each other. As in

the DC Amplifier circuit, the collector bias for Q1 is obtained from the base-collector junction of Q2.



## Complementary-Symmetry DC Amplifier

If another stage were added an additional and larger collector bias supply would be required to maintain the collector-to-base potential negative for each stage. This limitation is analogous to that of the dc supply for the vacuum-tube amplifier. It is also evident that a shift of dc bias potential would be amplified and passed along to the second amplifier, whereas in the ac coupled **(resistance-capacitance)** amplifier such a dc shift would be blocked by the coupling capacitor.

Note the use of complementary symmetry or the use of one transistor to bias another with dc coupling affords the miminum of component parts possible, and represents an economic advantage that is possible only with transistors.

Special bias circuits are used with dc amplifiers to reduce thermal effects; see bias stabilization previously discussed for the basic circuitry.

## TIME CONSTANTS

In the previous paragraphs on coupling circuits, it has been shown that lumped inductance, capacitance, and resistance are used to couple together various electronic circuits. It has also been shown that these basic components are affected in various ways when responding to signals of different frequencies. Properly connected they can be used to shape, control, or distort signal waveforms. Since R-C end LR combinations contain lumped capacitance or inductance, they always require a finite time to charge or discharge, and thus provide a simple arithmetical figure (time constant) which is useful in the discussion of the operation and performance of these circuits.

## **R-C Circuits.**

**The** time constant (TC) of an **R-C** circuit is defined as the time in seconds that is required to charge (*or* discharge) the R-C network to an arithmetical value of 63.2 percent. As normally used, it is defined as the time it takes the charge to reach 63.2 percent of the maximum charge, or to discharge 63.2 percent and to reach 36.8 percent of the initial (maximum) value. To obtain the time constant, the value of the resistance in ohms is multiplied by the value of the capacitor in farads (or megohms and microfarads); that is, TC = R x C.

Consider now the action of a series R-C circuit when a voltage is applied. The capacitor charges heavily in an exponential manner, following the charging curve shown in the following illustration. At the end of a period of time equal to one time constant the voltage across the capacitor reaches 63.2% of the maximum value of voltage applied. If the charge is continued, at the end of the second time constant interval it rises 63.270 of the value remaining at the end of the first time constant (36.8%), to reach a new value of 86.4% maximum voltage (23.2% remaining). Thus at the end of five time constants the voltage has reached a value of 99.370 of maximum or almost full charge. Theoretically, the condition of complete charge (or discharge) will not be obtained but the difference is so infinitesimally small after five time constants that the remaining value can be neglected.



capacitor Charging Curve

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When the capacitor is fully charged, if the applied voltage is removed and the capacitor is connected across the resistor, it begins to discharge through the resistor at an exponential rate. Discharge occurs as shown by the following cuwe. At the end of five time constant intervals of discharge the voltage across the capacitor is approximately zero.



capacitor Discharge Curve

Comparing the illustrations showing the charge and discharge, it is evident that the curves are identical in shape, but that one is the reverse of the other. That is, while it takes one time constant interval to reach 63.2% of the applied voltage (or charge) with 36.8% to go, conversely, it also takes one time constant interval to reach **36.8%** of the initial capacitor voltage (63.2% discharge). The vertical portion of each illustration represents the amount of voltage, current, or capacitor charge in percent.

A time constant interval may be considered short when the RC product is equal to, or less than, 1/10 of the period of the applied voltage. Likewise a time constant may be considered long when the RC product is equal to, or greater than, ten times the period of the applied (pulse) voltage.

Short time constant circuits are employed in differentiating circuits which change a square wave into positive and negative pips. Conversely, long time constant circuits are use to reproduce a square wave with fidelity, or to integrate (sum up) a series of pulses and change them into a single sawtooth, rectangular, or square wave. The following figure briefly illustrates

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the signal-shaping effects of long and short time constant circuits. For a complete discussion of the waveshaping effect of the R-C circuit, refer to the Special Circuits section of this handbook.



Waveshaping Effeets of RC Circuits

Time constants are sometimes used in audio coupling networks to define the low-frequency response. For example, the frequency at which the response of a single resistance< **oupled** stage falls 3 dB (theoretical cutoff frequency) is:

$$f_{\circ} = \frac{1}{27rRC}$$

Therefore, if the time constant of a network is 3000 microseconds, the low-frequency response limit of the network is found as follows:

$$f_{o} = \frac{1}{2x3000 \times 10^{-6}}$$

Time constant is also related to frequency by the formula

$$F = \frac{1}{TC}$$

where F is in Hertz, and TC is in seconds. **Thus** a time constant of .01 second corresponds to a frequency of 100 Hertz. Since TC equals R times C, this time constant could be produced by a **0.01-\muf** capacitor and a 1-megohm resistor (or 0.1  $\mu$ f and 100K).

R-C circuits are also used as decoupling networks, feedback networks, and high- and low-pass filters. The

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**figure** following shows a few basic R-C circuit arrangements which illustrate possible combinations.



#### **R-C Circuits**

**Part** A of the figure illustrates a typical low-pass **filter** arrangement, where the low frequencies are passed without attenuation, but the higher frequencies are attenuated. Input and output relationships are shown by the formula, and for a specific time constant vary directly as the capacitive reactance. Part B shows a typical high-pass circuit which passes the higher frequencies and attenuates the low frequencies. Here the attenuation increases with a decrease of frequency, with greater output for the higher frequencies. Part C shows a parallel R< network which is inserted in series with the coupled stages; it **functions** to bypass the higher frequencies across the resistor, with R and RI acting as a voltage divider at the lower frequencies.

Since most electron tube elements are biased through a series resistor bypass by a capacitor, it is evident that quite a number of time constant circuits *exist in any* circuit configuration. The effect that the time constant has with regard to frequency response and time delay becomes an important factor in the design of pulse circuits. See the Filter Circuits Section and the Special Circuits Section of this handbook for a complete discussion of these factors.

#### **R-L** Circuits.

The time constant (in seconds) of a circuit containing an inductor and a resistor connected in series can be found by dividing L (henrys) by R (ohms),

$$TC = \frac{L}{R}$$

If a dc voltage is applied to a series **L-R** circuit, the output current does not rise instantaneously to a maximum value at the instant the voltage is applied.

The rise of current is slowed down because the inductance produces a self-induced counter voltage which opposes the applied voltage, causing the inductance to oppose any change in cument flow. Thus, current flow begins at a zero rate and increases exponentially as the self-induced counter emf decreases. When a voltage is applied to an R-L circuit, the voltage across the inductor declines as shown in the following illustration.



Inductor charge Curve

At the end of tive L/R time intervals, the counter voltage across L drops to approximately zero volts. During the same time interval the voltage drop across R, which results from the current flow in the circuit, begins at zero volts and increases at an exponential rate until, at the end of five time constant intervals, the voltage across R nearly equals the applied voltage (similar to inductor discharge curve illustrated.)



Inductor Discharge Curve

When the applied voltage is removed, the inductor again opposes the change in current flow by attempting to keep the current flowing. The counter

## **ELECTRONIC CIRCUITS**

emf now produced causes the current to decrease at an exponential rate. The voltage across R (and across the inductance) during the decay period, shown in the inductor change curve, drops to approximately zero volts at the end of five time constant intervals.

The following figure shows the circuit for basic LR networks. Operation is identical for the comparable types of R-C networks, previously described.



#### L-R Circuits

Part A of the figure illustrates a typical low-pass filter arrangement. Since the reactance of Lincreases directly with frequency, the higher frequencies are attenuated and the lower frequencies are passed. Part B shows a typical high-pass circuit, which develops a larger voltage across the inductive reactance at the higher frequencies than at the lower frequencies. In part C the inductor acts as a variable shunt for R at the lower frequencies and as a voltage divider with RI at the higher frequencies.

Since the inductor has distributed (turns) capacitance across it, undesired resonant responses may occur in LR circuits containing large values of inductance; therefore, the use of these networks is usually limited to high-frequency applications. A practical application in resistance+ **oupled** circuits is the insertion of a small inductance in series with the plate resistor or in series with the grid coupling capacitor to improve video response. **These** circuits are called shunt and series peaking circuits, respectively, and are illustrated in the following figure.



Shunt and Series Peaking Circuits

In the shunt peaking circuit, the increased inductive reactance at the higher video frequencies produces an effectively higher load impedance and larger output signal for coupling to the next stage. When the peaking inductance value is selected to resonate with the shunt capacitance to ground of the electron tube, a parallel resonant circuit is obtained which also boosts amplification at and around the resonant frequency. The series peaking inductance is usually selected to produce a series resonant circuit with the grid-to-ground tube and circuit capacitance. By combining both shunt and series peaking in a stage, greater high-frequency response is obtained. Excessive compensation, however, may cause unwanted transient responses. See discussion of Video Amplifiers in another part of this section of the handbook for a more complete discussion of peaking circuits.

# SPECIAL CONSIDERATIONS FOR TRANSISTOR CIRCUITS.

The time constant as defined for electron tubes is the same for transistors. It is important to realize that transistors differ primarily from electron tubes in their input and output resistances and their capacitances. Where time constants are used in the grid

circuit of an electron tube with essentially **infinite** input impedance, it is not **necessary** to be concerned with the input-impedance effect on the time constant. Since the transistor has a finite and relatively low input impedance, however, it may affect a timeconstant circuit. **Also**, the capacitance to base of the transistor is usually larger than the electron tube plate-to-ground or grid capacitance; hence, when it shunts the time-constant circuit, it must be considered.

Thus it can be seen that R-C and LR circuits used for **time-delay**, coupling, and frequency-response effects and for the shaping of pulses and the controlling of switching circuits are practically interchangeable (except for shunting effects) between electron-tube circuits and transistor circuits. Transient conditions which produce large overshoots must be avoided in transistor circuits-because the transitor is more easily damaged then the electron tube by potentials which exceed the maximum rated voltages. Generally speaking, therefore, the R-L circuit is used less than the R-C circuit.

On the other hand, because of the shunting effects of the internal transistor parameters, the highfrequency response is degraded, even in the audio range. Consequently, when high frequency response is desired, more high-frequency compensating circuits are used with the transistor than with the electron tube. Therefore, the use of **time-constant** circuitry will be completely discussed in the applicable circuit analysis in other sections of this handbook, since it depends primarily on the type of transistor selected.

# PART 5-1. DC AMPLIFIERS

# DIRECT-COUPLED (DC) AMPLIFIER (ELECTRON TUBE)

#### Application

The direct-coupled amplifier, commonly known as the *dc* amplifier; is used where it is necessary to amplify extremely low-frequency signals extending down to, and including zero frequency (direct current). The most common application of the dc amplifier is in the dc vacuum-tube voltmeter. This amplifier also finds use in a balanced bridge circuit, where two dc voltages are to be compared, and the difference between them is to be indicated on a meter. Another important application is in the signal input amplifier of an oscilloscope which is designed to accept lowfrequency or direct-current inputs for waveform display. Other uses of a direct-coupled amplifier are: to isolate two dc circuits while allowing a transfer of signal from the first circuit to the second but not in the reverse direction; to add two or more dc voltages to produce a dc output proportional to their sum multiplied by a constant factor; and to reverse the polarity of a dc voltage while either keeping its numerical value unchanged or increasing its numerical value by a constant factor.

#### Characteristics.

The comection between the output (plate) of one stage and the input (grid) of the dc amplifier is a direct metallic connection, without the use of any intervening coupling device such as a capacitor, impedance, or transformer.

Amplification of very low frequencies, or very slow variations of voltage, is accomplished without distortion and with uniform response.

Speed of response is practically instantaneous; pulse **signals** maybe amplified without any distortion due to differentiation.

Input impedance is high; no grid current flows.

Output impedance is very low; can be made as low as one or two ohms.

Polarity (phase) of output signal is reversed by a single stage, or odd number of stages, of amplification. An inphase output signal may be obtained by use of an even number of stages.

## Circuit Analysis.

General. In most vacuum-tube amplifier circuits, the coupling device used between the output (plate) circuit of the preceding stage and the input (grid) circuit of the amplifier stage aUows only the alternating components of the output signal to pass through. At the same time, the coupling device serves to isolate the highly positive voltage, which often has a value of several hundred volts, at the plate of the preceding stage, from the low signal bias voltage at the grid of the amplifier stage. In resistancecapacitance-coupled and impedance-coupled amplifier circuits, the coupling capacitor prevents the plate sup ply voltage from being applied to the grid of the succeeding stage. In transformer-coupled amplifier circuits, the electricrd isolation between the primary and secondary windings prevents the plate supply voltage, which is present in the primary winding, from being applied to the grid circuit, which includes the secondary winding.

In the direct-coupled (or dc) amplifier, the output (plate) of the preceding stage is connected *directly* to the input grid of the amplifier, without the use of any intervening means of coupling such as a transformer or capacitor. This requires a more complex method of supplying the required voltages to the amplifier tubes, since the plate of each tube must be supplied a positive voltage with respect to its cathode, and the grid of the following tube must be supplied a negative bias voltage with respect to its cathode; this grid, of course, is rdready supplied with the positive plate **potential** of the preceding plate through a direct connection. A special voltage-divider network is therefore required to supply the various values of bias and plate voltage for each amplifier stage.

**Circuit Operation.** A typical dc amplifier circuit is shown in the following illustration. In this circuit, the input signal is applied, across grid resistor Rl, directly to the grid of the first section of twin-triode tube VI, which is used as a two-stage triode amplifier. The grid resistor is returned to the most negative point on voltage divider R4, designated as point a. The cathode is connected to point b on R4, which establishes the proper grid bias for operation of VIA, since point a is more negative than point b. The exact location of point b on voltage divider R4 is somewhat critical, since the terminal voltage at point b depends **upon** 

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the values of current flowing at each of the voltage divider taps b, c, and d, as well as upon the applied **voltage**,  $E_{bb}$ . **Plate voltage** is taken from tap d on R4, and applied through plate load resistor R2 to the plate of VIA. Plate load resistor R2 also serves as the grid resistor for the second amplifier stage, VIB, and the plate current flowing through the resistor establishes the grid voltage of VIB at the value existing at point d less the voltage drop across resistor R2. The location of point d on the voltage divider is such that approximately one half of the total power supply voltage,  $E_{bb}$ , is applied to the first amplifier stage, VIA.



**Two-Staged Direct-Couplad Amplifier Circuit** 

The cathode of the second amplifier stage, VIB, is connected to the voltage divider at point c, where the voltage is more positive than the voltage at the grid of VIB by the amount of the desired grid bias. (The voltage at point c is more positive than that at the grid of VIB because of the voltage drop through resistor R2.) The plate of the second stage furnishes the output of the amplifier, which is taken across plate resistor R3 by direct connection, without the use of any intermediate means of coupling. Resistor R3 is connected to the high side of voltage divider R4 at point e, and capacitor C 1 acts to smooth out any ripple from the power supply. The entire circuit comprises a resistance network which, because of its complexity, requires careful adjustment at the voltagedivider taps, in order to obtain the proper grid and plate voltages for both tubes. When these voltages are properly adjusted to obtain Class A operation, the circuit acts as a distortionless amplifier, having a uniform frequency response over a wide range, and a response time which is practically instantaneous.

Assuming that the voltages have been adjusted for Class A operation, the normal voltage conditions of the circuit with no signal applied to the input are shown in part a of the following illustration. The fixed value of grid bias, from the power supply, is indicated as a negative voltage, and the no-signal output voltage is indicated as a positive voltage. This is the value of voltage drop across plate resistor R2, resulting from the plate current-flowing under noinput-signal conditions. At time b of the illustration, a negative input signal voltage of fixed value has been applied to the grid. The negative input voltage adds to the fixed value of grid bias voltage, which is also negative, to make a new value of grid bias, ahown by the lower solid line at time b. This more negative grid voltage causes less current to flow in the plate circuit through plate resistor R2, producing a higher voltage at the plate, as indicated by the upper (output voltage) solid line at time b of the illustration.



DC Amplifier Input-Output Voltage Characteristics (For a Single Stage)

#### **ELECTRONIC CIRCUITS**

At time c the input signal has been removed, and the grid bias and output voltage values have returned to the levels shown at time a. At time d a positive input signal voltage has been applied to the grid of V1. The positive input voltage subtracts from the (negative) fixed value of grid bias voltage, to produce a new value of grid bias which is less negative, as shown by the lower solid line at time d of the illustration, close to the zero voltage bias level (if the positive input voltage is too high the grid will be drawn into the positive region, grid current will flow, and the output signal will be distorted. Under such conditions, the amplifier will not operate within Class A limits.) As a result of this less negative bias voltage, a greater current is caused to flow in the plate circuit, through plate resistor R2, and a lower voltage is produced at the plate, as indicated by the upper (output voltage) solid line at time d of the illustration. At time e the voltages have returned to their original values, following the removal of the input signal.

For purposes of explanation, the discussion of the effects of the input signal and the output voltage has referred to only one stage **(V1A)** of the two-stage direct-coupled amplifier circuit illustrated. The operation of the second stage **(V1B)** is identical. It should be noted that the signal at the output of the first stage is reversed in phase by 180 degrees. This is evident from the illustration of the input-output characteristics, where the negative input signal produced a positive output signal. An additional 180-degree phase reversal is produced by the second' stage, giving an output signal from the two-stage amplifier circuit which is in phase -with the input signal.

A very practical application of the dc amplifier circuit is found in its use as a dc vacuum-tube voltmeter. This circuit, utilizing a single triode, is shown in the following illustration. The voltage to be measured is applied, through a range switch, SW1, to a tapped voltage divider which "allows several ranges of voltage to be measured. The voltage divider is composed of several resistors, R1 through R4, with R4 also serving as the grid resistor for the triode dc amplifier, VI. Plate load resistor R5, having a value of 22K or higher, acts as a current- limiting resistor to protect the meter in the event of excessive input voltages. Variable resistor R6 functions as a balance control to allow the voltmeter to indicate zero volts with no applied input voltage. Voltage divider R8, connected across the input voltage from the power supply, is tapped to provide the proper grid bias and voltmeter balance voltages. When variable resistor R6 is adjusted for a zero voltmeter indication with no input signal, the voltage at point c on voltage divider R8 is exactly equal to the voltage at the junction of R5 and R6. Now when an input signal is applied, additional plate current flows through R5, R6, and R7, causing the voltage at the junction of R5 and R6 to drop to a lower value, while the voltage at point c on voltage divider R8 remains relatively constant. When properly calibrated, the meter indicates this voltage drop as the applied input voltage.



Vacuum-Tube Voltmeter Utilizing Direct-Coupled Amplifier Circuit

A disadvantage of this direct-coupled vacuum-tube voltmeter circuit lies in its poor stability of calibration. The plate current of the tube varies in a somewhat unpredictable manner with variations in filameter temperature, age of the tube, and variations in resistance of the coupling element with temperature variations. These variations are especially evident when an attempt is made to read small voltages accurately.

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### Failura Analysis.

No Output. Assuming that a signal whose amplitude (either positive, negative, or a combination thereof) is within the design limits of the dc amplifier, is applied to the input terminals, the primary cause of no output is a defective tube. If the tube is capable of satisfactory operation, the cause of a no output condition is obviously an incorrect voltage, or lack of voltage, at some point in the circuit. Referring to the first illustration (two-stage direct-coupled amplifier circuit), an open voltage divider R4 would cause one or more of the voltage taps to fail to supply the required voltage to either the cathodes of VIA or VIB or the plate of VIA. As a result, either VIA or VIB would fail to operate. An open resistor R2 would remove plate voltage from VIA, resulting in no output; a similar condition would occur if plate load resistor R3 opened, removing plate voltage from V1 B.

Reduced or Unstable Output. Assuming that a satisfactory signal is present at the input to the direct-coupled amplifier, an open grid resistor R1 would cause unstable output, along with intermittent grid blocking, or "motor-boating." A change in the supply potentials for any tube in a multi-stage dc amplifier would cause the currents and potentials of all succeeding stages to vary. If, for example, the grid potential of the first tube varies slightly, the gain of the amplifier will cause the current in the last tube to vary by a large amount. even to the point of decreasing to zero, or of increasing to an excessively high value. In either case, distortion will be introduced. A changed value of R4 (or portions or R4), or of plate resistors R2 and R3 would all have the effect of changing the supply potentials of the tubes. The amount of unbalance created, and, consequently, the amount of output distortion, will depend on whether the gain of one or both stages is involved in amplifying the unbalance. An open or partially shorted fillter capacitor Cl, if used, may cause hum or reduced output because of inadequate filtering of the input power,  $+E_{bb}$ . A decreased value of input power,  $+E_{bb}$ , due to a defective power supply, would also be a cause of reduced output.

# DIRECT COUPLED (DC) AMPLIFIER (SEMICONDUCTOR)

## Application.

**The** direct-coupled amplifier is used where high gain at low frequencies, or amplification of direct current (zero frequency) is desired. The direct-coupled amplifier is also used where it is desired to eliminate **loss** of frequencies through a coupling network. This circuit has numerous applications, particularly in computers, measuring or test instruments, and industrial control equipment.

## Characteristics.

Uses common-emitter circuit for high gain.

Usually requires thermal stabilization to prevent runaway.

Frequency response extends to zero frequency (direct current).

Responds equally well to pulses or sine waveforms.

## **Circuit** Analysis.

General. The transistor is a device which uses the change of current flow through a resistor to produce amplifying action. DC' bias potentials are applied to the transistor elements to fix the point of operation. In ac-coupled amplifiers, the dc biasing potentials are effectively isolated and remain unaffected by the operating signal. In dc coupled amplifiers, however, a change in voltage on one element (either ac or dc) appears also as a similar or amplified change on another element, so that the biasing point changes with the signal. In cascaded stages these changes are cumulative and thus present a problem in stability. Since transistors are also subject to thermal changes, it is evident that a thermal change appearing at one element is also applied to another element. No problem results if the circuit can be arranged so that the temperature increase or decrease is self< orrecting in the following transistor. In most instances, however, thermal instability becomes a major problem if more than two stages of dc amplification are cascaded.

## **ELECTRONIC CIRCUITS**

Germanium transistors are more subject to thermal instability than are silicon transistor, but in either case it is usually necessary to provide some form of temperature compensation if the temperature exceeds 55 degrees centigrade. The complexity of the compensation circuitry is dependent upon the amount of correction needed. Because of the rapid changes which are occurring in the semiconductor field, it is likely that temperature compensation will be eliminated or minimized to a great degree in the future. Even so, however, the primary limitation of direct coupling still remains, namely, the necessity for cumulatively increasing the bias and operating values as each stage is cascaded. While the use of low bias and collector voltage permits somewhat more range than can be obtained with the electron tube, the transistor, like the electron tube, is subject to maximum breakdown or reverse potential limitations.

In addition, noise is a problem since the dc amplifier amplifies any internal noise as well as the signal, and transistors are prone to produce greater noise at the lower frequencies. Thus, the ability of the dc amplifier to extend its response to low frequencies not normrdly available through other coupling methods is somewhat nullified by the amplification of the inherent noise in the transistor. Generally speaking, we can say the low-frequency response of the dc amplifier is limited only by the signal-to-noise ratio, while the high-frequency response is limited by the frequency-response characteristics of the transistor.

In the **direct-coupled** amplifier, the collector of the input stage is directly connected to the base of the second amplifier stage; therefore, any collector supply variation also appears at the base of the second stage, just as if it were a change in the input signal. Since the transistor in the second stage has no way of discriminating between actual input signal variation and first stage collector supply variation, it is evident that either type of variation will be amplified in the second stage.

By the same type of reasoning it can rdso be seen that, even in the absence of an input signal, a change in the gain of one stage (or the over-all gain of cascaded stages) as a result of collector supply variations, will produce an output signal. Similarly, a change in bias level in any stage or on any element will be amplified proportionally, and a change of output will occur. Such changes in bias levels normally occur as a result of temperature variations, aging, difference in transistor characteristic due to manufacturing processes, or changes in transistor leakage current, and are referred to as *drift*. (*This* has no comection with the process which occurs in drift transistors.)

The variation of the forward bias characteristics of a typical germanium diode with temperature is shown in the accompanying graph. The forward bias variation is usually expressed as a change in bias voltage with temperature at a constant forward bias current. It is usually small, but becomes significant because of the large amplification it receives because of the direct coupling arrangement.



**Emitter-Basa Diode Characteristic** 

The manner in which the collector-base diode varies its reverse saturation current with temperature is also shown in the following graph (for a typical germanium transistor). In this instance, the figure shows that the reverse-current characteristic is highly temperature-dependent, and relatively large current variations are produced as the temperature is increased.

In a similar manner, it can be shown that the forward-current transfer characteristic of a **germa**nium transistor also varies with temperature. However, in this case the gain can either increase or decrease with temperature (silicon types generally increase with temperature). The percentage variation in gain with temperature varies greatly with the operating point, and many units show a change in sign as

well as magnitude. The gain variation of a silicon type may be from two to ten times that of a germanium type. Thus, we can see that the major sources of drift in transistors are changes in the dc properties of the collector-base and emitter-base diodes, and changes in the dc forward transfer ratio. Generally speaking, in comparing the operation and performance of germanium and silicon transistors, it can be said that at temperatures below that of the reference temperature, TO, the two types are comparable. At and above the reference temperature, the silicon type tends to have lower drift. The reference temperature for silicon is 100 degrees centigrade, and that for germanium is 60 degrees centigrade. With low source resistance low values of drift are obtained above To, while with high source resistance the best performance occurs at temperatures where the reverse saturation collector current may be neglected.



Variation of Collector-Base Diode Reverse Current

In dc amplifiers, low drift is obtained by operating with low values of collector current; this reduces the reverse-leakage current by keeping the voltage between the collector and the base at a low value. This voltage is a forward bias for reverse current. Generally, any design precautions which reduce drift also reduce noise; conversely, with low noise less drift is obtained. When the collector current is reduced, the gain decreases and the internal emitter resistance increases. Because of the reduction of gain, the amount to which the collector current of the first stage can be reduced is somewhat limited. In **single-ended** amplifier stages, both the current drift and the voltage drift in the second stage tend to help cancel the input stage drift; in a differential dc amplifier, however, the drift in the second stage may either aid or oppose that of stage 1, depending upon the design.

Despite the apparent disadvantages of the dc amplifier, it does produce (for a two- or three-stage unit) high gain the good fidelity, particularly in the low-frequency portion of the spectrum. It also provides amplification with as few parts as possible; thus, it is economical to build. In actual practice the dc amplifier is usually limited to one or two stages of amplification because of drift, especially where dc must be amplified or where frequencies of O to 12 Hertz are of importance. To overcome the effects of drift in dc amplifiers a special "chopper amplifier" has been developed; this amplifier converts the dc into ac so that the stages can be isolated and thus prevent the cumulative drift which normally occurs. This is a special type of amplifier, which will be discussed later in this section of the Handbook.

Circuit Operation - Basic Circuit. The schematic of a basic common-emitter dc amplifier is shown in the accompanying illustration. The input signal is represented by the a-f generator with an internal resistance equal to  $\mathbf{R}_{\mathbf{G}}$ . The input signal is applied between base and emitter. Transistor Q1 is biased by  $R_{B}$ , using the form of external PNP self-bias explained in the introduction to this section of the handbook. (R<sub>B</sub> and the internal resistance of the base-emitter junction form a voltage divider across the collector supply, and a forward bias is developed across  $R_{p}$ .) The input signal opposes the bias between base and emitter, which is normally chosen for class A operation. The direction of electron current flow through the collector output load resistor,  $\mathbf{R}_{\mathbf{L}}$ , is indicated by the arrows. 'f'he polarity of the resulting dc voltage across the load resistor is as shown. When the positive alternation of the input signal is applied to the base, the base-toernitter bias is reduced (since the signal and bias voltages are of opposite polarity). Because the base-toemitter potential is now less than the normal value, the hole current from the emitter to the collector is lowered and electron flow through the output load resistor is reduced. The decrease is voltage drop across  $\mathbf{R}_{\mathbf{I}}$  produces a negative swing and, consequently, produces a negative output signal across  $\mathbf{R}_{\mathbf{I}}$ . As the sinewave input signal goes negative, the bias potential is

aided by the input signrd; and as the base-to-emitter bias is increased, more hole current flows to the collector. This produces more electron flow through the collector circuit, increasing the voltage drop across  $\mathbf{R}_{\mathbf{I}}$ , and produces a positive output signal swing during the time that the input signal is negative. This effectively produces an opposite-polarity output signal (sometimes referred to as a 180degree phase reversal). Since  $R_i$  is the load for both dc and ac, there is only one load line, and any internal noise voltages flowing through the load resistor add to the developed output voltage. Since the output across R<sub>1</sub> is applied directly to the base of the next stage, it can be seen that these noise components appear across the following input circuit. In an ac-coupled circuit these noise components, consisting of dc or very low frequencies, are usually eliminated (blocked by the coupling capacitor). These noise components are produced by thermal effects, and also result from electron flow through the load resistor. They include the so-called white noise generated by diffusionrecombination effects within the transistor (similar to shot noise in the electron tube), and surface and leakage noise from the transistor, which is sometimes referredto as semiconductor or I/f noise to distinguish it from white noise. Such noise is mostly confined to the region of from 1-to-10 kHz for white noise (in the audio range), with the semiconductor noise predominating and increasing for frequencies lower than 1 kHz. The dc noise results from supply voltage var<sup>i</sup>ations. Thus the noise components usually eliminated by the ac coupling capacitor in other types of amplifiers, creates a design problem in the small-signal type of dc amplifier. In large-signal amplifiers these noises are usually masked by the large input signaL Note also that any dc bias changes caused by thermal instability of the stage also appear across the load, and are applied to the input of the next stage. This is an inherent disadvantage of the dc amplifier. On the other hand, with proper input and output matching, maximum gain is obtained in the stage; moreover, with no coupling network to create a loss between stages, maximum output and efficiency are produced. Since all frequencies are present, including dc (zero

frequency), and are applied equally to the next stage, it can be understood why the dc amplifier presents maximum gain with excellent frequency response, particularly at the lower frequencies.



**Basic D-C Amplifier (CE)** 

Cascadad Stagas. Because of the high gain possible per stage, many applications require only a single stage of de-coupled amplification. Where more than one stage is required, transistors offer circuit arrangements that are not possible with electron tubes. For example, through the use of complementary symmetry it is possible to connect the collector of the input stage directly to the input of the second stage without disturbing bias arrangements, and to use the same supply. By using alternate arrangements of NPN and PNP transistors only one supply is needed. Recall that in the vacuum-tube dc amplifier, as each stage progresses the plate voltage is increased, with the grid being tapped back onto the preceding stage plate voltage to obtain the bias. Only tandem arrangements of similar type transistors can follow this principle. The term *complementary symmetty* is derived from the fact that the NPN transistor is the complement of the PNP transistor, with both circuits operating identically, but with opposite polarities. The accompanying figure shows a simple directcoupling circuit using complementary symmetry.

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**Tandem Coupling Arrangement** 

In this figure, the direction of electron flow is shown by the arrows. It is evident that the baseemitter junction of the second stage carries the collector current of the first stage. If the collector current of the first stage exceeds the maximum base-emitter current rating of the second stage, the collector resistor shown in dotted lines must be used. Otherwise, this resistor is not needed and proper design produces a saving in components. To do this, of course, the transistors must be of opposite types, (NPN to PNP, or PNP to **NPN**).

By the use of a special compounding connection, two transistors may be employed as a special type of dc amplifier to obtain linearity and almost unity gain (alpha). The accompanying figure shows the compound transistor connection using the common-base configuration.



**Compound Connection** 

Note that the input to the second stage is the base current of the first stage. Effectively, the input impedance is the series combination of the two transistors, while the outputs are in parallel. Such a circuit is roughly analogous to the push-push electron-tube circuit. Actually, this circuit is employed as a single-transistor compounded-type circuit, with emitter, base, and collector resistors used externally. The direction and relative values of current flow are shown in the figure, assuming the use of two transistors with an equal  $\mathbf{a_{fb}}$  of .95. When these values are converted to  $\hat{a}_{fee}$ , the total combination value (.9975) is equal to a gain of 399 as compared with an afe of 19 for a single transistor, or more than the normal gain of two stages in cascade (19x19 =381). Compounded transistors may be employed single-ended, or in complementary symmetry as push-pull stages, exactly es for single transistors. They represent a special end unique circuit alone; however, they are shown here to illustrate how they are derived from the basic **dc** amplifier. In most applications the compounded circuits form the output stages of an amplifier, or are used as the dc amplifier in a voltageregulator circuit. A typical high-gain preamplifier using an NPN and a PNP transistor in a directcoupled, cascaded, complementary-symmetry ampliier is shown in the following schematic. For simplicity end convenience, separate bias end collector supplies are shown. The output of the microphone is transformer-coupled (for proper matching) to the base of transistor Q1. Fixed class A bias is supplied to the emitter from a separate supply, and emitter swamping is provided by R1 shunted by Cl. Use of emitter swamping provides temperature stabilization for germanium transistors up to normal room temperatures, and for silicon transistors up to 100 degrees centigrade. The output of the first stage appears across collector resistor R2, and is directcoupled to the base of PNP transistor Q2. Capacitor C2 end resistor R3 form a low-frequency compensating circuit (or filter) across the load, shunting the higher frequencies to ground end effectively boosting the lower frequencies. This helps to compensate for loss of low frequencies in the microphone end transformer circuits. Transistor Q2 is emitter-stabilized by swamping resistor R5, bypassed by C3. Resistor R4, which is unbypassed, is placed in series with the emitter to provide degenerative feedback for improvement of the linearity end response. Resistor R6 is the

#### **ELECTRONIC CIRCUITS**

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collector load across which the output is developed. Fixed emitter bias is used with a **separate** collector supply for simplicity and convenience.



### Two Stage DC Amplifier (CE)

Assume that a sine-wave signal is applied to the input of T1; **as the** signal increases in a positive direction it adds to the forward bias of NPN transistor Q1. The increased flow of electrons through Q1 increases the emitter, base, and collector currents, and the external electron flow out of the collector produces a negatively polarized voltage drop across collector load resistor R2. Thus, for the entire half-cycle that the input signal goes positive and aids the forward bias, the output signal (at the collector of Q1) goes negative.

As the input signal changes polarity and becomes negative, it opposes the forward bias, causing a decreased electron flow through the transistor, and a proportional reduction in the emitter, base, and collector currents. The voltage drop across R2 is reduced **and** the collector voltage approaches that of the source, so that a positively polarized output is produced. Thus, for the entire half-cycle that the input signal goes negative and opposes the forward bias, the output signal (at the collector of Ql) goes positive.

Since emitter resistor R1 is bypassed by Cl, changes occurring during the audio cycle will have no effect. However, any slight changes in emitter current (produced by temperature variations in the transistor) which occur at a very slow rate develop a voltage across RI; this voltage increases or decreases the bias in a direction which opposes the change; see the introduction to this section of the handbook for an explanation of bias stabilization. Any noise voltage, thermal bias changes not compensated for by R1, and the amplified signal appear across collector resistor R2, and are applied directly to the base of Q2. Note that the signal at this point is opposite in polarity to that of the input stage. Capacitor C2 and resistor R3 form a high pass falter between the base and emitter of Q2, which shunts the high frequencies to ground; this effectively boosts the base response of the amplifier and compensates for any loss of low frequencies in the input transformer.

Transistor Q2 is a PNP type; the function of Q2 is just the opposite of the function of Q1. When the input to Q2 is positive, it opposes the fixed emitter bias and effectively reduces the forward bias. With reduced forward bias, the flow of hole current through the transistor is decreased, and the emitter, base, and collector currents are reduced proportionally. Therefore, the external flow of electron current through collector resistor R6 is reduced, and the collector voltage approaches that of the source, producing a negatively polarized output signal. The output is now of the same polarity as the input signal to transistor Q1, so that during the entire half-cycle that the input signal to Q1 is negative, the output of Q2 is negative.

When the input to Q2 is negative, the polarity is such as to aid the base-emitter bias and increase the effective forward bias. As the forward bias is increased, hole current flow through the transistor increases, and the emitter, base, and collector currents increase proportionally. Thus, the external flow of electron current through R6 into the collector of O2 is increased, and is in such a direction as to produce a positive output voltage. In a similar manner, this output voltage (of Q2) is of the same polarity as that at the input of Q1; thus, the effect of the two stages is to produce an output signal of the same polarity as the input signal (a similar effect is obtained when two electron tubes are used). To provide an oppositely polarized output signal, the stages must be an odd number.

Swamping resistor R5 is bypassed by C3, so that the audio-frequency changes will have no effect; however, slow thermal variations will produce a voltage across R5 in the proper direction to compensate for the thermal change, thus helping to stabilize the circuit.

Resistor R4, which is unbypassed, has a voltage developed across it for dc changes, noise changes, and audio frequency changes; since this voltage is in opposition to the bias produced by R5, it is degenerative, thus providing a form of negative feedback. The negative feedback improves the low-frequency response and stabilizes the stage so that input voltage variations are minimized. The amplified output of Q2 is either applied directly to a speaker or other output device, or transformer-coupled to other stages as desired,

A typical three-stage, single-ended dc amplifier is shown in the accompanying schematic. It represents the minimum of parts and dc supplies needed for a high-gain, three stage complementary symmetry type of dc amplifier for small signal applications.



Typical Three-Stage Amplifier

As shown, the base of the input stage is completed through the input device, it is effectively open, it has no driving voltage, and zero base current exists. The collector current, **ICEO1**, flows through the base of stage 2, which is biased by supply  $V_{\text{EE2}}$  in series with the emitter of stage 2. Since stage 1 uses an NPN transistor, the positive emitter bias of stage 2 is of the proper polarity to act as collector voltage for Q1.

Any change in the collector current of stage 1 appears at the collector of stage 2 in amplified form; that is,  $I_{c2} = B_2 I_{CEO1}$ , where B<sub>2</sub> is the current gain of stage 2. Stage 2 uses a PNP transistor; therefore, by complementary symmetry, stage 3 must also be an NPN stage similar to stage 1. The emitter bias for stage 3 is supplied through  $V_{EE3}$ , which is connected positive to ground. Thus, the collector supply of stage 3  $(V_{CC3})$  is of series-aiding polarity, and the total collector voltage is that of both the collector and emitter supplies of stage 3. In a similar manner, the collector voltage of stage 2 is supplied by  $V_{EE2}$  and  $V_{EE3}$ . The collector current of stage 2 is the base current of stage 3. The output of the amplifier appears across collector resistor R4, and the collector current is that of stage 2 multiplied by the amplification factor, or  $I_{c_3} = B_2 B_3 I_{CEO1}$ . Emitter resistor R1, R2, and R3, which are of a low value, provide degenerative feedback; they also act as emitter swamping resistors to help stabilize the amplifier with respect to temperature variations.

Assuming that the input stage has a collector current of 5 microampere and assuming a gain of 38, the second stage will have a collector current of 190 microampere. With a gain of 40, the thirci stage collector current will be 7.6 milliamperes. It is clear that any slight change in the current of stage 1 caused by temperature or noise will be greatly amplified and appear at the output of stage 3. With such sensitivity and amplification, therefore, it it almost mandatory that such an amplifier be temperature-co tnpensated. even if room temperatures do not vary excessively. Naturally, the amplitude of the input signal must be limited if true fidelity is to be obtained. Driving the transistor into cutoff and saturation would clip the peaks of the signal, just as in electron tube operation. It is also evident that **low-noise transistors must** be used; otherwise, the noise might mask the signal. Note that in this amplifier the small emitter bias of stage 2 operates as the collector voltage of stage 1. Low collector voltage is used to minimize noise generated in the input stage; this is similar to the techniques used for high-gain vacuum-tube amplifiers, where the plate voltage of the input stage is usually about 1/3 that of the other stages.

#### Failure Analysis

**No Output.** A no-output condition is generally indicative of either an open or shorted circuit, or a defective transistor. Usually, improper bias will cause

distortion or low output rather than no output at all. A resistance analysis should quickly reveal any opencircuited components, since only a few parts are involved. A forward and reverse resistance check of the transistor can be made to determine whether the transistor needs replacement. For a good transistor the forward resistance is low (less than a few ohms), and the reverse resistance is high(50K and higher.) With continuity throughout and components of the proper resistance, a simple voltage check should indicate the cause o f improper performance. Use a highimpedance vacuum-tube voltmeter; at the normally low voltages involved, the shunting effect of the usual 20,000 ohms-per-volt meter might be too great.

Low Output. Generally, low output results from improper biasing, causing either too great a flow of current or too small a flow of curren (but not cutoff). Defective bypass capacitors provide a leakage path for current which, in flowing through an associated series resistor, produces a voltage drop greater than normal. Usually such a condition can be easily checked by means of a voltage analysis. Where high-resistance paths have been introduced, either because of poorly soldered joints or aging components, a loss of output will usually occur. Ordinarily, these paths can be located by means of a resistance analysis. With the small number of components involved, either a voltage check or a resistance check should quickly isolate the trouble to a particular portion of the circuit. When making ohmmeter tests, be sure to observe the correct polarity and not to apply a forward bias to a circuit requiring a reverse bias or vice versa; exceeding the permissible bias can ruin the transistor. The use of a shorting bar (screwdriver) to ground should be avoided to prevent overload or accidental short-circuiting of the supply through components not designed to withstand the extra current. If the trouble cannot be located quickly by means of the simple voltage and resistance checks described above, the most effective trouble-shooting method is to apply an input signal and use an oscilloscope to check the signal path through the circuit. The highimpedance oscilloscope input will have little effect on circuit operation, and the disappearance of the signal or a change in amplitude will be immediately apparent as the signal is followed from point to point.

**Distorted Output.** Distortion is usually caused by operating the circuit with improper bias or supply voltage or by overdriving. The bias voltage should be checked with a VTVM to determine that they are

approximately normal. Then a test signal should be applied to the input and followed from point to point with an oscilloscope. A change in waveshape caused by distortion will then be immediately apparent. Where the circuit appears normal but a high ambient temperature exists, it is possible that thermal effects are changing the circuit parameters. The use of a fan to temporarily cool the unit should quickly indicate whether a thermal problem exists. A condition often occurs whereby a thermal problem exists while the chassis is installed in the equipment cabinet, but disappears when the chassis is removed to the bench for checking. When this situation is indicated, it is sometimes possible to make sufficient checks with the chassis in the cabinet to isolate the trouble. Overdriving is apparent if a reduction of the input signal amplitude eliminates the distortion. Overdriving will appear on the oscilloscope as a squaring off of the input waveform, since the tops and bottoms of the modulation peaks will be clipped. Since nonlinearity in either the input or output circuits of the transistors will cause distortion, it should be clear that a small amount of distortion will always be present. Where the distortion is excessive and other tests indicate normal values of voltage and bias, it may be necessary to select a more linear transistor. (This condition should not occur if the components meet Military Standards except where an overload has caused damage to the transistor.)

# PUSH-PULL DIRE CT-CO UPLEO (OC) AMPLIFIER (ELECTRON TUBE)

#### Application.

The push-pull direct-coupled amplifier (as well as the single-ended direct-coupled amplifier) can be used where it is necessary to amplify signals having a wide band of frequencies, especially in the lower-frequency range, which may extend down to and include zero frequency (direct-current). When, in addition, the requirements demand the amplification of a signal which has a larger voltage swing above and below a zero voltage level than can be handled by the singleended type, the use of the push-pull direct-coupled amplifier is mandatory. One application is in certain types of dc vacuum-type voltmeters, while another is in the signal amplifiers of an oscilloscope that is capable of displaying waveforms of various values of direct current. The push-pull dc amplifier is often utilized in the video circuitry of radar display systems.

In communications, it may be used as the amplifier for those teletype mark and space signals that consist of two voltage levels of direct current.

## Characteristics.

The connections between the plates (outputs) of one stage and the grids (inputs) of the push-pull dc amplifier are direct, metallic connections; no intervening coupling devices such as capacitors, impedances, of transformers are used.

Amplification of direct-current signals of varying voltage levels, as well as signals of very low frequency, is realized without distortion and with uniform response.

Distortion due to differentiation is eliminated; pulse signals of large amplitude may be amplified without change in waveform.

Speed of response is practically instantaneous.

Input impedance is high; Class A operation allows no grid current to flow.

Relative phase (with respect to ground) of the output signal is reversed over that of the input signal when a single stage, or odd number of stages, is used.

## Circuit Analysis.

**General.** The gain of an ordinary R-C coupled amplifier falls off rapidly as the frequency of the input signal is decreased below 40 Hz, because of the rapid increase in reactance of the coupling capacitor with a decrease in frequency. Therefore, the R-C amplifier is unsuitable for use in applications which require the amplification of very low frequencies, including zero frequency or direct current, without substantial loss of gain.

The push-pull direct-coupled amplifier is well suited for such applications, since the input signal is applied directly to the grids of two tubes, without the use of coupling capacitors. Frequency response is flat down to and including zero frequency, allowing the use of this circuit for amplification of steady-state dc voltages. The response at very high frequencies is limited by the stray capacitances in the circuit, which have a shunting effect, similar to that of the ordinary R-C coupled amplifier.

**Circuit Operation. The** accompanying schematic illustrates a typical two-stage push-pull direct-coupled (de) amplifier. This type of circuit may be found in applications such as the deflection amplifiers of radar scopes designed for electrostatic deflection, and the signal amplifiers (vertical-deflection amplifiers) of  $\checkmark$  high-quality test oscilloscopes designed for directcurrent waveform analysis.



## Typical Two-Stage Push-Pull Direct-Coupled (DC) Amplifier

The input signal, which may consist of positive or negative pulses, or both, or simply of a positive or negative dc level, is applied across the grids of VIA and VIB. These two triodes may be enclosed in the single envelope of a twin-triode such as type 12AU7A. Self-bias is provided both triodes by means of the common cathode resistor, R3, in combination with potentiometer R4, which provides a balance control for use in equalizing the gain of VIA and VIB. -. Plate voltage of a medium value (+150 volts) is applied through plate load resistors R5 and R6. Variable resistor R7 functions as a gain adjust control, and freed resistor R8 connected in series with it sets the low limit for the variable value of the total resistance between the two triode plates. This combination, R7 and R8, affords a relatively simple means, from the standpoint of circuit components, of adjusting the over-all gain of the amplifier, and thereby the amount of vertical deflection in oscilloscope applications. Resistor R8 should have a minimum resistance value on the order of 1.5K, in order to maintain this - minimum value of resistance as a plate-to-plate load when R7 is adjusted to its zero-resistance position. As R7 is adjusted from its maximum value, toward zero resistance, loading of the signal output from VIA and V1 B is increased, reaching a minimum value when R7 is adjusted to remove its resistance from the circuit. The maximum. positive and maximum negative excursions of the signal to be amplified may thereby be adjusted, while maintaining the over-all frequency response of the amplifier.

The amplified output signal from the plates of both triodes, VIA and VIB, is applied directly to the grids of the second stage triodes, V2A and V2B. Since the grids of the second stages are at the same positive potential as the plates of the first stage (some value less than +150 volts due to the voltage drop through R5 and R6), the cathodes of V2A and V2B must be placed at a somewhat greater potential than +150 volts (above ground), in order that the grids may be properly biased, i.e., negative with respect to cathodes. In this circuit, which utilizes self-bias, this is accomplished by the use of a large value of cathode resistance, composed of potentiometer R9 and resistors R1O and R11. Potentiometer R9 serves as a balance adjustment to equalize the gain in both halves of the second stage; in this application, it serves to "position" the waveform under observation on the oscilloscope screen. The bias on the cathodes is adjusted by means of variable resistor R11, while the total resistance of the combination R9, RIO, and RI 1 establishes the total bias voltage at the cathodes of V2A and V2B. This relatively large value of cathode resistance, which amounts to approximately 12K, would introduce degeneration into the circuit, resulting in a decrease in gain, if this were an unbalanced (single-ended) stage. In this (push-pull) circuit, however, the degenerative effect of one half of the circuit at any instant immediately cancels an opposite effect of the other half of the circuit, and no loss of gain occurs. Conversely, any tendency toward an unbalance in one half of the circuit introduces degeneration which acts in opposition to the initial tendency, thereby keeping both halves of the circuit balanced. Such a tendency toward an unbalanced condition might be caused by circuit drift, due to unequal cathode emission in the two triodes.

Plate voltage for the second stage triodes is applied, from a considerably higher voltage source than that of the first stage, through plate load resistors R12 and RI 3. Although an applied voltage of +400

volts, dc may appear to be excessive, it should be noted that the actual voltage at the plates of VIA and V1 B cannot exceed 250 volts positive with respect to the voltage at the grids, under any conditions (within Class A operating limits). Under normal operating conditions, with plate current flowing, the voltage on the plates will be considerably less than 250 volts positive with respect to the grids, due to the voltage drop in the plate load resistors, assuming that similar tubes are used in both stages (V1 and V2) with similar plate load resistors, and that no input signal is applied.

In the circuit illustrate, capacitors Cl and C2 are used in a compensation circuit; Cl connected between the output plate of one half of the circuit and the input grid of the opposite half, and C2 connected between the output plate of the second half of the circuit and the input grid of the first half. These capacitors are of very low value of capacitance, such as 0.5 pf, and function to allow positive (in-phase) feedback of the high frequencies only, leaving the midfrequency and low-frequency response unaffected. When the proper values of capacitance are used (these values vary with the values of plate resistance, operating voltages, and tube types), the response of the over-all circuit, which normally drops off with increasing frequency, may be maintained flat to a considerably higher frequency than would be possible without this compensation. The value of capacitance used in somewhat critical, in that if the capacitance is too high the amount of positive feedback will be excessive, resulting in oscillation and severe frequency distortion. In addition to maintaining the highfrequency response over an extended range, the use of high-frequency feedback offers an additional advantage. When direct current input waveforms are being amplified, in the case of the circuit illustrated, the extended high-frequency response acts to decrease the rise time of the leading edge of the input waveform. If, for instance, the input waveform is a direct current whose voltage increases instantaneously (the leading edge of a square wave) from one value of voltage to a more positive value, this perpendicular wavefront will be found, upon analysis, to be composed of an infinite number of frequencies. If all of these test frequencies could be passed by the amplifier circuitry, the output would be a perfectly perpendicular wavefront, as shown by 1 in the following illustration. Since no amplifier can pass frequencies which approach infinite values, without attenuation,

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the output of the amplifier will not be a waveform whose wavefront is perfectly perpendicular. Instead, the wavefront will begin to slope away from the perpendicular, causing an increased rise time, as shown by 2 in the illustration. As more and more of the high frequencies are attenuated by the amplifier circuitry (stated in another way, as the amplifier becomes more inferior in its high-frequency response), the sloping of the wavefront away from the perpendicular increases. Thus the originally perpendicular wavefront now becomes markedly sloped, with rounded corners as illustrated by waveform 3 below, whereas the original wavefront had sharp, 90-degree angles.



Waveform Distortion Due to High-Frequency Attenuation

Another typical circuit illustrating the use of a push-pull direct-coupled amplifier is given in the following illustration. Here, a voltmeter M having a zero-center scale is used in a vacuum-tube voltmeter circuit designed to indicate any unbalance between

the inputs to two halves of the push-pull circuit, and the direction and extent of such unbalance. The input circuit is center-tapped, to enable a comparison to be made between input A and B. The two direct-coupled tnode amplifiers, VI and V2, are connected in two legs of a bridge circuit, with the two input voltages to be compared applied to the grids of VI and V2, respectively. The grids are returned through grid resistors R1 and R2 to a negative fixed bias voltage. Plate voltage is applied through plate load resistors R3 and R4, with a voltmeter M shunted across both plates. With tubes V1 and V2 and resistors R1 and R2 properly matched, and no input signal applied to input A or input B, the circuit is perfectly balanced and no difference of potential across the plates of VI and V2 will be indicated by voltmeter M. This results from the fact that equal currents flowing through resistors R3 and R4 will give equal voltage drops across R3 and R4, and identical voltages will be present at the plates of both tubes. When a signal is applied across input A, the grid of V1 becomes more (or less) positive than the grid of V2, depending upon the polarity of the applied signal. If the input signal is positive, the more positive grid of V1 causes an increase in plate current through R3, creating an unbalance in the output circuit. As a result, the increased voltage drop across R3 causes the plate of V1 to become less positive than the plate of V2, and the difference between the two plate voltages will be indicated by voltmeter M. Voltmeter M is a centerscale-zero meter, and if the polarities of its connections in the circuit are correct, it will indicate a negative voltage. If a more highly positive signal is applied across input B, with the first signal remaining across input A, the grid of V2 will become more positive than the grid of V1. This will cause a higher *value* of current to flow through R4 than is already flowing through R3 due to the signal at input A, and the voltage at the plate of V2 will become less positive than the voltage at the plate of VI. As a result, the pointer of meter M will swing through zero to indicate a positive value of voltage difference between the two input Signals.

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Push-Pull Direct-coupled Amplifier Used in Vacuum-Tube Voltmeter Circuit for Two-Input Comparison

# Failure Analysis.

**No Output.** If a signal having an amplitude within the design limits of the push-pull dc amplifier is furnished at the input terminals, a defective tube should be first suspected as the cause of no output. Note that one defective tube will cause a no-output condition in a push-pull circuit only if this tube is a twin-type, and then only if both halves become defective at the same time. Referring to the first illustration (typical two-stage push-pull direct-coupled (de) amplifier), if VIA and VIB are the two halves of a twin-triode such as a type 12AU 7A, and if the VIA. section of the tube should become defective, the VIB section will still operate to furnish a reduced output. In a similar manner, the failure of any single resistor in the plate or grid circuits would *not* be a cause of a no-output condition, because the other half of the circuit would continue operating. However, if common cathode resistors R3, R1O, or R11 should become open-circuited or if the plate power supply to either stage (+150 VDC or +400 VDC) should fail, there would be no output.

Reduced Or Unstable Output. Assuming that a satisfactory signal is present at the input to the pushpull direct-coupled amplifier, a number of conditions could contribute to reduced output, which ordinarily would be a cause of a no-output condition in a single-ended amplifier. The failure of a single section

of a twin-triode, or of a single triode where singletriode type tubes are used, would cause a reduced output, as discussed in the previous paragraph. An "open" i any grid or plate circuit would **also** cause reduced output, because the other half of the circuit would continue to operate. The output, however, would probably be distorted, because either the positive or negative half of the input signal would be cut off. If either balance control R4 or position control R9 should become open-circuited at some point of rotation, an erratic output would be obtained with the control is operated across the point where the "open" exists. A simple misadjustment of R4 or R9, or of bias adjust control R11, with all other components operating normally, would contribute toward an unbalance which might result in reduced or distorted output. If capacitors C2 or C3 should change in value or become shorted, the circuit would become unstable and possibly go into oscillation. In this particular circuit, which is self-biased, a reduced value of plate voltage caused by a defective power supply would, in all probability, only result in a somewhat reduced output, the quality of which may remain acceptable. If, however, a circuit which employs freed bids should operate with reduced plate voltage, the output might be distorted, in addition to being reduced in value.

# DC CHOPPER AMPLIFIER (ELECTRON TUBE)

### Application.

The dc chopper amplifier is used mainly in analog computers as a high-gain low-frequency (de) amplifier.

# Characteristics

Uses both direct coupled and dc coupled amplifiers.

Uses a chopper to change the dc signal to an ac signal of proportional amplitude.

Provides essentially drift-free low-frequency amplification.

Is particularly suitable for linear amplification or small dc voltages.

Is normally Class A self-biased, although **fixed** bias may be employed in some applications.

# Circuit Analysis.

General. As has been explained previously in the discussion of the dc amplifier, extraneous circuit and tube noise, as well as temperature-induced gain variations in cascaded stages becomes cumulative, and tends to reduce the amount of amplification available. This occurs because these unwanted, slowly varying low-frequency signals cause a dc drift voltage to be produced. Such action does not occur in a conventional ac coupled amplifier because the coupling network passes only the ac component of the signal. Thus, any dc components resulting from noise, temperature, or other factors are isolated within the stage and are not passed on to the next stage. Consequently, with dc amplifiers used in instrumentation where the signal amplitude indicates a quantity being measured, or where it is used to control a measuring circuit, it has been found that converting the original signal to an ac voltage, amplifying it, and then reconverting it back to a dc voltage, eliminates the driftvoltage problem and permits more stable operation.

Another method of compensating for drift in high-gain dc amplifiers is to employ a compensating circuit in which the drift voltage is changed to an ac voltage, is amplified, and is then fed back as a dc voltage to compensate for the original drift voltage change. In other texts, the circuit which converts the dc voltage to an ac voltage is called a *modulator*, and the circuit which converts the ac voltage back to dc voltage is called a *demodulator*. In this sense, the chopper amplifier corresponds to the modulator. In this handbook the term *modulator* and *demodulator* are used in the conventional sense, involving the transfer of desired intelligence from one signal to another and the detection or recovery of this signal, respectively.

Prior to the use of the transistor, chopper amplifiers usually employed electromechanical vibrators, photosensitive crystals, and in a few cases, magnetic amplifiers. Because of the appreciable power required to drive the vibrator, coupled with problems of vibration and shock, and relatively short life (about 100 hours), the mechanical chopper is considered inferior when compared with a transistor chopper. The photosensitive devices, likewise, are less desirable because of their complex circuitry. While magnetic amplifiers are still in the developmental stage, their large physical size and relatively large power requirements restrict their use.

**Circuit Operation. The** accompanying schematic shows a typical mechanical chopper amplifier circuit.

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DC Chopper Amplifier

In the schematic RI, R2, and Cl form a low-pass input falter, while C2 is an input coupling capacitor. Tubes V1 and V2 are conventional triode resistancecapacitance coupled ac amplifiers using coupling capacitor C3, and plate resistors R4 and R5. Resistors R3 and R8 are the grid return resistors. Cathode bias is supplied by resistors R9 and R1O, bypassed by cathode bypass capacitors C5 and C6, respectively. Cathode bias is obtained by plate current flow through the cathode resistors. (See the introduction to this section of the handbook for a more complete explanation of cathode biasing.) Capacitor C4 is the output coupling capacitor with resistor R6 as its current-limiting resistor (R6 and C4 also form an integrating circuit when grounded). Resistor R7 and capacitor C7 form a low-pass smoothing filter at the output. Synchronous chopper vibrator G1 converts the dc input to ac, and the ac output to dc.

The dc signal to be amplified is applied to the input and Cl bypasses to ground any high frequencies while RI and R2 form resistive smoothing chokes to ensure that the input is only a slowly changing lowfrequency voltage equivalent to dc. With the synchronous vibrator arm of G1 resting on contact 1, the input to V1 is effectively grounded, and both V1 and V2 rest in the quiescent no conduction condition. Thus, there is effectively no output other than that generated internally by tube noise. With no input signal applied to V1 and the synchronous vibrator arm resting on contact 2, output coupling capacitor C4 is connected to ground, and charges to the quiescent plate voltage of V2. Simultaneously, output capacitor C7 is grounded through R7 and there is effectively no output.

When a positive dc input is applied to VI, the plate of VI goes negative because of the increase in conduction by V1, thereby causing the plate voltage to decrease. This negative swing is coupled through capacitor C3 to the grid of V2, driving it in a negative direction. The plate current of V2 is thereby reduced, and the plate voltage of V2 rises toward the supply voltage. With the synchronous vibrator arm resting on contact 2, capacitor C4 charges to the high positive plate voltage on V2. When the synchronous vibrator arm on G1 moves to contact 1, the input voltage to tube V1 is removed (shunted to ground) and both

plates VI and V2 return to their quiescent voltage values and, since C4 is no longer grounded, it discharges through R7 and the load, charging output capacitor C7 negatively. Thus, even though the signal has in effect passed through two stages of amplification, a positive input produces a negative output and effectively inverts the signal, as is required for a dc amplifier for computer use.

If a negative dc input is applied to the V1 grid, the plate voltage rises and drives the grid of V2 positive, drawing more plate current through plate resistor R5, and charges capacitor C4 negatively, provided that it is grounded through contact 2 of vibrator G1. Thus, when the input is grounded by the synchronous contact arm of Cl moving to contact 1, a positive discharge voltage is developed across C7. Again, the signal has been inverted and amplified through a twostage ac amplifier. The grounding of the input signal through vibrator contact 1 produces an ac signal from the dc input, while the grounding of C4 and the output by contact 2 effectively rectifies the output of the ac amplifier by acting as an integrator and providing a negative output. The action of R7 and C7 as a smoothing filter removes any ripple component and averages out the integrated capacity discharge to protide an essentially smooth dc output. The instantaneous waveforms are shown in the accompanying waveform chart.



**Operating Waveforms** 

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Waveform No. 1 shows the positive dc input to C2, while waveform No. 2 shows the chopped input waveform which is reduced to zero on alternate cycles. The chopped ac waveform averages itself about a new axis on the gride side of capacitor C2, as shown by waveform No. 3. The amplified and inverted plate signal is shown in wavefom No. 4 and appears on the grid of V2. The plate output of V2 is shown in waveform No. 5, while waveform No. 6 shows the discharge of C4 as a series of negative pulses. The smoothed pulses appear as a steady average negative dc output voltage, as shown in waveform No. 7. Since the chopping occurs at a constant rate and is equal for both input and output, the ac and dc signals are proportional. Since Class A bias is used in the ac amplifier, the overall amplification is linear.

### DC CHOPPER AMPLIFIER (SEMICONDUCTOR)

# Application.

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**The** transistor chopper type of dc amplifier is used in analog computers, instrument recorders, and servo-mechanism control systems to convert dc (lowfrequency) voltage to ac voltage, for drift-free amplification.

## Characteristics.

Uses common-emitter circuit normally, but may also use the inverted form (emitter connected as collector, and collector connected as emitter).

Is free of cumulative dc drift.

Is particularly suitable for linear amplification of small dc voltages.

Uses a rectangular audio-frequency input signal of steady amplitude to provide the chopping action.

Is Class A-biased and normally uses self-bias, although fixed bias may be employed in some applications.

## Circuit Analysis.

**General. As** has been explained previously in the discussion of the dc amplifier, extraneous circuit and transistor noise, as well as temperature-induced gain variations, in cascaded stages becomes cumulative and tends to reduce the amount of amplification available. This occurs because these unwanted signals cause a dc (drift) voltage to be produced. Such action does not occur in a conventional ac-coupled amplifier

because the coupling network passes only the ac component of the signal. Thus, any dc components due to noise, temperature, or other factors are isolated within the stage and are not passed on to the next stage. Consequently, with dc amplifiers used in instrumentation where the signal amplitude indicates a quantity being measured, or is used to control a measuring circuit, it has been found that converting the original signal to an ac voltage, amplifying it, and then reconverting it back to a dc voltage eliminates the drift-voltage problem and permits more stable operation.

# Failure Analysis.

**No Output.** Lack of input voltage or plate supply voltage, open resistor, shorted capacitors, as well as a defective tube can cause loss of output. If R1 or R2 is open, or Cl is shorted, or if vibrator Cl remains on contact 1, no input will be applied to C2 measure the plate voltage and cathode voltage of V1 and V2. If voltage is not present or is abnormal, resistors R4, R5, R9 and RIO may be defective or capacitors Cl, C5, and C6 could have shorted to ground. Determine if the 60 Ha voltage is applied to chopper Cl and observe that it operates. If ac voltage is applied and the chopper does not operate, the vibrator is defective. Check that a signal exists on the grid of V1. If no signal appears, check C2 for an open circuit (make certain the chopper ann is not resting on contact 1.) if a signal appears on V1 grid but not on the plate, V1 is probably defective. If a signal appears on the plate of V1 but not on the grid of V2, check C3. Check the resistance of R3 and R8 also to make certain they are not shorted. If an input exists on the grid of V2 but not at the plate, V2 is probably defective. If there is an output at the plate of V2 but not at the output terrninrd, check the resistance of R6 and R7, and rdso check C4 and C7, and make certain that the arm of vibrator Cl is not resting on contact 2.

**Low Output. Low** plate voltage, a defective tube, high bias, a high series resistance, or a leaky shunting capacitor can cause a lower than normal output. Check the plate voltage and bias, if it is normal, tubes V1 and V2 are probably defective. If the plate voltage or bias are abnormal, check the components involved (R4, R5, R9 and R1O). Also check Cl, C2, C3, C4 and C7 to determine whether they are leaky or have changed value. To determine if any of the series resistors have increased in value, measure the resistance of RI, R2, R6, and R7.

**High Output. High plate** voltage, low bias or a lowering of series resistance may produce a higher than normal output voltage. Measure the supply voltage to make certain that the power supply is not at fault, and measure the plate voltage. If the plate voltage is high with normal supply voltage, either plate resistors R4 and R5 or cathode resistors R9 and R10 have changed in value. Also check series resistors R1, R2, R6, and R7 for a change of value if the high output persists. It is most likely that a low output condition will be more often encountered than a high output condition.

Another method of compensating for drift in highgain dc amplifiers is to employ a compensating circuit in which the drift voltage is changed to an ac voltage, is amplified, and is then fed back as a dc voltage to compensate for the original drift voltage change. In other texts, the circuit which converts the dc voltage to an ac voltage is called a *modulator*, and the circuit which converts the ac voltage back to dc voltage is called a *demodulator*. In this sense, the transistor-chopper amplifier corresponds to the modulator. In this handbook, the terms of *modulutor* and *demodulator* are used in the conventional sense, involving the transfer of desired intelligence from one signal to another and the detection or recovery of this signal, respectively.

Prior to the use of the transistor, chopper amplifiers usually employed electromechanical vibrators, photo-sensitive crystals, and in a few instances magnetic amplifiers. Because of the appreciable power required to drive the vibrator, coupled with problems of vibration and shock, and relatively short life (about 1000 hours), the mechanical chopper is considered undesirable when compared with the transistor chopper. The photosensitive devices, likewise, are less desirable because of their complex circuitry as compared with the transistor. While magnetic amplifiers are still in the developmental stage, their large physical size and relatively large power requirements restrict their use. Thus, the transistor-chopper amplifier provides a simple and effective means of converting and amplifying the dc signal.

**Circuit Oparation.** The following schematic shows a typical transistor chopper using the ground'edemitter configuration.



Transistor Choppar (GE)

Self-bias is used with  $R_B$  and the internal baseemitter resistance providing the bias (it acts as a voltage divider connected across the supply). Emitter resistor  $R_E$  serves as an emitter swamping resistor provides thermal compensation. (See the introduction to this section of the handbook for a discussion of bias and bias stabilization.) The collector input, which is the signal from the dc amplifier stage, is direct-coupled, while the chopper (sometimes called "carrier") input may be either direct- or ac-coupled. In either instance, the circuit bias voltage must be arranged so that the direct coupling does not bias off

Q1 in an undesirable mode of operation. Note that the direct-coupled collector input is actually the collector supply voltage. Note also that the ac waveform shown as the dc input signal on the schematic represents the signal component produced by increasing the dc input above the level representing zero to produce a positive waveform, and decreasing the dc level below this zero level to produce the negative waveform. It actually is a dc voltage which varies at the signal frequency.

The operation is such that the transistor acts as a switch, being off when de-energized and on when energized. The switching action is obtained from the chopper input signal, which is a rectangular pulse of constant amplitude (usually in the audio range). On the positive peak, the forward base bias is reduced to a vahre which stops conduction through the transistor. On the negative peak, the forward base bias is increased and the emitter conducts heavily in the saturation region. During the vertical rise and fall times, the bias changes rapidly from one state to the other. It is during this time that the transistor is in its normal operating region, but because of the short duration of the rise and fall time no actual amplification occurs during this period.

Let us consider one cycle of operation. Assume that the transistor is-resting in its quiescent state with a small self-bias and with no inputs applied. Transistor Q1 will draw its quiescent value of collector current. Assume that a 1000-HZ rectangular pulse is applied as the chopper input to the base electrode. With equal on and off times the transistor will conduct heavily during the negative chopper-pulse when the forward bias is increased. Assume that the dc input signal is rdso simultaneously applied to the collector, and that it is positive. This will place a forward bias on the collector (instead of the normal reverse bias), and the transistor will quickly reach a steady saturation current. Note that the dc amplifier input signal is actually acting as the collector supply voltage. At point A on the schematic the input waveform will appear; however, at point B the input voltage is entirely dropped across collector resistor  $\mathbf{R}_{\mathbf{C}}$ , as a result of the heavy conduction, and no output appears. When the chopper input signal goes positive the forward base bias is opposed, and, since the square-wave input is always of greater amplitude than the bias, the base is reverse-biased and collector

current is effectively reduced to zero. It is not exactly zero because a small reverse current,  $I_{ceo}$ , flows through the internal resistance of the base-collector and emitter-base junctions of the transistor. This reverse current produces a voltage drop through collector resistor  $\mathbf{R}_{\mathbf{C}}$  in opposition to normal collector current flow, from points B to A instead of from points A to B. Therefore, the polarity of this reverse-generated voltage is in opposition to the dc input signal, and thus reduces it a small amount. However, for the present we may ignore this small loss of input voltage and say that during the nonconducting period the full amplitude of input voltage appears at the output. During the entire positive excursion of the dc input signal, the output will consist of a series of pulses having approximately the same amplitude as the input signal at the instant the transistor is turned off. When passed through coupling capacitor Ccc, this waveform will look exactly like the input since the dc portion is eliminated and only the varying ac portion appears at the output. As stated previously, this amplitude is slightly less than that of the input because of the reverse drop through R. Therefore, although called a "chopperamplifier," it is clear that the gain is always less than unity and the function is mainly one of converting the dc signal to an ac signal.

Consider now the operation on the opposite halfcycle of the dc input signal. In this instance the collector voltage is rdways negative, which is the normal reverse-biased collector condition. With the same rectangular chopper input signal, the base bias is alternately reduced and aided. In the reduced condition, effective zero collector current is obtained; during the aiding part of the chopper signal, the forward bias is increased. Thus, the same operating conditions prevail, with the transistor alternately driven to saturation (this time by the chopper signal alone) and to effective cutoff. During saturation (the on period) the collector input signal is dropped to zero through the collector resistor, and during effective cutoff (the off period) the signal appears at the output. In this instance, again, there is also a flow of reverse current, which produces a slight opposing voltage so that the input signal is slightly reduced. The output appears as a negative varying voltage which is identical in shape to the input signal. In the collector circuit it consists of a group of pukes with

an amplitude equal to the input signal amplitude (minus the reverse drop) during the off period.

The unique property of the transistor which permits it to operate with either a forward-biased or reverse-biased collector also serves to switch the functions of these elements. Thus, with forward bias the collector becomes an emitter, and the emitter functions as the collector. This allows the designer the choice of either connecting the transistor as a corrunon emitter, or of reversing the collector and emitter connections and have it operate in the inverted fashion. In either case the operation is identical except that the terms *collector* and *emitter* must be **interchanged** in the places they appear in the circuit discussion.

In some applications the emitter resistor is not used since its function is for temperature stabilization by small or incremental changes of emitter current. and the large value of saturation current requires  $R_{\rm E}$ to be a small value to prevent interference with circuit operation. By selecting Class A bias for quiescent operation, the transistor is biased in its midrange of operation, thus permitting the control signal to swing it equally in either direction for cutoff or saturation. This allows the use of a multivibrator type of chopper input signal as the trigger. With some transistors and design, base resistor R<sub>B</sub> is also omitted, with contact bias being supplied by the internal base resistance of the transistor. In any event, the chopper-amplifier is rdways easily recognized because of the dual inputs, with one of them acting as the collector supply.

To be linear in operation, the output signal must be proportional to the input signal. Unfortunately, the transistor is not a perfect switch. When it is closed there is a finite voltage drop across it, and, as stated previously, when it is open there is leakage current through it. The voltage drop across the transistor in the on state is referred to as the "offset voltage", and the leakage current is known as the "offset current". It is evident that either one reduces the amplitude of the input signal and thus affects the input signal by fixing the lowest limit of signal which may be chopped. These voltages and currents can be reduced by proper selection of transistors (silicon types are preferred) and by use of the inverted emittercollector (transposed) connection. With the inverted connection a lower offset voltage is obtained because of the effects of the emitter and collector ohmic

spreading resistances. This becomes a design problem since the reverse collector and emitter currents ( $I_{co}$  and  $I_{eo}$ ) are both dependent upon temperature (they double in *value* for each IOdegree rise in temperature) and upon voltage (the point of occurence varies with the voltage). With good design, the output is practically zero when the transistor is conducting, and it is rdmost equal to the instantaneous value of the input signal when it is non-conducting.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of conventional volt ohmmeters. Be careful also to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a f.dse low-resistance reading.

No output. If there is no chopper input to trigger the circuit, or if base resistor  $R_{\text{B}}$  is open or transistor **Q1** is defective, there will be no output. Check the base resistor for continuity with an ohmetter and the chopper input signa! with an oscilloscope. An open collector resistor or emitter resistor will also interrupt the output, and can be located by making a continuity check. If all components check normal and inputs to the base and emitter (or **collector**) are present, the transistor is defective.

**Reduced Output.** Any increase in resistance in the collector emitter circuit will reduce the amplitude of the output signal. Likewise, a reduction in chopper amplitude can result in insufficient drive for normal operation and produce a partial output. The circuit resistances can be checked with an ohmmeter, and the chopper signal with an oscilloscope. If coupling capacitor CCC is shorted, the output will also be reduced.

**Distorted Output.** A nonlinear output in this circuit is equivalent to distortion in conventional amplifiers. Once the circuit is designed, only a change in the value of the components, input signals, or the transistor can cause distortion. The chopper input signal can be checked on an oscilloscope, and the components can be checked with an ohmmeter. A leaky or shorted coupling capacitor (Ccc) can cause distortion with reduced output, depending upon the voltages existing in the next stage. The capacitor must be

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disconnected to check for leakage, but it can be checked for short-circuit conditions with an ohmmeter. If all components check normal, the transister must be defective.

## PART 5-2. AUDIO AMPLIFIERS

# AUDIO AMPLIFIERS

# General.

The audio amplifier is a circuit arrangement, composed of a tube or tubes and associated components, which is intended to amplify an ac signal whose frequency or composite frequencies fall within the audio range, usually considered to extend from 30 to 15,000 Hz.

This does not mean that all audio amplifiers will amplify all frequencies within this range. Only one particular application-that of the so-called "highfidelity" audio amplifier-is designed to accommodate the entire range, and amplify all frequencies within the range equally well. Amplifiers in many of the other applications are designed to amplify only portions of the audio range. Specifically, any amplifier that amplifies an input signal whose frequency lies between 30 and 15,000 Hz-whether the input signal consists of only one particular frequency or a multitude of frequencies-may be classed as an audio amplifier. This point should be borne in mind, because in some piece of equipment a circuit may be encountered which is referenced as an audio frequency amplifier, but which actually handles no "audio" intelligence in the sense that it is both within the range of audibility and is intelligible to the human ear. For illustration, the frequency-shift system of transmitting teletype information on a radiofrequency channel utilizes an audio frequency amplifier to raise the audio level of two specific frequencies-one for the "mark" and the other for the "space" in a teletype character-before these frequencies are converted to r-f signals for transmission. In this case the audio amplifier is required to amplify only two frequencies, such as 85 Hz and 170 Hz. Additional circuits may be included to actually restrict the response of the amplifier to a narrow range, such as from 30 to 200 Hz, in order to pass only the two frequencies mentioned above. Yet this amplifier is termed an audio amplifier.

# Classifications

Audio amplifiers may be divided into two general classifications: voltage amplifiers and power amplifiers. In each of these divisions there are several circuit configurations, each of which may utilize one or more different types of vacuum tubes: triodes, tetrodes, pentodes, or beam power tubes.

The specific characteristics and circuit operation of several configurations in each division are contained in the seven circuits to follow in this section. A brief discussion covering audio amplifiers in general is given in the following paragraphs.

In a voltage amplifier, the primary consideration is the ratio of the alternating output voltage to the alternating input voltage. This ratio is termed the *gain* of the amplifier. The amount of power which is available in the output circuit is both minute and incidental—the increase in signal voltage is the prime concern. In order to produce the largest possible output signal voltage, which is taken across the load, the impedance of this load must be as large as practicable.

In a power amplifier, the primary consideration is the delivery of a large amount of power to the load.

Since power is equal to voltage times current, generally speaking, a power amplifier must develop a sufficient voltage across its load to cause the required current to flow. The value of the load impedance is an important factor, because it will govern, to a large degree, the amount of current which will flow with a given voltage. The **value** of the load impedance is selected for one of two conditions at a given minimum allowable level of distortion: maximum output circuit efficiency or maximum power output. Output efficiency is the ratio of output power to the dc input power, and it is generally low in an amplifier which is designed for minimum distortion.

The circuit used in both a voltage amplifier and a power amplifier maY be one of several types: resistance-capacitance coupled, impedance coupled, transformer coupled, or direct coupled. Each type has certain advantages and disadvantages, which adapt it to specific applications. A resistance-capacitance audio amplifier is probably the most widely used type, with its components relatively inexpensive and their weight relatively light. Its frequency response can be designed to be uniform over the entire audio range.

An impedance-coupled audio amplifier utilizes an inductor in place of the load resistor used in the conventional resistance-capacitance coupled circuit. A large value of inductance is used, to obtain a maximum amount of **amplification**—**particularly** at the lower audio frequencies. The amplification is not uniform over the audio range because the load

impedance of the inductor varies with frequency, in accordance with the relationship:

$$Z_{L} \sqrt[a]{R^2 + (27r f_{L})^2}$$

where:  $Z_L$  = load impedance (ohms) R = resistance of inductor (ohms)

f = audio frequency (Hz)

L = inductance of inductor (henries)

The amplification is higher than in the resistancecapacitance coupled circuit with the same plate supply voltage, because the relatively low dc resistance of the inductor contributes to a higher voltage at the output.

A direct-coupled audio amplifier has the distinct advantage of distortionless amplification, when the operating voltages are properly adjusted for Class-A operation. Its response is uniform over a wide frequency range, especially at the low frequencies-and even to zero frequency (direct current). Its practically instantaneous response allows an absolute minimum value of phase distortion, making it especially useful in the amplification of square-wave pulses, such as are used in teletype communications. Its chief disadvantages are the complexity of the resistance network that is required to obtain the proper plate and grid voltages for each stage and the tendency toward instability of operation, as well as the successively higher voltages required to operate the second and any succeeding stages.

### Special Transistor Considerations.

The semiconductor type of audio amplifier is similar to its vacuum tube counterpart; however, there are a number of significant differences which must be considered. For example, the electron tube audio amplifier normally operates as a voltage amplifier except for the final output stage, while the transistor audio amplifier operates as a current amplifier in all stages. Thus, the electron tube represents a high-impedance, voltage-sensitive device, while the transistor represents a low-impedance, currentsensitive device.

Since the transistor is basically a low-resistance device, it may draw current from the input source or the preceding stage. (Except in class B audio amplifiers, the drawing of grid current in tube amplifiers represents distortion and is never used. While class C amplifiers do draw grid current in normal operation, they are never used for audio amplification,) In this respect, each transistor amplifier stage may be considered as a current or power amplifier operating at a current or power level higher than that of the preceding stage, but lower than that of the following stage.

While the types of transistor amplifiers are similar to the types of electron tube amplifiers, such as preamplifiers, driver-amplifiers, and output stages, the power levels employed are much lower. Thus, transistor preamplifiers generally operate in the microwatt range, amplifiers and driver stages operate in the low milliwatt range, and output stages operate in the high milliwatt or low watt range. At present, power output of 50 to 100 watts for transistor audio amplifiers are normal, whereas power outputs of 1 to 10 watts were considered high until recently. Therefore, any general statements relating to powers applicable to the following circuits must not be taken too literally, since they will change with the state of the art. Actually, except for extremely high-powered transmitter applications, the transistor audio amplifier today compares very favorably in many respects with the electron tube audio amplifier. The small size and reliability of the transistor, plus its long life and low heat-producing ability make its use popular in equipments normally requiring many stages; in addition, the ability to operate at low voltages makes the transistor particularly useful in portable and mobile equipments operating from battery supplies. In larger equipment, power for transistor operation may be obtained from special low-voltage power supplies employing semiconductor diodes and regulators, thus eliminating the need for batteries.

Transistor amplifiers may be operated class A, B, AB, or C, just as with electron tube amplifiers. When operated class A, they are operated on the linear portion of the collector characteristic. The class A biased transistor has a continuous flow of collector current during the entire cycle, whether a signal is present or not, which corresponds with the action in its electron tube counterpart. They may be operated in this manner, in either single-ended or push-pull circuits. Class B amplifiers can be biased either for collector current cutoff or for zero collector voltage. They are always operated push-pull to avoid serious audio distortion. The best power efficiency is obtained when they are biased for collector current cutoff, since collector current will flow only during that half-cycle of the input voltage that aids the forward

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bias. When biased for zero collector voltage, a heavy current flows when no signal is present, and practically all the collector voltage is dissipated across the load resistor. Although heavy current flows, the power dissipation in the transistor is very low because power is the product of both *current and voltage*, and the voltage is practically zero (due to the small voltage drop across the very low impedance of the transistor). The collector current varies only during that portion of the cycle when the input voltage opposes the forward bias. Under these conditions low efficiency is obtained and the forward current transfer ratio  $(\alpha_{ib})$  is appreciably reduced. The class AB transistor amplifier is biased for either collector voltage cutoff or current cutoff for less than a half-cycle of operation. In this case the efficiency is somewhat greater than that for class A, but less than that for class B, and the statements just made concerning the class B amplifier also apply to the class AB amplifier. Class C amplifiers are biased so that the collector current or voltage is zero for more than a half-cycle; thus, they are not used for audio amplification because of the series audio distortion produced. However, they can be used single-ended or push-pull (or push-push) for r-f applications.

The most important factors to be considered in an **analysis** of audio amplifiers are input and output impedances, signal and noise levels, and required frequency response. Since the transistor is basically a low-level current device it is most important that the input and output impedances be matched to obtain maximum power gain. (In the electron tube circuit this is usually only a problem in the output stage.) The radio of signal-to-noise power at the input to signal-to-noise power at the noise factor

(figure), Fn 
$${}^{s}S_{out}/N_{out}$$
-"

The smaller this ratio  $(F_n)$ , the better the noise quality of the **amplifier**. The noise factor is affected by the operating  $J_{-1}$  at, the signal source resistance, and the frequency of the signal amplified. The accompanying chart shows a typical variation of noise factor with collector voltage and emitter current.



Variation of Noisa with Operating Point



Source Resistance Versus Noise Factor

This figure shows several curves for various values of operating emitter current and collector voltage. As can be seen, the best condition for low noise is operation at emitter currents of less than 1 milliampere and at collector voltages of less than 2 volts. Note that an increase in collector voltage will increase the noise more rapidly than will a similar increase in emitter current. This corresponds to a similar condition in tube amplifiers where high-gain stages are operated at low voltages to reduce noise.

#### **ELECTRONIC CIRCUITS**

The effect of a change in the signal source resistance upon the noise factor is indicated in the following graph, which indicates that best operation is obtained with an input resistance of 100 to 3000 ohms.

The manner in which the noise varies with frequency is indicated in the following graph. For very low frequencies the noise is high, and for higher and higher frequencies it tends to decrease until at about 50 kHz the curve changes direction and noise again starts to increase. In particular, this illustration predicts that low-noise dc amplifiers are difficult to achieve and design.



Noise Variation with Frequency

The necessity for matching input and output circuits for greatest power gain dictates that particular circuit configurations be used. For example, a low input resistance can be obtained by using the common base (CB) circuit for values of 30 to 150 ohms, and the common emitter (CE) circuit for values of 500 to 1500 ohms. Although a high input resistance produces more noise, its use is necessary when a high-impedance device such as a crystal microphone or a transducer is used. Otherwise, a transformer is required for proper matching.

The common collector (CC) circuit, which is similar to a cathode follower in electron tube usage, provides a relatively high input impedance, as shown in the following basic circuit.



**CC** Input Circuit

The high input resistance is produced by the large negative voltage feedback in the base-emitter circuit. As the input voltage rises, the opposing voltage developed across  $\mathbf{R}_{\mathbf{L}}$  substantially reduces the total voltage across the base-emitter junction, and the current drawn from the signal source remains low. A low current produced by a relatively high voltage indicates low resistance (by Ohm's law); thus, if a **500-ohm** resistor is used as  $\mathbf{R}_{\mathbf{L}}$ , the input resistance for a typical transistor will be approximately 20,000 ohms. Unfortunately, however, small current changes in the circuit, caused by functioning of the following stage, produce large variations in the input resistance value; therefore, this type of input circuit is not very desirable.

A better input circuit can be obtained by use of the CE configuration with series resistance, as shown in the following schematic.

In this figure, r represents a typical **base-emitter** resistance of 2000 ohms with a load resistance of 500 ohms. To achieve the 20,000-ohm input resistance of the circuit previously described, an 18,000 ohm series resistor,  $\mathbf{R}_{s}$ , is employed; 18,000 ohms plus the initial 2000 ohms will produce the required value. By use of the series 18,000 ohm resistor the total input resistance can be kept relatively constant at 20,000 ohms, unaffected by variations in transistor parameters or by the current drain of the following stage. The disadvantages of this circuit are a small loss in current

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gain and the large resistance in the base circuit. The use of a large resistance in the base circuit can lead to bias instability if the bias voltage is fed to the transistor via this resistance.



Series CE Input Circuit

The following input circuit represents the best overall compromise.



Degenerative CE Input Circuit

The signal voltage developed across the unby passed emitter resistor,  $\mathbf{R}_{\mathbf{E}}$ , develops a voltage in opposition to the input signal. This degenerative (or negative) feedback voltage causes an increase in the input resistance. When a 500-ohm load resistor,  $\mathbf{R}_{\mathrm{L}}$ , is used with a 500-ohm emitter resistor,  $\mathbf{R}_{\mathrm{E}}$ , the total input resistance is approximately 20,000 ohms for a typical transistor. In addition, the emitter resistor acts as a swamping resistor, to help stabilize the transistor and minimize thermal variation effects.

Because the common-emitter configuration provides thermal stability (by means of emitter swamping), a relatively high input resistance, and high voltage-and-current gain, it is usually employed to the exclusion of other configurations. Therefore, the circuits to be discussed in later paragraphs will use the common-emitter configuration; the other forms of these circuits will not be mentioned unless considered pertinent to the discussion.

The transistor audio amplifier is usually classified as a *small-signal* amplifier or a *large-signal* amplifier. Actually, the small-signal condition represents excursions of the input signal over only a small range about the operating point (bias level), on the order of fractions of a volt. Small-signal conditions are normally calculated by appropriate formulae, since the values remain relatively linear or mathematically constant over the small range involved. On the other hand, with large-signal conditions, which are associated with the power amplifier (or output stage), there may be considerable departure from the formula for large values; thus, the power amplifier must be analyzed and designed graphically. In this respect, the transistor is somewhat different from the electron tube, with inherent nonlinearities which vary considerably from unit to unit. As a result, matched parts of transistors are used to produce the desired results where the individual parameter variation is too large.

# R-C COUPLED TRIODE AUDIO AMPLIFIER (ELECTRON TUBE)

## Application.

The R-C coupled triode audio voltage amplifier is used to increase the amplitude of an audio-frequency signal voltage when uniform gain is required over the entire audio spectrum and when a medium value of gain (between 5 and 70) is required. It is generally used to amplify low-level signal inputs, such as those generated by an audio oscillator circuit or by a microphone, vibration pickup, or magnetic tape pickup. It commonly appears in the audio section of communications receivers and transmitters, in sonar equipment, and in applications which utilize signal frequencies in the audio-frequency range instead of aural intelligence.

#### Characteristics.

Input is normally an audio-frequency signal of extremely small amplitude.

Input impedance is normally very high, ranging from several thousand ohms to several megohms.

Output impedance is usually high, ranging from several thousand ohms to approximately half a megohm.

Voltage gain ranges from 5 to 70, depending upon the application and circuit design.

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Operates Class A; no grid current flows under any conditions.

Frequency response is linear over the range of audio frequency for which the amplifier is designed. This may include the entire audio range, or may be restricted to a portion of it, depending upon the intended application of the amplifier.

Output (plate) signal and input (grid) signal are of opposite polarity.

Cathode bias (self-bias) is normally used; fixed bias may be used in some applications.

# **Circuit Analysis.**

**General.** The **R-C** coupled triode voltage amplifier circuit is one of the most widely used circuits in audio-frequency amplification. It has the advantages of being the least expensive, having the lightest weight components, having good fidelity over a wide frequency range, and being relatively free from undesirable currents induced by stray fields and ac heater wiring. Probably its only disadvantage is the higher plate supply voltage as compared to that of a transformer-coupled or impedance-coupled circuit; the higher voltage is required to compensate for the voltage drop across the plate load resistor.

Circuit Operation. The R-C coupled triode audio voltage amplifier is used to amplify and reproduce, without distortion, input siganal voltages of audio frequency which are applied to the grid of the triode tube. The circuit of a typical amplifier of this type is shown in the following illustration. In this circuit the input signal is applied to the grid of triode VI through coupling capacitor Cl. The grid is returned to ground through grid resistor R1. Cathode bias is furnished by means of cathode resistor R2, which is bypassed by capacitor C2 to maintain the bias at a constant average value and thus prevent degeneration. Plate voltage is furnished from the plate power supply, Ebb through plate load resistor R3. In some circuits, especially where several stages of amplification are utilized, an additional resistor may be used, connected in series between the plate load resistor and Ebb, with a capacitor connected from the junction of the two resistors to ground, to form a decoupling circuit. This addition prevents the possibility of audio feedback (and its result-oscillation) from an output stage or one operated at a high audio level, back to an input or low-level stage through the power supply, Ebb, which could act as a means of common coupling.



Typical R-C Coupled Triode Audio Voltage Amplifier Circuit

In order to obtain a high value of audio output voltage (a high signal voltage), the resistance value of the plate load resistor should be as high as possible. But this requirement imposes an additional one, because an increase in the resistance of the plate load will cause an increase in the voltage drop across it, resulting in a decrease in the actual voltage at the plate of the triode. In order to obtain the required effective plate voltage, with an increased resistance of the plate load, and only solution is to increase the plate supply voltage, Ebb. However, there is a practical limit to the amount by which the plate voltage may be increased. The maximum voltage obtainable from the plate power supply and the voltage rating of the bypass capacitors in the plate supply circuit both serve to establish this limit.

A frequency response curve for a typical **R-C** coupled triode audio voltage amplifier is shown in the following illustration. It may be seen, from the illustration, that the amplification decreases at both high and low frequencies. As the frequency increases toward the high end of the response curve, amplification falls off because of the shunting effect of the combination of output capacitance of the stage, the distributed capacitance of the coupling network, and the input capacitance of the following stage. These all act to shunt the higher frequencies to ground. As the frequency decreases toward the low end of the response curve, the amplification also falls off. In this case the reduced gain is caused by the increase in

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reactance of the coupling capacitor as the frequency decreases, and is also caused by the increase in reactance of the cathode bypass capacitor, which introduces degeneration at the lower frequencies.



# Frequency Response of an R-C Coupled Triode Audio Voltage Amplifier With Various Values of Plate Load Resistance

An R-C coupled triode audio voltage amplifier can be designed to give a good frequency response for almost any range of audio frequencies. For instance, an amplifier can be built to give uniform amplification for audio frequencies from 100 to 20,000 Hz. By changing the values of the coupling capacitor and the load resistor, the frequency range can be extended to cover the very wide frequency range of the video amplifier. However, this extended range may be obtained only at the cost of reduced amplification, or gain, over the entire range. This may be observed by referring to the previous illustration; it will be seen that the output response is relatively flat from approximately 100 Hz to well over 10,000 Hz when the value of the load resistor,  $R_1$  is 0.02 megohrn, but the over-all gain is relatively low compared to that obtained using higher values of plate load resistance. Thus, the R-C coupled triode audio voltage amplifier may be made to give a good frequency response over the entire audio range, at medium values of amplification.

# Failure Analysis.

No Output. A no-output condition in an R-C coupled triode audio voltage amplifier may be caused by any one of several defects. First, the presence of an input signal at the input to the amplifier should be verified. The triode tube should be checked to insure that it is capable of operation. The presence of plate voltage at the plate of the triode should be checked; if no voltage or a very low voltage is present, a defective plate load resistor or a defective plate power supply is indicated. If the voltage at the cathode is very high-approximately equal to the plate supply voltage, Ebb-an open cathode resistor may be the cause of no output, assuming that the plate load resistor and the triode have been both found in an operable condition. Finally, an open input coupling capacitor may be the cause of a no-output condition.

Reduced or Unstable Output. Reduced or unstable output from an R-C coupled triode audio voltage amplifier may be due to an aging tube having poor cathode emission, a reduced value of plate voltage due to a defective plate power supply, or an input signal of insufficient amplitude. An open grid resistor would cause severe distortion, greatly reduced output, and possibly intermittent operation due to "grid blocking". If the input coupling capacitor were leaky, distortion would be present in the output signal as a result of the presence of a positive value of voltage at the grid, from the plate of the previous stage supplying the input signal. A reduced value of output, without distortion, may be caused by an open cathode bypass capacitor, which would introduce degeneration in to the circuit. An excessive value of bias, caused by too high a value of cathode resistance (or too high a value of bias voltage if a fixed bias is applied), would also be responsible for an output signal of reduced value.

# R-C COUPLED AUDIO AMPLIFIER (SEMICONDUCTOR)

### Application.

The r-c-coupled transistor **audio amplifier** is commonly used where good fidelity over a large range of audio frequencies is desired. For example, it is used in the amplifier stages of receivers and communications equipment where little or no power output is required.

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#### Characteristics.

Uses **common-emitter** circuit for high gain and better impedance matching.

Operates Class A for linear operation and minimum distortion.

Usually amplifies small signals, but can be designed to handle large signals in cascaded stages.

Is usually fixed-biased from the collector supply, but may be self-biased in some applications.

Emitter swamping is normally used for themal stabilization.

Gain is fairly uniform over a range of approximately 100 to 20,000 Hz or more.

Both voltage gain and power gain are high.

## Circuit Analysis.

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**General.** The r-c-coupled transistor amplifier is similar in general to the r-c-coupled electron tube amplifier previously discussed in this section of the handbook. Use of the common (oI grounded) -emitter circuit, permits the analogy that the base is equivalent to the vacuum tube grid, the emitter is equivalent to the tube cathode, and the collector is equivalent to the tube plate. Thus, it is clear from the following schematic that the two r-c-coupled circuits are practically identical. Any differences are due to the internal parameters of the transistor and the matching requirements for maximum output with minimum distortion.

**Circuit Operation.** The following schematic shows a conventional PNP, triode, common-emitter r-ccoupled transistor audio amplifier circuit.



**R-C-Coupled Audio Amplifier** 

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The input is **shown** capacitively coupled, and voltage divider R1,  $\mathbf{R}_{\mathbf{B}}$  provides fixed bias from the collector supply. Emitter swamping is provided by  $\mathbf{R}_{\mathbf{E}}$  for temperature stabilization;  $\mathbf{E}_{\mathbf{E}}$  is bypassed by  $\mathbf{C}_{\mathbf{E}}$ . (See the introduction to this section of the handbook for a discussion of bias arrangements, and bias stabilization methods.) Collector resistor  $\mathbf{R}_{c}$  is the load across which the output voltage is developed; this voltage is applied through coupling capacitor CCC to the output circuit. Resistor R2 is the base-to-ground resistor in the next stage when cascaded amplifiers are used, or is the output load resistor (such as a headset) in single-ended stages.

Normally, the amplifier is a small-signal amplifier, with the bias fixed at the center of the transistor dynamic transfer characteristic. With no input signal a steady collector current, I<sub>c</sub>, flows as determined by the base bias voltage. With RI and R<sub>B</sub> connected across the collector supply as a voltage divider, a forward (negative) bias is developed across  $R_{\mu}$ ; this bias is sufficient to cause the quiescent value of I<sub>c</sub> to flow, even through the collector is reverse-biased. When the input signal goes positive, assuming a sinewave input, the forward base bias is decreased instantaneously by the amplitude of the input signal, and collector current I is reduced. The reduction in collector current causes the voltage across collector resistor  $\mathbf{R}_{\mathbf{C}}$  to rise toward the supply voltage, which is negative (this is exactly the reverse of vacuum-tube action); thus, a negative-swinging output signal is developed. When the input signal becomes negative, it adds to the forward base bias and causes I to increase. The increase in collector current through  $\mathbf{R}_{\mathbf{C}}$ produces a less negative voltage or positive swing. Therefore, the collector output follows the input signal except that it is reversed in polarity; when the input signal is positive, the output signal is negative, and vice versa. The collector output is developed across  $\mathbf{R}_{\mathbf{C}}$  between the collector and ground, and is applied through coupling capacitor CCC to the base of the next stage, or to the output load.

[n cascaded resistance-coupled stages the base bias resistor and base-to-emitter internal impedance of the next stage transistor offer a shunt path between coupling capacitor CCC and ground. Therefore, the reactance of CCC and the total parallel resistance from base to ground form a voltage divider across the collector resistor of the first stage. If the reactance of the coupling capacitor is large, the output voltage is greatly attenuated, and only a small output appears

between base and ground of the second stage. Since the reactance of CCC varies inversely with frequency, the lower audio frequencies are attenuated more than the higher frequencies. For good low-frequency response the coupling capacitor is made sufficiently large in value that its reactance is very small as compared with the base-to-ground resistance. This is similar to vacuum-tube practice, where relatively small coupling capacitors (such as .001 microfarad) are satisfactory, because the vacuum-tube grid-toground impedance is very high. Because the transistor base-to-erni.tter impedance is fairly low (about 500 ohms), a coupling capacitor of 50 microfarads or more is needed to achieve the low impedance required to pass the signal without excessive attenuation. (A 50-microfarad capacitor has a capacitive reactance of approximately 30 ohms at 100 Hz.) For good low-frequency response the reactance of the coupling capacitor should always be less than onetenth the effective base input impedance.

At the higher audio frequencies (above 20,000 Hz), the collector-to-emitter capacitance of the first stage and the base-to+ mitter shunting capacitance of the second stage tend to bypass the high frequencies to ground, causing a drop in the response. This frequency-attenuating action of the transistor occurs because the width of the internal transistor PN junctions are voltage-sensitive. With higher voltages the transition region is narrow, corresponding to the closely spaced plates of a capacitor with the associated high capacitance. The reverse bias on the collector also reduces the width of this transition region, so that transistors are generally characterized by a high inter-electrode capacitance. For example, an audio transistor may have a collector-to-base capacitance on the order of 50 picofarads, as compared with a vacuum-tube plate-to-grid capacitance of one or more picofarads. The collector-to-emitter capacitance is usually 5 to 10 times the value of the collector-to-base capacitance (in the commonanitter circuit), as compared with 8 picofarads or less for vacuum-tube plate-to-cathode capacitance. Thus, it can be seen how the high-frequency response is affected considerably by internal transistor parameters. Of course, any shunt wiring capacitance will also add to the shunting effects of the transistor. Both lowand high-frequency compensating circuits may be used to increase the effective frequency response of the circuit, as discussed in Wideband Video Amplifier Circuits later in this section.

Over the region of 100 to 20,000 Hz, the r-ccoupled amplifier has a relatively flat response, and with proper matching will afford high power and voltage gains. Hence, this form of coupling is universally employed where good audio response is required without any appreciable power output (voltage amplification). The common-base configuration is sometimes employed where better high-frequency response is desired than that provided by the common-emitter circuit, since the **collector-to-base** capacitance is only I/5th to 1/10 as great.

Transistor audio amplifiers are also characterized by a high inherent noise which is greatest at the lower audio frequencies. Operation with low values of emitter current and low collector voltages, together with low values of input resistance, tends to minimize the noise. In the common-emitter circuit, degenerative effects produced by an unbypassed emitter resistor tend to increase the input resistance. Thus, it is conventional practice to use large emitter bypass capacitors in the r-c-coupled circuit to avoid any possibility of degeneration. As with the electron tube, external feedback circuits provide better response, although emitter degeneration may sometimes be used. Since freed bias from the collector supply may be easily obtained by a simple voltage divider, it is used in both large-and small-signal applications. Selfbias is generally restricted in used to very small-signal amplifiers; otherwise, distortion and improper operation with a reduction in gain, or blocking, may occur on large signals. In the r-c-coupled amplifier, the emitter resistor functions mainly as a swamping resistor for temperature stabilization, and prevents large changes in amplification with temperature variations.

In considering the operation of the transistor r-c-coupled amplifier as compared with the electrontube r-c-coupled amplifier, it should be clear from the above discussion that one circuit is an almost exact counterpart (dual) of the other. The difference is that transistor stages operate with low input and output impedances, at low voltages, and at very low levels of amplification, whereas electron-tube stages operate with relatively high input and output impedances, at high voltages, and at high levels of amplification. Thus, the transistor is basically a current amplifier, while the electron tube is a-voltage amplifier. Consequently, the transistor requires closer matching (rather than mismatching) of impedances to produce maximum performance.

#### Failure Analysis.

**General. When** making voltage checks use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition may be caused by an open or short circuit, by improper bias or loss of collector voltage, or by a defective transistor. A voltage check will determine whether the bias and collector voltage are normal; also, a VTVM will indicate audio input and output voltages. With the few components involved, simple voltage and resistance checks will usually indicate the source of trouble. If the bias voltage divider is open because return resistor R<sub>B</sub> is d ef ec t ive, the transistor will conduct heavily in the saturat ion r eg ion. With R open. only contact bias exists and the trans istor will be cut off . If collector resistor  $R_{\rm C}$  is open, there will be no voltage indication as measured between between the collector and ground. If emitter resistor R<sub>E</sub> is open, the circuit will not operate; however, if emitter bypass capacitor  $C_F$  is shorted, the circuit will operate but it will be temperature-sensitive. Likewise, if the emitter bypass capacitor is open, it may reduce the output because of degenerative feedback, but normally will not cause complete stoppage of operation. If the input coupling capacitor or the output capacitor is open, no output will result. Check the input and output circuits with an oscilloscope; disappearance of the signal will indicate the location of the defective component. If the coupling capacitor is shorted or leaky, it will affect the base bias if located at the input, but will probably not be sufficient to stop operation. On the other hand, if the output capacitor is at fault, the collector reverse bias (which is normally high as compared with the base bias) will be applied as full forward bias to the base of the next stage and will bias it heavily into saturation; thus, no output will result, and the current may be sufficient to destroy the transistor. If the coupling capacitor is leaky, the effect will depend upon the amount of leakage. With slight leakage there may be practically no observable effect, or possibly distortion; with heavy leakage there will probably be no output. Of course, if the transistor is shorted or otherwise defective, a no-output condition will occur.

A rough check of transistor operation can be made (if the transistor can be easily removed from the circuit) by measuring the forward and reverse resistance with an ohmmeter. A high reverse resistance and low forward resistance indicates that the transistor is operable, but does not indicate if the gain is normal. Be certain to observe the correct polarities.

Reduced Output. Improper bias voltage or a change in the value of a component, as well as a defective transistor can cause reduced output. If the transistor gain is low, the output will also be low. If either of the base voltage-divider bias resistors changes in value, the bias will be either too low or too high and the output will be reduced, with accompanying distorion. A simple voltmeter check will determine whether the bias is correct. If the collector resistor is too high in value, the output will be increased because of the extra voltage drop across the resistor; if the resistor is too low, in value, the output will be decreased. If the coupling capacitors are defective, a loss of output at the low-frequency end of the spectrum will result when the coupling capacitance is less than the design value. A leaky capacitor will likewise cause improper bias voltages and reduced output. Capacitors usually must have one end disconnected from the circuit before they can be tested by means of a standard capacitance analyzer (in-circuit capacitance checkers do not require this).

Distorted Output. If the base bias is too high (reduced forward bias), the transistor will operate on the lower portion of its dynamic characteristic, and the negative input peaks will be clipped (positive collector swings). Likewise, if the bias is too low (increased forward bias), the transistor will conduct heavily and operate on the upper portion of its dynamic characteristic, with corresponding clipping of the positive peaks (negative collector swings). In both cases extreme distortion will be caused. If the bias is proper but the collector voltage is not, similar effects may be caused. If the collector voltage is too high, the negative collector swing will be clipped, and if too low the positive collector swing will be clipped; in either instance heavy distortion will result. An open emitter bypass capacitor will permit degenerative feedback to occur, and, depending upon the amount, will shown either as distortion or as reduced output. A change in load resistance produced by a defective collector or load resistor or by a leaky coupling capacitor (causing a heavy shunting of the

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output load) usually shows as a distorted output with reduced volume because of the mismatching. Use an oscilloscope to follow the signal through the circuit and determine the point at which the waveform departs from normal. In most instances the defective component will then be apparent. Do not overlook the possibility that distortion may be occurring in a previous stage, merely being amplified by the stage under suspicion. Too large an input (overdrive) will cause both positive and negative peak clipping with distortion, just as in an electron-tube amplifier. Apply a square-wave input from a signal generator and observe the output on an oscilloscope. Frequency distortion will be shown by a sloping rise and fall time (poor high-frequency response); a sloping flat top indicates poor low-frequency response. Electrontube techniques for locating distortion may generally be used for transistor trouble shooting if the proper voltages and polarities are employed.

## **R-C COUPLED PENTODE AUDIO AMPLIFIER**

#### Application.

The R-C coupled pentode audio voltage amplifier is used to increase the amplitude of an audiofrequency signal voltage when uniform gain is required over the entire audio spectrum and when a high value of gain (up to approximately 350) is required. It is used to amplify extremely low-level signals, where a high gain per stage is required and the number of stages which can be accommodated is limited.

#### Characteristics.

Same characteristics as electron tube R-C coupled triode audio amplifier, with following exceptions:

Input impedance is very high, usually greater than 0.1 megohm.

Output impedance is high, and as a rule is considerably higher than that of a triode amplifier.

Voltage gain is much higher than that of a triode ampfier, ranging from 100 to 350.

Operates Class A; no grid current flows under any conditions.

Harmonic distortion in the output signal is lower, for the same value of output voltage, than that of a triode amplifier. **Circuit Analysis.** 

General. The R-C coupled pentode audio voltage amplifier is widely used as the input stage in a high-gain amplifier assembly, where the value of the signal input voltage is extremely low. Because its input impedance is high, it can accommodate inputs from various high-impedance, sources by direct connection, without the necessity of impedancematching transformers to effect the connection. Such sources include crystal and high-impedance dynamic microphones, crystal vibration pickups (including phonograph pickups), and magnetic tape heads. The gain per stage of a pentode amplifier is much higher than that of a triode, and the pentode amplifier produces an output signal voltage of considerably greater amplitude than that of a triode when operated at the same plate supply voltage, Ebb. The total harmonic distortion contained in the output of a pentode audio amplifier is less than that of a triode audio amplifier for a given value of output (signal) voltage.

Circuit Operation. The R-C coupled pentode audio voltage amplifier is used to amplify, to high value, an input signal within the audio-frequency range, and reproduce the original waveform without appreciable distortion. The circuit of a typical amplifier of this type is shown in the following illustration. In this circuit the input signal is applied through coupling capacitor Cl to the grid of the pentode, V1. The grid is returned to ground through grid resistor R1. The pentode is operated with self-bias, with the bias being supplied by means of cathode resistor R2; the resistor is bypassed by capacitor C2 to maintain the bias at a constant average value, thereby avoiding degeneration of the amplified signal. Plate and screen voltages are supplied from the plate power supply,  $E_{bb}$ , through decoupling resistor R5 bypassed by capacitor C4, with R3 serving as the screen dropping resistor bypassed by capacitor C3 and with R4 serving as the plate load resistor. The decoupling circuit, composed of R5 and C4, serves to prevent feedback at an audio rate from the output (plate) of V1, back through the low impedance of the power supply to the plate of the previous tube, which furnishes the input signal to the grid of VI.

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Typical R-C Coupled Pentode Audio Voltage Amplifier Circuit

An example of the use of this circuit is its application as a servo preamplifier. With a type 5840 pentode used for VI, a **plate** voltage supply  $E_{bb}$  of 250 volts dc, and an input signal of 400 Hz, the circuit affords a voltage amplification of 70 when the following component values are used: RI, 1 megohm; R2, 3.3K; R3, 1.5 megohm; R4, 470K; R5, 220K; Cl, 0.01 $\mu$ f; C2, 30 $\mu$ f; C3, 0.1 $\mu$ f; and C4, 16 $\mu$ f.

The pentode tube used in the R-C coupled pentode audio voltage amplifier has a much higher plate resistance than a triode tube; because of this fact, the resistance value of the plate load resistor has a considerable influence on the amplification of the higher frequencies, especially at the upper frequency limit of the design bandpass. At the lower frequency limit, however, the output coupling capacitor to the following stage may have a somewhat lower capacitance value than in a comparable triode amplifier circuit, and still maintain the same low-frequency response. The effect of the value of the plate load resistor upon the frequency response, or bandpass, of the amplifier may be generalized: with a plate load of lOOK, the high-frequency limit is approximately 25,000 Hz, while a plate load of 500K gives a highfrequency cutoff in the neighborhood of 5000 Hz.

Since 25,000 Hz is far beyond the normal response range of an audio-frequency amplifier, a more realistic high-frequency limit of 10,000 Hz may be obtained by using a plate load resistance of 250K.

From the above discussion it appears that, as the plate load resistance is made lower and lower, the high-frequency cutoff limit becomes higher and higher, and that it would therefore be advantageous in any case to use a low value of plate load resistance. While this is true, a low value of plate load resistance has probably a greater disadvantage: the output signal will have a low amplitude. Therefore, in order to obtain sufficient output signal voltage (amplitude), the value of the plate load resistance must be a compromise between output voltage versus highfrequency response.

In connection with the use of a pentode as a voltage amplifier, the equation  $I_{load} = e_g g_m$  is often used. This expression, along with an equivalent circuit, can be derived from the equation for output voltage, e.:

$$\mu_o = \mu e_{\overline{g}} \frac{R_1}{r_p + R_L}$$

By substituting for  $\mu$  the relationship  $\mu = r_p g_m$ , we have:

$$e_o = e_g g_m (r_p \frac{R_L}{R_L})$$

The terms in parentheses will be recognized as the total resistance of a parallel circuit of  $\mathbf{r_p}$  and  $\mathbf{R_L}$ . Hence, the expression suggests the following equivalent circuit. As long as the load is purely resistive, this circuit gives exactly the same results as the original equivalent circuit. If the load is reactive, however, an error is introduced in calculations of phase shift unless the plate resistance  $\mathbf{r_p}$  is large compared to  $\mathbf{R_L}$  (with Pentode tubes  $\mathbf{r_p}$  is o fen very large compared to  $\mathbf{R_L}$ ). When this is true the parallel branch  $\mathbf{r_p}$  can be neglected, and the load current is equal to  $\neg \mathbf{e_g} \mathbf{g_m}$ . This speeds up calculations and is especially useful for pentode tubes when their values of  $\mathbf{r_p}$  and  $\boldsymbol{\mu}$  are not accurately known.

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Equivalent Circuit of a Pentode Voltage Amplifier

## Failure Analysis.

No Output. If an R-C coupled pentode audio voltage amplifier is defective in that no output is produced, the input signal source should first be checked to see that a signal of proper amplitude is present at the input terminals of the amplifier. The pentode tube should also be checked to insure that it is capable of operation. Plate and screen voltages at the tube socket terminals should then be measured, to determine whether the voltages are of the proper value. If no voltage is present at either the plate or the screen, the plate voltage power supply  $(E_{bb})$  may be defective in that no output is being furnished. Another possible cause may be an open decoupling resistor R5, a shorted capacitor C4, or an open cathode resistor R2. If plate voltage is present but screen voltage is not, screen dropping resistor R3 may be opencircuited or screen bypass capacitor C3 may be shorted. On the other hand, if screen voltage is present without plate voltage, an open plate load resistor R4 is indicated. If, however, both plate and screen voltages are normal and no output is obtained, an open input coupling capacitor Cl could be the cause of the trouble.

**Reduced or Unstable Output.** If the R-C coupled pentode audio voltage amplifier is defective in that a reduced value of output or instability is evident, the input signal should be checked to see that it is of sufficient amplitude, yet not of excessive amplitude that would overload the amplifier stage. If the input signal is present and has normal amplitude, the trouble may be due to a leaky coupling capacitor C 1, which might allow a positive voltage from the preceding step to be impressed on the grid of V1 thereby

introducing distoring. An open or extremely high resistance grid resistor R1 would tend to cause intermittent operation ("motorboating"); if this condition prevails, the grid resistor should be replaced. A reduced value of output could also be caused by an open cathode bypass capacitor C2 or by an open screen bypass capacitor C3, either of which would cause the circuit to be degenerative. Another cause of low output could be an open screen resistor R3, which would make the tube attempt to operate with plate voltage but without screen voltage. A decreased value of screen voltage, due to a leaky screen bypass capacitor C3, could cause low output. A decreased value of plate and screen voltage, due to a defective power supply Ebb, could likewise be responsible for low output. Finally, there is a remote possibility that low heater (filament) voltage, brought about by a loose connection or an overloaded circuit, maybe the cause of a low value of output.

# IMPEDANCE-COUPLED AUDIO AMPLIFIER (ELECTRON TUBE)

## Application.

The impedance-coupled triode audio voltage amplitier is used to increase the amplitude of an audio-frequency signal where wideband response is not desired, and higher gain than that of the wideband amplifier is desired.

#### Characteristics.

Frequency response is linear over a small band of frequencies, for example from 200 to 10,000 Hz, depending upon the design.

Input is normally an a-f signal of small amplitude. Input impedance is high, usually more than 50,000 ohms.

Output impedance is high (on the same order as the input), and is suitable for cascaded stages or magnetic output devices requiring little power.

Output signal is inverted in polarity from that of the input signal.

Operates class A biased; no grid current flows under normal conditions.

Cathode (self) bias is normally used, but fixed bias may be used in certain applications.

Requires less plate voltage than that of an equivalent R-C-coupled amplifier to produce an equivalent

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output. In this respect it is similar to the transformer-coupled amplifier.

# **Circuit Analysis.**

**General. The impedance-coupled** triode audio voltage amplifier resembles an R-C-coupled audio amplifier (previously discussed), except that an iron-core inductance (choke), instead of a resistor, is used as the plate load. It is sometimes referred to as a choke-coupled amplifier. Because the choke acts as a reactance at ac frequencies, the impedance determines the drop across the plate load. However, since the dc resistance of the choke coil is low, only a small dc voltage drop occurs across the choke. As a result, a much lower plate supply voltage can be used to provide the same effective plate voltage (as compared with an R-C amplifier).

**Circuit Operation. The schematic** of a typical impedance-coupled triode audio voltage amplifier is shown in the following illustration.





As can be seen, the input signal is capacitively coupled through Cl to the grid of tube V 1. Coupling capacitor C 1 and grid resistor RI form an audio voltage divider. The output of this voltage divider is the voltage which appears across R1, and is the

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signal voltage applied to the grid of VI. Capacitor Cl also acts as a dc blocking capacitor to prevent the plate voltage of a preceding stage or any dc voltage existing in the input circuit trom adversely biasing VI. The reactance of Cl to an audio-frequency signal is much smaller than RI; thus little signal is lost across the capacitor. Resistor R2 provides cathode bias through average plate current flow, and capacitor C2 bypasses the resistor to prevent degenerative effect. Choke coil L1 is the plate load impedance across which the output voltage,  $\mathbf{e_0}$  is developed; L1, C3, and Rg form the impedance-coupling network.

With no signal applied, static plate current flows through cathode bias resistor R2, and provides class A bias. A plate voltage drop across choke coil L1 is produced by the dc coil resistance. This drop is constant, regardless of whether a signal is present; thus it produces no output voltage since it cannot pass through coupling capacitor C3. When a positive-going input signal is applied to the grid of tube VI, it reduces the effective grid bias, and the plate current increases instantaneously. Assuming a sine-wave input, as the signal raises, the plate current also increases until the positive peak of the input cycle is reached. During this half of the cycle (from point a to point b on the output waveform), a continuously increasing voltage drop (negative swing) occurs across the load produced by the reactance of L1. This is the audio output voltage which is applied to coupling capacitor C3. With a positive-going input, a negativegoing output is developed by the increasing plate current, which drops the voltage across the impedance offered by choke L1. When the grid voltage reaches the positive crest, the plate voltage is at a minimum value (point b on the output waveform). As the grid voltage recedes, plate current decreases. Consequently, the voltage drop across Ll becomes less and less, reaching zero (point c on the waveform) at the completion of the positive half-cycle of the input signal.

As the input signal now swings negative, it adds to the applied bias produced by normal plate current flow, and reduces the plate current instantaneously. During the negative-going half-cycle of input signal, the plate current continuously decreases (point c to point d) until the negative crest is reached at point d on the input waveform. During this portion of the half-cycle, the plate voltage rises toward the source voltage and produces the positive-going portion of the output signal. At the negative crest (point d on the input waveform), the input signal is equal to the bias, but cutoff is not reached because the initrd bias is less than half of the cutoff value to insure that the tube is operated over the linear portion of its grid-voltage plate-current characteristic curve. At this time the plate voltage is equal to the source voltage less the small dc drop in the plate choke. As the negative input signal swings positive and returns to the zero level, the plate current continuously increases (since the effective grid bias is reduced), and the voltage drop produces across L1 increase. Plate voltage decreases from the maximum value to the static level (point d to e on the output waveform).

Since the input signal can never exceed the bias voltage without producing distortion by driving the grid positive, it can be seen that the peak input voltage is only on the order of a few volts or less. On the other hand, the plate swing is over a range of 100 to 200 volts, depending upon tube characteristics, supply voltages available, and bias values. Since the plate voltage swing is actually the output voltage which is applied to the coupling capacitor, it is easy to understand how a voltage gain from input to output of 100 or greater can be obtained. Because the output voltage reaches a negative peak when the input voltage reaches a positive peak, and vice versa, at any particular instant of time they are considered to be 180 degrees out of phase with each other. Actually, they are of opposite polarity and of the same phase because the current and voltage are both in phase (at extremely low frequencies there may be an actual phase shift). Since only a voltage output is desired, it is unnecessary to match the load impedance to the tube impedance. In fact, exactly the opposite approach is used; the load impedance is always selected to be much larger than the plate resistance (for a triode) so that the greatest output voltage is obtained. Because both positive and negative plate current swings are identical, assuming a sine-wave input, the average current remains the same and is not affected by the input signal. Therefore, the cathode current can be used to provide a steady selfbias (fixed bias may be used if desired).

For ease of discussion, the frequency spectrum over which the **impedance-coupled** amplifier operates can be divided into three convenient ranges: low-, middle- and high-frequency. The gain drops off at the low frequencies because the impedance of the choke coil becomes less as the frequency is reduced. To increase the low-frequency response, a large number

of turns are used to provide a greater inductance. However, the distributed capacitance produced by a coil winding of many turns creates a large shunting capacitive reactance, which causes a drop in the highfrequency response. Over the middle-frequency range the gain in more uniform. It is limited only by the parallel combination of tube plate resistance, plate choke-coil impedance, and the shunting effect of the input resistance (grid resistor) of the following stage. Generally speaking, the plate choke-coil-impedance over the middle-frequency range is very high as compared with either the tube plate resistance or the input resistance of the next stage; thus maximum gain is obtained. The gain of the impedance-coupled amplifier drops over the high-frequency range mainly because of the large distributed capacitance of the choke-coil turns, which effectively shunts the load to ground and offers a low-impedance path to high frequencies.

## Failura Analysis.

No Output. A no-output condition could be caused by no input signal, an open-circuited condition, lack of plate or fdament voltage, a shortcircuited condition, or defective tube. The presence or absence of an input signal can be determined by making an oscilloscope or vacuum-tube voltmeter check at the input. An open-circuited or shortcircuited condition can be localized to the defective portion of the circuit by making voltage measurements with a high-resistance voltmeter to determine whether the proper filament, cathode or grid, and plate voltages exist. In many instances open filaments can easily be located by observing that the fdament does not light and that the tube feels cold to the touch. Where improper or no voltage exists, check the power supply voltage to determine whether the fault is in the amplifier or in the power supply. If there is normal voltage at the output of the power supply, the trouble is in the amplifier. Lack of plate voltage then indicates a defective plate choke, LI. If the choke is open, there will be no voltage between the plate and ground. If it is shorted, there will be no voltage drop across the choke. If there is a short between the plate and ground, the power supply voltage will be dropped entirely across the choke. Removing the tube will clear the short if the tube is defective; otherwise, it can be assumed that the choke insulation has failed and that there is a dc path through the core to ground. A short-circuit condition is usually indicated

by burning or charring of the parts involved, and sometimes can be easily located by a visual examination. If such an examination does not reveal the trouble, it will be necessary to remove the power, discharge the B+ supply, and then remove the part and make a resistance check on it. A short-circuited condition is indicated by a low resistance **hetween** points that normally have a higher resistance.

No output can also be caused by an open coupling (input) capacitor, Cl. If the signal is present on the input side (as observed on an oscilloscope) but not on the grid side, either the capacitor is open or the grid side is shorted to ground. Use an in-circuit capacitance tester to determine whether the capacitor is defective. If the trouble is not revealed by this test, it will be necessary to disconnect the capacitor from the circuit and check it with a standard type of capacitance bridge. Output coupling capacitor C3 can also cause a no-output indication if it is open; check it in a similar manner, considering the plate side as the input side and the side connected to  $\mathbf{R}_{\mathbf{g}}$  as the output side. Unless shorted or open-circuited, a defective electron tube will usually cause reduced or distored output rather than none at all.

Reduced or Unstable Output. Reduced output is usually caused by lack of proper plate or grid voltages; unstable output is often caused by oscillation and intermittent circuit operation. Use a highimpedance voltmeter to check the grid or cathode bias voltage. A low bias voltage will cause a drop in output because heavy plate current causes peak clipping effects and distortion. A high bias will also cause lower output. If cathode bypass capacitor C2 is open, sufficient degeneration will be produced to appreciably reduce the output. Poor joint (soldering, etc) will create a high-resistance condition; if the poor joint is in the plate circuit, lower output will result. A leaky coupling capacitor (C 1) will improperly bias the stage, causing a reduction in output. If coupling capacitor C3 is leaky, it will improperly bias the next stage, draw more than normal plate current, and cause a dc voltage drop in L1; this voltage drop will reduce the effective plate voltage and the output, depending upon the amount of leakage. When normal voltage appears on the tube elements and the output is still below normal, the tube is probably defective. A gassy tube can cause high grid current, thus producing excessive bias with a reduction in output after a short period of operation. Normal output with the set initially operated, followed by a progressively

decreasing output shortly therafter is indicative of such a condition. Circuit oscillation at r-f requencies will also cause the output to drop and show up as a fuzzy pattern on the oscilloscope. If the oscillation is at audio frequencies, a howl or squeal will be apparent in the output, and will be indicated on the oscilloscope as a single frequency.

Unstable output can result from an intermittently open bypass capacitor in the cathode or plate circuit. Motor-boating (oscillating at a very low frequency) is sometimes caused by feedback through improper coupling of the gird and plate circuits or through common impedance coupling in the power supply; this is especially true with high-gain cascaded stages. Feedback through the power supply is usually caused by a defective bypass capacitor in the B+ line. This condition commonly occurs when electrolytic capacitors age and dry out, thus losing their capacitance gradually.

Distorted Output. Distorted output may be caused by poor frequency response, the introduction of hum, or improper grid bias. Distorted output due to poor frequency response is obvious when audible monitoring sources are available. To locate the distrotion, use an oscilloscope and a sine-wave generator to follow the signal path through the circuit. Observing where the waveform departs from normal will indicate the portions of the circuit involved. A squarewave generator may also be used. With a square-wave signal applied, a sloping leading edge indicates lack of high-frequency response, while a sloping flat top indicates lack of low-frequency response. Since a square wave is made up of many sine-wave frequencies, the application of a 2000 to 3000-Hz square wave will indicate the relative harmonic response over a range up to 5 to 10 times this frequency. Impedance coupling will normally produce a frequency response intermediate between that of resistance-coupled and transformer-coupled stages.

Hum distortion can be observed directly on an oscilloscope. When existing on the power supply leads, it indicates lack of sufficient power supply filtering. If it is not on the power leads, but is evident on the grid, plate, or cathode leads, check for induced hum pickup due to the nearness of grid leads to ac leads.

Improper bias is also a common cause of distortion; coupled with excessive drive, it causes the peaks or troughs of the voice signal to be clipped off. In a very weak tube, leak of sufficient filament **emission** 

can cause distortion on the peaks of amplification because of inability to supply sufficient peak current. While voltage measurements will determine whether the grid and plate voltages are correct, an oscilloscope must be used to observe the waveform. A distortion percentage of from 2 to 5 percent is normally considered acceptable in commercial audio amplifiers.

# IMPEDANCE-COUPLED AUDIO AMPLIFIER (SEMICONDUCTOR)

## Application.

The impedance+ **oupled** transistor audio amplifier is used where higher gain than the r-c coupled stage is desired with better response than that provided by transformer coupling.

## Characteristics.

Uses common emitter circuit for higher gain. Operates Class A for linear operation and minimum distortion.

Usually amplifies small signals, but can be designed to handle large signals in cascaded stages.

1s fixed biased from the collector supply, but may use self bias in some applications.

Emitter swamping is normally used for thermal stabilization.

Gain is fairly uniform over a range of approximately 100 to 15,000 Hz or more.

Both voltage and power gain are high.

# **Circuit Analysis.**

**General. The** impedance-coupled transistor amplifier is similar in a general sense to the impedancecoupled electron tube amplifier previously discussed in this section of the handbook. Use of the common (grounded) emitter circuit allows use of the analogy that the base of the transistor is equivalent to the electron tube grid, the emitter equivalent to the tube cathode, and the collector equivalent to the tube plate. Thus it is clear from the following schematic that the two impedance coupled circuits are practically identical. Any differences are due to the transistor internal parameters end the matching requirements to obtain maximum output with minimum distortion.

**Circuit Analysis. The** following schematic is that of a conventional PNP, triode, common-emitter impedance-coupled transistor audio amplifier circuit.



Impedance-Coupled Audio Amplifier

The input is shown capacitively coupled, and voltage divider R1,  $R_{\text{B}}$  provides fixed bias from the collector supply. Emitter swamping is provided by  $R_{\text{E}}$ for temperature stabilization;  $R_{\text{E}}$  is bypassed by  $C_{\text{E}}$ . (See the introduction to this section of the handbook for a discussion of bias arrangements and bias stabilization methods.) Collector impedance  $L_{\text{C}}$  is the load across which the output voltage is developed; this voltage is applied through coupling capacitor Ccc to the output circuit. Resistor R2 is the base-to-ground resistor in the next stage when cascaded amplifiers are used, or is the output load resistor (such as a headset) in single-ended stages. **(In** some applications R2 may be replaced by an iron-cored inductor similar to Le.)

Normally, the amplifier is a small-signal amplifier with the bias fixed at the center of the transistor dynamic transfer characteristic. With no input signal a steady collector current,  $I_c$ , flows as determined by the base bias voltage. With RI and  $R_B$  connected across the collector supply as a voltage divider, a forward (negative) bias is developed across  $R_B$ ; this bias is sufficient to cause the quiescent value of  $I_c$  to flow, even though the collector is reverse-biased.

When the input signal goes positive, assuming a sinewave input, the forward base bias is decreased instantaneously by the amplitude of the input signal, and collector current  $I_c$  is reduced. The reduction in collector current causes the voltage across collector inpedance  $L_C$  to decrease and rise toward the supply voltage, which is negative (this is exactly the reverse

of vacuum-tube action); thus, a negative-swinging output signal is developed, When the input signal becomes negative, it adds to the forward base bias and causes  $L_C$  to increase. The increase in collector current through  $L_c$  produces a large voltage drop across the impedance, reduces the negative collector voltage and produces a positive swing. Therefore, the collector output follows the input signal except that it is reversed in polarity; when the input signal is positive, the output signal is negative, and vice versa. The collector output is developed across the impedance of  $L_c$  between the collector and ground, and is applied through coupling capacitor Ccc to the base of the next stage, or to the output load.

in cascaded impedance+ oupled stages the base bias resistor and base-to-emitter internal impedance of the next stage transistor offer a shunt path between coupling capacitor Ccc and ground. Therefore, the reactance of Ccc and the total parallel resistance (or impedance) from base to ground form a voltage divider across the collector resistor of the first stage. If the reactance of the coupling capacitor is large, the output voltage is greatly attenuated, and only a small output appears between base and ground of the second stage. Since the reactance of Ccc varies inversely with frequency, the lower audio frequencies are attenuated more than the higher frequencies. For good low-frequency response the coupling capacitor is made sufficiently large in value that its reactance is very small as compared with the base-to-ground resistance or impedance. This is similar to vacuum-tube practice, where relatively small coupling capacitors (such as .001 microfarad) are satisfactory, because the vacuum-tube grid-to-ground impedance is very high. Because the transistor base-to-emitter impedance is fairly low (about 500 ohms), a coupling capacitor of 50 microfarads or more is needed to achieve the low impedance required to pass the signal without excessive attenuation. (A 50-microfarad capacitor has a capacitive reactance of approximately 30 ohms at 100 Hz.) For good low-frequency response the reactance of the coupling capacitor should always be less than one-tenth the effective base input impedance.

In those circuits where an impedance replaces R2 the coupling capacitor and inductor can be made to series-resonate at a low frequency to provide bass boost.

At the higher audio frequencies (above 15,000 Hz), the collector-to-emitter capacitance of the first stage and the base-to-emitter shunting capacitance of

the second stage together with the large distributed capacitance from turn to turn of the collectorinductance tends to bypass the high frequencies to ground, causing a drop in the response. The frequency-attenuating action produced by the transistor occurs because the width of the internal transistor PN junctions are voltage-sensitive. With high voltage the transition region is narrow, corresponding to the closely spaced plates of a capacitor with the associated high capacitance. The reverse bias on the collector also reduces the width of this transition region, so that transistors are generally characterized by a high interelectrode capacitance. For example, an audio transistor may have a collector-to-base capacitance on the order of 50 picofarads, as compared with a vacuum-tube plate-to-grid capacitance of one or more picofarads. The collector-tp-emitter capacitance is usually 5 to 10 times the value of the collector-tobase capacitance (in the common-emitter circuit), as compared with 8 picofarads or less for vacuum-tube plate-to-cathode capacitance. Thus, it can be seen how the high-frequency response is affected considerably by internal transistor parameters. Of course, any shunt wiring capacitance and that of the collector inductance will also add to the shunting effects of the transistor. Both low-and high-frequency compensating circuits may be used to increase the effective frequency response of the circuit, as discussed in Wideband Video Amplifier Circuits later in this section.

Over the region of 100 to 15,000 Hz, the impedance-coupled amplifier has a relatively flat response, and with proper matching will afford high power and voltage gains. Hence, this form of coupling is employed where good audio response is required with a moderate power output (for high output transformer-coupling is used). The common-base configuration is sometimes employed where better high-frequency response is desired than that provided by the common-emitter circuit, since the collector-to-base capacitance is only 1/5 to 1/10 as great.

Transistor audio amplifiers are also characterized by a high inherent noise which is greatest at the lower audio frequencies. Operation with low values of emitter current and low collector voltages, together with low values of input resistance, tends to minimize the noise. By using an inductor in place of the base-toground resistor ( $R_B$  or R2 in the schematic) a very low input resistance, and a lower noise figure over that of the r-c coupled amplifier is obtained. In the

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common-emitter circuit, degenerative effects produced by an unbypassed emitter resistor tend to increase the input resistance. Thus, it is conventional practice to use large emitter bypass capacitors to avoid any possibility of degeneration. As with the electron tube, external feedback circuits provide tretter response, although emitter degeneration may sometimes be used. Since fixed bias from the collector supply may be easily obtained by a simple voltage divider, it is used in both large-an-small-signal applications. Self-bias is generally restricted in use to very small-signal amplifiers; otherwise, distortion and improper operation with a reduction in gain, or blocking, may occur on large signals. The emitter resistor functions mainly as a swamping resistor for temperature stabilization, and prevents large changes in amplification with temperature variations.

In considering the operation of the transistor impedance-coupled amplifier as compared with the electron-tube impedance-coupled amplifier, it should be clear from the above discussion that one circuit is an almost exact counterpart (dual) of the other. The difference is that transistor stages operate with low input and output impedances, at low voltages; and at very low levels of amplification, whereas electrontube stages operate with relatively high input and output impedances, at high voltages, and at high levels of amplification. Thus, the transistor is basically a current amplifier, while the electron tube is a voltage amplifier. Consequently, the transistor requires closer matching (rather than mis-matching) of impedances to maximum performance.

# Failure Analysis.

**General.** When making voltage checks use a vacuum tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

**No Output.** A no-output condition may be caused by an open or short circuit, by improper bias or loss of collector voltage, or by a defective transistor. A voltage check will determine whether the bias and collector voltages are normal; also a VTVM will indicate audio input and output voltages. With the few components involved, simple voltage and resistance checks will usually indicate the source of trouble. If

the bias voltage divider is open because return resistor  $R_{p}$  is defective the transistor will conduct heavily in the saturation region. With R, open, only contact bias exists and the transistor will be cut off. If collector inductor L<sub>c</sub> is open there will be no voltage measured between the collector and ground. If emitter resistor  $R_{\mu}$  is open, the circuit will not operate; however, if emitter bypass capacitor  $C_{E}$  is shorted, the circuit will operate but it will be temperature-sensitive. Likewise, if the emitter bypass capacitor is open, it may reduce the output because of degenerative feedback, but normally will not cause complete stoppage of operation. If the input coupling capacitor or the output capacitor is open, no output will be obtained. Check the input and output circuits with an oscilloscope; disappearance of the signal will indicate the location of the defective component. If the coupling capacitor is shorted or leaky, it will affect the base bias if located at the input, but will probably not be sufficient to stop operation. On the other hand, if the output capacitor is at fault, the collector reverse bias (which is normally high as compared with the base bias) will be applied as full forward bias to the base of the next stage and will bias it heavily into saturation; thus, no output will result, and the current may be sufficient to destroy the transistor. If the coupling capacitor is leaky, the effect will depend upon the amount of leakage. With a slight leakage there maybe practically no observable effect, or possibly distortion; with heavy leakage there will probably be no output. Of course, if the transistor is shorted or otherwise defective, a no-output condition will occur. A rough check of transistor operation can be made (if the transistor can be easily removed from the circuit) by measuring the forward and reverse resistances with an ohmeter. A high reverse resistance and low forward resistance indicates that the transistor is operable, but does not indicate if the gain is normal. Be certain to observe the correct polarities.

**Reduced Output.** Improper bias voltage or a change in the value of a component, as well as a defective transistor can cuase reduced output. If the transistor gain is low, the output will also be low. If either of the base voltage-divider bias resistors changes in value, the bias will be either too low or too high and the output will be reduced, with accompanying distortion. A simple voltmeter check will determine whether the bias is correct. If the collector inductor develops a high resistance, the output will be de-

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creased because of the extra dc voltage drop across the choke. If the coupling capacitors are defective, a loss of output at the low-frequency end of the spectrum will result when the coupling capacitance is less than the design value. A leaky capacitor will likewise cause improper bias voltages and reduced output. Capacitors usually must have one end disconnected from the circuit before they can be tested by means of a standard capacitance analyzer (in circuit capacitance checkers do not require this).

Distorted Output. If the base bias is too high (reduced forward bias), the transistor will operate on the lower portion of its dynamic transfer characteristic, and the negative input peaks will be clipped (positive collector swings). Likewise, if the bias is too low (increased forward bias), the transistor will conduct heavily and operate on the upper portion of its dynamic transfer characteristic, with corresponding clipping of the positive peaks (negative collector swings). In both cases extreme distortion will be caused. If the bias is proper but the collector voltage is not, similar effects may be caused. If the collector voltage is too high, the negative collector swing will be clipped, and if too low the positive collector swing will be clipped; in either instance heavy distortion will result. An open emitter bypass capacitor will permit degenerative feedback to occur, and, depending upon the amount, will show either as distortion or as reduced output. A change in load resistance produced by a defective collector choke or load resistor, or by a leaky coupling capacitor (causing a heavy shunting of the output load) usually shows as a distorted output with reduced volume because of the mismatching. Use an oscilloscope to follow the signal through the circuit and determine the point at which the waveform departs from normal. In most instances the defective component will then be apparent. Do not overlook the possibility that distortion may be occurring in a previous stage, merely being amplified by the stage under suspicion. Too large an input (overdrive) will cause both positive and negative peak clipping with distortion, just as in a electron-tube amplifier. Apply a square-wave input from a signal generator and observe the output on an oscilloscope. Frequency distoriton will be shown by a sloping rise and fall time (poor high-frequency response); a sloping flat top indicates poor low-frequency response. Electrontube techniques for locating distortion may generally be used for transistor trouble shooting if the proper voltages and polarities are employed.

# TRANSFORMER-COUPLED AUDIO AMPLIFIER (ELECTRON TUBE)

#### Application.

The transformer+ **oupled** triode audio voltage amplifier is used principally for the development of large a-f voltage outputs with a minimum number of amplifier stages and for phase inversion to drive a push-pull amplifier. The limitations of frequency response generally restrict the use of transformer coupling to audio circuits, which do not require an exceptionally wide bandpass or frequency response, but do require large voltage outputs.

#### Characteristics.

Utilizes low plate-resistance triodes (7500 to 15,000 ohms) with amplification factors of from 8 to 20.

The transformer step-up ratio usually does not exceed 3:1 for good-quality audio. However, much higher ratios are sometimes employed to obtain extreme gain with a sacrifice of frequency response.

Opearate Class A; no grid current flows under normal conditions.

Frequency response is linear only over a relatively narrow band of frequencies (approximately 200 to 10,000 Hz).

Cathode bias (self-bias) is normally used, but fixed bias may be used of desired.

Output signal may be phased so that it is of the same polarity and phase as that of the input signal, or opposite as. desired.

#### Circuit Analysis.

General. The transformer-coupled triode audio voltage amplifier utilizes the transformer as a combined plate loading and coupling device. It is the primary of the transformer which serves as the plate load, while the secondary functions as the coupling element. The amplified version of the input signal is developed across the transformer primary. Assuming that the primary impedance is large as compared with the plate resistance of the triode, the voltage developed in the transformer primary is approximately equal to the amplification factor  $(\mu)$  of the tube multiplied by the input signal. Therefore, the induced signal in the transformer secondary, which is applied to the following stage, is approximately equal to  $\mu$  N, where N represents the step-up turns ratio between the primary and secondary of the transformer.

Transformer coupling has several distinct advantages over either R-C or impedance coupling. A lower value of plate supply voltage can be used, as compared with that of an R-C coupled stage, since the dc resistance of the primary winding is small. The secondary winding of the transformer, when center-tapped, can be used to supply two grid voltages 180 degrees out of phase to a push-pull amplifier, or two in-phase outputs for push-pull operation. The impedance-matching properties of the transformer may also be utilized if needed. Since the primary and secondary of the transformer are not connected together, the following stage (or the output device is isolated from the dc plate voltage of the amplifier stage, eliminating the need for an output network (such as a grid resistor and coupling capacitor), thus effecting a reduction of components. The transformer also has several disadvantages. Its cost is high, and it has large bulk and weight. Additional shielding is also required to prevent the stray fields introduced by the transformer from interfering with the operation of other stages, or causing unwanted feedback within the stage.

**Circuit Operation.** A schematic diagram of a typical transformer-coupled audio voltage amplifier with a high-impedance input is shown in the accompanying figure. Cl is the input blocking and coupling capacitor, and  $R_g$  is the grid return resistance. Resistor  $R_{\kappa}$  is the cathode bias resistor, bypassed by  $C_K$  to prevent degeneration. Refer to the introduction to this section of the handbook for a discussion of cathode biasing methods. Transformer  $T_1$  is the plate input and output transformer, coupling the output to the next stage or to the load.



Typical Transformer-Coupled Audio Voltage Amplifier

As can be seen from the schematic, the input signal is capacitively coupled through C 1 to the grid of tube VI. Coupling capacitor, C 1, and grid resistor,  $R_g$ , form an audio voltage divider. The output of this voltage divider is the signal voltage applied to the grid of V1. Capacitor C 1 also acts as a dc blocking capacitor to prevent the plate voltage of a preceding stage, or any dc voltage existing in the input circuit, from adversely biasing VI. The reactance of Cl to an audio frequency signal is much smaller than R1; thus little signal is lost across the capacitor.

With no signal applied, static plate current flows \_ through cathode resistor  $P_k$  and provides Class A bias. A plate voltage drop (E) across the primary of transformer T1 is produced by the dc coil resistance. This small voltage drop is constant, regardless of whether or not a signal is present; and produces no output voltage since it is not connected to the secondary, but does reduce the available plate voltage by a small amount. When a positive-going input signal is applied to the grid of tube V1, it reduces the effective grid bias, and the plate current increases instantaneously. Assuming a sine-wave input, as the signal rises the plate current also increases, until the positive peak of the input cycle is reached. During this half of the cycle (from point a to point b on the output waveform), a continuously increasing voltage drop (negative swing) occurs in the primary as the constantly increasing plate current flows through the load impedance (consisting of the primary reactance plus the reflected load from the secondary). The increasing plate current induces a voltage (esec) in the secondary of T1 which is the output voltage  $(e_0)$ . When the secondary is properly connected (phased), the input signal and the output signal are in phase with each other, otherwise they remain out of phase. When the \_ grid input voltage reaches a positive crest at point b on the waveform, the drop across the primary of T1 is at a negative maximum, and is 180 degrees out ofphase with the input, causing the effective plate voltage to reach its minimum value (the plate current is now at a maximum). As the grid input voltage now recedes towards zero, the effective bias is continuously reduced (made more negative), causing the plate current also to reduce. The reduction of plate current changes the direction of the magnetic field produced around the transformer primary, and induces an oppositely polarized voltage in the secondary of TI. While the primary voltage is positive-going, the secondary voltage is negative-going. When the

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sine-wave signal on the grid reaches point c on the waveform, the positive half-cycle of operation is completed and the tube is again at its quiescent point. Now, the grid signal continues to increase in a negative direction and adds to the cathode bias to make the effective bias still more negative, and reduces plate current flow below quiescent value. This action continues until the negative crest is reached at point d on the waveform. Since the plate voltage is increasing toward the supply value while the plate current is decreasing, at point a the plate voltage is maximum, and the primary voltage arop is positive and maximum also. Because the induced secondary voltage is opposite that of the primary, the output is a maximum negative voltage (it is in-phase with the input). As the grid input signal again reverses direction and falls back towards zero, the effective grid bias once again is decreased and becomes positive-going. Consequently the plate current increases towards quiescent or zero value, and in changing direction it again changes the direction of the field around T1 primary. Thus, a positive-going voltage is again induced in the secondary to complete the negative half-cycle of operation.

For convenience and ease of discussion, the transformer is represented by three equivalent circuits in the accompanying figure. Part A represents the lowfrequency range (below 200 Hz), part B represents the middle-frequency range 200 to 8000 Hz), and part C



Transformer-Coupled Amplifier, Equivalent Circuits

represents the high-frequency range (8000 to 20,000 Hz).

In part A of the figure, -peg is considered to be an ac generator which represents the amplified output voltage of triode VI;  $r_p$  represents the ac plate resistance of the tube, and  $L_p$  represents the inductance of the transformer primary. The dc resistance of the primary winding, which is normally small, can be considered as included in  $r_p$ . Ip and r form a voltage divider, with the output vo **itage taken** from across  $L_p$ . At low signal frequencies, the reactance of  $L_p$  becomes small; thus most of the developed voltage appears across  $r_p$ , thereby decreasing the voltage dropped across the primary, and hence the output voltage. For a given value of inductance, the lower the frequency the less the output voltage.

In part B of the figure, the reactance of  $L_p$  is . considered very large as compared with  $r_p$ . Consequently the voltage dropped across  $r_p$  is much smaller than that developed across  $L_p$  by generator  $-\mu e_g$ . The magnitude of the output voltage is determined by the tube amplification factor, the plate resistance, the amplitude of the applied signal voltage, and the turns ratio of the transformer. It is over this frequency range that the response is most uniform and the gain is maximum.

In part C of the figure,  $C_d$  represents the distributed capacitance between the windings of transformer T1 and interelectrode, stray, and wiring capacitances. The total distributed capacitance, which is appreciably large, shunts the higher frequencies to ground, since its reactance decreases with increasing frequency  $L_e$  represents the equivalent inductance of the transformer (both primary and secondary). The value of  $L_e$  depends on the leakage flux and the amount of mutual coupling between the windings. This inductance, together with  $c_d$  in the equivalent circuit, forms a series-resonant circuit which resonates at some high audio frequency. At and near resonance, the magnitude of the voltage across  $C_d$  is extremely large. If the applied frequency is raised above resonance, the reactance of  $c_d$  decreases; hence the output voltage,  $\mathbf{e}_{0}$ , decreases. The following figure, a typical response curve, shows a relatively uniform middle-frequency response, a gradual "rolloff" at low frequencies, and a sharper decay at high frequencies (which is preceded by a resonant peak).



Typical Response Curve of A Transformer-Coupled Amplifier

In practice, the gain of a so-called "flat response" transformer varies not less than 1 dB and sometimes as much as 3 dB or more over the range of **200** to **10,000** Hz.

# Failure Analysis.

No Output. Generally speaking, a no-output condition is caused by the lack of an input signal, an opencircuited condition by the lack of plate or filament voltage, a short-circuited condition, or by a defective tube. The presence of an input signal may be determined by using an oscilloscope or vacuum-tube voltmeter to check the input. An open-circuited condition can be localized to the defective portion of the circuit by using a high-resistance voltmeter to determine whether filament, cathode, grid, and plate voltages exist and are normal. Open filament circuits can sometimes be spotted by noting that the filament does not light and that the tube feels cold to the touch. When a lack of voltage is found, the source (power-supply) voltage should be checked to determine whether the voltage is present; if so, the fault is in the amplifier and not in the power supply. In any case, a lack of voltage indicates either a short-circuit or an open circuit in the associated component. For example, when B+ is present at the supply end of the transformer primary but not at the plate, T] is open. If the voltage between the primary and ground is equal on both the supply-side and the plate side, there is no voltage drop across the primary coil. Therefore, either the plate current drain is too little (with the possibility of cutoff bias), or, with normal current drain, a short-circuited primary is indicated. Where the primary resistance is known, as resistance check with the B+ supply off and the filter capacitors discharged will indicate whether the transformer is defective. Usually, a short-circuited condition is evidenced visually by burning or charring of the parts involved.

When all voltages appear normal and an input signal is present, but there is still no output, it is obvious that tube VI is at fault. Defects in the tube develop with age, and contribute to below-normal circuit operation, in the form of a low or distorted output rather than no output. However, vibration or excessive voltage can cause the tube to become open or shorted; therefore, this possibility must be considered. Indiscriminate replacement of tubes should be avoided.

**Reduced** or Unstable Output. Reduced output is usually caused by a lack of proper grid and plate voltages, or low filament emission, while unstable output is usually caused by oscillation or intermittent functioning of circuit components. Check the bias voltage on the grid (or cathode) to determine that it is normal. A low fixed bias voltage can cause reduced output due to heavy plate current and peak clipping effects; these symptoms are not applicable to selfbias, becuase with this circuit arrangement heavy plate current will increase the bias; thus the circuit tends to be self-compensating. A high bias will cause reduced output. An open cathode by-pass capacitor  $(c_k)$  can cause sufficient degeneration to reduce the output appreciably. Poor joints (soldering, etc), which create high-resistance conditions in the plate circuit will also produce reduced output. If all voltages are normal and reduced output still exists, the trouble is likely to be in the electron tube. Circuit oscillation may also cause the output to drop, and will show up as fuzzy pattern on the oscilloscope.

Unstable output, erratic operation, or distortion can result from a defective bypass capacitor in the cathode circuit. When in doubt, use an oscilloscope and a sine-wave generator to observe the waveform at the input and output of the tube. In the case of intermittent conditions where oscillation is suspected, the application of a square-wave signal will tend to produce oscillation if instability is the cause of the trouble. Oscillation can result only from feedback caused by improper coupling of the grid and plate circuits, or by common impedance coupling through NAVSHIPS 0967-0000120

the power supply in multistage amplifiers, resulting from aging electrolytic bypass capacitors. This form of oscillation is called "motorboating", since it consists of a very low-frequency signal. Direct feedback usually manifests itself as a squeal or howl in the output.

Distorted Output. Improper bias is a common cause of distortion in the amplifier output. Check for the proper voltages in the grid and plate circuits. (Check the transformer for a dc leakage path between the primary and secondary windings if the bias is positive on the following stage.) Tube performance deteriorates with age, and usually manifests itself in the form of distorted and weak output. In a weak tube, lack of sufficient filament emission can cause distortion on the peaks of amplification because of its inability to pass sufficient current. While voltage measurements will determine whether the grid and plate voltages are correct, it is usually necessary to use an oscilloscope to observe the waveform and determine the cause of the distortion. An oscilloscope and a sine-wave generator should be used to follow the signal path through the circuit; observing where the waveform departs from normal will indicate the defective portion of the circuit. When the observed waveform exhibits a flattening of the negative peak, the current should be checked for abnormal conditions, such as insufficient grid bias, overdrive, and a leaky coupling capacitor. Similarly, excessive bias or grid current flow is evidenced by an oscilloscope waveform pattern with a flattening of the positive peaks. Overloading the amplifier will also produce these same effects; in this case the waveform will show both clipping of the positive and negative peaks.

Oscilloscope waveforms are a valuable aid in failure analysis when poor frequency response is suspected as the cause of distortion. For example, when a wave form which is supposedly a sine wave shows a characteristic "rounded" effect on the positive peak, this is a clear indication of poor low-frequency response of the transformer. In making more precise measurements, a square-wave generator may be used. With a square-wave signal applied, a sloping leading edge indicates a lack of high-frequency response, while a sloping flat top indicates a lack of lowfrequency response. Since a square wave is made up of many sine-wave frequencies, the application of a 2000 to 3000-Hz square wave will indicate the relative harmonic response over a range up to 5 to 10 times this frequency.

Hum distortion can be observed directly on an oscilloscope. When it is on the power supply filtering. If it is not on the power leads, but is evident on the grid, plate, or cathode ,leads, check for induced hum due to the nearness of ac leads in the wiring. Poorly shielded and improperly grounded transformers may also be the cause.

# TRANSFORMER-COUPLED AUDIO AMPLIFIER (SEMICONDUCTOR)

### Application.

The transformer-coupled transistor audio amplifier is used where higher gain and power output than that provided by an r-f-coupled or impedance-coupled stage are required, and where the reduction in frequency response can be tolerated.

#### Characteristics.

Uses common emitter circuit for higher gain. Operates Class A for linear operation and minimum distortion.

Usually amplifies small signals, but can be designed to handle large signals in cascaded stages.

Is fixed-biased from the collector supply, but may use self-bias in some applications.

Emitter swamping is normally used for thermal stabilization.

Gain is fairly uniform over a range of approximately 100 to 10,000 Hz or more.

Both voltage and power gain are high.

### **Circuit Analysis.**

**General.** The transformer-coupled transistor amplifier is similar in general to the transformer-coupled electron-tube amplifier previously discussed in this section of the handbook. Use of the common-emitter (grounded-emitter) circuit permits the assumption that the base of the transistor is equivalent to the electron-tube grid, the emitter is equivalent to the tube cathode, and the collector is equivalent to the tube plate. Thusm it is clear from the following schematic that the two transformer-coupled circuits are practically identical. Any differences are due to the transistor internal parameters and the matching requirements to obtain maximum output with minimum distortion.

**Circuit Operation.** The accompanying schematic is that of a conventional PNP, triode, common-emitter,

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transformer-coupled transistor audio amplifier circuit. The input is shown transformer-coupled through Tl, and voltage divider R1,  $R_{\text{B}}$  provides fixed bias from the collector supply. Emitter swamping is provided by  $R_E$  for temperature stabilization;  $R_E$  is bypassed by  $C_{\text{E}}$ . (See the introduction to this section of the handbook for a discussion of bias arrangements and bias stabilization methods.) The output is transformer coupled through T2.



**Transformer-Coupled Audio Amplifier** 

The use of T1 to apply the input signal to the base circuit provides an almost ideal temperature response characteristic. The low transformer winding resistance produces a low base input resistance, and, when used with emitter swamping resistor  $R_{E}$ , any variation in gain with temperature is reduced to a very small value over a large range of temperatures (greater than for any other type of coupling circuit). Normally, transistor Q1 rests in its quiescent condition, with Class A bias provided by voltage divider RI, R<sub>n</sub>. The quiescent collector current, I<sub>c</sub>, is steady, producing only a small constant voltage drop across the primary resistance of T2. Thus, practically the full value of collec $t_{\alpha}$  supply,  $V_{cc}$ , is available. With a steady collector current no voltage is induced in the secondary of T2, and there is no output (assuming no input signal or noise). When a positive-swinging signal is introduced into the input circuit, current flow through the primary of T1 induces a voltage in the secondary, which is applied to the base of Q1. Assuming that the transformer secondary is connected in-phase with the primary, a positive increase in voltage appears at the base. This positive voltage swing cancels the forward negative bias, and a reduced flow of collector current occurs. As the instantaneous collector current decreases, the primary voltage drop also decreases, and allows the collector voltage to rise toward the negative supply voltage. Meanwhile, the reducing collector current induces a voltage in the secondary winding. The secondary winding is connected in-phase so that a reducing collector current produces a negative voltage swing in the secondary, and on increasing current produces a positive swing.

The emitter current flowing through  $R_{F}$  is the steady quiescent value, and any change in base bias with input signal is bypassed around the emitter resistor through capacitor  $C_E$ . Although the capacitor will not pass the quiescent dc current, it will pass the alternating audio voltage produced by the changing input signal. Thus, only dc current changes flowing through  $R_{E}$  (the thermally induced changes caused by temperature variation) produce an emitter bias. This emitter bias is in a direction which causes a reduced flow of emitter current, since it reduces the forward bias and hence reduces the collector current back to the original value so that it appears unchanged. If the emitter bypass capacitor were not used, the input signal voltage would produce a degenerative effect, since all collector and emitter current would be forced to flow through the emitter resistor.

Consider next the negative swing of the input signal. In this instance, the forward bias on the base element is increased (the two negative voltaged add), and a heavy collector current flow occurs. The increasing  $i_c$  through the primary of T2 induces a voltage into the secondary. Assuming the same in-phase connection of the primary and secondary, the output voltage is positive.

Note that this action is similar to that of the vacuum tube amplifier, except that it is opposite. That is, a positive input to an electron-tube grid increases the plate current, whereas a positive input to a PNP transistor base element reduces the collector current. In each instance, however, the polarization of the output is opossite that of the input. By changing the connections of the secondary winding of either T1 or T2, the signal can be changed so that it is of the same phase at both the input and the output; this is an advantage of transformer coupling.

Since the secondaries of T1 and T2 are not connected to their primaries, the transformers offer a convenient method of separating input or output signals from bias or collector voltages. By using the proper turns ratio, the primary and secondary impedances may be matched. In the base circuit the input resistance is matched, giving maximum gain, likewise, in the output circuit the proper turns ratio reflects the secondary load impedance into the primary, which, when added to that of the transformer primary itself, provides a matched load for maximum output.

Normally, the transformer-coupled stage is operated in the middle of its transfer characteristic to produce linear amplification. It is also a small-signal amplifier when used in preamplifier stages. In following cascaded stages it becomes a large-signal amplifier, operating with a larger bias over the linear range of its transfer characteristic. When necessary, bias resistor  $R_B$  is bypassed to ground with a large capacitor to prevent audio signal voltages from causing the bias to change with the signal, particularly in high-gain and large-signal amplifiers.

In cascaded transistor amplifiers the load on the secondary of T2 is the base resistance of the next transistor. Since this is resistive rather than reactive, there is less frequency distortion that would occur in an electron tube, where the load is predominantly reactive (even in output stages the speaker is a varying reactance). In low-power stages the flow or reverse (leakage) current,  $I_{ceo}$ , through the collector-to-base junction becomes important when it is a large percentage of the total operating collector current. Thus, the designer chooses a transistor with as large a beta as is possible, and as small a leakage current as can be obtained, in order to get the most gain with the least leakage current. (The flow of reverse current does not occur in electron tubes.)

The frequency response of the transformercoupled amplifier is lower than that of the resistancecoupled or impedance-coupled transistor audio amplifier. There is more shunting capacitance than in resistance coupling because of the transformer distributed turn capacitance, and there is a leakage inductance between the primary and secondary which does not exist in the impedance-coupled stage. The accompanying figure shows the equivalent circuit of a transformer-coupled stage and the factors that affect the response

In the figure, resistors R1 and R2 represent the de primary and secondary resistance, respectively. These resistances must be kept low since they are ohmic



**Transformer Equivalent Circuit** 

losses: also, the full collector current usually flows through R]. Therefore, the slope of R1 determines the de load line, and the transformers are designed to have a primary resistance of from 200 to 800 ohms for proper matching of transistors. inductances  $L_{P}$ and L<sub>s</sub> represent the magnetizing inductances of the primary and secondary transformer windings, respectively. The primary inductance is usually made from 2 to 5 times load resistance R<sub>L</sub> for good lowfrequency response. However, the lower the frequency the less the inductive reactance, so that the response tends to drop at low frequencies. Capacitors  $C_p$  and  $C_s$  represent the shunting capacitances of the primary and secondary windings, respectively. These include the shunt base-to-ground and collector-toground capacitances of the transistor, which are also large. Therefore, the high frequencies tend to be shunted to ground  $C_p, L_e$ , and Cs in combination form an effective low-pass filter, so that the high frequencies are attenuated (L is the leakage inductance between the primary and secondary). In substance, then, we see that the high-frequency response is primarily determined by the combination of shunting capacitance with load resistance and leakage inductance, while the low-frequency response is determined by the combination of load resistance and magnetizing inductance. In addition, the shunting capacitance and inductance form resonant circuits which produce humps in the response curve. Practically speaking, the response is very similar to that of the electron-tube transformer-coupled audio stage, with somewhat less high-frequency response. Loss of low-frequency response as compared with the electron-tube circuit becomes apparent when miniaturized transformers are used, because of the difficulty of building transformers with a sufficiently

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large iron core to provide a high inductance with the limited number of turns available in the space allocated.

Despite the apparent loss of response in the transistor transformer-coupled amplifier as compared with other forms of coupling and the use of electron tubes, relatively good response is obtained by using more stages and low-and-high-frequency peaking circuits where necessary. A miximum efficiency of about 50 percent is obtained as compared with 25 to 30 percent for resistance-coupled stages.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition may be caused by an open-or-short circuited transformer winding, by improper bias or loss of collector voltage, or by a defective transistor. A voltage check will determine whether the bias and collector voltages are normal; also a VTVM will indicate audio input and output voltages. With the few components involved, simple voltage and resistance checks will usually indicate the source of the trouble. If the bias voltage divider is open because return resistor  $R_{\rm p}$  is defective the transistor will conduct heavily in the saturation region. with R<sub>1</sub> open, only contact bias exists and the transistor will be cut off. If the primary of  $T_1$  is open, there will be no voltage measured between the collector and ground. If emitter resistor  $R_{\rm F}$  is open, the circuit will not operate; however, if emitter bypass capacitor  $C_{\rm E}$  is shorted, the circuit will operate but it will be temperature-sensitive. Likewise, if the emitter bypass capacitor is open, it may reduce the output because of degenerative feedback, but normally it will not cause complete stoppage of operation. If the input transformer or the output transformer is open, no output will be obtained. Check the input and output circuits with an oscilloscope; disappearance of the signal will indicate the location of the defective winding. If the transistor is shorted or otherwise defective, a no-output condition will occur. A rough check of transistor operation can be made (if the transistor can

be easily removed from the circuit) by measuring the forward and reverse resistance with an ohmmeter. A high reverse resistance and low forward resistance indicates that the transistor is operable, but does not indicate whether the gain is normal. Be certain to observe the correct polarities.

**Reduced Output.** Improper bias voltage or a change in the value of a component, as well as a defective transistor or transformer, can cause reduced output. If the transistor gain is low, the output will also be low. If either of the base voltage-divider bias resistors changes in value, the bias will be either too low or too high and the output will be reduced, with accompanying distortion. A simple voltmeter check will determine whether the bias is correct. If the collector winding of T2 develops a high resistance, the output will be decreased because of the extra dc voltage drop.

Distorted Output. If the base bias is too high (reduced forward bias), the transistor will operate on the lower portion of its dynamic transfer characteristic, and the negative input peaks will be clipped (positive collector swings). Likewise, if the bias is too low (increased forward bias), the transistor will conduct heavily and operate on the upper portion of its dynamic transfer characteristic, with corresponding clipping of the positive peaks (negative collector swings). In both cases extreme distortion will be caused. If the bias is proper but the collector voltage is not, similar effects may be caused. If the collector voltage is too high, the negative collector swing will be clipped, and if too low the positive collector swing will be clipped; in either instance heavy distortion will result. An open emitter bypass capacitor will permit degenerative feedback to occur, and, depending upon the amount, will show either as distortion o'r as reduced output. A change in load resistance produced by a defective output transformer (T2) or a load resistance change usually shows as a distorted output with reduced volume because of the mismatching. Use an oscilloscope to follow the signal through the circuit and determine the point at which the waveform departs from normal. In most instances the defective component will then be apparent. Do not overlook the possibility that distortion may be occurring in a previous stage, merely being amplified by the stage under suspicion. Too large an input (overdrive) will cause both positive and negative peak clipping with distortion, just as in an electron-tube amplifier. Apply a square-wave input from an audio signal generator

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and observe the output on an oscilloscope. Frequency distortion will be shown by a sloping rise and fall time (poor high-frequency response); a sloping flat top indicates poor low-frequency response. Electrontube techniques for locating distortion may generally be used for transistor trouble shooting if the proper voltages and polarities are employed.

# SINGLE-ENDED, R-C-CO UPLEO TRIODE AUDIO POWER AMPLIFIER (ELECTRON TUBE)

## Application.

The use of the single-ended, R-C-coupled triode audio power amplifier is limited to those applications where relatively small amounts (less than 5 watts) of audio power are required, such as an audio output stage with a loudspeaker load.

#### Characteristics.

Power gain is relatively low (usually not more than 5).

Plate efficiency is low (on the order of 25 percent).

Power sensitivity is low for triode power amplifiers operating under Class A conditions (power sensitivity is the ratio of output **power** in milliwatts to the square of the rms grid voltage which produces it).

Distortion is relatively low (5 percent maximum). Operates Class A at all times. no grid current flows under normal conditions.

Cathode bias (self-bias) is usually used, but fixed bias may be used if desired.

frequency response is relatively uniform over a range of 200 to 10,000 Hz.

## **Circuit Analysis.**

**General.** The primary function of a power amplifier is to deliver sufficient power to a circuit load; any increase of voltage is of secondary importance. In fact, the voltage amplifier uses the same circuit as the power amplifier. The main difference in the two circuits is that the power amplifier is usually the last stage (the output stage). In some instances a power driver may be employed, for example, to supply the driver power for the grids of a Class B high-power modulator. However, this is a special application in which the full output of the stage is usually not used. Since the objective is to obtain as much power output as possible, with as low a plate voltage as practicable, tubes with a low plate resistance are employed. As a consequence, these tubes are of the low-mu type rather than the high-mu type used in voltage amplifiers. (They are also larger in size, having plates capable of full dissipation of the dc power involved, use higher plate voltage and current, and are generally more rugged than tubes used as voltage amplifiers.) Because of the low mu, a large grid excitation voltage is usually necessary to drive the power amplifier. Therefore, a voltage driver stage is usually associated with the power amplifier. Consequently, at least three stages are necessary to provide audio power output when triodes are used, namely, a high-gain input stage, a driver amplifier, and the output stage. When only one tube is employed in the output stage, it is said to be single-ended. When two tubes are used, they are connected either in push-pull, in push-push, or in parallel. Where power output is considered more important than the distortion products, the parallel connection is generally used to provide about three fourths the rated power of two tubes. For full output and the least distortion, the push-pull connection is used (see the discussion of push-pull Audio Power Amplifiers later in this section). Although pentodes will produce more output than triodes, no further mention of them will be made in this circuit discussion since they are treated separately (see the discussion of Single-Ended, R-C-Coupled Pentrode Audio Power Amplifier later in this section.)

Operation under Class A conditions with lack of grid current and an effectively high-impedance R-C coupled input eliminates any possibility of grid losses. This however, does not mean that the effect of the loading of the input circuit on the output of the preceding (driver) stage may be neglected. Thus, the power-amplifier grid input circuit constants determine to a large extent the total amount of undistorted voltage drive available.

The large ac (audio) power output derived from the single-ended circuit is actually obtained from the dc plate supply by converting the dc power to ac power through tube action. Maximum *undistorted* power output is normally obtained when the load resistance is equal to twice the plate resistance of the tube. If the load resistance is made higher than this optimum value, a reduced output will be obtained; however, the distortion will also be greatly reduced. As a result, in those cases where sufficient power output is available, it will be observed that the load

resistance is more than twice the tube plate resistance. For each tube type and **given** set of circuit conditions, the same set of operating rules does not necessarily apply. Therefore, the preceding discussion is broadly applicable only, and varies considerably with design. It is of interest to note that the distortion present in the single-ended stage consists primarily of second-harmonic signal. While **other** harmonics are also present, they are of much lower amplitudes and are normally neglected. Output ratings are generally computed for the maximum power output obtained when the second-harmonic distortion does not **exceed** 5 percent. Thus, the stage may be operated at lower power outputs with appreciably less distortion.

This is usually what is done with so called "hi-fi" (high-fidelity amplifiers systems. For example, a 25-watt output capability is supplied to provide only 2 or 3 watts for normal use. Hence, instead of being 5 percent or more, the distortion is reduced to less than 1 percent. To obtain maximum undistorted power output, the stage must have a properly matched load. This is, the output *load* (usually a loudspeaker) must equal (match) the *desired plate load impedance*. In this case, the output transformer serves as an impedance-matching as well as a coupling device, and must be capable of handling the full input power constantly. Since a speaker output load offers a different impedance to different audio frequencies, it is customary to consider it as offering a purely resistive load, and to assume that it has no reactive components which may be sensitive to various frequencies. Design is accomplished under these ideal conditions; however, practical operation is not quite the same. An explanation of loading and matching effects is given in the following discussion of circuit operation.

**Circuit Operation.** A typical **single-ended** audio power amplifier is illustrated in the accompanying figure. The varying input signal is capacitively coupled through capacitor Cl to the grid of triode VI. Capacitor Cl and resistor R1 form a highimpedance input coupling network. The input voltage is impressed across resistor RI and is applied to the grid of tube V1. The reactance of capacitor Cl to the ac input signal is very small, therefore, the alternating input signal voltage is passed on to the grid with little or no attenuation over the audio-frequency range. Resistor R2 and capacitor C2 make up the cathode-bias circuit. (Refer to the introduction to this section of the handbook for a **detailed** discussion of cathode bias.)



Typical Single-Ended Triode Audio Power Amplifier

The varying voltage applied to the grid of tube V1 causes the instantaneous plate current  $(i_{P})$  to vary through the tube and through the plate-load impedance (primary of transformer Tl). The changing current  $(i_p)$  through the primary of T1 produces **an** ac voltage drop  $(e_{p})$  across the transformer primary, and causes an induced voltage (esec) to appear in the transformer secondary. This voltage (esec) causes current to flow in the load circuit. Thus, the transformer forms an output coupling network. It is important to realize that the transformer merely *reflects* into its primary circuit the load which is imposed on the secondary, and (neglecting internal transformer losses) does *not* place a load on the primary circuit unless a load is applied to the secondary. It is the turns ratio between the primary and secondary, not the number of turns in the primary, which governs the reflected impedance.

The current which flows in the transformer secondary will be larger than the primary current by the turns ratio. For example, in an output transformer which employs a step-down ratio of 40:1, the secondary current will be 40 times the primary current. The secondary voltage, however, will be only l/40th of the primary voltage. Assuming that a primary voltage of 400 volts is generated, the secondary voltage will be only 10 volts. The power transferred will, in the case of an ideal and lossless transformer, be the same in both secondary and primary. For example, assuming a primary current of 20 ma, the secondary current will be 800 ma. Since power equals 4

E x I, the primary power will be 400 x .02, or 8 watts, and the secondary power will be  $0.8 \times 10$  volts, or 8 watts also. Assume a loudspeaker load of 4 ohms; since 1<sup>2</sup>R equals power, a total of 0.64x 4, or 2.56 watts, will be transferred to the speaker voice coil. W-th 8 watts in the primary, this represents about 32 percent efficiency. In a practical transformer, inherent losses will reduce this figure closer to the previously specified nominal value of 25 percent.

As far as the circuit action is concerned, the power amplifier operates in a manner identicrd with that of the Transformer Coupled Triode Audio Voltage Amplifier discussed previously in this section. When a positive signal appears at the grid of Vl, the plate circuit develops a negative-going output. When this output is coupled from the primary to the secondary it will also be negative if so phased. When the secondary winding is connected in phase, the output will be positive for a positive input and negative for a negative input. Otherwise, the primary and secondary are always out of phase. The ability to connect the secondary for the desired phase is one of the advantages of transformer coupling.

To obtain maximum undistorted power output it is necessary to properly match the load to the tube. Here again the transformer offers a convenient matching method by choice of the proper turns ratio between the primary and the secondary. When used for impedance matching, the impedance ratio of primary to secondary varies as the square" of the turns ratio rather than directly, or, stated mathematically:  $N_p/N_s = Z_p/Z_{,,}$  or  $R_{Pri} = (N_p/N_s)^2 R_{sec}$ . Thus, assuming a 40:1 turns ratio, a 1600-to-1 impedance transformation is obtained. With a 4-ohm speaker and a step-up ratio of 40:1 (secondary to primary), the reflected load produced in the primary is 4 x 1600, or 6400 ohms. Such an impedance would be satisfactory as a load for a 3200-ohm plate resistance stage (the load is twice  $R_p$ ).

The example of impedance matching given above again illustrates the primary difference between the voltage amplifier and the power amplifier. While the impedance ratio is step-up for the load, it is stepdown as far as primary to secondary is concerned. Therefore, only a low-voltage can be obtained, but maximum power output with a minimum of distortion is supplied to the speaker. In the event that the amplitude of the grid voltage is held constant, maximum output can be obtained when the load is equal to the tube plate resistance; however, such operation in audio amplifiers is encountered only in special cases, usually where only one frequency rather than a range of frequencies is to be amplified.

The accompanying figure graphically illustrates typical triode plate current and plate voltage characteristics with an assumed load line, from which both power output and harmonic distortion may be determined



Graphic Determination of Power Output and Distortion

Note first that since the  $I_p$ - $E_p$  characteristics are not straight lines and are not equidistant, the current and voltage swings will be unequal, and some distortion will exist. The load line  $R_L$  is drawn equal to the desired load resistance, and the static bias frees operation at the intersection of the  $I_b$  and  $E_b$  lines, where the grid bias is -20 volts. Thus, in the ideal construction, equal positive and negative swings would occur, driving the bias to O and to-40 volts, respectively. The resulting plate current and plate voltage swings represented by  $I_{max}$  and  $I_{min}$  then determine the power output. Neglecting the second-harmonic distortion for the present, It can be shown that Po = 1/8 ( $E_{max} - E_{min}$ ). The illustration shows that with lower load resist-

The illustration shows that with lower load resistance (indicated by line  $R_L$ ) the voltage swings will be smaller and the current swings will be larger than for  $R_L$ , and will be unequal; therefore, the power output will be less and the current continuously increases (since the effective grid then higher plate and bias

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voltages are needed. In this case, as shown by load line R<sub>1</sub>", the plate voltage swings are greater but the current swings are less; thus, the power output is lower, while the distortion is less, since the swings are more nearly equal. For a given tube and plate supply voltage, the desired solution is obtained by adjusting the grid bias. With the proper adjustment, the positive signal peak just takes the total grid voltage to zero, and the negative signal peak just makes the grid sufficiently negative to reduce 1, to its minimum allowable vahre (without operating on the curved lower portion of the tube characteristics.) The accompanying graph shows the variation of power output and distortion with respect to the ratio of the output resistance and the plate resistance for a triode. It is obvious that the most power is obtained when  $R_{L}^{-2}$  $\mathbf{R}_{\mathbf{p}}$ . On the other hand, if a value of 4  $\mathbf{R}_{\mathbf{p}}$  is used, the power drops only 25 percent, but the distortion drops from 7 percent to only 2 percent, which is negligible.





It also can be shown **mathematically** that  $R_L = E_{max} - E_{min}/I_{max} - I_{min}$ . This is a simple Ohm's **law relationship**, which, by substitution in the proper formulas, becomes:

$$R_{L} = 2_{rp}$$

The amount of distortion present is determined from the maximum and minimum plate currents, and is illustrated in the following figure.



**Development of Harmonic Distortion** 

In this figure a triode  $I_p - E_p$  characteristic is shown; with sine-wave voltage  $e_g$  impressed on the grid, the resultant plate current is represented by  $I_p$ . Since the maximum and minimum amplitudes are unequal (the curvature of the characteristic causes partial rectification to take place), the average value of  $I_b$  rises to  $I_b'$  when the signal voltage is applied to the grid. This increase in average current is equal to the amplitude of  $I_b'$ , shown by **b** in the figure. The fun damental component is  $a^{-1/2} (I_{max} - I_{min})$ , while the second harmonic component is  $b = 1/2 (I_{max} + I_{min}) - I_b/2$ ; the percentage of secon<sup>d</sup> harmonic distortion is equal to  $100_{b/a}$ . The rise in average plate current with distortion shows as a fluctuating plate current, with the plate meter wiggling as the signal fluctuates in intensity.

Assuming that the cutoff voltage of the grid is E@, the maximum power **output** of a triode under Class A operating conditions can be estimated roughly in terms of its plate supply voltage and plate resistance by:

# $P = E_{h}^{2}/36 rp$

It is evident from the formula, then, that for moderate plate voltages the internal resistance of the \_

triode *must* be small to obtain relatively large power outputs.

#### Failure Analysis.

**General.** Since the circuit of the single-ended power amplifier is identical with that of the triode transformer-coupled amplifier, the failure analysis listed for the Transformer-Coupled Triode Audio Voltage Amplifier, previously discussed in this section, is generally applicable.

The power amplifier ordinarily operates at higher voltage and current than the voltage amplifier. Therefore, visual evidence in the case of flashovers and short circuits is usually more apparent. Excessive heating of a component usually indicates as incipient failure, since prolonged heating accelerates the aging process. Lack of proper bias is usually indicated by increased plate dissipation. Tube plates showing signs of color indicate excessive loading or current drain. Since the tube is generally working at full capability, lack of sufficient emission can usually be observed by a reduction of output, together with distortion. When trouble shooting the circuit, it is important to be certain that the proper load is connected at the output, otherwise, the tube may appear to be operating normally but be incapable of the proper output. To check for proper operation, apply a sustained tone from an audio generator to the amplifier input. Use an oscilloscope to check the waveform from input to output; any distortion will be immediately apparent. Use a vacuum-tube voltmeter to measure the actual ac input voltage, and substitute a resistor equal in value to the proper load impedance at the output. The ac voltage measured across this resistive load wiU, by use of Ohms' law, indicate the power output  $(P_0 =$ E\*/R).

# SINGLE-ENDED, R-C COUPLED PENTOOE AUDIO POWER AMPLIFIER

### Application.

**The** single-ended, R-C-coupled pentode power amplifier is used in applications where a relatively large audio power output is desired from a small input voltage, and where some distortion can be tolerated.

## Characteristics.

Input impedance is high, usually greater than 0.1 megohm.

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Uses an output transformer to match the load to the output device.

Power sensitivity (ratio of output-power to grid voltage producing it) is relatively high.

Power gain is high, on the order of 8 to 20.

Distortion is normally higher than that of the triode (always more than 5 percent and generally on the order of 7 to 10 percent) unless special design considerations or negative feedback is used.

Operates Class A at all times; no grid current flows under normal conditions.

Cathode bias is usually used, but fixed bias maybe used in some applications.

Frequency response is relatively uniform and linear over a range of 200 to 10,000  $H_z$  without requiring any special design considerations or compensation.

### Circuit Analysis.

**General.** While the single-ended triode audio amplifier is characterized by low power sensitivity, low plate efficiency, and low distortion, the pentode counterpart is just the opposite; it is characterized by high power sensitivity, high plate efficiency, and high distortion. Because of its basically higher distortion, the pentode power amplifier requires more attention to design. Fortunately, however, the increase in power obtainable with the pentode permits the use of various feedback methods, and what essentially amounts to mismatching to attain power outputs equivalent to or greater than the triode with the same distortion. Usually the use of a pentode output stage eliminates the necessity of a driver stage, since the pentode can be adequately driven by small signals.

The screen element in the pentode requires a dc source of power, which does not contribute materially to the output directly and represents an additional constant loss of power (as compared with a triode). Because the  $I_p-E_p$  characteristics are parallel, the amount of second-harmonic distortion is very low, and third-harmonic distortion predominates. Consequently, push-pull operation will not materially help in reducing the distortion. On the other hand, when the load is designed so as to produce more second-harmonic distortion, the use of push-pull operation provides cancellation of this conponent, and the third-harmonic component is also reduced by the load mismatching. See the discussion of Push-Pull Audio Power Amplifiers later in this section for further details on push-pull operation.

As contrasted with the triode, instead of having a load with twice the plate resistance, the pentode uses a load with ONY 1/5 to 1/10 the plate resistance. Such mismatching is necessary because of the extremely high plate resistance inherent in the pentode.

This discussion also applies generally to tetrodes and beam power tubes, except that the secondharmonic distortion of these tubes is greater, more like that of the triode. However, like the pentode, they do have a higher plate resistance and greater over-all distortion, which requires negative feedback or other compensation to provide an acceptable output.

Circuit Operation. The schematic of typical singleended pentode power amplifier is shown in the accompanying figure. The circuit load is a loudspeaker. The varying audio input signal is applied to the grid of pentode VI, through coupling capacitor Cl. Capacitor Cl and resistor R1 make up the input coupling network, and the input signal is impressed across resistor R1. The reactance of capacitor Cl to the ac signal is very small; therefore, the alternating signal voltage is readily passed on to the grid without excessive attenuation. The bias circuit consists of cathode resistor R2 and capacitor C2. (See the introduction to this section of the handbook for a discussion of cathode bias.) As is evident from the schematic, the cathode and the suppressor grid are maintained at the same voltage level, being connected together internally or at the socket (depending upon the type of tube used). The varying input voltage applied to the grid of pentode V1 causes the instantaneous plate current  $(i_p)$  to vary similarly though the tube and through the plate-load impedance (primary of transformer Tl). Capacitor C3 bypasses the screen to ground to prevent the signal voltage from changing the screen voltage at an audio frequency rate. Capacitor C3 is chosen to present a minimum of reactance to the signal voltage; thus, the screen-grid voltage is maintained at a relatively constant dc level. The positive screen-grid voltage is obtained from the plate supply through voltage-dropping resistor R3 to avoid the necessity of providing a separate screen-grid power supply. The changing plate currentt  $(i_p)$  through the primary of T1 produces an audio voltage drop  $(e_p)$ across the transformer primary, and also causes an induced voltage  $(e_{sec})$  causes current  $(i_{sec})$  to flow in the load (output) circuit. Thus, the transformer secondary forms an output coupling network.



Typical Single-Ended Pentode Audio Power Amplifier

As far as specific circuit action is concerned, the operation is identical with that of the Transformer-Coupled Audio Voltage Amplifier Circuit and the Single-Ended Triode Audio Power Amplifier Circuits discussed previously. When a positive signal is applied to the grid of Vl, a negative-going signal is developed in the plate circuit, and coupled from the primary to the secondary of T1 as a negative-going output signal if T1 is connected in-phase. When a negative signal is applied to the grid, a positive-going amplified signal is developed in the plate circuit, thus inducing a voltage in the secondary of T1. When connected in-phase, the secondary output is positive for a positive input signal and negative for a negative input. Otherwise, the primary and secondary voltages and currents are always out-of-phase.

To obtain maximum undistorted output, it is necessary to properly match the load to the tube. The transformer offers a convenient method of accomplishing load matching since the impedance ratio of primary to secondary varies as the square of the turns ratio, rather than directly. Stated mathematically,  $Z_{pr} = (N_p/N_s)^2 Z_{sec}$ . Thus, with a transformer having a 50:1 turns ratio and a 4-ohm loudspeaker load, the primary would reflect a load of 2500 times the secondary impedance, or 10,000 ohms. Such a load is suitable for matching pentodes having a plate resistance of 50,000 to 100,000 ohms, with the least distortion being obtained from the higher-plateresistance tubes. The manner in which the output power varies with the ratio of the load and plate resistance of a typical pentode, together with the amounts of distortion produced, is graphically illustrated in the following figure.



Typical Power Output and Harmonic Distortion Relationships

The large amount of second-harmonic distortion at high load impedances shown in the graph occurs because of the crowding together of the typical pentode plate characteristics at low plate voltages. This causes a greater in change during the negative peak than during the positive peak of the output waveform, thus tending to flatten the positive peak. During the interval over which the negative and positive swings are equal, practically no second-harmonic distortion occurs. The large amount of second-harmonic distortion with low load impedance is caused by the unequal spacing of the plate characteristics at low plate currents, which tends to flatten the negative peak of the alternating plate current. Because the load for maximum power output is different from the load for minimum distortion, the choice of the load is a compromise between the amount of power output desired and total distortion that can be tolerated. The load is

usually chosen so as to produce minimum secondharmonic distortion. While it is possible with some tubes and designs that optimum power output may occur at the point of minimum distortion, this is the except rather than the rule. Because of the extreme variations between tube types, simple design formulas like those used for the triode are not obtained; therefore, most of the design must be determined graphically.

The accompanying figure shows the  $I_p$ - $E_p$  characteristics for a typical pentode with the proper load line. In this example the plate resistance is 60,000 ohms and the load is 7000 ohms.



Typical PentOde  $I_p = E_p$  Characteristics and Load Line

Examination of the plate characteristics reveals that for equal grid swings, equal plate current swings are produced with the 7000-ohm load line. It can easily be seen **hat** if the load line were drawn with less slope (for example, an increased load resistance of 9000 ohms, shown by dotted load line),  $I_{max}$ would be less than  $I_{max}$ , and if the load were increased further the maximum current would change greatly while the minimum would remain practically the same. As a result, second-harmonic distortion would be increased. It is important with pentodes, therefore, to prevent the load from increasing with frequency, as normally happens when a loudspeaker is the load. To minimize this increase in distortion of

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the higher audio frequencies, a capacitor connected in series with a resistor is used in shunt with the transformer primary (in some cases it is in the form of a tone control, and in other cases only a shunting capacitor is used). The variation of the effective loudspeaker impedance with frequency when the RC network is not used is shown by the solid curve (a) in the following graph, and the variation when the RC network is used is shown by the dashed curve (b). Because of the high plate resistance of the pentode, the effective resistance shunting the loudspeaker is less than that for a triode. This reduction of damping on the speaker sometimes causes objectionable "booming" because of resonances which otherwise would be subdued (damped out). It is also of interest to note that the screen grid of a power pentade is not as effective (as compared with a voltage pentode) in shielding the control grid from the plate. As a result, the plate-to-grid capacitance is larger than in the voltage pentode. In addition, because the control-grid connection is made through the base rather than through a tube cap, the grid-to-cathode capacitance is also larger. Therefore, the total effective input capacitance of the power pentode may sometimes be considerably larger than that of the power triode. The result is to produce greater frequency distortion in the preceding amplifier stage. Because of these facts the over-all distortion is so large that negative feedback is practically mandatory to keep the distortion



Variation of Loudspeaker Impedanee with Frequency

within acceptable limits if the full power output of the pentode is required.

While it is possible to eliminate the cathode bypass capacitor (C2 in the schematic) and thus obtain degeneration to help reduce the distortion. It is usually easier to use negative feedback. Because of the high gain in the pentode, a larger cathode bypass capacitor is required than in a triode amplifier.

Although the load line as discussed above was considered to be a straight line for convenience, in actual operation the dynamic load line is not straight, but varies in accordance with the reactive component of load impedance in the circuit. The result is to shift the operating point slightly about the bias value assumed for the ideal condition, particularly when self-bias is used. With proper design this is of no consequence, since the circuit is arranged to produce equal shifts for the positive and negative grid swings. If unequal shifts are permitted to occur, however, the effect is to obtain performance entirely different from the assumed values of plate current, voltage, bias and, grid drive, with greater distortion and phase shift. Thus, the gain, output, and response characteristics may sometimes be entirely different from those which are assumed or calculated.

## Failure Analysis.

**No Output.** A no-output condition is normally caused by the lack of an input signal, an opencircuited condition, lack of plate or fdament voltage, a short-circuited condition, or a defective tube. The presence of an input signal can be determined by checking the input with an oscilloscope or vacuumtube voltmeter. An open-circuited condition can be localized to the defective portion of the circuit by making voltage measurements to determine whether the fdament, cathode, grid, plate, and screen voltages are present and are normal.

An open cathode circuit will cause a **no-output** condition. With an open input circuit (Cl or RI open), the high gain and high impedance of the **pen**-tode may permit a slight output; however, for all practical purposes the output will be so low that it can be considered nonexistent.

If the screen shows color and the plates does not, it usually indicates that the screen is attempting to act as the plate because of an open plate circuit. In this case the plate voltage will be zero. An open screen resistor, R3, or shorted screen bypass capacitor, C3, will also cause a no-output condition. In either case no voltage will appear on the screen of the tube. An open screen resistor will be cool. With a short-circuited bypass capacitor, since the screen resistor will be dropping the full voltage from the plate supply to ground, it will be abnormally hot and probably will eventually bum out; a visual inspection will normally show discoloration or even smoke in this instance.

With an input signal present and normal tube voltages, either the tube is defective or the transformer **secondary** is open. Replace the tube with one known to be good, and check the secondary for continuity with an ohmmeter.

Reduced or Unstable Output. Reduced output is usually caused by improper bias, or low plate or screen voltages. Unstable output is usually caused by oscillation, or by intermittent functioning of circuit components. An open cathode bypass capacitor, C2, will permit sufficient degeneration to reduce the output appreciably, as will an open screen bypass capacitor, C3. If the bias is excessive or if cathode bias resistor R2 has increased in value, the output will also be reduced, depending upon the amount of change. If the screen resistance increases in value or by-pass capacitor C3 becomes leaky, the increased voltage drop across R3 will produce a lower screen voltage and thus reduce the output by reducing the maximum plate swing. If the reflected load impedance is too high, the output will also be reduced. A shorted input coupling capacitor, Cl can place the plate voltage of the preceding stage on the grid of VI, cause increased plate and screen current, increase the cathode bias, and reduce the output. (In some cases it can cause complete cutoff.)

With all voltages normal, the trouble is most likely in the electron tube; reduced emission will cause a loss of output, particularly on the signal peaks when more electrons are needed to increase the plate current.

Unstable output can result from intermittently open or shorted components, and can usually be located by using an oscilloscope to follow the waveform through the circuit. Oscillation can also cause erratic response. If it occurs at radio frequencies, it will show on the oscilloscope as a fuzzy pattern; if the feedback is at an audio frequency, it will be observed as a separate audio frequency. Oscillation will also show in the output as a howl or squeal, or as a very low-frequency "put-put" (motorboating). Howl or squeal is usually caused by undesired coupling between the plate and grid circuits. Motorboating is usually caused by faulty bypassing (in the power supply or B+ leads), particularly where electrolytic capacitors are used; electrolytic capacitors tend to dry out with age and lose their capacitance.

Distorted Output. Improper bias or improper load matching is a common cause of distortion. Check for proper plate and grid voltages. Lack of sufficient emission in the electron tube will also cause distortion on the signal peaks. Where the voltages are normal and the load is correct, the tube is probably at fault; it should be replaced with a tube known to be good. Use an oscilloscope and audio signal generator to follow the waveform through the circuit. Flattening of both positive and negative signal peaks indicates overdrive (too large an input signal). Flattening of the negative peaks indicates excessive bias or low plate voltage; this symptom can also be caused by low screen voltage. Too low a bias or too high a screen voltage is usually indicated by flattening of the positive peaks. Check the frequency response characteristics. Rounded-off peaks on sine waves or sloping sides or tops on square waves indicates loss of lowand high-frequency response. A 2000- to 3000-Hz square wave applied to the input will provide a signal which can indicate the relative harmonic response over a range of 5 to 10 times this frequency (the square wave is composed of many sine-wave frequencies).

Hum distortion can be observed directly on the oscilloscope. When hum is present on the power leads, lack of sufficient power-supply faltering is indicated. If it is not on the power leads, but is evident on the grid, plate, or cathode leads, check for induced hum due to the nearness of ac leads in the wiring. Additional checks should be made to insure that the transformer is properly grounded and that the shielding is adequate.

# PUSH-PULL AUDIO POWER AMPLIFIER (ELECTRON TUBE) (CLASS A, AB, AND B)

## Application.

The push-pull audio power amplifier is used where large amounts of undistorted audio power are required. This circuit is commonly employed in receiver output stages, in hi-fi and public address systems, and in AM modulators.

#### Characteristics.

Power gain is moderately high, on the order of 4 to 10.

Requires twice the drive of a single tube.

Power output is more than twice that of a single tube (about 2-1/2 times).

Second and higher even-order harmonic distortion is cancelled out in the plate circuit.

Distortion varies with the class of operation; it is minimum for Class A operation, and greatest for Class B operation.

Plate efficiency varies with the class of amplifier; it is lower for Class A operation, highest for Class B operation, and intermediate between the two for Class AB operation.

Cathode (self) bias is normally used for Class A or AB operation, but fixed bias is usually used for Class B operation. (Specially designed Class B tubes requiring no bias are sometimes used.)

Cathode bypass capacitor is usually omitted in Class A stages, but is included in Class AB stages,

### **Circuit Analysis.**

General. In push-pull operation, the plate current of one tube is increased, while that of the other tube is simultaneously decreased, and vice versa. As originally conceived, one tube was considered to be pushed while the other tube was pulled; hence the term push-pull. While this is true of Class A or Class AB operation, it is not strictly true of Class B operation. Class B amplifiers utilize the push-pull circuit; however, one tube effectively amplifies only the positive portion of the input signal, while the other tube amplifies only the negative portion. This occurs because only one tube conducts at a time, while the other tube is cut off. Push-pull stages require twice the grid drive of single-ended stages; however, each tube may be driven to its full capability, and usually more than twice the output possible with a singleended stage is supplied. Distortion is reduced because the even-order harmonics are cancelled out. For triodes, this provides a maximum reduction of distortion. For pentodes, since the second-harmonic distortion is small or negligible, only a slight reduction in distortion is obtained. However, with special design in which the pentodes are loaded so that they produce more than normal secondharmonic content, a reduction in both second- and third-harmonic distortion is achieved. With the beampower tube, distortion is also reduced since this tube

has a large second-harmonic content than the pentode, although not as great as the triode.

Since in a balanced push-pull amplifier the plate currents are equal and opposite, dc saturation effects on the core are eliminated; this permits more efficient transformer design, together with a reduction in both amplitude and frequency distortion. Actually, only 40 percent more turns in the primary (as compared with single-ended stages) are needed to handle two tubes in push-pull. Thus, the transformer design is economical. With a balanced input and output, any hum present in either the input or in the output tends to cancel out. This, together with the reduction in harmonic distortion, provides better audio quality.

With triodes, usually Class A or Class AB operation is employed, and the drive is such that no grid current is drawn. With pentode or beam-power tubes, usually Class B operation is used, and some grid current is drawn. As a result, Class B stages usually require power diver stages, while Class A or AB stages require only voltage driver stages.

**Circuit Operation.** A typical push-pull circuit using a minimum of components is shown in the **accom**panying figure. For ease of explanation, fixed bias is assumed. (For a discussion of circuit biasing methods, refer to the introduction to this section of the handbook.) The circuit load is a loudspeaker.



Typical Triode Push-Pull Audio Power Amplifier

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It is evident from the schematic that the grids of VI and V2 are biased equally negative with respect to the respective cathodes. With no input signal applied to T1, the tubes rest in their quiesent (static) state, and equal but opposite dc currents flow in the two halves of the primary of T2. The steady flow of dc current does not induce a voltage in the secondary of T2, since the current in each half of the primary is equal and opposite in direction, and the magnetic flux around the primary cancels. Thus the core is not subjected to a continuous magnetizing force. Consequently, the possibility of dc core saturation is minimized (for a specific core, any dc induced flux adds to the ac induced flux produced by a signal, and thus limits the total amount of flux that can be carried through the iron without saturating). As a direct result, a higher primary inductance is obtained with the same number of turns. On the other hand, when saturation occurs the inductance is reduced just as if the core size were reduced, and this changes the load impedance and creates distortion. The reduction in saturation effects is an inherent advantage of the push-pull circuit. When an input signal is applied to the primary of transformer T1, equal but opposite voltages are induced-in the secondary (the schematic shows the instantaneous polarities or one half-cycle of operation; during the other half-cycle they are oppositely polarized). Therefore, when the plate end of T1 is positive the grid of VI is driven positive, while the grid of V2 is driven negative (assuming that T1 is connected in-phase). The alternating drive voltages,  $e_{g1}$  and  $e_{g2}$ , are equal and are connected in series with bias voltage  $E_{cc}$ . Assume for the moment that the drive voltages are just equal to the bias. It is evident, since they are of opposite polarity, that V1 will conduct heavily (the bias is reduced to zero), and V2 will be biased twice normal, or to zero plate current. The heavy current flow through the primary of T2 to the plate of V1 produces a maximum voltage drop across the load, reducing the plate voltage of VI to its minimum value. The flux produced by the flow of ac plate current through T2 induces a voltage in the secondary in accordance with the turns ratio of the transformer (the relationship of transformer turns ratio, impedance, and power output will be discussed in more detail in a following paragraph). The secondary of T2 is assumed to be connected out-ofphase with the primary, so that the polarity of the output for the half-cycle discussed above is positive, as shown in the schematic waveforms.

When the plate current of V1 decreases (on the other half of the cycle), the plant current of V2 increases. The altercating currents in the primary of T2 are in phase while the dc currents and their resulting voltage drops are opposing. The net result is that the magnetomotive force produced by the two halves of the primary is zero with no signal impressed. With an input signal applied, the plate current of the two tubes is equal to a current equivalent to the difference in the current flowing in tube VI and tube V2, both flowing through one half of the primary winding. For example, assume a quiescent current of 30 milliamperes and a drive signal that causes one tube to increase 10 milliampere instantaneously. Since the grid swings are equal and opposite, the plate current of the other tube is reduced. For ease of discussion also assume that the tube characteristic  $E_g$ - $I_p$  curves are exactly identical (in practice they are slightly different). Then, the reduction of plate current in the second tube will be exactly 30 minus 10, or 20 milliamperes. With an upward swing of 10 ma to 40 ma, the difference in current between the two tubes is 40 minus 20, or a total 1<sub>p</sub> of 20 ma, which is exactly double that of one tube. With a unity turns ratio between each half of the primary and the secondary, equal a-f voltages are inducted in the output. Since they occur simultaneously and are in-phase, they are effectively series-connected and the output voltage is doubled. The same effect would be produced by the difference current (20 ma) flowing through one-half of the primary. Consequently, the dynamic characteristic for two tubes operating in push-pull is constructed by subtracting the currents through the two tubes in order to approximate the effect of the transformer.

Class **A Operation**. The accompanying dynamic characteristic curve illustrates Class A operation. The dotted curve labeled VI represents the dynamic characteristic of one tube, while the dotted curve labeled V2 represents the dynamic characteristic of the other. Both of these characteristics are assumed to be identical. Although the dynamic characteristics of the individual tubes are curved, the resultant pushpull characteristic is straight. As is evident from the figure, the dynamic characteristic for Class A pushpull operation is extended over that for a single tube, and is even more linear. Thus, greater grid-signal, plate-current, or plate-voltage swings are possible without any noticeable increase in distortion. With a greater swing, greater power output is obtained. By

projecting the various points of the grid (input) signal to the solid-line, push-pull characteristic shown in the figure, the output waveform is obtained.



#### Dynamic Characteristic Curve for Class A Oparation

The output transformer turns ratio and load impedance relationships in the push-pull amplifier are based upon a unity turns ratio of secondary to onehalf of the primary. Thus, when the whole primaryto-secondary turns ratio is considered, that is, the plate-to-plate load, the ratio is 2 to 1. Since the transformer impedance between the primary and secondary varies as the square of the turns ratio, a 4-to-1 impedance transformation is obtained. For example, with a 1000-ohm load across the secondary, the plate-to-plate load is 4000 ohms, and the individual tube load is 1000 ohms. The proper load for a particular tube varies in accordance with the design and class of the amplifier, and is beyond the scope of this handbook. The effectiveness of the push-pull circuit results basically from the elimination of second-harmonic distortion, which permits the tube parameters to be increased much beyond those of the single-ended stage for an equivalent amount of distortion, thus providing a much greater power output. Another reason is that the apparent internal plate resistance of the push-pull combination is much lower than that of a single tube (on the order of rp/2).

Therefore, with the same voltage and bias as that of a single tube, the lower dynamic plate resistance permits much greater output. In addition, the amount of distortion does not increase greatly when the tubes are driven to zero bias or even into the positive region. Therefore, Class B operation becomes feasible, and is used where large amounts of audio power are desired.

The manner in which second-harmonic distortion is eliminated can be more easily visualized if the accompanying equivalent circuits are examined. Part A of the figure shows the fundamental and odd-order



A - ODO - ORDER HARMONICS



**B-EVEN -ORDER HARMONICS** 

Simplified Push-Pull Equivalent Circuits



Distortion and Power Output Variation with Load Resistance for a Typical Push-Pull Amplifier

equivalent circuit, while part B shows the second and even-order harmonic circuit. Note that in part A of the figure  $\boldsymbol{i_p}$  flows in the same direction through the primary of T2; thus the fundamental and odd-order harmonics induce an output in the secondary and appear across  $\mathbf{R}_{\mathbf{L}}$ . The current flow is in opposite directions through the power supply, however, so that the fundamental cannot appear as feedback through the common supply impedance; thus oscillation from this cause is prevented. In part B of the figure the flux in the primary developed by  $i_{\mathbf{p}}$ cancels, and, while the second-harmonic current does exist in the primary, it does not appear in the secondary as long as the circuit is balanced. Even with an unbalanced current, however, any second-harmonic output is considerably reduced. The reduction of second and even-order harmonics also contributes to a much reduced third and odd-order harmonic content. Since the second and third harmonics produce most of the distortion encountered in the amplifier circuit, the push-pull amplifier automatically provides a much larger undistorted output than that of the single-ended stage. The manner in which the output power and third-harmonic distortion vary in accordance with the plate load for a typical two-tube push-pull amplifier is shown in the accompanying figure. The tube types, plate voltage, bias, and grid drive are the same as those used in a similar graph shown in the discussion of the Transformer-Coupled Triode Audio Power Amplifier, discussed previously in this section of the handbook. Comparison of these charts shows almost a threetime power increase over that of a single tube for the

same load resistance, with a total absence of secondharmonic distortion and very little third-harmonic distortion.

Class AB Operation. In Class AB push-pull operation, sometimes referred to in other texts as Class A prime operation, the grid bias is increased over that of Class A operation, and plate current does not flow during the entire 360 degrees of the cycle. During the peak grid excursions, therefore, some rectification of the grid signal occurs when the plate current is interrupted, causing distortion and high peak plate currents. With self-bias this increases the bias during the peaks and produces nonlinearity, which is the main cause of the increased distortion. With fixed bias the abrupt change which occurs with self-bias is not encountered, and the distortion is less. This occurs because there is no abrupt increase in plate (cathode) current to produce the bias change; instead, the bias at the peaks is determined by the resistance in the grid circuit and any grid current flow so that the change is proportional to the signal increase, it is somewhat more linear, and less amplitude distortion is created. Therefore, self-bias is usually avoided in Class AB operation, Regardless of distortion effects, however, the increase in bias (over that of class A operation) at a particular plate voltage reduces the total operating current and the plate dissipation. Therefore, the efficiency in the plate circuit increases and greater power output is obtained. If desired, the plate voltage (for triodes) many be still further increased to restore the plate dissipation to the full rated value with still greater output. For this reason, Class AB operation is generally referred to Class A operation where power output is the main consideration and a slight increase in distortion can be tolerated. Since the plate current range, and hence the cathode current (in self-biased operation), is greater than that of Class A operation, a slight unbalance between the tubes usually occurs. Therefore, a cathode bypass capacitor is generally used in selfbiased Class AB operation to prevent degenerative effects due to this unbalance. Although matched tubes are desirable, whether or not cathode bypassing is used, it is considered to be more economical and practical to provide a current-balancing control in the bias circuit and to use unmatched tubes. Actually, for Class A or AB operation, it is only necessary to match the quiescent value of current to obtain a balance within 10% over the operating range.

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The dynamic characteristic of Class AB push-pull operation is obtained in the same manner as that of Class A push-pull operation. A typical characteristic curve would show that the bias is closer to the platecurrent cutoff value than is true of the Class A pushpull circuit. In addition, the resultant characteristic is linear over a greater length as compared with Class A operation. This result is less distortion and greater plate efficiency. Maximum efficiency for Class AB operation is on the order of 50 to 55 percent.

**Class B Operation.** A typical dynamic characteristic curve for Class B operation is shown in the accompanying figure.



### Typical Class B Dynamic Characteristic Curve

Note that the bias is higher than that for Class AB operation and is nearer to, but not quite sufficient to cause, plate current cutoff. This, a slight idling (static) current exists with no input signal. With the greater bias, a greater drive signal is required. Since the grids are usually driven positive and grid current is drawn (that is, Class B operation), a power-driver stage is necessary.

Because grid current flows on the peaks of the input signal, a low-impedance grid circuit is necessary, and is usually provided by using a step-down turns ratio from the primary of the input transformer to the secondary. This also has the effect of reducing the internal plate resistance of the driver tube, and produces better over-all voltage regulation to help diminish distortion on the peak input signal swings. While the circuit operates in a manner similar to that of a Class A or AB push-pull amplifier, it differs in the only one tube is operative at a time. It can be seen, then, with each tube operating separately, that large fluctuations exist in the plate current and voltage, as well as grid current and voltage, and wellregulated power and bias supplies are necessary to avoid distortion. The distortion is caused by flattening of the peaks due to poor regulation. Since the plate current, and hence the cathode current, fluctuates greatly, self-bias is impracticable, and fixed bias is used; in some applications special hi-mu Class B tubes designed to operate at zero bias with very small plate current flow are used. Because only a small static plate current is drawn when no input signal is present, the average plate current is less than that for Class A operation, even though the plate current swing is greater. This is the reason for the higher efficiency produced by the Class B push-pull amplifier. For example, it can be demonstrated that with a plate efficiency of 60%, the power output is 1.5 times the plate dissipation. On the other hand, for a Class A stage operating at 25% efficiency, the power output is only .25 of the plate dissipation. Thus, it is possible to obtain six times as much power output from the same tube in Class B operation as in Class A operation.

Because each tube of the Class B push-pull amplifier operates on alternate half-cycles, the cancellation of the second-harmonic component (a feature of the Class A or AB push-pull amplifier) does not exist (except for the period during which both tubes operate). Harmonic distortion at the input is transmitted in amplified form to the output. Any secondharmonic distortion generated in the stage is also induced in the secondary of the plate transformer. This occurs because the only time that flux exists in the core of the output transformer from both tubes is during the small idling period between signals or during static operation. Class B operation also tends to produce second-harmonic distortion because the dynamic characteristics of each tube is not affected by the other tube's plate current; these currents occur separately during opposite half-cycles (unlike the

Class A or AB stage, where one current is coupled to - the other by flux produced by simultaneous current

flow in the primary of the plate transformer). Regardless of the tendency toward distortion, the operation of the two tubes "back to back" in the push-pull circuit permits selection of the straight-line portion of the dynamic characteristic for operation. Since operation in this region is linear, second-harmonic distortion is effectively eliminated. However, if operation occurs in the nonlinear region beyond this, or if the tubes are mismatched badly (10% difference in current will produce 570 distortion), then secondharmonic distortion will be produced and the effectiveness of the push-pull connection will be lost. Despite the apparent disadvantages of Class B operation, when careful attention is paid to design much greater output is obtained with not too much additional distiotion. Therefore, Class B operation is universally used for high-power audio applications, particularly for transmitter modulator stages. Practically, efficiencies on the order 60 to 66% are obtained, although the theoretical maximum efficiency possible is n/4, or 78.5 percent.

The accompanying figure shows typical waveforms developed in the Class B amplifier over two cycles of operation, and clearly illustrates the current and voltage relationships. In part A of the figure the input (grid) signal is shown as a sine wave, with an amplitude sufficient to exceed cutoff bias E<sub>c</sub> and drive the grid slightly positive. Half-cycles (1) and (3) are identical, as are (2) and (4). However, the odd and even half-cycles are 180 degrees out of phase with each other. As the input signal swings positive, plate voltage  $E_{b}$  is reduced by the drop across load  $E_{L}$ until the peak value of input signal is reached. This corresponds to E<sub>min</sub>, as shown in part B of the figure. Simultaneously, as shown in part C of the figure, the plate current of tube V1 increases to value Imax at the peak of the signal. As the input signal recedes and falls to the cutoff bias value,  $E_{t}$  decreases to zero (supply value of  $E_{h}$ ) at cutoff. At this time, the plate current is at a minimum rather than zero, the plate voltage is that of the supply, and the drop across the land is zero. Actually, this is the time when idling or static current exists, and is some small value other than zero; it is indicated by the overlap of the current waveforms in part D of the figure. Part D also shows the plate currents for the two tubes, where  $i_{p_1}$  is that for V1 and  $i_{p_2}$  is that of V2. Current  $i_{p_2}$  is shown dotted since it is 180 degrees out of phase with  $i_{n}$  and occurs during the time V1 is cut off. With matched tubes these waveforms are identical,

and with unmatched tubes they vary slightly. (A 100% current difference will produce approximately 5% harmonic distortion.)

The waveform for V2 is produced in exactly the same manner as that for VI by the even-order half-cycles, (2) and (4) in the figure, while (1) and (3) keep VI nonconducting. Part E of the figure shows the output voltage in the secondary of the plate trans-



Typical Class B Current and Voltage Waveforms

former. The positive and negative swings are produced through the primary on alternate halfcycles of operation. Thus, the output voltage is similar to the input voltage and is twice that produced by one tube.

For small-amplitude input signals, operation occurs around the point of idling or static (zero) current. In this region the characteristic of each tube is extremely nonlinear and much distortion occurs. However, when large input signals are applied, this area represents only a small fraction of the range; hence its effect is negligible. This nonlinearity at the zero bias point, plus that caused by grid current flow, and unmatched plate currents caused by a difference in tube characteristics, add together to increase the total harmonic distortion. Thus, the Class B amplifier alsways has more inherent distortion that either the Class A or AB amplifier.

**Other Considerations.** A special form of Class B operation is that known as Class B *quiesceru* operation. In this case the operation is  $B_1$ , that is, the grids are never driven into the positive region. This type of operation is essentially similar to Class AB operation, except that the bias is higher. Because the grids are not driven positive, Iess distortion is produced and less driving power is required. However, the extremely large output obtained with  $B_2$ operation is not possible; thus it finds rather limited use. Since the theory of operation is similar to those types discussed above, it will not be further explained in this handbook.

Because of the extremely large fluctuations of current and voltage which occur in the typical Class B amplifier, and because some tubes exhibit a negative resistance effect over part of the cycle, transients may be produced and parasitic oscillations sometimes occur in the grid or plate circuits. These undesirable effects are eliminated by placing small bypass capacitors between the cathode and grid or across the primary of the plate transformer. In some instances, in the plate circuit, a series R-C combination may be placed from plate to plate. In such cases, these components act as simple high-pass filters to reduce transient response. They are not essential to the operation of the circuit, and serve only to prevent the possibility of undesired parasitic. The insertion of these components and the determination of their values are design problems not concerned with circuit operation.

## Failure Analysis.

No Output. Lack of an input signal, defective input or output transformers, lack of plate or filament voltage, or a defective tube can cause a nooutput condition. The presence of plate or filament voltages can be determined by a voltage check. Use an oscilloscope or a vacuum-tube voltmeter to determine whether an input signal exists. Follow the signal through the circuit; when the signal disappears, the trouble will be localized. While an open input winding (Tl primary) will prevent the development of an output signal, either secondary may be open without stopping operation; in this case the circuit will operate on one tube with reduced output. Likewise, in the plate transformer (T2), while an open secondary will prevent any output, an open primary will not (unless both halves are open). Loss of plate voltage on one tube with normal supply voltage indicates that half of the primary is open. One defective tube will not prevent output; however, if both tubes are defective there will be no output. While short circuits across the input can cause loss of output, it is rather unlikely except where capacitors are placed from grid to cathode or from plate to plate in order to prevent transients and parasitic. If such capacitors are used and no output is observed, the capacitors are probably shorted. A resistance check of the windings with the power off will indicate continuity; a resistance reading of less than 1 ohm will probably indicate a short circuit.

Reduced Output. Many conditions can cause reduced output. The most common cause is loss of amplification in one tube. This condition can result from a defective tube, loss of filament or plate voltage, or a short circuited condition. Remove one tube and then the other. If one half of the circuit is operative, the output will be reduced considerably or cease entirely when the good tube is removed. If the tube removed is defective, the output will not change; it may even increase. Loss of plate voltage to one tube can be determined by a voltage check. Visual indication such as the plate showing color indicate excessive plate dissipation in the good tube. However, this *is* only a relative check, since a short circuit can also exist in the tube showing color. An oscilloscope waveform check will show definitely whether one tube is operating normally, but not the other tube. If this is the case, the plate voltage and bias may be

checked on the inoperative tube to determine the fault.

With normal plate, filament, and grid voltages but with reduced output, the trouble is either a tube (or tubes) or a short-circuited (grounded) transformer winding. Check the output load or device, since improper loading will cause reduced output.

Distorted Output. Improper bias, plate voltage, or load impedance, as well as overdrive, will cause distortion. Distortion resulting from poor frequency response may be caused by poor transformer construction, and also by improper loading. If the transformer is defective, replace it. Also, examine the load to make certain that it is of the proper value. Check for the proper bias and plate voltage with a highresistance voltmeter. Use an oscilloscope to determine the grid drive and observe the waveform. Excessive second-harmonic content in a Class B amplifier indicates distortion in a previous stage, or nonlinearity of a tube (or tubes). Check the tube for matched currents, or substitute a pair of tubes known to be matched and note whether the response improves. With matched currents (linear response), very little second-harmonic distortion will be present. With unmatched tubes, a 105% difference in currents can produce as much as 5% distortion. In a Class A or AB push-pull amplifier, second-harmonic distortion indicates that the tubes are improperly loaded or that one tube is defective, since this type of distortion will cancel out in the secondary if the circuit is operating normally. If balanced adjustments for bias and plate current are provided in the equipment, a readjustment will probably return the operation to normal. Operate Class A or AB stages with one tube in the circuit at a time and note on an oscilloscope whether both circuits perform identically, observing the waveform at both the input and the output. The source of distortion should be obvious. When Class B stages are operated with one tube only, the output will be highly distorted; both tubes are necessary to minimize distortion.

# PUSH-PULL AUDIO POWER AMPLIFIER (SEMICONDUCTOR) (CLASS A, AB, AND B)

### Application.

The push-pull transformer-coupled transistor audio amplifier is used where high power output and good

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fidelity are required. For example, it is used in receiver output stages, public address amplifiers, and AM modulators.

#### Characteristics.

Collector efficiency is high with moderate power gain.

Requires twice the drive of a single transistor stage.

Power output is more than twice that of the single transistor stage.

Second and higher even-order harmonic distortion is cancelled.

Distortion varies with the class of operation; it is least for Class A operation, and greatest for Class B operation.

Collector efficiency varies with the class of amplifier, from 50 percent maximum in Class A to 78 percent maximum in Class B, with an intermediate value for Class AB.

Fixed bias is usually used, but self-bias may be encountered in some Class A applications.

Operates as a large-signal amplifier for all except very small inputs.

Emitter swamping is used for thermal stabilization.

## Circuit Analysis.

**General.** The semiconductor push-pull audio power amplifier is similar to the electron tube version discussed previously in this section of the handbook. Use of the common (grounded) emitter circuit allows use of the analogy that the base of the transistor is equivalent to the electron tube grid, the emitter equivalent to the cathode, and the collector equivalent to the tube plate. Examination of the accompanying schematic reveals that the transistor pushpull circuit is practically identical to the electron tube push-pull circuit. Any differences are due to the transistor internal parameters and the matching requirements to obtain maximum power output with minimum distortion.

Push-pull amplifiers can be operated Class A, Class AB, or Class B, as determined by the amount of forward bias. Like the electron tube push-pull circuit, the least amount of distortion and power output is produced in Class A operation, and the greatest amount of distortion and power output is obtained in Class B operation. Class AB stages operate between these levels of distortion and power output. For a given equipment and type of transistor, selection of the operating bias, distortion, and power output is a design problem. The following discussion will cover each type of operation; although the different types of operation are similar, there are significant differences amont them.

**Circuit Operation.** The following schematic shows a PNP push-pull, transformer-coupled output' stage. The load resistance may be a loudspeaker, a Class C r-f stage, or other type of load. The load is considered to be resistive unless stated otherwise in the text.



## Push-Pull Transformer-Coupled Translator Power Amplifier

The input signal is applied to the base of both transistors through transformer T1. The polarity for the positive half-cycle of input is shown on the schematic to facilitate proper understanding of the operation. Note that when the top end of the secondary of T1 is positive, the bottom end is negative. Thus, equal and oppositely polarized signals are applied to the base of transistors QI and Q2 when an input signal appears in the primary of T1.

The input signal is obtained from a preceding driver power amplifier stage. Very little power is required for Class A **operation**; increasingly more drive power is required for Class AB and Class B operation. The actual amount of drive power needed depends upon the circuit design and the transistors used; it is on the order of 2 or 3 percent of the output. Transformer input coupling is used to provide maximum drive power and proper matching of the driver stage. Fixed bias from the collector supply is applied through voltage divider resistors R1 and R<sub>B</sub>. Resistors R<sub>E1</sub> 'and R<sub>E2</sub> are the emitter swamping resistors, which are left unbypassed to provide a slight amount of degeneration. Refer to the introduction to this section of the handbook for a discussion of bias arrangements and bias stabilization methods. The collector load consists of the primary resistance of output transformer T2 plus the resistance reflected from the load connected across the secondary.

Class A Operation. With no input signal, the stage is resting in its quiescent condition, drawing heavy collector current and operating at the point of lowest efficiency. Since no change in collector current occurs, no output voltage is induced in the secondary of T2. Assuming a positive input swing on the base of Q1 and an in-phase connection of Tl, the positive voltage of the signal subtracts from the normal forward (negative) bias, effectively reducing the base bias and causing less collector current to flow in Q1. As the collector current is reduced, the changing lines of magnetic flux between the primary and secondary of T2 induce a voltage in the secondary. At the peak of the input signal, the collector current of Q1 is reduced to a small value, and the collector voltage approaches the supply voltage (reaches its most negative value). Thus, the common emitter circuit makes the polarity of the output signal opposite that of the input signal. Simultaneously, the input signal in TI is applied as a negative voltage swing to the base of Q2 (the ends of the secondary winding are oppositely polarized when a voltage is induced), which adds to the forward bias of Q2. The increase in forward bias causes an increase in the collector current through the primary of T2, and induces an in-phase voltage in the secondary of the output load.

The net result of the input signal is to decrease the signal output of Q1 and to increase the output of Q2. These induced output voltages are combined in the secondary of T2 to produce the effect of a collector current equivalent to twice that of a single transistor. Note that this action is the same as the action that occurs in the electron tube push-pull circuit. In the same manner, the collector-to-collector (plate-to-plate) load impedance is also four times the load, since the primary-to-secondary turns ratio is based on a one-to-one ratio of half the primary to the secondary.

During the negative half-cycle of input signal excursion, the opposite action occurs. The negative

signal adds to the negative forward bias and increases the collector current of QI. Meanwhile, the base of Q2 is driven positive at the same time Q1 is driven negative. The positive increase in the input signal reduces the forward bias and causes the Q2 collector current to decrease. Again, the net result is the same as if twice the collector current of a single stage were involved in flowing through T2. Note also that the collector current flows in opposite directions through the two halves of the primary of T1, so that any in

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Elimination of 2nd Harmonic

phase primary-induced voltage components are cancelled out (second and all even harmonics); thus, the output voltage unduced in the secondary consists of the fundamental component and any odd harmonics. The manner in which the second-harmonic component is cancelled out in the secondary is shown in the following illustration. In part A of the figure, the positive signal is enhanced by the second harmonic, while the negative signal is reduced. In part B, the opposite action is shown for the second half-cycle of operation. The separate resultant waveforms are shown in part C. In part D, they are combined together to form a complete amplified signal with no second-harmonic content.

For Class A operation, maximum output efficiency and the least dissipation are obtained with maximum signal swing. To make certain that the power dissipation ratings of the transistor are not exceeded, only half the maximum permissible collector voltage is applied, since the applied voltage tends to double because of the inductive effect of the transformer. For Class A operation, the transistor is biased and operated at the center of the forward transfer characteristic curve, so that equal base current swings will produce approximately equal collector current swings; thus, it functions as a largesignal amplifier. Since a large-signal amplifier operates over a much greater range of current and voltage than a small-signal amplifier, circuit design is accomplished graphically, using the actual transistor currents to determine the range over which minimum distortion and maximum power output can be obtained. Usually, the transistor is slightly less linear than the electron tube, but with good design its operation compares favorably with electron tube operation.

Since much heat is dissipated at the collector for large power outputs, the shell of the power transistor is usually comected firmly to the chassis for direct conduction and reduction of heat (chassis acts as a heat sink). Where the shell must be insulated from the chassis, it is usually separated by a thin wafer of mica (or other suitable material) to prove insulation and yet allow full heat transfer.

Where minimum distortion is required, the transistors are selected in matched pairs, as is true with electron tubes. Because of the high power-handling capability required for Class A operation, transistors are usually operated Class B or Class AB.

**Class B Operation. In true** Class B operation, the bias is such that **no** collector current flows for one-half of the cycle. Thus, each transistor reproduces only half of the cycle, and two transistors are required to faithfully reproduce any signal (an exception is the Class B r-f amplifier, discussed later in this section, which uses a tank circuit and amplifies only a single frequency). Since at cutoff a reverse current flows in the transistor, collector current is never completely cut off, and a small quiesent current flows during the inactive half-cycles of transistor operation. (This quiescent reverse current should not be confused with the small forward current which flows in Class AB operation because the bias is not at cut off.)

For two transistors complely biased off, the forward transfer characteristics as shown in the following illustration. The two transfer curves are placed back-to-back to make the complete dynamic operating curve. Note how this curve is rounded off at the beginning and at the end instead of being a straight line. This is typical of the nonlinearity obtainable at cutoff, and illustrates why Class B operation produces the greatest distortion.



Composite Current Transfer Characteristic, Class B Operation

The accompanying circuit is that of a typical Class B stage operated with zero bias. Emitter swamping resistors RI and R2 are used for thermal compensation, and are unbypassed to provide a slight amount of degeneration.



Class B Push-Pull Stage

Note here one of the differences between the electron tube and the transistor. At zero bias the conventional electron tube conducts heavily, and it is necessary to apply considerable negative bias to achieve Class B operation. On the other hand, the transistor always has the collector reverse-biased; thus, in the absence of a forward base bias (that is, at zero bias), no collector current can flow. In this respect the transistor is similar to specially constructed Class B (zero bias) electron tubes.

When a signal is applied to input transformer T1, a voltage is applied to the base of transistor Q1 and an oppositely polarized voltage is applied to the base of Q2 (the polarity for the initial half-cycle is shown on the schematic). With transistors Q1 and Q2 at zero bias, only reverse leakage collector current flows in the absence of a signal. When the input signal is applied, the flow of current in the primary of T1 induces an oppositely polarized signal on the base of Q1 (transformer connected out-of-phase). Thus, the positively swinging input appears as a negative (forward) bias on the base of Q1, causing collector current to flow in the top half of the primary of T2, and

induces an output voltage in the secondary. At the same time the input voltage applied to Q2 is opposite in polarity and produces a reverse bias, keeping Q2 cut off. During the entire half-cycle Q1 conducts while Q2 remains cut off. When the input signal reverses polarity, reverse bias is applied to cut off Q1 collector current, and forward bias is applied to Q2. Consequently, Q2 conducts and the increasing collector current through the bottom half of the primary of T2 induces a voltage in the secondary of the output transformer. During this half-cycle Q1 remains cut off while Q2 conducts. Thus, Q1 and Q2 alternately conduct when the input signal produces a forward bias. Since the outputs of Ql and Q2 are combined in the secondary of the output transformer, the input signal is reproduced in amplified form, but of opposite polarity. If the output transformer is connected inphase, the same polarity of output exists as in the primary; when it is connected out-of-phase, the opposite polarity exists. This transformer action is identical with that occurring in the electron tube push-pull circuit.

Since there is no heavy flow of quiescent current when no signal is applied, maximum dissipation occurs during the signal (at about 40 percent maximum collector current), and less heat is developed for the same signal as in a Class A amplifier. Hence the transistor can be diven harder to obtain greater efficiency and more power output than is obtained in the Class A stage. The flow of reverse leakage collector current represents a loss of efficiency since no useful action is produced by this current. Such current flow does not exist in the electron tube. To minimize this loss, transistors are selected for a low  $I_{CEO}$ . Since audio power is produced, the transistors heat during operation (a maximum of 78 percent efficiency is theoretically obtainable) and the reverse leakage current increases. Emitter swamping resistors RI and R2 provide a small opposing bias voltage to prevent thermal runaway. They are not bypassed with capacitors as in Class A operation because the capacitors would charge during the operative half-cycle and discharge during the inoperative half-cycle, thus causing a change in bias. Because of the large peak current which flows through these resistors, they are kept to a very low value of resistance to prevent excessive degeneration and loss of amplification. In some applications, by proper selection of transistor types and good design they are not needed. In any event, when used, their main function is to provide

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thermal stabilization; any beneficial degeneration which may occur from their use is only a secondary consideration. Otherwise, they have no effect on the operation of the circuit.

Since the transistors operate alternately in Class B operation, there is no basic cancellation of second and even-order harmonics in the output transformer as in Class A operation. There is, however, an increase in third-harmonic distortion produced when the waveform passes through zero (this is known as crossover distortion). The development of this type of distortion is shown by projecting a sine-wave input signal on the transfer characteristic curve, as shown in the accompanying illustration. The distortion is greatest for small input signals and least for large input signals. This distortion is eliminated by applying a small forward bias to the base-emitter junction of the transistors, or what amounts to operation as a Class AB amplifier. Class B operation is used only when the large amount of third-harmonic distortion can be tolerated.



**Development of Crossover Distortion** 

**Class AB Operation.** The schematic of the Class AB amplifier is basically identical with that of the Class A amplifier shown previously. The only difference is that bias voltage divider resistors R1 and  $R_{\rm B}$  are of different values. Only a slight forward bias is applied, and only a small collector current flows with no signal applied. While this current is essentially wasted, it does eliminate the crossover distortion

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which would be produced if the bias were reduced to zero. It is evident, then, that Class AB operation produces slightly less output than Class B operation. Because of the small resting current, the transistor can be driven harder than the Class A stage; consequently, greater output can be obtained than for Class A operation. The efficiency averages about 65 percent for a well designed Class AB stage.

The small resting current, like the average current drawn in Class A operation, cancells out the flux in the primary of the output transformer (each side flows in a different direction), and there is no output produced until a signal is applied. When the input signal is applied, Q1 conducts and Q2 is driven to zero conduction on one half-cycle, while on the other half-cycle Q2 conducts and Q1 is driven to zero. The resultant signal swings are unequal and considerable second-harmonic distortion is produced in the primary of the output transformer; however, it is canceled out in the secondary when both signals are combined (assuming that the transistors are fairly well matched). Thus, only fundamental and thirdharmonic distortion can exist in the output. This form of operation is identical with Class A operation except that more odd-harmonic distortion is produced because the transistors operate for less than 360 degrees of the cycle.

The accompanying illustration shows the composite transfer characteristic for a typical Class AB stage. When compared with the transfer curve for the Class B stage shown previously, it is evident that the operation is more linear except for very large signal swings.



Composite Current Transfer Characteristics, Class AB Operation

Projection of the input signal on the composite transfer curve shows the collector output, which, when compared with that of the Class B stage shown previously, indicates the improvement in fidelity obtained with Class AB operation, and the total elimination of cross-over distortion.



**Development of Class AB Signal** 

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance ordinarily employed on the low-voltage ranges. Be careful **also** to **observe** proper polarity when checking ,continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition can be caused by an open circuit in either the input transformer, Tl, or output transformer, T2, or in the swamping resistors,  $R_{E1}$  and  $R_{E2}$  as well as by lack of supply voltage. The supply voltage can be checked with a voltmeter, and lack of collector or base bias voltage can also be determined. Continuity checks of the transformer (WITH THE POWER TURNED OFF) will determine whether one or more of the windings are open, and the resistors can be checked for proper resistance with the ohmmeter. Normally, failure of the transistors will not cause complete loss of output unless both transistors fail completely.

Low Output. Lack of sufficient drive power, low supply voltage, improper bias, or a defective transistor can cause reduced output. The supply voltage and bias can be checked with a voltmeter. Lack of drive power can be determined by observing the waveform with an oscilloscope and noting whether there is sufficient drive to cause eventual flat-topping or bottoming of the output waveform. A shorted or inoperative transistor can also cause low output. Depending upon conditions, removing the transistor (from a plug-in socket) will either increase or reduce the output. In the case of a shorted transistor, the output will probably increase when it is removed. A transistor with low gain or poor performance, when removed, will probably cause further reduction of the output. If the shorted transistor is left in the circuit and the good one is removed, there will also be a decrease in the output.

Distorted Output. Distorted output may be caused by lack of proper bias or supply voltage, by underdrive or overdrive, or by defective transistors or transformers. If one half of a transformer is open or shorted, one transistor will not operate properly and distortion will occur. Likewise, if the bias is too high, clipping will occur on the peak of the input signal, and if it is too low, collector bottoming will produce the same effect at the troughs of the signal. Transformer resistance and continuity can be checked with an ohmmeter, while the bias and voltage can be checked with a voltmeter. In Class A or Class AB stages, one half of the circuit can be inoperative and the until will function with reduced output and increased distortion. Use an oscilloscope to observe the waveform, checking from input to output. When the waveform departs from normal, the cause of the trouble will usually be obvious.

# PUSH-PULL, SINGLE-ENDED COMPLEMENTARY SYMMETRY AUDIO POWER AMPLIFIER (SEMICONDUCTOR)

### Application.

The push-pull, single-ended complementary symmetry audio amplifier is used where high power output and fidelity are required. For example, it is used in receiver output stages, in public address amplifiers, and in AM modulators, where reduced weight and space is a prime requirement.

#### Characteristics.

Collector efficiency is high with moderate power gain.

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Requires **only** half the drive of the conventional push-pull amplifier.

Power output is twice that of a single transistor stage.

No input or output transformer is used.

Distortion varies with the class of operation.

Usually is Class B biased, but may be biased Class A in some applications.

Fixed bias is usually used, but self-bias may be encountered in some applications.

## Circuit Analysis.

General. Complementary symmetry is unique with tmnsistors, and has no electron-tube counterpart. Recall from basic theory that a transistor may be either the PNP or NPN type, and that the bias and polarities are opposite. Thus, two different types of transistors may be used back-to-back to provide push-pull operation without the necessity for phaseinverting input and output transforms. An economic advantage is gained in that the cost of the transformers is eliminated, and a more uniform response is obtained since the reactive effects of the transformers are also removed from the circuit.

Circuit **Operation**. The accompanying schematic shows a typical single-ended, common-emitter, push-pull complementary symmetry circuit. The operation in Class B at zero bias.



Zero Bias Complementary Symmetry Push-Pull Circuit

Resistance-capacitance input coupling is used, with CCC acting as the coupling capacitor and  $\mathbf{R}_{\mathbf{B}}$  as the base return resistance across which the input signal is applied. With both emitters grounded and no bias applied, the bases of the transistors are zero-biased at cutoff. No current flows in the absence of an input signrd. When an input is applied, both bases are biased in the same direction. Since Q1 is an NPN transistor, the positive-going input signrd produces a forward bias. Q2 is a PNP transistor and requires a negative potential for forward bias; the input signal has no effect other than to reverse-bias Q2 and hold Q2 in a cutoff condition. Thus, during the positive half of the input signal only Q1 conducts. During the negative portion of the input signal Q1 is biased off beyond cutoff by a reverse bias, and a forward bias is applied to Q2, causing collector current to flow for the entire negative half-cycle. Thus, each transistor conducts alternately for half of the cycle, and two transistors are required to reproduce the input signal. Note that the bases are connected in parallel, and, since only one transistor operates at a time, only enough drive for a single stage is required instead of twice the drive as in normal push-pull operation.

Because the transistors are of opposite types, two equal-voltage collector power supplies are required, one negatively polarized and the other positively polarized. (A single supply can be used with proper circuit changes, but twice the collector voltage of a single stage is required.) The load resistor,  $R_1$  (which may be the voice coil of a loudspeaker), is connected from the common connection between the power supplies and the emitters. In this instance the emitter end is grounded, so that the power supplies are actually floating above ground. When the input signal is applied and develops an output for each half-cycle, the output is added together in the common load and no transformer is required. To develop maximum power, a low-impedance is needed. Otherwise, if high-impedance loads are used, an output transformer will be required for proper load matching. In this instance, however, the winding need not be centertapped since the output is single-ended. Because the output is single-ended (taken between the collector and ground), the collector load is calculated on the basis of the full primary-to-secondary turns ratio-not on one-half the primary-to-secondary turns ratio as in the conventional push-pull stage. Thus, the loading is 1/4 the normal push-pull output, which accounts for the low-impedance output.

In most electron tube or transistor circuits it is necessary to separate the dc component in the output from the output from the ac component by capacitive or transformer coupling (except in the special case of the dc amplifier). In the complementary symmetry arrangement such provisions are unnecessary. Both dc power supplies are connected in series with the transistors, and only one transistor is operative at a time; thus, there is no net flow of dc around the circuit. When Q1 conducts, there is a flow of current through  $R_{I}$ , the transistor, and the power supply in one direction. When Q2 conducts, the flow is through  $\mathbf{R}_{\mathbf{I}}$ , Q2 and the power supply in the opposite direction; thus, there is no circulating current, and the dc is effectively removed from the load circuit since only the continuous flow of dc, since the circuit flows out of the base when Q2 conducts, and into the base when Q1 conducts. Therefore, the charging and discharging of the coupling capacitor and its possible effect on changing the base bias are of no consequence in this circuit.

In the preceding discussion it was assumed that the transistors are balanced (or matched), having identical gain and collector currents. Like the conventional push-pull amplifier, this matching is necessary to obtain maximum output with minimum distortion. Unlike the electron tube circuit, which uses identical plate voltages and matches the plate current, the complementary symmetry circuit has identical collector (plate) currents since the transistors are seriesconnected and the biasing is adjusted to equalize the collector voltages. In the case of Class A or AB operation, the bias point in the base circuit is affected by drive and base current drain. Thus, keeping the signal from affecting the bias is one of the important design problems. So far as the techician is concerned, the practical effect is that with better design less distortion is obtained, with a maximum of amplification.

Better performance is obtained from the common-collector circuit when complementary symmetry is employed; even though the commonemitter circuit is the more widely used configuration. Although the over-all gain and output are slightly less, the stability of the circuit is improved; the collector supply can be grounded instead of floating (which reduces power supply ripple), and the effect of negative feedback is obtained, thus requiring less closely balanced transistors and improving fidelity and response characteristics. Both circuits are identical except that the ground is removed from the emitters and placed on the common power supply connection, as shown in the accompanying schematic.



## Common (Grounded) Collector Complementary Symmetry Push-Pull Circuit

As in other common-collector circuits, no polarity inversion of the output signal occurs, so that the inputs and outputs are of the same polarity. In operation, the circuit functions in the same manner as the common-emitter push-pull complementary-symmetry amplifier previously described. Only one transistor operates at a time, zero bias is employed, and the output is taken from the emitters to ground. Collector current flows through Ql, power SUpply  $V_{ccl}$ , and load resistor  $R_{\scriptscriptstyle L}$  in one direction, and through  $V_{cc2}$ , Q2, and  $R_L$  in the opposite direction, as the transistors are alternately forward-biased by the input signal. There is one difference, however, in that more input (drive) voltage is required to obtain full output because of the degenerative effect of connecting the load between the emitters and ground.

The accompanying schematic shows the complementary symmetry push-pull circuit connected for use with a single power supply, and with feedback from collector to base. Connecting capacitor Cl in series with load resistor  $\mathbf{R}_{\mathbf{L}}$  permits the use of a single power supply. Since no dc normally flows through the load, the insertion of the blocking capacitor has no effect on either ac or dc operation. Since both transistors are connected in series with the power

supply, twice the dc voltage of one supply is necessary. In addition, resistors R1 and R2 are employed to provide a fixed base bias and a slight amount of feedback from collector to base. The feedback reduces the matching requirements, and the dc bias is adjusted by selecting the values of RI and R2 so that equal collector voltages are obtained (with the series connection of transistors the same value of current flows throughout the circuit).



# Complementary Symmetry Push-Pull Amplifier with Common Power Supply

As far as dynamic operation is concerned, it is also identical with that of the previously discussed common-emitter complementary symmetry circuit. When a forward bias is applied by the signal, the transistor conducts. With a sine-wave input signal applied, a sine wave of current flows (at audio frequencies) through capacitor Cl and load  $R_{\perp}$  to develop the output signal.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any

of the transistor junctions will cause a false low-resistance reading.

No Output. An open or short circuit in the power supplies or transistors, or an open coupling capacitor or load resistance can cause no output. A voltage check will indicate whether the proper voltage and polarities are applied. Since Class B zero bias operation is normally employed, no base-to-emitter (or ground) voltage exists in the absence of a signrd. However, if an attempt is made to measure this voltage with a meter, a false reading may be obtained through the voltmeter shunting resistance. Therefore, only the polarity and supply voltage sould be checked, and the input signal should be observed with an oscilloscope. Lack of input signal on the oscilloscope indicates an open coupling capacitor, CCC, or a shorted input circuit caused by a defective transistor. If the supply voltage and polarity are correct and a signal is visible at the input, but not in the load, either the transistor is defective or the load is shorted. A resistance or continuity check will determine whether the load is normal. If it is normal, only the transistors can be at fault. Since only one transistor is operative at a time, both transistors must be defective to cause a loss of output; otherwise, a reduced or distorted output exists.

Reduced Output. If one of the transistors is defective, or if one of the supply voltages is low or the supply is defective, a loss of output will occur. Use an oscilloscope to observe where the input waveform or output waveform departs from normal. Check to make sure that there is sufficient drive in the preceding stages. A leaky coupling capacitor will place a fixed bias on the base circuit, causing conduction in one transistor and rendering the other inoperative. Depending on the amount of bias, the circuit may be such as to very slightly reduce the output or to cause severe distortion. Unbalanced collector voltages, if sufficiently different, will cause loss of amplification and distortion on one side of the circuit, which can be observed on the oscilloscope. Since there are only a few components in the circuit, a resistance and voltage check should quickly indicate whether the components or power supply is defective.

**Distorted Output.** Improper bias or load resistance can cause a distorted output. Use an oscilloscope to determine where the signal departs from normal. The trouble will then be localized to that portion of the circuit showing the distorted waveform. In the common-emitter circuit, if the distortion occurs on the negative portion of the waveform, the trouble is in the PNP transistor circuit, if it is on the positive portion of the waveform, the trouble is in the NPN transistor circuit. Since there is no inversion of polarity in the common-collector circuit, the indications will be the opposite. That is, distortion on the positive waveform indicates trouble in the NPN transistor circuit, and distortion on the negative waveform indicates trouble in the PNP circuit.

# PUSH-PULL, SINGLE-ENDED, SERIES-CONNECTED AUDIO POWER AMPLIFIER (SEMICONDUCTOR)

#### Application.

The push-pull, single-ended, series-connected audio amplifier is used where high power output and fidelity are required. For example, it is used in receiver output stages, in public address amplifiers, and in servo amplifiers, where compactness and reduced weight through elimination of the output transformer are desired.

## Characteristics.

Collector efficiency is high with moderate power gain.

Requires the same drive as a conventional pushpull amplifier.

Power output is twice that of a single transistor stage.

No output transformer is required, and identical types of transistors are used.

Distortion varies with the class of operation.

Class B bias is normally used, but Class A or AB applications may be encountered.

Fixed or zero bias is normally employed, but selfbias may be used in some applications.

### Circuit Analysis.

**General.** The series-connected, single-ended pushpull amplifiers used two similar-type transistors in the equivrdent of the complementary symmetry circuit to provide a transformerless output. It requires fewer components than the conventional push-pull amplifier, but more than that of the complementary symmetry amplifier, since a push-pull input is necessary; it is single-ended in the output only. A compound-connected transistor input circuit may be used; however, since this circuit requires two additional transistors, an input transformer is usually used instead. Because of the series transistor connection, two separate collector supplies are required, or a center-tapped supply that is twice the value of a single supply is necessary.

**Circuit Operation.** The schematic of a typical single-ended, series-connected push-pull PNP audio amplifier is shown in the accompanying figure.



Single-Ended, Series-Connected PNP Push-Pull Amplifier Circuit

Note: Read the Direct-Coupled Audio Amplifier circuit discussion earlier in this section for background information.

Transistors QI and Q2 are zero-biased and are nonconducting in the absence of a signal. Both transistor are the PNP type. The input transformer has two separate windings rather than the center-tapped arrangement conventionally used in push-pull circuits, to provide out-of-phase (opposite-polarity) input signals to the series-connected common-emitter stages. This provides an input connection which is separate for each transistor; the base of Q1 is driven positive while the base of Q2 is driven negative, and vice versa. With Class B, or zero bias, only one transistor operates at a time. One of the secondaries of T1 is connected so as to invert the signal. Thus, on the positive input signal, Q2 is driven negative and the forward bias causes conduction; meanwhile, the base of Q1 is held at cutoff by a positive input. On the opposite half-cycle, Q2 is held at cutoff while Q1 is driven to

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conduction by the negative input signal. In this example the secondary connected to Q1 is comected in-phase, while the secondary connected to Q2 is connected out-of-phase.

The load, R<sub>1</sub> is connected from the common point of the two power supplies to the emitter of Q1 and the collector of Q2. Disregarding this load connection for the moment, it is clear from observation of the schematic that the two transistor are connected in series with each other and their separate power supplies. In the absence of an input signal no current flows, and, since each transistor conducts separately, with current flow in opposite directions through R, there is no net flow of dc through the load in one direction to unbalance it. Therefore, the voice coil of the speaker may be placed directly in this circuit to act as a load, without requiring any dc isolation through coupling capacitors or transformers.

When collectors current flows in Ol, the electron path is from the emitter, through  $R_1$  and the power supply, back to the collector. When collector current flows in Q2, the electron path is from the emitter of Q2, through the power supply and load  $R_1$ , back to the collector. These currents flow in opposite directions through the load resistor, each producing one half-cycle of the signal. There is no continuous flow of dc through the circuit or through the load. In Class A or Class AB stages, a forward bias is supplied to the base, and both transistors conduct continually. DC flows through the series transistors and power supplies, but does not flow through the load resistor. This action occurs because, with a balanced circuit and identical collector current flow in both transistors, equal but opposite voltages are developed across the load resistor; therefore, they cancel, producing an effective zero dc flow through the load.

In Class A operation, any second-harmonic current is canceled out in the load as in conventional pushpull circuits. In Class B operation, there is no cancellation of second-harmonic current, and the predominant distortion is third harmonic. Thus, regardless of the method by which it is obtained, second-harmonic distortion is reduced in this circuit as in the conventional push-pull circuit.

## Failure Analysis.

General. When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance ordinarily employed on the lowvoltage ranges of conventional volt-ohmmeters. Be

careful also to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition can be caused by an open- or short-circuited input transformer, T], or load, R<sub>1</sub>, as well as by a lack of supply voltage. The supply voltage and the collector or base bias voltage can be checked with a voltmeter. Continuity checks of the input transformer windings (or the load) will locate any open circuits, and short-circuited windings (or load) will be indicated by ohmmeter readings of less than 1 ohm. In Class A or AB stages the bias resistors can be checked for proper values with an ohmmeter. Normally, failure of the transistors will not cause complete loss of output unless both transistors fail completely.

Low Output. Lack of sufficient drive power, low supply voltage, improper bias, or a defective transistor can cause reduced output. The supply voltages and bias can be checked with a voltmeter. Lack of drive power can be determined by observing the waveform with an oscilloscope and noting whether there is sufficient drive to cause eventual flat-topping or bottoming of the output waveform. Either a shorted or otherwise inoperative transistor can cause low output. Depending upon conditions, removing the transistor (from a plug-in socket) will either reduce or increase the output. In the case of a shorted transistor, the output will probably increase when it is removed. Where the transistor has low gain, a slight reduction of output will usually be noted when it is removed. If the defective transistor is left in the circuit and the good one is removed, a decrease in the output will also be observed.

Distorted Output. Distorted output may be caused by lack of proper bias or supply voltage, by underdrive or overdrive, by defective transistors, or by a defective input transformer. If the primary winding of the input transformer is open, either no output will occur or a very low output may be obtained by capacitive coupling between the turns. However, if either one of the secondary windings is open or shorted, one transistor will not operate properly and distortion will occur. Likewise, if the bias is too high, clipping will occur on the peak of the input signal; if it is too low, collector bottoming will produce the same effect at the troughs of the signal. Transformer resistance and continuity can be checked with an ohmmeter, while the bias and collector

voltages can be checked with a voltmeter. In Class A or Class AB stages, one half of the circuit can be inoperative and the unit will still function with reduced output but with increased distortion. Use an oscilloscope to observe the waveform, checking from input to output. When the waveform departs from normal, the cause of the trouble will usually be obvious.

# PUSH-PULL, CAPACITANCE-DIODE COUPLED AUDIO POWER AMPLIFIER (SEMICONDUCTOR)

### Application.

The push-pull, capacitance-diode-coupled audio amplifier is used where high power and fidelity are required in receiver output stages, public address systems, and modulators. It is usually employed as the power output stage of a resistance-coupled amplifier.

## Characteristics.

Collector efficiency is high with moderate power gain.

Requires the same drive as a conventional pushpull amplifier.

Power output is twice that of a single stage.

No input transformer is used, and identical types of transistors are used.

Input circuit is push-pull (oppositely polarized signals from either a phase inverter or a push-pull drive are required).

Distortion varies with the class of operation; operation may be Class A, AB, or B, with Class AB use predominating.

Fixed bias is normally used, but self-bias may be encountered in some applications.

## Circuit Analysis.

**General. The capacitance-diode-coupled** push-pull amplifier differs from the conventional push-pull amplifier only in the input circuit. Diodes are used to prevent the charging or discharging of the coupling capacitor from producing a shift of base bias with signal, and causing distortion. The use of capacitive coupling eliminates the necessity for an input transformer and provides a reduction in weight and space, and an increase in economy. Any improvement in response characteristics through elimination of the input transformer and its reactive effects are somewhat minimized by the shunting and loading effects of the diodes. Thus, the operation and performance are substantially the same as the conventional transformer-coupled push-pull amplifier, with a slight improvement in the high-frequency response.

Circuit Oparation. The accompanying schematic shows a typical **push-pull**, capacitance-diode-coupled PNP transistor audio amplifier. The operation is considered to be Class B with a slight forward bias to eliminate crossover distortion (actually Class AB), as determined by voltage divider resistors R3 and R4. Because diodes CR1 and CR2 are comected in series opposition across the input, and are isolated by coupling capacitors Cl and C2, conduction through the diodes is necessary to establish a bias on the base of the transistors. With R4 connected between the diodes and ground, a slight negative voltage appears at their cathodes, so that they normally conduct slightly. In the absence of an input signal, conduction through CR1 and CR2 permits a continuous flow of dc base current, which, in turn, permits a small idling collector current to flow through the forwardbiased bases. This static (quiescent) current flows in opposite directions through the primary of the pushpull output transformer, Tl, and the effective flow is zero. No secondary output occurs because the flux in each half of the primary of T1, produced by dc current flow, cancels (as in conventional push-pull operation).



Capacitanea-Dioda-Couplad Push-Pull Stage

When an input signal is applied, oppositely polarized signals are supplied to coupling capacitors Cl

and C2 simultaneously. (Resistors RI and R2 represent the driver stage output resistance, normally taken between the driver stage collector or emitter and ground.) With a negative-going sine wave signal applied through Cl, a forward bias is applied to the base of transistor Ql, causing collector current to flow through the upper half of the primary of **T1** into Q1. At the same time, a positive-going input signal is applied through C2 to the base of Q2, producing a reverse bias, and reducing collector current flow through the lower half of the primary of T1 into Q2. Since Q2 is normally producing only a small current flow, this reduction in forward bias drives the transistor nearly to cutoff. Thus, the current in Q2 is reduced while the current in QI is increased (this is conventional push-pull action.) When the negative input signal is applied to Ql, it also reverse-biases the anode of CR1, and the diode appears as a very high resistance; therefore, the input signal is not bypassed to ground via R4, and there is no effect on the bias circuit. On the other hand, when the positive input signal is applied to CR2 and the base of Q2, the diode is forward-biased and it conducts heavily. This action permits C2 to discharge rapidly through the low resistance of CR2 and R4 to ground on one side, and from ground through R2 to the other side of C2, as shown by the dotted arrows in the schematic. The electron flow path is from ground through R4, and CR2 to C2 on one side, and from ground through R2 to the other side of C2. Thus, a small instantaneous positive voltage is developed across R4. This voltage further reverse-biases CR1 so that it cannot conduct and affect the operating bias. If CR1 and CR2 were resistor (instead of diodes), the voltage developed through these resistors would appear in series with the bias applied to both transistors and cause a shift in operation. The bias developed would add to the normal bias and place the total bias in the Class C region of operation, thus producing serious distortion and clipping,

With Q1 conducting because of-the negative input signal, capacitor Cl charges quickly through the low resistance of the base-emitter junction of Ql and ground, as shown by the solid arrows in the schematic. When the sine-wave input signal becomes positive-going on the opposite half-cycle, the base of **Ql** is reverse-biased and the collector current is reduced. At the same time, CR1 is forward-biased (by the positive input signal) and Cl is quickly discharged through R4 to ground on one side, and through

ground and **R1** to the other side of Cl. The voltage developed across R4 has no effect on the operating bias, since CR2 is reverse-biased while Q2 is conducting. In addition, it should be noted that the voltage produced across R4 by the discharge of C 1 or C2 is polarized in a direction opposite that of the normal bias produced by the voltage divider action of R3 and R4. Since the signal is never allowed to exceed the bias, to prevent distortion, this reverse bias is only a fraction of the operating bias and is thus effectively swamped out of the circuit. Only through failure of one of the diodes can it affect the operation of the circuit.

The operation of the collector and output circuits is exactly the same as previously explained for the conventional push-pull amplifier. Second- and evenharmonic distortion is cancelled in the primary of the output transformer, and the output contains only the fundamental and odd harmonics. The collector-tocollector load resistance is 4 times that of the individual collector-to-ground load, as in the conventional push-pull circuit. Since the input circuit uses the reverse-biased diode resistance as the base-to-ground" impedance, the capacitance-diode input circuit offers a high input impedance. Thus, the moderate output impedance of common-emitter phase-inverting driver stages may be conveniently matched.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output**. Open coupling capacitors, defective transistors, or a defective output transformer can cause a no-output condition. Observe the signal with an oscilloscope, checking from input to output. Lack of a base signal indicates that coupling capacitors Cl and C2 are open; lack of a collector-signal indicates either defective transistors, an open primary on Tl, or an open collector supply (check the supply with a voltmeter). Lack of an output across the secondary indicates an open secondary winding. Note that since each transistor will operate separately, a distorted output can be obtained if only one half of the circuit

is defective. Thus, both coupling capacitors, both transistors, or both halves of the primary of T1 must be open simultaneously for a no-output condition. Likewise, in the case of a short circuit, one half of the circuit must be biased off while the other is shorted to cause no output. Only an open circuit or a short circuit of the TI secondary can produce a no-output condition by failure of a single part.

Low Output. Low output can be caused by a number of conditions. Failure of one half of the circuit, regardless of cause, will result in reduced output. If bias resistor R4 opens, the forward bias will increase and full Class A operation will occur. Where the stage is normally operated Class AB or B, an open R4 will cause a reduction in output. The bias voltage can be checked with an ohmmeter, or R4 can be measured with an ohmmeter. If R3 becomes open, the bias will be removed and the stage will operate Class B, zero-biased. If the drive is insufficient, loss of output will occur. With sufficient drive available, however, it is possible for the output to increase, with an increase in distortion. If R3 is shorted, the increased forward bias will hold the stage in heavy conduction and the input signal will most likely be shunted through CR1 and R4 to ground, resulting in reduced output with distortion. If either CR1 or CR2 is shorted, one half of the input signal will be shunted to ground through R4 and the output will be reduced. If either Cl or C2 is leaky, the bias on Q1 or Q2 will be changed, depending upon the polarity of the voltage on the drive side of the capacitors. A negative supply for a PNP driver stage will cause increased forward bias and reduced output. A positive voltage for an NPN driver stage will produce constant heavy conduction through diode CR1 or CR 2, and cause shunting of the input, loss of drive, and reduced output. Either or both transistors may be defective and cause loss of output. Shorted primary or secondary windings on T1 will also reduce the output. Therefore, it is necessary to use an oscilloscope to observe the waveform and follow the signal through the circuit. When the waveform amplitude decreases, check the parts in that portion of the circuit for proper resistance or continuity as applicable.

**Distorted Output.** Improper bias, overdrive, or clipping because of too low a collector voltage can cause distortion. Use an oscilloscope to follow the waveform through the circuit; the source of the distortion will usually be easy to locate when the waveform differs from the input. Leaky coupling capacitors will cause improper bias and possible peak clipping. Defective diodes can also **cause** clipping of the input signal and consequent distortion. Defective transistors can produce distortion through nonlinearity or unbalance. For the least distortion, matched transistors are usually used. In some instance poor frequency response in the output transformer may also cause distortion. Poor response can also result from an improperly matched load or from a change in the load resistance. In any event, it is necessary to observe the waveform with an oscilloscope to determine whether the distortion increases or decreases as the signal is followed through the circuit.

# COMPOUND-CONNECTED AUDIO POWER AMPLI-FIER (SEMICONDUCTOR)

### Application.

The compound-connected power amplifier is used as the output stage in receiver, public address amplifiers, and modulators where large audio power outputs are required. It is also used as a directcoupled control amplifier in transistorized voltage regulators.

## Characteristics.

High voltage and power gain are obtained.

Operation is usually Class A.

Fixed bias is normally employed but self-bias may be encountered.

High input resistance is obtained (much greater than for a single CE stage).

Input is series-connected, and output is parallelconnected.

Two or more transistors are required.

Ratio of emitter current to collector current remains constant; there is no drop-off of collector or current high emitter currents.

High current amplification can be obtained with very little distortion (less than  $\frac{1}{2}$  percent).

## Circuit Analysis.

General. Two compound-connected transistors may be employed as a single transistor and used in other circuit configurations, such as, **push-pull** audio amplifiers, to obtain greater output and more linear response than can normally be obtained in the circuit. Because the forward current gain does not drop off at

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high emitter currents, the operation is linear and since the collector current continues to increase proportionally as the emitter current increases, the **transis**tors can be driven to **full** output without any increase in distortion. The increase in linearity of the collector current which the compound comection provides can be clearly seen from the accompanying graphic comparison of emitter and collector currents.



Graph Showing Differences Between Compound-Connected and Single-Transistor Operation

Note that in the graph the ratio of collector current to emitter current for a single transistor remains constant (as indicated by the straight-line portion of the curve) until approximately 400 ma is drawn; then the collector current increases less rapidly as the emitter current increases (as indicated by the curved portion). This is reduction in collector current linearity indicates a loss in forward current amplification, which is most pronounced in power amplifiers that draw heavy emitter current. The variation of the total collector current with input emitter current for compound-connected transistor is also shown in the graph. Observe that the total collector current of the compound-connected transistor does not drop off as the emitter current increases, but varies linearly over the entire range of operation (it is a straight line instead of a curve).



Circuit Operation. The basis schematic for a pair

of compound-connected transistors used as an audio

amplifier is shown in the accompanying illustration.



Compound-connected Common-Emitter Audio Amplifier Circuit

Fixed Class A bias is supplied to the base of transistor Q1 through voltage divider resistors R1 and R2 connected across the common power supply. (Refer to the introduction to this section of the handbook for a discussion of the types and methods of biasing.) The bias on Q2 is supplied by emitter current flow through Q1 and Q2 to ground, the actual value being determined by the emitter current of **Q1** and the forward gain of Q2. Capacitive input coupling is provided by Ccc. The output load,  $\mathbf{R}_{\mathbf{L}}$ , is comected in series with both transistors and a common source of power; the collectors are connected in parallel, and thus share a common load. The output is taken through coupling capacitor Cl (in some circuits  $\mathbf{R}_{\mathbf{L}}$ and Cl are replaced by a transformer for greater power output).

Both transistor are connected in the commonemitter configuration, and, since the base of Q2 is directly connected to the emitter, which is the cornmon leg of Ql, transistor Q2 provides a certain

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amount of negative feedback. Because both transistors are series-connected across the input, a much higher input resistance (100 times as large, or more) is offered than with a single CE stage. In the **absence** of an input signal, both transistors operate in the Class A region, as determined by the fixed voltage divider bias supplied by **R1** and R2. The bias on **Q2** is just slightly less than that appearing on the base of Q1 because of the small voltage drop between the base and emitter of Q1.

Assume that a negative input signal appears at the base Ql; this increase in forward bias causes the collector current of Q1 to increase to a value determined by the forward gain characteristics of Q1 and the amplitude of the input signal. The flow of  $i_{d}$  (and  $i_{C2}$ ) through R<sub>1</sub> produces the output voltage, which, as in the conventional common-emitter circuit, has a polarity opposite that of the input voltage. At the same time, since the base and emitter of Q2 are in series with the input, a forward bias is also applied to Q2 to increase collector current  $i_{C2}$ . While the amount of collector current through Q2 is not as great as that through Ql, it adds to the output since it flows in the same direction through  $R_1$ . The total collector current flowing through  $R_{L}$  is the sum of the two collector currents  $(i_{el} + i_{C2})$ . It is not double that of a single transistor, but varies in accordance with the ratio set by the individual forward gain values and the amount of base current drive applied to Q1. It is not necessary that both transistors be matched or have equal forward gain. However, it is convenient to show how the currents are distributed, assuming that the two transistors are identical. In a conventional cascaded stage the gain of two stages would be equal to the gain of the first stage times that of the second. Assuming a value of a fe = 19, the total gain of two stages would be 361, while for a compound connection a value of 399 is obtained (approximately 10% additonal gain). This increase in gain is obtained because the collector current does not fall off at high emitter currents. The accompanying figure shows the two transistors compoundconnected in the common-base circuit, for ease of explanation. Assuming a forward gain or alpha of .95 for both transistors (equivalent to a CE beta of 19), the current relationships through the circuit are as shown in the figure. In this circuit Q1 handles most of the load current while Q2 provides additional power during peak conditions. The flow of emitter current in the external circuit is from Q2, through the

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base of Ql, through the input resistance, and back to the collectors of both transistors through the output resistance. The collector current of Q1 is 0.95  $I_{\rm F}$ ; therefore, 0.5  $I_F$  flows into the base, since the emitter current is the sum of the base and collector currents. Since 0.95  $I_E$  flows into Q1 and the total collector current is 0.9975  $I_{\scriptscriptstyle E}$  the collector current of Q2 is the difference, or .0475  $I_E$ . Finally, since .05  $I_E$ flows from the emitter of Q2 into the base of Ql, the base current of Q2 is the total emitter current of Q2 less the collector current of Q2 or .0025 I<sub>e</sub>. While this might be considered to show little contribution of Q2 to the operation of the circuit, recall that in the common-base circuit the gain cannot exceed unity, which for all practicrd purposes is equal to **0.9999999....** etc; thus, a change from 0.95 to 0.9975 represents a considerable increase in gain. Expressed in terms of the common-emitter circuit (as previously mentioned) it is a change of from 19 to 399 in gain, which is a very noticeably increase.



**Current Relationships in Compound CB Circuit** 

Because the transistors are direct-connected in the compound circuit, there is no reactance to deteriorate the frequency response (it extends the low frequency bass response to zero or de); therefore, although an increase in gain results, no sacrifice in response occurs. With a series-connected input, only sufficient drive for one transistor is required, as the current through a series circuit is uniform. Thus, the addi-

tional gain is achieved without requiring more drive. Although it might be thought that the increased input resistance requires more drive for the same input, it does not, since a smaller current through a higher resistance produces the same voltage drop as a higher current through a smaller resistance. With the collectors connected in **parallel**, the output resistance is lower than that of a single transistor, but not half as might be expected. It is approximately equal to the ratio of the two collector currents and is not of much significance, because the compound connection produces a larger output mainly by its ability to pass a greater current through the same load. In the basic schematic the output is shown capacitively coupled; where large power outputs are desired, an output transformer is usually used as in the conventionrd single-ended power amplifier. The compound comection may be used in any of the previously described circuits in this handbook to obtain greater linearity and output, but it requires two transistors for each one used in the conventional circuit.

When the load resistance is connected in series with the emitter of Q2 instead of the collector, this compound circuit becomes the cascaded emitterfollower amplifier, sometimes referred to as the **Darlington circuit**. Because of the large amount of degeneration provided, the operation is slightly different from that of the compound circuit described above. In other publications, the compound comection is also referred to as the **Tandem connection** or the **Super-alpha connection**.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of most volt-ohm-milliameter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output**. Lack of supply voltage, either an open or short-circuited input or output or defective transistors, will cause a no-output condition. The supply voltage and the presence of collector and base bias can be checked with a voltmeter. With the proper voltage and polarities existing in the circuit, observe the waveform with an oscilloscope. Loss of signal on the base side of the input indicates either and open

coupling capacitor or a shorted input. Since the emitter of Q1 is connected in series with that of Q2, failure of either transistor will produce loss of output. An open output coupling capacitor (or transformer, if used) will also cause loss of output. Leaky coupling capacitors usually will not cause a complete loss of output. On the other hand, a shorted input capacitor can bias the circuit to cutoff or into heavy saturation depending upon the polarity of the collector supply of the preceding driver stage. Since all short circuits will most likey change the bias and circuit voltages, and open circuits will show normal voltages, a simple voltmeter check will determine the type of trouble. With only a few parts in the circuit, they may be checked separately to determine the defective part.

Reducad **Output.** Improper bias, low collector voltage, or defective transistors will cause reduced output. A leaky coupling capacitor will produce a larger than normal bias and cause the transistors to operate closer to cutoff or to saturation, depending upon the polarity of the bias. The reduction in output may be slightly noticeably or very evident, depending on the value of the bias change; and may be easily determined by a simple voltage check. If the bias and voltages are correct and the proper load is connected, a reduced output with normal input indicates that either one or both transistors are defective.

Where the wrong load or a short-circuited load is used, the output will be reduced. Check the value of the load with an ohmmeter. Where capacitive output coupling is employed, a leaky or shorted capacitor can cause a steady flow of dc through the output circuit. In the case of a speaker, a steady flow of dc through the voice coil will hold the cone in a steady position and require a large output to move it. Check the output load for a dc voltage to ground using a ---voltmeter. Where the load has changed in value, reduced output will usually be accompanied by distortion; the same indication will occur for reduced collector voltage, which can be determined by a simple voltage check.

**Distortad Output.** Audio distortion will be obvious when a monitoring speaker or headphone is provided. Improper bias or low collector voltage, an improper load or defective transistors can cause distortion. Check the bias and collector voltages with a voltmeter. Use an oscilloscope to observe the input waveform and to follow it through the circuit. When it departs from normal; the location of the trouble

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will be obvious. Clipping of one side of the signal indicates improper bias or other voltages, while clipping on both sides indicates over-drive, as it does in electron-tube operating. Make certain that the input waveform is not distorted, since subsequent amplification will increase the distortion, making it appear to originate within the stage. With proper bias and other voltages and with a normal load, if distortion appears the transistors are likely to be defective.

# BRIDGE-CONNECTED AUDIO POWER AMPLI-FIER (SEMICONDUCTOR).

## Application.

The bridge-connected power amplifier is used in receiver output stages and public address systems or other equipments where a large audio power output with low distortion is required, and no output transformer is employed.

### Characteristics.

Over-all frequency response is improved by direct output coupling.

Operation can be Class A or B, with the least efficiency obtained in Class A, and the most efficiency in Class B operation, as in conventional push-pull stages.

Produces twice the power output of a conventional push-pull stage.

May be operated at twice the normal supply voltage instead of half the voltage as in other circuits.

Each transistor dissipates only half the power of its counterpart in the conventional push-pull stage; therefore, smaller transistors may be used for the same output, or a greater power can be obtained for the same transistors.

A single untapped source of supply voltage may be used.

No dc current passes through the load.

Requires push-pull input (opposite polarity and twice the drive of a single stage).

## Circuit Analysis.

**General. The** bridge circuit is developed from the basic dc bridge, sometimes called the *Wheatstone* bridge, using equal-ratio arms. In the basic two-transistor circuit, two equal power supplies form the other arms. With equal transistors and equal power supplies, the bridge is balanced for dc flow and there is no flow of dc through the load until the bridge becomes unbalanced by application of a signal. The

push-pull, single-ended, series-connected audio power amplifier discussed in this section of the handbook is an example of a simple type of bridge circuit. The full bridge circuit utilizes four identical transistors in a bridge arrangement, or two PNP and two NPN transistors in a complementary symmetry arrangement. The use of four transistors as the bridge arms permits operation with a single (or untapped) power supply, and provides twice the power output of the simple bridge circuit, with less distortion.

**Circuit Operation.** The schematic of a typical four-transistor PNP bridge amplifier is shown in the accompanying illustration.



#### **Full Bridga Circuit**

Note that transistors Q1 and Q3 have the load connected in the emitter circuit, while Q2 and Q4 have the load connected in the collector circuit. Therefore, Q1 and Q3 are common-collector configurations (the output is taken from the emitter) with high input impedances requiring large-voltage input signals. Transistors Q2 and Q4 are common+ **mitter** configurations (the output is taken from the collector) with low input impedances requiring low-voltage input signals, to produce an emitter-collector current equal to that of the common-collector connected transistors, and thus equalize the bridge currents.

The input signal is connected in a push-pull arrangement to the bases of Q1 and Q3; the base input to Q4 is taken from the emitter of Q1 through cur-

rent limiting resistor R2, and the base of Q2 is supplied with a signal from the emitter of Q3, taken through current limiting resistor RI. In this manner the opposite bridge arms are comected to similarly pcdarized and smaller inputs (as required for the common-emitter circuit); otherwise, a special transformer or a complementary symmetry arrangement would be necessary to provide proper amplitude inputs. When a negative input signal is applied to Q1, the forward bias is increased and both the collector and emitter currents increase. With increased emitter current flowing through R<sub>1</sub>, a negative voltage is developed across the load and applied through R2 to increase the forward bias on Q4. Therefore, the collector and emitter currents of Q4 also increase. The transistors are selected for equal gain, and R2 for equal L, so that the emitter and collector currents of both transistors are equal.

Meanwhile, an oppositely pcdarized (positive) input signal is applied to the base of Q3 simultaneously with the input signal applied to Q1. The positive input signal reverse-biases the base of Q3 and reduces any flow of collector and emitter current. Similarly, the emitter voltage of Q3 developed across load resistor  $\mathbf{R}_{\mathbf{L}}$  becomes more positive because of the reduction in current flow, and through R1 places a reverse bias on the base of O2, causing the emitter and collector currents of Q2 be reduced also. An increased current through one side of the bridge with a reduced current through the other side of the bridge produces the same effect as in conventional push-pull operation. In Class A operation, the total current flowing through the load is the same as if twice the normal current flow existed. In Class B operation, only two transistors conduct at a time, while the other two remain cut off.

When the input signal changes polarity on the opposite half-cycle (assuming a sine wave input) it becomes positive and a reverse bias is placed on the base of Q1. The reverse bias reduces the emitter current Ql, producing a positive polarity at the emitter; it is also applied through R2 to reverse-bias the base of Q4. Thus, both Q1 and Q4 emitter and collector currents are reduced simultaneously. Meanwhile, the input signal applied to the base of Q3 also changes, becomes negative, and applies a forward bias to the base of Q3, which increases the emitter current. The increased emitter current flows through the load in the opposite direction, as shown by the dashed arrow

on the schematic. The change of current flow creates an opposite polarity across  $R_1$ .

Since the voltage developed in the emitter circuit of Q3 is negative and the base of Q2 is connected to the emitter of O3 through R1, a forward bias is also placed on Q2. Thus, the emitter-collector current flow of Q2 is increased simultaneously with that of Q3. As a result, the transistors interchange roles; Q3 and Q2 become conducting, while Q1 and Q4 are driven toward cutoff in Class A operation, or are entirely cut off in Class B operation. Assuming equal transistors, biases, and drives, equal but oppositely polarized voltages are produced across the load resistor by the current flowing in different directions in the bridge arms, so that the effective dc flow is zero. Since the varying (ac) load current flows first in one direction during one half-cycle of input and then in the opposite direction during the remaining halfcycle, the output load can be direct-connected in the bridge, and no output transformer is needed to develop the output signal. While the input resistance of the bridge is high, the output resistance is low, and no impedance transformation is necessary to match loudspeaker of servo loads. (The transistors are usually selected to have an output impedance near that of the load, in which case  $R_1 = Vc/Ic$ .)

Because there are always two transistors across the supply, the collector voltage of each transistor is always less than the supply (usually half). Since no transformer is used, the collector voltage can never exceed that of the supply, so that the designer can apply twice the normal collector voltage to both transistors in order to apply the full rated collector voltage to each transistor. Therefore, a greater output can be obtained than would normally be possible in other amplifier circuits where the maximum collector voltage is never allowed to exceed half the supply voltage. Likewise, since each transistor dissipates only half the power dissipated by each transistor in a conventional push-pull amplifier, a four transistor bridge circuit can produce twice the output of the conventional push-pull circuit. This accounts for the high output power of the bridge circuit. Because the inputs to Q4 and Q2 are obtained from the emitters of Q1 and Q3, only enough drive is required to drive the bases of Q1 and Q3. Therefore, no additional drive power is required over that of the conventional pushpull amplifier.

In Class A operation, the quiescent currents of the
transistors are equal, and no dc flows through the load because the bridge is balanced. During operation, the current through one pair of arms increases while the current through the other pair decreases. On the opposite half-cycle the conditions are reversed. On the other hand, in Class B operation all transistors are zero-biased with no signal applied, and no current flows. When an input is applied, one pair of arms conducts while the other pair remains cut off. During the remaining half-cycle the other pair of arms conducts while the first pair remains cut off. Thus, twice the current of a single transistor flows through the load during either type of operation. Because no transformer is used and the transistors are directconnected, both low-frequency response and highfrequency response are improved. This accounts for the decrease in distortion of the bridge circuit as compared with any of the other push-pull circuits.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of most volt-ohm-milliameter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions **will** cause a false low-resistance reading.

No Output. If the output load or collector supply is open or short-circuited, no output will be obtained. A short-circuited load will be indicated by a resistance reading of iess than one ohm, while an open circuit will be indicated by infinity or a very much larger than normal resistance. Check the supply voltage with a voltmeter to determine whether the supply is defective. On the other hand, since the bridge is normally balanced across the points to which the load is connected, a voltage check across the load will usually not pinpoint an open load. Instead, the voltmeter shunt wiU replace the load, if open, so that a false reading will be obtained. If a transistor is shortcircuited, the other portion of the bridge will operate; thus, a single defective transistor will not produce a complete no-output indication. If transistor Q4 or Q2 is shorted, Q1 and Q3 will still operate. On the other hand, if Q1 or Q3 is shorted, the large input signal will probably bias Q2 and Q4 into cutoff and saturation, producing no output (in some instances a slight output may still be obtained, depending upon the

applied bias). If either R1 or R2 is open Q2 or Q4 will not operate and no output will be obtained in Class B operation. Likewise, if Q1 or Q3 is open, the remaining half of the bridge will not operate.

In Class A operation, all four transistors would have to be defective simultaneously to cause no output. Since in Class B operation only two transistors conduct at a time, while the other two are cut off, it will be necessary for two transistors to be defective for no output to occur. When transistors are replaced, they should be replaced in pairs.

Reduced Output. Reduced output may be caused by failure of a single transistor, defective bias resistor R1 or R2, or an open input circuit to one arm of the bridge. The resistors may be checked with an ohmmeter, and the supply voltage may be checked for proper value with a voltmeter. While unbalanced voltages across the separate arms of the bridge may indicate the probable location of the trouble, an oscilloscope check is preferable. Follow the signal from the input and check the output waveform of each transistor. Where the waveform departs from normal, the trouble is in that portion of the bridge. Since the inputs to Q4 and Q2 are taken from the emitters of Q1 and Q3, it will be normal to find the amplitude of Q1 and Q3 larger than that of Q4 and Q2. The emitter outputs of Q1 and Q3 will be of the same phase as their inputs, while the outputs of Q4 and Q2 will be oppositely polarized with respect to their inputs, because of the common-emitter connection.

Distorted Output. Distorted output may be caused by a defective transistor, improper collector voltage, or too large a drive (input signal). The collector voltage may be checked with a voltmeter to determine whether it is normal. Too large an input signal will cause clipping of the signal in the output circuit, as in other amplifier circuits. Too low a collector voltage will produce bottoming, a form of clipping which results when the supply voltage cannot follow the peak signal demands. Hence, it is almost mandatory to use an oscilloscope to check the signal waveform through the circuit. Flattening of the signal at the peaks or troughs of modulation indicates clipping and the resultant distortion. If RI and R2 and the load are the proper value, and the supply voltage is normal, the transistors are defective.

# FEEDBACK AMPLIFIERS

**General.** Feedback amplifiers are divided into two basic types, those employing positive feedback, and

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those employing negative feedback. Positive feedback consists of feeding back a portion of the signal inphase with the input so that the overall output is increased because of the feedback. If left uncontrolled the additional output, in turn, supplies a proportionately larger input and the overall output is further increased. This cumulative effect of building up the signal amplitude is termed *regeneration* When the output of an amplifier is fed back into the input in a regenerative manner the final result is to cause the circuit to oscillate at some particular frequency or over a small range of frequencies. Thus the r-f osciUator is basically a regenerative feedback amplifier, which eventually stabilizes at some maximum amplitude. Generally speaking, the use of positive feedback is restricted to oscillators, or special regenerative receivers operating at radio frequencies. It is also used sometimes at lower frequencies (within the audio range) to supply high gain over a single stage of amplification, which is controlled by additional stages with negative feedback.

When the feedback is made 180 degrees out-ofphase with the input signal so that it reduces the overall output of the amplifier, it is considered to be degenerative and is known as negative or rnverse feedback. Although the application of negative feedback reduces the gain of the amplifier below that which would normally be obtained without feedback, it provides many desirable features. In general, it improves the behavior of the system, and increases the bandwith. It improves the linearity of the system, and consequently produces less intermochdation and harmonic distortion. At the same time, the input impedance is increased and the output impedance is decreased. Any noise generated within the amplifier system itself is reduced, but it has no effect on any externally induced noise. Since a portion of the output is fed back to the input, any change in circuit values is in effect automatically compensated for, so that the circuit gain is stablized. The following graph shows the overall frequency response and gain for an amplifier without any feedback, an amplifier with 3 dB of negative feedback, and one with 15 dB of negative feedback. Although the overall amplification is decreased by the feedback, the frequency response is increased, and is made flatter over a greater range. The peaks occurring at the extreme low and high frequencies are due to phase shift caused by reactance effects changing the feedback at these frequencies from negative to positive. The loss of amplification

when feedback is used can be recovered by employing additional stages of amplification. In fact, with good design it is possible to use a single stage of positive feedback to provide the lost gain, with the remaining amplifier stages using inverse feedback. Typical positive and negative feedback circuits are discussed in the following paragraphs.



Typical Negative Feedback Response Curves

# POSITIVE FEEDBACK AMPLIFIER (DIRECT, REGENERATIVE) (ELECTRON TUBE)

## Application.

**The** positive feedback (regenerative) amplifier is used in audio and r-f stages to supply a greater output than is possible through normal gain in a single-tube amplifier.

### Characteristics.

Uses self-bias, but fixed bias may also be used if desired.

Provides the amplification of two or three tubes in a single stage.

A portion of the output voltage is fed back (inphase) with the input signal.

Distortion is increased in proportion to the amount of feedback.

Feedback may be accomplished by resistive, inductive, or capacitive methods.

Usually only one stage of positive feedback is employed.

Oscillation may occur at extremely low or extremely high frequencies because of reactance effects.

#### Circuit Analysis.

General. Because the electron tube amplifier inverts the signal in the plate circuit, it is necessary either to use a transformer to reverse the phase, or to pass the signal through another stage to obtain positive feedback. The input circuit operates as a mixer and adder, with the output signal being the sum of the input signal and the positive feedback voltage, multiplied by the gain of the stage. In r-f amplifiers, general practice is to couple a portion of the plate output back to the input through an r-f transformer, and to vary the coupling between the two coils mechanically or electrically to control the amount of feedback. Since the design and operation is unique for each application, the following typical circuit shows only one particular arrangement of positive feedback. It will serve, however, to illustrate and describe the basic principles and operation of positive feedback so that they can be applied in the analysis of similar circuits even though the circuits are not identical.

**Circuit Operation.** A typical cathode feedback arrangement using positive feedback to overcome degeneration provided by unbypassed cathode resistors with improved audio gain and response is shown in the accompanying schematic. The two-stage amplifier consists of a triode cathode-resistance-coupled stage driving a pentode transformer-coupled output stage. Capacitor Cl and resistor R1 form the RC



cathode Coupled Positive Feedback Amplifier

input circuit to triode V1. Cathode self-bias is provided by cathode resistor R3, and the output is developed across plate resistor R2. Capacitor C2 and resistor R5 are the plate RC coupling circuit for driving pentode V2, with cathode bias supplied by R6. Both cathode resistors R3 and R6 are unbypassed, which normally provides degeneration. However, by connecting the cathode of V2 to the cathode of V1 through feedback resistor R4, the positive feedback voltage cancels the degenerative effects of cathode resistor R3. Thus, the output of VI is increased by the feedback voltage. Resistor R7 is the screen voltage dropping resistor for V2, bypassed by C3. The output of V2 is transformer coupled through T1 to a loudspeaker or to another amplifier stage, as desired.

Assume a sine-wave input signal applied to Cl and is passed to the grid of Vl, appearing across R1. On the positive excursion of the signal, VI grid is driven in a positive direction. The increasing plate current through plate resistor R2 produces a negative-going output voltage, which is coupled through C2 to drive the grid of pentode V2. The negative driving voltage appears across R5, and causes the plate current of V2 to decrease. The changing plate current through the primary of output transformer T1 induces an output in the secondary. Screen voltage is obtained by dropping the supply voltage through R7, which is held at ground potential for audio voltage changes by screen bypass capacitor C3, so that the screen voltage remains a constant dc and is unaffected by the signal variations. When the plate current of V2 decreases with the negative driving signal, the cathode voltage developed across R6 is negative-going. A portion of this voltage is coupled back through feedback resistor R4 to the cathode of VI. Thus as the increasing plate current of V1 causes an increasing (positive-going) cathode voltage across R3, the negative voltage from V2 cathode cancels it and prevents the input signal from producing a degenerative cathode voltage on V1. Thus instead of the instantaneous bias on V1 increasing, it is held at the same level or even slightly decreased by the negative feedback voltage from V2 cathode. When the feedback is made sufficient to produce a slightly decreasing bias on VI, the output voltage is increased by this positive feedback. The effect is as though the grid input signal were increased.

On the negative-going **portion** of the input signal the opposite action occurs, The negative swinging grid

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voltage causes VI plate current to decrease, and produces a smaller bias across cathode resistor R3. At the same time, the plate voltage of VI becomes positivegoing and drives V2 grid in a positive direction. Thus the plate current of V2 is increased, and a higher cathode voltage is developed across V2 cathode resistor R6. This positive voltage, in turn, is fed back through R4 to the cathode of VI, which is the same as increasing the bias, or applying a larger negativegoing input signal. The plate output of VI, therefore, is greater. Since R4 is larger than R3 and R6, the cathode voltage developed across R3 has little effect on V2. Because of the feedback arrangement, the output resistance (plate resistance) of V2 is decreased to a lower value and less turns are needed on T1 to produce an appropriate output match, and a large power output is developed. The reduced turns on T1 produces a reduction in total capacitance between turns and increases the effective high frequency response over that which would normally be obtained.

Circuit Variations. A typical positive feedback circuit using a tapped output transformer to supply voltage feedback over a single stage is shown in the accompanying schematic. From an examination of the schematic, it is seen to be a conventional audio amplifier, with a resistance coupled input and transformer coupled output, except for the special feedback provisions. This consists of current limiting resistor R2 in series with V1 grid, and the feedback arrangement of R4 and C5 connected from the secondary of the output transformer back to the grid of V1. While T1 secondary is tapped, a similar arrangement may be produced by using an untapped secondary with a resistive voltage divider across it. The important point to remember about T1 is that the secondary is phased to produce a positive feedback signal Normally, the primary signal of **T1** is inverted from that of the input signal by conventional tube action, thus it is necessary that the secondary winding be phased so as to again invert the signal (otherwise an additonal stage of amplification would be necessay to complete the inversion). When the input signal is applied, assuming a positive-going sine wave, the increased psoitive signal on the grid of V1 causes an increasing plate current. This change of current through the primary of T 1 induces a positivegoing output in the secondary. The amount of feedback between the tap and ground is applied in shunt with the input signal, and both signals are combined

across R2. Thus the input signal is increased and the output likewise. On the negative-going excursion, the opposite action takes place. The decreasing plate current through the primary of T1 induces a positivegoing voltage in the secondary, which is phased by reversing the winding to be a negative-going signal, and a portion of this voltage is fedback through R4 and C5 to enhance the negative swinging input signal and further decrease the output. By using capacitor C5 the feedback becomes phase controlled. The larger the feedback capacitor, the greater the effect on low frequencies, while R4 acts as an attenuator and a phase shifting resistor. With proper proportioning of these parts the feedback is stabilized and prevented from developing into negative feedback (because of excessive phase shift at the low frequencies). However, positive feedback used alone tends to increase distortion, hence it is usually combined with negative feedback in following amplifier stages to accomplish the increase of gain with reduced distortion.



Transformer Coupled Positive Feedback Amplifier

#### Failure Analysis.

**No Output.** Lack of plate voltage, improper bias, as well as a defective tube, open coupling capacitors or output transformer can produce a loss of output. Measure the plate and bias voltages with a high resistance coltmeter. If no voltage appears on the plate of V1, R2 is open, while if no voltage appears on V2 plate, the primary of T1 is open or shorted to ground. Use an ohmmeter to check for resistance and shorts — to ground. If no signal appears at the input on V1

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## **ELECTRONIC CIRCUITS**

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grid when using an oscilloscope, coupling capacitor Cl is open. Likewise, if a signal appears on VI plate but not on V2 grid, coupling capacitor C2 is open. If a signal appears on V2 grid but not on V2 plate, either V2 is defective, or screen resistor R7 is shorted by capacitor C3. If screen resistor R7 is open, a small output signal will appear on V2 plate because of the tube acting like a triode. If V2 is considered at fault replace it. When a signal appears on the grid of V1, but does not appear on the plate and the measured cathode bias is normal, replace VI. If cathode resistors R3 or R6 are open no signal can appear on either V1 or V2, respectively.

> Low Output. Low screen or plate voltage will produce a low output. Check for proper plate, bias, and screen voltage with a voltmeter. Too high a bias caused by heavy plate current from an external short or defective tube will cause the tube to operate near saturation or cutoff and reduce the output accordingly, usually with noticeable distortion. If feedback resistor R4 **opens** degeneration will cause a reduced output. If C2 is leaky, the bias on V2 grid will show positive and the tube will be held in heavy saturation producing little or no output.

> **Distorted Output.** With positive feedback it is normal for greater distortion to occur than for the same stage without feedback, unless compensated for by a later stage using negative feedback. Excessive distortion can be caused by low plate or screen voltages or by improper feedback voltage. There may even be oscillation occuring at extremely low or extremely high frequencies because of phase shift effects. Use an oscilloscope to follow the **signal** through the circuit and note where the distortion appears, then check the associated parts.

# NEGATIVE FEEDBACK AMPLIFIER (INVERSE, DEGENERATIVE) (ELECTRON TUBE).

#### Application.

Negative feedback is used in speech amplifiers, modulators, and high-fidelity sound systems to improve the overall response and stabilize the gain.

## Characteristics.

Uses self bias, but fixed bias may also be used, if desired.

Usually requires an additional stage or more of amplification to make up for the loss produced by negative feedback.

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A portion of the output voltage is fed back outof-phase with the input signaL

Distortion is decreased in proportion to the amount of feedback.

Oscillation may occur at extremely low or high frequencies because of adverse phase shifts causing the feedback to change to positive instead of negative.

Noise or distortion generated within the amplifier is always reduced.

Externally induced noise (such as thermal noises generated in preamplifier stages) is not affected.

Bandwidth and linearity of the system is improved, and output impedance is reduced.

Change of circuit values is automatically compensated for so that circuit gain is stabilized and operation is improved.

#### Circuit Analysis.

**General.** There are many methods of developing negative or inverse feedback. It may be used over a single stage or over a number of stages (usually not more than three). Since the feedback must always be degenerative, and odd number of stages are usually used. Either voltage or current feedback may be employed. Although the circuit is usually arranged so that the feedback is accomplished in series with the input signal, it may be connected in shunt, if desired.

The accompanying block diagrm shows the manner in which feedback is normally accomplished.



Typical Inverse Feedback Arrangement

The total output voltage is made up of two parts: that resulting from the input voltage  $e_{in}$  and that resulting from the feedback input  $\beta e_0$ . The first part consists of fundamental output ef which is equal t.  $\mu e_{in}$ , plus harmonic and intermodulation distortion components  $e_h$ , plus any noise  $e_n$  generated within the stage. The sum of these components is the total output  $e_{o}$ , which would normally exist without feedback. With feedback voltage  $\beta e_{o}$  applied to the input, the second part of the output voltage is  $\mu\beta e_{o}$ , which contains a portion of all the three previously mentioned components, plus new harmonic and intermodulation distortion components. Since the feedback opposes the normal signal, the noise and harmonics are reduced by the inverse feedback to a negligible value, and the fundamental output is also reduced. Mathematically it can be demonstrated that both the fundamental, harmonics, and noise are reduced by the factor 1/1-L@, where  $\mu\beta$  is the feedback factor.

**Circuit Operation.** The accompanying schematic shows a typical two-stage triode inverse feedback amplifier.



Two-Stage Triode Negative Feedback Amplifier

Except for the feedback connection, VI and V2 form a conventional triode resistance coupled amplifier chain, using an output transformer in the final stage. The negative feedback is inserted in series with the cathode bias resistor of VI through a voltage divider consisting of R6 and R7 connected across the secondary of the output transformer. When a positive input signal is applied, it passes through Cl and appears across grid resistor R1, driving the grid of V1 in a positive direction and increasing plate current flow. The increased plate current flow through plate resistor R3 causes a voltage drop, which is applied as a

negative-going driving voltage through C3 to the grid of output amplifier V2. For the moment, assume that V1 cathode resistor, R2, is grounded, so that only the dc bias developed by average current flow appears. Since R2 is bypassed by C2, any instantaneous changes in signal current have no effect on the bias and full tube amplification is obtained. With the negative driving voltage from VI appearing across grid resistor R4, V2 plate current reduces, and the reduction of current through the primary of T1 induces an output voltage into the secondary winding of the output transformer. V2 is also cathode biased, with average plate current flow through R5 developing the dc bias, and is bypassed by C4 so that the signal variations have no effect on bias voltage. With the positive side of the T1 secondary comected to voltage divider R6 and R7, a positive-going portion of the output voltage taken across R7 is applied in series with cathode resistor R2 of tube V1 (R2 is grounded through R7). Thus, this small portion of positive output voltage instantaneously increases the cathode bias, reducing the output accordingly.

When the input signal goes negative the opposite action ensues, a negative output voltage is developed across the feedback voltage divider, and is applied to the V1 cathode to decrease the bias and increase the output. In both instances, the feedback voltage acts in opposition to the normal effect of the input signal, just as if a voltage 180 degrees out-of-phase with the input signal was inserted on the grid of V1. Since the feedback voltage is only a fraction of the input (about one tenth), the input signal is only slightly reduced, but the additional amplification obtained through the gain of the amplifier increases the amount of feedback voltage in the plate of the output stage. Thus, the overall gain is considerably reduced over what it would normally be without feedback. The net effect is to flatten out the amplifier response curve so the gain at low, mid-ban, and high frequencies is about the same. Hence with a flatter response greater fidelity is obtained, Any hum produced by the final amplifier supplies a correcting feedback voltage which effectively cancels and reduces the hum, and any harmonic distortion is affected likewise. When the input signal is increased in amplitude, the output also increases but the gain remains relatively constant because of the feedback. Thus the amplifier may be driven harder and still produce better fidelity and less distortion than without feedback. The limit

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of drive is reached when grid current flows in the input stage, since the input signal itself becomes distorted and feedback will not correct this condition. With proper design, up to three stages of high gain amplification may be used. Beyond this, excessive phase shift is produced through the feedback, network, so that the feedback changes from negative to slightly positive at the low and high frequency ends of the response curve and usually causes oscillation and distortion, which makes the extra amplification useless.

# Failure Analysis.

**No Output.** An open input, cathode, or plate circuit, lack of plate voltage, or a defective tube can cause a loss of output. Check the plate voltage and cathode bias with a high resistance voltmeter. This will verify that resistors R2, R7, and R5, as well as R3 and the primary of T1 are not open, and that neither C2 or C4 is shorted. Check for an input signal using an oscilloscope, if the signal appears at the input but not on the grid of Vl, either Cl is open or V1 has a grid to cathode short. If V1 is good, check the capacitance of Cl with an in-circuit capacitance checker. If the signal appears on the grid but not on the plate, and normal plate voltage exists, VI is probably defective. If the signal appears on the plate of V1 but not on the grid of V2, capacitor C3 is open or V2 is defective. If the condition persists check the capacitance of C3. If the signal appears on the grid of V2 but not on the plate, either the tube is defective

or T1 primary is shorted. A resistance check will determine if T1 is shorted. If the signal appears on the plate of V2 but not at the output, the secondary of T1 is either open or shorted. Check the resistance and continuity of T1 with an ohmmeter.

Racked Output. If the plate voltage is low, or the cathode bias is too high, there will be a reduction of output. A defective tube can cause both low plate voltage and high cathode bias, because of heavy conduction due to a shorted condition. Likewise, low emission will also cause a reduced output. Check the plate and bias voltages with a voltmeter if the condition persists, since aging plate or bias resistors may increase in value and cause either a reduction of plate voltage or bias, or both. If either coupling capacitor Cl or C3 is leaky or shorted, the output will be reduced because of improper bias (plate voltage from the preceding stage will be applied the grid). If either the primary or secondary of T1 is partially shorted or develops a low leakage to ground the output will be lower than normal. If an oscilloscope check shows all grid "and plate signals normal except that for V2 plate, transformer T1 maybe defective.

**Distorted Output. Since** the negative feedback practically eliminates harmonic distortion, excessive distortion indicates failure of the feedback loop. Check R6 and R7 with an ohmmeter for the proper value. Check to be certain that the input signal itself is not causing the distortion. Any other condition will be revealed by bias and plate voltage checks. Too low or too high a bias or too low a plate voltage can cause distortion.

# PART 5-3. PHASE IN VERTERS

# TRANSFORMER TYPE PHASE INVERTER (ELECTRON TUBE)

#### Application.

The transformer type of phase inverter is used for driving push-pull amplifiers, in public address systems where grid current flow is sufficient to cause distortion in other types of inverter circuits.

# Characteristics.

**Uses an output transformer** with a common secondary center tap.

Uses self bias, although fixed bias may sometimes be used.

Provides maximum output and gain.

Output amplitude is primarily determined by the transformer turns ratio.

Frequency response is uniform over a range of approximately 100 to 5000 Hz.

Two outputs, balanced with respect to ground, are supplied.

# Circuit Analysis.

The transformer type of phase inverter is basically a transformer coupled audio amplifier with a center tapped secondary. When the center tap is grounded, two opposite polarity outputs are produced which are essentially out of phase with respect to each other. Thus, a single input signal will provide a dual output with polarity and correct phases for driving a push pull stage. Because the transformer secondary has a low dc resistance, this type of circuit is usually employed where grid current is drawn, such as in Class B push-pull stages. While also classed as a phase splitter and paragraph amplifier, these terms are considered to be more applicable to other types of inverters which use special circuit arrangements to obtain the phase difference and dual output.

**Circuit Operation. The** schematic of a typical transformer type of phase inverter is shown in the accompanying illustration. A triode tube is employed for simplicity, since it will usually supply sufficient drive (output) for moderate powered push-pull amplifiers. Where greater power or drive voltage is required, a pentode tube may be used, or an additional push-pull driver stage can be added.



Transformer Coupled Phase Inverter

The high impedance resistance coupled input uses  $C_c$  as the coupling capacitor and  $R_g$  as the triode grid resistor. Cathode bias is supplied through cathode resistor  $R_k$  bypassed by  $C_k$ . Plate voltage is applied to V1 through 'he primary of T1. The secondary of T1 is center tapped, and the outputs are obtained between each end of the winding and the center tap.

With no signal applied, tube V1 is resting in the quiescent condition, with the voltage drop across cathode resistor  $R_k$  supplying Class A bias (plate current flows continuously for the whole cycle). Cathode bypass capacitor  $C_k$  prevents degeneration so that instantaneous plate current variations have no effect on the bias. (Refer to the introduction to this section of the handbook for a discussion of cathode bias.)

When a positive input signal is applied, the grid of V1 is driven positive and increased plate current flows. The increased plate current flow through the primary of transformer T1 produces a greater magnetic field linking the windings and causes a voltage to be induced in the secondary. With a center tap provided at the electrical center of the winding, two outputs can be obtained, as shown by the polarity indicated in the schematic. With opposite polarities, these outputs are of the proper phase for driving a push-pull stage. When the positive half-cycle is completed and the negative half-cycle begins, assuming a sine wave input signal, plate current is reduced. The reduction of plate current flow through the primary of T1 induces a voltage in the opposite direction in the secondary, because the direction of the magnetic

field is now changed. Thus a negative output is produced during the negative half-cycle. The polarity of the secondary winding is now opposite that shown on the schematic. However, because of the grounded center tap, points 1 and 2 on the winding will be of equal amplitude, but of opposite polarity, or phase.

#### Failure Analysis.

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**No Output.** Lack of plate voltage, improper bias voltage, as well as a defective tube will cause a loss of output. Loss of plate voltage or improper bias, may be determined by making a voltage check with a **volt**-meter. With plate voltage at the supply but not on the plate of VI, transformer T1 primary is open of V1 is shorted. With V1 shorted there will be a larger than normal voltage drop indicated across the primary resistance of T 1. Replace V1, and recheck the plate voltage, and no output, either grid resistor  $\mathbf{R_g}$  is open or the secondary of T1 is open. Make a resistance and continuity check of these parts with an ohmmeter to determine which is at fault.

Low Output. Low plate, or high bias voltage, as well as a defective tube can cause a low output. If abnormal plate current is drawn, the plate voltage of V1 will be lower than normal and the cathode bias will be higher than usual and thus less output will be obtained. Use a voltmeter to check plate and bias voltages. If bias and plate voltages are normal, replace V1 with a good tube, since low tube emission can also cause a reduced output. If the low output condition persists after tube replacement, transformer T1 is probably defective. A slight increase in plate voltage with a reduced primary dc resistance, as checked with an ohmmeter, coupled with poor low frequency response is an almost positive indication of a partially shorted primary. Any short or high resistance condition in the secondary will usually show on a resistance check of the secondary, and will probably cause a reduction in one of the output signal amplitudes, if not in both. Use an oscilloscope or VTVM to compare output voltage indications.

**Distortion. Use** an oscilloscope to observe the input signal waveform and amplitude, then check the output waveforms. If any difference of waveform occurs between the two output signals. the distortion is probably caused by the tube or transformer, particularly when normal plate and bias voltage readings are obtained.

# SINGLE-STAGE PARAPHASE INVERTER (ELECTRON TUBE)

# Application.

The single-stage paraphase inverter supplies a push-pull output from a single-ended input. It is used mainly to drive audio push-pull power amplifiers in public address systems, or modulators, and in receiver audio-stages.

#### Characteristics.

Self-bias is usually used although fixed bias maybe used, if desired.

Two out-of-phase outputs are provided, one from the plate circuit, and one from the cathode circuit.

Frequency response is relatively uniform from about 100 to 15,000 Hz.

Either triodes or pentodes may be used (pentode provides slightly higher output with improved high frequency response).

Provides less gain than is possible with transformer coupling (output is always less than the input).

#### Circuit Analysis.

General. The single stage paraphase inverter, also known as a *phase splitter* utilizes the phase inverting property between the grid and plate of the electron tube to supply a 180 degree out-of-phase output. The plate output together with an in-phase output, which is taken from the cathode, provides the desired pushpull output. Since balanced signals are desired, the amplification is limited to that which can be obtained from the cathode, which is always less than unity for a cathode follower. Thus, when plate and cathode outputs are made equal, the output is always less than the input signal. This circuit, however, is more economical to produce and has a better overall response than the transformer coupled circuit. Hence it is usually used in lower priced equipment. For best results two-tube paragraph circuits are preferred, since the overall amplification and" response may be arranged to provide better performance with a large output than either the transformer coupled, or the single-tube stage.

**Circuit Operation.** The schematic of a typical single-stage paraphase inverter is shown in the accompanying illustration.

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Single-Tube Paraphase Inverter

The input signal is RC coupled through Cl and R1 to the grid of triode V1. Cathode bias is supplied by R3 bypassed by capacitor C4. The outputs are developed across plate load resistor R2, and cathode load resistor R4, and are capacitively coupled to the pushpull driver or output stage by C2 and C3.

With no signaf applied, V1 rests in the quiescent condition with Class A bias supplied by cathode current flow through cathode resistor R3. Since grid coupling resistor R1 is returned to the ground side of R3, any voltage developed across R4 by cathode flow has no effect on the bias between the grid and cathode of VI. Furthermore, since the voltage developed across R4 in the quiescent condition is steady (de) no output appears from coupling capacitor C3. Likewise, any plate voltage drop developed across plate resistor R2 is also a steady dc and no output appears from C2.

Assume a sine-wave audio input signal is applied to the input terminals. During the positive excursion, the grid of VI is driven in a positive direction in the conventional manner and an increasing plate current flows. When plate current increases, electrons flow from ground, through R4 and C4 (which bypasses R3), within the electron tube from cathode to plate, and through plate resistor R2 to the voltage supply, creating the polarities shown on the schematic. Note that the cathode voltage is positive, is in phase with and folfows the input signaf, while the plate voltage drop is negative and out-of-phase with the input signal. Since these two voltages are constantly varying at an audio frequency they appear as outputs across C2 and C3, and ground. The values of R2 and R4 are made approximately equal so that equal amplitude output signals are produced.

When the input signal reaches its peak positive excursion and swings in a negative direction, the plate and cathode current through V1 is reduced, and the output voltage is reduced, likewise. As the input signal reaches the zero level and swings down into the negative region, the polarities across R2 and R4 are reversed. That of R2 rises towards the plate supply source and becomes positive-going, while that of R4 continues towards zero, drops below the quiescent level and is effectively negative-going because of the reduced cathode current flow. Again, two oppositely polarized (phased) and equaf output signals are produced from the single input signal. Thus as the input varies at audio frequency, the cathode and plate outputs do likewise, but oppositely. Since R3 is bypassed for audio frequencies by C4 the bias remains unaffected by the signal current variations. (See explanation of cathode bias given in the introduction to this section of the handbook.

As long as R2 and R4 are equal, and C2 and C4 together with their coupling (load) resistors ( $R_L$ ) are equal, the frequency response of both circuits is almost identical. At frequencies about 20 kHz the plate output of VI tends to drop off because of the effect of the appreciable triode grid-plate capacitance which is usually larger than the grid-cathode interelectrode capacitance. Therefore, where higher audio frequencies are desired, the pentode tube is used instead of the triode so that its reduced interelectrode capacitance minimizes this effect.

# Failure Analysis.

**No Output.** Open input or output circuits, a defective tube, improper bias, or lack of plate voltage can result in loss of output. Check the bias and plate voltages with a voltmeter. Use an oscilloscope to observe the input waveform and follow it through the circuit from grid to cathode to plate, and then across the outputs. If an input appears across the input terminals but no signaf appears on the grid, coupling capacitor Cl is open. If the grid of V1 reads positive — Cl is shorted or leaky. When checking the bias across

R3, measure from grid to cathode using the proper polarity, and then from R4 to cathode. If the grid to cathode reading is zero, grid return resistor RI is open. If an output appears across R4 but does not appear on the plate of V1, either the tube is defective or R2 is open. With plate voltage present from R2 to ground, V1 is defective (if the voltage is equrd to the supply on both sides of R2, the resistor is shorted). When an output appears on the plate of VI but not at the output load, coupling capacitor C2 is open. If Cl is shorted the **plate** voltage of the preceding stage will drive V1 into saturation, a constant high voltage will appear across R4, and a constant low voltage across R2 (on the plate of V1) and no output will be obtained.

Low Output. Insufficient bias on VI due to R3 changing to a low value (or if C4 is shorted) will cause a low plate voltage and a high cathode voltage, and reduce both outputs. If Cl is leaky the grid of V1 will show a positive voltage to ground. If RI is open the grid of VI will tend to block or build up a higher than normal bias, operating at or near cutoff with reduced output. If V1 is leaky or gassy, a positive voltage cause by grid current flow will appear between grid and ground. Should normal bias and plate voltage be indicated by a voltmeter but low output still exists, tube VI may be low in emission and produce a much weaker than normal signal. When operating properly, the cathode and plate outputs will be equal and just slightly less than the input signal amplitude, because of cathode follower action reducing the gain to less than unity.

Distorted Output. Normally, the output signal will be of the same shape and of only slightly less amplitude than the input signal. Use an oscilloscope to observe the input and output waveforms, with a constant sine-wave input signal applied. Flat-topping or rounding off of the positive peaks of the output signal indicate distortion caused by low emission or reduced plate voltage on VI. If the plate voltage is normal and flat topping occurs the tube is defective. If the tube is operated with too high a bias (near cutoff) the peaks will also be clipped when the tube is driven to cutoff. If cathode bypass capacitor C4 is open, the bias on VI will change with the signal, and amplification will not be linear, some amplitude distortion will occur and degeneration will cause a drop in output at the signal peaks. For small input signals little or no distortion will be observed. However, on large signals the bias may be driven into the

cutoff region causing bursts of distortion. If C4 is open, the cathode bias will vary instantaneously with the input signal variations and show on a voltmeter as a constantly varying (instead of a steady) voltage. With normal plate and bias voltages, distortion can also be caused by overdrive (too large an input signal). When the distortion observed on the oscilloscope at the outputs disappears as the input signal amplitude is reduced overdrive (or improper biasing) is the cause. Since output coupling capacitors C2 and C3, together with the associated load resistance  $R_{L}$ , are in parallel across the plate and cathode resistors, any change in these components or in the load can create some distortion. Such a condition will usually create an inbalance and result in different output amplitudes. Leaky coupling capacitors will show a positive voltage on the load side as well as on the plate or cathode sides and are easily detected by a high resistance voltmeter.

# SINGLE-STAGE PARAPHASE INVERTER (SEMICONDUCTOR)

#### Application.

**Same application** as electron tube version.

### Characteristics.

Requires more drive than for a single-stage amplifier.

Supplies two outputs with one input signal.

The outputs are oppositely polarized and of approximately the same amplitude.

The bias and load resistance are selected to provide equal output signals.

Provides better frequency response than is possible with an input transformer.

Is Class A-biased for equal swings; normally does not use either Class AB or B operation.

Is usually fixed-biased, but self-biased applications may be encountered.

# Circuit Analysis.

**General.** Where a single-ended stage is used to drive a push-pull amplifier, it is necessary to supply two oppositely polarized input signals to the push-pull stage. While a center-tapped transformer may be used, it has been found that RC coupling generally provides better frequency response, with a saving in economy

through elimination of the transformer, plus a reduction in weight and space. The use of the paraphase inverter circuit provides the necessary dual output. The unbalanced paraphase inverter uses a load in the emitter and a load in the collector to develop the oppositely polarized outputs, and is sometimes referred to in other publications as the *split-load* circuit. Actually, the load is not split; identical load resistors are used to obtain equal output amplitudes. A balanced output condition may be obtained in the single-stage paraphase inverter by adding another resistor, as will be explained-later.

**Circuit Operation. The accompanying** schematic is that of a one-stage unbalanced paraphase inverter.



**One-Stage Unbalanced Paraphase Inverter** 

Fixed voltage-divider bias is supplied by resistors RI and R2. (See the introduction to this section of the handbook for a discussion of bias arrangements.) The bias is normally Class A with the transistor operating at the center of its dynamic transfer curve. Thus, equal swings about the bias point (with equal loads) will produce equal output signals. R3 is the collector load, and R4 is the emitter load. Both loads are of the same value to produce equal output signals, which are capacitively coupled through  $C_{cc1}$  and  $C_{cc2}$  to the push-pull stage.

When a negative input signal is applied to the base of Q1, it adds to the forward bias of Q1 and causes the emitter and collector currents to increase. Electron flow is in the direction indicated by the arrows. The emitter current flowing through R4 produces a

negatively polarized signal, while the collector current flowing through R3 produces a positively polarized signal. Since R3 and R4 are identical in value, and the collector current is practically equal to the emitter current (less the small amount of base current), equal-amplitude output signals of opposite polarity are produced. On the opposite half-cycle of operation, the input signal becomes positive and reduces the forward bias, thus reducing both the emitter and collector currents. In this instance, assuming that the drive is such as to almost stop conduction, the collector output becomes negative and almost equal to the supply voltage. Simultaneously, the emitter cur. rent is reduced almost to zero and the emitter becomes positive with respect to the collector. Thus, the emitter and collector outputs change polarity as the input signal changer; the emitter output signal is in-phase and the collector output signal is out-ofphase with the input signal.

Unfortunately, the collector output impedance is higher than the emitter output impedance, and an unbalanced output condition results. Even though equal-amplitude output signals are developed, the push-pull input is basically mismatched for the emitter output and matched for the collector output. As a result, distortion occurs with strong signals.

A balanced output is provided by connecting R5 (shown dotted in the schematic) between the emitter and  $C_{cc2}$ . In this case, the input impedance becomes high for both push-pull transistors, since the impedance of the emitter is now determined by R4 and R5 connected in series, and their total value is chosen to provide an impedance equal to R3. Thus, the distortion produced by strong signals is eliminated. Because a voltage drop occurs across R5, R4 is made larger than R3 to compensate for the loss in output \_ voltage which would otherwise occur.

Since R4 is unbypassed, the voltage developed at the emitter is degenerative, and in effect opposes the input voltage in essentially the same manner as negative feedback; thus, a larger driving voltage must be applied to the base of the phase inverter than would normally be required for an amplifier without feedback. Where this input drive is limited or unavailable, a two-stage paraphase inverter is generally used because of its reduced drive requirements.

# Failure Analysis.

General. When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of

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shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false lowresistance reading.

No Output. Lack of supply voltage, no input signal, a defective transistor, or an open collector resistor (R3), emitter resistor (R4), or bias resistor (R2) will produce a no-output condition. The supply voltage can be checked with a voltmeter, and the voltage to ground checked from the emitter, base, and collector, to determine whether normal voltages exist and whether resistor R2, R3, or R4 is open. With an abnormally high voltage between the base and ground, Ql will be driven into saturation (this indicates that R2 is open). If R2 is shorted, or no input signal is applied, a no-output condition will also exist. If either R3 or R4 is open, emitter and collector current flow will be interrupted and no output will be developed. If either R3 or R4 is shorted, only a single output will be obtained from the portion of the circuit which is not short-circuited. Both resistors would have to be shorted to cause a complete nooutput condition. Failure of coupling capacitors  $C_{cc1}$ and C<sub>cc2</sub> will cause loss of output only if they are both either open or shorted to ground; if only one capacitor fails, only one output will be affected. If either capacitor is leaky, a reduced-output condition rather than a no-output condition will occur.

Reduced Output. Low supply voltage, improper bias, changes values of load resistors R4 and R3 (or R5), as well as leaky or defective coupling capacitors, can cause reduced output. The supply voltage and bias may be checked with a voltmeter. However, if R2 were open and a voltage check were made between the base and ground, the voltmeter shunt would replace R2. If the shunt were nearly the same value as R2, a false indication of nearly correct value would be obtained. If the values of R3 and R4 (and R5 if used) increase, then the output signal amplitudes will be less, or unequal at best. With an audio input applied, follow the waveform through the circuit, observing it with an oscilloscope. When the waveform departs from normal, the location of the trouble should be obvious.

**Distorted Output.** If the bias or supply voltages are incorrect, the load resistance' is not of the proper value, or the transistor is defective, a distorted output

will be obtained. Use an oscilloscope to observe the waveform. Since the operation is Class A, equal swings about the bias point should produce equal-amplitude and undistorted outputs of opposite polarity. If overdriven, the tops and bottoms of the waveform will be clipped (a sine wave will appear as a rectangular wave). In the unbalanced circuit (where R5 is not used), strong signals will cause distortion to appear on the collector output but not on the emitter output. In the balanced circuit, strong signals should not cause distortion until they exceed the bias value, and then both outputs should be equally distorted.

# TWO-STAGE PARAPHASE INVERTER (ELECTRON TUBE)

# Application.

Same application as single-stage version.

#### Characteristics.

Self bias is usually used, although fixed bias may be used, if desired.

A single-ended input is converted into two out-ofphase outputs.

Amplification may be obtained in addition to the phase inversion.

Either triodes or pentodes may be used, with the pentodes providing higher gain and improved frequency response.

Inherently not self-balancing (usually requires rebalancing if tube is replaced).

Frequency response is relatively uniform from about 100 to 15,000 Hz.

## Circuit Analysis.

**General.** The two-stage paraphase inverter usually employs a single, dual-triode with each half-section connected as a separate amplifier-inverter. Both outputs are taken from the plate circuit, and full amplification can thus be obtained. This type of inverter uses a small portion of the output of one half-section (taken off of a voltage divider across the output) to supply the out-of-phase drive to the second halfsection. Balance is primarily determined by the stage gain of the tube. If the gain is different between two tubes (or two half-sections) the voltage divider ratio must be changed (or separate cathode bias resistors are used instead of a common cathode resistor) to

keep the outputs equrd. Since such balancing is difficult, the two tube circuit usually is subject to a slight unbalance. However, the large amplification possible permits the stage to be used both as a driver and phase inverter (and sometimes as an output stage) thus economically combing two stages into one.

**Circuit Operation.** The following schematic illustrates a typical two-stage triode paraphase inverter. Triodes are used to simplify the discussion.



#### Triode Two-Stage Paraphase Inverter

Pentodes operate in the same fashion as described below for triode operation, except for considerations of the effect of screen current and voltage (for the same plate voltage a larger swing is possible, and a greater sensitivity and output are obtained with a slight increase in overall frequency response).

The input to triode V1 is RC coupled through Cl and RI, while the inverted input to triode V2 is direct-coupled from voltage divider R5 and R6 connected across the output of VI (a circuit variation is to employ capacitance coupling and a grid return resistor from V2 to ground). Cathode bias is obtained individually from  $R_{k1}$  and  $R_{k2}$  bypassed by  $C_{k1}$  and  $C_{k2}$ , respectively. (In other circuit variations a common cathode resistor, either unbypassed or bypassed,

may be used. Where the single dual-triode is used and separate cathodes are supplied, the circuit shown in the schematic permits closer tube balancing.) Resistors R3 and R4 are the plate load resistors for tubes V1 and V2, respectively, and the outputs are RC coupled through C2, C3, and R5, R6, and R7. Capacitor C2 and voltage divider R5, and R6, provide the output labelled El and V1. The inverted input signal for V2 is obtained across R6. Thus R6 also serves as the grid resistor for V2. By direct-coupling from R6 to the grid of V2, any deleterious reactance effects produced by passing the signal through an additional coupling capacitor are avoided (the two coupling capacitors connected in series would reduce the effective low frequency response). Normal operating bias for VI and V2 is either Class A or Class A prime (AB) operation. Because the input for V2 is taken from across R6, and both R5 and R6 are in series with the grid of the following (output) stage, Class B operation cannot be used (grid current flow on the signal peaks through R6 would produce a distorted input to V2). With no signal applied, the circuit operates in the quiescent condition. Plate current flows through cathode bias resistors  $R_{k1}$  and  $\mathbf{R}_{\nu}$  providing normal **Class** A or AB bias. (See the introduction to this section of the handbook for an explanation of cathode biasing.)

Assume that a sine-wave input signal is applied to the grid of V1. As the signal goes through its positive-going excursion, the grid is driven in a positive direction causing the plate current to increase. The increasing plate current of V1 produces a voltage drop across plate load resistor R3, and reduces the instantaneous plate voltage. Thus a negative-going voltage is developed across R3 (during the positive half-cycle) and is applied to coupling capacitor C2. Since the signal is constantly changing the ac component appears across output resistors R5 and R6, which are connected in series between coupling capacitor C2 and ground. This is the output voltage El from tube VI. Resistor R6 is usually one tenth the value of R5, and together they form a voltage divider, so that one tenth of the output of V1 appears as an inverted exciting signal voltage which is applied directly to the grid of V2. This negative-going voltage on V2 grid produces a decreasing plate current in V2, and the voltage across R4 (at the plate of V2) rises towards the source (becomes more positive). The increasing positive-going plate output from V2 is coupled through C3, producing output voltage E2

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**across** R7. Thus the output of **V2** is opposite to that of VI in polarity (out-of-phase) completing the other half of the desired push-pull output. As the plate currents of V1 and V2 rise and fall, the cathode currents do likewise. However, since they are bypassed by capacitors  $C_{k1}$  and  $C_{k2}$ , they do not affect the steady bias voltage developed by average current flow through the cathode resistors.

When the input signal reaches its positive peak and reverses, conditions, likewise, reverse. The grid of V1 is now driven in a negative direction and the plate current of V1 falls. Output voltage E1 now becomes positive-going and continues to increase until the negative input peak is reached. Meanwhile, the voltage across R6 (which is applied to V2 grid) also rise in a positive direction with the plate voltage of V1. towards the voltage of the supply. Therefore, the grid of V2 is effectively driven positive, causes an increase a plate current and produces a negative voltage drop across plate resistor R4. This negative-going output is coupled through C3 and appears across R7 as output voltage E2. When the input signal reaches the negative peak and swings positive again towards zero level, conditions again revert to that of the initial halfcycle. Thus the positive and negative half-cycle of



**Triode Two-Tube Topped Plate Inverter** 

input signal control the grids of tubes V1 and V2 to produce relatively identicrd, but inverted and amplified signals (the relatively large current flow through the large valued plate resistors develops an output voltage much larger than that of the input voltage). Although V2 grid is excited by the output of V1, operation is practically instantaneous so there is no appreciable delay between the input voltage on VI and that on V2.

A circuit variation of the above described circuit is shown in the accompanying schematic.

In this circuit arrangement, the input to triode VI is also RC coupled through Cl and RI. However, the inverted input to triode V2 is capacitance coupled by C3 from plate voltage divider R3 and R4 connected across the plate output of V1. The grid of V2 is returned to ground through grid return resistor R5. Cathode bias is obtained individually from R2 and R6 bypassed by C2 and C5, respectively. (In other circuit variations a common cathode resistor, either unbypassed or bypassed, may be used. Where the single dual-triode is used and separate cathodes are supplied, the circuit shown in the schematic permits closer tube balancing). Resistors R3 and R4 are the plate load resistors for tube V1 while R7 is the plate resistor for V2, and the plate outputs are capacity coupled through C4 and C5. Normal operating bias for V1 and V2 is either Class A or Class A prime (AB) operation. With no signal applied, the circuit operates in the quiescent condition. Plate current flows through cathode bias resistors R2 and R6 providing normal Class A or AB bias (see the introduction to this section for an explanation of cathode biasing).

Assume that a sine-wave input signal is applied to the grid of VI. As the signal goes through its positive-going excursion, the grid is driven in a positive direction causing the plate current to increase. The increasing plate current of V1 produces a voltage drop across plate load resistors R3 and R4, and reduces the instantaneous plate voltage. Thus a negative-going voltage is developed across R4 (during the positive half-cycle) and is applied to coupling capacitor C3 to drive V2. Since the signal is constantly changing the ac component appears across plate resistors R3 and R7, which are connected to coupling capacitors C4 and C5. The output voltage from tube VI is El. Resistor R4 is usually one tenth the value of R3, and together they form a voltage divider, so that one tenth of the plate output of VI

appears as an inverted exciting voltage which is applied through C3 to the grid of V2. This negativegoing voltage on V2 grid produces a decreasing plate current in V2, and the voltage across R7 (at the plate of V2) rises towards the source (becomes more positive). The increasing positive-going plate output from V2 is coupled through C5, producing output voltage E2. Thus the output of V2 is opposite to that of VI in polarity (out-of-phase) completing the other half of the desired push-pull output. As the plate currents of VI and V2 rise and fall, the cathode currents do likewise. However, since they are bypassed by capacitors C2 and C5, they do not affect the steady bias voltage developed by average current flow through the cathode resistors.

When the input signal reaches its positive peak and reverses, conditions, likewise, reverse. The grid of V1 is now driven in a negative direction and the plate current of V1 falls. Output voltage El now becomes positive-going and continues to increase until the negative input peak is reached. Meanwhile, the voltage across R4 (which is applied to V2 grid) also rises in a positive direction with the plate voltage of VI, towards the voltage of the supply. Therefore, the grid of V2 is effectively driven positive causing an increase in plate current and producing a negative voltage drop across plate resistor R7. This negative-going output is coupled through C5 and appears as output voltage E2. When the input signal reaches the negative peak and swings positive again towards zero level, conditions again revert to that of the initial half-cycle. Thus the positive and negative half-cycle of input signal control the grids of tubes V1 and V2 to produce relatively identical, but inverted and amplified signals (the relatively large current flow through the large valued plate resistors develops an output voltage much larger than that of the input voltage). Although V2 grid is excited by the output of VI, operation is practically instantaneous so there is no appreciable delay between the input voltage on VI and that on V2.

In both of the circuits described, the gains of two tubes will vary slightly, and there is a difference in amplitude between the two outputs, unless the bias is changed slightly on one tube. Thus the circuit is seen to be inherently unbalanced, and it does not of itself provide any automatic balancing, as does occur in the cathode-coupled or in the differential types of paraphase circuits. While the circuit values are selected properly by the manufacturer and designer, it is usually necessary to change cathode and plate resistance values in one tube when a new tube is substituted, to minimize amplitude distortion (this does not authorize any modifications to be made to Navy equipment, since circuit design is presumed to adequately cover such a condition). In most cases the additional distortion produced by tube gain differences is within acceptable limits and is of academic interest only.

When dual-triodes with a single, common-cathode are used in this type of circuit, bias is obtained by a common cathode resistor. In some cases this cathode bias resistor is also bypassed by a capacitor, and a constant unbalance occurs due to the differences in gain between the two half-sections. In other instances, this cathode bias resistor is not bypassed. When unbypassed, the two instantaneous cathode currents flowing in opposite directions tend to cancel out, as in push-pull amplifiers, so that the steady state bias remains substantially constant. Any remaining signal effects which are not balanced out become degenerative, and add to the bias to reduce the total output. When properly designed, this helps to balance the output signals and provide an increase of linearity and a reduction of inherent distortion. Since these circuit variations are only effective to a limited extent, the self-balanced type of paraphase inverter is usually preferred for use where distortion is to be limited to a absolute minimum. Such circuits are discussed later in other paragraphs in this section of the handbook.

#### Failure Analysis.

No Output. An open input or output circuit, improper bias, or lack of supply voltage, as well as a defective tube can cause of loss of output. Check for the proper bias and plate voltage on V1 using a high resistance voltmeter. Too high a bias will almost produce plate current cutoff and reduce the output so low that it is practically no output at all. Measure the bias first from cathode to ground, and then from the grid to ground. If normal bias is obtained from cathode to ground but not from grid to ground, R1 is open. If input capacitor Cl is shorted, tube V1 will be driven into saturation by the plate voltage from the preceding stage driving VI grid highly positive. If Cl is open, no signal will appear on the grid side but will appear at the input (use an oscilloscope to observe the waveform). If a signal appears at the grid, and in inverted form at the plate of VI but not at the output, either coupling capacitor C2 (or C4 for the

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tapped plate inverter) is open or the output is shorted.

Checking the resistance of R5 and R6 to ground will quickly determine if the output is shorted, if not, then C2 (or C4) is open. Use a capacitance checker to determine if C2 (or C4) is satisfactory. With proper bias and plate voltage, and an input to VI but still no output, tube V1 is defective. Since the **output** of VI is used to supply an input for V2, the output of VI should always be checked first. When there is an output from V1 but not from V2, either the bias is **too** high, the plate supply or load is open, the output circuit is open or shorted, or tube V2 is defective. With normal plate voltage and cathode bias on V2 but no signal visible on the plate, tube V2 is defective. Check tube V2; if good, coupling capacitor C3 (or C4) is open, or the output is shorted.

Redueed Output. Improper bias, reduced plate voltage, or a defective tube can cause a reduced output. Check the bias and plate voltage with a high resistance voltmeter. The voltages should be within the limits shown in the instruction book. If the bias is too high on V1, the tube can be driven almost to cutoff on the negative peaks; or if it is too low, VI may be driven into saturation on the positive peaks. In either case there will be a reduction in output and distortion. Clipping of the waveform can easily be observed with an oscilloscope. If output E<sub>1</sub>is satisfactory, a similar set of conditions can cause a reduction of output in V2. Use the oscilloscope to observe the cathode, grid, and plate of V2. Any signal on the cathode indicates  $C_{k2}$  (C5 on the tapped plate inverter) is not properly bypassing or open. Lack of or low grid signal indicates improper voltage division, check R5 and R6 (R3 or R4 on tapped plate inverter) for normal resistance with an ohmmeter.

**Distorted Output.** Improper bias, low plate voltage, or a defective tube can cause a distorted output. Use an oscilloscope to follow the signal through the circuit from input to V1 grid and plate, to V2 grid and plate, and note when the distortion appears. Too low a bias will cause clipping on the positive peaks, and too high a bias will cause clipping on the negative peaks. Likewise, low plate voltage or low tube emission will also cause peak clipping. If plate voltage reads normal on the voltmeter, and clipping occurs on the positive peaks, the tube emission is low and insufficient to supply the peak current demand.

Since V1 drives V2, any distortion which appears on the output of VI will also appear on V2 grid, and

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will be amplified and appear in V2 output also. With V1 showing no distortion, and V2 distorted, check V2 bias and plate voltage. If these voltages are normal, V2 is probably in need of replacement. Because of the inherent unbalance of this circuit the outputs of **V1** and V2 will usually be slightly different, and a slight amount of distortion, say 1 to 2 percent, can be considered as normal operation. Make certain, also, that overdrive is not causing the distortion. Too large an input signal will cause clipping, which can be observed to disappear es the gain is reduced.

# TWO-STAGE PARAPHASE IN VERTER (SEMICONDUCTOR)

#### Application.

The two-stage paraphase inverter is used in receivers, public address systems, and modulators to produce sufficient power to drive a high-power pushpull stage from a single-ended input.

#### Characteristics.

Only a small input signal is necessary to drive the stages to full output.

Supplies two output signals for a single input signal.

The output phase (and polarities) are opposite and suitable for a push-pull input.

Operation is usually Class A, although Class AB or B applications may be encountered.

More than twice the power output of a single-stage phase inverter is obtained.

Distortion is **equal** to or less than that of the single-stage circuit.

#### Circuit Analysis.

**General.** The two-stage paraphase inverter uses two separate transistors operating at their full capabilities in the common-emitter circuit to provide a larger power output than the one-stage phase inverter circuit. Since the output is taken from the collector of each stage, there is no negative feedback in the emitter circuit to overcome (as in the single stage), so that less drive than that required for the single-stage paraphase inverter is required. As a result, more output power is obtained with less drive than for a single stage.

Circuit Operation. The schematic of a typical twostage PNP transistor paraphase inverter is shown in the accompanying illustration. Transistors Q1 and Q2 are basic common-emitter-connected amplifiers, each supplying a single output. Q2 is connected in cascade with Q1, but has R5 connected in series with the base to limit the current and drop the driving signal to a value equal to that applied to Q1. Thus, with the input signal to Q2 held to the same value as the input to Q1, the output of Q2 is made to equal the output of Q1; also, since the CE circuit produces an inverted output polarity, the two separate output signals are equal and oppositely polarized, and suitable for driving a push-pull stage. Fixed Class A bias is provided for both stages through voltage divider resistors; R1 and R2 bias Ql, while R6 and R7 bias Q2. (See the introduction to this section of the handbook for explanations of types of biasing and stabilization methods.) Resistors R4 and R9 are emitter swamping resistors used for thermal stabilization, and are bypassed by Cl and C2 to prevent degeneration. Since the capacitors bypass any ac component of the signal, they are affected only by dc current variations produced by changing temperature. When a temperature change increases the emitter current, it produces a dc voltage across the swamping resistors which oppose the operating bias and automatically reduces the emitter current to compensate for the temperature-



Two-Stage Paraphase Inverter

caused increase. Resistors R3 and R8 are the collector loads of Q1 and Q2, respectively, across which the output voltage is developed. The collector of Q1 is capacitively connected to the base of Q2 by  $C_{cc1}$ , and the push-pull outputs are coupled through capacitors  $C_{cc2}$  and  $C_{cc3}$ .

When a negative input signal is applied to the base of Q], the forward bias is increased and the emitter and collector currents are increased above the resting (or quiescent) value. Electron flow is from the emitter through C 1 to ground, and from the collector supply through R3 to the collector. As shown in the illustration, the collector output of Q1 is positive, and is applied through Cccl to the base of Q2 and through dropping resistor R5 to drive Q2. (The inverted output from the collector of Q1 is supplied to the push-pull circuit by C<sub>cc2</sub>.) The value of R5 is chosen to supply an input to Q2 just equal to the amplitude of the input signal applied to Q1. With a positive signal applied to the base of Q2, the forward bias is reduced and the emitter and collector currents of Q2 are reduced. Electron flow is from the emitter of Q2 through C2 to ground, and from the collector supply through R8 to the collector. Since Class A bias is used, and assuming that the base voltage applied to Q2 is just equal to the bias, collector current flow is reduced to zero and the collector voltage rises to that of the negative supply (both ends of R8 are negative with respect to ground). Thus, a negative output is obtained from the collector of Q2 and is applied through  $C_{cc3}$  as the oppositely polarized (in-phase) push-pull driving signal. Since Q2 operates practically instantaneously (there is no inherent delay), the two outputs appear on the push-pull grids simultaneously. (Note that passage through one stage inverts the signal, while passage through two CE stages returns the signal to the original polarity.)

Assuming a sine-wave input, when the negative half-cycle is completed the signal reverses, and a positive input is now applied to the base of Q1. The positive input reduces the forward bias of Q1 to zero (assuming full swing) and the collector voltage rises to that of the negative supply, thus producing a negative output. The large-amplitude negative collector output is dropped through R5 so that it is approximately equal to the input signal amplitude applied to Q1. This small negative input to the base of Q2 increases the forward bias and causes the collector current flow through R8 to increase. Electron flow is from the supply through R8 to the collector, which produces a

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positive voltage drop at the collector (the polarity of this voltage drop is opposite that of the previous half-cycle), so that the output from Q2 is now positive. Since there is no inherent delay in the operation of the transistor, the positive output from Q2 and the negative output from Q1 appear paretically simultaneously at the push-pull inputs.

Dropping resistor R5 acts as a balancing resistor to equalize the output of both stages. The transistors need only be of similar types; matched pairs are not required. The collector resistors are usually made equal so that identical currents will produce equal output voltages. Where little power is required, such as that needed to drive a conventional Class A pushpull stage, swamping resistors R4 and R9 and their associated bypass capacitors Cl and C2 may be eliminated from the circuit, and the emitters connected directly to ground. In applications where distortion becomes critical, the use of feedback from the collector is resorted to by connecting bias resistors RI and R6 to their collectors. In this instance resistors R2 and R7 could be eliminated by changing the values of both RI and R6. Thus, it is evident that the basic schematic may vary slightly, according to individual design, using different bias and stabilization methods. However, the operation is essentially the same since two stages of amplification are used to invert one of the outputs and thus provide a push-pull output.

# Failure Analysis.

General. When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false lowresistance reading.

No Output. Lack of collector voltage, improper bias, or an open R3, R4, or Cccl will prevent Q1 from driving Q2 and there will be no output. The same result will be obtained if **Q1** is defective. A defective Q2 or a component in that stage will affect only the output from Q2; the output from Q1 will be unaffected. Measuring the supply voltage, collector voltage, and bias with a voltmeter will usually indicate the portion of the circuit in which the defective part is located. If either R2 or R7 is open,

the bias will be determined by the internal baseto-emitter resistance of the transistors. However, when measured with a voltmeter from base to ground, the meter shunt will act as the lower portion of the bias divider, and cause a false indication. Check also for the presence of an input signal (use an oscilloscope or VTVM probe) since the phase inverter is usually RC-coupled to a preamplifier stage. An open output resistor or coupling capacitor in the preamplifier will not permit any input to appear at the base of Q1. Swamping resistor R4 or collector resistor R3, if open, will prevent the flow of emitter and collector current. If R4 is shorted, the circuit will be temperature-sensitive, but it will operate normally otherwise; with a shorted collector load resistor (R3), no output will be obtained from Q1 and, consequently, Q2 also. A leaky coupling capacitor, Cccl will not produce a no-output condition, but will cause partial clipping of the signrd and distortion. If shorted, the increase in bias will drive Q2 into heavy saturation, and, while the output Q2 will be lost, an output will still be supplied from Q]. If R5 is open, no output will be obtained from Q2; if R5 is shorted, the outputs of Q1 and Q2 will be greatly different in amplitude, and distortion will be present. If bias resistor R6 is opwn, contact bias will be placed on Q2; and thus the output will be distorted, and of larger amplitude than normal. If R9 is open, there will be no output from Q2. If collector resistor R8 is open or shorted, no output will be obtained from Q2. If the output coupling capacitors are open, no output will result; if they are otherwise defective, only reduced output will occur.

Reduced Output. Low collector voltage, improper bias, of a defective transistor can cause reduced output. Usually, a voltage check of the supply and bias will determine whether one or more of these voltages are at fault. If either of the swamping resistor bypass capacitors, Cl or C2 is open, the degenerative effect of the swamping resistors will cause reduced output and require greater drive in the stage affected. Since O1 drives O2, and open Cl will change both outputs; if only C2 is open; only the output of Q2 will be affected. A leaky coupling capacitor Cccl will improperly bias Q2 and cause a clipped and reduced output. If one or more of the coupling capacitors are completely shorted, the collector voltage will be placed on the following transistor base, cause heavy flow of forward current, and bias the transistor into saturation, thus reducing the output of the stage to a

ORIGINAL 491-044 0- 73 - 27 small value. When normal voltages and bias appear to be present, use an oscilloscope to follow the waveform through the circuit. When the waveform changes amplitude, the location of the trouble should be obvious. If all voltages and resistances check normal and yet the waveform is defective, then the transistor in that portion of the circuit is at fault.

Distorted Output. Improper bias or supply voltage, overdrive, or a defective transistor can cause distortion. Use an oscilloscope to check the waveform, after checking the bias and collector voltages with a voltmeter. Follow the input signal through each stage to the output, checking for proper amplitude and polarity. The signal at the collector of Q1 should be similar to that on the base, but of opposite polarity. The signal on the base of Q2 should be equal in amplitude to that on Q1, but of opposite polarity also. Both collector outputs to ground should be of equal amplitude but of opposite polarity. If the dc bias and collector voltages are normal but a distorted collector output occurs, the transistor is probably defective. Replace the transistor with one known to be good. Make certain that the input signal is undistorted; otherwise, the distortion will be amplified and inverted in passing through the circuit. Clipping of the peaks and troughs of the signal indicate that the input drive is too great.

# PARAPHASE, CATHODE-COUPLED INVERTER (ELECTRON TUBE)

#### Application.

The paraphase cathode-coupled inverter is used to drive a push-pull audio amplifier from a single-ended source. It is used in audio amplifier systems where self-balance together with amplification is desired, and good frequency response and a minimum of distortion is required.

# Characteristics.

Self bias is usually used, although fixed bias may be used, if desired.

A single-ended input is converted into two equal and out-of-phase outputs.

Amplification is restricted to about half the maximum value obtainable from a single tube.

Is self-balancing, with a relatively uniform frequency response of approximately 100 to 20,000 Hz. Either triodes or pentodes may be used, with the pentodes providing higher gain and slightly improved high frequency response.

# Circuit Analysis.

**General.** The cathode coupled inverter is usually used with dual triodes having a common cathode. This circuit offers a saving in space and weight over those of the two tube type of inverters with a slight reduction of components. The inherent self-balancing feature makes it particularly valuable for circuits requiring a minimum of distortion, since a slight amount of degenerative feedback occurs in the cathode circuit and improves the linearity. In addition there is no necessity to rebalance the circuit when tubes are changed, and hum due to cathodeto-heater leakage is kept to a minimum.

**Circuit Operation.** The following schematic illustrates a typical cathode-coupled paraphase inverter. Although separate cathodes are shown for simplicity and ease of discussion, the tube is actually a dual section triode with a common cathode.



Cathode-Coupled Paraphase Inverter

The input signal is RC coupled through capacitor Cl and grid resistor **R1** to the grid of triode VIA, a half-section of dual-triode tube V1. Cathode bias and signrd injection for tube VIB, the other half-section of VI, is provided through common cathode resistor R2. The outputs of both half-sections are also RC coupled to the following push-pull stage. Resistor R3 is the plate load resistor for VIA from which the

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out-of-phase output is coupled through C2, while resistor R4 is the plate resistor for VI B, and the in-phase output is coupled through C3.

In the quiescent condition with no signal applied, both VIA and VIB conduct and develop cathode bias across R2. The value of R2 is chosen so that the bias is set at the center of the tubes dynamic operating range, with about half normal plate current flowing through each half-section of V1. Since a push-pull output is produced, **the** cathode and plate current of one half-section **increases** while that of the other decreases. Thus the average bias remains substantially constant and there is no necessity for bypassing the cathode resistor.

When a sine-wave signal is applied to the input it is effectively passed through capacitor C 1 and appears across R1. Assume that the sine-wave is starting its positive half cycle of operation, the grid of VIA is driven in a positive direction, and causes an increased plate current to flow. Electron flow is from ground through cathode resistor R2, tube VIA, and plate resistor R3 to the supply. This electron flow creates an instantaneous polarity as shown in the accompanying simplified drawing.



Simplified Polarity Diagram For Positive Half-Cycle of Operation

As can be seen from the drawing, the cathodes of both VIA and VIB become more positive, while the instantaneous plate voltage is decreased by the voltage drop across R3, producing a negative output at the plate. This negative output is coupled through C2 to drive the next stage. The normal grid to plate phase-inverting property of an electron tube is used in this half-section to develop the **out-of-phase** signal. Meanwhile, with an increasing positive voltage applied to the cathode of VIB, you recall from basic theory that this is the same as applying a negative signal to the grid, and VIB plate current is, therefore, decreased. As the plate current of VIB is decreased, the plate voltage rises towards that of the supply, and a positive output is developed across R4. This posi. tive output is coupled through C3, as the in-phase signal, to drive the following push-pull stage. When the input signal reaches its positive crest, VIA is heavily conducting while VIB is lightly conducting, and opposite and equal output voltages are produced.

As the input signal changes direction and becomes negative-going, operation reverses and the instantaneous polarity becomes opposite that shown on the drawing. Thus tube VIA plate current reduces and VIB plate current increases. The cathode voltage developed across R2 also reduces, which is the same as driving VIB grid positive and causes VIB plate current to increase. A negative output is now produced by the voltage drop across plate resistor R4, and a positive output voltage is developed across R3 as the plate voltage of VIA rises towards the supply voltage with the reducing plate current. Thus the outputs are reversed to produce the negative half-cycle of input signal.

When the negative input signal peak is reached, operation again changes back to the original state with V1A plate current increasing while VIB plate current decreases.

# Failure Analysis.

**No Output.** Too high a bias, lack of supply voltage, an open input or output circuit, or a defective tube can cause loss of output. Check the bias and plate voltage with a high resistance voltmeter. With normal bias and plate voltage and no output, either there is no input signal or coupling capacitor Cl is open, or output coupling capacitors C2 and C3 are open, or the tube is defective. Use an oscilloscope

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and check for a signal on both sides of Cl. If the signal appears at the input but not on the grid side of the capacitor, it is open. Likelike, if the signal appears on the plate but not at the output, the associated output coupling capacitor (either C2 or C3) is open. If grid resistor RI is shorted no signal will appear on the grid of VIA also. A simple resistance check from grid to ground will reveal if the input is shorted. If both half-sections of VI are defective, or if VIA is defective no output will be obtained, but if only half-section VIB is defective an output will be obtained from VIA.

Low **Output.** Improper bias, low plate voltage, or a defective tube will cause a reduced output. If input capacitor Cl is shorted or leaky, a positive voltage will be applied to the grid of VIA, will cause a heavy flow of plate current and bias off the tube near the cutoff point. If extreme, practically no output will occur, otherwise, a reduced output will be obtained depending upon the amount of bias produced. Usually such a condition will be indicated by a high cathode bias, with a positive grid voltage, and a low plate voltage caused by the large drop through the plate load resistor, produced by the excessive plate current flow. If R2 changes to a lower value, the bias across R2 will tend to remain the same because a larger plate current flows, the increased flow of plate current will, however, cause a larger than normal drop across the plate resistor(s), reduce the plate voltage, and hence the output. If the emission of tube V1 is low, apparently normal grid and plate voltages may be measured on the voltmeter, but the output will be weak and distorted when a signal is applied since the plate current will not be able to follow the signal.

Distorted Output. Due to the common cathode and bias arrangement a decrease in plate current flow on one side will be compensated for by an increase on the other side. Hence distortion is kept to a minimum. Use an oscilloscope and compare the input, grid, and cathode waveforms; they should all be uniform and of the same relative amplitude. Now compare the plate and output waveforms. They should be identical and of larger amplitude. If distortion appears and is eliminated by reducing the input signal, overdriving is indicated. If distortion appears in the plate circuit but not in the grid circuit, either the tube needs replacing or the plate voltage or load is at fault. If either of coupling capacitors C2 or C3 are leaky, a reduced plate voltage may be produced because of voltage division effects across the next stage input resistors, and cause unbalance and distortion. Check the plate voltage with a voltmeter, if below normal, check the associated plate load resistance with an ohmmeter and check the coupling capacitor with a capacitance checker.

# DIFFERENTIAL PARAPHASE INVERTER (ELECTRON TUBE)

# Application.

The differential paraphase inverter is used to drive a balanced push-pull audio amplifier from a singleended (unbalanced) source. It is used in audio amplifier systems where high amplification and good balance is necessary.

#### Characteristics.

Self bias is usually used, although fixed bias may be used, if desired.

A single-ended (unbalanced) input is converted into two equal and out-of-phase outputs.

Almost full tube amplification is obtainable.

Circuit is self-balancing with a relatively uniform frequency response of 100 to 20,000 Hz or more.

Pentodes are used for high gain and increased high frequency response, but triodes may be used in special instances.

### Circuit Analysis.

**General.** The differential paraphase inverter uses the difference between the two output signals to supply the driving signal for the in-phase output. Pentodes are usually employed, since their high gain permits reducing the difference signal to such a small value that for all practical purposes the outputs can be considered identical. The method of obtaining the difference signal provides an effective negative feedback which stabilizes the gain through the circuit and improved its self regulating properties.

**Circuit Operation.** The following schematic illustrates a typical differential paraphase inverter.

The input signal is RC coupled through input coupling capacitor Cl and grid resistor R1 to the grid of V1. Cathode bias for V1 is developed across unby passed cathode resistor R2, and through R3, bypassed by C2, for tube V2. Screen voltage is obtained from the common plate supply source through series screen voltage dropping resistor R4, and the screens are

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Typical Differential Paraphase Inverter Circuit

bypassed to ground by screen capacitor **C3**. The suppressor elements of the tubes are connected to the cathode. Resistive plate loads and capacitive output coupling is provided. The output is developed across plate resistors R5 and R6, and is applied through C4 and C5 to the output voltage divider consisting of R7 and R9 connected in series with difference resistor R8 to ground. Resistors R7, R8, and R9 also function as grid resistors for the following push-pull stage driven by the inverter.

Tube V1 operates as a conventional resistance coupled amplifier, with the unbypassed cathode resistor providing a slight amount of degenerative feedback to improve the overall response and stabilize the gain. In the quiescent condition, with no signal applied VI, the cathode current consisting of the sum of the screen current and plate current flows through cathode resistor R2 to establish the normal bias level. With a steady screen current flow., a constant voltage drop is produced across screen resistor R4, and together with the screen current of V2, is sufficient to drop the plate supply to the desired screen voltage value. Since R4 is bypassed by C3, the screen voltage remains unaffected by any signal variations when the signal is later applied. Any dc voltage drop across plate resistor R5 reduces the plate supply to the desired quiescent plate voltage value, and no output is

produced. In a similar manner, V2 rests in the quiescent condition with its bias determined by the sum of the screen and plate currents (total cathode current) of V2 through separate cathode bias resistor R3. Since R3 is bypassed by C2, the bias on V2 also will not change with the signal later when it is applied. With both V1 and V2 screens connected in parallel the same screen voltage is applied to both tubes. Although quiescent plate current flow through R6 produces a voltage drop which reduces the supply voltage to that desired for the plate operating value, it is a steady dc and no output appears from C5. From the discussion and an examination of the schematic, it is evident that V2 also operates as a conventional resistance coupled stage similar to V1 except for the source of input voltage. With R7 and R9 connected as a voltage divider in series with R8 across the output of V1 and V2, when a voltage appears across R8 an input is applied to V2 grid. Since the outputs of V1 and V2 drive a push-pull stage they are opposite in polarity and equal, and the effective voltage across R8 is zero. However, the bias network is designed so that the output of V1 is always slightly greater than that of V2, the difference voltage then appears across R8 and is the driving voltage for V2.

With the basic conditions now established, assume that a sine-wave input signal is applied to the grid of V1. During the positive half-cycle of the input signal, the grid of V1 causes an increased plate current flow, and produces a negative-going voltage drop across plate resistor R5, which is applied through C4 to output voltage divider R7 and R8. The portion of negative output voltage appearing across R8 is applied to V2 grid, produces a reduction in plate current, and the plate voltage of V2 rises towards the supply value. Thus, positive-going output is applied across C5 to output voltage divider R9 and R8. The output voltage from V2 appearing across R8 opposes the output developed by VI across R8, and all but a small fraction of this voltage is cancelled out. This small difference voltage is the actual drive voltage applied V2 grid.

When the input signal on V1 reaches its positive peak and reverses, it becomes negative-going. This negative grid voltage on V1 causes a reduction in the plate current of VI, and the plate voltage rises towards that of the supply. Thus a **positive-going** output voltage is developed, which is applied through C4 to output voltage divider R7 and R8. The positive

portion of voltage across R8 drives V2 grid in a positive direction, and causes an increased plate current flow through plate resistor R6. The voltage drop across R6 is negative-going and is coupled to output divider R9 and R8 through C5. The negative output voltage from V2 cancels all but a small fraction of the positive voltage across R8. Because the plate output of V2 is also connected back to the grid by voltage divider R9 and R8, a feedback loop exists. Since the output of V2 is always out-of-phase with the grid of V2 the feedback is essentially negative. Thus V2 is stabilized and improved response and linearity are obtained. At the same time, this feedback ensures that the output of V2 is always slightly less than that of V1. Since negative feedback is provided from plate to grid, the cathode of V2 is bypassed by C2 so that full amplification without further degeneration may be obtained.

When the input signal reaches its negative peak and reverses, once again it is positive-going and the initial action discussed above for V1 is repeated. Thus alternate positive and negative half-cycles of input signal produce equal and balanced out-of-phase outputs. The VI output is always out-of-phase with the input, while the output of V2 is always in-phase with the input.

## Failure Analysis.

No Output. An open input or output circuit, lack of supply voltage, input signal, or a defective tube will cause a no-output condition. Check the cathode bias, and plate and screen voltages with a high resistance voltmeter. If the voltages are normal but no output exists, check the input with an oscilloscope. If the signal appears at the input but not on VI grid, coupling capacitor Cl is open or RI is shorted. Check the resistance from grid to ground to determine if the input is shorted. If the signal appears on the grid but not on the plate, make certain that proper screen voltage exists. If C3 is shorted the entire screen voltage will be dropped across R4 and no output will appear, likewise, if R4 is open no screen voltage will be applied either VI or V2. Loss of screen voltage will be detected during the other voltage tests since both plate and bias voltages will be higher and lower than normal, respectively. With normal plate and screen voltage applied, if still no signal appears on the plate, either the tube is defective or plate resistor R5 is shorted.

If a signal appears on the plate but does not appear at the output, either coupling capacitor C4 is open or R7 and R8 are shorted. Check the capacitor with an in-circuit capacitance checker and the output voltage divider resistors with an ohmmeter.

If an output appears from V1 but not from V2, check with the oscilloscope for a signal on V2 grid. If no signal appears, R8 is either open or shorted. If a signal appears on the grid of V2 but not on the plate, V2 must be at fault. Previous voltage checks were made for bias, screen, and plate voltage so that C2, R3 and R6 cannot be at fault.

Check V2; if no output can be obtained either C5 is open or R9 is shorted. Check the capacitance of C5 with an in-circuit capacitance checker, and measure - the resistance of R9. Also measure the resistance from C5 to ground to determine that a short does not exist across the output. Such a condition could be caused by a shorted grid-to-cathode element in the following push-pull stage.

Low or Unbalanced Output. Improper bias, low plate or screen voltage, as well as a defective tube can cause a reduced output. If return resistor RI is open or becomes high in value with age, the grid of V1 will tend to develop a negative bias and block causing reduced output from both tubes. Check the value of R1 with an ohmmeter. If R4 changes to a higher value, the screen voltage and output will be reduced. Check the screen voltage with a voltmeter and the resistance of R4 with an ohmmeter. If C3 is partially shorted or leaky, the excess current drain through R4 will also lower the screen voltage. If the screen voltage rises when C3 is disconnected from ground, replace the capacitor. If the emission of either tube is low, the voltages may show normal, and signals appear on grids and plate, but a reduced output occur because of the inability of the tube plate current to follow the signal completely.

If bypass capacitor C2 becomes shorted, the cathode resistor of V2 will be effectively removed from the circuit, and the tube will operate at zero bias. Such operation will cause an unbalanced output with distortion. Checking the resistance of R3 to ground with an ohmmeter will determine if C3 is shorted. If bias resistors R2 or R3 change in value the balance will also be upset, depending upon the amount of change. An ohmmeter check of the resistors will determine whether they are at fault. If either plate resistor R5 or R6 increase in value the output will be above normal, but if they decrease in value the output will be below normal. While the supply voltage drop may be different for each of these cases, the

current will also change and may make the plate voltage reading fall within tolerance values. Therefore, a resistance check of the plate resistors will quickly show if they have changed in value. Changes in voltage divider resistors R7, R8, and R9 will change the gain, drive, and output. Tube VI output is affected mostly by R9. Defective tubes in the push-pull circuit following this stage can cause a heavy load with a consequently reduced output.

Distorted Output. Improper bias, screen or plate voltage, as well as a defective tube or overdrive can

cause distortion. Check the bias, plate, and screen voltages with a voltmeter. If all voltages are normal but the output is distorted and low the tubes are probably defective, replace them with known good ones. If the distortion reduces when the input signal is reduced, it is the result of too high a drive for the bias used. Poor balance will also cause distortion. Use an oscilloscope and follow the signal from grid to plate through the circuit, and compare outputs. When the distortion appears the cause will be found in the parts associated with that portion of the circuit.

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# PART 5-4. CATHODE FOLLOWERS

# BASIC CATHODE FOLLOWERS (ELECTRON TUBE)

# Application.

The cathode follower is used for two purposes: To isolate the output of a critical circuit from the loading effects of a circuit to which the output is fed; and to match the output impedance of a signal source to the input impedance of a load circuit. Both purposes are accomplished with an absolute minimum of distortion of the input signal.

# Characteristics.

Utilizes a single-stage degenerative amplifier, to furnish an output which appears across an **unby** passed cathode resistor.

Input impedance is high; no grid current flows.

Output impedance is low; output signal is in phase with input signal.

Output voltage gain is less than unity; output exhibits a power gain.

Operated Class A to obtain, in the output signal, a faithful reproduction of the input signal.

# Circuit Analysis.

General. In the basic circuit shown in the accompanying illustration, a triode tube is used, but a pentode tube may be employed in a similar manner. In the basic circuit the cathode bypass capacitor is absent, and the plate is tied directly to the supply voltage,  $+E_{hh}$ . The input signal is applied through coupling capacitor Cl to the grid of the tube, V1, and the grid is returned to ground through a relatively high value grid resistor, RI. The output is taken across the cathode resistor, R2, and since this resistor is unbypassed, the output signal voltage is a direct function of the plate current which flows through this resistor. As the input signal rises, or goes in a positive direction, the plate current increases, causing an increased voltage drop across the cathode resistor. As the input signal falls, or goes in a negative direction, the plate current decreases, causing a decrease in voltage drop across the cathode resistor. Thus the output signal *follows* the input signal, both in value and in polarity, although the actual (voltage) value of the output signal is somewhat less than that of the input signal.



**Basic Cathode Follower Circuit** 

**Circuit Operation.** In the basic cathode follower circuit, under conditions of no signal input to the grid, a certain amount of plate current flows through the tube because of the positive potential applied to the plate from the plate supply  $(E_{bb})$ . This plate current flows through the cathode resistor, R2, and the resultant voltage drop across R2 establishes the no-signal bias level, with the grid effectively at zero (ground) potential, and the cathode at some positive (above ground) potential.

When a positive signal is applied to the grid, the resulting increase in plate current through cathode resistor R2 increases the voltage drop across R2, making the cathode "more positive. In like manner, a negative signal applied to the grid causes the plate current flowing through cathode resistor R2 to decrease, making the cathode less positive. Thus the signal variation on the grid produces a variation in plate current through the cathode resistor, and the resulting variation in voltage drop across the resistor develops the bias voltage. This bias voltage, being in phase with the input signal, subtracts from the input signal during the positive half cycle, and adds to the input signal during the negative half cycle. The resulting change in bias in both cases reduces the amplitude of the grid-to-cathode voltage, producing degeneration of the output voltage. For this reason, the voltage gain of a cathode follower is always less than one.

Cathode followers are normally operated with the grid negative with respect to the cathode under conditions of no input signal. The input impedance is high, and remains high when an input signal is applied. When a positive signal is applied to the grid, the degenerative action increases the grid bias to such an extent that no grid current will flow. This is the same result that would be obtained if the input impedance had been increased. When a negative signal is applied to the grid, no grid current can flow, even though the grid bias is decreased through the degenerative action. Thus the input impedance remains high. As a result of this high constant input impedance, the cathode follower presents a negligible loading effect to the circuit driving it.

The effective input capacitance of a cathode follower is low, compared to that of a conventional amplifier. This results from the fact that the degenerative action reduces the amplitude of the ac component of the grid-to-cathode voltage, and thus causes less current to flow through the tube capacitances.

The output impedance of a cathode follower is **10W**; because of this fact there is a minimum of amplitude distortion of the output signal, under normal operating conditions, even though current is drawn from the output terminals. However, if the amplitude of the input signal is high enough to swing the voltage at the grid too far positive or negative, the tube may be driven to saturation or to cutoff, respectively. When either of these points is reached, limiting action occurs, and any further change in the input signal will not appear in the output waveform. The output signal will thereby be distorted with respect to the input.

Occasionally, a cathode follower circuit may be encountered which is actually designed to operate partially in the region of cutoff. In radar circuitry, video and transmitter trigger pulses, which may be positive pulses, might be applied to a cathode follower which is biased near cutoff. As a result, the cathode follower will pass the signal in normal cathode follower fashion; at the same time it will clip any negative transients which may be present in the input signal, and, in addition, it will eliminate the possibility of any dc loading effects by allowing only the signal voltages to be present across the output cathode resistor. Although this of circuit may be termed a *cathode* follower circuit (because the output is taken from across the cathode resistor), it does not satisfy that definition of a cathode follower where the output signal shall follow the input signal without change in waveform. In this respect such a circuit,

sometimes referred to as a *cutoff cathode follower*, should more properly be termed a *limiter-follower*.

If limiting occurs only on the negative peaks of the input signal, i.e., if the input signal drives the tube to cutoff but not to saturation, the circuitry of the cathode follower may be modified as shown in the accompanying illustration.



Modified Cathode Follower Circuit to prevent Negative Peak Limiting

In this modified cathode follower circuit, the grid resistor, R1, is returned to a positive (above ground) potential at the junction of a two-section cathode resistor composed of resistors R2 and R3. The value of the positive potential (the relative values of R2 and R3) is determined by the anticipated input voltage level. By returning the grid resistor to a tap on the cathode resistor in this manner, the grid bias is reduced by the amount of the voltage drop across resistor R3. Therefore, the input signal can swing to a greater negative value without driving the tube to cutoff, than it could had the grid resistor been returned to ground potential. In addition, the input impedance of the circuit is increased to a very high value.

A further modification of this circuit is frequently used as a wide-band cathode follower. This circuit, shown in the following illustration, contains an input coupling capacitor, Cl, and a resistor, R4, of small value in the plate circuit for decoupling purposes. Wide-band cathode followers find extensive use when

application requirements demand power amplification over an extreme range of audio frequencies, from 70 to 20,000 Hz, such as in high-fidelity audio circuits. In the circuit shown below, these requirements may be met by the use of a single triode section of a type 12AT7 twin-triode, with values of Cl = 0.01  $\mu$ f, RI = 1 megohm, R2 = 180 ohms, R3 = 820 ohms, and R4 <sup>=</sup>47 ohms. Other values would of course be required with other tube types.

The voltage gain (, V. G.) of a cathode follower, when a triode-type tube is used, is given by the following equation:

V. G. = 
$$\frac{\mu R_k}{r_x + (\mu + 1) R_k}$$

When a pentode-type tube is used,  $\mu$  is large and the term  $\mu + 1$  may be reduced to  $\mu$ . The equation for voltage gain @. G.) may then be reduced to:

$$V. G. = \frac{R_k}{\frac{1}{g_m} + R_k}$$

The output impedance  $(Z_{out})$  of a cathode follower is given by the following equation:



Other modifications of the basic cathode follower circuit are often encountered in radar and communications circuitry. These modifications are included in the following illustrations, which show five circuit variations of cathode followers. In part A. a fixed negative bias is applied, from a power supply, to the grid of a triode at a tap on the grid resistor which is composed of R1 and R2. The output is taken across the cathode resistor, R3. The negative bias applied to the grid, together with the bias developed across the cathode resistor, establishes the initial operating point on the grid voltage-plate current  $(\mathbf{E_g} \cdot \mathbf{I_p})$  characteristic curve of the particular triode used. The value of negative bias applied depends upon the value of input signal to be handled. This is particularly true in applications where the input signal consists of a series of positive pulses with the interval between each pulse relatively long as compared with the pulse width. For example, if a positive input pulse having an amplitude of 4 volts with instantaneous peak values of +96 volts and +100 volts is applied to the input capacitor of a cathode follower circuit, the pulse which appears at the input grid of the tube would settle down to an average ac value of O volts, with most of the pulse appearing above this average value. This is shown in the following "input waveform" illustration, with the input signal shown in part A and the signal voltage which appears at the input grid shown in part B. Fixed biasing is necessary in this situation, in order to place the geometric center of the pulse at the center of the tube's  $\mathbf{E_g}$ - $\mathbf{I_p}$  curve, as shown in part C of the illustration. If, for a given tube, the center of the straight-line portion of the  $\mathbf{E}_{o}$ - $\mathbf{I}_{n}$  curve occurs at -5 volts with a given plate voltage, and the input signal is 4 volts peak to peak with the pulse waveform as shown, a total bias of -7 volts on the tube would be necessary in order to displace the average value of the signal so that its geometric center occurs at -5 volts (the center of the  $E_g - I_p$ curve), as shown in part D of the illustration. If the value of the cathode resistor is such that, when the tube is operating with -7 volts bias, it produces a 3-volt drop, then the additional amount of fixed bias required is equal to -4 volts.

Wide-Band Cathode Follower Circuit

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ELECTRONIC CIRCUITS NAVSHIPS 0967-0000120 AMPLIFIERS + E 66 CI C١ CI 9 0 С O INPUT INPUT INPuT OUTPUT R 3 Srz R3 **≷**R4 RŻ R3 OUTPUT OUTPUT O n Ecc Ecc Ecc В С Еы I. R4 CI CI 0-16 R 2 С O INPUT RI INPUT R3 C.3 OUTPUT R 3 C2 OUTPUT R2 0 0 Е Ecc D

Cathode Follower Circuit Variations

In part B, a triode-connected pentode tube is used, with fixed negative bias applied to the grid in a manner similar to circuit A. Since the power-handling capabilities of pentodes are substantially higher than those of conventional triodes, considerable power output may be obtained from such a circuit. Otherwise, operation of this circuit is generally similar to that of circuit A, with the addition of the screen resistor, R4. This resistor serves to decrease the voltage at the screen grid slightly below the plate voltage, in order to keep the screen dissipation within the operating limits of the tube. When certain tubes are used, or when the plate is operated considerably below the maximum rated voltage, this resistor may be omitted. Sines no bypass capacitor is used between screen and ground, the plate and screen currents vary with the input signal, and the tube operates as a triode.



In part C, a twin-triode is used as a cathode follower, with both sections comected directly in parallel. The use of a twin-triode doubles the power output over that of a single tube section, and in addition provides some measure of assurance of continued output, even though reduced in value, in the event of failure of one of the triodes. The operation of this circuit is similar to that of circuit A, with a few exceptions. A fixed negative bias from a power source is applied through resistor R4 to the grids of both triode sections at a tap on the grid resistor

which is composed of RI and R2. Resistor R4 provides isolation between the grid circuit and the bias voltage supply. The acturd bias voltage available at the grid will be somewhat reduced, however, because of the voltage divider effect of R2 and R3. The input signal is applied directly to both grids, which are connected in parallel, although in some cases resistors of low ohmic value, used as parasitic suppressors, are connected between the input and each grid to suppress intermodulation effects between the two tube sections. This effect is a result of slight differences in electrical characteristics, such as cathode emission and transconductance, between the two sections of the tube. The output from the circuit is taken across R3, which is the cathode resistor common to both sections.

In part D, a pentode tube is used. Fixed negative bias is used, as in circuit A. Screen capacitor C2 maintains the dc voltage at the screen relatively constant with variations in input signal. As a result, the power output obtainable across cathode resistor R3 is somewhat greater with this pentode-connected circuit than it is using the triode comection in circuit B.

In part E, a triode-connected tetrode tube is used, although a triode could be connected in an identical manner. In this circuit the grid return is composed of resistors R1 and R2, with R2 providing additional isolation between the input circuit and the tube, and also serving as a grid current limiter. A coupling capacitor, C2, is also employed in the output circuit, to block the dc component when only the ac signal output is desired. Plate supply isolation may be employed, by means of the decoupling filter composed of C3 and R4, which in additon helps to prevent variations in the voltage at the plate and screen during positive peaks of the input signal.

Another variation of the cathode foUower circuit -

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may be encountered in some equipments, where the cathode resistor and output coupling capacitor are physically located in another chassis, and are connected by means of interconnecting cables. In order to protect the tube against a possible voltage break-down between cathode and filament, in the event of an open cathode circuit caused by a disconnected or broken cable, an additional resistor of a substantially higher value of resistance may be employed directly at the cathode connection of the tube. Since this resistor is connected in parallel with the main cathode load resistor, its presence will not affect the output  $\checkmark$  during normal circuit operation.

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#### Failure Analysis.

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**No Output.** If an input signal is being supplied, an open coupling capacitor C 1 in the input circuit or an output coupling capacitor, if used, would interrupt the circuit output, as would also an open cathode resistor R3 or a shorted plate capacitor C3. (Refer to Cathode Follower Circuit Variations, circuit E.) Failure of the plate (and screen) power supply, or an open plate decoupling resistor R4, if used, or a defective tube, would also be responsible for a condition of no output.

**Reduced or Unstable Output.** If a normal input signal is being supplied, a weak or intermittently shorted tube, or leaky input or output coupling capacitors may be the cause of reduced or unstable output. A reduction in the applied plate (and screen) voltage will cause the output to be reduced, while an unstable supply voltage will cause unstable output signal amplitude. A change in grid bias, brought about by a changed value of grid resistors RI and R2, or of cathode resistor R3, will also affect the output signal, and may distort the signrd by biasing the tube nearly to cutoff or to saturation.

# LOW-LEVEL VIDEO CATHODE FOLLOWER (ELECTRON TUBE)

#### Application.

The low-level video cathode follower is used to match the output impedance of a low-level video source, such as a video limiter, to a low-impedance transmission line, without deteriorating the waveform of the video signal.

#### Characteristics.

Positive output signal is in phase with the positive input signal.

Input impedance is high; no grid current flows within the designed operating range.

Output impedance is low; values shown give an actual output impedance of 100 ohms.

Output voltage gain is less than unity; values shown give an actual gain of approximately 0.5.

Class A output gives undistorted reproduction of input signal within designed operating range.

## **Circuit Analysis.**

**General.** In the circuit shown in the accompanying illustration, a type 5670 twin-triode is used, with

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both sections connected in parallel. Actual values of resistance and capacitance used in this circuit are shown in the illustration; these values govern the input and output limits and the operating level discussed under Circuit Operation. An input capacitor is used in the grid circuit, and the plates are tied directly to the plate supply voltage,  $+E_{bb}$ . The grids are returned, through grid resistor R1, to a fixed negative bias, -EC., from a voltage divider composed of R2 and R3, which is fed from a -150V bias supply. The output is taken from the paralleled cathodes across cathode resistor R5. Resistor R4 acts as a parasitic suppressor to prevent intermodulation between the two triode sections, due to slight variations between them.

**Circuit Operation.** This circuit is designed to accept a positive input signal, and reproduce it without distortion in the positive output signal. Under normal operating conditions, the circuit will handle an operating level of 2.2-volt positive input pulses, and produce an output level of approximately 1.0 volt. As a maximum limit, an input signal of 4.2 volts amplitude will produce an output amplitude of 2.0 volts. This output level approaches the grid-current region of the type 5670 tube, and therefore is about the maximum that can be obtained using this tube type. The gain of the circuit is approximately 0.5.



Low-Level Video Cathode Follower Circuit

The input signal is applied through coupling capacitor Cl to the grid of section A of a type 5670 twin-triode, and through suppressor resistor R4 to the

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grid of Section B. A fixed value of grid bias is supplied from a negative 150-volt bias supply, to a voltage-divider circuit composed of 150K resistor R2 and 2 .7K resistor R3. The junction of the two resistors, at which the voltage is approximately -2.6 volts, furnishes the actual bias to which the grid resistor, R1, is returned. The unbypassed cathode resistor, R5, is common to both triode sections, and the voltage drop appearing across it, which is an exact reproduction of the input signal, constitutes the output of the video cathode follower.

A particular form of distortion of the input signal, known as *droop* or sag, is of significance in low-level video cathode followers. Droop is the decay in amplitude, with time, of the flat top portion of a positive square wave input signal. The amount of droop is largely determined by the ratio of the pulse length to the RC time constant of the input coupling circuit. For small values, the percentage of droop is equal to the pulse length **divided** by-the RC **time** constant:

Droop (%) = 
$$\frac{\text{pulse length (seconds)}}{R_{(OHMS)} \times C_{(FARADS)}}$$

For example, for Values of  $Cl = .05\mu f$  and RI = 1 meg, and a pulse length of 500 #see,

Droop % = 
$$\frac{500 \text{ x } 10^{-6}}{(1 \text{ x } 10^{-6}) \text{ x } (.05 \text{ x } 10^{-6})} = .01 = 1\%$$

#### Failure Analysis.

**No output.** Assuming that a signal of the proper positive value is applied at the input to the video cathode follower, the primary cause of no output may be a defective tube. If the tube is found to be operational, an open coupling capacitor, Cl, would interrupt the operation of the circuit. An open resistor R3 in the grid bias voltagedivider circuit would allow the full value of the -150-volt bias voltage to be applied directly to the tube grids, cutting off the tube. Failure of the plate supply voltage would interrupt operation of the circuit, as would also an open-circuited cathode resistor, R5, provided that there is no continuous dc path paralleling R5 in the output circuit.

**Reduced or Unstable Output.** With a proper positive input signal present at the input to the video

cathode follower, a leaky (partially shorted) grid coupling capacitor, Cl, may be responsible for a severely distorted output. This leaky condition. acting as a partial short, would allow any value of dc voltage which is present at the input to be applied to the grid of the tube. This voltage would appear to the tube as a change in grid bias, and shift the operating point on the tube's  $E_g \cdot I_p$  characteristic curve into either the cutoff or saturation region. An open grid resistor, RI, may cause the tube to "block", or to "motorboat", or to exhibit no effect other than a distortion of the output waveform. With an open grid resistor the tube may "block" because the grid coupling capacitor, Cl, has no readily available discharge path, and may gradually accumulate a negative charge, sufficient to cut off the tube, through grid current on the positive peaks of the input signal. Intermittent conduction of the tube, or "motorboating", may result if leakage through Cl allows Cl to discharge down to the point where the tube is momentarily "unblocked". In some cases of an open grid resistor no immediately discernible symptoms will be evidenced other than a distortion of the output waveform. This may be caused by the grid "floating" at some intermediate value and the input signal continuing to be coupled through by the capacitive voltage divider action of coupling capacitor Cl and the grid to cathode capacitance of the tube. Since the interlectrode capacitance of the tube is very small as compared with the capacitance of Cl, most of the input signal will continue to appear across the grid and cathode, and the tube will react in very nearly a normal manner. Should resistor R2 in the voltage divider network be come open-circuited, the fixed negative bias from the -150V power supply would not be applied to the grid. As a result, the input signal may be sufficient to drive the tube to saturation, seriously distorting the output on the positive peaks of the signal. If, on the other hand, resistor R3 became open-circuited, the full value of -150 volts from the bias power supply would be applied to the grid, and the tube would be driven far beyond cutoff. Reduced output may also be traced to an open parasitic suppressor resistor, R4, which would cause one triode section to the tube to be without an applied input signal, reducing the output to half the initial value, with a possibility of distortion on the most positive portion of the input signal due to reduced bias. The reduction in bias would be the result of the "blocked" grid, causing a reduction in current flow

**through** the common cathode resistor, and hence a lower value of voltage drop across the common cathode resistor. If the cathode resistor should change in value, because of age or overload, the output voltage would be changed accordingly.

# PULSE CATHODE FOLLOWER (ELECTRON TUBE)

# Application.

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The pulse cathode follower is used as an isolation stage between a critical circuit and the circuit which it feeds as a load, while at the same time preventing any loading effects from appearing at the output of the critical circuit. This is accomplished by means of the cathode follower's characteristic of a high input impedance and a low output impedance.

#### Characteristics.

Output signal is in phase with input signal.

Input impedance is high: no loading effects are reflected at the output of the previous stage.

Output impedance is low: considerable power may be supplied to the output load circuit.

Output voltage regulation is good, due to low output **impedance**, even through the input signal may have poor voltage regulation due to its high impedance.

Input capacitance is low: approximately 2.5 pf excluding capacitance of circuit wiring.

Rise time response is fast: approximately  $0.02 \mu$ sec.

## **Circuit Analysis.**

**General.** In the circuit shown in the accompanying illustration, a single triode section of a typical twintriode such as a type 5814A, is used. Actual values of resistance and capacitance used in the circuit are determined by the operating characteristics desired, and are therefore not given in the diagram. Typical values used to produce specific operating characteristics, and a discussion of the effects produced, are given under Circuit Operation. An input capacitor, Cl, is used in the grid circuit, and the grid is returned to ground through grid resistor R1. Plate voltage is supplied directly from the supply voltage,  $E_{bb}$ , and the output is taken across the unbypassed cathode resistor, R2.

**Circuit Operation.** The pulse cathode follower using an input capacitor (C 1) of 0.047  $\mu$ f and a grid resistor (Rl) of 680K, with a type 5814A tube (one triode section), has a very low input capacitance of approximately 2.5 pf, and a fast rise time response of 0.02  $\mu$ sec. The rise time is in large part dependent upon the transconductance of the tube and its associated interelectrode capacitances. A typical rise time of 0.02  $\mu$ sec or 0.03  $\mu$ sec is satisfactory for most radar and other pulse timing applications.



Pulse Cathode Follower Circuit

The transition time of the negative-going edges of pulses, such as the fall time of a positive pulse or the rise time of a negative pulse, is increased by a cathode follower. This transition time depends upon pulse amplitude, while the positive-going edges of pulses are unappreciable affected by pulse amplitude. This is due to the fact that the tube transconductance is of a different value during the fall of the pulse than during the rise of the pulse. The tube is nearer cutoff during the fall of the pulse; transconductance is at a low value and the combination of pulse amplitude, capacitance, and the value of cathode resistor all combine to determine the fall time. The negative transition time may be improved by the use of a negative voltage connected to the cathode resistor, from a negative power supply. If this is done, the tube will draw a higher value of plate current in its quiescent state, compared to a similar tube having its cathode resistor returned to ground. As an alternative, the returned end of the grid resistor may be

connected to a tap on the cathode resistor. Since a higher value of plate current is now drawn by the tube when quiescent, its operating point is appreciably removed from cutoff. The tube's transconductance is hence at a higher value, and the fall time, or negative transition time, is thereby decreased.

Additional capacitance in the output circuit has an effect on the negative transition time, as shown in the following illustration. It can be seen that the capacitance in the output circuit should be kept to a minimum where small values of negative transition time are required.



Effect of Additional Output Circuit Capacitance on Negative Transition Time

The over-all effect of a cathode follower on the transition time of positive and negative pulses, and a visual definition of transition time as applied thereto, may be better understood by referring to the following waveform illustrations.



# Effect on Negative-Going Edges of Pulses Due to Cathode Follower

Typical values of gain, input and output limits, output impedance, rise and fall times, for a single triode section of type 5814A twin-triode operated with plate voltages of +150 and +300 volts and cathode resistance of 10K and 22K, are given below.

Rk (ohms)	10K	10K	22K (–150V)
Ebb (volts)	150	300	300
Voltage gain	0.87	0.87	0.9
Input limit			
(volts)	0 to 70	0 to 170	-100 to +180
Output limit			
(volts)	0 to 61	0 to 148	-90 to +162
Output imped-			
ance (ohms)			
for 20-volt in-			
put. pulse	300	420	300
Rise time (µsec)	0.02	0.02	0.02
Fall time (#see)			
for 20-volt in-			
put pulse with			
added 15 pf	0.2	0.15	0.05

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The preceding output impedances were measured with a load of such values as to reduce the output voltage to one-half the value of the no-load voltage. The effective output impedance for large values of signal depends upon pulse polarity. As shown above, when a cathode resistance of 22K returned to -150 volts is used, the output impedance is 300 ohms for a positive pulse. For a negative input pulse, however, the output impedance is approximately 1400 ohms. Note the marked improvement in fall time and the increased signal handling capacity gained by returning the cathode-resistor to a negative supply.

# Failure Analysis.

No Output. The input circuit should be checked to insure that an input signal is being applied to the pulse cathode follower. The tube should also be checked to insure that it can function properly under normal conditions. If the input signal is present and the tube is good, an open coupling capacitor, Cl, would prevent the signrd from reaching the tube. If this capacitor were shorted, any value of dc voltage that may be present at the input terminals, from the previous stage, would be applied to the grid of the tube, and would seriously affect its biasing level. Insufficient or no voltage at the plate of the tube, due to failure of the power supply, would obviously result in no output. Another cause may be an open-circuited cathode resistor, R2, assuming that the output circuit has no continuous dc path which could act as a cathode resistor by paralleling R2.

Reduced or Unstable Output. If it has been ascertained that a normal input signal is present at the input to the pulse cathode follower, several conditions could contribute to a faulty output. A leaky coupling capacitor, Cl, would effectively lower the input impedance by providing a path of lower resistance in the grid circuit, thus changing the operating characteristics of the tube. Any dc voltage present at the input would appear at the grid, thereby changing the bias. If this voltage is positive and of a sufficient value, the tube may be driven to saturation, resulting in severe distortion of the output signal. An open grid resistor, RI, may cause the tube to "block", or to "motorboat", or to exhibit no effect other than a distortion of the output waveform. (For a more detailed discussion, refer to the Failure Analysis of the Low Level Video Cathode Follower, discussed previously in this section. A change in vrdue of cathode resistor R2, due to aging and/or excessive current, may be the cause of reduced output. A reduced value of plate voltage, due to partial failure of the power supply or to excessive loading of the supply by some other defective circuit, may also be responsible for a reduced value of output from the pulse cathode follower.

#### PART 5-5. VIDEO

#### VIDEO AMPLIFIERS

General. The frequency range covered by the video amplifier is greatly extended over that of the audio amplifier. Video frequencies extend from dc, or a few Hz, to as high as 5 or 6 MHz, depending upon the type of signals. For example, in television applications the picture information requires a uniform bandwidth of from 60 Hz to 4 MHz, whereas in radar applications a band width of from about 30 Hz to 2 MHz is sufficient. In circuits where sawtooths or pulsed waveforms are to be amplified, it is necessary to cover a range of frequencies from about one tenth that of the lowest frequency employed to at least ten times that of the highest frequency. This extended range is necessary because waveshapes which are not sinusoidal contain many harmonics, which must be amplified equally and without any phase delay in order to avoid distortion. The sinusoidal waveform requires only sufficient uniformity of response to pass its second and third harmonics, because any other higher harmonics are of such small amplitude that they can be considered negligible as far as their effect on the shape of the waveform is concerned; on the other hand, the square wave, **pai** ticularly at the lower frequencies, requires that an infinite number of harmonics be passed for accurate reproduction of the waveshape. In practice, however, it has been found that for square waves, harmonics above the tenth, like those greater than the third for the sinusoidal signal, are actually of negligible amplitude and have little effect on the shape the final waveform.

Since the video amplifier requires the best possible uniformity of response R-C coupling is used rather than transformer coupling (which has a narrow bandwidth), and cascaded stages are used to supply sufficient gain. This requires that the interstage coupling circuits be modified to obtain the required bandpass, and that inverse feedback be used where possible to flatten out the response. Low-frequency response is improved by using large values of coupling capaci-

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tance to lower the series reactance and reduce the voltage drop across the coupling capacitor. The values of the coupling capacitor used between transistor circuits are much higher than the values used between electron-tube circuits (on the order of 10 µf). Even so, further compensation is required through partial bypassing of the collector load resistance to improve the low-frequency response and to prevent phase distortion at frequencies lower than 30 Hz. Because the gain is highest at the lower frequencies, it is general practice to reduce the low-frequency gain and boost the high-frequency gain, to obtain uniform response for both low and high frequencies. The high-frequency response is increased by using compensating circuits with inductance in the load circuit. The higher load reactance at the higher video frequencies causes a larger output voltage to be developed (when the output would normally be dropping), and thus extends the frequency response. The series inductance in the load circuit also resonates with the stray (shunt) circuit and transistor capacitance, to produce a high-impedance parallel-resonant circuit which is effective over a large range of frequencies; this is known as shunt peaking. Further extension of the response at the highest video frequencies employed is obtained by the use of an additional inductor in series with the coupling capacitor. The series inductor and coupling capacitor form a series-resonant circuit at the very high video frequencies, to boost the response at the upper limits of amplification; this is known as sen"es ptnkr"ng. In the transistor video amplifier, the use of combined shunt- and series-peaking circuits provides the maximum extension of high-frequency response.

In the electron-tube video amplifier, further increase in high-frequency response is obtained by using a lower load resistance than normal and by sacrificing some additional gain. Such compensation is not possible with the transistor video amplifier, however, since maximum gain occurs up to f<sub>max</sub>, which is the upper limit of usable transistor gain. Above f<sub>mu</sub> the transistor gain drops off to practically nothing, and the transistor no longer amplifies. In the electron tube, however, the gain does not drop off until far past the highest video frequency (actually in the high r-f ranges), so that heavy loading can improve the response. Since the common-emitter circuit produces high gain, cascaded transistor stages can be mismatched so that the low-frequency gain is reduced to equal the high-frequency gain, and still provide uniform response with adequate over-all gain. Matching to obtain more gain is usually required only at the transistor cutoff frequency  $(f_{max})$ , since excess gain exists at the lower frequencies. Because of the extended frequency range, and since the low-frequency gain and forward amplification vary from transistor to transistor, considerable care is necessary in design to avoid regeneration and circuit instability. Partird bypassing of the emitter resistor is generally used to provide some degeneration and thus stabilize the circuit. Where a number of stages are used, an external negative feedback loop is uaually provided to improve the stability and response. However, since the use of external negative feedback is not peculiar to video amplifiers alone (it may be employed in many other circuits), it will not be further discussed in this section.

# TRIODE VIDEO AMPLIFIER (ELECTRON TUBE)

## Application.

The video amplifier finds extensive use in television circuits, where actual "picture video" signals are amplified; in radar circuits, where wide ranges in frequency must be handled; and in communications where a number of voice-frequency channels are successively "stacked" in frequency, one above the other, to occupy a complete 6-MHz channel.

## Characteristics.

Class A operation is utilized to insure an output which is a faithful reproduction of the input signal.

Polarity of output signal is inverted over that of input signrd.

Frequency response is broader than that of a standard R-C coupled amplifier.

Input signal may consist of pulses of either positive or negative polarity, or both.

## Circuit Analysis.

**General.** At low frequencies, the gain of an ordinary R-C coupled amplifier decreases rapidly as the frequency decreases, because of the corresponding increase in reactance of the input coupling capacitor with decrease in frequency. The increased reactance causes a greater proportion of the input signal voltage to drop across the capacitor, leaving a smaller proportion of the input signal to appear at the input to the tube, across the grid resistor. In addition, bypassing of the cathode resistor becomes less effective for the same reason, resulting in degenerative effects and

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further reducing the gain. This loss of gain at low frequencies may be partially overcome by the use of a larger value of coupling capacitance. If, however, too large a value of coupling capacitance is used, the high-frequency response may be adversely affected.

At high frequencies, the gain of an ordinary R-C coupled amplifier also decreases with an increase in frequency. This is due to the capacitive effects of the wiring, the tube and socket, and interelectrode capacitance itself, all of which effectively add capacitance across the plate load, from the plate of the tube directly to ground. This stray capacitance,  $C_d$ , acts as a bypass capacitor in the plate circuit in parallel with the output voltage, bypassing the higher frequencies. As the frequency is further increased the gain continues to fall, eventually reaching a point where the amplifier circuit no longer amplifies.

In order to counteract this action and extend the amplification range in the direction of increasing frequency, the plate load resistance must be decreased. As an approximation, the response may be extended from a given limiting value, such as 10 kHz, to a value ten times as great (1 MHz) by decreasing the value of the plate load resistor in the same proportion, such as from 220K to 22K. However, by so doing, the overall gain of the amplifier, including the middle and lower frequency gain, is considerably reduced. This loss must either be tolerated, if the extended frequency response is required or overcome by using additional stages of amplification.

Circuit Operation. The accompanying schematic illustrates a triode video amplifier circuit. The input signal, composed of video pulses of either positive or negative polarity, is applied to the grid of the triode amplifier through coupling capacitor Cl. The grid is returned to ground through grid resistor R1. The combination CIR1 forms an R-C circuit at the input to the tube, and the time constant of this circuit limits the low-frequency response of the amplifier. The time constant must be long, in comparison to the period of the lowest frequency to be amplified. At the middle and high frequencies, the value of Cl is sufficiently large that its reactance is negligible, and the full input voltage appears across grid resistor RI and is thereby applied to the grid of the tube. But, as the frequency decreases, the reactance of Cl increases according to the formula:

$$\mathbf{X}_{\mathbf{c}} \cong \frac{1}{2\pi \mathbf{f} \mathbf{C}}$$

As a result, the effect of Cl is no longer negligible; its reactance and the resistance of R1 form a voltage divider across which the input voltage is applied. The voltage drop across Cl is lost, for all practical purposes, and only that value which appears across RI is effective at the grid of the tube. The voltage drop across Cl may be reduced by increasing the capacitance of Cl, which will decrease its reactance, but the extent to which Cl can be increased is limited because an increase in physical size results in an increase in stray capacitance. The stray capacitance, in turn, acts in the same manner as a bypass capacitor in the plate circuit, to decrease the gain at the high frequencies.



**Triode Video Amplifier Circuit** 

The grid bias, in the triode video amplifier circuit, is obtained by utilizing the voltage drop across resistor R2, connected in series with the cathode of the tube. The total electron current flowing through the tube passes through this resistor. Since the tube current vanes with the variations of the applied signal voltage, a corresponding varying voltage is developed across cathode resistor R2. In order to obtain a steady value of grid bias voltage, these signal variations must be bypassed around the bias resistor by means of a filter capacitor, which is the cathode bypass capacitor C2. The reactance of this capacitor must be low, in order to provide a low-impedance path around the resistor for the alternating current components of the signal. This capacitor must have a value of 5 microfarads or greater for audio-frequency amplifiers. For video-frequency amplifiers, which may be required to pass frequencies much lower in

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value, the capacitance of the cathode capacitor C2 must, in many cases, be much greater, such as 100 microfarads or more. As a general rule, the time constant of R2 and C2 must be long in comparison to the period of the lowest frequency to be passed by the video amplifier. In order to provide effective by-passing for the ac components of the signal around the cathode resistor, the value of capacitive reactance at the lowest frequency to be amplified is generally accepted to be one-tenth (or less) the resistance value of R2.

The value of plate load resistor R3 has a controlling effect, not only on the gain of the amplifier, but on its frequency response as well. The gain increases with higher values of plate load resistance, but the bandpass of the circuit becomes less. Conversely, lower values of plate load resistance will decrease the gain of the amplifier, but will extend its frequency response. This is illustrated in the following diagram.



Effect of Value of R1 on Video Amplifier Bandpass

The value of the plate load resistor may be decreased down to approximately 1.5K in some applications. Further extensions of the frequency range require the use of high-frequency and low-frequency compensating networks.

Stray (or distributed) capacitance, due to the capacitance of the circuit wiring and the interelectrode capacitance of the tube, is a cause of poor high-frequency response, and, therefore, distortion. The distortion of the output waveform, as a result of poor high-frequency response, is shown in part C of the following illustration, while the input waveform and the ideal output waveform are shown in parts A and B, respectively. If the parallel combination of the plate resistor, R3, and grid resistor  $\mathbf{R}_{\mathbf{g}}$  of the following Stage allows the stray capacitance,  $C_{\mathbf{d}}$ , to

charge and discharge quickly, the output will show little or no distortion. If, however, R3 and  $R_g$  are large values of resistance,  $C_d$  will require a relatively long time to charge or discharge, and the steep sides of an applied square wave will be distorted, as shown in part C of the illustration.





This condition may be overcome in one of two ways. The first is to reduce the size of  $C_d$  by using special amplifier tubes with low values of input and output capacitance between the lead wires and ground. The second is to decrease the time required by  $C_d$  to charge or discharge. This can be accomplished by reducing the value of R3 or  $R_g$ . If  $R_g$  is reduced, however, the low-frequency response will suffer. If R3 is reduced, the gain of the stage will be reduced in turn, but this may be overcome by using additional stages of amplification.

The decreased response at high frequencies is caused principally by the shunting effect of the distributed capacitance of the circuit and the interelectode capacitance of the tube, which together act to reduce the impedance of the plate load. This effect may be compensated for, and the high-frequency range may be extended, by the addition of a small

**value** of inductance, Ll, in series with plate resistor R3, as shown in part A of the following illustration. This inductance sewes to boost the response of the high frequencies, while having practically no effect upon the lower frequencies. The boost in response at high frequencies is due to the high inductive reactance of the inductance, Ll, which produces a back EMF, resulting in a sharp peak at high frequencies, as shown in D and E of the illustration. This sharp peak, or introduced distortion, 'will counteract that caused by the stray capacitance, and the resultant output will be almost a pure square wave as shown in F. **At** low frequencies, the inductive reactance of the inductance is low, and has negligible effect on the circuit. This method, known as shunt compensation, is

effective when the maximum-frequency limit is not too high, and there are only a few stages of **amplifica**tion.

Another method of compensating for this effect, known as series compensation, is shown in part B of the following illustration. In this method, a small value of inductance, L2, is connected in series between the plate and the output to the following stage. This small inductance resonates with the input capacitance of the following stage at high frequencies, and acts to cancel the shunting effect of the input capacitance by the increased impedance of the series resonant circuit. This results in an increased voltage at the input to the following stage, and, therefore, an increase in gain.



Triode Video Amplifier Frequency Compensation Circuite

The advantages of both of the above methods may be combined in a single circuit. This circuit, known as series-shunt compensation, is shown in part C above. This combined method utilizes both the inductance L1 in series with plate resistor R3 and the inductance L2 in series with the plate and the output. The combination gives the high-frequency peaking effect of the shunt-compensation circuit along with the increase in gain at high frequencies due to the resonant effect of the series-compensation circuit.

The decreased response at low frequencies is caused principally by the increased reactance of the input coupling capacitor, which reaches an appreciable **value as** the frequency decreases below 200 Hz. This decreased response, or loss of gain, can be counteracted by the addition of a low-frequency compensation network, or falter, in series with the load resistor. This compensation network consists of a capacitor, C3, and a resistor, R4, connected into a filter circuit as shown in the following schematic. The filter, connected in series with plate load resistor R3, accomplishes two purposes:

(1) It introduces a phase shift into the plate circuit which compensates for the phase shift in the output coupling circuit. (2) It increases the effective plate

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load impedance at low frequencies, and thereby maintains the low-frequency gain. This is explained as follows: At low frequencies R4 plus R3 make up the plate load of the circuit. The addition of R4 will increase the gain of the circuit, and the low-frequency response. The capacitive reactance of C3 will be high, thereby preventing any shunting effect. At high frequencies the reactance of C3 is lower, causing the signal to be shunted around R4, effectively removing R4 from the circuit. In this manner the plate load becomes lower at high frequencies, and the highfrequency response will not suffer.

Frequency response is an important consideration in video amplifiers, but it is not the only one. Phase distortion, which can be tolerated in an audio amplifier, is capable of destroying the image on a cathoderay-tube screen. Phase distortion is produced when the time or angular relationship of electric waves to each other changes as they pass through any electrical system. As an example, consider the wave shown in part B of the following figure.



Low-Frequency Compensation Circuit



Composite Waveforms of Fundamental Plus Third Harmonic

This wave is actually composed of a fundamental frequency in combination with its third harmonic, as shown in part A of the illustration. If the effect of the circuit on each of these two waves is different, the two waves may appear as in part C of the illustration, where the third harmonic has changed its position with respect to the fundamental. That is, its phase relationship has changed. The resultant of these two waves will now assume the shape given in part D of the illustration, which is certainly different from the original waveform shown in part B.

At low frequencies, the phase of the voltage at the grid of the amplifier is governed by the amount of opposition offered by the coupling capacitor to the ac waveform passing through the circuit. The coupling capacitor and grid resistor are, in effect, a series circuit. As the applied signal becomes lower and

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lower in frequency, the ever-increasing capacitive reactance causes the circuit current to lead the applied (signal) voltage in ever-increasing amounts approaching 90 degrees. The voltage drop across the grid resistor is in phase with the current through it, and would also lead the applied voltage by the same amount. In the middle range of frequencies, from 200 to 2000 Hz, the capacitive reactance of the coupling capacitor becomes small enough with respect to the reactance (resistance) of the grid resistor to have a minimal effect on the passing waveform; therefore, phase shift can be considered negligible in the middle-frequency range. At the high-frequency end of the band, the input capacitance between the grid and the cathode becomes important and must be considered. The input capacitance and the grid resistor form, in effect, a parallel circuit. As the capacitive reactance of the input capacitance becomes less and less with increasing frequency, the current in the parallel combination will become more and more capacitive and will begin to lead the applied voltage by everincreasing amounts approaching 90 degrees. Another way of expressing this thought is that the voltage across the parallel combination will begin to lag by ever-increasing amounts as the applied frequency is increased. The shift in phase angle at the grid of the tube is **opposite** to that caused at the low frequencies, but in either case the result is the same: phase distortion. An illustration of the relationship between phase distortion and frequency response in an ordinary amplifier is given in the following figure.

The high-frequency and low-frequency compensating networks previously described, in addition to compensating for frequency response, help to correct for phase distortion, as they shift the phase back in an opposite direction to make the circuit appear resistive over a wider frequency range.



Phase **Distortion** and Frequency Response Characteristics of an Ordinary Amplifiar Stage Failure Analysis.

No Output. With a video signal of sufficient amplitude applied at the input to the video amplifier, a defective tube is the primary cause of no output in the majority of cases. If the tube is found to be operational, an open coupling capacitor Cl would prevent an input signal from reaching the video amplifier grid. An open cathode resistor R2 would interrupt the operation of the circuit, resulting in no output. If a compensation circuit is employed in the plate circuit, a shorted capacitor C3 would prevent the application of plate voltage to the tube, and would probably burn out plate resistor R4. (Refer to Low-Frequency Compensation Circuit diagram.) Failure of the plate sup ply voltage would interrupt circuit operation in the same manner. Application of plate voltage to the tube would also be interrupted if plate resistors R3 or R4 became open-circuited, again resulting in no output.

Reduced or Unstable Output. Assuming that a video signal of proper amplitude is present at the input to the video amplifier, a partially or completely shorted grid coupling capacitor Cl may be the cause of a reduced or severely distorted output. If the capacitor is partially shorted, any value of a dc voltage which may be present at the input terminals of the circuit would be applied to the grid of the tube. Appearing to the tube as a change in grid bias, this voltage, if positive, may shift the operating point of the tube toward or into the saturation region, causing severe distortion by limiting the positive peaks of the input signal. If grid resistor RI became open-circuited, grid blocking would result from the accumulation of charges due to the signal voltages on the grid, which could not return to ground. Should cathode capacitor C2 become shorted, the cathode bias would be removed, and the cathode would operate at a fixed ground potential. This would change the operating point on the tube's  $E_g-I_p$  characteristic curve, allowing more plate current to flow, and probably operate into the saturation region, with the consequent severe distortion in the output signal. If, on the other hand, cathode capacitor C2 became opencircuited, the cathode voltage would rise and fall with the grid input signal in cathode follower fashion. This would introduce degeneration, which would result in a reduced value of output signal. If the video amplifier circuit contains low-frequency compensation, and capacitor C3 in the compensation network became open-circuited, the compensation characteristics

would be lost, and distortion might result, rdthough this distortion might not be very noticeable.

# PENTODE VIDEO AMPLIFIER

# Application.

The pentode video amplifier is used to amplify, without attenuation, a band of frequencies between approximately 10 Hz and 6 MHz. This amplifier is normally used to amplify a higher level of input signal than the triode video amplifier, and as a result it can furnish an output signal of considerably higher power than may be realized from a triode amplifier. The pentode video amplifier is used in television and communications applications, and in particular in radar receivers, where it often follows the detector stage.

## Characteristics.

Operated as a Class A amplifier to obtain an output signal which reproduces the input signal without distortion.

Output signal is of reverse polarity to that of the input signal.

Input signal may be continuous or pulsed, and of either positive or negative polarity, or both.

Frequency response is more linear throughout the operating range than that of a triode video amplifier.

Over-all gain per stage is higher than that of a triode video amplifier.

Output voltage is higher than that of a triode video amplifier when operated from the same supply voltage as a triode.

Harmonic distortion is less, for the same output voltage, than that of a triode.

# Circuit Analysis.

**General.** Pentode video amplifiers may be classified in four circuit variations, according to the type of bias and the type of screen supply. The bias may be either zero-bias or self-bias, while the screen **sup**ply may utilize either a screen resistor or a fixed value of screen voltage. The basic circuits for each of these variations are shown in the accompanying illustration.

The pentode video amplifier has higher plate efficiency and greater power sensitivity than a triode video amplifier, as a general rule, but at the same time it suffers higher odd-harmonic distortion. In order to reduce this type of distortion to a minimum, negative or degenerative feedback may be used. However, this reduces the over-all gain of the amplifier. The output circuit usually utilizes resistance coupling or resistance-capacitance coupling, although in some applications transformer coupling or inductancecapacitance (choke) coupling may be used. When resistance coupling (or resistance-capacitance coupling) is used, the load resistance for maximum power output is usually within 10 percent of the value obtained by the formula:

$$\mathbf{R}_{\mathbf{L}} \simeq \frac{0.9 \ \mathbf{E}_{\mathbf{b}\mathbf{b}}}{\mathbf{I}_{\mathbf{p}}}$$

where:  $\mathbf{R}_{L}$  = plate load resistance

 $\mathbf{E_{bb}}$  = plate supply voltage (on the source side of  $R_L$ )  $1_P$  = plate current

The power output is less than the value  $E_{bb}I_p/2$ , because of the power loss in plate resistor  $R_L$ . Plate efficiency, for a total harmonic distortion of less than 10 percent, is approximately  $35 \pm 7\%$ . The overall output circuit efficiency is lower than this value, since the output efficiency is a function of both the plate current and the screen current, and the screen current is wasted insofar as the output is concerned.

Circuit Operation. The following schematics illustrate four basic circuit variations of the pentode video amplifier. In circuit A, the the tube is opperated at zero bias, with the cathode grounded, and the screen voltage is supplied through screen resistor R2, which is bypassed by capacitor C2. In circuit B, the tube is operated at zero bias, but the screen is held at a fixed voltage through a direct connection to the screen power supply. In circuit C, the tube is operated with cathode bias obtained through the use of cathode resistor R2, which is left unbypassed to provide degeneration, in order to improve the over-all frequency response. The screen voltage is supplied through screen resistor R3, which is bypassed by capacitor C2. In circuit D, the tube is operated with cathode bias by means of cathode resistor R2, which is left unbypassed by provide degeneration. Inductor L1 is connected in series with plate-load resistor R3. Inductor L1 and resistor R3 act to extend the response to the higher frequencies.

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Pentode Video Amplifier Basic Circuit Variations

In circuit A, the pentode is operated at zero bias, since no cathode resistor is used, and the grid is returned to the grounded cathode through grid resistor RI. Cathode circuit degeneration at low frequencies, and the resultant loss of gain, is thereby eliminated. This loss of low-frequency gain is evident in circuits using cathode bias, with a bypass capacitor shunting the cathode resistor, because of the increasingly higher capacitive reactance offered by the bypass capacitor as the frequency is decreased below a few hundred Hz. The disadvantage of zero bias, however, is the limitation imposed on the input signal, in that the input signal must not be so great as to drive the grid to saturation and the condition of grid current flow. The screen voltage is supplied, from the power supply, through screen resistor R2, in order to operate the tube at the proper screen potential, which under normal conditions is of a lower value than the

plate voltage. The screen resistor is usually bypassed by a screen capacitor, C2. The **R-C** circuit which results from the combination of R2 and C2 provides a small amount of degeneration similar to that provided by an unbypassed cathode resistor. Since the normal screen current is only a small percentage of the plate current (1 O to 15 percent), the amount of degeneration is proportionally smaller. The degeneration approaches a negligible value when the time constant of the R-C circuit, R2 and C2, is greater than four times that of the lowest frequency which is to be passed by the amplifier.

In circuit B, the pentode is operated at zero bias, similar to that of circuit A. The screen, however, is supplied directly from the power supply, without the use of a screen dropping resistor. By this means the screen voltage is held to a practically constant value, assuming that the impedance of the power supply is

of a relatively low value. As a result, no degeneration is provided by the screen circuit, and the voltage gain of this circuit is slightly higher than that of circuit A.

In circuit C, the pentode is operated with cathode bias, the amount of which is determined by the values of the cathode resistor and the plate and screen currents. The cathode resistor is left unbypassed, in order to provide degeneration, which increases the over-all frequency response of the amplifier and reduces the distortion and/or noise which may be introduced within the amplifier itself. In a number of amplifier circuits, including those designed for audio frequencies, the cathode resistor is bypassed by a capacitor of a relatively large value. The capacitor acts as an extremely low impedance path for all frequencies higher than approximately 200 Hz. As the frequency of the signal to be amplified decreases below this value, the reactance offered by the bypass capacitor increases very rapidly, and as a result the gain at lower frequencies decreases. In order to avoid this decrease in gain in the video amplifier, this bypass capacitor is omitted from the circuit. The gain at the low frequencies is thereby held to approximately the same value as the gain at the medium frequencies, but the over-all gain of the circuit -at all frequencies - suffers a decrease in value, because of the degeneration introduced by the cathode resistor. The screen voltage is dropped, from the power supply potential, through screen resistor R3 to the proper value for pentode operation. The effect of the screen

resistor-capacitor combination is similar to that described for circuit A.

In circuit D, the pentode is operated with cathode bias, in a manner similar to that of circuit C. The screen is supplied by a fixed potential directly from the power supply, and no screen resistor is used. Degeneration due to the screen circuit is thereby avoided, as in circuit B. In this plate circuit, in series with plate load resistor R3. This comprises a shunt peaking circuit, which acts to keep the response flat to a much higher frequency than may be obtained with a simple resistive plate load. A more complete discussion of compensation circuits, including shunt peaking, is given in connection with the triode video amplifier, previously described.

A practical application of some of the circuit variations already discussed is given in the following illustration, which shows the pentode video amplifier circuit used in the AN/SPS-10D Radar Set. In this circuit, the video input signal is applied through coupling capacitor Cl to the grid, which is returned to ground through grid resistor RI. The amplifier tube, a type 6AU6, is operated with cathode bias obtained by means of cathode resistor R2. Partial bypassing is provided by capacitor C2, which, because of its low value of capacitance (130 pf), offers a low impedance only to the higher frequencies. The screen grid is held at a relatively fixed potential from the power supply, through the voltage divider R3 and R4 and its filter.



Pentode Video Amplifier Circuit Used in AN/SPS-10D Radar Set

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network C3 and C4. In this case, the **R-C** circuit consisting of R4 and C4 provides negligible screen degeneration, because the junction of R4 and R3 is held at a relatively constant potential by voltage-divider action. A shunt peaking compensation circuit is provided in the plate circuit, by means of inductance L1 in series with plate-load resistor R5. The use of plate shunt peaking maintains the output response flat to a much higher frequency than possible without its use. The output of the video amplifier is taken through C5, the output coupling capacitor.

## Failure Analysis.

**No Output.** Assuming that a signal of sufficient amplitude and proper polarity is applied at the input to the pentode video amplifier and no output is obtained, the tube should be checked for proper operation. An open coupling capacitor Cl or an open cathode resistor, if used, would interrupt the operation of the circuit. An open plate resistor or screen resistor, if used, or failure of the plate or screen power supply would likewise be a cause of no output. If shunt peaking is used in the plate circuit, an open-circuited inductance L1 would interrupt the plate current and result in no output.

Reducad or Unstable Output. With a video signal of proper amplitude and polarity present at the input to the pentode video amplifier, a leaky or shorted input coupling capacitor Cl may be the cause of a reduced or unstable output. A leaky capacitor may allow a dc voltage from the output of the previous stage to be present on the input grid; this would change the value of bias and cause distortion in the output signal, or reduce the output to a low value or even to zero. An open grid resistor R1 would probably cause grid blocking, or audio oscillation at a slow rate. If the cathode bypass capacitor C2 became open-circuited, if one is used, degeneration would be introduced and the output would be considerably reduced in value. If the capacitor became shorted, the cathode would operate at zero bias, and the output would probably be distorted although of a higher value. Should the screen bypass capacitor become shorted, the output would be reduced to an extremely low value, and in addition the screen resistor would probably overheat or burn out, because of excessive current flow. Another cause of reduced output may be traced to a reduced value of plate or screen voltage, due to a faulty power supply. If a

voltage divider is used in the screen voltage supply, similar to that shown in the illustration of the AN/SPS-10D video amplifier circuit, an open resistor at the ground end of the voltage divider would in crease the voltage at the screen. This would probably increase the plate current sufficiently to overload or burn out the tube. In either case, the output signal would be severely distorted.

# TRIODE VIDEO DRIVER AMPLIFIER (ELECTRON TUBE)

#### Application.

The video driver amplifier is used to amplify radar or other video signals to the proper level for driving the cathode-ray indicator tube.

### Characteristics.

**A negative** output signal is provided for application to the CRT cathode.

Cathode bias is used, in combination with a fixed negative bias on the grid.

A positive video-input signal is required.

The cathode is partially bypassed at high video frequencies to provide gain stabilization and high-frequency compensation.

The tube elements are connected in parallel to provide increased transconductance.

Shunt or series peaking is not required.

Dc restoration is provided by a separate diode.

Law coupling resistance provides improved frequency response.

## Circuit Analysis.

General. A negative video output provides some definite advantages over a positive video output. Since the tube is necessarily biased near cutoff, the quiescent or resting current is much lower than would be required for positive video. As a result, the maximum tube rating for plate dissipation is seldom reached even when the tube is over-driven. By using a dual-triode with low coupling resistance, more gain can be obtained for a given bandwidth than from a single pentode stage. By connecting the triode elements in parallel, the theoretical transconductance is doubled; however, full advantage cannot be taken of this circuit arrangement, because a low value of loading resistance is employed in order to widen the bandwidth. Since the capacitances of both tube elements are in parallel, the effective input capacitance

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and output capacitance are greater. The triode driver stage is uaually the final (output) stage in a video amplifier chain. This stage always drives the cathoderay indicator tube, which requires a large voltage drive for intensity modulation of the CRT beam (little power is required); therefore, it is usually spoken of as a "videodriver stage" rather than a "video power-output stage".

**Circuit Operation.** The accompanying schematic shows a typical dual-triode video driver. The negative output of the driver is usually applied to the cathode of the indicator tube to reduce the cathode bias and illuminate the tube with full beam intensity at the negative peak of the output signal (which occurs at the positive peak of the input signal).



Triode Video-Driver Circuit

Capacitor C<sub>e</sub> is the input coupling capacitor; the output of the stage is uaually direct-coupled to the CRT cathode. Fixed negative bias is obtained from a voltage divider, consisting of RI and R3, to supply a few volts of negative bias to the dual-triode grids through common grid resistor R2. Grid resistor R5, in series with the grid of V1 B, is a parasitic suppressor, or "grid stopper", which prevents high-frequency oscillations due to the parallel connection of elements. Diode CR1 is a de restorer which operates as a

biased clamp on the input signal, so that the output signal always produces the same intensity on the CRT for identical input signals. Cathode bias is also supplied by R6, which is bypassed by Cl so that cathode degeneration occurs, improving the frequency response; thus, special video-frequency compensating circuits are not needed in the plate circuit. A positive input pulse produces an amplified negative output pulse across plate load R4.

With no signal applied, the fixed bias prevails and holds both half-sections of V1 near cutoff. (The total quiescent current flow is on the order of 0.5 to 1 milliampere.) The output voltage is zero, and practically the full plate voltage is applied, since the drop across load resistor R4 is less than 2 volts, Similarly, the cathode bias developed for the quiescent value of current is only a small fraction of a volt, and thus has practically no effect on the circuit at this time.

Assume that a positive-going video signal is applied through coupling capacitor CC. The positive input voltage reduces the fixed negative bias, thus increasing the plate current flow. The increased flow of plate current produces a voltage drop across plate load resistor R4 and cathode resistor R6. The plate voltage drop appears in the output as a negative and amplified output voltage, while the cathode voltage increases the applied fixed bias. Thus, as the amplitude of the input signal increases, the cathode bias also increases, and the effective bias is the total of both the fixed negative bias and the instantaneous cathode bias. The use of combined bias in this fasion provides a more linear input-versus-output voltage relationship. Normally, adequate cathode bypassing prevents instantaneous changes in bias from producing degenerative voltages which oppose the effect of the input voltage. In this circuit, however, the value of the cathode bypass capacitor is selected to be sufficient only for the very high frequencies-not for medium and low frequencies. Thus, at high video frequencies the average cathode voltage remains constant, while at the lower frequencies the instantaneously developed cathode voltage opposes the input signal and reduces its amplitude. As the frequency becomes lower, the reduction is correspondingly greater. Thus, cathode degeneration assumes the form of inverse feedback and attenuates those frequencies which are normally amplified the most. The over-all result is to produce a wider and more uniform bandpass with a slight reduction in gain.

When the video input' signal swings in the negative direction, the signal adds to the bias and reduces plate current flow. The voltage drop across the plate load resistor is correspondingly reduced, and the output voltage rises toward zero. The negative-going input signal eventually reaches the fixed bias level, at which time the circuit is again in the quiescent condition. If the negative input signal drops below the bias level, the cathode of clamping diode CR I becomes negative with respect to the anode and the diode conducts, shunting the signal around grid resistor R2 so that no further reduction in output voltage can occur. The diode conducts until the input voltage equals or becomes more positive than the bias; during this time the output remains at the zero level. When the input signal again goes positive, plate current again flows, producing a voltage drop across R4 and a negative output.

By using a fixed negative bias of the proper value, the tube operates in the Class Al region and the zero output level is fixed to be almost that of the plate supply voltage. Thus, full advantage can be taken of the large supply swing available; that is sufficient voltage drive can be obtained from a single driver stage without using excessively high plate voltage or large values of quiescent current, as would be required in Class A operation, so that more output voltage is obtained for the same input signal. With the input signal operating on a low duty cycle and consisting of short-duration pulses, the amplitude is usually less than the bias level and the clamping diode will not operate. However, with large input signals greater than the bias level, and operating on a high duty cycle, the clamping diode will operate and hold the output at the same zero level. By properly selecting the value of the cathode bypass capacitor, sufficient cathode degeneration is produced to reduce the rise time to the same value as would normally occur in a properly bypassed driver cathode circuit with shunt peaking employed in the plate circuit. This eliminates the necessity of providing compensating inductance in the plate load, and avoids any adverse affect on the transient response of the amplifier. When properly designed, this circuit will produce a rise time of less than .05 microsecond without exessive overshoot and undershoot.

## Failure Analysis.

**No Output.** Lack of an input signal, improper bias, loss of plate voltage, a defective tube, or an open

cathode circuit can result in no output. If coupling capacitor C<sub>c</sub> is open, no signal will appear at the grid and there will be no plate output. Check for an input signal with an oscilloscope or a VTVM. If bias divider resistor R3 is open, full supply bias will be applied to the grid; thus, the tube will be biased far beyond cutoff and will not operate. If R3 is open, the voltage measured from R3 to ground will be the same as the bias supply voltage. If grid resistor R2 is open, no bias will be applied to the V1 grid and the tube will conduct heavily, with cathode bias from R6 biasing it near cutoff. In this case, with very large drive there is a possibility that a small output will be obtained. Ordinarily, however, this output will probably be so small as to be considered no output at all. If bias divider RI is open, a similar result will occur because of a lack of fixed bias on the grid; if it is shorted, the full bias supply voltage will appear on the grid, thus cutting off the plate current and the output. Use a voltmeter to determine whether the bias appears and, if so, whether it is normal. If cathode resistor R6 is open, the circuit will be incomplete (open) and no output will occur. If R6 is open, shunting the cathode to ground will produce an output, in which case R6 should be checked with an ohmmeter with the power off. (With the power on and R6 open, the voltmeter may act as a high-value return resistor and cause the stage to be biased off; or when used as an ohmmeter and properly polarized the batteries in the meter can furnish an almost normal bias to V1 cathode and cause an erroneous indication.)

If plate resistor R4 is open, no plate voltage will be applied and no output will be obtained. Check the supply, first with a voltmeter to determine that voltage is present, and then check the plate voltage to ground. If plate voltage is normal, and no output can be obtained with proper bias and input signal, V1 is probably defective.

Low Output. Improper bias, low plate voltage, or a defective tube can cause a low output. If the bias is low the diode restorer will clip off part of the input signal and cause a reduced output. Likewise, if the bias becomes too high it will take a larger drive to obtain the same output. Check the bias supply and voltage across RI, R2, and R3 with a voltmeter. If diode CR1 is shorted, grid resistor R2 will be removed from the circuit and the grid signal voltage will be developed across R3 alone. This will lower the grid input impedance and reduce the drive, resulting in a reduced output. Check CR1 for forward and reverse

resistance with an ohmmeter. If R2 is large, which it normally is, the diode need not be disconnected for this check. If there is no difference between forward and reverse indications and a low resistance is measured the diode is shorted. If a high resistance is indicated in both directions, it is open. Check the supply voltage and then the plate voltage with a voltmeter. If the plate voltage is low the output will be reduced. If plate resistor R4 increases in value with age an abnormally low plate voltage will result. Measure the resistance of R4 with plate voltage OFF, when the plate voltage appears to be extremely low, and the supply voltage is normal. A similar symptom can be produced by a defective tube which causes heavy plate current flow, or by low bias. If the tube is good, there is a possibility that the tube is oscillating and that the value of R5 is insufficient to prevem it. Check R5 with an ohmmeter with the plate voltage off. If resistance is normal, connect an oscilloscope across the grid and ground, and then across the plate and gound. If the waveform is found obscured by a broad, light, solid band across it the circuit is oscillating at radio frequencies. Check the wiring, particularly the parallel connections to the tube elements, to be certain they have not been lengthened or changed, substitute another tube, and as a last resort change the value of R5 to a much larger value.

Distorted Output. If the cathode degeneration is changed because bypass capacitor C 1 is open or shorted, frequency distortion will occur. The high frequency output (without degeneration) will be lower than the output at medium and low frequencies, and the stage will act like an uncompensated amplifier. Use an oscilloscope and a square wave input. Observe the input and output waveforms; with a positive input, the output signal should be negative, larger in amplitude, and of the same general waveform. A sloping vertical edge on the square wave indicates the rise or fall time is excessive, while a sagging flat top indicates low frequency distortion. Cl can be roughly checked by temporarily shorting it while observing the waveform on the oscilloscope. If the circuit is operating properly the waveform will be more distorted when Cl is shorted. If no change is observed, Cl is either open or shorted. Check Cl with an incircuit capacitance checker, or disconnect it and check for the proper capacitance value and for leak. age. Excessive leakage will cause Cl to act as resistor in parallel with cathode resistor R6. Checks for distortion should be made at frequencies which are not

effectively bypassed by Cl. If the check is made at a frequency to which Cl offers little or no reactance, the signal will probably appear slightly distorted whether Cl is working properly or not.

Check the rise and fall of the waveform for overshoot and undershoot. In test equipment applications it should be less than 170, in TV or Radar applications 5% to 10% is satisfactory, while in **Servo-equipment** 40% to 50% is acceptable. These tests should be made on a normally operating equipment so that the technician is familiar with the correct waveform appearance and permissible amount of distortion before trouble occurs. Waveforms are not required to be any better than those shown in the appropriate Technical Manual covering the equipment under test.

## BEAM-POWER VIDEO DRIVER AMPLIFIER.

## Application.

The beam power video driver is widely used in search radars to amplify video signals to the 35- to 60-volt level necessary for intensity modulation of the cathode ray indicator tube.

# Characteristics.

Fixed negative bias is employed to provide operation in the Class Al region.

A negative output is produced for a positive input signal.

Shunt peaking is used to compensate for increased rise time produced by the higher output capacitance of the pentode.

DC restoration is provided by a separate diode.

Provides greater output, more amplification, and better linearity than a single triode driver operating at the same voltages.

Requires more dc power than the triode (screen is - added) and plate current is larger.

## Circuit Analysis.

**General.** The beam-power video driver is similar to the triode video driver previously discussed in this section of the handbook. The use of a beam-power pentode tube provides greater amplification than the triode with an increase of linearity. The low input capacitance of the pentode decreases the rise time considerably, however, the large output capacitance greatly increases the rise time, so that the overall result is to increase the rise time to about double the triode value. Consequently, it is necessary to include

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a shunt compensating inductance in the plate circuit, since cathode degeneration, as used in the triode, is unable to provide sufficient compensation. The shunt-peaking compensating circuit is designed to reduce the total rise time to from 40 to 50 percent of that obtained without compensation, depending upon the tube type used. Because of the compensating circuit inductance the overshoot is increased to about 3% or about double that of a triode driver. The addition of the screen element in the pentode causes additional dc current to be drawn over that of the triode, which, since it does not directly contribute to useful output, causes a greater dc power loss and a drop in overall efficiency. It is necessary that the screen be bypassed to ground effectively for all frequencies employed. While the screen bypass capacitor is effective for the higher frequencies, it usually offers sufficient impedance at the low frequencies to provide a droop in low frequency output, which does not occur in the triode. The low frequency component of screen current, in effect, produces an inverse feedback voltage across the screen bypass impedance, which lowers the instantaneous screen voltage and reduces output at these frequencies. This action is similar to the degenerative action developed across a lightly bypassed cathode resistor. Unfortunately it is greatest at the very low frequencies near the dc level (1 to 15 Hz) which are normally amplified less than frequencies above this range, unless special low frequency compensation is used. Hence such screen degeneration cannot be used to flatten the overall response since it only further attenuates the low frequencies.

Although the single triode driver lacks the amplification of the beam-power driver, the parallelconnected, dual-triode driver usually provides equivalent performance and amplification without the problem of low frequency droop introduced by the screen element. With proper design, either circuit is effective in driving the indicator tube.

**Circuit Operation.** The schematic of a typical beam-power video driver stage is shown in the accompanying illustration.



**Typical Beam-Power Video Driver** 

Resistance coupling is employed in the input circuit;  $C_c$  is the coupling capacitor and R3 is the grid resistor. The output circuit is usually direct-coupled to the CRT cathode. Diode CR1 is a dc restorer connected across the grid resistor, and fixed bias is obtained from voltage divider R1, R2 connected across the separate negative bias supply. Screen voltage is obtained from the plate supply through series dropping resistor R5, bypassed by Cl. Resistor R4 is the plate load resistor, and L1 is the shunt-peaking inductance.

With no input signal, VI rests in a quiescent condition with a plate current of approximately 18 milliamperes, as determined by the fixed-bias voltage divider, RI and R2. The bias is in the Class Al region and is on the order of 10 volts negative. For small input signrds or for short duty cycle signals diode clamp CR1 has no effect, but for large input signals with long duty cycles, it clamps the bias at the fixed value, and prevents the grid from being driven into cutoff. Whenever the input signal makes the cathode of CR1 more negative than the bias value applied to its anode, forward conduction occurs, and the signal

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is shunted across grid resistor R3 to ground via R2. Thus the zero output level is maintained at the fixed bias value (see the Clampers section for a discussion of biased clamp operation). When a positive-going input signal appears on the grid of VI, plate current is increased. As the plate current is increased, a voltage drop occurs across plate load resistor R4; this is the negative-going output voltage. When V1 is operating, current flows from the cathode, through the grid wires, through the screen wires, and to the plate. A small dc screen current flow is caused by the positive screen absorbing some electrons as they pass through the screen wires. This screen current flows through screen voltage chopping resistor R5 to the plate supply and ground. The voltage drop across R5 maintains the screen voltage at the desired value. The effective screen voltage is that of the supply less the drop in R5, since screen current flow is in a direction which develops a voltage that opposes the supply voltage. Any instantaneous (ac) variations in screen current are bypassed through Cl to ground. However, at the very low frequencies the impedance of C 1 develops an additional instantaneous voltage drop between the screen and ground. This voltage is degenerative and opposes the screen voltage. Since the capacitive reactance of Cl varies inversely with frequency, the screen voltage is reduced at these instants, proportionately to the frequency, and the amplification is, likewise, reduced since the screen voltage controls the plate current. Thus, there is a droop in the waveform at the lower frequencies which are not adequately bypassed by screen capacitor Cl.

When the trailing edge of the positive input signal returns towards zero it is negative-going and the plate current is reduced. The reduced voltage drop across R4 produces the positive-going trailing edge on the negative output waveform. Any excessive drive in the negative direction is eliminated by the clamping diode as explained perviously above. When the plate current changes direction, the inductance of L1 tends to continue current flow in the same direction and causes a slight overshoot. Because the overshoot is kept below 3% by proper design and selection of component values, it causes only a slight amount of distortion. Peaking coil L1 is connected in series with plate load R4, and the total drop across this combination load varies in accordance with its impedance. As the frequency is increased, the reactance and hence the impedance of L1 increases as does the high frequency output, thus high frequency compensation is

achieved. For further information on this type of frequency compensation see the previous discussion of the Triode Video Amplifier in this section.

# Failure Analysis.

**No Output.** Improper bias, lack of plate or screen voltage, an open input circuit, or 10ss of input signal, as well as a defective tube can cause a loss of output. If voltage divider resistor R2 is open, the full negative bias supply voltage will be applied to V1 grid, the plate current will be cut off, and no output can occur. The same condition will occur if R1 is shorted except that, in this instance, the entire bias supply will be dissipated across R2, will cause it to heat, smoke, and eventually burn out. In either case check the voltage across R2 with a voltmeter. If either R1 or R3 is open no bias will be applied to VI, heavy plate current will flow and overload R4 and L]; eventually this will cause the weakest one to burn out. Meanwhile, the output will be held at a constant maximum negative value, causing the CRT to be constantly illuminated, and no signals will appear. Check the bias supply to ground, first with a voltmeter, then from R1 to ground, and finally from the grid of V1 to ground. Lack of voltage indicates that the failure is between the bias supply and the point measured. If the coupling capacitor C<sub>c</sub> is open, no signal will appear on the grid, and no output will occur even though normal bias and plate voltage are indicated on the voltmeter. On the other hand, if C<sub>c</sub> is shorted the plate voltage of the preceding video amplifier will drive V1 heavily into conduction and cause an indication similar to that of no-bias. In this case, the voltmeter will show a large positive voltage on the grid of V1.

If the plate supply is at fault, no plate or screen voltage will exist on V1, and no output will be obtained. Check the supply with a voltmeter and then check the voltage from screen to ground. If R5 is open, no voltage will appear on the screen, and the plate current will be so small that practically no output will be obtained. A shorted screen capacitor (Cl) will also cause a lack of voltage indication at the screen, since the entire supply will be dropped across R5. In this instance, R5 will heat abnormally, and will probably smoke and then burn out. If either R4 or L1 are open, no plate voltage will appear on V1; the screen of V1 would then attempt to function as a plate, and the heavy current flow will cause the  $\checkmark$ 

R5, cause it to smoke, and burn out. With normal bias voltage and screen voltage, and a higher than normal plate voltage, if no output voltage exists and an input signal is known to be applied, either tube VI is defective, or R4 is short circuited.

Low Output. If clamping diode CR1 is shorted, the input signal will be shunted to ground through R2 and a lower than normal output will be obtained. Should R2 increase in resistance the bias will be higher than normal and a reduced output will also occur. In the case of R2 the bias value can be checked with a voltmeter. However, to check the diode, it must either be removed from the circuit, or the plate and the bias supplies must be disconnected and the forward and reverse resistance measured. If the diode resistance is low, and is the same in both directions, it is shorted. If it reads a high resistance in both directions it is open. (It will normally indicate a high resistance in the reverse direction and a low resistance in the forward direction.)

If V1 is low in emission a low output will be obtained. If R5 increases in value, the screen voltage will measure lower than normal with rated supply voltage, and the output will also be low. A similar condition may be caused by a high resistance leak to ground through screen capacitor Cl. Check C 1 with an incircuit capacitance checker, or measure R5 with an ohmmeter, with the power OFF. When C 1 is disconnected the screen voltage will return to normal if the capacitor is defective.

If the plate supply is low, both the screen and plate voltages will be proportionately lower. If the supply and screen voltages are normal, but the plate voltage is low, V1 may be defective. Check L1 and R4 individually for resistance, with the supply voltage OFF. A poor soldered joint, or an increase in the resistance of L1 or R4 will cause a lower than normal voltage. If L1 measures more than 20 ohms, check its rated dc resistance in the equipment technical manual. Small inductors and chokes showing a higher than normal resistance will usually increase greatly in resistance when loaded, but appear close enough to normal to be within the allowable tolerance of a resistance check (20 percent maximum). In any event, the dc voltage drop when operating should only be a few volts.

**Distortion.** Usually a simple voltage and resistance check of the circuit will determine defective or offvalue parts. To determine distortion, however, it is necessary to observe and compare waveshapes, and check the input waveform against the output waveform against the output waveform. Also check the waveforms against the specific waveshapes indicated in the equipment technical manual. Use an oscilloscope to observe the operating waveform. The point where it departs from normal indicates roughly the circuit area at fault. Remember, also, that all amplifiers have a slight amount of distortion, but there are tolerances which must not be exceeded. For example, the excessive output capacity of the beam driver circuit and that of the CRT cathode to ground, plus the wiring capacitance, will reduce the rise time. Thus, the leading and trailing edges may have a slight slope rather than being ideally vertical. Likewise, the flat top portion of the pulse can be expected to droop or sag slightly. With inductive parts in the plate circuit there will also be some overshoot and undershoot, caused by the effect of inductance on the transient response. Thus the output waveform will never be identical to that of the input waveform, but they will resemble each other closely. The response of the vertical amplifiers in the test oscilloscope will also affect the apparent waveshape appearing on the screen. When checking waveforms, always make certain that the test equipment is capable of producing the same result as that of the original.

When sloping vertical shapes are observed, look for deteriorated high frequency response caused by an excessive shunting capacitance to ground. For sloping horizontal lines, look for deteriorated low frequency response caused by a defective low frequency compensating circuit, or inadequate cathode and plate, or screen bypassing. By temporarily paralleling the suspected component with a similar part it is usually easy to determine if the suspected part is having the effect on waveshape for which it was designed. Do not make any unauthorized modifications in Navy equipment because it may appear to be better to you, since you may be overcompensating instead.

# CHAIN (MIXER, AMPLIFIER, AND DRIVER) VIDEO AMPLIFIER (ELECTRON TUBE)

## Application.

The chain video amplifier is used in a radar display system to mix positive radar video with positive marker pulses, to invert the combined signals, and amplify them to a level sufficient to intensity modulate the cathode ray indicator.

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## Characteristics.

Consists of three basic circuits combined together in cascade.

Uses fixed or self bias, as applicable.

Uses dual triodes to save space and provide adequate amplification.

Requires positive inputs, and supplies a negative output.

Amplification is variable from 30 to 60 times.

Minimum rise time is 80 nanoseconds, with a maximum delay time of 50 nanoseconds.

Droop is not greater than 6% for a 500 microsecond pulse.

Maximum input signal is l-volt peak, with a maximum duty factor of 0.05.

Maximum output is 60 volts peak.

## Circuit Analysis.

General. The chain amplifier consists of three basic circuits: a common cathode type video mixer, a two-stage intermediate amplifier, and a video driver. Each of these basic circuits is described separately in this handbook. For an explanation of the video mixer, see the Common Cathode Video Mixer in the Mixers and Heterodyners Section of this handbook. The intermediate amplifier consists of two identical stages, with the exception that a volume control is added in the cathode of the second stage. See the discussion of the Triode Video Amplifier, and that of the Triode Video Driver Amplifier earlier in this secion for a detailed discussion of these two basic circuits.

Circuit Operation. The accompanying schematic illustrates a typical chain video amplifier.



Chain Video Amplifier

Since each of the basic circuits is fully described elsewhere in this handbook, as stated above, the circuit operation discussion will be limited to a simple functional signal description with characteristics. See the specific basic circuits for any additional information.

Tube VI is a dual-triode connected as a common cathode video mixer. Resistance coupling is used to supply two identical, high-impedance, grid-input circuits. The plates are paralleled and the output is taken from cathode resistor R3, which is common to both circuits. When a positive input is applied to either grid of VI a positive output voltage is devel-

oped across the cathode output resistor. Because of the cathode follower connection, the circuit is degenerative and no gain is obtained. With approximately 1-volt positive input, about 0.65 volt positive output is developed. For equal amplitude inputs which are in time coincidence, the output is additive and at a maximum. The extent of the adding, primarily, depends upon the value of the cathode resistance and the input signal amplitude. Generally speaking, the largest input signal tends to dominate the output, and the additive factor becomes zero if one of the signals is more than double the amplitude of the other. The low impedance output of VI is RC coupled to two

intermediate level, cascaded triode video amplifiers. V2 is a dual triode using each half-section as a separate stage of video amplification. The positive signal from the cathode of VI is applied to the grid of V2A, which develops a negative output signal across plate load resistor R5. The plate of V2A is RC coupled to the grid of second half-section V2B, so that both stages are cascaded. When the negative driving signal appears on V2B grid, a positive output is developed across plate load resistor R8 for application to the driver stage grid. The cathodes of both stages supply cathode bias through partially bypassed resistor R6 and R9, to provide degeneration at the lower frequencies and thereby improve high frequency response. The fixed cathode resistors of these two stages are identical, however, they are bypassed, with different values of capacitance, because additional resistance in the form of gain control RIO is connected in series with cathode resistor R9 of the second stage and ground. Gain control R1O is only partially bypassed to retain the full degenerative action of these cascaded stages. Overall gain is approximately 15 times, and the gain control permits control of volume over a 2 to 1 range.

The positive output of V2B is also RC coupled to driver stage V3, another dual triode. The elements of V3 are paralleled to provide greater transconductance and more gain. Fixed bias is applied the V3 grids from separate bias source, with partially bypassed cathode resistor R14 supplying degenerative cathode compensation so that plate peaking circuits are not required. The driver stage supplies a gain of approximately 6, and uses a diode dc restorer (CR1) as a biased negative clamp for high level signals. When a positive signal is applied to the grid of V3, a negative output is developed across plate resistor RI 5 for application to the CRT cathode. A maximum peak voltage drive of 60 volts is obtained for intensity modulation of the CRT indicator. The low output capacitance of the triodes provides good rise time response, and the samll quiescent. current of 0.5 milliampere provides efficient operation. The overall pass band is useful from 10 Hz to 1.7 MHz; by changing values and using subminiature tubes, the pass band can be extended to about 3.8 MHz. The high frequency limit is affected slightly by the setting of the gain control, because of the increased degeneration afforded at the low gain settings. Because of the limits permitted by tube specification MIL-E-I, the amplification may be changed by 25% if the tubes

are all selected for high tolerance. A ten percent change in both filament and plate voltage will only vary the amplification 12.5 percent overall. The previously stated values of input, output, and bandpass are made assuming normal plate and filament voltages, and tubes of average tolerance.

### Failure Analysis.

**General.** The detailed failure analysis for the individual stages is discussed at the end of each of the separate circuit discussions referenced at the beginning of this circuit description.

Use an oscilloscope and a square wave generator to isolate the trouble to a basic circuit, then troubleshoot the defective circuit in accordance with the detailed failure analysis for the specific circuit. For example, apply a 400 Hz square wave input signal to one input and observe the output with the oscilloscope. If the output waveform is normal, apply the square wave to the other input and observe that a similar output occurs. Any difference in output indicates trouble in the individual channels of stage VI. Then apply two equal signals simultaneously to both inputs and check for a similar but larger output. If no output, a low output, or a distorted output is obtained during any of these checks connect the oscilloscope successively to the output of each stage. Proceed from the output back towards the input and note when the signal observed on the oscilloscope assumes its normal shape and approximate output level. As an example, assume that with normal input applied both input channels, the driver output is found to be almost normal in amplitude, but distorted. When the oscilloscope is removed and connected to V3 grid, the signal amplitude is reduced, but the distortion is still evident. However, when the oscilloscope is connected to the grid of V2B the distortion disappears. The trouble then exists in tube V2B, its associated circuit, or in the coupling circuit between V2 and V3. Observing the waveform at the plate of V2B will quickly eliminate the coupling circuit. A voltage check of V2 will then reveal if the element voltages are normal, if the voltages are normal tube V2 is probably at fault.

Note that in this case no tubes were replaced or voltages measured until the approximate location of the trouble in this circuit was pin-pointed by the visual waveform check. While the tube could have been replaced and the element voltages measured as soon as the output was seen to be abnormal, it is evident

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that a procedure of this sort is basically a waste of time, and even though the trouble might have been elimnated in this manner, three tubes would have been replaced when only one tube actually was defective. Further tests of the tubes would then be necessary to determine which was at fault.

When operation of the circuits is understood and the trouble symptoms are carefully evaluated, much needless testing can be avoided. The cause of the trouble can usually be determined by applying basic circuit theory. In the doubtful cases, a systematic method of testing such as just described will prove superior to any cut-and-try methods, or hit-and-miss guessing.

# CATHODE-COUPLED (IN-PHASE) VIDEO AMPLIFIER

## Application.

The cathode coupled video amplifier is used as an input matching amplifier, or as an intermediate level video amplifier in cascaded direct-coupled video states.

# Characteristics.

Usually is self-biased, **although** combination **fixed**and self-bias can be used.

Usually employs a twin triode for space and economic reasons.

Operates in-phase (a negative output occurs for a negative input and vice-verse).

Provides a high input impedance with a moderate output impedance.

Requires no special frequency compensating circuits.

Inverse feedback from the degenerative cathode produces wideband response.

# Circuit Analysis.

**General.** The cathode-coupled video amplifier can be considered to be a combination of two basic circuits (a cathode follower and a grounded grid amplifier) comected in a cascade arrangement without any coupling elements. The elimination of the necessity for coupling elements through the use of directcoupling improves the low frequency response. Since most detectors provide a negative output, this circuit may also be conveniently direct-coupled to the detector, and can be either dc or ac coupled at the output. All the advantages of the cathode-follower input are maintained, while the grounded-grid output circuit provides more gain with greater stability and less tube noise. The output circuit can also be easily matched to the following stage for maximum output by proper choice of load resistor. Since the cathode degeneration is effective for both input and output stages, increased linearity is obtained with better overall frequency response and a wider bandpass than for conventional plate-coupled stages.

**Circuit Operation.** The accompanying schematic illustrates a typical cathode-coupled circuit with an in-phase output.



Cathode-Coupled (in-Phase) Video Amplifier

A twin-triode tube is used, with one half-section, VIA, operating as a cathode follower, while the second-half-section, V1 B, operates as a grounded grid output stage. Cathode resistor  $\mathbf{R}_{\mathbf{k}}$  functions as a common cathode resistor which supplies bias for both tubes, and as the load across which the input is developed and applied to the output stage. The output voltage is developed across plate resistor  $\mathbf{R}_{\mathbf{k}}$  in the second half-section of VI.

With no input signal applied, both tubes rest in the quiescent condition, and, since  $R_k$  is common to both tubes, the initial bias is determined by the total cathode current of both tubes. When a negative input signal is applied to the grid of VIA the plate current is reduced, and less cathode voltage is developed

across R<sub>1</sub>. Since the cathodes of both half-sections are connected together, the instantaneous cathode bias is reduced, and both half-sections tend to draw more plate current. Plate current flow through VIA is determined by the effective bias, which is the difference between the input signal and the developed cathode bias. Current flow through R<sub>k</sub> is in a direction which places a positive polarity on the cathodes and a negative polarity at ground. Since the grid of VIB is grounded the reduction of cathode voltage has the same effect as if the grid of V1 B were driven less negative, or in a positive direction. Thus plate current flow through load resistor  $\boldsymbol{R}_L$  increases and produces a plate voltage drop. The increased drop across the load resistor appears as a negative-going output voltage. Thus the output polarity is the same as the input polarity. The increased plate current flow in VIB, in turn, increases the total cathode current through  $\mathbf{R}_{\mathbf{k}}$ and produces an increasing positive cathode bias. Thus circuit operation is degenerative and operates with the effect of inverse feedback. Design is such that the common cathode resistor is lower in value than the plate load resistor. Hence, for any change in plate current of VIB the degenerative cathode voltage developed is less than the output voltage. The effective drive voltage for VI B is the difference between the degenerative voltage developed across the cathode resistor and the input signal applied to the grid of VIA. It is less than the input voltage, because the cathode follower stage has less than unity gain, otherwise, the input signal would be cancelled out and no output would occur.

When the input signal swings positive, the opposite action occurs. Plate current in VIA is increased, and produces an increased cathode current and larger bias across  $R_k$ . The larger bias is applied as a negative swing to the grid of VI B and reduces the plate current, likewise. Reduction of plate current in V1 B causes a reduced cathode current flow through  $R_k$ . This inverse or degenerative feedback reduces the totai output voltage over what it would normally be without degeneration, but still permits effective amplification of the overall output.

Design is such that the total amplification is about half of that normally obtainable from the same stage, using plate coupling instead of cathode coupling. Although full tube gain is not obtained, cathode degeneration provides an improvement in linearity and prevents any possibility of overdrive and distortion occuring. In addition, the overall response of the amplifier is broadened by the degenerative feedback. Any tendency of the amplifier to amplify a signal of one frequency more than another frequency is reduced automatically by the increased degeneration produced by the stronger signal. Thus the amplification is made more constant over a wider range than normal, so that the response curve is flattened, resulting in a wider bandpass. The use of direct coupling between the two stages eliminates any problem of phase shift in the coupling capacitor or any reactive effects which would attenuate the lower frequencies. Consequently, shunt- or series-peaking circuits are not required to produce satisfactory video response. In some applications, two twin triodes are cascaded to supply maximum gain.

If a plate load resistor is connected in series with the plate of VIA, operation is substantially the same, except that an out-of-phase output can be obtained. With resistors in both plates, dual and opposite outputs can be obtained with the circuit operating as a phase inverter for push-pull operation.

# Failure Analysis.

**No Output.** Lack of supply voltage, plate voltage, or improper bias will cause loss of output. If either half-section of V1 is defective, or if no signal exists on VIA no output will be obtained. A simple voltage check of the supply, and then from plate to ground will determine if lack of plate voltage is the cause. A check of the bias voltage developed across  $R_{k}$ , with no signal applied, will determine if the proper bias exists; if not, either the tube or resistor is at fault. Loss of input signal can be checked with a VTVM or by observation with an oscilloscope.

Low Output. Improper plate or bias voltage, a defective tube, or a reduced input signal will cause a reduced output. Check the plate and bias voltages with a voltmeter. If the input signal is normal in amplitude as observed on an oscilloscope or VTVM, but the output is low, replace V1 with a known good tube.

Distorted **Output**. Distortion can best be observed with an oscilloscope and a known input (apply a signal from a signal generator connected to VIA grid, or use a steady input signal to the detector). Observe the waveform on VIA grid, a similar waveform, but reduced in amplitude should appear at the cathode. Then check the waveform at the plate of VIB, a similar but amplified signal should appear. When distortion is visible at any of these points the cause is in the preceding circuit.

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# WI DE-5AND VIDEO AMPLIFIER (SEMICONDUCTOR)

The wide-band video amplifier is used to provide uniform amplification of video frequencies in radar and television receivers and display amplifiers before application to the cathode-ray-tube indicator or other video output device.

# Characteristics.

**Common-emitter configuration** is used to provide high gain. Transistors used must have an alpha (or beta) cutoff frequency higher than the highest frequency it is desired to amplify.

Class A bias is normally employed to minimize distortion.

Amplifier is specially frequency-compensated to provide wide-band response.

Compensating circuits may be employed in the base, emitter, or collector leads, and even between stages in the coupling circuit, to obtain the desired response curve.

Input impedance is on the order of 10,000 to 15,000 ohms, while the output impedance may be either high or low, depending on the requirements of the output device (high for CRT drive and low for coaxial line drive).

# Circuit Analysis.

General. The wide-band amplifier may be either a single stage for light loads, or a number of cascaded stages to supply large driving voltages, where appreci-

able output power is needed. Usually the CRT indicator is driven by the wide-band amplifier since only a little power is required to drive most cathode-ray tubes. The overall response is usually from 30 Hz to 6 MHz, although the response of television stages may be restricted to 4 MHz, and that of radar stages to as low as 2 MHz. When a response greater than 6 MHz is needed, special design techniques are employed, and the overall gain is usually much lower than that of the average wide-band amplifier. The transistors need not be matched, since design is accomplished for each stage individually, and the CE circuit provides better over-all response for mismatched stages. The relatively high-impedance load provided by a CRT is usually considered to be capacitively reactive, whereas the low-impedance load offered by the video (coaxial) line is normally considered to be resistive, since it is usually terminated by a resistor whose value is equivalent to the characteristic impedance of the line to avoid reflections. The types and methods of compensation are standard, but they may be used differently by each designer. It is usually considered more important to obtain the desired gain and response than to effect a savings by the limit use of parts and transistors. Where high power output is required, an external feedback loop is usually employed to provide stability and to improve the over-all response characteristic, in addition to the internal compensating circuits normally used.

Circuit Operation. The following schematic illustrates a typical wide-band amplifier using two transistors in cascade.



Wide-Bend Video Amplifier

In the schematic,  $\boldsymbol{C}_{\boldsymbol{cc1}}$  couples the base of Q1 to the preceding stage, usually the video detector, and prevents the dc base bias from being shunted through, or affected by, the detector circuit, Resistor R1 and R2 supply fixed voltage-divider bias to Ql, while R6 and R7 perform the same function for Q2. (See the introduction to this section for a discussion of bias arrangements and bias stabilization methods.) R3 and R8 are the emitter swamping resistors for Q1 and Q2, which are bypassed by Cl and C3, respectively. L1, L2, L3, L4, and L5 are compensating inductors inserted to improve the high-frequency response, while R5 and R9 are the collector load resistors. R4 and C2 form a low-frequency boost circuit in the collector circuit of Q1. C<sub>cc2</sub> is the interstage coupling capacitor. L3, together with the input capacity to Q2 form a series peaking circuit to improve the high-frequency response. The operation of the amplifier is similar to that of any other common-emitter, RC-coupled amplifier except for the effects of the compensating circuits.

When a sine-wave input signal is applied to Cccl, a voltage is developed across the series impedance of L1 and R2, and is applied to the base of Q]. Assume for

the sake of discussion that the sine wave is increasing in a positive direction. This positive swing reduces the negative base bias of Q1 and causes a reduction of emitter current. Since emitter resistor R3 is bypassed by Cl no degeneration is produced. However, as the emitter current reduces, collector current flow through R4, R5, and L2 also reduces. As the collector current reduces, the collector voltage rises towards the negative supply voltage and produces a negativegoing output voltage. This output voltage is applied in series with L3 and C<sub>cc2</sub>, appears across base resistor R7, and is also applied to the base of Q2. The negative-going output of Q1 increases the forward bias on Q2 and causes a greater flow of collector current through R9 and L5. At the same time the emitter current in Q2 also increases, but since it is bypassed by C3 only the high frequency component flowing through L4 changes, and the medium and low frequency components are not affected. Thus, as the input waveform goes positive, a positive going and amplified output waveform is developed in the collector circuit of O2.

During the negative half of the input signal, the signal adds to the negative forward bias and increases

current flow in the collector of Q1. The increased collector current flow creates a large drop across resistors R4 and R5 and inductance L2, developing a positive-going output voltage. This voltage applied in series with L3 and  $C_{cc2}$  appears across R7 and the base of Q2. Since it is positive-going, the forward base bias on Q2 is reduced and causes both the emitter and collector currents to fall also. The collector voltage of Q2, therefore rises towards the supply value and develops a negative-going output signal. Thus the input and output waveforms and voltages are in-phase. Since the transistors operate Class A, a linear and amplified output is produced. The frequency response and bandpass are affected by the compensating networks as follows.

The low-frequency response of the Q1 stage is basically determined by the time constant of Cccl and R2. Although L1 is in series with R2, its effect at low frequencies is negligible since its reactance is very small as compared with the resistance of R2. L1 is used to provide a high reactance (much larger than **R2**) at the high video frequencies, to avoid shunting them to ground through the relatively low resistance of R2. Since there is more than adequate gain at low frequencies, it is unnecessary to avoid, or to compensate for, any low-frequency shunting at this point. Fixed bias is used so that QI may be kept at the center of its operating curve for equal positive and negative swings, as is typical of Class A operation. R3 is affected only by dc changes caused by temperature differentials. When an increased emitter current flows through R3, a positive voltage is produced; this voltage opposes the forward bias, reduces emitter current and returns the operation to normal. Thus, R3 provides conventional emitter swamping action. Since Cl bypasses R3, the ac (signal) variation of emitter current do not pass through R3; hence, R3 has no effect on normal signal operation. As the collector current increases, electron flow is from the supply through R4, R5, and L2 to the collector. A low frequencies the reactance of L2 is very small, and it has practically no effect. Also, at these frequencies the reactance of C2 which bypasses R4 is very large, and can be considered as open. Thus, both R5 and R4 combine to form the collector load at low frequencies. At medium and high frequencies the reactance of C2 becomes very small and can be considered to short-circuit R4. Therefore, as the frequency increases, R4 is shunted out of the circuit, the collector load becomes smaller, and less output voltage is devel-

oped. Note that at the lower frequencies the output voltage is increased over what it would normally be without R4 and C2 in the circuit. Consequently, the combination of R4 and C2 function to extend the low-frequency response. As the high frequencies increase, the shunt output capacitance of Q1 and the shunt input capacitance of Q2 tend to bypass the signals to ground, thus lowering the output voltage at the higher frequencies. To compensate for this effect, L2 offers an increasing reactance (as the frequency increases) and, together with the output capacitance of Q1 (and stray shunt circuit capacitance to ground), forms a parallel-resonant circuit. Since collector resistor R5 is in series with this resonant circuit, it is broadly resonant so that the load impedance is increased over the mid-high-frequency ranges, and the output voltages does not drop over these ranges as it normally would. Thus, the bypassed resistor and the series inductor extend the low-frequency response and the high-frequency response of the circuit, respectively.

The output of the Q1 stage is coupled through capacitor  $C_{\scriptscriptstyle CC2}$  to the base of Q2. Although L3 is connected in series between the collector of Q1 and coupling capacitor  $C_{\rm\scriptscriptstyle CC2}$  , it has little reactance at  $\ensuremath{\text{low}}$ frequencies and thus has practically no effect on the low-frequency response.  $C_{\scriptscriptstyle CC2} is$  large and appears as a short circuit to the output signal from Q1, so that the signal is applied to the base of Q2 with practically no attenuation. Although the low value of bias resistance, R7, tends to shunt the input signal to ground, it is not frequency-responsive and does so equally for all frequencies. However, the input capacitance to Q2 is frequency-responsive and shunts the higher video frequencies to ground. To compensate for this loss and to increase the high-frequency response, the value of L3 is chosen to resonate with the input capacitance of Q2 at the higher video frequencies. Thus the highfrequency response is extended by this series peaking circuit to compensate for any input shunting effects. The signal at the base of Q2 is, of course, inverted in polarity by passage through the Q1 stage, and is again inverted in the Q2 stage to provide an output polarity which is identical to that of the input signal.

At the low video frequencies, swamping resistor R8 is shunted by C3, even though L4 is connected in series with C3, since the reactance of L4 is negligible at the low frequencies. As the video frequencies increase, however, the reactance of L4 increases while the reactance of C3 decreases. In effect, L4 acts as a

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choke preventing the passage of high-frequency components around R8. Since the high frequencies must now pass through R8, a degenerative voltage is developed by the flow of signal emitter current through R8. This degenerative voltage opposes the normal forward bias and requires a larger input signal to produce the same output. This is the same action that occurs with a partially bypassed emitter resistor, and is equivalent to negative feedback. Thus, the response at the middle and upper video frequencies is kept uniform, and positive feedback through capacitive coupling of the input and output signals is prevented with a slight loss in gain. At the frequency where the reactance of L4 and C3 are equal, series resonance occurs, and R8 is completely shunted (short circuited); there is no degeneration, and a peak response occurs. For all other frequencies L4 and C3 function as a variable-impedance shunt around R8.

Q2, like Q1, is biased Class A, and operates at the center of its transfer characteristic. Therefore, equal input swings develop equal and undistorted outputs across collector resistor R9. Compensating inductor L5 is connected in series with R9 as a shunt peaking circuit, to improve the high-frequency response and correct for the shunting effects of the collector-to-emitter capacitance of Q2, as well as the stray circuit capacitance in shunt to ground. When the output is applied to the control electrode of a CRT, the value of collector resistor R9 is made large in order to develop a large voltage drive. With a low-impedance output, R9 is usually made to match the impedance of the load, being on the order of 50 to 300 ohms, as required.

The schematic circuit just discussed illustrates the standard forms of frequency compensation employed in video amplifiers; however, each wide-band amplifier varies somewhat because of the desired response characteristics and the differences between the transistors. For example, in one amplifier compensating circuits may not be used in the base or emitter loads, but only in the collector and coupling circuits, whereas in another amplifier compensating circuits may be used in the leads of each transistor element. Usually, the greater the number of compensating circuits used, the greater the bandwidth and the better the uniformity of response.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of

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shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be careful, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. Lack of an input signal, improper bias, lack of supply voltage, or a defective transistor can cause a no-output condition. Use a voltmeter to determine the supply voltage and bias. Note that the voltmeter shunt will complete the circuit when you are reading voltages across open components; thus, erroneous indications can be obtained, leading to false conclusions. To avoid errors of this kind, it is better to use an oscilloscope to observe the waveform on the base of QI, and to follow the signal through the circuit, noting where it disappears. The trouble exists between the points where the signal last appears and where it disappears. If a signal exists on the base of Q1 but not on the collector, either R2, R3, R4, R5, L1, or L2 may be open. Continuity or resistance measurements will determine the defective part. This same condition can also be caused if Q1 is defective. If a signal exists at the collector of Q1 but not at the base of Q2, either L3, C<sub>cc2</sub>, or R7 may be open, or Q2 may be defective. A resistance check will determine whether L3 or R7 is open; if neither is open,  $C_{cc2}$  or Q2 must be at fault. Check the value of the capacitor with an in-circuit capacitance checker. If a signal exists at the base of Q2 but not at the collector, either R8, R9, or L5 is open, or Q2 is defective. If R8, R9, and L5 show continuity and proper resistance when checked with an ohmmeter, Q2 must be defective.

**Reduced Output.** Reduced output may be caused by improper bias, low collector voltage, a change in the value of the emitter and collector resistors, or defective transistors. The approximate bias and collector voltages can be determined with an ohmmeter. Then use an oscilloscope to follow the waveform through the circuit, noting where the amplitude of the signal changes to localize the trouble to the defective portion of the circuit. If R1 increases in value, the base bias on Q1 will be lowered; if R1 opens, the fixed base bias on Q1 will be effectively zero. Either condition will cause a reduction in output and probably an increase in distortion. If R6 increases in value or opens, it will create a similar condition for Q2. If either Cl or C3 is open, excessive emitter degeneration will occur and drastically reduce the output. If either R5 or R9 becomes shorted or changes to a lower value, less output voltage will be developed. A similar condition will be caused if Q2 is defective. The resistors can be checked for their proper values with an ohmmeter, and the capacitors can be checked with an **in-circuit** capacitance checker.

**Distorted Output.** Improper bias, overdrive, low collector voltage, or defective transistors can cause distortion. The bias and collector voltages can be determined with a voltmeter. Distortion can be most quickly seen and located by the use of an oscillo-scope. Apply an undistorted signal and check the waveform through the circuit. The location of the trouble will be evident when the waveform departs from normal. Overdrive will usually be indicated by a flattening of the tops and bottoms of a sinusoidal waveform, indicating that the signal is exceeding the bias voltage at the peaks. In the case of a square wave the amplitude will be reduced, causing amplitude distortion. Since the wide-band amplifier covers a large

range of frequencies, and the low frequencies are particularly susceptible to phase distortion, it is preferable to use a square wave for testing. Because it takes a number of harmonics to produce a square wave properly, the entire audio range may be checked by applying only two different square-wave frequencies, such as 60 and 1000 Mz. The video response can likewise be checked every 5 KHz up to 50 KHz (the usual limit of generator range). A sloping response to the leading or trailing edge of the waveform indicates poor high-frequency response, while a sloping flat top indicates poor low-frequency response. By temporarily short-circuiting a specific compensating circuit, the effectiveness of the portion under suspicion can be gauged. Distortion caused by regeneration (positive feedback) sometimes occurs in high-gain amplifiers, and is shown by a large-amplitude response peak (sometimes by oscillation), usually over a small range of frequencies. In comparison with a wide-band amplifier known to be operating properly, it will show as a hump or peak in what ordinarily would be a flat curve of uniform response.

PART 5-6 RF

# **R-F AMPLIFIERS**

### General.

R-F amplifiers are similar in many respects to other forms of electron tube amplifiers, but differ primarily in the frequency spectrum over which they operate. There are two general classes of r-f amplifiers, the untuned amplifier and the tuned amplifier. in the untuned amplifier, response is desired over a large r-f range, and the main function is amplification alone. In the tuned r-f amplifier, very high amplification is desired over only a small range of frequencies, or at a single frequency. Thus, in addition to amplification, selectivity is also desired to separate the wanted from the unwanted signals. The use of the tuned r-f amplifier is generally universal, while that of the untuned r-f amplifier is relegated to a few special cases. Consequently, when r-f amplifiers are mentioned, they are ordinarily assumed to be tuned unless otherwise specified. The tuning element usually consists of a parallel-resonant L-C circuit. It may be inductively tuned by a movable slug, with the tank capacitance fixed in value or consisting of the stray and distributed capacitance existing in the circuit. Or, as is usually the case, a fixed or slightly adjustable inductor determines the high-frequency limit, and a tuning capacitor is used to tune to the desired frequency or over a range of frequencies.

In receiving equipment, the r-f amplifier serves to both amplify the signaf and choose the proper frequency; in addition, it serves to fix signal-to-noise ratio. A poor r-f amplifier will make the equipment able to respond only to large input signals, whereas a good r-f amplifier will bring in the weak signals above the minimum noise level (determined by the noise generated in the receiver itself) and thus permit reception which would otherwise be impossible.

In transmitters, the r-f amplifier serves to amplify a single frequency (including any sideband frequencies produced by modulation) to a value suitable for application to the antenna. Basically, the receiver r-f amplifier is a voltage amplifier, while the transmitter r-f amplifier is a power amplifier.

As might be suspected, since the r-f amplifier is employed over the entire r-f spectrum, careful attention to design parameters is necessary to obtain proper operation. In the medium-, low-, and highfrequency ranges, conventional tubes and components are used. In the UHF, SHF, and microwave ranges, specially designed tubes and components are required to obtain optimum results (for example, the traveling-wave tube and the multi-cavity klystron).

In addition to the design requirements imposed by frequency, other considerations are often involved to obtain less noise and good selectivity with sufficient amplification, such as those involved in cascaded and cascoded stages. In other instances the r-f amplifier not only amplifies, but also serves to multiply the frequency. Each of the various types and classes of r-f amplifiers will be discussed.

The transistors used for r-f amplifiers differ in a number of respects from electron tubes. The forward transfer admittance is roughly 15 to 40 times larger than the corresponding tube transconductance. Both the input admittance and the input capacitance are also correspondingly larger. The base-to-collector capacitance may be equal to, or even less than, the grid-to-plan capacitance of an electron tube. However, because of the lower impedance levels involved in the transistor, this capacitance does not have as much importance as it has in tube circuits. The series resistances of the transistor elements also become higher at radio frequencies and produce a number of effects. For example, the base spreading resistance increases the amount of drive power required and causes instability in the amplifier. The emitter series resistance decreases the amount of drive power required, and also limits the amount of usable amplification because of the additional degeneration produced. The collector series resistance adds to the total output impedance to increase the gain, but also reduces circuit stability because of the possibility of regenerative feedback due to the higher gain. A phase shift is also produced in the output because of this collector resistance. Each of the above items will be discussed in more detail at the appropriate points below.

The tuned r-f amplifier is considered to be a narrow-band amplifier rather than a wide-band amplifier because it passes only a relatively small range of frequencies about the center of its band pass. Whereas the video (wide-band) amplifier passes frequencies from zero to 6 MHz or more, the r-f amplifier used in communications equipment usually does not pass more than 10 to 15 KHz, and in most instances less than this range. On the other hand, it

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should be noted that the r-f amplifiers used in television service, or for puked modulation, require a much larger bandwidth to accommodate the many sideband frequencies associated with these types of transmissions. Such amplifiers are considered to be special wide-band r-f amplifiers, except when the carrier frequency is so high that the modulation frequency is a small percentage' of this figure. For example, a 300-MHz carrier with a 10-MHZ modulating frequency would be adequately handled by a narrowband r-f amplifier, but a 30-MHz carrier containing a 10-MHZ modulation frequency would require a wideband r-f amplifier. Since semiconductor wide-band r-f amplifiers are not yet commonly used, the circuits to be discussed later in this section concern the conventional mrrow-band r-f amplifier.

R-F amplifiers are used for both receiving and transmitting. A receiver uses a low-power, smallsignal amplifier, while a transmitter uses a highpower, large-signal amplifier. Except for the conditions required by the power consideration, both types of amplifiers are similar and operate identically. Unfortunately, however, the transistor response or power gain is reduced as the frequency is increased. The response curve of a transistor is similar to that of a low-pass filter. That is, up to a certain frequency the gain is fairly uniform, and beyond this cutoff frequency the output drops rapidly toward zero. The limit of this upper cutoff frequency and the rapidity of dropoff depend to a great extent on the type of transistor and its composition. Many different types of transistors have been developed to extend the usable high-frequency range, such as the surface barrier transistor, the drift transistor, and others.

In addition to the loss of gain at the higher frequencies, the action of the transistor becomes complex; the transistor does not operate exactly the same at high frequencies as it does at lower frequencies. The internal resistance changes, and the effects of the junction capacitances become more pronounced. In high-frequency-amplifier applications, the collectorto-base capacitance causes positive feedback that may result in oscillation. The average value of collectorto-base capacitance for high-frequency transistors is on the order of 2 picofarads, as compared with 50 picofarads or more for transistors used at the lower (audio) frequencies. The base spreading resistance (resistance of bulk material of base) of the transistor increases at high frequencies, and the shunting effects of the low-resistance path produced by forward con-

duction of the base emitter junction tend to lower the input resistance, while the forward bias acts to reduce the width of the depletion areas and thus increase the base-to-emitter capacitance. At the same time, the internal flow of emitter current through the base-collector junction also reduces the width of the PN junction and increases the capacitance between the base and collector. It is this capacitance which causes feedback and tendency toward oscillation as the operating frequency is increased. At high frequencies the collector-to-emitter capacitance may be as high as 100 times that of the base-collector junction capacitance. For this reason, the common-base circuit generally gives better high-frequency response than the common-emitter circuit, but lacks the high gain of the common+ mitter circuit. Since the common-emitter circuit tends to be more stable at the higher frequencies than either the common-base circuit or the common-collector circuit, the design trend is to use transistors with a high alpha cutoff frequency, and the CE configuration for higher gain. Both CB and CE circuits will be discussed later in this section.

Unilateralization and Neutralization. In electrontube r-f amplifiers used at the higher radio frequencies, interelectrode capacitance causes positive feedback and oscillation. Neutralizing circuits are usually provided to prevent oscillation and to insure maximum gain with stability. Likewise, in the transistor r-f amplifier, the effect of the base-collector capacitance and the development of negative resistance through a change in internal parameters also causes oscillation. Neutralization circuits are used to prevent this oscillation and to obtain maximum gain. Neutralization represents a special form of unilateralization at a single frequency. When we speak of unilateralization, we are talking about the methods of making the transistor a one-way device. In other words, the input circuit is unaffected by the output circuit. Recall from basic theory that there is a reverse current effect and common impedance coupling within the transistor. This means that any change of current in the output circuit also develops a feedback current which affects the input circuit, and vice versa. Thus in tuned amplifiers a change of tuning in the output stage reflects back as a change of capacitance in the input circuit, and also as a change in the amount of output fed back into the input. In cascaded tuned stages such effects would cause alignment problems. As each stage was adjusted the

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preceding stages would have to be readjusted, since each adjustment would change the previous adjustment. The result would be that no two alignments would be alike and, likewise, neither would the performance and selectivity of the r-f amplifiers stages be comparable. Unilateralization deals with the method or circuitry whereby both the resistive and reactive portions of the circuit are cancelled so that there is no feedback from output to input, and, power is transferred unilaterally in only one direction, from input to output. Unilateralization of the circuit is not frequency-responsive; it is effective for all frequencies. On the other hand, neutralization is effective for only a single frequency or a relatively small range of frequencies. For example, it is only necessary to neutralize an i-f stage because it operates at a fixed center frequency. However, an r-f amplifier used in a multi-band receiver requires unilateralization to prevent the possibility of feedback or oscillation on any of the frequency ranges over which it operates.

A typical example showing the feedback elements and unilateralization elements involved in a commonbase amplifier is illustrated schematically in the accompanying figure. The elements  $\mathbf{r}'_{\mathbf{b}}, \mathbf{r}_{e}$ , and  $C_{cB}$  in the illustration are the internal parameters which cause feedback and oscillation at radio frequencies. Resistor  $\mathbf{r'_{b}}$  is the *base spreading resistance*,  $\mathbf{r_{c}}$  is the resistance of the collector-base junction, and C<sub>CB</sub> is the capacitance of the collector-base junction. The resistance of the collector-base junction is very high because of the reverse bias placed on the collector. At very high frequencies  $C_{CB}$  effectively shunts  $r_c$ . Assume that an input signal adds to the forward bias on the base (the base and collector bias supplies are not shown on the schematic for simplicity) and causes the emitter to be more positive than the base. Collector current i<sub>c</sub> increases in the direction shown by the arrow. A portion of the increase in collector current is fed through  $C_{CB}$  and  $\mathbf{r'}_{\mathbf{h}}$  in the direction shown by the arrow, and produces a voltage with the indicated polarity. This internal feedback voltage developed across  $\mathbf{r'_h}$  is of the same polarity and adds to the input voltage, causing a further increase in  $i_c$ ; this action is regenerative and represents positive feedback, which will produce oscillation. The external circuit elements inserted to neutralize this action are  $\mathbf{R_{N1}}$ ,  $\mathbf{R_{N2}}$ , and  $\mathbf{C_{N}}$ ; they correspond respectively, to  $\mathbf{r'}_{b}$ ,  $\mathbf{r}_{c}$ , and  $\mathbf{C}_{CB}$ . Since at high frequencies  $C_N$  shunts  $R_{N2}$ , this resistance is necessary

only at the lower radio frequencies. It is clearly seen that when the input signal causes a feedback voltage across r'b, a portion of increased collector current ic is also fed back through  $C_{N}$  and  $R_{N1}$  to the base. The direction of this external feedback voltage is as indicated on the schematic, and is direct opposition to the voltage developed across  $r'_{h}$ . When the internal and external feedback voltages are made equal, since they are of opposite polarity, they cancel and no positive or negative feedback occurs; thus, the circuit is unilateralized. In the common+ mitter circuit, since the polarity of the collector is opposite that of the input, it is necessary to develop an out-of-phase voltage and feed it back to the input. This is done through the use of a transformer, using the secondary winding to invert the feedback voltage, through a tapped tank circuit, or by use of a bridge circuit, as will be shown in some of the following circuit explanations. In some instances an inductance connected in series with a blocking capacitor is used between the collector and the base, with the inductor and the distributed capacitance in the collection circuit operating as a tuned, parallel-resonant circuit. However, inductive arrangements tend to be critical in adjustment since they are resonant only over a small range of frequencies near the center resonance point, and thus are not as frequently used. Partial emitter degeneration is sometimes employed in a similar manner to provide the feedback voltage. The accompanying figure shows some typical feedback circuits used for neutralizing the common-emitter configuration. The parts identifications are identical with these used in the common-base circuit explained



Feedback and Unilateralization Elements





Typical Common-Emitter Neutralizing Circuits

above, and operate in exactly the same manner; therefore, no further explanation is included to supplement the figure.

Selectivity and Impedance Matching. Since the narrow-band amplifier operates to amplify a band of frequencies around the center (carrier) frequency, tuned circuits are always used to obtain the desired selectivity. R-F amplifiers and i-f amplifiers are almost identical. Both are actually r-f amplifiers, but the i-f amplifier operates at a fixed (intermediate) frequency, which is usually lower than the frequency of the r-f amplifier. The amplifier normally consists of only one (or at the very most two) stages, whereas the i-f amplifier uses a number of cascaded stages to obtain high gain with the desired selectivity at the fixed i-f frequency. While the r-f amplifier is tunable over the entire range of reception, the i-f amplifier is fixed-tuned over only a small frequency range about the intermediate frequency. The selectivity is determined by the Q of the tuned circuit; the higher the unloaded Q, the greater the selectivity. When loaded the Q will drop; thus, the design is based upon the unloaded Q, since the loading is usually determined by the circuit configuration and bias. The bandpass of the tuned circuit is considered to be that range of frequencies covered between the half-power points on the selectivity curve (these occur at 70.7 percent of peak amplitude). Thus, a response down 3 dB at 5 kHz on either side of the center (carrier or i-f,) frequency covers a range of 10 kHz in bandwidth.

Although matching input and output impedances will provide maximum transistor power gain, this is not always possible. It is sometimes necessary to sacrifice gain to obtain the desired selectivity. In some instances by mismatching stages with individual high gain it becomes unnecessary to unilateralize or neutralize the stages. It is also difficult to obtain a high-Q circuit if the input or output resistance of the transistor which shunts it is low. Therefore, a variety of circuit devices are used to obtain the desired matching impedance while maintaining a high Q for optimum selectivity. Hence we find the simple singletuned, parallel-resonant tank, so popular with electron tubes, replaced by a tapped tank, or tuned by a capacitance divider for impedance transforming purposes. The following figure shows typical forms of coupling circuits used between cascaded stages of r-f or i-f amplifiers.



Im@danca-Transforming Circuits

In circuit A, the conventional single-tuned, transformer-coupled circuit is shown; the impedance relationships vary as the square of the turns ratio. In circuit B, a tapped auto-transformer is used; L1 plus L2 are the primary, while L2 is the secondary producing a stepdown impedance ratio. In circuit C, a capacitance divider is used to reduce the impedance between the input and the output. In circuit D, both the input and output impedances are different, and L1 helps to improve the over-all Q of the tank circuit. In E, a double-tapped transformer is used to supply high-Q primary and secondary tanks with the proper impedance matching for the input and the output. Since the Q of the circuit depends on the ratio of reactance to resistance in a coil, the lower the resistance and the higher the inductance, the larger the Q. Therefore, to match the low values of input and output resistance in the common+ mitter circuit, the large inductance is tapped at an appropriate point along the inductance. The square of the turns ratio between the lower and upper halves of the inductance determines the empedance at the tap. For example, in circuit B of the preceding figure, assume that the collector output impedance is on the order of 10,000 ohms and that the tap is located 1/5 of the distance between L1 and L2; since L1 will have 5 times as many turns as L2, a 25-to-1 impedance reduction results (impedance varies as square of turns ratio). The output impedance across L2 then would be roughly 400 ohms, and suitable for matching the input to a common-emitter stage. Naturally, the exact calculation is not as simple as in the example, since the loading effects of circuit capacitance and shunt

internal impedance must be considered; however, the example serves to illustrate the basic principle involved. In practice, the exact location of the tap is made experimentally, using the design equations as a guide.

At the higher frequencies, with a smaller number of secondary turns, unity coupling in r-f or i-f transformers becomes difficult to achieve; thus, capacitive coupling is generally used. Where extreme selectivity is desired, the transformers are usually double-tuned (both primary and secondary are tuned). This produces a sharper response, since two tuned circuits are used instead of one, and a flatter over-all response also results. Cascaded stages are often stagger tuned to provide a wider band pass; this is universally done in television i-f amplifiers.

The receiving r-f amplifier uses Class A bias to avoid distortion, while the transmitting r-f amplifier operates Class B or C for efficient power generation. At the present time, the following circuit discussions are limited to receiving types of r-f or i-f amplifiers.

## TRIODE GROUNDED-GRID R-F AMPLIFIER

## Application.

The triode grounded-grid r-f amplifier is used in receivers as a tuned voltage amplifier, particularly in the ultra-high-frequency ranges where it is impossible to use pentodes or beam power tubes. It is also used as a Class C linear power amplifier, especially in television transmitters.

#### Characteristics.

No neutralization circuit is necessary.

Can use either fixed or self-bias.

Has low power gain, but relatively high voltage gain.

Requires more driving power than a groundedcathode stage.

Grounded grid effectively isolates plate from cathode.

Operates Class A biased for reception, and Class C biased as r-f power amplifier.

Usually used with disc seal or pencil-type, closely spaced triodes at frequencies where coaxial lines are used as tank circuits.

Particularly useful in wideband applications such as TV, because it produces increased output power and efficiency in a particular tube for a given bandwidth.

## Circuit Analysis.

General. While the grounded-grid amplifier is most useful at UHF, it is sometimes used on lower frequencies for its inherent stability, and to avoid neutralization. With proper design, it also helps reduce "first stage noise" in receivers. However, the grounded-grid circuit is not generally used at the lower frequencies because of the extremely high gain possible with grounded-cathode pentodes. In transmitting applications it is usually used as a Class C linear amplifier, particularly in those applications where the driver stage has surplus driving power, because only a small amount of power is absorbed by the grid circuit, and the remainder is "passed through" to the plate circuit and adds to the total output because of the grounded-grid connection.

**Circuit Operation.** The accompanying schematic illustrates a typical grounded-grid circuit. For convenience, the tank circuit is shown as a conventional LC parallel-tuned circuit; in actual practice, however, coaxial lines or cavities are used at the high frequencies, where this circuit is usually used.



Typical Grounded-Grid R-F Amplifier Circuit

Input coupling capacitor  $C_{c1}$  functions as both a coupling capacitor and a dc blocking capacitor to isolate the input circuit from the antanna or previous stage. Thus, the cathode bias is not affected by the input circuit. Radio-frequency choke RFC keeps the cathode above ground, since the grid is grounded to the chassis. Resistor R1 is a conventional but unby passed cathode bias resistor which supplies Class A bias for VI (see the introduction to this section for

an explanation of cathode bias). The plate of VI is series-fed through voltage-dropping and decoupling resistor R2 and tank coil L1. Bypass capacitor C2 keeps the lower end of tank coil L1 at ground potential, and bypasses R2 for rf. Cl is the tank tuning capacitor, and the rator is grounded to eliminate body capacitance effects when tuning. The output is capacitively coupled through  $C_{c2}$  to the next stage.

When an r-f signal appears at the input, the low reactance of  $C_{c1}$  allows it to appear on the cathode of VI without any appreciable attenuation. The input signal may be from an antenna or a preceding r-f stage, and in some cases it may be that output of a tuned tank circuit. With the grid at ground potential, V1 is biased by the total cathode current flow through R1. With a positively biased cathode, the grid is effectively biased negative, and only quiescent Class A plate current flows. With no input signal there is no change in plate current and, consequently, no output.

Assume that an unmodulated r-f signal of constant amplitude appears at the cathode of V1. Since this signal appears between the cathode and ground, it can be considered as being supplied by a generator connected in series between the V1 cathode and ground. The r-f choke presents a high impedance to ground, and prevents shunting of the input signal to ground through bias resistor R1. On the positive r-f half-cycle the cathode is momentarily more positive resulting in the grid becoming more negative, so that a reduction of plate current occurs. In the plate circuit, the tuned parallel tank circuit, Ll, Cl, appears as a high impedance to the r-f component of the plate current. With less plate current flowing through the tank impedance, less voltage drop is developed across it and the plate voltage rises toward the source voltage (becomes positive-swinging). Thus, a positive output signal is developed and fed through C<sub>c2</sub> to the next stage. It is evident that the grounded-grid circuit produces an output signal which is in phase (of the same polarity) with the input signal producing it.

During the negative half-cycle of operation, the cathode becomes less positive (is driven in a negative direction). A negative cathode swing causes the plate current to increase, the produces a large voltage drop across the output load impedance (tank circwt). Since the voltage drop across the tank causes the effective plate voltage to be less, a negative output swing is developed. Again the output signal is in phase with the input signal. (This action is opposite the conventional 180degree phase shift produced in the 4

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grounded-cathode circuit, and corresponds with the action of the common (gounded)-base circuit in semiconductors). With the grounded-grid amplifier operated Class A, and with equal positive and negative swings, the average value of plate current does not change. The current flow from the cathode remains steady and occurs during the entire cycle; thus, cathode bias can be used, since the plate current is never interrupted. At the same time, the instantaneous signal changes cause larger (amplified) instantaneous r-f pulses of plate current, which produces the voltage drop across the tank impedance and an amplified output voltage. Note that the tank circuit must be tuned to the r-f signal to produce a high impedance and develop an output. Thus, signals with a frequency outside the tuned circuit bandpass are not amplified, or are greatly discriminated against.

From the above description of circuit functioning, it can be seen that the basic functioning of the grounded-grid circuit is similar to that of other types of r-f or audio amplifier circuits. Further consideration is necessary to develop the actions that are peculiar to this circuit alone.

Considered the following simplified equivalent of the grounded-grid circuit.



Simplified Equivalent Grounded-grid Circuit

The input signal is shown as an ac generator connected in series with input resistance  $R_k$ . Actually, the cathode input impedance is inherently very low, and electron flow is from ground to the cathode, through the grid to the plate, and back into the supply, producing the polarities shown in the simplified circuit. Since the grid is placed between the cathode and the plate, when grounded it acts as a shield which divides the circuit into two parts–an

input circuit and an output circuit, both at above--ground potentials. Hence, any coupling is effectively minimized by the grounded grid. Since electrons flow from cathode to plate, some electrons will be intercepted by the grid and carried to ground. Thus, there will be a greater flow of grid current than in the grounded-cathode circuit, where the grid is isolated from ground by a relatively high impedance. For this reason, the grounded-grid amplifier requires more drive than the conventional grounded-cathode amplifier. Since feedback resulting in oscillation normally occurs from capactive coupling between the output and input circuits, the good shielding of the grounded grid reduces this effect to a minimum. In addition, the interelectrode capacitances are reduced. The output capacitance is the grid-to-plate capacitance, which is usually the lowest in an electron tube; thus, capacitive shunting effects on the output are reduced at the higher radio frequencies to provide better performance. In addition, the plate-to-cathode capacitance is reduced, since it is the series capacitance produced by the plate-to-grid and grid-tocathode interelectrode capacitance. Actually, in practical tubes it is reduced to a value on the order of 0.2 picofarad, which is negligible, so that neutralizing is not normally required.

Since signal voltage  $e_{in}$  is connected between the cathode and ground, it is effectively in series with the tube place circuit; thus, in tuned r-f voltage amplifiers the output voltage is produced as though the circuit were driven in the normal manner (grounded cathode), but had an increased amplification amplification factor of  $\mu$  + 1. Hence, high voltage gain is obtained.

It is important to remember, however, that the matter of gain is relative. A low amplification factor tube will not give as much amplification as a high amplification factor tube. Nor will a triode give as much gain as a pentode at the lower frequencies. Thus, even though we speak of the grounded-grid circuit as providing high gain, it does not mean that the gain is as great as that provided by the groundedcathode circuit using the same tube and voltages. At the ultra-high frequencies where this circuit is most useful, the performance and gain are better because of the poor performance of the pentode. At the lower radio frequencies, it usually requires two stages of grounded-grid amplification to obtain results equivalent to those obtained with a single groundedcathode pentode stage.

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In power amplifier applications, low power gain is obtained because of the increased drive requirement and the low input impedance. The low input impedance, however, does not absorb all of the input (driving) power and cause a complete loss. Instead, the driving power is fed into the plate circuit (it is connected in series with the plate and cathode circuit), and adds to the total plate power (less the amount needed to drive the tube). The additional plate power supplied by the driver is distributed between the internal tube resistance and the tank circuit, so that only a portion is lost or dissipated in the tube plate. The total **outp:** power in watts is **equal** to  $I_p(e_{in} + E_p)$ , where  $e_m$  is equivalent to the rms value of grid voltage ( $E_p$ ).

In r-f power amplifiers with directly heated filaments, since the filament is also the cathode, it is necessary to use r-f chokes in the filament leads, or provide some other arrangement to keep the **filament** above ground and balanced. If the filament is not kept above ground, the filament and grid would be short-circuited, and the circuit would not operate.

When employed as a modulated power amplifier, the small portion of drive power which is inserted into the plate circuit remains unmodulated, making it practically impossible to obtain 100 percent modulation when plate modulation alone is used.

# Failure Analysis.

**No Output.** With proper bias and plate voltage, as checked with a voltmeter, only an open input circuit, lack of an input signal, or an open output circuit can result in no output. With input coupling capacitor  $C_{c1}$  open, no signal will be applied to the cathode and there will be no output. With output capacitor  $C_{cc}$  open, the signal will not appear at the output. Likewise, if the tube is defective, no output signal will appear. If capacitor C2 is shorted or R2 is open, there will be no plate voltage on the tube plate; thus, no output will be obtained. The capacitors can be checked with an in-circuit capacitance checker, while R2 can be checked with an ohmmeter. If the tube is suspected, check it with a tube checker. Do not neglect the possibility that the plate supply fuse may be open. The voltmeter check will usually indicate any abnormal operation. An open plate circuit will be indicated by no voltage at the plate. If the tuned output circuit is shorted, plate voltage will appear to be normal at the supply, but will be entirely dropped across R2 and thus be zero at the tube plate. If the

plate voltage is low, and excessive plate current is the cause, it will also cause a high cathode bias. If the bias is sufficient, the tube will be almost at cutoff and the output will be so low as to be mistaken for no output at all. If the cathode r-f choke is shorted, the bias and plate voltage will appear to be normal, but the input signal will be bypassed to ground through cathode resistor R1, and there will be no output. Where VI acts as a power amplifier, if Ccl is shorted or leaky, the cathode will be biased excessively by the plate voltage of the driving stage; this bias may cause plate current cutoff, and result in no output.

Low Output. If the bias is high, the plate voltage low, or the tube defective, a low output will be obtained. Check the bias and plate voltage with a voltmeter; if the voltage appear to be normal, check the tube with a tube checker. With selective tank circuits, a small amount of detuning of capacitor Cl will attenuate the signal considerably. Likewise, a high resistance in the tank circuit, caused by a poorly soldered connection, may cause sufficient loss of signal because of low circuit Q (and reduced selectivity) to produce a reduced output. An increase in the resistance of R2 due to aging will cause an increased voltage drop, low plate voltage, and low output. A change in the output load can cause a detuning effect on the tank and a reduction of output; the detuning can be compensated for by a slight readjustment of the tuning capacitor. If bypass capacitor C2 opens, the tank circuit, Cl, L1, will tune broadly and resonate over a different range of frequencies, and, if R2 is sufficiently small, will cause loss of signal through absorption by the power supply.

Distortion. The grounded-grid amplifier is subject to the same distortion possibilities as other r-f amplifiers. If the bias is too low, large r-f signals will in effect drive the grid positive, causing nonlinearity and saturation effects; thus, the plate waveform will be clipped at the peak of the cycle. If the bias is too high, the negative peaks will drive the tube to cutoff, clipping off the bottom of the signal. In both cases, a distorted output will result. Where modulated signals are amplified, it is imporatnt that the bandpass of the tuned circuits be wide enough to avoid sideband cutting, or the missing frequencies will cause distortion. The possibility of increased selectivity due to regeneration is less with the grounded grid than with 4 other circuits; however, the good shielding between the input and output may be nullified if the lead

dress is charged during a repair. Hence, when distortion seems to occur only at certain frequencies or over a narrow portion of the tuning range, or if whistles or squeals occur, neutralization or a lead dress correction may be required.

# PENTODE R-F VOLTAGE AMPLIFIER

# Application.

The pentode r-f voltage amplifier is universally used as the input stage in receivers or other cascaded r-f amplifier stages to provide a high signal-to-noise ratio with maximum voltage amplification.

## Characteristics.

May be either or untuned.

Operates at a specific r-f frequency or is tunable over a range of r-f frequencies.

Provide high gain (100 or better).

Uses impedance coupling at input or output where high gain is not required, and transformer coupling with or without tuning for high gain.

Uses cathode bias, or contact bias for small input signals.

Operates Class A at all times.

# Circuit Analysis.

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**General.** The pentode r-f voltage amplifier maybe either tuned or untuned. When untuned, the stray wiring and distributed circuit capacitance plus the tube capacitance to ground limit the high-frequency response, and hence the highest r-f frequency at which it can be used. On the other hand, the tuned r-f amplifier uses a parallel-resonant circuit to supply a high impedance across which the load voltage is developed. In this instance, the stray, distributed, and tube capacitances merely add to the value of tuning capacitance so that higher frequencies and greater amplification (as compared with the untuned stage) at these higher frequencies is obtained. Therefore, the tuned r-f amplifier is universally used, and the high gain of the pentode provides amplification not possible with a triode or untuned stage. The tuned r-f amplifier is further subdivided the narrow-band amplifier and the broad-band amplifier into two classes: Narrow-band amplifiers are used to amplify CW or voice- modulated signals (including broadcast signals), whereas broad-band amplifiers are used to amplify television, video, or pulse-modulated signals. Narrowband amplifiers accept a maximum of 5 to 10 kHz around the center frequency, whereas broad-band amplifiers cover the range of 5 to 10 MHz around the center frequency. Generally speaking, narrow-band amplifiers used the same types of pentode tubes used with resistance-coupled audio amplifiers, and broad-band amplifiers use the same type of pentode as is used with video amplifiers.

The tuned r-f amplifier may also be subdivided into two other classes: single-tuned and double-tuned. Since the double-tuned type is usually employed in tuned interstage amplifiers and cascaded stages, and these are the subjects of separate discussions later in this section, only single-tuned amplifiers are discussed here.

The use of the pentode, with its high transconductance and amplification factor, results in a high value of voltage amplification. In addition, the low grid-to-plate capacitance of the pentode reduces the tendency toward plate-to-grid feedback and selfoscillation. A lower effective tube input capacitance also increases the high-frequency limit of operation. By the use of coils with a high ratio of inductance to resistance (Hi-Q), the amplification provided by each stage of the tuned r-f amplifier can be made greater than of the amplification factor of the electron tube alone. Since the amplification of the r-f amplifier depends greatly upon the transconductance of the tube, it is also possible to vary the grid bias for the stage in accordance with signrd amplitude, and hence automatically control the gain.

**Circuit Operation. The accompanying** schematic shows a typical pentode signal-tuned r-f voltage amplifier circuit.



Pentode R-F Voltage Amplifier

In the schematic, T1 is an r-f transformer which matches the antenna to the control grid of the pentode. Tuning the secondary of TI with Cl permits a larger signal to be developed across the Hi-Q tuned circuit, and applied to the grid, than if no tuning at all were employed. Resistor RI and capacitor C2 form the conventional cathode bias resistor and bypass capacitor. (See the introduction to this section for a discussion of cathode bias.) Resistor R2 is the screen voltage-dropping resistor, and capacitor C3 is the screen bypass capacitor, which stabilizes the screen voltage and prevents it from being affected by the signal. The suppressor element of VI is grounded directly. In some circuits it is connected externally to the cathode; in certain types of tubes it is connected internally to the cathode. R-F transformer T2 acts as the plate load and couples the output to the next stage. The output winding is tuned by C4 to the desired r-f output frequency. While C4 could be placed across the primary of T2 and the secondary left untuned, the conventional approach is to tune the secondary. With proper disign the circuit is effective either way, and the secondary load is reflected into the plate circuit.

When a signal appears on the antenna, it is coupled through the primary of T1 to the tuned secondary (grid input) circuit. With capacitor Cl tuned to the frequency of the incoming signal, a relatively large r-f voltage is developed across the tuned circuit and applied to the grid of VI. The r-f signal, if unmodulated, consists of equal-amplitude positive and negative cycles occurring at the frequency to wish the circuit is tuned. For the moment, any fading or noise is considered negligible and the input signal is considered to be of constant amplitude. On the positive half-cycle the grid bias is decreased, causing a plate current increase. On the negative half-cycle the bias is increased, causing a plate current decrease. This changing plate current flowing through the primary of output transformer T2 induces an output in the tuned secondary winding. This operation is practically identical with that of the Transformer-Coupled Audio Voltage Amplifier previously discussed in this section.

For ease of discussion, the signal is considered to be a sine wave with equal-amplitude positive and negative r-f swings. The average plate current flow, therefore, will be constant, and cathode bias may be employed. It is important to note that the r-f amplifier operating as the first stage in the receiver is

usually a small-signal amplifier. That is, the input voltage is on the order of microvolt, except in strong-signal areas; Therefore, a small signal voltage change causes only a very small bias change, and it is necessary to employ high-transconductance electron tubes to produce effective amplification. The pentode tube is well suited for this purpose, since it has both a high amplification factor and a high transconductance. By using a large value of inductance and a small tuning capacitance for the frequency involved, and also as small a coil resistance as is practicable, the tuning circuit exhibits a Hi-Q. Thus, its effective impedance is much larger than that presented by a tuning tank of low Q. Hence, a large input voltage is developed between grid and ground across the tuned circuit. With a step-up turns ratio from transformer primary to secondary, if closely coupled, a still larger input voltage is produced. The step-up of voltage in the transformer and the Hi-Q tuned grid tank increase the small input voltage before it is applied to the tube for further amplification. Normally, Class A bias is used to produce linear swings and to minimize distortion. With very small input signals however, operation occurs over the curved portion of the plate-current grid-voltage characteristic. For example, typical bias values range from 0.5 to 1 or 2 volts maximum. Thus, the tube is clearly operating very close to zero bias, and the  $E_g$ - $I_p$  curve in this region is never straight. This results in uneven positive and negative swings, and this produces distortion. For r-f stages, a larger bias and a more linear portion of the curve are used.

When the input signal is modulated, each r-f cycle may be of different amplitude; thus, considering each cycle to be amplified linearly, the modulation is likewise amplified proportionately producing an over-all modulation envelop which is almost identical with that of the original modulation. A light difference (usually a reduction in modulation factor) exists; this is produced by distortion, which will be discussed in more detail Failure Analysis.

When small values of bias are used in the input stage and large signals are applied, distortion occurs because the signal is partially clipped off in the plate circuit. In addition, grid current flow creates a lowresistance (shunt) path between the grid and the cathode, which effectively lowers the grid tank Q. As a result, the input signal and over-all amplification of the stage are reduced. Therefore, it is common practice to employ a variable cathode resistor for manual gain control, or to provide some means of automatic bias (gain) control. For a complete discussion of AGC circuits, refer to the Special Circuits Section of this Handbook.

# Failure Analysis

No Output. Loss of plate, screen, or filament voltage, or a defective tube, can cause no output. The voltages can be checked with a voltmeter, and a open filament can sometimes be observed by noting that the tube is not illuminated and feels cold to the touch. If the plate, screen, and filament voltages are normal, the tube may be defective. If the tube checks good, check the input transformer by applying a modulated voltage from a signal generator to the input terminal and observe whether there is an input voltage on the grid (use a VTVM or an oscilloscope and r-f probe as the indicator). An open screen resistor (R2) will be indicated by the lack of screen voltage. Similarly a shorted screen capacitor (C3) will drop the screen voltage to zero and cause R2 to heat abnormally. The short circuit condition may be observed visually by smoke from or discoloration of the resistor. An open or shorted cathode bypass capacitor (C2) will not necessarily produce a no-output indication; however, an open bias resistor (Rl) usually will. In fact, on very small signals either trouble may not be obvious or may show only as a slight increase in distortion. If tuning capacitor Cl or C4 is defective, depending on whether it is short-circuited or @pen-circuited, there may be no output or a considerable reduced output, respectively. Since each capacitor is shunted by a coil, it will be necessary to disconnect one end to check for capacitance or a short. Where an open coil is suspected, it can be checked for continuity with an ohmmeter.

**Reduced Output.** When there is an open circuit in either transformer TI or T2, if sufficient capacitive coupling exists between the windings (especially at the higher frequencies), the output will be reduced, rather than nonexistent. On the other hand, at the lower r-f frequencies the output may be reduced practically to zero. A check with an ohmmeter will determine whether there is continuity in the coils. A change in the value of screen resistor R2 to a higher value will lower the screen voltage and reduce the output. Likewise, a reduced plate voltage caused by a high-resistance joint or winding will lower the output. Low output can also be caused by a defective tube, that is, a tube with low filament emission or an in-

ternal short. If the tube has an internal short, it will draw a heavy cathode current, thus producing a much greater than normal bias and reducing the output accordingly. A defective antenna or transmission line can cause a weak input signal and an apparent lack of output. In this instance the circuit will check normal in every respect, and changing tubes will make no difference. Substitute another signal from a different antenna, if possible, or apply an input from a signal generator with a calibrated attenuator. If a large value of attenuation is required to reduce the output signal to a low value or zero, the stage is operative and the trouble is external.

Distorted Output. Improper plate or screen voltage will cause a certain amount of distortion. While improper bias will also cause distortion, it will depend to a great extent on the tube used, the input signal amplitude,. and the value of bias. Intermodulation between the side (modulation) frequencies of a modulated input signal will create a slight amount of distortion due to the curvature of the tube  $E_g - I_p$  characteristic. Normally, special test equipment is required to determine this condition; besides, it is of little consequence except to the designer. Likewise, a change in the modulation factor is caused by the fact that the individual modulated r-f cycles are of different amplitudes. Thus, the larger signals are amplified more than the smaller signals because of the curvature of the tube characteristic; this is also a design problem. Hum distortion may occur because of induced hum on the carrier at low signal levels. This is normally minimized by proper filament bypassing and plate supply filterring, together with screen bypassing. There should be no hum distortion in the equipment as originally supplied, except where the falters or bypass components are defective. The use of an oscilloscope will show where the hum appears and usually localize the source.

Curvature of the tube characteristic can also cause distortion which appears in the form of intermodulation between two strong applied r-f voltages, one of which may be outside the range of the tuning circuit; when sufficient to be annoying in the reception of the desired signal it can be eliminated only by attenuating the undesired frequency. Intermodulation distortion is recognized by the fact that the distortion occurs to the modulation frequencies of signals which are normally loud and clear. It should not be confused with selective fading, which also causes frequency distortion in AM reception.

Another prevalent from of distortion which occurs when two strong modulated signals are nearby is cross modulation. This actually causes modulation of the carrier of the desired signal by that of the undesired signal. Cross modulation is recognized as a form of "monkey chatter" heard in the background of broadcast stations, particularly where strong adjacentchannel signals are present. It it also recognized in voice communication by the clear, undistorted, but weak reception of the undesired station superimposed on the desired station. In the pause between syllables and words, the cross-modulating station can be heard clearly. The interfering signal may not be within the tuning range of the receiver used, although usually it is. Here again, the fault is due to curvature of the tube characteristic, and is eliminated by attenuation of the unwanted signal, either by selectivity or some other means. While usually a design problem, these types of distortion are mentioned here because it is possible in certain instances that design specifications may be overridden by circumstances beyond the control of the technician, such as when the ship is temporarily located close to another station. In this event, needless time might be sent looking for trouble within the circuit.

If too great a selectivity is employed, the sidebands will be partially clipped from a modulated signal, resulting in a form of frequency distortion. This can result from an incorrect setting of a selectivity control or from regeneration within the stage, which will produce sharper tuning. Regeneration can be produced by operating with two low a screen voltage or insufficient screen bypassing, and by improper leaddress when components in the grid or plate circuit are replaced. "

# CASCADE R-F AMPLIFIER (ELECTRON TUBE)

The cascade r-f amplifier is generally used in tuned radio frequency receivers to supply high gain and selectivity before detection.

#### Characteristics.

Uses a number of stages connected in cascade.

Operates Class A for linear amplification.

Usually operated self-biased, rdthough fixed bias may be used.

Uses a single tuned stage in the grid circuit of each tube, for selectivity.

Uses pentode tubes for high gain, although any tube type may be used.

## Circuit Analysis.

General. The cascade r-f amplifier is a conventional amplifier whose output is connected to the input of a similar stage, which, in turn, is connected to another similar stage. Thus, the outputs are cascaded from one stage to the other, and a number of similar stages are used to provide high amplification. Usually three tuned stages are used, and the amplification varies as the cube of the single stage gain (a gain of 10 per stage produces a total gain of 1000). While it is not necessary that the stage be tuned (untuned stages may also be cascaded), a higher gain is obtained from the tuned stage than from the untuned stage. Hence, the untuned r-f amplifier is generally used only for special, wide-band applications. Likewise, it is apparent that either triodes or pentodes may be employed. However, with triodes less over-all gain is obtained and the high grid-to-plate interelectrode tube capacitance produces inherent instability. Thus, to avoid the problem of neutralization and to achieve high gain per stage, the pentode tube is usually employed.

**Circuit Operation. The schematic** of a typical cascade r-f amplifier is ifhrstrated in the accompanying figure.

Three stages of r-f amplification are provided, using transformer coupling for convenience. While all stages are basically identical, the component values are not always the same. Usually the bias, plate, and


Typical Cascade Three-Stage R-F Amplifier

screen voltages are different in the various stages, or at least they differ between the first and the remaining stages. Since each stage handles the output of the preceding stage, the bias is usually the smallest on the first stage and the largest on the last stage; the large bias on the last stage is necessary for this stage to handle the large output voltage swings developed in the first and second stages. Since the first stage plate swing is the smallest, it can operate with a lower plate voltage and thus produce less "shot noise", to provide a better signal-to-noise ratio without loss of gain. The final stage, of course, has the largest plate voltage. The screen voltage is usually the same for all stages, except perhaps the first stage.

In the schematic, T1, T2, T3, and T4 are tuned radio frequency transformers. T1 is the input transformer, and T4 is the output transformer; T2 and T3 are interstage transformers. The primaries of the r-f transformers are untuned, while the secondaries are tuned by variable capacitors. Although not shown in the schematic, these tuning capacitors are mechanical ganged together for single-knob tuning; otherwise, each of the tuning capacitors would have to be tuned separately for maximum response when a different

frequency is selected. The use of a parallel-tuned circuit provides a high impedance at the grids of V1, V2, and V3, thus producing high gain and good selectivity. Resistors R2, R5, and R8 are screen voltagedropping and decoupling resistors, which are bypassed to ground for rf by screen bypass capacitors C3, C7, and C1O, respectively. Resistors R3, R6, and R9 are plate voltage-dropping and decoupling resistors for tubes VI, V2, and V3, respectively, and are bypassed by capacitors C5, C9, and C12. Cathode (self) bias is supplied by resistors R1, R4, and R7 for VI, V2, and V3, respectively. The cathode bias resistors are bypassed by capacitors C2, C6, and Cl 1. (See the introduction to this section for a discussion of cathode bias.) Capacitor Cl 3 is a large filter capacitor used to minimize hum components in the supply source and possible impedance coupling effects due to the use of a common supply. The input may be from an antenna or other source, and the output can be applied to other r-f stages or to a detector.

When a signal is applied to the primary of the input transformer, signal current variations through L1 produces a varying magnetic field which induces a voltage in secondary L2 by transformer action. When

tuned to resonance by Cl, a large voltage is developed between the grid of VI and ground, across the tuned circuit, and the turns ratio between L1 and L2 determines the impedance presented by the input to the V1 grid. In the case of an antenna input, a step-up turns ratio matches the low antenna impedance to the high impedance of the parallel-tuned circuit, for efficient power transfer. Assume for the moment that the r-f signal is increasing in a positive direction. The instantaneous positive grid swing produces a large instantaneous current flow in the plate circuit. This plate current flowing through the impedance presented by primary coil L3 produces a voltage drop across the T2 primary, and the changing value of plate current also induces a voltage into secondary L4. When L4 is tuned by C4 to the same frequency as the input signal, a large voltage is also developed across this tuned circuit and is applied to the grid of V2. Stage V2 operates in a similar manner and supplies an output to stage V3, which further amplifies the signal and produces a final negative output from T4. (An even number of stages would produce an output of the same phase or polarity as the input.)

When the input signal decreases, the plate current through V1 is reduced, and the reduction in current flow through L3 induces a smaller input voltage in V2, and likewise in V3, with a resultant smaller total output. With each tube operating Class "A", equal positive and negative input signals produce amplified output signals of the same shape, but of larger amplitude and opposite phase. Cathode resistor R1 is variable to provide manual control of the first stage bias, and allow adjustment to prevent strong input signals from driving the tube to saturation and producing distortion.

As can be seen from the above explanation, operation of the cascade r-f amplifier is similar to that of any other pentode r-f amplifier (discussed previously in this section), but with each stage designed to handle the full output of the preceding stage. The cascade r-f amplifier is the counterpart of the tuned interstage (i-f) amplifier, discussed later in this section. It differs principally in the fact that it operates at a higher frequency, is continuously tunable over a large range of frequencies, and has somewhat less selectivity because only single-tuned circuits are used, with slightly less gain (depending upon the operating frequencies and number of stage employed). While simple transformer-coupled stages are shown and discussed, it is possible to use capacitively coupled stages, or other bandpass arrangements.

The suppressor grid is shown grounded in the schematic to minimize plate-to-grid coupling through the interelectrode tube capacitance, and to provide better shielding between 'he input and output; thus, at high radio frequencies, the possibility of oscillation due to regeneration is rather remote, so that no neutralizing arrangement is necessary. At the lower radio frequencies, the suppressor may be connected to the cathode without causing undesirable effects, since the r-f feedback is less.

# Failure Analysis.

**General.** The failure analysis for each stage of the cascade r-f amplifier is essentially the same as that for the single-stage pentode r-f amplifier discussed previously. In fact, the first-stage components of the cascade amplifier and the components of the single-stage amplifier are identically symbolized, except that the plate decoupling filter (R3 and C5) was not included in the single-stage amplifier. Therefore, this failure analysis will be confined to generalities concerning multistage circuits.

No Output. Any trouble which produces a nooutput condition in a single stage will result in either a similar condition or a considerably reduced output in the multistage circuit. Because of the high gain and the possibility of signal feed-through to a following stage by stray capacitive effects at radio frequencies, it is possible for a single stage to be inoperative and still have a substantial output from cascaded stages. In this special case, the loss in amplification can be observed by inserting an input from a signal generator and noting the output. Then, by successively applying the signal to the following stage inputs (grids) again observing the output produced by the signal generator, it will be noted that the output suddenly increases when the defective stage is passed. Ordinarily, the output would decrease from stage to stage, requiring a constantly increased signal generator output as each stage is passed. If plate decoupling filter R3, C5, or R6, C9, or R9, C12 fails (either the resistor opens or the capacitor shorts), the plate voltage of the affected stage will be zero and no output will be obtained (neglecting the possibility of stray coupling).

Check the plate, screen, and cathode voltages to ground with a voltmeter; any abnormal voltage will — localize the trouble to a specific stage and to the parts

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associated with that tube element. Be certain to check the supply voltage also; there may be a defect in the power supply. With normal voltages and no output, either an r-f transformer or a tube is defective.

Low Ouput. High bias, low plate or screen voltage, and a defective r-f transformer or tube can cause the output to be low. First check the plate, screen, and cathode voltages of each tube to verify that the dc bias and operating conditions are normal. Connect an output indictor to the output terminals, and insert a strong signal (within the tuning range) from a signal generator to the grids of V3, V2, and VI, respectively, (use a dc blocking capacitor in series with the generator output). As the generator is moved from stage to stage, adding additional amplification, it should be necessary to decrease the generator output to maintain a constant output indication; otherwise, a lack of gain is indicated. If an oscilloscope and an r-f probe are available, the signal generator can be left connected to the input, and the signal traced from the grid to the plate of each stage with the r-f probe. With the generator set to a specific frequency, tune the tank capacitors about this frequency. An increase in amplitude should be obtained as the signal is peaked; if an increase is not obtained, the tuned circuits are probably defective. Since the screens and cathodes are grounded (for rf) through bypass capacitors, no signal will be observed at the screen or cathode unless one of these capacitors is inoperative. Remember that placing the r-f probe across a circuit adds the probe capacitance, and will cause detuning of the circuit at radio frequencies. Best results are obtained when the signal or output is inserted in the circuit immediately ahead, or taken immediately after the point to be checked. For example, if the output of the first stage is to be checked, the input should be applied to the grid of V1 and the output measured across the T2 secondary. If she signal is applied to the plate of V1 instead, and measured at T2, the loading effects of the signal generator will affect the tuning of T2 and, therefore, the V2 gain. By inserting the signal at the plate of V2, only r-f transformer T2 will be checked, whereas by inserting the signal at the grid of V2, both the amplification of V2 and the operation of T2 will be checked. Loss of gain due to aging of tubes over a long period of time can occur in multistage (cascaded) r-f amplifiers, and may not be apparent until the reduction is severe. In this case all indications and voltages appear normal, except that

the equipment does not seem to be performing satisfactorily and most signals are weak. Where maintenance standards are provided for the equipment, a simple comparison will reveal the deficiency. It should be kept in mind that each stage should produce additional gain; therefore, any stage showing no gain is probably defective.

**Distortion or Poor Selectivity. Low** bias or plate voltage will cause distortion, as will low screen voltage. Since the screen voltage **fixes** the range of plate swing, it has more effect in producing distortion than a similar change in plate voltage. Driving the plate voltage below the screen voltage will produce distortion, and in some instances cause a negative resistance condition resulting in unwanted self-oscillation. In multistage amplifiers, the possibility of cross-modulation and intermodulation distortion exists to a greater extent than in single stages; however, the causes are the same.

In tuned radio frequency amplifiers a strong signal tends to block the amplifier and broaden the response curve, so that cross modulation effects are not as noticeable. By adjustment of the manual gain control, the effective amplification can be reduced to prevent overloading on strong signals; thus, the nonlinearity introduced is avoided, and any cross modulation and intermodulation distortion are minimized. Poor tracking of ganged tuning capacitors can also produce either a loss of gain or distortion by cutting off frequencies outside the pass band of the individual stage. However, single-tuned r-f stages are usually so broad in tuning that slight differences (in bandpass or resonance) merely broaden the over-all response curve, so that only poor selectivity results. Proper adjustment of timmer and padding capacitors will restore the initial selectivity, but cannot compensate for poor design.

# CASCODE R-F AMPLIFIER (ELECTRON TUBE)

#### Application.

The cascode r-f amplifier is employed as a highgain, low-noise r-f input stage to high-frequency receivers.

#### Characteristics.

Two triodes provide the equivalent maximum gain of a pentode with reduced noise.

Noise equivalent is equal to that of a single triode stage.

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Grounded-grid stage stabilizes the circuit so that neutralization is not normally required.

Uses Class A self-bias, although-fixed bias can be used.

# Circuit Analysis.

**General.** The cascode circuit consists of a single, conventional grounded-cathode input amplifier, connected in series with a grounded-grid amplifier stage which contains the output load. In most instances the two tubes are triodes, although they could be triode-connected pentodes or a combination of pentode

input and triode output. To obtain the low-noise feature, the triode output must be used. This circuit, like the grounded-grid circuit discussed previously, is usually employed at frequencies where the effective amplification of pentode and beam power tubes drops off as a result of high-frequency effects. It is seldom used at frequencies lower than 30 MHz, since equivalent or better performance can be obtained with careful design by using a single pentode tube.

**Circuit Operation.** The accompanying schematic illustrates a typical triode cascode r-f amplifier circuit.



Typical Cascode R-F Amplifier

In the schematic, Cl is a coupling capacitor tapped on the lower end of tank coil L1. It is made variable to provide a slight amount of input tuning. Input tank circuit L1, C2 is coupled through capacitor C3 to the grid of V1. The low reactance of C3 to the r-f signal allows maximum signal (developed across the tank) to appear on the V1 grid and prevents the dc shunting of the grid signal to ground through L1. Cathode bias is provided by R2 bypassed for rf by C7, and R1 is the grid-return resistor. Tube VI is connected as a conventional grounded-cathode amplifier, with V2 acting as the plate load impedance. Inductor L2 helps match the low input impedance of grounded-grid stage V2. The grid of V2 is returned to the cathode by R3, which develops contact bias, and is grounded for rf by C4. The plate load of V2 consists of the parallel-tuned tank, L3, C5, with output winding LA inductively coupled to it. Resistor R4 is a plate decoupling and voltage dropping resistor, bypassed by C6. This series-feed plate arrangement allows the rotor of C5 to be grounded to avoid body capacitance effects when tuning.

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# **SRAIFILERS**

.bəqoləvəb decreases, an output voltage of opposite polarity is

are effectively connected in parallel. cathode and the other is grounded-grid, their grids the other tube. Although one stage is groundedresistance of one tube acts as a dropping resistor for are fed their plate voltage in series, so that the plate operates in exactly the opposite manner. Both tubes grid connected effectively in series. The cascode stage tier operates in parallel with the supply, and with its across the plate supply. The normal cascaded amplithese amplitiers operate when connected in series it is now necessary to examine the manner in which tion. To complete the discussion of circuit operation without considering the effects of combined operation of the separate stages of the cascode amplifier The discussion above covers the individual opera-

.IV dguordt tysoxs ground or between the cathode and grounded of V2 there is no de connection between the grid and the dc representation of the circuit. It is clear that The simplified equivalent schematic below shows

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Simplified Equivalent Cascade R-F Amp. Circuit

loading are explained in the detailed functioning of tupical). This action and the effect of circuit duction, the circuit is prevented from oscillating the amplitied output signal. In addition to noise retube. So that a large reduction in tube noise occurs in one quarter of that produced by a single high-gain would be with one tube. The noise, however, is only

former action. Similarly, when the plate current voltage is induced in coupling coil L4 through transage drop appears across tank coil L3, and an output tubes. When the plate current of V2 increases, a voltconnected, and the same current flows through both This is necessary since both VI and V2 are seriesdoes the current of V2 (both in the same direction). direction. That is, as the current of V1 increases, so grid stage are in phase, both tubes operate in the same of V2. Since the input and output of the groundedgrid signal, and causes an increase in the plate current versely, a negative cathode signal appears as a positive causes a decrease in the plate current of V2. Con-V2 appears as a negative signal on the grid of V2, and the grid. Thus, a positive output on the cathode of in effect appears as an oppositely polarized signal on cathode of V2, and, since the grid of V2 is grounded, pearing on the plate of VI also appears on the Because V2 is direct-coupled to V1, any signal ap-L2 also helps match the V2 grid to the V1 plate. increased by the series reactance added by L2. Thus, stage, also shunts the output of VI to ground, but is V2. The input resistance of V2, the grounded-grid series is effectively paralleled with the plate load of series with VI, the plate resistance of both tubes in presented to the V2 plate. Since V2 is connected in L4 affects C5 tuning and the value to total impedance In addition, the reflected load from output winding consists of V2 and its associated tank circuit, L3, C5. which is the output. However, the plate load for VI through the load produces a varying voltage drop ventional amplifier, this change in plate current a decreased plate current flows. Normally, in the connegative, the bias on VI is momentarily increased and vent self-oscillation of VI. When the input signal goes plate-grid interelectrode capacitance, and helps prethe voltage fed back from plate to grid through the rent develops a small emf, which is out-of-phase with momentarily flows. In flowing through L2 the curmentarily decreased and an increased plate current again going positive. The bias on the VI grid is mosi langis tuqui off that thomom off rol omuseA portions of the circuit as discussed below.

## **AMPLIFIERS**

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#### ELECTRON 12 CIRCUITS

the input, the grid of VI is isolated from the input and blocking capacitor C3. Since C3 is in series with cuit, and is applied to the VI grid through coupling appears as an r-f voltage across the tuned input cirtween the antenna and the tank. The input signal tank. Thus maximum power transfer is obtained bevalue of parallel impedance offered by the tuned to step the low antenna impedance up to the large on tuning coil L1, autotransformer action is obtained tuned tank consisting of L1, C2. By tapping C1 down an input signal appears on CI, it is coupled into the of the input signal is shunted to ground. Thus, when operation. The value of R1 is large enough that none cannot accumulate, bias-off the tube, and block returned to ground through RI so that electrons current transfer characteristic curve. The grid of VI is

circuit as far as de is concerned, but is connected for

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phase with the input signal is produced. ing connected in-phase, an output voltage that is in output by secondary coil L4. With the output windflow in L3, C5 which is inductively coupled to the the drop across the plate tank develops a tank current V2 grid. Thus the plate current of V2 also rises and ettect is as though a positive voltage were applied to since the grid of V2 is held at ground potential the V2) drives the cathode of V2 more negative, and increased plate current flow through L2 (and tube effect on R2 since it is bypassed by C7. However, the The instantaneous increase of cathode current has no and causes the cathode and plate current to increase. a positive direction, the grid bias on VI is decreased of VI. Assuming that the input signal is increasing in age across R1, which, in turn, is applied to the grid provides an increased signal to C3 and develops a voltthrough C1 to the tank L1, C2, which at resonance When an input signal is applied, it is coupled

Conversely, when the input signal to VI is operating over the negative half-cycle, the bias on VI is increased by the input signal, and plate current flow in VI is reduced. The reducing plate current apply value, driving the direct-coupled cathode of W2 in a positive direction. When V2 cathode becomes more positive, the plate current of V2 is reduced, while the plate voltage rises and induces an increasing voltage in the tank. When connected in-phase the tank wills the plate voltage tises and induces an increasing while the plate voltage tises and induces an increasing voltage in the tank. When connected in-phase the tank while the plate voltage is only half of what it normally it connected in series, when output voltage is only half of what it normally the output voltage is only half of what it normally the output voltage is only half of what it normally the output voltage is only half of what it normally the output voltage is only half of what it normally the output voltage is only half of what it normally the output voltage is only half of what it normally

> hence, there is no final output at T4. variations of plate current which produce noise); from any of the stages (except for slight thermal voltage. With no signal applied, there is no output Thus, any r-f variations cannot change the dc plate only direct current flows through the plate resistor. tent or (ereaging a signal appears) so that Capacitor C5, C9, or C12 bypasses any r-f current ducing the effective plate voltage to the desired value. polarity which opposes the supply voltage, thus re-R3, R6, or R9, it produces a voltage drop with a output. However, in flowing through plate resistor primary L3, L5, or L7 is steady and this produces no value of plate current flowing through transformer can flow through the screen resistor. The quiescent ground (when a signal appears), so only de current C7, or C10 bypasses the r-f current variations to age to the desired value. Screen bypass capacitor C3, the source voltage, and thus reduces the screen voltduces a voltage drop with a polarity which opposes screen current flow through the screen resistor prodrop developed across the cathode resistor. Similarly, which biases the grid negative because of the voltage (also including grid current, if allowed to flow), tube, including both the screen and plate current cathode current is the total space current through the resistor R3, R6, or R9, back to the supply. The plate, through primary coil L3, L5, or L7 and plate R4, or R7, through the grid and the screen to the current. Electron flow is from ground through R1, drawing its static value of screen, plate, and cathode In the absence of a signal, each tube is resting and

over the linear portion of its grid-voltage, plateflows at all times (Class A), and so that V1 operates cathode bias.) Bias is selected so that plate current introduction to this section for a discussion of bias because R2 is bypassed for 11 by C7. (See the through it. Signal current variations do not affect the since the total currents of VI and V2 flow is series cathode bias of VI. Cathode bias is supplied by R2, voltage of V1 is half that applied to V2 less the equal plate currents and plate resistances, the plate acts simply as a dropping resistor. Thus, assuming plate voltage for VI is obtained through V2, which the plate directly connected to the next stage. The plifier using cathode bias and shunt grid feed, with bined. VI represents a conventional triode r-f amrately, and then operation of the two tubes comderstood it operation of each tube is considered sepa-Operation of the cascode circuit can be better un-

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With no signal applied, the tubes are resting in a quiescent condition, with the same plate current flowing through both VI and V2. The plate voltage of V1 is determined by the drop across V2 and R4, and is further reduced by the amount of cathode bias developed across R2. As the VI plate voltage increases (with a signal), the V2 plate voltage decreases, since the total supply voltage does not change. The V1 grid voltage is the cathode voltage drop produced by the total cathode current times cathode resistance R2, plus any signal-excitation voltage. With a practically constant cathode current, this bias voltage changes very little. When the plate current through V1 decreases (because of a negative-swinging input signal), the plate voltage of VI increases; at the same time the V2 grid voltages increases, since the plate voltage increase of V1 is applied directly to the cathode of V2. Thus, the current through V2 is caused to decrease also to correspond with that of VI. Any increase or decrease in plate current through V1 and V2 (caused by the input signal) produces a corresponding increase or decrease in output voltage across load resistance R4. This load resistance is the impedance offered by the tuned tank at the frequency of the input signal. The result is to provide a relatively constant amplification through VI and V2, equivalent to that of a single triode tube operated with a reduced plate voltage.

Although maximum gain is obtained, since it is produced at a relatively low plate voltage with a minimum change in plate current, less noise is produced than for an equivalent gain obtained with a large change in plate current. The isolation provided between the input and output circuits by grounded-grid stage V2 minimizes any feedback between the input and output. Therefore, self-oscillation is prevented and neutralization is unnecessary. (Although in some circuit versions V1 is neutralized, this is not done to prevent oscillation, but rather to increase the input admittance so that high gain may be obtained.) by maintaining a relatively constant plate current, the circuit produces a very linear output signal, because the gain is independent of plate resistance and equal to the tube amplification factor at all times. Thus, the normal dropping off in effective amplification at high radio frequencies is overcome by the cascode circuit. The decrease in noise output and the increased gain at high frequencies make this circuit most useful, and provide a much better signal-to-noise ratio than any other circuit combination.

The reason for the decreased noise is not the reduction in shot-effect alone (random variations in the rate of electron emission from the cathode produce a hissing noise called *shut effect*), because of the low plate voltage used. The decreased noise is also due to a reduction in the "induced grid noise" and the "flicker effect". The induced noise is reduced because of the low effect impedance of the grounded-grid circuit. The flicker effect, which occurs because of small temperature changes in oxide-coated cathodes, is reduced by holding the plate current relatively constant. Thus, the space charge within the tube remains relatively large and constant, and any increase caused by flicker effect is swamped out, since any increase in the negative space charge returns the stray electrons to the cathode rather than to the plate.

The combination of a cascaded grounded-cathode and grounded-grid stage is also often used and referred to as a cascode amplifier. This change in circuit is accomplished by adding plate voltage dropping resistor R<sub>x</sub>, shown in dotted lines in the previous schematic. This circuit is not two series stages with a common plate voltage ;,,.it is simply two separate circuits connected in cascade. Although constant gain is not achieved by keeping the plate current in V2 relatively constant, almost identical results are obtained. In fact, the cascaded form of cascode circuit provides additional gain, since each stage operates separately as an amplifier. However, the flicker effect is not eliminated, and as each stage usually operates at a slightly higher plate voltage than each stage in the original cascode circuit, slightly more shot noise is produced. Because of the increased signal gain, however, the increase in the noise figure is not very evident, since the signal tends to override the noise.

#### Failure Analysis.

**General.** The failure analysis applicable to the grounded-cathode r-f amplifier and the grounded-grid r-f amplifier may be used as a guide, particularly where the cascaded form of cascode circuit is used. Since the tubes normally have their plates series-connected, the following analysis applies only to the orginal cascode circuit.

No **Output.** In the series plate circuit consisting of R4, L3, V2, L2, V1, and R2, any open circuit will prevent operation and thus cause loss of output. Normal plate and cathode voltages will indicate either no signal applied, a defective tube, or an open input or output circuit. Always check the supply voltage

when checking plate and bias voltages, to verify that the supply is operating normally. If the input circuit is defective, placing the antenna (or other input) directly on the grid of VI should produce an output. A resistance check of L4 will verify continuity, but not necessarily indicate a short circuit since the coil resistance is usually less than 1 ohm in either case. With an oscilloscope and r-f probe, the signal can be checked at the plates of both tubes; if the signal is present, L4 is defective. If R3 opens, the grid of V2 can become blocked by the accumulation of electrons on C4. A resistance check will indicate whether R3 is of the proper value. If either Cl or C3 is open, no signal will be applied to the V1 grid. Use an in-circuit capacitor checker or temporarily add a capacitor equivalent in value to Cl or C3 to determine whether an output can be obtained. If the tubes are suspected, check them in a tube checker. A no-voltage indication on the plate of V2 can be caused by a shorted bypass capacitor C6. If C6 is shorted, the entire plate supply will be dissipated across R4, causing it to overheat, smoke, and possibly burn out.

Low Output. Low plate voltage, high grid bias, or a defective tube will produce a reduced output. The plate and bias voltages can be checked with a voltmeter. If C7 is open, the output will be reduced because of cathode degeneration. Likewise, if either C2 or C5 is detuned or open, the output will be reduced. If Cl or C3 is defective but stray capacitive coupling exists, low output may also be obtained. Use an in-circuit capacitance checker to check the capacitors. If grid return resistor R1 or R3 is open or increases in value with age, it is possible for the associated tube to block or have reduced output after a strong signal. Use an ohmmeter to check the values of RI and R3 when in doubt. Since the output is an r-f signal, L4 can be open and yet a low output be obtained through stray capacitive coupling.

Distortion or Poor Selectively. The cascode amplifier is subject to the same causes of distortion and poor selectivity as other types of r-f amplifiers. Low bias or plate voltage will cause clipping and distortion. Use a voltmeter to deterr-rine whether the proper bias and plate voltages are present. High resistance in the tuned circuits, caused by poorly soldered joints, will cause board tuning and poor selectively. Such joints in the antenna or transmission line system can cause rectification of the r-f signal and produce spurious responses or beats which might be misinterpreted as distortion. Changing the antenna will usu-

ally cause this condition to disappear. When in doubt, insert a modulated signal from a signal generator tuned within the range of operation. Use an oscilloscope and r-f probe to follow the signal from input to output. Any distortion will be visible as a change in pattern on the scope. Any cross-modulation effects will be due to overloading by strong local signal, and can be eliminated only by attenuating the signals or by inserting circuits that provide additional selectivity before the input.

# **TUNED INTERSTAGE (I-F) AMPLIFIER** (ELECTRON TUBE)

#### Application.

The tuned interstage (i-f,) amplifier is universally used in superheterodyne receivers to supply high r-f amplification and the desired selectivity.

#### Characteristics.

Uses pentode-type electron tubes to obtain high voltage gain.

Uses double-tuned tank circuits to obtain sharp selectively.

Uses radio-frequency transformers to isolate input and output circuits, for voltage step-up and impedance matching.

Operates Class A, self-biased to minimize distortion, although fixed bias can also be used if desired.

Uses a number of similar stages connected in cascade to obtain greater gain and selectivity.

Employs fixed tuning, adjustable over a narrow range, for exact alignment of each stage.

# Circuit Analysis.

General. The tuned i-f amplifier may consist of a single stage, or as many as six or more cascaded similar stages to obtain the desired amplification and selectivity. Generally speaking, one to two stages are used for radio broadcast reception, while two to four stages are used in selective communications receivers, and six or more stages are used for radar, television and microwave reception. The intermediate frequency chosen usually determines the number of stages. The lower frequencies, such as 50, 175, and 250 kHz, produce more amplification and better selectivity than 450 kHz; at 21 or 44 MHz (as in TV applications) or at 30 or 60 MHz (as in radar applications), less gain per stage is obtained, and the response curves are broader, so that more stages are

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Two-Stage 1-1-1 Schematic

Further examination of the schematic also reveals that the stages are simple pentode r-f voltage amplifiers. Self-bias for the stages is provided by cathode resistors RI and R4, bypassed for rf by C3 and C8, voltage-dropping resistors R2 and R5, while plate voltage is supplied through R3 and R6. The screen resistors are bypassed to ground for rf by C4 and C9, and the plate resistors are bypassed by C5 and C12, which also form a decoupling network.

·pəsn əq cycle (with or without signal), and cathode bias can steady plate and screen currents flow throughout the tent oz betenimile ere (beilqqs zi lengiz e nehw) bypassed to ground, any r-f variations of plate current proper operating value. Since each of these resistors is resistors R3 and R6 drop the plate voltage to the provide sufficient plate current swing. Likewise, plate voltage to the value of screen voltage necessary to bias.) Screen resistors R2 and R5 drop the supply duction to this section for a discussion of cathode the same as a negative bias on the grid. (See the introand develop a positive bias at the cathode, which is flow steadily through cathode resistors R1 and R4, in their quiescent condition. Plate and screen currents With no signal applied, both VI and V2 are resting

When an input signal is applied to T1 primary, a high impedance is offered the signal at the resonant frequency to which C1 tunes L1. With secondary L2 tuned to the same frequency by C2, a high impedance

suoitel the transformers, this is taken care of in design calcuplate-to-ground capacitance, plus internal leakage in some shunting effects due to grid-to-ground and the highest impedance at resonance. While there are at the trequency to which it is tuned, since it presents that the largest voltage is developed across either tank primary and secondary is optimum. It is also evident age transfer, provided that the coupling between the always provides sufficient matching for efficient voltmum. Thus, it is seen that double-tuning in itself oped on the grid, and grid losses are kept to a minitube grid circuit so that maximum voltage is develondary presents a high impedance to the following induced in the secondary. At the same time, the secprimary, and by transformer action a large voltage is circuit tank causes a large voltage drop across the nected. The high impedance produced by the plate impedance to the circuits in which they are conparallel-tuned circuits and they both present a high and secondary of each i-f transformer are high-Q, usually of academic interest only, since the primary tween the plates and grids of the cascaded stages is ratio is used, and any difference in impedance bethe turns ratio in the transformers. Normally, a 1-to-1 ondary circuits can be accommodated by changing change in impedance between the primary and secusually supplies the i-f signal to the detector. Any of the preceding mixer or converter stage, while T3 Transformer T1 couples the grid of V1 to the plate

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# **ELECTRONIC CIRCUITS**

#### **SRAIFILFIERS**

bandpass, as compared with synchronous tuning (each tank tuned to the same frequency), assuming optimum coupling between the i-f primary and secondary coils, is shown in the accompanying illustration.



Stagger-Tuning and Synchronous-Tuning Response Curves

**Circuit Operation.** The schematic of a typical two-stage i-f amplifiet is shown in the accompanying illustration. The dashed line divides the circuit into two separate stages. Note that in the inter-stage amplifier T2 is common to both stages. Thus, T2 matches and couples the output of V1 to the input of V2 for efficient signal transfer. Since the stages are operating Class A, no grid current flows and power transfer is not a real concern; however, maximum voltage transfer is important.

> needed. In addition, the bandpass requirement introduces another factor, since a simple 5 to 10 kHz bandpass can be obtained with a few tuned circuits, whereas a broad bandpass of 4 to 5 MHz, with sharp cutoff, which is required in TV and radar receivers, requires a number of stagger-tuned stages. The bandpass is measured at the half-power points of the receiver response curve, that is, at 70.7 percent amplitude each side of the i-f center frequency. For example, if we have an i-f amplifier output of 100 volts of the center intermediate frequency, and it drops to 70.7 volts when the amplifier is detuned 5 kHz each side of resonance, the amplifier bandpass is 10 kHz, as illustrated in the accompanying figure.



Typical I-F Response Curve

The mannet in which the shape of the response curve selectivity) is changed by stagger-tuning (each tank tuned to separate frequencies) to achieve a broad L

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appears between the grid of VI and ground. When the input signal causes an increase in current through L1, a corresponding increase in voltage is induced in L2 by transformer action, and the increased voltage appears on the V1 grid. As the grid of VI is made more positive on the first half-cycle of operation, a larger plate current flows through the primary of T2. With tuned circuit L3, C6 tuned to the same frequency as the signal, a high impedance is presented to plate current flow, the plate voltage is reduced toward zero, and a large voltage drop occurs across L3. This voltage drop induces a negative-going signal in the secondary of T2 by transformer action. When tuned circuit L4, C7 is resonant at the signal voltage, a large negative voltage also appears between the grid of V2 and ground.

Since V1 and V2 are biased at the center of their grid-voltage plate-current transfer characteristic curve, large positive or negative swings of voltage can be accommodated without causing any distortion. Thus, the amplified input signal from V1, which appears on the V2 grid, is reproduced in amplified form in the plate circuit of V2. The operation of the tube V2 is similar to that of tube V1 except that the signal is oppositely phased. The negative grid signal from the first stage causes the plate current of V2 to decrease, and the plate voltage of the second stage rises toward the supply voltage (goes **positive**). At the same time, the primary of T3 offers a high impedance to current flow. The reduction in plate current flow through tuned primary circuit L5, C10 produces a large positive-going voltage and induces a voltage in the secondary of T3. When secondary circuit L6, Cl 1 is tuned to the same frequency as the signal, it produces a high impedance, and a large output voltage is developed across it.

When the input signal at the first stage goes negative, on the remaining half-cycle of operation, the action of VI and V2 is exactly the opposite of the described above. As the plate current of V1 is reduced by the input signal, a positive-going voltage is produced across the T2 primary-, and this voltage is applied to the V2 grid. In turn, the V2 plate current is increased, producing a negative output voltage across T3. Since Class A bias is employed, a sine-wave input produces a larger and amplified sine-wave output. As long as the grid signal does not drive the grid of V1 or V2 to the point where it draws current, and the plate voltage does not fatl below zero and cause plate current cutoff, no distortion occurs. The output waveform of the amplifier is the same as the input waveform, but is much larger in amplitude.

Since the grounded-cathode circuit inverts the input signal, the output of an even number of stages is of the same polarity as the input. Therefore, any feedback from output to input will produce regenerative oscillations. However, the very small plate-to-grid capacitance of the pentode reduces any such feedback to a negligible value, and neutralization is not required. The use of plate decoupling capacitors C5 and Cl 2 prevents feedback through common impedance coupling in the power supply. Thus, a stable, high-gain, and highly selective amplifier is produced by connecting the two double-tuned stages in cascade. From the discussion above it is is clear that the operation is identical to that of the single-stage pentode r-f voltage amplifier in all respects, except for the effects of the double-tuned circuits in providing higher gain and selectivity than is possible in a single stage.

#### Failure Analysis.

**General. The** discussions of failure analysis for the Pentode R-F Amplifier and the Cascade R-F Amplifier, previously discussed in this section, are generally applicable to the interstage i-f amplifier.

No Output. A defective i-f transformer, and open bias resistor (Rl or R4), loss of screen or plate voltage, or a defective tube can cause loss of output. Check the plate, screen, cathode, and supply voltages with a voltmeter. Lack of plate voltage can result from a defective power supply, an open plate resistor (R3 or R6), a shorted plate bypass capacitor (C5 or C12), or a defective transformer (T2 or T3). If the voltage is zero at the junction of C5 and R3, or C12 and R6, the cause is either an open plate resistor or a shorted plate bypass capacitor. A resistance check, , using an ohmmeter (with the power off), will determine which is at fault. With plate voltage of C5 and C12, but not at the plate of one of the tubes, and i-f transformer primary is defective, or the primary and secondary are shorted; in either case, replacement of the transformer is necessary. An open plate circuit in a screen-grid tube can usually be determined quickly by noting that the screen is red, because of an overloaded screen, which tries to take the place of the plate. In this case screen resistor R2 or R5 will be excessively hot; it may smoke, and will eventually burn out. Where voltage exists on the plate of one of the tubes, but not on the screen, bypass capacitor C4

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or C9 may be shorted, or screen resistor R2 or R5 may be open. A resistance check from each screen bypass capacitor to ground (with the power off) will indicate zero if the capacitor is shorted, and a resistance check of the screen resistor will reveal the condition of the resistor. Since the screen voltage determines the plate current of a pentode, to a great extent, it is not always necessary for the screen voltage to be zero in order to cause loss of output. Since cathode resistor R1 or R4 is in series with the tube, if the resistor is open the circuit to ground will be incomplete and the tube will not operate. Likewise, if it increases in value sufficiently the tube can be biased off to almost zero plate current, and cause such a small output as to be considered practically no output at all.

If the tube is defective and no emission occurs, the cathode voltage will be zero. With C3 or C8 shorted, there will also be no cathode voltage, but the output will be distorted because of heavy plate and screen current; in this case the plates will get red and the tube may be damaged. Where the indications are otherwise normal, the tube should be suspected. With normal plate, screen, and cathode voltages, and no output, and the tubes are known to be good, it is certain that the **secondary** of output transformer T3 is open or totally detuned. Usually such a condition will produce a slight output because of stray capacitive coupling between windings, but it could be mistaken for a no-output condition.

Low Output. Low output can be caused by a defective tube, low screen or plate voltage, or too high a bias. First check the tube element voltage with a voltmeter. A low voltage on the plate or screen indicates excessive current drain in that circuit (producing a large voltage drop through the series resistor), an off-value plate or screen resistor, or a leaky bypass capacitor. The resistors can be checked by means of an ohmmeter (with the power off), and the capacitors with an in-circuit capacitance checker. Larger than normal plate and screen current will also cause a corresponding increase in bias voltage, since cathode bias is produced by the sum of all currents flowing in the tube. A leaky screen or plate bypass capacitor will cause reduced plate or screen voltage, reduce the cathode current flow, and hence decrease the bias. Low tube emission is usually indicated by

higher than normal plate and screen voltages, with reduced cathode bias. As the condition becomes worse, the output will continue to decrease progressively until the tube emission is insufficient to produce an output. When all voltages appear normal and the output is low, either a tube may be defective or the alignment may be at fault. If during alignment one of the tuning capacitor (or tuned inductors where inductive tuning is used) does not seen to have any effect, the transformer being tuned is defective; replace it with a good one.

When the set suddenly blocks on receiving a loud signal and becomes almost inoperative, the **i-f** ampli**fier** is probably oscillating and developing sufficient bias to cause the reduction in the output signal. Sometimes blocking will not occur, but a strong squeal or howl will occur instead. In either case a plate or screen bypass capacitor may be open. In some instances drying out of the last electrolytic capacitor in the power supply will cause loss of **fil**tering ability, produce hum, and through common impedance coupling cause a similar effect.

**Distortion.** Distorted output can be caused by an improper bias, plate, or screen voltage. When the plate voltage drops below zero, plate current cutoff occurs, and this stoppage of plate current flow causes distortion. If the plate voltage is driven into plate current saturation no further change in plate current can occur, and a similar type of distortion will exist. Excessive bias will cut off the lower portion of the drive signal, reduce the plate current swing, and cause distortion. Likewise, excessive input (drive) voltage will cause the bias to be driven to zero (or above) and cause grid current flow; this will cause plate current saturation on one signal peak, and cutoff on the opposite signal peak. Both distortion and reduced signal output will occur. Usually, a voltage check for this condition will indicate improper or fluctuating voltages on the tube electrodes. However, it is easier to use a scope with an r-f probe and observe the signal. A simulated (signal generator) input with modulation applied also provides a simple signal for observation on a scope. Localization of the trouble to a specific portion of the circuit will usually involve only those components in the circuit where the distortion is observed, so that further simple voltage or resistance checks of the parts involved will locate the defective part.

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# TUNED INTERSTAGE (I-F) AMPLIFIER (SEMICONDUCTOR)

#### Application.

The tuned interstage i-f amplifier is used in superheterodyne receivers to produce high gain and the desired selectivity.

#### Characteristics.

Operates at a fixed frequency and is tunable over a small range for alignment and adjustment of bandpass.

Uses either single- or double-tuned coupling (i-f) transformers.

Uses Class A bias to minimize distortion.

Common+ **mitter** configuration normally used, although common-base circuits may be encountered in some applications.

Usually includes a neutralization circuit to preventy internal feedback from causing self-oscillation.

# Circuit Analysis.

**General.** The i-f amplifier in a superheterodyne receiver determines the selectivity and gain. By using a number of cascaded tuned stages operating at a relatively low radio frequency as compared with the fundamental received frequency, higher gain per stage is obtained than would be possible at the signal frequency, By using a number of tuned circuits, the selectivity is increased over that of a single tuned circuit. The accompanying figure illustrates the manner in which the selectivity and bandpass are affected by a number of tuned circuits.



Effect of Tuned Circuits on Bendpass

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produced by a single tuned circuit is shown. In part B, the double-humped curve produced by a staggertuning two i-f stages is shown (overcoupled circuits also produce a similar response). In part C, the individual response curve are super-imposed on each other. In part D, the idealized response is shown. These coupling circuit techniques are similar to those used in electron tube circuits. Since the tuned circuits in the i-f amplifier form a coupling network matching the output of one stage to the input of the next stage, it is necessary to hold losses in the network to a low value. It is also necessary to match the output and input impedance to obtain maximum gain. At the same time, the unloaded Q of the coupled circuits must be kept as high as possible to retain a good selectivity characteristic. Because of the relatively low input and output impedance of the transistor and the large capacitance between emitter, base, and collector, deisgn problems are created which do no occur in the electron tube circuit. For example, the power transfer efficiency between the primary and secondary of a tuned transformer is maximum when both the unloaded Q and the bandpass are large. Thus, a high power transfer and a narrow band pass pose conflicting requirements. Since the bandpass requirement is determined by the amount of selectivity desired, if the input and output impedance are matched, the power transfer can be improved only by raising the unloaded Q.

In part A of the figure, the selectivity curve

The common-emitter circuit has a low input resistance together with a high input capacitance, and the output impedance is moderately high with a large shunt capacitance, Therefore, in interstage coupling transformers an impedance ste-down (which varies as the square of the turns ratio) is required to match the high output impedance to the low input impedance of the next stage. In addition, the total circuit capacitance must be considered when determining the inductance needed to resomte at the intermediate frequency. Thus, the reflected input (secondary) capacitance (which varies inversely as the square of the tuns ratio), plus the primary shunt collector and wiring capacitance, together with the actual primary tuning capacitor, form the total tank tuning capacitance. When calculated for a given set of design considerations, the inductance is often very small and, at an i-f of 455 kHz, requires a very large tuning capacitance to obtain resonance. While the large tuning capacitance has the beneficial effect of swamping out the comparatively small transistor capacitances, it is difficult to build a small inductance with a high Q. Therefore, it becomes necessary to increase the small value of primary inductance to a larger and more practical coil value. By increasing the inductance (for example 100 times), the tuning capacitance can be reduced to only one one-hundredth of its former value and still resonate at the same intermediate frequency. Although a high-Q circuit, the primary tank now has an impedance of 100 times the original value. To retain the original impedance to match the transistor, the tank is tapped to produce a 10-to-1 turns ratio (the inductance functions as an autotransformer), and the transistor is connected across the lower-impedance portion of the primary winding.

With the primary tank matched for proper power transfer the turns ratio between the entire primary and secondary is selected to produce the proper stepdown ratio. Thus, all impedance involved are matched for efficient power transfer. If necessary, the i-f secondary may also be tapped in a similar manner to obtain a high-Q input tank. The following figure illustrates the manner in which the desired selectivity and impedance matching are obtained in a simple singletuned i-f transformer designed for a 455 kHz i-f.



**Typical Matching Circuit** 

**Circuit Operation.** The schematic of a typical interstage i-f amplifier with neutralization, employing the common-emitter configuration, is shown in the accompanying illustration.



Typical Common-Emitter i-f Stage

The input signal is coupled to the base of Q1 through T1. I-F transformer T1 is double-tuned, with L1, Cl forming the primary tank and L2, C2 forming the secondary tank. The low, base-input impedance is matched for maximum transfer of power by tapping it down on inductance L2, thereby retaining the high Q necessary for good selectivity. Trimmer capacitors Cl and C2 tune the i-f transformer over a small range about the center frequency, permitting exact alignment at the intermediate frequency. Class bias is supplied to the base of Q1 through voltage divider RI and R2. R2 is bypassed for rf by C6. R3 and C3 are the conventional emitter swamping resistor and by- " pass capacitor. (See the introduction to this section for discussions of biasing methods and stabilization methods.)

Output transformer T2 couples the collector of Q1 to the base of the following stage. The primary of T2 consists of L3 tuned by C4, and the secondary consists of L4 tuned by C5. L3 is tapped to match the collector output, provide maximum power output, and yet retain the high Q necessary for selectivity. Capacitor C7 is used to bypass the collector supply. Neutralization is provided by RC network CN, RN, connected from the secondary of T2 to the

base of Q1. The feedback is taken from the transformer secondary to provide a 180-degree phase shift or polarity inversion, to cancel the internal feedback developed within the transistor.

In the absence of an input signal, the fixed bias" determined by the ratio between R1 and R2 causes Q1 to draw its quiescent value of collector current. Q1 operates at the center of its characteristic transfer curve to permit equal positive and negative swings. Since the quiescent current is steady, no output is developed. Assume an input signal within the intermediate frequency bandpass is applied to the T1 primary. Primary tank Cl, L1 appears as a high impedance to those frequencies within the bandpass, and, since it is a resonant load for the preceding stage, it develops a large voltage across L1. This primary voltage, in turn, induces a voltage in the L2 secondary. The secondary is tuned by C2, and is resonant at the same intermediate frequencies. Therefore, a large voltage is developed for those frequencies which are within the bandpass, and a portion of this voltage developed between the tap and ground (since C6 provides an r-f shunt around R2, and places the rotor of C2 and the lower end of L2 at ground potential) is applied to the base of QI. These i-f frequencies are essentially sinusoidal; they consist of the fundamental (or carrier) and modulation which appears as sidebands above and below the center frequency. Assume that a half-cycle of this frequency is negative and adds to the normal forward bias applied to Q]. For the duration of this negative-going half-cycle, the emitter and collector current of Q1 increases sinusoidally, in synchronism with the amplitude of the applied signal.

Since the collector is tapped to L3 any current flow through the tap to the ground end of the coil also induces a voltage in the top portion by autotransformer action. Capacitor C4 tunes L3 to the intermediate frequency, and the tank appears as a high impedance to those frequencies within the i-f bandpass. Thus, a large voltage is developed across the primary of T2 and induces, by transformer action, a voltage in the tuned secondary circuit. The tapped portion of L3 also provides an impedance transformation. With the lower end of L3 supplying an impedance equal to the collector impedance, maximum power transfer occurs through the transistor. The upper portion of L3 (above the tap) provides a higher impedance, which allows a sufficiently high Q to be obtained to provide sharp tuning and selectively

despite the loading effect of collector current flow through the bottom of the coil. Thus, only frequencies within a narrow bandpass around the carrier (i-f) frequency are amplified strongly, and the frequencies outside the bandpass are reduced in amplitude and effectively rejected.

During the remaining (positive) half of the single r-f cycle, the signal opposes the forward bias and causes a reduction in the emitter and collector current. These alternate increases and decreases in current occur at i-f rates, and are equivalent to an ac current flow; thus, the ac signal variations induce an output voltage in the secondary of T2. If the current did not vary with the signal, but rather remained steady, no transformer action could occur.

While the dc emitter current flows through R3, the i-f variations are bypassed by capacitor C3 so they have no effect on emitter resistor R3. Thus only small current changes (induced by temperature changes), consisting of slow, dc variations of emitter current, affect R3. Since electron flow is from emitter current, affect R3. Since electron flow is from emitter to ground, the current changes produce an oppositely polarized voltage which subtracts from the normal forward bias and returns the emitter current to its previous value. This is conventional emitter-swamping action.

The output impedance of the collector is reduced by the step-down turns ratio between the primary and secondary to a value suitable for matching the input impedance of the next i-f stage. Tank circuit LA and C5 is also tuned to the intermediate frequency and selects only the desired signals for application to the next stage. The use of a number of tank circuits provides a relatively flat but sharp selectivity curve, as explained perviously in the introduction to this circuit.

When the intermediate frequency is high enough to cause some of the collector output to be coupled back to the base through the collector-to-base capacitance and develop a feedback voltage through the internal base spreading resistance, oscillation occurs in the i-f stage. Therefore,  $C_N$  and  $R_N$  are used to feed back a voltage from the secondary of T2, whose phase is opposite that of the collector output, to the base of Q1. With an equal voltage of opposite polarity, the internal feedback voltage is cancelled and oscillation cannot occur. In some circuits  $R_N$  is not used;  $C_N$  is sufficient. In some circuit designs, mismatching of the stages is used to avoid feedback and

oscillation, with some loss of gain. Usually, only as many stages as are necessary are used to provide satisfactory selectivity, since the more the stages the greater the feedback possibility. Likewise, doubletuned circuits are not used where single-tuned transformers are satisfactory.

# Failure Analysis.

**General.** When making voltage checks, **use a** vaccum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of most volt-ohm-milliammeter testers. Be carefuI, also, to observe proper polarity when checking continuity or making resistance measurements with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. Lack of an input signal, improper bias, lack of supply voltage, or a defective transistor can cause loss of output. Check the bias and supply voltages with a voltmeter. If R1 is open, the base bias will be zero, which corresponds to Class B operation, and there is a possibility that strong signals may produce a partial output. However, if R2 is open or if the secondary of T1 (L2) is open, the base circuit of Q1 is also open and no output can occur. Should the primary of T1 (Ll) be open, there will be no collector voltage applied to the preceding stage, and no transfer of signal to Q1. Since the i-f stage operates at radio frequencies, use an r-f probe in conjunction with a VTVM, or an oscilloscope, to determine whether a signal appears on L1. If R3 is open, the emitter circuit will be incomplete and no output will be obtained. Use an ohmmeter to determine the continuity and resistance of R3. If a voltage exists at the base of Q1 but not at the collector, either T2 is defective or C7 is shorted. A dc voltage reading between the collector and ground with no output indicates that either Q1 is defective or T2 is short-circuited. Check T2 for shorts with an ohmmeter. If neutralizing capacitor  $C_N$  is shorted, the base of the following stage will be directly connected to the base of O1 and will shunt transistor O1. There will be a loss of amplification, but not necessarily a complete loss of output. However, if the capacitor is open, oscillation will occur and may cause blocking due to a change of bias (the transistor will rectify the oscillation and produce a dc bias). Or, if the oscillation is not strong enough, a partial output may be obtained

(with or without distortion). Check the capacitor with a capacitance checker; also check the value of resistor  $R_v$  with and ohmmeter.

Low Output. A number of conditions can cause reduced output. For example, low collector voltage, low bias voltage, loss of transistor gain, an open or high-resistance tuned circuit in the i-f transformers, and short-circuited or changed values of other parts. Check the bias and collector voltages with a voltmeter. Use an oscilloscope and r-f probe and test from point to point throughout the circuit, to determine where the signal drops in amplitude. The signal at the collector of **O1** should be larger in amplitude than the signal at the base of Q1. If the signal appears at the input to T1 and is greatly reduced at the base of Q1, either T1 or Q1 is defective. If C3 is opencircuited, the emitter current flowing through R3 will produce degeneration and oppose the bias. The output will be reduced in proportion to the amount of degeneration. With a collector output equal to or less than the output at the base of O1, either T2 or O1 is defective.

Insufficient Selectivity. Lack of selectivity can occur because of poor alignment of tuned circuits, which is usually indicated by loss of gain, together with broad tuning. In most cases, however, special tests are necessary to determine whether realignment is needed, and special procedures and equipment are required for proper alignment. Therefore, readjustment of the i-f trimmers should be attempted only when it is ascertained that the circuit is otherwise operating normally. Where i-f transformer(s) are replaced, it is necessary to make proper adjustments to restore the initial selectivity. A rough approximation of performance may be obtained by observing the detected output on an oscilloscope and tuning an r-f signal generator through the i-f bandpass. The amplitude of the signal observed on the oscilloscope will be nearly uniform for a flat-topped response curve. The 70-percent response points below and the above the i-f center frequency will indicate approximately the low- and high-frequency limits of the bandpass. Where lack of selectivity is suspected, the necessary check can be made by determining the equipment specifications, following the manufacturer's recommended alignment procedure, and comparing results, noting the effect of each adjustment of the response curve.

# TRIODE R-F BUFFER AMPLIFIER (ELECTRON TUBE).

#### Application.

The triode r-f buffer amplifier is employed in receivers, test equipment, and transmitters as an intermediate amplifier stage, between the oscillator and the output stage, to minimize or eliminate the effect of impedance or load changes in the output on the oscillator frequency.

#### Characteristics.

Operates Class B or C in transmitter applications, and Class A (or  $AB_1$ ) in test equipment and receiver applications.

Gain and power output are usually low.

Normally operates on the same frequency as the oscillator and output stage.

Plate efficiency varies with the bias; Class A is lowest and Class C is highest, with Class B at some intermediate value.

Requires more grid drive than a pentode buffer.

Usually requires neutralization to prevent feedback and self-oscillation.

# Circuit Analysis.

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General. In receiver applications, the r-f buffer amplifier is generally used between the local oscillator and the mixer as shown in the accompanying block diagram. Thus, any changes in mixer operation or load, such as might be caused by automatic volume control, affect only the buffer stage, and the oscillator frequency is not pulled or changed. This type of operation is used mostly for single sideband reception, where the oscillator frequency must be kept stable within a few cycles of the desired fundamental or output frequency. In transmitters, the buffer amplifier is used to isolate the high-level modulated r-f output stage from the oscillator, to prevent frequency modulation effects on the carrier and to avoid distortion. It is also used in low-level stages for the same purpose, and in cw operation it prevents sudden changes in load with keying from affecting the oscillator frequency. It is sometimes used as a dual-purpose amplifier to supply additional drive power, plus isolation. When used as a power amplifier, however, its isolating effect is nullified with the larger outputs and loads, so that sometimes more than one power buffer stage may be used. In test equipment, the r-f buffer is not necessarily used only to provide a stable oscillator

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frequency, but may be used to prevent the changing of load in one stage from having any other effect on the stage preceding the buffer. Because test equipment and receivers require linear operation with minimum distortion, these buffer stages are always operated Class A (or  $AB_1$ ). Although the transmitter buffer stage could also be operated Class A, it would result in an unnecessary loss in efficiency; hence the reason for Class B or C operation. Because the Class C stage requires a large drive and this grid current requirement loads the preceding stage, Class C operation is not used when Class B operation will suffice. Since only an r-f carrier is amplified, the tank circuit eliminates any distortion caused by single-tube Class B operation.



**Buffer Loeetions** 

**Circuit Operation.** The schematic of a typical triode r-f buffer amplifier is shown in the accompanying illustration.

Capacitive input and output coupling are provided through Ccl and  $C_{c2}$ , respectively. Both fixed grid bias and protective cathode bias are employed (although either could be used alone). Resistor RI provides the grid bias by means of the grid current



**Triode R-F Buffer Amplifier** 

flow in Vl, obtained through grid drive from the oscillator input. Radio-frequency choke RFC 1 keeps the input rf from being shunted to ground through the grid return resistor. Protective cathode bias is supplied by R2, bypassed by Cl for rf. The plate tank consists of L1 and C2, with C2 being a split-stator type of variable capacitor. Thus, with the center plate of C2 grounded, the tank is balanced, and opposite polarities exist at the ends of the tank coil. One end of the tank coil is coupled through  $C_{c2}$  to the next (output) stage, while the other end of the coil is fed back through C to supply a neutralizing connection, and the plate voltage is applied to the center of the coil. RFC2 keeps the rf in the tank out of the power supply, and C3 assures this by bypassing any remaining residual rf around the power supply to ground.

In the absence of an input signal, cathode current flow through R2 develops a protective cathode bias which is sufficient to prevent damage to the tube, but is not sufficient for normal operation. When the oscillator input signal is applied through  $C_{c1}$  to VI, grid conduction occurs during the positive half-cycles. Grid current flow from the cathode to the grid, charging the coupling capacitor. During the negative alternation, the grid current is cut off by the negative signal and the bias voltage developed by the charge on

the coupling capacitor discharging to ground through R 1. After a few alternations this signal bias develops a steady bias voltage. The total tube current flow through VI and cathode bias resistor R2 adds a slight amount to the signal bias, and the operating bias is a combination of both. Normally, the tube operates Class B, and plate current is cut off during the negative half-cycle (when operated Class AB only a portion of the negative half-cycle is cut-off). Thus, plate-current pulses flow only during the positive half-cycle, and loss of the negative half-cycle would normally cause distortion. However, the tuned tank circuit, consisting of LI and C2, acts as a reservoir for rf and supplies the missing negative half-cycles. This action occurs because, once the tank circuit is excited, oscillations do not immediately cease unless there are heavy losses in the tank. Otherwise, once the source of rf is removed, the circuit continues to oscillate with diminishing amplitude each cycle until the rf is dissipated in the resistance of the tank. Since pulses of rf energy are supplied each positive halfcycle, the tank is effectively returned to its initial amplitude once each cycle. Any tank losses are thus supplied by the cycle during which conduction occurs. Therefore, than tank operates as though it were continuously excited, and no distortion in the output exists because of the loss of the negative halfcycle of operation. Single-tube, Class B operation is possible in an r-f amplifier because of the tuned tank circuit. In an audio amplifier, two tubes are necessary, one operated by the positive half-cycle and the other by the negative half-cycle, to provide an undistorted signal.

With the output tank tuned to the same frequency as the input (drive) signal, positive feedback can occur through the large grid-to-plate capacitance of the triode. Although the polarities of the grid and plate are opposite in the common or groundedcathode circuit, the capacitive feedback voltage leads the predominantly inductive (high-Q) tank voltage, and is, therefore, of the proper phase to combine regeneratively with the input signal. Hence, neutralization is necessary to prevent self-oscillation. Neutralization is accomplished by feeding back an equal but oppositely polarized voltage through C<sub>n</sub> from the other side of the tank. Since at any instant the opposite ends of any tank coil are of opposite polarity, taking the feedback voltage off the end of the coil opposite the plate always provides the correct polarity for neutralization. The use of a center-tapped coil

with a split-stator tuning capacitor **insures** a completely balanced tank. Thus, it is only necessary to adjust  $C_n$  to approximately the same value as the grid-to-plate capacitance to obtain neutralization.

The manner in which the neutralizing circuit forms a reactive bridge with equal arms is shown in part A of the following simplified schematic. This plate-togrid feedback system is known as the Hazeltine or *neutrodyne* type of neutralizing circuit. A similar form of feedback from grid to plate is known as the *Rice* system, and is shown in part B of the schematic. While other forms of neutralization are also used, these two types are the most popular and commonly used circuits. In part A of the illustration,  $Z_g$  is the input impedance, and coils L<sub>p</sub> and L<sub>n</sub> together form tank coil LI in the plate circuit. The voltage across  $C_n$  is equal, and opposite in polarity, to that across  $C_{gp}$ ; thus, there is no flow of current from output to input, and complete neutralization results. In part B of the figure, the opposing voltages are developed in the grid tank across  $L_{p}$  and  $L_{n}$ ; otherwise, the operation is the same.



**Typical Neutralizing Circuits** 

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Although the triode buffer described above uses capacitive input and output coupling, inductive coupling can be used instead. In this case the grid circuit usually contains a tank, with a coupling coil, and the plate likewise. The operation is the same except for the inductive input and output coupling, which merely transfers the signal into the input tank and out of the output tank. Push-pull stages may also be used as buffer amplifiers, in which case neutralization is easily accomplished by using cross-connected grids and plates, since they are oppositely phased and polarized.

The basic triode r-f buffer amplifier originally consisted primarily of a low-gain voltage amplifier which did not draw grid current and was lightly loaded, since it only supplied the grid current (drive power) necessary for the final output stage. Therefore, it offered no load to the self-excited oscillator, and allowed it to operate at maximum stability. At the same time, the tube was chosen with a power rating which was more than sufficient to supply the grid power needed by the final amplifier. Thus, the buffer stage effectively isolated the oscillator from the output stage, so that it was" affected very little by any modulation peaks, or on-off keying of the output stage. For satisfactory performance Class A operation of the buffer was required, and low efficiency was obtained. In later years oscillators of better stability were produced, and Class B operation permitted a more efficient output with slight oscillator loading. Thus, as the state of the art advanced and electron tubes and parts improved; it was found that even Class C operation could be used. Hence, the buffer amplifier is now generally considered to be any amplifier used between the oscillator and output stages and operating on the fundamental frequency. By using Class AB<sub>1</sub> operation, high efficiency with no grid current flow can now be obtained. However, the high gain of the pentode has virtually made the triode buffer obsolete except for special applications.

When operated Class A, the operation is the same as that described previously except that it is not necessary for the tuned tank to supply the negative portion of the waveform.

#### Failura Analysis.

**No Output.** Lack of an input signal, loss of plate voltage, a defective tube, or a detuned output tank will cause loss of output. The supply voltage should be checked with a voltmeter to determine whether

the proper voltage is available. The grid drive maybe checked by reading the grid voltage developed across RI (in stages where grid current is drawn). Usually, transmitters are equipped with a milliammeter to read grid and plate current for tuning indications. Plate current indications will usually pinpoint the trouble to a particular location. For example, no plate current indicates an open plate or cathode circuit, a defective tube, or lack of plate voltage. In this case, it is a simple matter to turn off the plate power, discharge *the filter* with a shorting stick, and then make a resistance check of cathode resistor R2, and a continuity check of L1 and RFC2. If plate current is present, tune C2 for minimum dip in plate current. With sufficient drive, there should be a large current off resonance and a small current at resonance. If the drive is lacking, the ratio between the nonresonant and resonant condition will be small. If the ratio is large and the resonant current is lower than normal, there is no load or only a light load on the output, and  $C_{c_2}$  is a probable open. In this instance, an r-f indicator will show rf on the plate side of the capacitor, but not on the output side; use a small coil connected directly to the vertical plates of an oscilloscope (not through the scope amplifier) to couple to the plate tank and indicate rf. Lack of grid drive will show as a large plate current indication which cannot be dipped to a normal low value, since the bias will be only that provided by R2. If C3 is shorted, the power supply plate fuse or circuit breaker will open, no plate voltage will be applied, and loss of output will occur. Where the plate voltage is normal and the grid drive is sufficient, but the plate current is low (or slowly decreases as the stage operates), the emission of the tube is probably low.

Low Output. Low plate voltage, low grid drive, improper bias, or a defective tube can cause low output. The plate supply voltage and grid bias across R1 and R2 can be checked with a voltmeter. It is important to note the difference between receiving and transmitting r-f amplifier voltage measurements. In the receiver stage, any rf on the grid or plate is usually so small that it will not damage the meter; however, in the transmitter stage, large r-f circulating currents are produced in the grid and plate circuits which can damage the meter when dc measurements are made to ground. Therefore, it is necessary to use a radio-frequency choke in series with the voltmeter, or use a probe which is adequately faltered for rf. A vaccum-tube voltmeter may be used on receiving equipment, but it is usually unable to withstand the high voltage present in transmitters. As a general rule, therefore, all dc voltages measurements are made in portions of the circuit which are "cold" to rf (no rf exists), and other indications, such as plate current, are used instead. (In special instances, r-f voltmeters can be used.)

With proper plate voltage and bias, low output will be obtained if the r-f grid drive is not sufficient to make the tube draw the proper value of plate current. Likewise, low emission will make it impossible to obtain the proper plate current, and thus the proper output. When all indications other than plate current are normal, the tube is probably at fault.

If cathode capacitor Cl opens, plate current variations occurring at radio-frequency rates will momentarily develop high cathode bias voltages, produce degeneration, and cause reduced output. Temporarily grounding the cathode in this case will restore operation and the output to normal, and prove that Cl is defective, Do not try grounding the cathode unless grid drive is present; otherwise, the tube will operate at zero bias, will be overloaded, and will be damaged if current is allowed to flow for a prolonged period of time. Sometimes low output will be obtained because of parasitic oscillation at a very low frequency. This occurs when a feedback loop occurs through the neutralizing circuit and an associated r-f choke and bypass or tank tuning capacitor(s). The symptoms are high plate current with low r-f output at the desired frequency and larger than normal grid current. Once started, these oscillations will usually continue when the normal grid excitation is removed. If the circuit operates and tunes normally with reduced plate voltage and at a reduced output, but will not do so when full plate voltage is applied, parasitic are probably " the cause. Usually, this will not occur in Navy equipment when initially received, but can sometimes be caused by a change in components with age, by a part failure, or by improper bias, or change of lead dress during a repair.

Improper Neutralization. When a stage is incompletely neutralized or misadjusted, operation will become erratic. The tube may operate normally and then suddenly start oscillating when shocked by a transient pulse. To determine whether the stage is properly neutralized, *remove the plate voltage* and tune the plate capacitor through resonance while

observing the grid meter indications. A steady, unchanged meter reading indicates complete neurtrdization; a slight change or sharp flick of grid current as resonance is passed indicates that neutralization is incomplete. Adjust the neutralizing capacitor while tuning the plate through resonance until the grid meter remains steady.

# PENTOOE R-F BUFFER AMPLIFIER (ELECTRON TUBE)

Application.

The pentode r-f buffer amplifier is universally used in receivers, test equipment, and transmitters as an isolation stage. It is generally used between an oscillator and an output stage to prevent modulation or load changes from affecting the oscillator frequency.

#### Characteristics.

Usually operated Class A or AB, self-biased, although Class B or C operation is sometimes employed.

Has relatively high voltage and power gain.

Provides more output than a triode r-f buffer amplifier, with less drive.

Does not normally require neutralization.

Operates on same frequency as input and output stages.

Has greater isolating effect than a triode.

#### Circuit Analysis.

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General. The pentode r-f buffer amplifier is an effective isolation amplifier because of the low grid voltage drive required for full output, which places very little loading on the oscillator (or input) stage. Thus, the oscillator can be designed for maximum stability under a light or idling load. In addition, the effective shielding supplied by the screen and suppressor elements of the pentode reduces the grid-toplate capacitance to such a small value that feedback is practically eliminated. Therefore: no neutralizing circuits are needed, so that fewer parts are required and the neutralizing adjustment is eliminated. Finally, the high amplification factor of the pentode produces a large output voltage under the control of only a small grid voltage. Since the screen prevents plate current variations from affecting the grid or input circuit to any marked extent, a much larger power can be developed in the pentode plate circuit than in a triode

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operating at the same plate voltage. Because of the small drive required, the pentode r-f buffer amplifier may also be used to drive another pentode (or tetrode) output tube without losing its ability to act as an isolation stage. The resultant transmitter output, then, is equivalent to that developed by two or three triodes operating at higher plate voltage and currents.

Circuit Operation. The accompanying illustration is a schematic of a typical pentode r-f buffer amplifier.



Typical Pentode R-F Buffer Amplifier

The grid of V1 is capacitively coupled through  $C_c$ to the oscillator. Resistor RI is the grid return resistor, across which the input voltage appears. Cathode bias is supplied by R2, which is bypassed for rf by Cl. Screen voltage is obtained through dropping resistor R3, which is bypassed to ground for rf by C2. The plate voltage is series-fed through L1 to the plate of VI, and is tuned to resonance by C3. L2 is the output coil, which is inductively coupled to L1 (Ll and L2 form r-f transformer Tl). The radio-frequency choke (RFC) prevents any rf from entering the supply and is bypassed to ground for rf by C4.

When the oscillator operates, a signal which is approximately a sine wave is developed in its plate circuit, and is applied through C<sub>c</sub> to the VI grid. The low reactance of C<sub>c</sub>ensures that a minimum voltage drop (and very little loss of signal) occurs across the coupling capacitor. Grid resistor RI provides a high impedance across which the oscillator signal is developed. Since the grid does not normally draw any grid

current, no current flows through R1 at any time (unless Class B or C operation is employed). Cathode resistor R2 provides bias voltage which is developed across it by space charge current flow, that is, the sum of both the screen and plate currents. When plate and screen voltage is applied to V1, current flows from ground through R2, producing a positive cathode bias which is equivalent to a negative bias voltage applied to the grid. Since R2 is bypassed by Cl for rf, no change occurs in bias when an input signal appears across VI (between grid and ground). Any r-f current variations are bypassed around R2 by Cl; hence, the bias is affected only by a steady change in plate or screen current, and not by instantaneous r-f variatioris. Thus, as the load changes the bias will also change accordingly. It is important that the load be held constant to produce the desired operating bias. When operated Class A (in receivers and test equipment), the operation is over the linear portion of the  $E_q\mathchar`-I_p$  curve. In Class AB operation a slightly higher bias is used. (See the introduction to this section for discussions of cathode bias and classes of amplifier operation.)

As the oscillator signal is applied to the grid of Vl, assuming a sinusoidal input signal, the positive halfcycle of operation causes the plate current to increase, and the negative half-cycle causes the plate current to decrease. The plate current swing is determined by the screen voltage appearing on the screen of V1, which is controlled by the value of R3. The screen resistor is chosen so that with the proper plate voltage applied, and with no signal, the V1 screen and plate current flowing through cathode bias resistor R2 provides the normal bias, During operation, the screen current flows steadily, producing a voltage drop across R3 of sufficient value to drop the plate supply voltage to the desired screen voltage value. Any electrons striking the screen are bypassed to ground through capacitor C2. Likewise, any change in plate current will not effect the screen voltage, since R3 is always kept at ground potential for r-f variations; hence, only dc current flow determines the screen voltage, and this does not vary with the signal. Since the screen is closer to the grid than to the plate, it exerts a strong control over the plate current; also, since it is grounded for rf through C2, no feedback can exist between the grid and the plate (it acts as a shield). Thus any possibility of feedback and selfoscillation is eliminated, and neutralization is unnecessary. Tank circuit L1, C3 is connected in series with

the plate of VI, and when tuned to resonance offers a high impedance. Thus, as the input voltage swings positive, the plate current of V1 increases, and in flowing through L1 induces a voltage in secondary L2 by transformer action. Meanwhile, the high impedance of the tank produces a large plate voltage drop and the actual plate voltage falls toward zero. The design is such that the plate voltage is not allowed to drop below the actual screen voltage. (Otherwise, the screen of V1 would tend to act as a plate; thus it would be overloaded and cause distortion.)

As the oscillator signal changes its cycle and swings negative, the VI plate current is reduced, and the reduced value of current through L1 induces an oppositely polarized output voltage in L2 by transformer action (the current now flows in the opposite direction). At the same time, the plate voltage rises toward the supply voltage. The actual plate voltage is almost equal to the supply voltage at the negative peak of the input cycle. The grounded-cathode circuit produces a polarity (or phase) inversion, When the input signal goes negative, the plate output signal is positive and of opposite phase or polarity; conversely, when the input signrd goes positive, the plate output signal is negative. The output voltage induced into secondary coil L2 is polarized similarly when it is connected in-phase. If connected out-of-phase, the output signal polarity is the same as that of the input signal.

Capacitor C4 keeps the lower end of tank C3, L1 at r-f ground potential, and the RFC ensures that any residual rf is offered a high impedance, so that it flows to ground through C3 rather than attempting to flow through the low impedance offered by the output falter capacitor of the plate supply.

If tank circuit Ll, C3 is not tuned to the oscillator or input frequency, a very small impedance is offered in the plate circuit and little or no output voltage is developed. The unloaded Q of the tank circuit is made high, so that the loaded Q (at resonance) provides sufficient selectivity to pass only a narrow band of frequencies between the half-power points, and the tank is able to discriminate between wanted and unwanted signals. While in Class A operation plate current flows at all times during the cycle, in Class AB or B operation part of the signrd is missing (it is beyond cut off). During this period, r-f **energy** is supplied from the tank circuit so that the operation is the same as if plate current flowed constantly without any interruption of output, and no distortion is

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developed. The plate tank is reinforced during each positive half-cycle with sufficient rf to overcome any tank losses, so that the tank is never depleted.

Grounding the suppressor grid provides a shielding action between the screen and plate, and thus prevents secondary emission from the plate. Therefore, coupling between the plate and grid is only through the electron stream, and is at a minimum. In those tubes with suppressors internally connected to the cathode, the operation is identical except there is slightly more coupling between the grid and plate through the electron stream.

Although the input is shown capacitively coupled, it is sometimes inductively coupled, in which case a tuned tank is used in the grid circuit in place of resistor R]. The operation is the same except for the development of a slightly larger grid excitation, since the parallel-tuned tank usually offers a higher impedance than the grid resistor and will cause the input voltage to increase at resonance. Thus, when Class B or C operation is employed, the tank is sometimes added to provide better grid regulation, since grid current tends to shunt the input and lower the grid input impedance.

As is evident from the discussion above, the buffer amplifier operates in practically the same manner as the pentode r-f voltage amplifier previously discussed as a separate circuit. The only actual difference is in the design considerations, which are based upon light grid and plate loading to provide maximum isolation rather than output voltage or power.

#### Failure Analysis.

**General.** The discussion of failure analysis for the Pentode R-F Voltage Amplifier, previously discussed in this section of the handbook, is generally applicable, and is particularly slanted toward receiving application.

No **Output.** Loss of plate, screen, or filament voltage, a defective tube, defective coupling capacitor Cc, open output coil L2, or shorted grid return resistor RI can cause no output. Check the tube voltages and supply voltage with a voltmeter. WARNING: Voltages dangerous to life usually exist in the plate and screen circuits; be certain to observe all safety precautions when checking these voltages. An open filament can sometimes be observed by noting that the tube is not illuminated and feels cold to the touch. If there is still no output, coupling capacitor  $C_c$  is probably open; check for proper capacitance with an in-circuit

with an r-f probe (or an oscilloscope), check for voltage between the input and ground. If there is a voltage indication on one side of the coupling capacitor but not on the grid of V1, the capacitor is open or R1 is shorted. (If C<sub>c</sub> were shorted, a high positive voltage would appear on the grid from the oscillator plate and cause high cathode bias voltage.) An open screen resistor (R3) will be indicated by lack of screen voltage, although a shorted screen capacitor (C2) will give a similar indication. In the latter case, however, R3 will heat abnormally and drop the screen voltage to zero. This short-circuit condition may be observed visually by smoke from, or discoloration of, the resistor. If the short is prolonged, the resistor will bum out. An open or shorted cathode bypass capacitor (Cl) will not necessarily produce a no-output condition; however, if cathode resistor R2 is open, no output will be obtained.

capacitance checker. Using a VTVM or voltmeter

If there is no plate voltage, coil L1 or the RFC may be open (be certain to check the supply voltage to ascertain that the power supply is not defective). If plate bypass capacitor C4 is shorted, the plate supply will be dropped across the RFC, which will heat up and bum out. Coil and RFC continuity can be checked with an ohmmeter *with* the *power off.* 

Usually, a millimeter is provided in transmitters for measuring the plate current (or a meter can be connected in series between the plate supply and the RFC.) No plate current indicates loss of supply voltage or an open circuit (either in the meter or in the plate circuit). If no dip in plate current can be obtained as C3 is tuned through resonance, either C3 is shorted, there is no drive, or L2 is partially shorted. If the plate current is low and C3 can be dipped properly, but no output exists, output coil L2 is open.

**Reduced Output.** Excessive bias, insufficient screen or plate voltage, lack of drive, or a defective tube can cause reduced output. Check the bias, plate, screen, and supply voltages with a voltmeter. Low screen voltage will cause insufficient plate and screen current, and will result in low bias and reduced output. Low plate voltage with normal screen voltage will cause the screen to act as a partial plate; the screen may run hot, depending on the value of plate voltage. This can result from a high resistance in the plate circuit caused by a poorly soldered connection, or from a defective tube.

If C3 cannot tune L1 to resonance at the output frequency, a reduced-output condition will be obtained. This can result from a lack of sufficient inductance in L1, caused by a shorted turn, or by a short or open in C3 itself. A check with a grid-dip oscillator, or a wavemeter, will reveal whether the tank circuit is resonant at the wrong frequency.

A leaky or shorted input capacitor (C<sub>c</sub> will place a positive bias on the grid and cause larger than normal plate current to be drawn; at the same time the cathode bias will be increased, so that the effective plate voltage will be reduced. Depending upon the amount of leakage voltage applied to the V1 grid, the output will be reduced, and because the operation is at the bottom of the transfer characteristic curve, the positive signal peaks will be clipped by plate current saturation, causing some distortion in the output. If R1 opens or becomes too high in value with age, coupling capacitor C<sub>c</sub> will charge through V1 when the grid is positive with respect to the cathode, but cannot discharge except through existing leakage paths; therefore, the capacitor will tend to accumulate a negative charge and block V1 from operating. Actually, when C<sub>c</sub> is charged, no further grid current flows. When the input signal becomes negative-going, C<sub>c</sub> discharges through the high shunt leakage paths in the tube and grid circuit, producing a negative bias.

Since the capacitor cannot completely discharge before the next conduction period, it eventually accumulates sufficient charge to hold the grid at cutoff.

Distortion and Other Effects. The buffer amplifier is subject to all forms of distortion common to other r-f amplifiers, except that buffer operation usually implies the amplification of only a single radio frequency. Since tuned tank circuits are used, any tendency toward distortion is usually swamped out by the tank. The tuned tank also minimizes any distortion caused by multiples of the original frequency, or harmonics. Although harmonics exist, they are not selected by the tuned circuit and are greatly attenuated in the output. Clipping and bottoming can cause a tendency toward peak flattening, but the tank circuit tends to supply the energy during the cutoff periods. Thus, the usual effect is to produce a reduction in amplitude and to retain the sinusoidal waveform. When the buffer also acts as a power amplifier, this reduction in distortion may not be obtained to as large an extent. Normally, no neutralization is required; however, it is possible to change the lead dress during repair and cause external feedback because of inductive or capacitive coupling between the relocated leads. Do not change the lead dress of r-f amplifiers unless absolutely necessary.

# TUNED COMMON-BASE R-F AMPLIFIER

### Application.

The tuned common-base r-f amplifier is used in receiver input stages to provide low noise, and good selectivity rather than high r-f gain, and to eliminate images and spurious signals in superheterodyne receivers.

#### Characteristics.

Uses common-base configuration.

Uses fixed bias (except when automatic gain control is employed), although self-base applications may be encountered.

Uses a single-tuned tank circuit to provide selectivity.

Transistor gain is less than unity, but tuned resonant circuits provide some gain.

Does not require thermal compensation.

Because of lower output capacitance, is operable at higher frequencies than any other configuration.

Usually requires neutralization or unilateralization to prevent oscillation.

# Circuit Analysis.

**General.** Because of its lack of gain, the tuned common-base r-f amplifier is generally used as an isolation stage between the antenna and mixed stage, particularly in medium-frequency (broadcast) receivers. While the tuned circuits offer some increase in signal gain, the transistor gain is always less than one. Since images and spurious signals are not discriminated against in receivers having their inputs coupled to the mixer stage, the selectivity and noise reduction effects of the tuned r-f amplifier provide better performance.

Because of the low base-collector capacitance in r-f transistors, the common-base circuit is usually used for very high frequencies (the shunt output capacitance is much lower, and better performance can be expected). With the base grounded, a low base circuit resistance exists, and thermal compensation is usually omitted. The common-base circuit is also considered to be inherently unstable over the entire range of operation, so that neutralization or unilateralization networks are used to prevent oscillation.

Circuit Operation. The accompanying schematic illustrates a typical common-base r-f amplifier using fixed base bias. For simplicity of circuit discussion, it is assumed that no automatic-gain-control (ACC) voltage is applied. (ACC circuits are discussed in the Mixing, Heterodyning, and Automatic Control Circuits Section.) The tuned input circuit consists of parallel-resonant tank Ll, Cl, with the antenna tapped at the lower end for proper input matching and maximum power transfer. The circuit is arranged for negative ground, which allows both tuned circuit tanks to be grounded in order to avoid body capacitance effects. The input tank is coupled to the emitter by capacitor C2 thus avoiding shunting of the emitter to ground through the low value of dc coil resistance. The emitter dc return is completed by R1. This is essentially shunt feed bias. While RI could be replaced with an r-f choke (shown in dotted lines in the figure), it is made resistive to avoid "dead spots" caused by any spurious resonances formed by the stray and element capacitance with the RFC, since the stage usually must be tunable over a wide range of frequencies. Fixed voltage divider bias is provided by R2 and R3. (See the introduction to this section for a discussion of base bias.) C5 places the base at r-f ground and removes the dc bias circuits from the radio-frequency path, so that the initial bias is unaffected by signal variations. Output tank C3, L4 is tuned to obtain maximum selectivity, and the collector output is matched to the base of the next stage through r-f transformer secondary L5. The tuned circuit is placed in the primary rather than the secondary, since tuning the secondary would tend to shift the phase relation ships between the primary and secondary. Thus, feedback loop  $C_N$ ,  $R_N$ , provided for neutralization and cancellation of internally developed feedback, remains unaffected by circuit tuning. Transistor Q1 is a high-frequency type of transistor; the case is grounded to provide further shielding and isolation between the input and output circuits. Capacitor C4 bypasses any r-f around the supply, and prevents it from entering the bias circuit.



Typical Common-Base R-F Amplifier

The functioning of the r-f amplifier is basically the same as that of an RC-coupled audio amplifier, with tuned tank circuits L1, Cl and L4, C3 acting in place of the emitter and collector resistors, respectively. The difference is that the operation occurs at radiofrequency rates rather than audio-frequency rates. Instead of the amplitude of the audio signal itself causing the emitter and collector currents to vary; it is the amplitude of the r-f envelope at any particular instant which causes these currents to vary. In the case of modulated emissions, the modulation varies the amplitude of the r-f envelope in proportion to the modulation. Thus, the received signal can be considered as an r-f carrier which rises and falls sinusoidally in accordance with the amplitude of the modulation, and is amplified exactly as if it were a single audio frequency, assuming that the input and output circuits are properly tuned and have the required bandwidth. If these conditions are not met, the r-f envelope becomes distorted; that is, a differently shaped signal is formed. The r-f envelope is produced by individual radio-frequency signals varying above and below the zero carrier level. Each cycle produces equal positive and negative alternations, and causes the transistor bias to be increased and decreased equally. The average value over a half-cycle of modulation determines whether the total effect is that of an increased or a decreased signal. Thus, the tips of the r-f pulses trace out a relatively slowly varying signal, which is the audio (or other) modulation, and occurs at an audio (or other) rate-not an r-f rate.

Depending upon the rapidity of rate of change of the audio modulation, a few of the r-f cycles could be lost without significantly affecting the over-all modulation waveshape. The accompanying illustration shows the concept of an r-f envelope and the manner in which it is formed, using a single carrier frequency and a single 400-Hz sinusodial modulation frequency for ease of explanation. Other more complex waveforms also produce a similar result, which can be demonstrated by a mathematics analysis beyond the scope of this handbook.



Development of an R-F Envelope

With no signal applied, Ql rests at its quiescent value of emitter and collector current as determined by base bias divider R2, R3, together with emitter resistor R1 and collector resistor R4, Since the quiescent current is steady, no output is produced. When a signal is applied to L1 from the antenna, a large resonant voltage is developed across tank L1, Cl, and is applied through C2 to the emitter of Q1. For ease of discussion, the input tank can be considered as an r-f generator connected between emitter and ground, with an output amplitude equal to the r-f envelope of the signal.

Assume that the input signal amplitude is increasing and becoming more positive, and that the instantaneous value of the signal adds to the emitter bias. As the emitter bias increases in a forward direction, the emitter and collector or current increase. Internally in transistor Q1, there is a flow of holes from emitter to collector; externally, the flow consists of electrons from emitter to collector. A small base current flows from base to emitter (through the base junction), through blocking capacitor C2 and tank Ll, Cl to ground, and through C5 to the base. The collector current flow is from ground through R4 and tank L4, C3 to the collector, and through the collector-to-base junction and C5 to ground. Note that in the common base circuit the collector current is always less than the emitter current ( $\mathbf{u}_{L} = \text{IE-IB}$ ). When the collector current increases with a signal, a large voltage drop is produced across the output tank impedance, thus developing a positive output signal (the common-base input polarities are identical). Since the L5 secondary is coupled to the L4 primary, current flow through the primary induces an output voltage in the secondary by transformer action. The secondary by transformer action. The secondary output may be either in-phase or out-of-phase, depending upon the connections.

Assume now that the input signal amplitude decreases and goes negative. The emitter forward bias is reduced and less collector current flows. As the input signal goes negative, the collector voltage rises toward the supply value. Since the collector is reverse-biased by the negative supply, a negative output signal is produced. Collector resistor R4 prevents large positive swings from dropping the collector voltage pass zero, and causing an overshoot which would drive the collector positive and produce a forward collector bias with consequent high current pulse and distortion, by limiting the total available supply voltage. Thus, a large signal can drop the collector voltage to zero, but the supply voltage will still be less than zero by the drop in R4. (This resistor may not be used in some circuits.) Capacitor C6 bypasses the rf around R4 so that it remains unaffected by signal variations, and in effect grounds tank capacitor C3 to avoid body capacitance effects when the capacitor is tuned.

Neutralizing network  $C_N$ ,  $R_N$  is connected between the secondary of the output transformer and the emitter so that it feeds back an out-of-phase voltage to the emitter and prevents oscillation due to internal feedback within QI. In r-f amplifiers operating over large frequency ranges, this neutralizing network is usually replaced by a more complicated unilateral ization network. Thus, the input circuit remains unaffected by any changes in output, or tuning, over the entire range of operation.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of volt-ohmmeters. Be careful also to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

When checking r-f voltages, always, always use a vacuum-tube voltmeter (VTVM) or an electronic voltmeter with an r-f probe. The conventional voltmeter only indicates dc. Therefore, it is necessary to first rectify the r-f before the voltmeter will indicate properly. This is done automatically in the VTVM, and separately by the r-f probe when the electronic voltmeter is used.

No Output. No input signal, a shorted input or output tank, an open emitter circuit or defective transistor, as well as improper bias, can cause no output. If R1 is open, the emitter circuit will be open, and if R4 is open, the collector circuit will be open; in either case there will be no output. If R2 is open, Q1 will operate at approximately zero bias and no output will occur except for extremely strong signals. Check the dc voltages on QI to determine the bias. With a normal supply voltage, for a PNP transistor (with negative ground), all voltages will read positive with respect to ground. The emitter will always be a few tenths of a volt more positive than the base, and the collector will read the lowest (sometimes zero). For example, if R4 were shorted, L4 would be connected to ground, the collector would be at ground potential, and the meter would indicate zero, even through full collector voltage would still be applied.

The tank coils can be checked for continuity with an ohmmeter to determine whether they are open; they must be disconnected when the tuning capacitors are checked. If coupling capacitor C2 is defective, there will be no output. If C2 is open, the emitter voltage will be normal, but there will be no output. If C2 is shorted, the emitter voltage will be low (depending on the resistance of RI), and no output will be obtained. In this case RI will get hot and possibly burn out.

If bypass capacitor C4 is shorted, the supply will be shorted, with consequent loss of output; if the capacitor is open, only a reduced output may occur. If capacitor C5 is open, the base will be connected to

ORIGINAL 491-044 () 73 - 32 ground through the bias network, and the r-f signal between emitter and base will be attenuated (depending upon the frequency) and will produce either a very weak or practically no output at all. If L5 is open, no output will be obtained (provided that the capacitive coupling between the primary and secondary is very small. Oscillation caused by a defective neutralizing network, if sufficiently strong, can bias off and block the transistor and thus reduce the output to zero. Check the value of  $R_{\text{N}}$  with an ohmmeter, and check  $C_{\text{N}}$  with a capacitance checker.

Defective r-f tanks can cause a no-output condition. Defective tanks are most easily located in an operating amplifier by observing whether they tune to a specific frequency, particularly when the tuning dial is calibrated, since any change in component values will change the resonant frequency. If the circuit bias voltages appear to be normal and there is no output, connect a modulated r-f signal generator to the antenna, the emitter, the collector, and the output winding, successively. If the input circuit is defective, the signal will appear when the generator is connected to the emitter. If the transistor is defective, the signal will appear after the generator is connected to the collector. With a defective collector tank, the signal will appear when the generator is connected to the output winding. If the signal does not appear, the output coil is open.

It is important to keep in mind that any slight capacitive coupling at radio frequencies will pass a weak signal, so that a weak output is possible under circumstances which at audio frequencies would be impossible. Thus, where more than one r-f stage is used, it is possible to have a "dead" input stage and yet, through stray capacitive coupling, obtain sufficient signal "leak-through" into the following amplifier to produce a weak output.

Low Output. Low output can be caused by improper bias or supply voltage, a defective transistor, high seties resistance or impedance, or a low shunting impedance or resistance. The bias and sup ply voltage can be checked with a voltmeter. If the value of R1 increases, the emitter bias will be increased, and if the value of R4 increases, the collector voltage range will be reduced; both cases will cause reduced output, and can be checked by use of an ohmmeter. If C5 opens, the base return to ground will be through R3, which places it in series with the input signrd; thus the input signal will be reduced, as well as **the** output signal. High resistances produced by poorly soldered connections can also cause reduced output. Applying a hot iron to the defective joint will usually restore operation to normal. If RI deteriorates to a very low value, the input signal will be partially shunted to ground and the output will be reduced. No current gain is obtained through transistor in the common-base circuit, since the collector current is always less than the emitter current by the amount of base current. Nevertheless, when low impedance is used in the input and high impedance in the output, a relative voltage gain will be obtained because of the greater voltage drop across the larger impedance.

Distorted Output. Receiver r-f amplifiers are operated Class A to avoid distortion. If the bias is too high the peaks will be clipped, or if the bias is too low a similar effect will be caused by overdriving, and saturation will occur on strong signals; both effects are forms of amplitude distortion. If the selectivity is too sharp, frequencies outside the bandpass will be cut off entirely or partially attenuated. Thus, on modulated signals some of the sideband frequencies will be lost, and frequency distortion will occur because of the loss of some of the audio signals. Normally, deterioration of parts caused by aging, moisture absorption, etc, will produce a reduction in the tuning circuit Q, and thus result in reduced performance and decreased selectivity, but this will not cause distortion. On the other hand, parts value changes can cause regeneration (positive feedback) at certain frequencies or over a range of frequencies. Such feedback increases the sharpness of tuning and can cause distortion due to sideband cutting. The prime cause is failure of the neutralizing or unilateralization network. Such effects can also be caused by a defective transistor. First check the neutralization network for proper component values, and then check the supply and bias bypass capacitors. In multiple-stage receivers, common impedance coupling can occur through deterioration of the power supply bypass capacitor, thus producing unwanted feedback similar to that encountered in electron tube operation.

Distortion caused by "cross modulation" from strong local signals sometimes exists, and is primarily a fault in design (lack of sufficient selectively) or the result of too close coupling to the antenna, which produces **fundamental** overload. Thus, saturation occurs, and the nonlinearity produced causes the unwanted signal to appear on the desired signal as cross modulation. This effect is most noticeable when operating in the immediate vicinity of strong shore or ship stations. It cannot be remedied by normal parts replacement, but rather by external means, such as changing the input and antenna coupling or inserting a loss network at the input.

#### TUNED COMMON-EMITTER R-F AMPLIFIER

#### Application.

**The** tuned common-emitter r-f amplifier is universally used in receivers and test equipment to provide high r-f gain and selectivity, and to eliminate images or other spurious responses.

#### Characteristics.

Uses common-emitter configuration.

Uses fixed bias (except when automatic gain control is employed), and some self-bias combinations may be encountered.

Transistor provides high gain (100 or better).

Usually requires thermal compensation.

Requires neutralization or unilateralization only at the lower r-f frequencies, since it is inherently stable.

# **Circuit** Analysis.

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General. The large collector-to-base capacitance of the transistor tends to shunt the output to ground, when connected in the common-emitter configuration. Therefore, the amplification tends to drop at the higher radio frequencies. On the other hand, a small change in base current causes a very large relative change in collector current. Thus, the small signal input controls a large current which develops the output voltage; this action is similar to electron tube operation using the grounded-cathode configuration. Although the output impedance of the commonemitter circuit is not as high as that of the commonbase circuit, the large collector current flow through a moderate output impedance produces a much larger output. Hence, the cornmorwnitter circuit always gives a large gain. Even at the higher radio frequencies where the gain drops off, it may be possible to obtain sufficient gain over that of the common-base circuit to justify use of the common-emitter circuit instead.

The common-emitter circuit also has a higher input impedance than that of the common-base circuit (on the order of a few hundred ohms). Consequently, it is easier to match the input (and the output) circuit for efficient power transfer. As a result, the common-emitter circuit, rather than the common-base circuit, tends to be used universally.

Circuit Operation. The accompanying illustration shows a typical tuned r-f amplifier using the common-emitter configuration. L1 and C 1 form the input tuning circuit, with both the antenna and the base tapped onto L1 to provide a proper impedance match. Capacitor C2 bypasses the lower end of L1 to ground for rf, and also bypasses bias resistor R1. Fixed base bias is provided by voltage divider Rl, R2. (See the introduction to this section for discussions of bias and bias stabilization.) Thermal stabilization is provided by emitter swamping resistor R3 bypassed by C3. The output tank consists of C4 and L2, with the supply voltage fed at approximately the center of the coil. Thus, an out-of-phase voltage is obtained and fed through  $C_N$  for neutralizing the transistor. L2 is also tapped at appropriate points to match the collector and the output circuit. The output is capacitively coupled through CCC. Capacitor C5 functions to bypass rf around collector resistor R4 and the supply, and also to maintain the center of the coil at ground potential, in order to insure the proper phase relationships between the ends of the tank coil. R4 is a voltage-dropping and isolation resistor in the collector circuit (it is not always necessary to use R4).



**Typical Tuned Common-Emitter R-F Stage** 

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Operation of the tuned common-emitter r-f amplifier is very similar to the previously discussed R-C coupled audio amplifier using the common-emitter circuit, with the tuned tank circuits replaced by resistors. The basic difference is that the audio amplifier operates at low frequencies with relatively slowly varying signals, whereas the r-f amplifier operates at much higher frequencies and follows the relatively slowly varying envelope amplitude when modulated. When not modulated, continuous-wave signals within the bandpass of the tuned circuits are amplified equidly on the positive and negative half< ycles and vary in amplitude with the average amplitude of the input signal. Thus, as the signal fades in the output signal is larger, and as it fades out the output signal is smaller. The action, meanwhile, occurs at the r-f rate; for example, a continuous r-f signal of 30 megahertz requires a time of only one thirty-millionth of a second to complete one cycle of operation.

At the start of the cycle of operation the transistor is resting in a quiescent condition, with the collector current determined by the dc base bias, which is fixed for a specific supply voltage by voltage divider resistors RI and R2. It is usual practice to bias the base negative with respect to the emitter (forward bias). The difference in potential is normally only a few tenths of a volt, and is set at the center of the forward transfer characteristic curve for Class A operation. Since the received signal is normally on the order of microvolt, the low bias value is adequate to prevent overloading (except in the case of strong local signals). Either automatic or manual gain control is usually provided in practical r-f stages to accommodate large signals; this is not shown in the schematic, to avoid circuit complication and for ease of discussion. (See the Mixing, Heterodyning, and Automatic Control Circuits Section for the functioning and operation of semiconductor automatic gain control circuits.)

Assume that an r-f signal within the bandpass of the tuned input (tank) circuit, consisting of L1 and Cl, appears at the antenna. With the antenna tapped onto L1 at the proper number of turns to match its impedance, the low-impedance antenna resistance is transformer by autotransformer action to match the large parallel resonant impedance of the tank. Thus, maximum signal transfer from the antenna to the coil is obtained. In turn, the base is also tapped onto L1 for a proper impedance match, to change the low input resistance offered by the common-emitter circuit to a value that more closely matches the high impedance of the tuned input circuit. With bypass capacitors C2 and C3 effectively grounded the bottom of L] and the emitter, respectively, as far as rf is concerned, the tuned input circuit is connected between the base and the emitter. Thus, the r-f signal does not flow through the bias voltage divider or the emitter swamping resistor (R3).

Assume, for the moment, that the input signal is swinging negative and adds to the forward base bias, thus producing an increase in collector current, (which is a flow of electrons from the supply through L2 to the collector). Application of the instantaneous negative signal voltage to the base of Q1 causes a flow of holes from emitter to base. This is the same as a flow of electrons from base to emitter, and a circulating base current flow occurs from the emitter through C3 to ground, and through C2 and the lower portion of L1 back to the base. On the positive half of the input signal the forward bias is reduced, and the collector current, likewise, is reduced. Electron flow and base current flow are through the same path as given previously for the negative half-cycle, but is diminished in value. With equal positive and negative swings, an average value of base current flow occurs, and varies in accordance with the signal amplitude. The collector current follows, but it is larger in amplitude since it is approximately equal to beta times the input signal.

Since the input tank circuit is tuned to the frequency of the incoming signal, only r-f signals within the bandpass of the tuned circuit appear at the base and affect the collector current. The amount of selectivity of the tuned circuit depends upon the unloaded Q of the tank. When this Q is high, the tuned circuit is highly selective, and only a narrow band of frequencies is accepted by the tuned circuit. Thus, the base current is controlled by the tuning of the tank circuit. When the tank circuit is resonant to the signal, a base current is injected into the transistor; when it is nonresonant, only the dc (bias) value of base current flow exists.

In the collector circuit, the load impedance across which the output is developed consists of tuned tank circuit L2, C4. Coil L2 is bypassed to ground for rf at the supply voltage tap by C5. Thus, the rotor of tuning capacitor C4 can be grounded to avoid body capacitance effects when tuning. The portion of L2 \_

between the supply and the lower end of L2 forms a neutralizing winding, which furnishes 180-degree phase shift and supplies an out-of-phase voltage back to the base through  $C_{N}$ . Thus, the effect of the tuned input and output circuits being coupled through the transistor collector-to-base capacitance and the internal base spread resistance of Q1, which causes positive feedback and oscillation, are cancelled out. This type of neutralizing circuit is similar to the Hazeltine neutrodyne method used with electron tube operation. Since the output impedance is the low input resistance of a following common-emitter stage; the coupling capacitor is tapped at some intermediate valuelof turns ratio between the supply and collector taps. Thus, a step-down ratio is provided to match the transistor output for maximum power transfer and gain. The collector is also shown tapped down on L2 for proper matching, assuming that the tuned tank impedance is higher than the collector impedance. This is usually true at low r-f ranges; however, at high radio frequencies, such as in the UHF region, the tank and collector impedances may be of the same order, in which case the collector may be connected to the top of L2. (In some circuit versions a deliberate mismatch may be arranged and the neutralizing arrangement dispensed with.)

Regardless of the impedance-matching or neutralizing methods used, however, the output signal is developed across the impedance provided by the parallel tuned tank circuit. At resonance the impedance is high, and off resonance it is a lower value. Thus, for frequencies within the bandpass of the tuned circuit, the impedance is high, and a large voltage drop occurs across this impedance. With a negative-going input signal the collector current flow causes a drop across the parallel-tuned tank which reduces the collector voltage toward zero. Since the collector is reversebiased, the output is positive-going. When the input signal swings positive, the forward bias is reduced. which reduces the collector current also. Less voltage drop occurs across the output tank, and the collector voltage increases in a negative direction, thus producing a negative output signal (common-emitter output and input polarities are always opposite). These positive and negative signal excursions occur at an r-f rate. For a constant-amplitude input, a constant, amplified output signal is developed. If the signal is modulated, the output amplitude follows the waveform envelope, and the output amplitude varies in accordance with the modulation. With signal

swings less than the applied base bias, no distortion is produced. If the input signal is greater than the bias, or if the collector voltage is dropped to zero before the peak occurs, then clipping and distortion effects are produced. Resistor R4 is used to drop the collector voltage to the proper value and to act as a decoupling resistor. It also prevents the collector voltage from being driven positive by strong signals, which would forward-bias the collector and cause heavy current flow with distortion. The transistor case is grounded to provide better shielding and prevent r-f feedback.

Normally, swamping resistor R3 is affected only by slow dc variations of emitter current caused by ambient temperature changes. The increased emitter current flow with temperature produces a voltage R3 which opposes the bias voltage and reduces the emitter current back to its original value. Any r-f signal is bypassed across R3 by C3. This is conventional emitter swamping action.

The output is shown capacitively coupled since it is **usually** more economical than providing a secondary winding to couple out of L2, plus the fact that at high frequencies it is sometimes difficult to obtain optimum coupling between windings because of high-frequency effects. Any of the tapped tanks shown in the schematic can be replaced by tuned transformers without any change in operation, if they have sufficient coupling, if they tune to the same frequencies, and if they tune over the same range. Circuit cost and designer's preference usually determine which are used.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low-voltage ranges of volt-ohmmeters. Be careful also to observe polarity when checking continuity **wit**<sub>11</sub> the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

When checking r-f voltages, always use a vacuurntube voltmeter (VTVM) or an electronic voltmeter with an r-f probe. The conventional voltmeter indicates only dc. Therefore, it is necessary first to rectify the rf before the voltmeter will indicate properly. This is done automatically in the VTVM, and separately by the r-f probe when the electronic voltmeter is used.

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No Output. Open base, emitter, or collector circuits or short-circuited input or output circuits, as well as lack of supply voltage or a defective transistor, can cause no output. If either L1 is open or C 1 is shorted, no output will be obtained. If LI is disconnected from Cl, both the continuity of L1 and the shorting of Cl can be checked with an ohmmeter. Lack of supply voltage as well as bias voltage can be determined by use of a voltmeter. Proper base bias indicates that the bias divider and lower part of L1 are connected to the base. Likewise, proper collector voltage indicates that R4 and L2 are satisfactory and that tuning capacitor C4 is not shorted. If C5 is shorted, the full supply voltage will be dropped across R4, and there will be no output. If coupling capacitor CCC is open, no output will be obtained (although there is a possibility that a strong signal may still feed through as a weak signal by stray capacitive coupling). If emitter resistor R3 is open, there can be no output. If neutralizing capacitor  $C_{N}$  is open and the feedback is sufficient, the transistor may be blocked, with consequent loss of output, although it is more likely that a low output with squeal and distortion will be obtained. However, if C<sub>N</sub> is shorted, the base and collector will be shorted through the neutralization coil and no output will be obtained.

Normally, the collector voltage will be lower than the supply voltage **because** of the drop across R4. A high collector voltage will indicate improper bias on the base, or lack of collector current due to a defective transistor or an open emitter resistor (R3).

Low Output. If the forward bias is too low, if the collector voltage is low, or if the transistor gain has deteriorated, a low output will be obtained. Highresistance soldered connections in the input and output tanks or nonresonance can also cause a reduction of the output. If emitter resistor R3 increases in value or bypass capacitor C3 opens, the output will likewise be reduced by emitter degeneration effects. The bias and collector voltages can be checked with a voltmeter, and R3 can be checked with an ohmmeter. An open bypass capacitor C2, C3, or C5 can cause a reduction of the output through loss of r-f signal in the bias and supply circuits and by emitter degeneration; a bypass capacitor can be quickly checked by temporarily shunting an equivalent capacitor across it. An increase in output when this is done indicates that the original capacitance is insufficient. To determine that the tuned circuits are operating properly, insert a modulated signal from a signal generator

into the antenna, and use an oscilloscope with an r-f probe to determine whether the signal appears at the base and the collector. Tuning the tank circuits will cause the signal to increase in amplitude at the resonant frequency. If the tuning has no effect, the tanks are open or shorted and must be disconnected and checked individually. When the circuit components appear to be operating normally and the output is low, the transistor is probably defective.

When AGC voltage is fed into the base circuit to control the volume automatically, do not neglect the possibility that too great an AGC voltage may be biasing-off the stage. With a properly functioning circuit, the AGC voltage will vary in accordance with the strength of the input signal, or with the tuning, as the desired signal is selected. With delayed AGC it is normal for the AGC bias voltage to be almost zero with weak signals so that full sensitivity is obtained.

Distorted Output or Poor Selectivity. If the bias is too high or too low, the signal may be clipped by operating at or near saturation or cutoff, respectively. If there is excessive regeneration at some frequency, the tuning may be sharpened sufficiently to cause sideband cutoff, and frequency distortion will result from the loss of original frequencies now outside the reduced bandpass. Poor selectivity (broad tuning) is usually caused by high resistance in the tuned circuits due to poorly soldered joints or aging. A lowering of the tuned circuit Q can also cause a broadening of the selectivity curve and reduce the apparent gain. With calibrated dials, reception of the signal at the wrong frequency indicates a change in circuit constants in the tank, or a change in the stray and distributed shunt capacitance in the tuned circuit. Usually, a readjustment of the trimmer capacitors will restore the calibration to normal. It is particularly important while repairing or trouble-shooting r-f circuits not to disturb the lead dress or reroute the wiring; otherwise, a change in stray capacitance (or inductance) will cause improper tracking of the tuned circuit. Moisture absorption in coils and dielectrics plus aging effects can cause a loss of Q, which can be restored only by replacing the tuned circuits or by removing them and baking them in an oven to remove the moisture. A salt spray film can cause a low shunt resistance across a tuned circuit and require washing and drying to provide normal results. In receivers using multigang tuning capacitors, it is common for the oscillator to become detuned and off-calibration enough that the signal is outside the r-f bandpass of

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the tuning capacitor in the r-f and mixer stages. A 10ss of gain, cutting of sidebands, and distortion can result.

# SINGLE-ENDED R-F AMPLIFIER (ELECTRON TUBE) (CLASS B OR C)

# Application.

The single-ended Class B or C r-f power amplifier is used universally as an intermediate r-f power amplifier (driver) stage, or output (final) amplifier for transmitters, and in special instances for test equipment. (Normally, receivers and test equipment use Class A amplifiers.)

#### Characteristics.

Uses either Class B or Class C bias.

Output efficiency varies with bias; approximately 50 to 60 percent for Class B operation, and 70 to 75 percent for Class C operation.

Uses a tuned r-f tank circuit to develop the output frequency.

Is neutralized for triodes, but not for pentodes or screen-grid tubes.

Input frequency is usually the same as the output frequency.

Provides high output power and current gain.

Requires grid drive power equivalent to approximately 10 percent of plate output power, or less, depending upon type of tube used.

Normally uses fixed bias, but can also use self (signal) bias and protective cathode bias, or a combination of both.

### Circuit Analysis.

**General.** The alternating component of plate current in a Class B r-f amplifier is proportional to the amplitude of the input (exciting) signal. Therefore, the power output varies as the square of the excitation (drive) voltage. Normally, in CW operation, maximum drive and maximum output are used. When used to amplify a modulated r-f signal, the output must vary linearly with the input so that no distortion is produced; also, the output varies in amplitude in accordance with the modulation. Consequently, for operation as a linear r-f amplifier, more stringent limits must be placed on bias, excitation, and plate voltage than for CW operation. In addition, to allow for the constant load and provide an overload safety

factor, the stage is usually operated at a 20 percent reduction in rated maximum (CW operation) power. (Since the CW stage is keyed, it does not operate at full power continuously, and can therefore be used at the higher ratings without damage.) Other considerations which are applicable to the modulated Class B linear amplifier will be discussed at the end of this article, since slightly different operating conditions are necessary to provide for modulation amplitude increases.

The Class C r-f amplifier is similar to the Class B r-f amplifier, except that it operates at a much higher grid bias, it requires correspondingly greater excitation with more drive power, and it usually operates a higher plate voltage and current. As a result, greater output and efficiency are obtained. In the Class C stage the alternating component of plate voltage is directly proportional to the plate voltage (not the grid voltage as in Class B operation). Thus, the output power is proportional to the square of the plate voltage. This is why high-level modulators vary the plate voltage of the Class C r-f amplifier stage to pro. duce amplitude modulation.

**Circuit Operation.** The schematic of a typical Class B or C triode r-f power amplifier is shown in the accompanying illustration.



class B or C Triocle R-F Power Amplifier

Although pentode, tetrode, or beam-power tubes could have been used in place of the triode, the triode is used here for ease and simplicity of discussion. Considerations involving other types of tubes will be

discussed at the end of this article. The input circuit is shown capacitively coupled by CC, although any other form of coupling could be used instead. Grid bias (in addition to bias from the fixed supply) is produced by the driving signal, which causes rectified grid current flow through R1; RFC1 prevents shunting of the drive signal to ground via R1. (Protective cathode bias is sometimes provided by cathode resistor  $R_k$  bypassed by  $C_k$ , and is shown in dotted lines since it may not be used. When it is not used, the cathode is connected directly to ground.) See the introduction to this section for a complete discussion of cathode bias and shunt grid-leak (signal) bias. The tuned plate tank consists of Cl and L1, with output link coil L2 inductively coupled to it (capacitive coupling or another form of coupling such as a Pinetwork is sometimes used instead of L2). The plate voltage is series-fed through RFC2, which is bypassed by C2 for rf (shunt plate feed is also often used). This arrangement ensures that any rf at the center tap on L1 is bypassed to ground through the low-impedance path offered by C2 rather than the high-impedance path offered by RFC2 and the power supply filter capacitor. With the center of L1 grounded, both ends of the coil are at opposite and equal potentials. Splitstator tuning capacitor Cl maintains the balanced arrangement, and permits the rotor to be grounded in order to avoid body capacitance tuning effects (shunt plate feed permits the capacitor and coil to be directly grounded). A neutralizing voltage is taken from the end of the tank opposite the plate, and is fed back to the grid through capacitor  $C_{p}$ . In this plate neutralization method, C<sub>n</sub> effectively forms part of a bridge circuit which balances out the plate-to-grid interelectrode tube capacitance and prevents feedback and self-oscillation of V1.

As is evident, the schematic is similar to that of a neutralized r-f voltage amplifier, which has been previously discussed in this section of the handbook. The difference in operation is due to the use of cutoff bias, greater drive, and short pulses of plate current conduction, which provide greater power output. Class B and Class C amplifiers are discussed separately in the following paragraphs because of the differences in their operation.

class B Oparation. Normally, VI conducts for only a portion of a cycle, usually for 180 electrical degrees, but not less then 160 degrees (otherwise, the

operation becomes Class C). The tube is supplied with energy from the tank circuit during the nonconducting portion of the cycle, which provides a so-called "flywheel effect" to keep the circuit oscillating despite the absence of plate current flow for the nonconducting half-cycle of operation. Thus, the r-f output is continuous and a steady output signal is maintained, as long as the key is down. (In Class B audio (untuned amplifier) operation, another tube is needed to supply the energy for the negative half-cycle.)

When the drive signal (r-f excitation) is applied through CC, the grid of VI is momentarily driven positive when the positive half-cycle of input signal exceeds the fixed negative bias voltage, and both plate current and grid current flow during this interval. Plate current flow is not continuous throughout the cycle, but is in the form of short pulses of energy, one for each cycle. During this time dc grid current flows from ground to the cathode and charges Cc, when the input goes negative, C<sub>c</sub> discharges through R1 back to ground. Electron flow is in the direction which makes the grid end of R1 negative, thus producing a signal bias. Radio-frequency choke RFC1 presents a high impedance to the exciting r-f signal and presents it from being shunted to ground through R1. Thus, only the rectified dc component of grid current flows through R1 to develop the bias. The amount of dc grid flow is averaged over the complete cycle to provide a steady dc bias voltage. This signal bias is in addition to the negative dc fixed bias voltage, which is applied between  $\mathbf{R1}$  (or the grid of V]) and ground. The fixed bias automatically provides protection in the event that the grid drive is interrupted, so that complete loss of bias cannot occur. The total bias is the sum of both the fixed bias and the signal bias. Regardless of the type of bias employed, the operation is similar. Tube VI does not conduct until the exicting voltage drives the grid above cutoff. Once above cutoff, plate current flows and increases as the grid voltage increases. Grid current does not flow until the grid-drive voltage reduces the total bias to nearly zero. From this point on grid current also flows, reaching its peak at the same time as the peak of plate current flow.

When plate current flows, the tuned tank circuit offers a resistive impedance at the frequency of resonance, which drops the effective plate voltage to its minimum value at the peak of the conduction cycle. d

# **ELECTRONIC CIRCUITS**

At this time the tank **circuit** absorbs energy from the plate circuit. At the same time the plate is also dissipating some energy; this plate dissipation is at a minimum, since the effective plate voltage is at its minimum also, and maximum efficiency is obtained.

As the amplitude of the grid excitation now decreases toward zero and then swings negative on the following half-cycle, the grid bias is increased and the plate current is decreased. When the plate current decreases, the voltage drop across the load (or tank impedance) also decreases and the plate voltage rises. When plate current cutoff is reached, the plate voltage is just equal to the source. However, the circuit does not cease operation, since the tank circuit contains r-f energy which is now released to the load. From the moment of cutoff until current is again drawn on the next half-cycle of operation, the tank keeps supplying the energy. This is so-called "flywheel" action of the tank circuit. During this time (when no plate current flows) the tank circuit is completing its half-cycle of operation, and the instantaneous plate voltage continues to rise until the peak tank voltage is reached. The plate voltage at this point is higher than the source or supply voltage, but, since the tube is biased far below the point of conduction, it has no effect on V1. The tank circuit now swings negative and the plate voltage drops toward the dc supply voltage. At the same time, the peak of negative grid swing is reached and the grid drive signal swings positive, thus reducing the total bias. Eventually, cutoff is passed and the tube is driven into conduction again. As the positive drive voltage increases, the effective bias decreases and plate current flow continues to increase. The plate current flow causes a voltage drop across the impedance of the load (or tank circuit), and the effective plate voltage is again reduced. Near zero bias grid current again flows, increasing to maximum at the peak of the drive signal, which corresponds with point of minimum plate voltage. The cycle now repeats over and over again as long as the circuit is completed (key is held down).

The accompanying illustration shows the manner in which the plate current varies with grid voltage. The grid-plate transfer characteristic curve is assumed to be linear. Actually, there is always a slight amount of curvature near zero bias (the bottom) and near saturation (the top). Therefore, in linear operation the bias for "projected cutoff", which is slightly different than for actual cutoff, is employed, and any curvature near cutoff is neglected (it will produce only a small amount of distortion, which can normally be tolerated). As can be seen from the figure, the plate current is proportional to the drive signal amplitude up to saturation. After the saturation region is reached, the plate current will vary only slightly for a large change in excitation until full saturation is reached, at which point there is practically no change in plate current for any further change in excitation. This is shown more clearly in the following graph, which also indicates how linearity and saturation are affected by different load impedance in the plate tank. Note that in the first curve, produced by a high load impedance, it takes less grid excitation voltage to reach saturation than for moderate and low impedances, as shown in curves 2 and 3. The closer the curve is to saturation, the nearer the output voltage is to the plate voltage. The output voltage never equals or exceeds the plate supply voltage, since the minimum plate voltage is always made greater than the peak value of the grid excitation voltage in order to prevent excessive grid current flow. If the positive grid were allowed to become greater than the effective plate voltage the grid would ten act as a plate and tend to carry all the cathode current. Besides causing grid overload and damage to the tube structure, the plate current would actually be interrupted, which is the same as if the plate were driven negative at this time, and distortion would be produced. Recall that at the peak of grid swing the plate current is greatest and rf is being absorbed by the tank circuit; thus, an interruption of current at this point cannot be tolerated

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Grid Voltage and Plata Currant Relationship for Unmodulated Class B Linear Amplifier



Saturation Curves, Showing Effeet of Load Impedanee

In CW operation it is unimportant whether or not the transfer curve is exactly linear, since no modulation is applied and maximum output with a usable waveform is all that is necessary. Any slight distortion due to nonlinearity is effectively swamped out by the

effect of the tuned tank circuit, so that approximately a sine-wave output is always supplied. Even when driven into heavy saturation the plate waveform will be satisfactory, but more drive power than is needed will be used, and the driver tube may be overloaded. On the other hand, when a modulated signal is to be amplified, it is important that the characteristic curve be linear in order to retain the shape of the modulation without distortion. The following gridvoltage, plate-current curve shows the relationship when modulation is applied. As long as the linear portion is not exceeded (the drive is adjusted correctly), no distortion exists. This is normal Class B linear operation. Should the drive be too low the output will be undistorted, but the full amplified power output will not be obtained and the efficiency will be lower than normal. Since the linear amplifier must provide four times the resting power for full 100 percent modulation capability, the carrier level is normally adjusted for half the maximum current with full excitation and no modulation. When the current doubles on the modulation peaks, the power output will vary as the square of this current, and produce a peak output four times normal. When modulated, the Class B r-f amplifier stage has stricter requirements. The grid bias must not vary with modulation; hence, only fixed bias is used and a constant plate voltage supply is required. Usually, the driver is larger than necessary for CW operation and the grid of the linear amplifier is loaded down with resistance to provide better regulation with a more nearly constant load on the driver. Since maximum plate dissipation occurs in the resting (or quiescent) condition, the efficiency at this point drops to about 33 percent, and reaches maximum efficiency at the peak of the modulating signal of about 65 percent. Since the peaks on voice modulation are of short duration, the total over-all efficiency drops (where in CW operation full power and efficiency are obtained constantly), so that a maximum of 50 to 55 percent is obtained under modulation. To ensure that the tube is not overloaded in the resting (quiescent) condition, lower plate voltage is used than for CW operation. Since Class C operation allows the amplifier to the driven harder and greater efficiency to be obtained, Class B linear operation is used mostly for amplifying lowlevel AM modulated signals. In the case of singlesideband operation, the linear Class B stage is the only type of amplifier suitable for producing undistorted amplification of the r-f sideband signal
$\sim$ 

(Class C would cause distortion). Where the modulation is developed in the output (high-level modulation), the Class C amplifier is always used.



Grid-Voltage, **Plate-Current** Relationships for Modulated Class B Linear Amplifier

Class C Operation. The Class C stage is biased far beyond cutoff (2 to 4 times), so that the conduction occurs only over a range of 100 to 120 electrical degrees of the cycle. Since plate current flows for a shorter period of time, greater efficiency is obtained (the losses are less), reaching a maximum of 75 to 80 percent. The circuit is identical with that of the Class B stage, but higher plate voltage and more grid drive are required (the bias is much higher). During the nonconducting portion of the cycle, energy is supplied to the circuit from the tuned tank, just as in the Class B stage. The operation is identical except that the plate conduction period is shorter, and the output is no longer proportional to the amplitude of the excitation signal. Instead, the output is now proportional to the plate voltage. The r-f drive is kept constant at maximum amplitude in order to drive the tube to full saturation. The Class C amplifier is also

linear, but with respect to plate voltage. If the plate voltage is doubled, the plate current is also doubled, and the power output is then four times normal.

In CW operation, maximum drive and maximum plate voltage are used to obtain a greater output. Because of the greater efficiency obtained, the power output of the Class C power amplifier for a given plate voltage is greater than that obtained from a Class B amplifier for the same plate voltage.

When a modulated signal is applied to the grid of a Class C amplifier, the amplifier, the amplifier conducts only while the signal is above cutoff, and a distorted plate output signal appears with part of the modulation cut off. This is shown graphically in the following illustration. On the other hand, if the modulation is applied in the form of an ac plate voltage which alternately adds to and subtracts from the normal dc plate voltage instantaneously in accordance with the modulation, then the modulation envelope will be reproduced without distortion, since the instantaneously varying plate voltage produces a varying output of similar waveform, as shown in the accompanying illustration.



Grid-Vdtage, Plate-Current Relationships in a Modulated Class C Amplifier

# **ELECTRONIC CIRCUITS**



Plate Voltage and Plate-Tank Current Relationships in a Modulated Class C Amplifier

Note that the tank circuit current variations produce equal positive and negative swings so that a symmetric output envelope is generated, and a minimum plate voltage greater than exciting voltage  $E_g$ always occurs. Thus, at no time is the grid voltage more positive than the plate voltage, and excessive grid current cannot flow. The following waveforms show the instantaneous voltage and current relationships in both the grid and plate circuits on the same time basis. Plate voltage variation is shown in part A of the figure, grid current and plate current variations are shown in part B and grid voltage is shown in part C.



Plate and Grid Waveforms in Class C Operation

# **ELECTRONIC CIRCUITS**

The grid bias is shown as E<sub>c</sub> and the exciting or drive voltage as  $E_g$ . The supply voltage is  $E_b$ , and the ac plate voltage drop across the load is El, which is also the output voltage,  $E_0$ . Note that  $E_{min}$  and Egmax always occur simultaneously, and that all waveforms are sinusoidal since they are developed across tuned tank circuits. (If the grid circuit of V1 does not contain a tuned tank, the effect of the driver stage tank produces the same result.) The platecurrent pulse is always much less than half a cycle, and grid current  $i_g$  flows only when the grid is positive. The total instantaneous cathode current is the sum of  $\mathbf{i_p}$  and  $\mathbf{i_g}$  (in a pentode the screen current is added). The average value of the plate-current pulse over a complete cycle is the direct current,  $I_{\rm h}$ , which is drawn from plate supply  $E_b$ . Likewise, the average value of the instantaneous grid current,  $i_g$ , is the dc grid current,  $I_{g}$  (averaged over a complete cycle). The plate input power is  $I_b \ge E_b$ . The plate load impedance is connected in series with the plate supply to develop the desired output voltage when plate current pulses flow. The output magnitude is controlled by varying the coupling of the load to the tuned plate circuit. While the plate tank appears as a purely resistive load at resonance, the actual load is the antenna and associated transmission line. When matched, this combination is resistive also, but if not properly matched it may produce a reactive effect (either capacitive or inductive), and require that the plate tank be returned to resonance. This detuning will vary with the degree of coupling to the load. The division of energy between the tuned circuit and the tube is always proportional to the respective voltage drops across them. The drop across the tuned circuit (and reflected load represents useful r-f output, while the drop across the tube resistance represents a loss of energy which is dissipated by the plate as heat. This plate loss is equal to the instantaneous plate current multiplied by the instantaneous plate voltage  $(i_{p} x e_{n})$ ; except for the small amount lost in the resistance of the tank circuit, the plate loss represents the bulk of the inefficiency, which is usually not more than 25 percent.

The accompanying figure shows the saturation characteristics of a typical Class C amplifier for different values of bias and degrees of excitation. In part A the solid curve, "A", represents Class C operation, and the dotted curve, "B", represents Class B operation. The Class B stage is always operated between zero and point 1, where saturation begins. The region is linear; that is, the output varies directly with the input. The Class C stage, however, is always operated to the right of point 1, and usually around point 2, which is in the heavy saturation region. Thus, no current flows until sufficient excitation exists to drive the tube into conduction. As the drive is increased, the current also increases quickly to light saturation at point 1. From point 1 to point 2 there is not much increase in plate current with an increase in drive, and beyond point 2 there is practically no change at all. This is the normal operating point at heavy saturation, and represents the most efficient operation. While below point 1 the output will vary with the input, it is not linear and much distortion will be produced. In part B, the start of saturation is indicated for various values of loading. The highimpedance load at X1 will require less drive than that at X2 for the medium-load impedance, and much more drive is needed to reach X3 with a low-load impedance. In each of these cases the operation is still Class C, but the plate currents, minimum plate voltages, and drive power required are all different. A small tuning capacitance (lo-C) is used to produce the high-impedance condition, while a large tuning capacitance (hi-C) is used for the low-impedance condition. The hi-C tank will also have more losses because of heavier circulating current, and, since the minimum plate voltage is also higher, the output voltage will be less and the efficiency will be at its lowest value. Part C of the figure shows the effect of gridleak bias on saturation. In this case, the operation is always set at point X to avoid distortion, loss of efficiency, and reduced output. Since the grid bias will vary with the amount of excitation, a low drive current will change the operation into the Class B region, or somewhere between Class B and Class C, with reduced output and distortion.

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Thus, it can be seen from the figure that full saturation is always required in a Class C amplifier to prevent any change in drive from affecting the output. With a saturated drive, a larger output can be obtained only by increasing the plate voltage.

Other Considerations. Beam power, pentode, and screen grid tubes are generally used instead of triodes because they require less drive and a larger output can be developed. Also, the screening effect of the screen grid provides reduced grid-plate capacitance and minimizes feedback, so that oscillation will not usually occur, and no provision for neutralization is required. Thus, an over-all saving in parts is obtained. Since the plate is farther from the grid than the screen, it is important to keep the screen voltage higher than the excitation; otherwise, the grid current becomes excessive. However, the minimum plate voltage can now be made lower, and a larger plate obtained. The limiting factor is usually the screen voltage, since if the plate voltage were made much lower than the screen voltage the screen would have a greater attraction for electrons which should go to the plate, and the screen would tend to act as the plate.

At high frequencies, where the transit time becomes an appreciable portion of the cycle, the pulses of plate current are lengthened and distorted, causing reduced output power and lower efficiency. Electrons which are in transit when the negative part of the cycle occurs are driven back to the cathode, and cause a heating effect which can result in damage to the cathode. In addition, extra driving power is required because of power lost in the grid circuit. As a result, different tube designs have been developed to eliminate or at least reduce these effects. As the frequency increases, ubterekectride lead inductance and capacitance limit the highest resonant frequency obtainable with grid or plate tank circuits. Lead losses increase and lower the highest value of impedance which can be obtained with reasonable efficiency. Hence, transmission lines are used instead, and grounded-grid circuits are employed to minimize external coupling between the grid and plate circuits, and to reduce feedback within the tube.

The application of modulation and its effect on amplifier operation and performance have been mentioned at appropriate points throughout this circuit discussion. For further information, the interested reader is referred to the Modulators Section in this Handbook, where the subject is covered in detail.

# Failura Analysis.

No Output. An open or shorted input or output circuit, is defective tube, or lack of supply voltage can cause a no-output condition. If coupling capacitor  $C_c$ is open, no grid drive will be obtained. No current will be indicated on the grid meter, and the plate meter will also read zero, since the fixed bias will keep the tube beyond cutoff. An open grid choke, RFC1, or grid resistor, RI, will remove the bias from V1; in this case sufficient plate current will be drawn to blow the plate fuse or supply breaker. Such a condition cannot occur where cathode bias is supplied by  $\mathbf{R}_{k}$ , since the tube current will be limited by the cathode resistor to a safe value. If either plate choke RFC2 or tank coil L1 is open, or if bypass capacitor C2 is shorted, no plate voltage will be applied to VI and an output cannot occur. The open-circuit condition will be indicated by no plate meter reading, while the short-circuit condition will be indicated by an off-scale deflection of the meter and the blowing of the plate fuse or supply fuse. If output coil L2 is open, no output can be obtained; the grid meter indication will be normal, with a low plate meter indication. If tank capacitor C 1 is shorted, high plate current will be indicated and a blown plate fuse will result; on the other hand, if Cl is open, a minimum plate current dip at the usual resonance position will not be obtained, and the plate current will most likely be high since the circuit is out of resonance. When driven to full saturation, detuning of the tank circuit off-resonance will usually cause excessive plate current (two or three times the normal value). Leaving the tank detuned will probably cause the plate fuse or breaker to open. This is normal, and is due to improper operation rather than a circuit failure. If neutralizing capacitor  $C_n$  is shorted, full plate voltage will be applied to the grid of V1, excessive plate current will be indicated, and the fuse or breaker will open.

Where trouble is indicated by high or low meter readings, the bias and plate voltages can be checked with a voltmeter, to be certain they are present and correct. Open circuits indicated by zero current can be checked for continuity, with the POWER OFF and the filter capacitors discharged, using an ohmmeter. Be certain to observe all safety precautions. Since the voltages used in the grid and plate circuits of transmitters are usually very high and extremely dangerous, your first mistake may be your last!

Reduced Output. Low bias or plate voltage, as well as improper drive, will cause reduced output. in modulated amplifiers, lack of sufficient filament emission or inability of the power supply to furnish full peak current will also cause a reduction in the output, with distortion. Bias and plate voltages can be measured with a voltmeter. When measuring dc voltages in r-f circuits, inaccuracies and meter burnout can occur if sufficient r-f filtering is not employed. It is the usual practice, therefore, to measure the voltages on the dc side of the circuit, and rely on continuity measurements in the r-f circuit, using plate and grid current meters and, when available, r-f tank current meters to indicate when the circuit is operating properly. Usually, low bias should be suspected when both grid and plate currents are larger than normal, and the tube plate shows excessive plate dissipation. Insufficient drive is usually found by noting that the grid current is below normal. With normal grid current, low plate current indicates either low plate voltage, improper load, or a weak tube. Under certain loading conditions where excessive reactance is reflected into the circuit, tuning for minimum dip may reveal that the dip is very broad or hardly noticeable. In this case, the tuning should be adjusted for maximum r-f output as indicated on a thermocouple meter.

When tubes other than triodes are used, the screen voltage becomes important in determining the plate current and hence the output. Make certain that the proper screen voltage is applied, and that normal screen current is obtained. Inserting a meter in the screen circuit (when a meter is not provided) will enable a more certain check on the operation. Normal screen current indicates that the trouble is elsewhere. Low screen current indicates insufficient drive or screen voltage, while high screen current usually indicates high screen voltage or a defective plate circuit. Maximum screen current at the point of minimum plate current is normal, provided that it does not exceed the rated value.

Reduced output is sometimes due to trouble in the antenna or transmission line; therefore, it is always good practice to use a dummy load when checking out the transmitter to make certain that the trouble is not outside the unit. A rough check on tube emission can be made by temporarily detuning the plate tank and immediately returning it back to the proper setting, meanwhile observing that the plate current increases considerably. It held off resonance too long, it

is possible to damage the tube. Where the tube is normally operated so that there is no trace of color, and a reduced output is obtained with color showing on the plate, a loss of efficiency is indicated, most probably involving bias and drive.

In equipment where a C battery is used to supply the fixed bias, the battery voltage should be measured with the equipment inoperative; the battery should be replaced when its voltage drops below 15 percent of the rated value.

In triode amplifiers, improper neutralization can cause reduced output and erratic operation. The neutralization should be checked when reduced output is obtained with greater than normal plate current indication, usually accompanied by increased plate dissipation. The same symptom is also possible when parasitic oscillations exist either at low frequencies or at extremely high frequencies. This should not occur in properly designed and tested Naval equipment, but sometimes will occur in off-the-shelf commercial procurements, or after repair and replacement with a part having a slightly different value. In this case a wavemeter or grid-dip meter will indicate the frequency of the undesired parasitic oscillation. If lowfrequency parasitic exist, the bias and plate r-f chokes and bypass capacitors will usually be at fault (they form a tunad tank at that frequency). If highfrequency parasitic exist, they are usually easily eliminated by installing parasitic suppressors in series with the plate lead, between the plate and the tank circuit (the closer to the plate connection at the tube, the better).

Distortion. In CW operation any distortion that exists will be in the form of harmonics; usually, on the 2nd or 3rd harmonics are of great enough amplitude to be of any importance. In this case, besides wasting some useful output, they may radiate at frequencies which may interfere with other services. Placing a low-pass filter between the transmitter and the antenna will eliminate any unwanted harmonic radiation. A reduction of the bias and drive, plus an increase in the tank circuit Q, will also minimize this type of distortion. (This is not to be considered as authorization to make unapproved changes in the equipment, but is discussed in case such conditions are encountered in the field.) When modulated, nonlinearity of the transfer characteristic and improper bias or drive will cause a distorted modulation envelope. The waveform may be observed on an oscilloscope (use an r-f probe or connect directly to the

plates); adjust the equipment so that the values used are those which eliminate the distortion. It is also important to determine that the modulation is not distorted before being applied to the amplifier suspected of being at fault. Normal oscilloscope checks will reveal the cause (compare with typical faulty waveforms).

# **PUSH-PULL** R-F AMPLIFIER (CLASS B OR C)

#### Application.

The push-pull Class B or C r-f power amplifier is used universally at high frequencies as an intermediate (driver) stage, or as the final output stage for transmitters, where a large output with reduced second harmonic distortion is required.

#### Characteristics.

Uses either Class B or Class C bias. Fixed bias is normally used, but self bias (either signal or cathode bias) may also be used; sometimes a combination of both types of bias are used.

Uses a tuned r-f tank circuit to develop the output frequency.

Output efficiency varies with bias; approximately 50 to 60 percent for Class B operation, and 70 to 80 percent for Class C operation.

Triodes require neutralization, other tube types do not.

Input and output frequencies are usually the same. Provides high output power and current gain.

Requires approximately twice the grid-drive power of the single-ended stage, and a push-pull input.

Second harmonic output is considerably reduced or eliminated.

Input and output capacitance is hrdf that of the single-ended stage.

#### Circuit Analysis.

**General.** In the push-pull configuration, the input and output capacitances of the tubes are effectively connected in series. Therefore, only about half the normal grid and plate tuning capacitance is required for a specific frequency. Consequently, high frequency tanks are easier to construct and use of this type of circuit is more prevalent on the higher frequencies (above 30 MHz) although it can be, and is, used on the lower frequencies. The push-pull grid

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input also provides a step up of input impedance of about four times over that of a single tube. Thus it is easier to drive the push-pull amplifier, since the driver stage can be more easily matched. Because two tubes are driven, twice the drive power of a single-ended stage is required. It should be noted that the Class B or C power amplifier although connected in pushpull, does not actually operate in push-pull fashion like the Class A stage. That is, instead of increasing the current of one tube while simultaneously decreasing the current of the other tube (the action from whence the name push-pull was derived), each tube operates separately. Operation occurs only during the positive portion of grid swing when the drive exceeds the bias, and plate current flow is cut off during the negative portion of the cycle as the tank circuit supplies the output. While not operating in true push-pull fashion, this circuit retains most of the advantages of the basic circuit. Since the individual plate load is one quarter the total load, low impedance triodes can be used to develop a high power output. And, although the second and even harmonic content is not cancelled out in the primary of the r-f output transformer, the even harmonics are eliminated in the output circuit (the secondary). The push-pull connection also affords a slight increase in power output; normally, 2-1/2 to 3 times the single tube rating can be obtained, particularly in unmodulated operation (CW). When triode type tubes are used, their large grid-plate capacitance causes feedback, and the circuit tends to operate like a tunedgrid, tuned-plate oscillator; therefore, triodes are always neutralized. The pentode, tetrode, or beam power tube types normally do not require neutralizing because of reduced interelectrode capacitance and better shielding. However, arrangement of components is sometimes such as to permit external coupling (particularly at high power and at high frequencies and neutralization is then necessary.

> Although cutoff bias is required, cathode bias may be used since one of the tubes is always conducting (both conduct alternately). However, since the pushpull circuit is a balanced circuit, it is usually easier to apply a **fixed** negative bias and avoid selecting or matching the tubes to get equal currents. Since grid current is always drawn, a grid leak resistor is usually connected in series between grid and ground to provide some signal bias, and reduce the voltage requirement on the separate C-bias supply.

**Circuit Operation.** The schematic of a typical triode push-pull r-f power amplifier is shown in the accompanying illustration. The triode is used for ease of explanation. Considerations for screen grid and other type tubes will be discussed at the end of this article.



Triode Push-Pull R-F Power Amplifier

Coil L1 couples the output of the driver stage to tuned input circuit L2, Cl. Grid bias is supplied to a tap on L2 from a fixed bias supply, supplemented by signal bias provided by R1, and bypassed for rf by C2. The cathodes of V1 and V2 are grounded, and the plate tank consists of split stator capacitor C5 and coil L3; the output is inductively coupled through L4. Cross neutralization is provided, with the plate of V1 coupled through neutralizing capacitor C4 to the grid of V2, and the grid of V1 coupled to the plate of V2 by neutralizing capacitor C3. Series plate feed is used with the supply tapped to the center of tank coil L3, and bypassed by rf by C6.

With a fixed negative bias applied to the center tap on L2 from the separate negative bias supply, the grids of tubes VI and V2 are biased far beyond cutoff (about 2-1/2 times). In the absence of excitation, both tubes are cut off, no current flows and no output is

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obtained. When r-f excitation is applied to coil L1 a similar r-f voltage is induced in tank coil L2. Since the center tap of L2 is bypassed to ground for rf it is effectively at r-f ground potential (zero voltage) and the ends of the coil to which the grids of V1 and V2 are attached are at equal and opposite r-f potentials. When a positive voltage appears on the grid of Vl, a negative voltage appears at the grid of V2. With a balanced input the voltages are of equal amplitudes and of opposite polarities. Grid tank capacitor Cl tunes the input tank to resonance at the frequency of the drive voltage. The maximum current flows in the closed tank circuit, and maximum drive voltage is developed across the parallel-connected tank and applied to the grids. Assuming a sine wave exciting signal going positive on the grid of V1, the grid of V2 is driven further negative into cutoff and no plate current flows in V2. As long as the signal on VI grid is below the cutoff level no current flows in V1 also, and both tubes remain cut off. As the positive-going input signal rises above the bias level on VI, the tube is eventually driven into conduction, and plate current flows. Since the tubes are fixed biased beyond cutoff, plate current flows only during the time the grid is above cutoff, or for about 120 degrees of the positive half cycle of excitation signal. As the positive grid voltage increases, plate current increases, reaching its peak at the same time the excitation voltage reaches its crest. At the beginning of the conduction cycle the grid voltage is only sufficiently positive to reduce the fixed bias voltage so that the effective bias is just above cutoff (but still negative). However, as the amplitude of the drive voltage increases, the grid is driven to the zero bias level and then positive. At or near zero bias grid current also begins to flow, increasing to its peak value at the crest of the cycle. Grid current flow is from the cathode of V1 to the grid, through coil L2 and the center tap to grid resistor R1, then to the bias supply and ground. In flowing through Rl, a negative voltage is developed across R1 which adds to the instantaneous bias. The value of RI is chosen so that the maximum desired bias is produced with a specified grid current drive before the crest of the cycle is reached, with light saturation for Class B amplifiers, and with heavy saturation for Class C amplifiers (see Single-Ended (Class B or C) R-F Power Amplifier circuit in this section of the handbook for an explanation of saturation, and the introduction to this section for a discussion of signal bias).

When plate current flows in V1 there is a flow of  $\checkmark$ electrons from the cathode through the grid wires to the plate, and from the plate through the top half of tank coil L3, out the center tap to the plate supply and ground. Current flow through half of L3 produces an electric field around the coil (which acts as the primary of a transformer), and the magnetic lines of force link output coil L4 (which acts as the secondary) inducing an output voltage in it. At the same time, the field around the lower half of L3 induces a voltage which is in a direction to continue current flow through L3. This induced current charges the lower half of split stator capacitor C5 negatively, while the upper half of the capacitor is charged positive. The effect is the same as if the split capacitor were a single capacitor connected across L3 with the upper plate positive and the lower plate negative. Since tank L3 and C5 are parallel resonant at the output frequency, a circulating current is built up within the tank which continues to oscillate back and forth. Reinforced first by V 1, and then by V2 as it operates. The resonant tank selects the desired output frequency and discriminates against any harmonics which also tend to develop across the tank impedance. The tank impedance is a maximum at the fundamental output frequency and very low at any of the harmonic frequencies. Thus maximum voltage is developed across the maximum impedance presented at the desired fundamental frequency. The tank coil also acts as a tapped autotransformer with a turns ratio of one half to one (2 to 1). Since transformer impedance always varies as the square of the turns ratio, it presents a load impedance to the single tube of one quarter the plate to plate load impedance. At the positive crest of the drive cycle the voltage drop across the tank impedance is maximum and causes the effective plate voltage to be at a minimum value. At this time the tank is absorbing, or being charged with r-f energy, and only a small amount is applied to the plate for dissipation in the form of heat. This is the most efficient part of the operating cycle.

As the excitation voltage passes the crest and reduces the amplitude it becomes negative going. The effective bias becomes more negative and plate current flow is reduced. This action continues until zero bias is reached and grid current flow, likewise, reduces and ceases. From here until cutoff the plate current continues to reduce, and ceases when cutoff bias is reached. While the plate current is reducing, it induces a tank current flow in the opposite direction L

causing the tank capacitor to discharge. This discharge continues beyond cutoff when both VI and V2 are non-conducting, and is the so-called "flywheel" effect of the tank, which continues to supply an r-f output even though neither tube is operating. When the positive half cycle of drive is completed, the negative half cycle starts, the grid of V1 is driven further into cutoff and is held inoperative for the remaining portion of the half cycle.

V2 grid is now being driven positive by the negative half-cycle of input signal. (The input signal is inverted by the push-pull input tank.) During the negative half-cycle, tube V2 is made to operate exactly as described above for VI. The effective bias is reduced until plate current flows, and as the bias decreases grid current flow starts near zero bias, reaching its peak at the negative crest of the drive signal (the grid voltage applied V2 is positive). Plate current flow through V2 and the lower half of the tank coil, now flows in the other direction and charges C5 in the opposite direction to the previous half-cycle of operation. Actually, operation is only over 120 degrees as mentioned before, and the tubes are quiescent over 60 degrees of the 180 degree halfcycle. Thus it can be said that the tank alone supplies energy for a total of 120 degrees, and the tubes for 240 degrees out of a single cycle of operation. Operation of V2 is identical in every respect with that of V1, their currents and voltages are, however, 180 degrees out of phase, but there is no canceling effect since each tube operates separately. The tank circuit, meanwhile, continues to oscillate first in one direction for 180 degrees and then in the other direction for the remaining 180 degrees of the complete cycle, being reinforced each half-cycle by a different tube. Output coil L4 supplies a continuous r-f output to the antenna or transmission line from the tuned tank circuit to which it is inductively coupled. Since the tank is tuned to the fundamental frequency, even harmonic content is almost entirely cancelled in the secondary (L4) since equal and opposite voltages are produced. The closer the circuit is to a balanced condition the more nearly is the even harmonic output reduced to zero. Since the odd harmonics occur inphase a small amount also appears in the output. The amount is dependent upon the impedance the tank presents to odd harmonics. Usually it is so small as to be considered negligible. However, in extremely high powered stages (megawatts) this output may be on the order of tens of watts (or more) and require extra

filtering to prevent it from being radiated on the undesired harmonic frequency. The manner in which the tank current and the fundamental and harmonic plate current components vary is shown in the accompanying figure to illustrate the manner in which the even harmonics are cancelled.





The instantaneous tank current varies continuously throughout the cycle flowing first in one direction (shown as positive) and then flowing in the opposite direction (shown as negative). During a portion of this time  $i_{p_1}$  and  $i_{p_2}$  (curve 1) flow alternately as V1 and V2 operate. Any second and third harmonic currents flow as shown in curves 2 and 3, respectively. Since the second harmonic current is always out-ofphase with the fundamental plate current it cancels out. The third harmonic current (curve 3) in in-phase more than it is out-of-phase, therefore, a small amount of odd harmonic distortion remains in the output. The selectivity of the output circuit also helps discriminate against any harmonics, since the impedance it offers to these frequencies determines the output amplitude, and most output circuits are resonant at the fundamental frequency.

With the grid V1 and V2 cross connected to the opposite tube plate through neutralizing capacitors C3 and C4, equal and opposite feedback voltages are applied which cancel out any in-phase plate to grid feedback and prevent the stage from going into self-oscillation. The additional capacitance added by the neutralizing circuit reduces the input impedance,

hence, triodes are only used when necessary, or the push-pull grounded-grid circuit is used instead. The use of a well shielded tetrode or pentode makes neutralization unnecessary, because the plate and grid are shielded from each other by the screen grid and its associated bypass capacitor, which hold the screen at r-f ground potential. The low excitation requirements of the tetrode or pentode makes them especially suitable for use in the intermediate stages of a transmitter. When the power used by the screen grid is considered, however, the overall efficiency of these tubes is not as great as the triode. Because of the easier drive requirement and the lack of neutralization provisions, the tetrode, or beam power tube is generally favored over the triode. Particularly in band-switching transmitters where a neutralizing adjustment is not required for each band.

# Failure Analysis.

No Output. Loss of excitation (drive), bias, supply voltage, or defective tube(s) can cause a nooutput condition. If input coil L1 is open, no drive will be obtained and the tubes will rest in the cutoff condition. Lack of both grid current and plate current will be indicative of this condition. Check L1 for continuity with the POWER OFF. If drive is present in L1, but L2 is open, or C1 is shorted or nonresonant, a similar condition will exist. If L2 is open the symptoms will be the same as when L1 is open. However, if Cl is shorted no drive will appear on VI or V2 grid and the fixed bias supply will be grounded through RI. Usually extremely heavy grid current will flow and R1 will heat, may smoke, and will eventually burnout if the condition is prolonged. Meanwhile, the plate current will also be extremely high because of loss of bias and will usually blow the plate fuse or open the plate circuit breaker, if provided. The same symptoms will occur also if grid bypass capacitor C2 is shorted. Check VI and V2 grids with a voltmeter for the proper negative bias. If L2 is not open and C 1 or C2 is not shorted the proper dc bias will appear on both tubes (make this check with driver plate voltage OFF, otherwise, r-f drive may burn out the meter). If Cl is not tuned to resonance, sufficient drive may exist to produce a low output, but normal loading and output will not be obtained. Normal bias voltage also indicates that both neutralizing capacitors C3 or C4 are not shorted. When either C3 or C4 are shorted, plate voltage will be

applied to the grids of both VI and V2, cause heavy plate current, and blow the fuse or breaker.

When the loss of output is caused by lack of plate voltage it may be due to shorted plate bypass C6, or defective power supply, shorted tank capacitor C5, or defective tube(s). Check the supply voltage first with a voltmeter, be certain to observe all safety precautions since the plate voltage is dangerously high. Make certain that the transmitter plate switch is OFF when checking the supply. If either C5 or C6 is shorted and the supply is good the plate fuse or breaker will operate, and high plate current with normal or slightly higher than normal grid current indication will be obtained momentarily. Usually C5 can be checked visually since arcing will occur as the rotor is varied throughout its range and whenever it touches or moves too close to the stator. If not, make certain the plate voltage is removed, and use a shorting stick to discharge the capacitors in the plate circuit. Disconnect plate bypass capacitor C6 and check continuity to ground with an ohmmeter, no continuity should exist and resistance should be infinite. Then disconnect C5 and L3, and again check for continuity to ground. With the tank disconnected check the plates of VI and V2 to ground; any resistance other than infinity probably indicates a defective tube. Note: be certain to observe the polarity of the ohmmeter so that a negative potential is applied from plate to ground. Otherwise, if the plate is made positive and the tube filament is operating there will be a flow of current, and a false resistance-to-ground reading will be obtained. Check output coil L4 for continuity at the same time to avoid making a later check.

If proper grid current indication is obtained, but a very low plate reading (or a high plate reading) rapidly tuned C5 back and forth to determine if a minimum dip indicating resonance can be obtained. With a sharp minimum and a reduced plate current either L4 is open, and load is not connected, the drive is too low, or L4 is not coupled sufficiently close to tank coil L3. In the case of heavy plate current and broad dip, usually some output will be obtained, and too large, or an overcoupled load is indicated.

Use of grid and plate meter indications, plus the tuning of Cl and C5, should be made to determine whether normal currents and tuning are obtained, since these offer a quick means of trouble-shooting. In most instances, moderate and high power transmitters and tanks are constructed mechanically and

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electrically rugged so that visual observation will locate grounded parts (usually some sign of an arc such as charred insulation or a black spot will mark the point of improper grounding due to the high voltage and currents involved).

In the event of tube trouble, usually both tubes must be defective to cause no output in a push-pull circuit, since the stage is capable of operating at reduced output with only a single tube.

Reduced Output. Low drive, grid bias, or plate voltage, as well as a defective tube can cause a reduced output. Low drive will be indicated by a low grid current reading usually with reduced plate current, and output. Low grid bias will usually cause operation in the Class A or AB region with a higher than normal plate current. Check the bias with a voltmeter from the junction of C2 and R1 to ground; this will indicate the sum of both the fixed bias and the signal bias, and should be made with C 1 tuned to resonance and normal grid current. Closer coupling between L1 and L2 will increase the drive if necessary. If the plate current suddenly increases and the output reduces, particularly during voice modulation (or while being keyed off and on), improper neutralization can be suspected. Remove the plate voltage and tune tank capacitor C5 through resonance, the grid current indication should hardly change as resonance is passed. If it flicks sharply, adjust C3 and C4 in small increments, simultaneously, first in one direction and then in the other. No change in grid current will be observed at the point of proper neutralization.

Normal plate voltage and loading accompanied by reduced plate current indicates the possibility of low tube emission. If plate voltage is low with normal load the power supply rectifiers are probably in need of replacing. A dynamic check on the power supply can be made by quickly detuning and resetting C5 to resonance. The heavy off-resonance current should not cause the plate voltage at C6 to drop more than approximately 25 or 30 volts. If it does, the power supply regulation is poor. A poor soldered joint or bad connection can introduce a high resistance in the plate circuit and cause a reduction in applied plate voltage with a low plate current indication. To check this, remove plate voltage from the driver AND finally, discharge the filter capacitor with a shorting stick, and check the resistance between the tap on L3 and the plates of V 1 and V2. Indications should be zero or a few tenths of an ohm.

#### TRAVELING-WAVE TUBE R-F AMPLIFIER

#### Application.

The traveling-wave tube r-f amplifier is used at super-high frequencies as an untuned r-f amplifier (or mixer) in microwave receivers, as a linear amplifier in transmitters, and in test equipment. Its broad-band characteristics make it particularly useful for highband television and electronic countermeasures (ECM) applications.

#### Characteristics.

Range of operating frequencies is from approximately 200 MHz to 15,000 MHz.

Efficiency varies from 10 to 40 percent.

Power handling capabilities vary from as low as 100 microwatt to 1 kilowatt for continuous-wave emissions. Peak power capabilities for pulsed operation extend up to 50 kilowatts.

Power gain in a single tube varies from 20 to 60 dB maximum.

Noise figures from 5 dB to 30 dB can be obtained, depending on the frequency (increases with frequency, but not linearly).

Uses positive bias and high voltage to control emission of an electron gun.

Amplifies by virtue of a distributed interaction between an electron beam and a traveling wave.

Is a nonresonant device inherently capable of enormous bandwidths.

Usually employs magnetic focusing of the electron beam; however, electrostatic focusing is sometimes employed.

#### Circuit Analysis.

**General.** Traveling-wave tubes are used for both large and small signal applications; each tube is rated for a specific power-handling capability over a certain frequency range. They supplement the presently available microwave tube types, such as planar triodes, klystrons, and magnetrons. They are particularly useful for wideband applications where a large range of frequencies must be covered. Since the tube is completely self-contained and nonresonant, it has no bulky cavities or large magnets to pose a design problem. Either coaxial or waveguide input and output fittings are provided, depending upon the frequency range in use, so that only filament and collector power are needed in addition to the input and output leads to provide an operating amplifier.

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Although the traveling-wave tube has high gain and is easily tuned by changing the collector voltage, it possesses noise characteristics that are somewhat less desirable than those of some of the other types of microwave tubes. Recent improvements along this line have produced noise figures of 6 dB at 3000 MHz and 11 dB at 10,000 MHz or better, as compared with 30 dB for the early versions. The 6-dB figure is approximately the same as that obtained with a crystal mixer. It is well known that crystals are easily damaged by r-f energy. However, the traveling-wave tube is not so easily damaged since an input over-load will merely cause saturation (instead of burnout as in the case of the crystal); hence, with this tube, a simpler duplexing system maybe used.

Circuit Operation. The accompanying figure shows the essential elements of a traveling-wave tube. These are a long, narrow electron beam and a circuit capable of sustaining a slow electromagnetic wave with a longitudinal component of electric field, which can travel along in synchronism with the beam. The slow-wave circuit usually consists of a helix or long coil of wire. In such a circuit the wave travels along the wire with approximately the speed of light. If the length of the wire is 13 times as long as the axial length of the coil or helix, the wave will travel along the electron beam at one-thirteenth the speed of light, and the electrons in the beam, passing through the center of the coil, will be in synchronism with this slow traveling wave if they are accelerated by about 1500 volts. The speed of the electron beam is controlled by the potential applied to the accelerating anode. Since the helix is connected to the collector at the end opposite the cathode, the helix also serves as an additional accelerating anode. An axial magnetic field is used to focus the electron beam, to keep the beam from spreading and to guide it through the center of the helix.



**Basic Traveling-Wave Tube Elements** 

When the electrons travel along in synchronism with the slow wave, there is a cumulative interaction which results in amplification of the traveling wave. At wavelengths of around 10 centimeters, the power gain may be of 1000 to 10,000 times or even greater, in a distance of 10 inches. Because no resonant circuits are involved, the traveling-wave tube is inherently broad-band; substantial gain has been obtained over bands of thousands of megahertz and of several octaves. Waves traveling backward, against the electron stream, are practically unaffected by its presence. To make a stable and useful amplifier, attenuation of the backward wave must be added in the slow-wave circuit. Usually, it is lumped near the center of the tube, and introduces a loss to the backward wave which is much greater than the amount by which it reduces the forward gain. The necessity for the attenuator and its reduction of forward as well as backward gain is a basic limiting parameter, which hinders high-power tube development.

The following figure illustrates a typical travelingwave tube amplifier using a solenoid type of magnetic focus coil. The electronic beam is obtained from a PIERCE electron gun, which produces a series of essentially parallel-path electrons. The tendency of the parallel electrons to be deflected or to stray from the parallel path is overcome by adding a solenoid on the glass envelope of the tube whose axis is in the longitudinal direction. The focusing field of the solenoid deflects any stray electrons back into the electron stream so that ehy must travel through the center of the helix.



Typical Traveling-Wave Tube Amplifier

The r-f input signal is fed into the helix at the cathode end of the tube, while the r-f output signal, is taken from the opposite end of the tube, near the collector (or anode). The accelerating anode creates the initial electric field which attracts the electrons from the cathode, while the collector (or anode) serves to collect the spent electrons after they have passed through the helix, and return them to the power source. The helix is connected to the collector internally, and also acts as an accelerating anode for the electron beam. The r-f signal is coupled to and from the helix inductively. There is no direct connection between the helix and the input and output circuits. The helix consists of a continuous spiral of wire or strap 10 to 12 inches in length, whose natural resonant frequency is much lower than the range of operation so that it acts as a nonresonant device. The purpose of the helix is to provide a path for the input signal in proximity to the electron beam so that interaction can occur between the beam field and the signal field. When the r-f input signal is induced on the helix, a conductive path is provided by the helix from the cathode end to the collector end of the tube, through which the r-f signal current flows. Signal current flow induces a field around the helix which travels with the signal from input to output; thus, a traveling wave is produced along the helix. While the electron beam and r-f signal both travel at the speed of light, the path around the helix is longer. Therefore, the signal field progresses from turn to turn through the helix at a much slower speed than the electron, which travels through the center of the helix and follows the shorter direct path between cathode and collector.

When the input signal field opposes the field of the electrons passing through the center of the helix the electrons are decelerated, and are overtaken by other electrons. During the time the beam electrons are decelerated, they relinquish kinetic energy to the field of the r-f signal, and tend to form in bunches. When the signal field increases, it enhances the electron field and accelerates the electrons, and energy is transferred from the r-f field to the electron field. As the signal field and electron beam progress through the tube, more bunching occurs. Thus, more electrons are available to give up kinetic energy while a particular bunch is passing through a decelerating field. Since more time is spent by an electron in a decelerating field than in an accelerating field, it gives up more energy to the r-f field than it receives. Thus, as the

signal progresses along the helix, it increases in strength, and is amplified.

No energy transfer is possible until electron bunching commences. As bunching increases, the signal amplitude increases and causes even greater deceleration of the electrons (in the following bunch). This causes the signal strength to increase exponentially, as shown in the accompanying illustration. Eventually, a point is reached at which the electrons in the bunches are slowed to the extent that they are no longer in synchronism with the signal field. At this time the forward speed of the beam electrons and that of the signal are no longer near the same value, and the efficiency drops.



**Development of Growing Wave** 

Operation of the traveling-wave tube is sometimes explained on the basis of a total of four waves existing within the tube, three forward waves and one backward wave. The three forward waves are the result of the division of the input into three components, each with an amplitude of one-third the input strength. The first wave (which is the one we have been discussing) travels more slowly than the electron beam, and increases in strength. Another wave also travels at this same speed and diminishes in strength (as it gives up its energy to the first wave). The third wave travels at the fastest speed, faster than the electrons, and maintains a constant strength. The resultant of these three waves is the constantly growing signal or output.

The gain of the traveling-wave tube is also affected by the input and output coupling circuits. For amplifying a wide frequency band, high gain can be maintained by changing the helix voltage with frequency to maintain the necessary synchronism between the

helix velocity and the beam velocity. In addition, the maximum output power depends upon the input (drive) power, and the power-handling ability of the helix. The amount of power in the beam input power is a factor. Also, since the output end of the helix is heated by r-f currents and electron bombardment, if the beam disperses before passing the output end, the power-handling ability of the helix is another factor. Dispersement of the beam and bombardment by beam electrons can be caused by a maladjustment of the magnetic focusing field. Since a helix mounted in glass has a low heat-dissipating ability, the power output at the present state of the art is limited to values less than 100 watts unless special cooling systems are employed. High-power tubes use either water or forced-air cooling.

The thermal noise of the electrons in the beam affects the noise figure of the traveling-wave tube amplifier, just as it affects the noise figure of other types of amplifiers. The noise signal is induced onto the helix and is amplified in the same manner as any other signal. Lowering the operating voltage will generally result in a slower beam velocity and less thermal noise. If the gain per unit length is low, less noise amplification will also occur; tight focusing of the beam will also produce less noise. Uneven cathode emission, particularly from an aging tube, will produce a nonsymmetrical beam and noise, as will ion movement caused by gases within the tube. When the signal injection point is properly spaced from the end of the electron gun, a reduction in noise occurs because of certain periodic fluctuations in noise current within the tube. Thus, injection of the signal at a point of low noise current results in a greater signalto-noise ratio.

When the long solenoid focusing coil of the traveling-wave tube is replaced by a series of small coils spaced along the tube, as shown in the accompanying illustration, less energy is required to focus the electron beam, and tighter focusing is achieved. The same effect is produced by using a series of permanent magnets to produce a periodic magnetic field. These types of tubes are called PPM (periodic permanent magnet) traveling-wave tubes. Better over-all efficiency is obtained, since the loss of beam current through dispersion of stray electrons is prevented.



Periodic Electro Magnet Focusing

When a series of opposing electrodes.or plates are placed along the tube inside the glass and connected to a dc source as shown in the accompanying illustration, an electrostatic field is produced between the electrodes. This is similar in all respects to the magnetic field produced by the solenoid or the periodic permanent magnets. Focusing in this instance, is done electrostatically, and no change in operation occurs. Because the construction of this tube is more difficult and more expensive, and since the performance is about the same, the electrostatic type of travelingwave tube is seldom used.



Electrostatic Focusing

The attenuator which prevents the backward wave from causing oscillation and loss of amplification is provided by spraying a resistive film (produced by an aquadag solution) on the helix and tube envelope at the proper location. In a high-power tube the attenuation is concentrated near the center of the tube, while in a low-power tube it is usually not more than onethird the distance from the cathode.

Whife more could be said about the various phases of design, the discussion above is sufficient to acquaint the reader with the primary functioning of traveling-wave tubes. Since the tube is a freed package, there is nothing the electronic technician can do to change its operation. of course, faulty operation can result from incorrect connections or operating voltage and polarities. Therefore, further discussion at this time is unnecessary. Additional data can be obtained, when desired, by reference to other texts or to manufacturers' information sheets.

#### Failure Analysis.

**No Output.** Lack of input signal, an open output circuit, or a lack of filament or plate voltage can cause loss of output. Use a voltmeter to determine whether the fdament and plate voltage are correct. WARNING: *High plate voltage* exists between the collector and ground; be certain to observe *all safety precautions* when measuring this voltage. Since the cathode is usually connected to one side of the filament, measure the fdament voltage *only* when *the plate voltage is off.* 

*The* input and output circuits can be checked for continuity with an ohmmeter, with the power off. If the external circuits appear to be satisfactory, use a signaf generator to supply an input to determine whether there is loss of input signal. Likewise, in the output a dummy load may be substituted. If the input and output circuits are apparently satisfactory and proper electrode voltages are applied, a no-output condition will probably indicate a defective tube.

Low Output. Low output can be caused by improper plate or filament voltage, low drive, or a defective tube. Check the plate and fdament voltages, observing all safety precautions. In transmitting applications, insufficient r-f drive will cause reduced output. In the special case where sweep voltages are used to tune automatically over a band of frequencies, it is important that the drive waveform and sweep waveform be of the shapes and amplitudes specified; otherwise, reduced performance will occur. Low tube emission can sometimes be found by noticing that the output fluctuates in amplitude and that a high noise is developed in the output. The beam current in this case will be reduced, and low output will occur. Unfortunately, other conditions, such as load reflections or a change in accelerating voltage or collector voltage, will also change the beam current. Where solenoid focusing coifs are used, lack of sufficient field will also cause a reduction in the beam .current, and can be caused by a defective coif, low focusing voltage, or loss of power to the coil. In this case, the focus supply can be checked with a voltmeter and the resistance of the coif determined by means of an ohmmeter, with the power off. Comparison with a good coil will indicate whether the resistance is high, low, or normal.

Because of the few parts involved, usually a voltage check, a waveform check, and a beam current check are the only simple checks possible. In tubes having a low noise figure, disconnecting the antenna from the input in receiving applications will reduce the noise, and serve as a rough indication that the tube is functioning. However, in tubes having high noise figures this change may be masked by the tube noise. Thus, a more positive check is to insert a signaf from a known source and determine whether normal amplification is obtained. A change in load should also cause a change in beam current, as should a change in focusing-magnet current.

In the case of overdrive, increased current usually occurs, followed by a reduction in output as the collector is heated by electron bombardment. Once saturation is reached, no further increase in current occurs as the drive is further increased; this indication can sometimes be mistaken for reduced output.

# MULTICAVITY KLYSTRON R-F AMPLIFIER

#### Application.

The multicavity klystron r-f amplifier is used to supply high r-f power to the transmitting antenna of television, radar, microwave, and electronic countermeasures equipment operating in the VHF, UHF, SHF, and EHF regions.

#### Characteristics.

Uses a positive grid voltage.

Uses a number of cavities tuned .to the same frequency for narrow-band operation (synchronous tuning), or is stagger-tuned to different frequencies for wide-band operation.

Power gain is on the order of 30 to 50 dB.

Power-handling capabilities range from microwatt

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in receiving or test equipment applications, to the tens of megawatts in transmitting applications.

Efficiencies of 40 to 50 percent are possible.

Uses velocity modulation of an electron beam to form electron bunching for amplification.

Each cavity provides additional amplification, and extremely high gain is thus obtained.

External magnetic beam-focusing is usually employed to improve efficiency.

# Circuit Analysis.

General. The basic multicavity klystron consists of an electron gun, an input (buncher) cavity, an output (catcher) cavity, and a collector anode. The cavities may be integral within the tube or constructed externally so that the tube can be inserted within them. A focusing coil arrangement is usually included to prevent divergence of the electron beam, loss of electrons, and consequent ieduction in efficiency. Any number of cavities can be used by increasing the tube length, as long as the transit time across the lips of the cavity is short as compared with the wavelength of the signal. The high-power klystron operates at voltages of 25 to 100 kilovolts or more, and the current is in terms of amperes or tens of amperes, rather than milliamperes. The unit is usually shielded as a protection against high voltage, and special lead shields minimize the X-radiation produced as a consequence of the high electron voltages used. Since the physical construction of the various tubes available are slightly different for different manufactures, the following discussion applies generally as far as basic theory is concerned. The effects of cavity shape and construction, windows, and apertures or coupling loops are generalized so that the discussion will be applicable to most types of klystrons. Moderatepower tubes use forced-air cooling, while the highpower units use hollow water jackets with forcedwater circulation to provide artificial cooling.

Because of the noise produced by the electron beam (noise figure averages 25 dB, the multicavity klystron is normally used for transmitting applications instead of receiving applications. While feedback can be employed between the cavities to provide oscillation, the multicavity klystron is generally used as a linear r-f amplifier, being driven by a **lower-power** klystron or a traveling-wave tube.

**Circuit Operation.** The simplified schematic of an elementary multicavity klystron is shown in the accompanying illustration.



Simplified Klystron Multicavity Amplifier

At the left is the cathode of the electron gun, from which the long electron beam is accelerated, and at the right is the collector, which finally collects the beam. The electron beam first passes through the input resonator. The input signal produces a longitudinal electric field across the part of the resonator through which the beam passes. This field alternately retards and accelerates the electrons passing through the resonator. The retarded and accelerated electrons all travel along through the drift space between the cavities. There, some of the accelerated electrons catch up with some of the retarded electrons which left the input resonator earlier, so that bunches are formed. These bunches are composed of electrons, which pass through the input resonator while the field was changing from retarding to accelerating. These bunches eventually pass through the output resonator (or catcher) and induce a current from which the output is derived. In the 3-cavity klystron, an intermediate resonator is placed between the input and the output cavities to provide, in effect, a twostage amplifier in one tube envelope. The bunched electron beam produces a field across the intermediate resonator, and this again retards and accelerates the beam (that is, velocity-modulates it anew). In tubes for very broad-band operation, several intermediate resonators may be used.

The manner in which the electron beam is formed and bunched can be understood by following the action step by step. The initial electron beam is produced by a Pierce-type electron gun. The electrons emanate from a flat cathode under the attraction of a positive accelerating field produced by an accelerating

#### **ELECTRONIC CIRCUITS**

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grid located near the cathode (between it and the input resonator). This electrode is shaped to permit passage of the electrons through a small orifice. In low-power guns the electrode may contain an actual grid structure through which most of the electrons pass without hindrance and from an essentially parallel-path beam of electrons. The tendency of these electrons to expand around the axis of the beam and disperse is corrected by a magnetic field placed along the axis of the tube by a focusing coil (permanent magnets are also used). Any electrons which tend to fly off at a tangent, or in a radial direction, are forced back into the beam path by the parallel flux lines from the coil. In extreme cases they cause the recalcitrant electrons to follow a spiral path back to the axis of the beam. The parallel beam of electrons, all traveling at the same speed, passes through a pair of buncher grids, as shown in the accompanying illustration. Each of the buncher grids is connected to one side of a tuned circuit (cavity). (The tuned circuit and the buncher grids are at the same dc potential as the accelerator grid.) The input signal is usually inductively coupled into the tuned circuit or cavity, and produces an ac field between these grids. Assuming a sine-wave input, when the buncher grid closest to the cathode is positive, the buncher grid farthest away is negative. These voltages add to or substract from the applied dc accelerating voltage. Therefore, the alternating (signal) voltage between the buncher grids causes the velocity of the electron leaving the buncher grids to differ, depanding upon the time at which each electron passes these grids.



**Electron Gun and Buncher Grids** 

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An electron that passes the center of the buncher cavity at the same time the input signal is passing through zero leaves the buncher at the same velocity at which it entered (since no change in accelerating potential occurs). The position of the electrons plotted against time is shown in the following Applegate diagram, which indicates how bunches are formed. The slope of the lines in the figure represents the velocity of the electrons.



Applegete Diagram of Electron Bunching

Electrons which pass the center of the buncher a few electrical degrees earlier than the point of zero voltage (such as at C and D in the diagram) encounter a negative opposing field, and leave the buncher with reduced velocity, since the decreased voltage of the buncher slows them up. Electrons which pass a few electrical degrees after the instant of zero voltage, as at F and G in the diagram, leave with increased velocity since the buncher voltage is now slightly higher than the voltage of the accelerator grid (positive signal adds to positive electrode voltage). In the fieldfree drift space between the buncher and the intermediate cavity, faster electrons F and G catch up with electron E, which previously passed the bunch with no change in velocity. Slower electrons C and D lag behind, and hence draw near to E. At some point between the two cavities, electrons C, D, E, F, and G draw close together in a group. Now consider electron A', which leaves the buncher a half-cycle later than E. In this case its neighboring electrons draw away, since H is slightly slower and-B' will be slightly faster. Consequently, the electron stream along the tube consists

of electron bunches separated by regions in which there are few electrons. From the diagram, it appears as though bunching occurs in the first half-cycle of operation. Actually, bunching really occurs two or three cycles later in the relatively free drift-space between cavities. Also, bunching occurs twice in the three-cavity klystron (once between the input and center cavities, and once again between the center and output cavities). Since it is less complex and somewhat easier to understand, this diagram is used to emphasize bunching action, although it really is a representation of a two-cavity klystron with the retardation and acceleration of electrons overemphasized by using a much greater electron-line slope than actually occurs.

Since a continuous stream of electrons enters the buncher grids, the number of electrons accelerated by the alternating (signal) field between the buncher grids on one half-cycle of alternation is exactly equaled by the number of electrons which are decelerated on the other half-cycle. Therefore, the net energy exchange between the electron stream and the buncher is zero over a complete cycle (assuming a sinusoidal signal), except for any losses that occur in the tuned circuit or buncher cavity. As the electrons travel down the tube, they pass through the intermediate cavity grids and induce an oscillation into the middle cavity. Thus, an ac potential similar to the input signal is produced between the middle cavity grids. When the middle cavity is tuned to a frequency slightly higher than that of the buncher cavity, it presents an impedance with an inductive component. This provides a phase relationship between the cavity voltage and the electron stream which causes further velocity modulation of the electron stream. In this case, since the cavity is a high-Q resonant circuit, it causes a voltage build-up which is larger than that of the input signaL Therefore, the electrons are again bunched; this time they are formed into denser bunches, and the free electrons between the bunches are still further reduced (some are absorbed into the new bunches). The new bunches of electrons form in the drift space between the middle cavity and the output (or catcher) cavity, pass down the tube, and enter the catcher cavity.

The conditions at the catcher cavity are somewhat different. This cavity is located along the tube so that the passage of the electron stream in bunches through the first grid creates a negative potential upon it. This negative potential retards the electrons, and, in slowing them down absorbs energy from them. The spacing between the two catcher grids is equivalent approximately to a half-wavelength at the frequency of operation. Thus, by the time the first bunch reaches the second catcher grid, the first catcher grid has reversed polarity and becomes positive, while the second catcher grid is now negative, as shown in the accompanying illustration.



Catcher Grid Polarity

Since the second grid is also negative, it further slows down the electrons and again absorbs energy from them. Thus, in delivering energy to the tuned cavity connected to the catcher grids, the speed of the electroni is greatly reduced. After passing this second set of catcher grids the spent electrons are collected and removed from the tube by the positive collector plate.

A complete multicavity klystron r-f amplifier can be shown schematically as illustrated in the accompanying figure. The operation is exactly as described in the paragraphs above; therefore, it will not be repeated.



Multicavity Klystron R-F Amplifier Schematic Diagram

#### Failure Analysis.

No Output. Lack of or improper accelerating voltage, loss of drive power, or improper cavity tuning can result in loss of output. Usually, excessive beam current indicates improper tuning or voltage. A voltage check will indicate whether the voltage is sufficient. WARNING: Dangerous High Voltage is present; all safety precautions should be taken to make certain that no shock hazard exists. In practice, the shell of the tube is grounded and a high negative voltage is applied to the cathode. It is particularly important not to remove any lead shielding while troubleshooting; otherwise, X-radiation effects will produce a hazard to maintenance personnel. Normally, a nooutput condition will be caused by an open circuit (or short circuit) or by a defective tube, rather than by mistuning or low voltage, since in these latter cases some small output normally occurs. When both filament and anode voltages are correct and the proper drive voltage exists, the tube is probably at fault. Substitution of a tube will not immediately restore full output, since the proper tuning and adjustment

procedure must be followed to enable the tube to function properly. Use the manufacturer's recommended procedure for tuning and placing the unit in service, and note any deviations in performance or any abnormal indications as the procedure is followed. Investigate each deviation as it occurs, and make certain that it is cleared up before proceeding further.

**Reduced Output.** Low filament, drive, or anode voltage, as well as mistuning, can cause reduced output. Check the filament and plate voltages with a voltmeter, observing all safety precautions. An increased beam current can result from improper tuning or improper load. Check the drive, using a dummy load at the input to be certain that sufficient power is available. With sufficient drive established, connect a dummy load to the output and follow the proper tuning procedure. As the tuning procedure is performed, the beam current should reduce, more r-f drive should be required, and a greater output should result. Where focusing coils are used, loss of focus magnetism will show as a reduction in focusing-coil

current and a reduction of beam current (the stray electrons are absorbed before reaching the collector). An increase in beam current can usually be traced to improper cavity tuning. For maximum output, both the input and output cavities should be tuned to the same frequency. In broad-band operation it is necessary that each cavity be tuned to the proper frequency; otherwise, loss of output or of frequency range will occur. As with all other power amplifiers, the proper load must be attached; otherwise, improper impedance relationships will cause unwanted reflections and a loss of power. In receiving applications, low cathode emission will usually cause an increase in noise because of uneven electron emission.

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# PART 5-7. RF FREQUENCY MULTIPLIERS

# **RF FREQUENCY MULTIPLIERS**

# General.

Several applications exist for use of r-f frequency multipliers. For example, a harmonic generator consists merely of a number of frequency-multiplier stages connected in cascade. They are used in receivers, being driven by a stable local oscillator which operates at a low fundamental frequency and is multiplied through several stages to supply an oscillator signal to a VHF or UHF mixer. Likewise, in test equipment, a suitable oscillator has its output frequency multiplied for use as a signal generator or frequency standard, or for other purposes. In a transmitter, the multiplier stage (or stages) allows the use of a single crystal to provide drive for r-f amplifiers operating on harmonically related output frequencies, or it may be used to supply a crystal-controlled output at higher frequencies, where crystal operation at the output frequency is not feasible.

The power output of the multiplier stage varies roughly as the reciprocal of the number of multiplications. Thus, a frequency doubler produces about one-half the output power of a conventional Class C r-f amplifier stage, and a frequency tripler produces about one-third the power; hence, the necessity for cascaded operation at the higher multiples. For example, two doubler stages operated in cascade will deliver twice the power of a single quadruple stage.

The loaded tank circuit impedance increases roughly in proportion to the number of harmonic multiplications required, since the output power decreases and a greater impedance is necessary to provide the same voltage drop across the tank. This places a practical limit on the number of multiplications possible in a single stage.

Although either triode or pentode tubes may be used as frequency multipliers, the pentode is more commonly used because of the reduced grid drive required for pentode operation, plus the larger power output obtainable for the same plate voltage. Since grid current flows in Class C operation, the multiplier stage requires a slight amount of power from the oscillator to drive it. The reduced drive of the pentode, therefore, allows the oscillator to operate more stably, and permits a lower-rated oscillator tube to be used. Normally, a Class C amplifier is biased at 2 to 2% times cutoff. The frequency multiplier is

essentially a Class C stage which utilizes its rich harmonic content, or, rather, is operated so as to develop a greater harmonic content than normal. Selection of the desired harmonic by a tuned output circuit produces a relatively large output at that harmonic. To produce the distorted plate current with its rich harmonic content, the stage must be biased higher than for normal Class C operation, and must be driven harder than normal. Thus, plate current flows only during a small fraction of the cycle, roughly from 60 to 120 electrical degrees (depending upon the amount of harmonic multiplication desired). Therefore, the normal grid bias for a multiplier is usually 3 to 4 times cutoff. Because the plate output tank is tuned to a different frequency from that of the input (drive) signal, no plate-to-grid feedback occurs. Therefore, neutralization is never required, regardless of whether triodes or pentodes are used.

#### PENTODE RF FREQUENCY MULTIPLIER

#### Application.

The frequency multiplier stage is used to provide an output frequency which is some integral multiple of a fundamental crystal-controlled, or self-excited oscillator frequency. It is universally used in receivers, test equipment, and transmitters.

#### Characteristics.

Uses Class C operation at all times.

May be self-biased, fixed biased, or a combination of both.

Output frequency is always some multiple of the fundamental.

Normally doubles or triples, but can operate up to about the seventh harmonic.

Efficiency varies inversely with frequency.

Maximum usable efficiently is on the order of 70 percent, and lowest efficiency is about 45 percent.

Grid bias is higher than in the normal Class C amplifier.

Requires more grid drive than would be necessary for operation at the fundamental frequency.

Does not require neutralization.

#### Circuit Analysis.

**General.** Schematically, the pentode r-f frequency multiplier appears identical with that of the conventional Pentode R-F Voltage Amplifier or the Pentode R-F Buffer Amplifier previously discussed. However,

#### AMPLIFIERS

there are differences in parts values to provide the correct bias and operation, and the plate tank resonates at a multiple of the fundamental frequency. Detailed differences in operation are discussed below.

Circuit Operation. A typical frequency multiplier circuit is shown in the accompanying illustration. In this configuration, the oscillator output is capacitively coupled through C<sub>c</sub> to the grid of VI. Grid bias is obtained through grid current flow in R1, and protective cathode bias is supplied by R2, which is bypassed for rf by Cl. The screen voltage is dropped to the proper value by screen resistor R3, bypassed for rf by C2. Variable capacitor C3 and inductance LI form the output tank circuit, which is inductively coupled to output coil L2. While series plate feed is employed, one end of the tank is bypassed to ground by C4, and the radio-frequency choke (RFC) insures that any residual rf remaining flows to ground by way of C4 rather than through the low impedance of the power-supply filter.



Typical Fraquency Multiplier Circuit

With no signal applied no grid bias is developed, and the plate and screen current flow through cathode resistor R2 provides sufficient cathode bias to limit the static current flow to a safe value. When the oscillator signal is applied, the low reactance of coupling capacitor C<sub>c</sub> allows practically all of the input to appear across RI and the V1 grid. On the positive half-cycle of the input signal the plate current increases, and on the negative half-cycle it decreases. During the positive half-cycle C<sub>c</sub> charges, and during the negative half-cycle it discharges from the capacitor to ground, a negative bias is developed across R1; this grid bias voltage and the cathode voltage stored in Cl produce a high bias many times the cutoff value. (See the introduction to this section for a further discussion of cathode bias and grid-drive, or signal bias.)

Because of the extremely high bias, the plate current conduction period is reduced to a small fraction of the total cycle. Actually, it is less than a half-cycle and varies with the amount of multiplication desired. For a frequency doubler it is about 120 electrical degrees, and for a quintuple it is about 60 degrees. The short time during which plate current flows produces a very distorted plate pulse which is rich in harmonics. When plate tank C3, L1 is tuned to the desired output frequency, it offers a high impedance at the frequency, so that a large drop in plate voltage occurs across the tank. With an increasing plate current, caused by the positive input signal, the plate voltage is dropped toward zero; during cutoff, produced by the negative portion of the input signal, the plate voltage increases to almost the full value of the supply voltage. A decreasing plate voltage induces a negative output signal in L2 by transformer action, since it is coupled via tank coil L1, while an increasing plate voltage induces a positive output signal in L2.

The instantaneous current and voltage relationships in a frequency doubler are graphically illustrated in the accompanying illustration.

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Plate Current and Grid Voltage Relationships

As can be seen from the figure, the plate current flow time is longer than the grid current flow time, but both maximums occur together. Thus, as instantaneous grid voltage e<sub>c</sub> starts its positive excursion, no plate current or grid current flows until the grid voltage reaches cutoff. At this time plate current starts to flow. Slightly later, at zero bias, grid current flows also. The grid current flow is supplied from the oscillator or drive source. The increasing plate current (obtained from the power supply) causes a voltage drop across the plate tank impedance (tuned, for example, to twice the frequency of the oscillator). When the plate current is at its maximum, the plate voltage is at its minimum. At this time some plate power is absorbed by the tuned tank circuit. As the drive signal reverses and causes the instantaneous grid voltage to fall toward zero, the plate current decreases and the plate voltage increases. The grid signal continues to swing in the negative direction while the plate voltage rises (in a positive direction). At the static dc level of plate voltage  $(E_b)$ , the grid drive is approximately equal to the dc bias (zero bias), and as the grid voltage increases toward cutoff, en continues to rise. At cutoff, the tank circuit supplies power, and e<sub>p</sub>rises, even though the plate current ceases. This is the so called "flywheel" action of the tank circuit, which continues operation during the time the tube is inactive beyond cutoff. When the instantaneous negative grid voltage reaches the dc bias level (EC), plate **voltage**  $e_p$  reaches its positive peak and is approximately equal to  $E_o$ , the output voltage.

As the instantaneous grid signal continues to decrease beyond the dc bias level, the plate voltage now falls and becomes negative-going, since the tank is operating at twice the grid frequency, and the input signal, being highly negative, has no effect on the plate current. At the negative peak of drive voltage  $E_g$ , plate voltage  $e_p$  completes its second negative excursion and starts its second positive excursion. The drive voltage also swings positive again and now starts back toward cutoff and zero bias. When the drive is again equal to the dc grid voltage, the second positive peak excursion is reached and the plate voltage starts dropping. As the grid voltage passes cutoff, plate current is again drawn and the plate voltage continues to drop until it reaches the third minimum, when the plate and grid currents are again at a maximum. Once again the plate power is absorbed by the tank to overcome the losses in the tank and to recover the energy supplied to the circuit during the inactive period.

With the tank replenished; it is again ready to supply the flywheel effect of the next cycle of operation. Note that always during the short pulses of plate current flow, the tank is absorbing power from the plate circuit. While on the negative grid swing (where the tube plate current is normally cut off and no output should occur), the tank circuit continues to oscillate and thus supplies the missing portion of the signal. Since the tank oscillations are twice that of the fundamental oscillator frequency, two peaks occur for every fundamental peak (in the tripler three peaks occur). The greater the number of oscillations required between the periods of pulses of plate current, the more the energy required from the tank to sustain these oscillations. Hence, the efficiency and output drop off as the multiplication of frequency is increased. In addition, the flywheel action of the tank maintains an approximately sinusoidal waveform in the output, while the fundamental plate current pulses are greatly distorted. When the grid bias and drive voltage amplitudes, as well as plate voltage, are adjusted for maximum output at a particular frequency, a slightly distorted output may be obtained; however, this can usually be compensated for by a slight adjustment of the tank tuning capacitor.

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While push-pull operation can be used to supply more power output, more drive is required and only the odd harmonics are multiplied, since the even harmonics cancel out in the plate circuit. Therefore, push-push operation is employed, as explained in the next circuit discussion.

#### Failure Analysis.

**General.** The discussion of failure analysis for the Pentode R-F Voltage **Amplifier**, and for the Pentode R-F Buffer Amplifier, duscussed previously in this section of the handbook, are generally applicable to the frequency multiplier.

No Output. Lack of grid drive, plate, screen, or supply voltage, or a defective tank, output coil, or tube can cause loss of output. Check with a voltmeter to make sure that the supply voltage is normal. If the cathode voltage is also normal, the proper plate and screen currents probably exist, so that either the plate tank is detuned or insufficient drive is indicated. Connecting a milliammeter in series with R1 and ground will indicate the amount of grid current flow; this will shown that R1 is not oper and serve as a check on CC. If  $C_c$  is open, no drive would be present to cause current flow through R1; if it is shorted, the plate voltage of the preceding oscillator stage will bias the grid heavily positive, cause a large plate current flow, and produce a high cathode bias with practically no output. If cathode bypass capacitor Cl is open, degeneration will reduce the output but not completely eliminate it; if Cl is shorted, a large plate current will flow in the absence of drive voltage, but the plate current will appear normal as long as enough drive is present to produce sufficient signal bias. If screen capacitor C2 is open, self-oscillation and erratic operation (with some output) will probably occur; if C2 is shorted, the supply voltage will be normal but will be entirely dropped across R3. Therefore, R3 will heat, probably discolor or smoke, and eventually burn out. Meanwhile, no plate output will be obtained because of the lack of screen voltage to attract electrons from the cathode. Although a very small plate current may flow because of plate voltage attraction, this output will be practically negligible.

If plate bypass capacitor C4 is shorted, a similar condition will exist, with the entire supply voltage being dropped across the RFC, eventually causing the choke to burn out. Although screen voltage will be present, the plate voltage will be zero and no output can occur. In addition, the screen will tend to act as the plate and collect all electrons, so that excessive screen current will flow; in this case the screen will be overloaded and heat sufficiently to shown color, and if prolonged the tube may be damaged.

If C3 will not tune L1 to resonance at the desired harmonic, no output will be developed across the tank, since its impedance will be too low to produce an output. The resonant frequency of the tank can be checked with a grid-dip meter or a wavemeter. If all voltages are present, but the screen and plate voltages appear higher than normal while the cathode bias is lower than normal, and with low plate current and no output, either output coil L2 is open or the tube is defective. Check L2 (and the load) for continuity with the power off; if satisfactory, it is likely that tube V1 is defective.

Low Output. With a low screen or plate voltage, a low drive, a high-resistance plate circuit, or a defective tube, a reduced output will be obtained. The plate, screen, and cathode bias voltages can be checked with a voltmeter. Use an r-f choke in series with the meter and check the voltage across R1; this will determine whether grid bias exists and also whether sufficient drive exists. If the bias is low because of lack of drive, the stage will operate Class A, lose efficiency, and result in reduced power output. If screen resistor R3 increases in value with age, the screen voltage will be reduced, as will the output. A similar condition can be caused if screen bypass capacitor C2 is leaky. Check C2 with an in-circuit capacitance checker, or disconnect it from ground and check for a constant voltage between the capacitor and ground by use of a voltmeter. A similar condition can also occur if plate capacitor C4 is leaky. A high resistance in the tank can be caused by a poorly soldered joint. This will usually shown as a broad dip in plate current with tuning, rather than the normal sharp dip. Leaky insulation on C3 can also cause a loss of rf and output. Check the capacitor insulating supports for indications of an r-f burn, or accumulated dirt and moisture, which can produce a shunting resistance to ground (particularly salt deposits from spray). Remove the capacitor, and clean and dry it thoroughly if it appears to be dirty; normal gravish oxidation of plates and metal supports does not indicate the need for cleaning. Do not lubricate the capacitor bearings because of rotor binding (adjust the tension screw instead); otherwise, bad contact will create a high r-f resistance. When the bias and

voltage indications appear normal, but the plate current is low and cannot be increased to a normal value (or if it drops immediately after turn-on, or progressively decreases), low tube emission is probably the trouble.

# PUSH-PUSH RF FREQUENCY MULTIPLIER (ELECTRON TUBE)

#### Application.

The r-f push-push frequency multiplier is used as a frequency doubler in transmitters and test equipments that require a greater output and better efficiency than is possible with the single-tube multiplier.

#### Characteristics.

Uses Class C bias at all times.

May be self-biased, fixed-biased, or a combination of both.

Provides approximately twice the output of a single-tube multiplier stage.

Provides efficiency almost equivalent to that of a normal Class C amplifier.

Requires a push-pull input connection and a paralleled-plate output.

May use triode or screen-grid tubes.

Operates push-push instead of push-pull (a plate pulse is provided for each cycle of operation).

Does not require neutralization, since output frequency is double the input frequency.

#### Circuit Analysis.

General. Like the single-stage frequency multiplier, previously discussed in this section of the handbook, pentodes are used in preference to triodes, since the low drive requirement provides less load on the input stage, and a greater output is obtainable than from a triode operating at the same plate voltage. Where the single-stage multiplier may be used to double, triple, or further multiply the input frequency, the push-push stage is usually operated only as a doubler. While it will also operate as a quadruple (since only even harmonics can be produced with appreciable output), the same output can be more easily obtained with two single-stage doublers, which require slightly less than half the drive power. Thus, push-push operation is more limited in its application than the basic single-stage multiplier. It is mainly used

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where a large doubler output is required, since it will produce this output without any loss because of multiplication. This is true because a plate current pulse is provided for each positive half-cycle of the input signal, or one for each output cycle. Thus, the tank circuit requires less replenishing, and greater output and efficiency are obtained. Although a push-pull input is required, this can easily be obtained with a grid tank circuit. In addition, harmonics of odd order, which can sometimes cause a final output on an unwanted frequency, are minimized, and a purer output waveform is supplied than that by the singletube doubler stage.

**Circuit Operation.** The accompanying illustration shows a typical push-push doubler stage.



**Push-Push Frequency Multiplier Stage** 

As is evident from the schematic, a push-pull input is provided by r-f transformer T1. L1 is the primary, and L2 is **tur.ed** by split-stator capacitor Cl to the fundamental frequency. Signal bias is supplied by grid drive, causing grid current flow through R1, with RFC1 keeping any rf out of the bias circuit. A protective cathode bias is also supplied by R2, which is bypassed for rf by C2. Tubes V1 and V2 are pentodes with their suppressors directly grounded, although tubes having the suppressor connected to the cathode internally could also be used. Screen voltage for the tubes is dropped to the proper value by R3 and R4, which are bypassed for r-f by C3 and C4, respectively. The plates of V1 and V2 are parallel-connected to plate tank L3, C5. The secondary of r-f transformer T2, winding L4, provides an inductively coupled output, although capacitive coupling could have been used as well. Series plate feed is used, and the dc plate voltage is applied through RFC2 to the bottom end of L3, which is bypassed for rf by C6. Thus, any rf at this point flows to ground through C6 rather than through the power supply filter capacitor, and any body capacitance effects which otherwise would occur when tuning tank capacitor C5 are also eliminated.

When the input signal is applied to input transformer T1, the input voltage in primary winding LI induces a voltage into secondary winding L2 by transformer action. The center of the L2 secondary is connected to ground through RFCI and R1. The windings are polarized so that the top end of L2 (connected to the V1 grid) is positive when the top end of L1 is positive. Thus, when the top end of L2 is positive, the bottom end of L2 is negative. Since the bottom end is connected to the grid of V2, V2 is negative when the V1 grid is positive, and vice versa. Thus, a push-pull input connection is provided. Tuning capacitor CL is a split-stator type which provides a balanced tank arrangement to ground, and also resonates L2 to the operating frequency of the oscillator, or input stage.

In the absence of an input signal, protective cathode bias is provided by plate and screen current flow through R2. The cathode bias and the signal bias are effectively series-aiding, so that the total Class C bias is a combination of both. (See the introduction to this section for a discussion of cathode bias and signal bias.) As the input signal is applied, either the VI or V2 grid conducts on the positive half-cycle of operation, and grid current flows through R1, producing the signal bias, which is added to the cathode bias. Since only one tube conducts at a time, the cathode bias at any particular instance is produced essentially by only one tube. (When signal bias is absent both tubes will conduct, so the protective bias is produced by both tubes.)

On the positive half-cycle of input signal when VI conducts, plate current flows for approximately 120 electrical degrees of operation. During the remainder of the cycle, tube V1 is cut off. When the input signal

goes negative, a positive grid voltage is induced in L2 and applied to V2, while VI is held at plate current cutoff by a negative signal. The positive grid input to V2 causes plate current to flow for a period similar to that of V1. Both plates are parallel-connected, so that a pulse of plate current occurs for each half-cycle of input signal. During current flow, the plate voltage is dropped across the high impedance of output tank L3, C5, which is tuned to twice the input frequency. Each time the plate voltage is reduced to its minimum value, energy is absorbed by the plate tank. Hence, it receives a push to keep it oscillating each negative half-cycle, from which action the term push-push was derived. Note that in push-push operation each tube operates alternately while the other tube remains at rest; this should be distinguished from push-pull operation, where the current of one tube increases while the current of the other tube decreases (both simultaneously).

The relationships of the grid voltage and plate current, and grid current and plate voltage waveforms is shown in the accompanying figure.



Plate and Grid Waveforms and Their Relationships

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As the grid voltage  $(e_{g1})$  to VI rises in a positive direction, it drives the tube above cutoff, and plate current flows. Plate current  $\mathbf{i}_{\mathbf{p}}$ , in flowing through the tank impedance at the resonant frequency, produces a voltage drop which opposes the applied plate voltage and reduces it toward zero. As the grid voltage continues to increase grid current flows when zero bias is reached, and develops a bias voltage across R1. RFC1 prevents shunting of the r-f input to ground through Rl, so that only the rectified dc bias current flows through R1. The current flow is from ground through cathode bias resistor R2, to the cathode, to the grid, and back through R1 to ground. The cathode bias is increased by the small amount of grid drive current, but this bias remains constant as long as grid current flows, and averages to a somewhat smaller value over the entire cycle. Because of the low value of cathode resistance employed, the over-all bias is enhanced by only a volt or two. Most of the bias voltage is developed across Rl, which is a large value of resistance (1OK to 50K). As the grid current reaches its peak, so does the plate current of V1. At this time the plate voltage of V1 reaches a minimum value, and power is absorbed by the resonant tank circuit. When the input signal reaches its positive peak and changes direction (assuming a sine wave), it swings negative and falls toward zero. Meanwhile, the plate curraent and grid current also fall. When the grid voltage drops below zero bias, the grid current stops flowing and the plate current continues to decrease, while the plate voltage increases still further. The plate voltage continues to increase, even at cutoff when the plate current ceases, because of the flywheel action of the tank circuit. At this time the tank is supplying energy to the circuit while the tube is inoperative.

When the input signal on the V1 grid reaches zero and continues further in a negative direction (the negative **half-cycle**), a positive-going signal is induced on the V2 grid through T1. Thus, as the V2 grid rises above cutoff, plate current again flows, but this time in V2. The flow of plate current causes a plate voltage drop across the high tank impedance, and the effective plate voltage of V2 follows. At zero bias, grid current flows in V2 and produces a negative bias equal to that produced by VI on the opposite halfcycle. When the grid current in V2 is at a maximum, so is the plate current, and the effective plate voltage is again at a minimum. As the input signal reaches its negative maximum and reverses direction it swings

positive, as does the plate voltage. Simultaneously, V2 plate current decreases, first zero bias and then cutoff is reached, and V2 stops conducting. Meanwhile, since the tank circuit is oscillating in synchronism, the plate voltage continues to rise until the positive peak voltage is reached. At this time  $e_{g1}$  and  $e_{g2}$  are equal to bias voltage  $E_c$  and to each other, plate current is completely cut off and the tank is again supplying energy to the circuit. As  $e_{g2}$  goes more negative,  $\mathbf{e_{g1}}$  goes more positive. When cutoff is reached VI conducts again, and the plate voltage again drops toward its minimum value. At the plate voltage minimum, the plate current is again at its maximum value (as is the grid current), and the tank again absorbs power from the plate circuit. Since the tank oscillates in synchronism, completing one oscillation for each half-cycle of input, the output is twice the input frequency. Because the tank is reinforced for each half-cycle of the input, or once for each cycle of operation, not as much power is expended from the tank as in a single-stage circuit. The plate efficiency, therefore, increases over that of the single stage, since only half as much energy is expended by the tank, and less is absorbed from the plate. As the input signal continues, the action just described is repeated over and over again. Since L4 is inductively coupled to L3, the circulating tank current induces an r-f voltage in L4 by transformer action, and the output is approximately equal to the plate voltage drop developed across one tube. Any other harmonics in the plate circuit are offered a very small impedance, since the tank is not tuned to that frequency; thus, only the desired harmonic frequency exists in the output.

Although the pulses of plate current occur for only 120 degrees and are highly distorted, the flywheel action of the tank circuit tends to smooth the output into approximate sine waves at double the frequency. Since frequency multipliers are usually never modulated, any remaining waveform distortion is of little significance.

#### Failure Analysis.

**No Output.** Lack of an input (drive) signal, loss of screen or plate voltage, an open output circuit, or defective tubes can cause loss of output. Check the plate, screen, and supply voltages with a voltmeter. For no output it is usually necessary for both tubes to be defective; if one tube is operative, the output will be reduced rather than eliminated entirely. If

cathode bias resistor R2 is open, the circuit will be incomplete and no output can occur. If r-f transformer **T1** or T2 is open or shorted, no output can occur. Lack of input (drive) is indicated by no bias voltage, as measured across RI. Likewise, no input will produce high plate and screen current because of the loss of grid bias, and thus cause the protective cathode bias voltage across R2 to be larger than normal. Similarly, if either RFC1 or RI is open, no grid bias will be obtained, and R2 will produce a larger than **normal** protective bias with no output. When in doubt, a resistance check of Ll, L2, R1, R2, and RFC1 with the power OFF can be quickly and easily made - or either an oscilloscope or a VTVM can be used to check the grids of VI and V2 for rf. If no drive exists and C2 is shorted, the tubes will show color and be damaged (if the short is prolonged), while no output will be obtained.

If screen resistor R3 or R4 is open, or if capacitor C3 or C4 is open or shorted, there will be a reduction in output, but not complete loss of output; however, if both resistors are open or if both capacitors are shorted, no screen voltage will appear and there will be no output. If either C3 or C4 is shorted, R3 or R4 will heat abnormally, show color, or smoke, and will eventually bum out. If plate choke RFC2 is open, no plate voltage will be applied to either V1 or V2, and there will be no output. A similar condition will result if C6 is shorted; in this case the supply is dropped across the r-f choke, which will probably cause it to smoke and burn out. If C5 does not resonate L3 to the proper frequency, little or no output will be developed. Check L3 for continuity with an ohmmeter, with the plate voltage OFF. Use a grid dip meter or a wavemeter to check the tank resonant frequency. If the condition of C5 is in doubt, coil L3 must be disconnected checking C5 with a capacitance checker. If secondary L4 opens, no load will appear on either V1 or V2 and a lower than normal plate current will be indicated. L4 can be checked for continuity with an ohmmeter.

A milliammeter can be inserted in the grid and plate circuits to faciliate the location of trouble. It will indicate the grid current, which shows whether sufficient drive is present; it will also indicate the plate current, which can be checked for a dip (indicating resonance) and for proper loading. A sharp dip in the plate current with very low minimum current and no output indicates that the load is not coupled sufficiently or that the output circuit is open.

Low Output. No voltage or low voltage on the screen or plate, insufficient drive, or a defective tube will cause low output. The screen and plate voltages can be checked with a voltmeter; the grid drive can also be checked with a voltmeter by measuring the grid bias voltage developed across RI. If either R3 or R4 is open, no screen voltage will be applied to VI or V2, respectively, and reduced output will result. Likewise, if either C3 or C4 is shorted, a similar condition will occur. Low screen voltage can be caused by a change in value of resistor R3 or R4, or by a leaky capacitor C3 or C4. A milliammeter inserted into the supply side of each screen resistor will indicate whether proper screen current is obtained. Inability to obtain the rated screen current at the correct voltage indicates a defective tube. If RFC2 is open or if C6 is shorted, no plate voltage will be applied to either VI or V2. In this case the screen will tend to act as the plate, get hot, and eventually be damaged (if the condition is prolonged). A high resistance due to a poorly soldered joint in the plate circuit of V1 or V2 will cause reduced voltage and output, and will usually be indicated by broad tuning of tank capacitor C5, with low plate current. If the output is low and the voltages appear normal, remove one tube at a time, noting whether the output rises or drops. A partially shorted tube can cause the output to rise when the defective tube is removed. Normally the output should drop to about half value; if no change occurs, the removed tube is probably defective.

Incorrect Output Frequency. If other than the desired output frequency is obtained, one of the tubes is probably inoperative. Since a push-push cir- — cuit can produce only even harmonics (2nd, 4th, 6th, etc.), an odd harmonic can be produced only by single-tube operation. In this case the output will usually be reduced. Normally, the tank circuit does not tune through more than one harmonic. However, in multiband equipment using shorting switches to change the inductance, it is possible for a poor or open contact to allow the incorrect value of inductance to be used, and thus cause resonance at some undesired harmonic.

#### PART 5-8.' DEFLECTION

# **DEFLECTION AMPLIFIERS**

#### General.

A deflection amplifier is intended to accept, as an input, a signal whose waveform may be simple (as in the case of a direct-current waveform) or exceedingly complex (as in the case of several fundamental frequencies in combination with a multitude of their harmonics), amplify it, and furnish an output in which the original waveform remains unchanged. An amplifier intended for use as a horizontal deflection amplifier is required to increase the amplitude of the sawtooth sweep waveform, in order to produce sufficient horizontal deflection. In radar displays of certain types, a triangular type of sawtooth waveform is used for a horizontally swept timebase. An amplifier intended for use as a vertical deflection amplifier is required to increase the amplitude-sometimes to enormous proportions-of almost any type of waveform. Since the requirements of the vertical deflection amplifier are generally more stringent than those of the horizontal deflection amplifier, insofar as gain, bandwidth, and frequency response are concerned, the following discussion will be particularly applicable to the amplifier intended for vertical deflection.

The most complex waveform which may be required to be amplified is a perfect square wave. Such a wave contains a fundamental frequency and an infinite number of odd harmonics. It has zero rise and decay times, and a perfectly flat top and bottom. The voltage changes from a maximum positive value to a maximum negative value instantaneously. In order to amplify a waveform containing an infinite number of harmonics, without distortion, an amplifier having an infinite bandwidth would be required. Such a waveform and such an amplifier do not exist, for the following reasons: Any change in voltage, no matter how abrupt, requires a certain amount of time to occur. The presence of shunt capacitance, which in some amount is always present in a circuit, causes the rate of change of voltage to be further reduced. This results from the fact that the voltage across a capacitor cannot change instantaneously. In addition, every amplifier, no matter how careful the design, introduces some degree of distortion, which deteriorates the (perfect) square wave.

In actuality, the square wave applied to a vertical amplifier contains several hundred (rather than an in-

finite number) odd harmonics. The following illustration shows the output waveforms from amplifiers in which the high-frequency response was purposely restricted. The input to the amplifiers, in each case, was a "perfect" square wave. In A, the output was restricted to the tenth harmonic of the fundamental frequency. In B the output waveform contained frequencies as high as the one-hundredth harmonic of the fundamental, while in C the output contained over five-hundred harmonics. In order to reproduce a square wave with reasonable fidelity the vertical deflection amplifier should have a bandwidth sufficiently wide to pass the tenth odd harmonic of the fundamental frequency. Note that this is a frequency which is 21 times the fundamental. More accurate reproduction of the input waveform requires a bandwidth wide enough to pass the fortieth odd harmonic (81 times the fundamental) of the fundamental frequency.



#### Output Square Waves Having Restricted Odd-Harmonic Content

A waveform having a very short time duration, such as a timing pulse, requires a different method of calculating the minimum high-frequency response required of the deflection amplifier. The minimum upper limt of response required is inversely proportional to the pulse duration, as follows:

$$f_{max} \cdot \frac{1}{d}$$

where:  $f_{max}^{\dagger}$  required minimum upper limit of amplifier response, in megahertz

#### d = pulse duration, in microseconds

As an example, a l-microsecond rectangular pulse requires a minimum frequency response which is uniform up to 1 megahertz. A 1 /4-microsecond rectangular pulse requires a minimum frequency response uniform up to 4 megahertz.

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In addition to pulse duration, the high-frequency response requirements of the vertical deflection amplifier also depend upon the rise time of the pulse to be amplified. The rise time is the time required for the pulse to increase from 10 percent to 90 percent of its maximum amplitude. The shorter the rise time required, the higher the frequency response of the vertical deflection amplifier must be to reproduce the waveform.

Finally, in order to accurately reproduce the original waveform in the amplified output, the vertical deflection amplifier must have an absolute minimum of phase shift. That amount of phase shift which is present must be proportional to the frequency of the component frequencies of the input waveform. As an example, suppose a complex waveform which is composed of a fundamental sine wave plus its second harmonic is applied to the vertical deflection amplifier. Suppose, further, that the amplifier delays the fundamental by the interval of time equal to onequarter cycle. In order to preserve the original waveform, it is necessary that the second harmonic be delayed by an equal interval of time, to maintain the time relationship between the fundamental and the second harmonic. In order to obtain the same interval of time delay, the second harmonic must be delayed by onecycle. A third harmonic, if present in the input waveform, would have to be delayed by three fourths of a cycle. By this means a linear phase shift is produced in which the angular degree of phase shift is directly proportional to the frequency ratio of the harmonic to its fundamental.

# BASIC DEFLECTION AMPLIFIER (ELECTRON TUBE)

#### Application.

The deflection amplifier is used to amplify the signals before they are applied to the deflection plates of an electrostaticdeflection type of cathode-ray tube or to the deflection coils of an electromagneticdeflection type of cathode-ray tube. Two separate amplifiers are associated with each cathode-ray tube: the horizontal deflection amplifier, which normally amplifies the horizontal sweep signals, and the vertical deflection amplifier, which normally amplifies the input waveform to be displayed on the screen of the cathode-ray tube.

#### Characteristics.

**Horizontal Deflection Amplifier.** Input impedance is high; loading of the preceding horizontal generator circuit is thereby prevented.

Input capacitance is low; attenuation of high frequencies is thereby prevented.

High-frequency response is good, but not generally as good as the response of the vertical deflection amplifier.

Bandwidth usually covers 10 Hz to 100 kHz; certain applications may require a range of 1 Hz to 500 kHz; other applications (such as fixed sweeps of radar deflection) may require only a limited range in bandwidth.

Output impedance depends on intended application: impedance is high if amplifier is designed for voltage (electrostatic) deflection; impedance is relatively low to match the impedance of deflection coil if designed for current (electromagnetic) deflection.

Gain of the amplifier depends on application; the gain is usually lower than that of the vertical deflection amplifier, because the sweep generator output normally feeding the horizontal deflection amplifier is ordinarily higher and more constant than the input signal feeding the vertical deflection amplifier.

Balanced output (push-pull) is desirable, to prevent distortion caused by unequal amplification of positive and negative signals.

**Vertical Deflection Amplifier.** Input impedance is very high; loading of the preceding output circuit, with the consequent waveform distortion, is thereby prevented. (Special applications may require a low input impedance, which must then be matched to the source impedance of the input signal.)

Input capacitance is very low; attenuation of highfrequency components of input signal is thereby prevented.

High-frequency response is very good; application generally demands a better response than that of the horizontal deflection amplifier.

Bandwidth usually covers 10 Hz to 1 Mhz; certain applications may require a range of 2 Hz to 10 MHz; other applications may require a range which includes zero hertz (direct current), but at the same time they may require only a limited high-frequency response.

Output impedance depends on the intended application, in the same manner as in the horizontal deflection amplifier. The impedance is high if the

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#### **ELECTRONIC CIRCUITS**

amplifier is designed for voltage (electrostatic) deflection; it is relatively low and must **match** the impedance of the load (deflection coil) if the amplifier is designed for current (electromagnetic) deflection.

Gain of the amplifier depends on its intended application: it must be sufficient to produce a pattern of acceptable size, on the particular cathode-ray tube used, from the smallest (voltage) input signal required to be displayed on the screen.

Balance output (push-pull) is desirable-more so than in the horizontal-in order to reduce pattern distortion and beam defocusing. Since the input signal to the vertical deflection amplifier is generally much lower in amplitude than that of the horizontal input signal, the amount of gain required of the vertical amplifier is generally higher, and hence the possibility of distortion is also higher.

#### Circuit Analysis.

**General.** The circuit discussed here is a basic type of circuit and is given only for the purpose of discussion. More detailed discussion on actual circuits used

as deflection amplifiers will be found in the two amplifier circuits to follow: Voltage Deflection Amplifier and Current Deflection Amplifier.

The following circuit is actually a simple paraphase amplifier, which is used to produce two output voltages, equal in amplitude and opposite in phase (polarity). Since 50 volts per inch is a common deflection sensitivity for cathode-ray tubes, and since the gain of the stage (Vi) is less than one, the amplitude of the input signal to this stage should be on the order of 50 volts. The input signal is applied through coupling capacitor Cl to the grid of the deflection amplifier tube, V1. The grid is returned to cathode through grid resistor R1. Plate voltage is applied through plate load resistor R4, and the cathode is biased by means of R2, which is bypassed by C2. The values of R3 and R4 are equal, and the same current passing through them will produce signals which are equal in amplitude but opposite in phase (polarity) at the plate and cathode. These two outputs, which provide push-pull deflection, are coupled through C3 and C4 respectively, to the vertical deflection plates of



Typical Deflection Amplifier Used for Vertical Deflection

cathode-ray tube V2. Equal deflection above and below a zero-voltage base line is provided by a centering control network consisting of dual control R5/R6, and resistors R7 and R8, which are bypassed by C5 and C6, respectively. Capacitors C5 and C6 insure that any electrons striking the deflection plates will be removed, to prevent a negative charge from building up. If a positive pulse of short time constant is applied at the input to the circuit, to C 1, the output at the plate of V1 will be an inverted, or negative pulse, which is shown at the top plate of cathode-ray tube V2 as a pulse below the reference voltage. The output at the cathode of V1 will be an upright, or positive pulse, which is shown at the lower plate of V2 as a pulse above the reference voltage.

#### Failure Analysis.

**No Output.** If a signal having an amplitude within the input limits of the deflection amplifier is applied to the input terminals, a defective tube is the most probable cause of a no-output condition. An open coupling capacitor Cl, a shorted grid resistor R1, an open cathode resistor R2 or R3, or an open plate resistor R4 would also be responsible for no output, as would also a power supply failure.

Reduced or Unstable Output. In the typical circuit illustrated, the failure of a component is more likely to cause a reduced, distorted, or unstable output, rather than no output whatsoever. A leaky coupling capacitor Cl or a change in value of any resistor would contribute to a reduced or unstable output. If cathode resistor R2 or R3 changed in value, the outputs from the plate and cathode would be shifted from the designed center (which may or may not be at ground potential, depending upon the designed application), and the output would be shifted with respect to the zero reference. If shifted too far, peak distortion may result. A similar condition would occur if resistor R5, R6, R7, or R8 became either opencircuited or changed in value, or if capacitor C3, C4, C5, or C6 became leaky. If capacitor C3 or C4 became open-circuited or if capacitor C5 or C6 became shorted, one half of the normal output signal would be removed from the cathode-ray tube, which would then display only the positive or the negative portion

of the signal, depending upon the half of the circuit which continued to function.

# VOLTAGE DEFLECTION AMPLIFIER (FOR ELECTRO-STATIC CRT) (ELECTRON TUBE) Application.

The voltage deflection amplifier is used to amplify the input signals before they are applied (normally) to the vertical deflection plates of an electrostaticdeflection type of cathode-ray tube. It is also used to amplify the output signals of a sweep generator, before they are applied as a horizontal sweep voltage to the horizontal deflection plates of an electrostaticdeflection CRT.

## Characteristics.

Horizontal Deflection Amplifier. Input impedance is high, thereby preventing any loading of the preceding horizontal generator circuit.

Input capacitance is low, thereby preventing the attenuation of high frequencies.

High-frequency response is good, within the design limits of the amplifier (which in many cases are more restricted than those of the vertical deflection amplifier).

Low-frequency response is good, but only in exceptional cases do the requirements demand response down to zero frequency (direct current).

Bandwidth depends on application design: usually covers a range of approximately 10 Hz to 100 kHz; special applications may require a range of 1 Hz to 500 kHz; other applications may require only a limited range, as in the switch-selected fixed sweeps used in radar deflection.

Output impedance is high, since no current need be supplied to the deflection plates of a CRT.

Gain depends on application design: as a rule it is relatively high, but not as high as that of a vertical deflection amplifier, because the input to the horizontal deflection amplifier is usually furnished by a sweep generator having an output level of appreciable value.

Balanced output, furnished by a push-pull type circuit, is desirable, in order to obtain a uniform deflection field, and avoid pattern distortion and defocusing effects inherent is single-ended output.

# **ELECTRONIC CIRCUITS**

Vertical Deflection Amplifier. Input impedance is extremely high, thereby preventing any waveform distortion due to loading of the preceding output circuit supplying the signal to be displayed on the CRT. (Special applications may require a low value of input inpedance, which must then be matched to the source impedance of the input signal. Normally this would occur only when the deflection amplifier is permanently connected to a signal source. This would not be true in the case of a deflection **amplifier** used in a test oscilloscope, which must function with widely varying source impedances.)

Input capacitance is very low, thereby preventing the attenuation of the high-frequency components of the input signaL

High-frequency response is very good, generally better than that of the horizontal deflection amplifier.

Bandwidth depends on intended application; usual range is 10 Hz to 1 MHz. Test oscilloscopes of high quality may have a vertical amplifier bandwidth covering 2 Hz to 10 MHz. Other applications, such as oscilloscopes designed for use in teletype and audio work, may require a range which includes zero hertz (direct current), but they may require only a limited range in the higher frequencies.

Output impedance is high, since only a potential difference (no current) is required by the deflection plates of a cathode-ray tube.

Gain is usually high, and a gain control is usually included in the circuit, calibrated both in step and vernier values of voltage gain and/or decibels.

Balanced output (push-pull) is desirable-more so than in the horizontal deflection amplifier, because the gain required of the vertical deflection amplifier is usually much higher than that of the horizontal amplifier, in order to obtain a uniform deflection field and reduce the effects of beam defocusing and pattern distortion.

#### Circuit Analysis.

**General.** The most versatile voltage deflection amplifiers are those used in the horizontal and vertical deflection circuits of highquality test oscilloscopes. For this reason, the discussion that follows will be directed toward this application. In this way, circuitry peculiar to other applications will, in most cases, be included in this discussion as a matter of course.

A horizontal (voltage) deflection amplifier is designed to amplify the signals from a sweep generator, and apply the amplified (sawtooth waveform) signals to the horizontal deflection plates of an electrostatic deflection type of cathode-ray tube. The sawtooth sweep voltage is applied to the grid of the amplifier tube through a potentiometer, which affords control of the amplitude of the signal used as the horizontal time base. This control is normally front-panel mounted and captioned HORIZONTAL AMPLI-TUDE. In order to amplify a sawtooth waveform of voltage whose frequency may be (in a test oscilloscope) switch-selectable to a range which may include 10 Hz and 50 kHz as the low and high limits, respectively, the high frequency response must be maintained up to 350 kHz. The reason such highfrequency response is required is that, in order to reproduce a sawtooth waveform without appreciably distorting it, it is necessary to pass all frequencies up to the seventh harmonic of the fundamental frequency of the sawtooth wave. Thus, to pass a 50-kHz sawtooth wave, a minimum bandpass up to seven times this value is required.

A vertical (voltage) deflection amplifier is designed to amplify the input signals - often extremely minute in value - which are to be displayed on the cathoderay tube screen. The waveform of the input signal may vary from one extreme - a direct current, or zero frequency - to the other extreme - a square wave whose fundamental frequency in itself is relatively high. In order to pass a signal of zero frequency, a direct-coupled amplifier is the only choice. In order to pass a square wave with reasonable fidelity, a bandpass is required that includes the tenth odd harmonic of the fundamental frequency, which is a frequency of 21 times the fundamental. Therefore, the over-all bandpass required of the vertical amplifier has an extremely wide range. High-frequency compensation is usually included in the circuit, in order to extend the high-frequency response to the limits required. The gain is usually adjustable by means of both "coarse" and "fine" controls. The coarse adjustment, when provided, usually consists of a set of resistancecapacitance networks designed to have various degrees of attenuation. The networks of resistors and capacitors are used to maintain the attenuation of any one network constant over a wide range of frequencies. The fine adjustment of vertical gain is usually a potentiometer, located in the grid circuit of some stage of amplification other than the first. Here,

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it is isolated from the critical constants of the attenuation networks (which are located in the first stage), and does not vary the input impedance presented by the circuit to the signal source.

In small and inexpensive vertical deflection amplifiers, a single output tube is sometimes used. The output signal is coupled directly from the plate of this tube to one deflection plate of the CRT, while the other deflection plate is grounded. This is an unbalanced output, and has the following disadvantage: Each time the ungrounded deflection plate goes positive, on a peak of signal voltage, the average potential of the two vertical deflection plates rises to a considerable value above that of the second anode. This causes the electrons in the beam to be accelerated to a higher velocity than that imparted to them by the second anode potential. As a result, the trace brightens on positive peaks of the signal, and the beam is not deflected as much by a given increment of signal voltage because of the higher velocity. Negative peaks have an opposite effect, in that they reduce the average potential of the deflection plates, decelerating the beam to a lower velocity. As a result, the trace is reduced in brilliance on the negative peaks, and the sensitivity is increased because the beam is deflected more than it should be by a given increment of signal voltage. These effects may be eliminated by the use of a balanced, or push-pull, type of output circuit.

In both vertical and horizontal deflection amplifiers of better design, balanced or push-pull deflection is always used. In this type of circuit, signals that are equal in amplitude and opposite in polarity are applied to both deflection plates, neither of which is grounded. The positive side of the high-voltage power supply, which is connected to the accelerating anode of the cathode-ray tube, is grounded. These connections produce a minimum difference of potential between the accelerating anode and the deflection plates. As a result, two advantages are realized: First, the effect of the accelerating anode potential in distorting the deflection field is minimized, because of the fact that as one deflection plate is charged to a potential which is positive with respect to the accelerating anode (which is at ground potential), the opposite deflection plate is simultaneously charged to a potential which is an equal amount negative with respect to the accelerating anode. Under these conditions, a line of equal potential midway between the two charged plates is maintained at the same potential (ground) as that of the accelerating anode. This results in a minimum of beam defocusing and pattern distortion. The second advantage of the positivegrounded connection of the high-voltage power supply is that no high-voltage insulation is required between the accelerating anode and the deflection plates and their associated circuitry. In this respect the problems common to high-voltage circuitry, such as corona and high-voltage breakdown, are eliminated from the region of the cathode-ray tube which includes the neck, the flared portion, and the face (screen), as well as from the output circuits of the deflection amplifiers which feed the signals to the deflection plates. The high (negative) voltage is contained within a small portion of the tube neck at the base, wherein are located the filament and cathode. and the first anode.

Circuit operation. The following schematics illustrate two common types of deflection amplifiers used for electrostatic deflection. The first shows a phase inverter used to obtain two output voltages, equal in amplitude and opposite in polarity, from a single-ended input signal. In this circuit, the input signal, which is shown as a positive pulse, is applied through a coupling capacitor, Cl to the grid of a triode amplifier, V1. The grid is returned to ground through grid resistor RI. The amplified output, which is a negative pulse due to phase inversion in the tube, is taken from the plate and applied, through coupling capacitor C3, to one of the vertical deflection plates of the cathode-ray tube, V3. The plate voltage is applied through plate load resistor R3 and potentiometer R4. The negative output puke at the plate of V1 also appears across R3 and R4, which act as a voltage divider. A reduced value of the negative output pulse is taken from a tap on the voltage divider \_ by means of potentiometer R4 and applied, through coupling capacitor C2 and resistor R6, to the grid of the phase inverter tube, V2. Resistor R2 serves as the grid return for this tube. The output at the plate of V2 is a positive pulse, the amplitude of which is exactly equal to (although of opposite polairty) the amplitude of the output of V1, provided that potentiometer R4 is properly adjusted to furnish the correct value of signal input voltage to the grid of V2. This positive pulse output of V2 is coupled, through C4, to the other vertical deflection plate of the cathoderay tube, V3. In this manner, equal and opposite signals are applied to the two deflection plates, to protide a balanced deflection.

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Typical Phase Inverter Used as Voltage Deflection Amplifier

A shift circuit is usually included as part of a deflection amplifier for electrostatic deflection, by means of which the electron beam of the cathode-ray tube may be positioned in the exact center of the screen, or may be moved to any desired initial position under conditions of no input signal. Although the shift circuit is not, in a strict interpretation, actually part of the deflection amplifier (because the amplifier furnishes its output at the point of coupling to the CRT - at coupling capacitors C3 and C4 in the previous schematic), it is usually shown along with the amplifier circuitry in order to show the complete load circuit. In the illustration shown, the shift circuit is composed of equal resistors R7 and R8, isolation resistor R1O, and potentiometer R9. The bottom deflection plate of cathode-ray tube V3 is fixed at a potential half-way between +250 volts and ground, by the voltagedivider action of resistors R7 and R8. When the adjustable arm of potentiometer R9 is set exactly half-way between the two ends of its resistance, the voltage at this point - which is furnished through isolation resistor R1O to the top deflection

plate - will be exactly equal to the voltage at the junction of R7 and R8. Hence, the fixed dc voltages applied to the top and bottom deflection plates will be equal, and the electron beam will be positioned midway between them. By adjusting the movable arm of potentiometer R9 away from its center position, the top plate of the CRT may be made positive or negative with respect to the bottom plate, thereby positioning the beam above or below the center position on the screen.

The second type of deflection amplifier used for electrostatic deflection is the paraphase amplifier, shown in the following illustration. In this type of circuit a balanced output is obtained from a singleended input signal by means of common coupling in the cathode circuit of both tubes, **which** accounts for the circuit being known as a cathode-coupled paraphase amplifier. The input signal, again shown as a positive pulse, is applied through coupling capacitor Cl to the grid of triode amplifier VI, with the grid returned to ground through grid resistor RI. Cathode bias is obtained by means of cathode resistor R2,

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Typical Paraphase Amplifier Used as Voltage Deflection Amplifier

which is common to both VI and V2. Since R2 is unbypassed, the input signal at the grid of VI also appears at the cathode, while the inverted signal appears at the plate as one output of the circuit. The signal at the cathode of VI is applied, through direct connection, to the cathode of V2. The grid of V2 is connected to a balance potentiometer which acts as a voltage divider between Ebb and ground, to furnish the proper bias so that the output signal of V2 can be adjusted to equal that of V1. The positive pulse at the cathode of V2 will increase the bias, decrease the plate current, and produce a positive output at the plate of V2. The output signal at the plate of V2 is reversed in polarity from the input signal, as in any ordinary vacuum-tube amplifier. But, because the input to V2 is the signal voltage developed across cathode resistor R2, and because this signal is applied to the cathode of V2, which has its grid returned to ground through R5 and is thereby at ground potential insofar as the signal is concerned, the output signal at the plate of V2 has the same polarity as the input signal at the cathode of V2 or the input signal at the grid of V1. In this way, the output signals from the plates of VI and V2, which are applied to the deflection plates of the CRT, are equal in amplitude but opposite in polarity (phase). Resistors R5, R6, and R7 and potentiometer R8 comprise a shift circuit which allows the electron beam to be positioned on the screen of the cathode-ray tube as desired, in the " same manner as described in the preceding typical phase inverter circuit.

The previous circuit operation and schematics have, for simplicity, omitted the additional compensation networks which are often included in specific applications. In order that deflection amplifiers do not restrict the bandwidth of the input signal, they must have wide frequency response, low distortion, and time delay proportional to frequency, similar to the characteristics of video amplifiers. Compensation circuits similar to those discussed under the paragraphs on Video Amplifier Circuits are used in

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deflection amplifiers, depending upon the amplifier design and intended application.

# Failure Analysis.

No Output. Assuming that a signal of proper amplitude (and polarity if the deflection amplifier is specifically designed for single-polarity pulse operation) is applied to the input terminals, a defective tube should first be suspected as the cause of a nooutput condition. An open input coupling capacitor Cl, a shorted grid resistor R1, or an open common cathode resistor R2 (refer to paraphase amplifier circuit diagram), or a faihrte of the power supply would individually be responsible for no output. An open plate resistor on the input side of the circuit (R3 in the illustrations) would also result in no output. Components peculiar to a specific circuit may also be cause of circuit failure. As an example, referring to the second illustration on a typical paraphase amplifier, if plate resistor R4 became shorted, the high value of plate current that would flow through V2 would of course flow through the common cathode resistor, R2. As a result, both cathodes would be at a high positive potential. The grid of VI would therefore be highly negative with respect to its cathode, and might possibly be biased beyond cut off. No signal output would thereby be obtained.

Reduced or Unstable Output. In both of the typical circuits illustrated, a number of conditions could contribute to a reduced, distorted, or unstable output. The failure of out-of-phase amplifier tube V2, its plate resistor, or its output coupling capacitor; if open, would be responsible for an output of approximately one-half the normal amplitude. An open output coupling capacitor from the plate of VI would also result in an output signal of one-half normal amplitude. A change in the value of input grid resistor R1 would change the input impedance to the stage; this might affect the amplitude and possibly the waveform of the input signal. An open-circuited positioning potentiometer or its associated resistor (R9, R1O in typical phase inverter circuit; R7, R8 in typical paraphase amplifier circuit) would prevent the positioning of the waveform display on the screen of the CRT in the normal manner. An open resistor in the voltage divider connected across the positioning potentiometer (R7 or R8 in the typical phase inverter circuit; R5 or R6 in the typical paraphase amplifier circuit) would also be responsible for the failure of the positioning potentiometer to properly position the waveform display on the CRT screen.

# CURRENT DEFLECTION AMPLIFIER (FOR ELECTROMAGNETIC CRT (ELECTRON TUBE)

# Application.

The current deflection amplifier is used to amplify input signals before they are applied (normally) to the vertical deflection coils of the deflection yoke used with an electromagnetic-deflection type of cathode-ray tube. In addition, it is used to amplify the sweep signals which are used as a time base before they are applied (normally) to the horizontal deflection coils of the deflection yoke used with an electromagneticdeflection CRT.

## Characteristics.

**Horizontal Deflection Amplifier. Input** impedance is high; loading of the preceding horizontal generator circuit is thereby prevented.

In put capacitance is low, attenuation of high frequencies is thereby prevented.

High-frequency response is very good: must be so to avoid the possibility of distorting the trapezoidal input waveform of voltage which is required to produce a sawtooth waveform of current through the horizontal deflection coils.

Low-frequency response is good, but does not include zero frequency.

Bandwidth depends on application design: may cover a range of 10 Hz to 100 kHz, but the range is usually more limited because the specific application normally requires only a few fixed sweep frequencies.

Output impedance is relatively low, and must be matched to the load (deflecting coil) for maximum transfer of current with minimum waveform distortion. This requirement acts to restrict the bandwidth.

Gain depends on application design: the current gain (power gain) is usually high, but the voltage gain may be low—even less than one.

Balanced output, furnished by a push-pull type circuit, is desirable, in order to obtain a uniform deflection filed. However, the principal applications of the electromagnetic deflection type of cathode-ray tube, namely, radar and television, do not require the precise duplication of the input waveform that is essential in the principal applications of the electrostatic deflection CRT, namely, waveform analysis and complex wave amplitude measurement.

Vertical Deflection Amplifier. Input impedance is normally extremely high, in order to prevent any

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waveform distortion due to loading effects on the circuit supplying the input signal. However, since any particular application of an electromagnetic deflection type of **cathode-ray** tube normally operates with a permanently connected input circuit, the input impedance of the amplifier maybe of a fairly low value, which must be matched to the source impedance of the input signal.

Input capacitance is low, in order to prevent the attenuation of high frequencies.

High-frequency response is very good: must be so in order to respond to extremely sharp input pulses without introducing appreciable time delay.

Low-frequency response is good, but does not include zero frequency.

Bandwidth depends on application design: may cover a range of 10 Hz to 100 kHz, but the range may be more limited when only the leading edge and the length of an input pulse, and not the shape of the top of the pulse, is of consequence, as in pulse display applications (radar).

Output impedance is relatively low, and must be matched to the load (deflecting coil) for maximum current transfer with minimum waveform distortion.

Gain depends on application design: the current gain (power gain) is high, but the voltage gain maybe low.

Balanced (push-pull) output is desirable, both from the standpoint of the high power output with minimum distortion required for magnetic deflection, and the need for an absolute minimum of beam defocusing when pinpoint radar target presentation is required.

# Circuit Analysis.

**Generel.** The deflection of the electron beam in an electromagnetic deflection type of cathode-ray tube is proportional to the strength of the magnetic field set up within the tube, which is in turn proportional to the value of current passing through the deflection coil. Since it is desirable to deflect the electron beam linearly, the current through the coil must increase linearly with time. When the end of the sweep is reached, the electron beam must be returned to its starting point quickly. The current wave required for electromagnetic deflection must therefore be of sawtooth shape if the resultant sweep is to be linear. It should be observed that it is the *current* wave which must be of sawtooth shape for an electromagnetic

tube, not the voltage wave as in an electrostatic tube.

The deflection coils, through which the deflection amplifier output current flows, consist of wire wound around either a non-magnetic core or an iron core. The wire used in the coil has, in addition to the desired inductance, some amount of resistance. As a result, the sawtooth current must flow through the equivalent of a series resistive-inductive (R-L) circuit. Since a square wave of voltage will produce a sawtooth wave of current in a pure inductance, while a sawtooth wave of voltage will produce a sawtooth wave of current in a pure resistance, the combination of a square wave and a sawtooth wave of voltage is required to produce a sawtooth wave of current in a circuit containing both resistance and inductance. Such a combined waveform has the shape of a trapezoidal waveform of voltage. This, then, is the waveform which must be amplified by the current deflection amplifier.

Circuit Operation. The accompanying schematic illustrates a simplified typical deflection amplifier for producing a horizontal time base using magnetic deflection. The input signal, which is a trapezoidal waveform of voltage as shown in the illustration, is applied through coupling capacitor C1 to the grid of pentode amplifier VI. The amplifier is operated as a Class A stage, with fixed bias applied from a negative power source. Sufficient bias is applied to the grid, through grid resistor R1, to prevent the grid from going positive with maximum signal input, The amplifier tube, Vl, is a pentode or a beam power type, in order to obtain the power amplification that is required to furnish sufficient current to the deflection coil. This coif may require between 50 to 100 milliamperes of current for maximum beam deflection. The output of VI is applied to the deflection coil, which in the illustration is presented by an inductance, L1, with a resistance, R2, in series with it, shown as a dotted resistance because it is actually a part of LI. The output voltage waveform at the plate of V1 is trapezoidal. when this waveform is applied to the series R-L circuit (deflection coil), the voltage waveform appearing across the resistance is resolved to a sawtooth shape, while that appearing across the inductance is resolved to a square-wave shape. The square wave of voltage across the inductance causes a sawtooth wave of current through it, which is the required waveform for producing a horizontal time base deflection on the screen of the cathode-ray tube.



Typical Current (Electromagnetic) Deflection Amplifier

The development of the sawtooth current waveform from the trapezoidal voltage input waveform is shown in the following illustration. The trapezoidal voltage input waveform to the grid of amplifier VI is shown at A; differentiated voltage which appears across the inductance is shown at B; the integrated voltage which appears across the resistance (of the coil) is shown at C; the current through the deflection coil, which is the composite result of waveforms B plus C, is shown at D.

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## AMPLIFIERS



Development of Sawtooth Current Waveform in Deflation Coil from the Trapezoidal Voltage Waveform Input to Amplifier

A second circuit for producing a horizontal time base for magnetic deflection is shown in the following illustration. The input signal to this amplifier is a square wave, instead of the trapezoidal wave required in the previous circuit. This signal is applied, through coupling capacitor Cl, to the grid of a pentode or beam power amplifier, VI. The grid is returned to ground through resistor RI. The positive voltage applied to the cathode of VI, from the plate supply by means of the voltage-divider action of resistor R3 and cathode resistor R2, maintains V1 biased to cutoff in the absence of an input signal. When the first positive pulse of the input square wave reaches the grid, the tube conducts heavily. The resulting plate current, flowing through deflection coil L2 and inductor L1, rises exponentially toward a value which would be limited only by the resistance of the circuit. Before this limiting point is reached, however, conduction of the tube is suddenly interrupted by the negative-going end of the square-wave input pulse. In this way, only a relatively linear portion of the exponentially rising waveform is utilized. When the conduction of the tube is interrupted at the end of the positive square wave, V] is cut off, and the current decays rapidly to zero. This rapid decay is due to a change in the time constant of the circuit between the rise and fall of the current. During the rise of current, the circuit time constant (which is given as inductance divided by resistance, or L/R) is long, because of the large value of inductive reactance (due to the large inductance) and the small value of resistance in the circuit. The resistance is composed of cathode resistor R2 and the low value of plate resistance of V1. During the decay of current, the time constant is made short, as a result of the increase in the value of plate resistance when V1 stops conducting. With the shortened time constant, the current decays rapidly. The additional value of inductance in the circuit due to inductor L1 increases the time constant, to produce a slow build-up of current. Inductor L1 maybe effectively removed from the circuit, by shorting across it, when faster sweep deflection rates are required.



Current (Electromagnetic) Deflection Amplifier Utilizing Square-Wave Input

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The sudden decay in current flowing in the deflection coils, when the tube stops conducting, causes a counter e.m.f. to be produced in the coil which opposes the current decay. In addition, the circuit may be shock-excited into oscillation by the sudden change in value of current. Although the oscillations gradually die out, they may continue into the following sweep, especially if the circuit Q is high. This condition may result in a nonlinear start of the buildup of current in the coil, and therefore a nonlinear sweep, as shown in the following illustration.



Undamped Oscillations in Deflection Coil Current

These oscillations may be eliminated, or damped out, by lowering the Q of the circuit by means of a resistor shunted across the coil. However, this wastes some of the deflection current; a more satisfactory method incorporates the use of a damping diode shunted across the deflection coil, as shown in the following illustration. In this circuit, diode V2 acts to damp out the oscillations in the following manner: When the current through V1 is increasing (during the rise of the sawtooth, current wave shown in the illustration above) to provide the sweep deflection, the voltage at the plate of VI is lower than the plate supply voltage by the amount of voltage drop in the deflection coil and inductor. The cathode of damping diode V2 is therefore more positive than its plate, and the diode will not conduct. When the current through V1 falls to zero (at the end of the sawtooth current wave illustrated), the voltage at the plate tends to rise above the plate supply voltage due to the fact that the counter e.m.f. generated by the inductance adds

to the plate supply voltage. When this condition is reached, damping diode V2 conducts, and any oscillations are dissipated in resistor R5



Deflection Amplifier Output Circuit With Damping Diode Added

Balanced output (push-pull) circuits, when used, usually operate by means of a phase inverter circuit fed from a single-ended source, as described in the previous circuit on Voltage Deflection Amplifiers. In some cases in radar deflection circuitry, the two outputs obtained by means of a phase inverter are separately amplified by individual single-ended deflection amplifiers, and then applied to the two separate windings of a split-winding deflection yoke.

#### Failure Analysis.

**No Output.** Assuming that a signal of proper amplitude and waveform (square wave or trapezoidal wave, depending on circuit design) is applied to the input terminals, a defective tube would be the most likely cause of a no-output condition. If the tube is found capable of operation, an open input coupling capacitor Cl or open grid resistor RI, or open cathode or screen resistors, if used, may be the cause of no output. Since a currentdeflection amplifier is characterized by a relatively high value of platecurrent flow, a common source of trouble is an open deflection coil. If the coil is open-circuited, and the circuit is similar to these previously shown under Circuit Operation, the application fo screen voltage to

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the tube with no plate voltage present may result in a burned out tube or poor emission, because of excessive screen current. The same condition may prevail if the deflection coil is remotely located from the amplifier, and the interconnecting cable is inadvertently disconnected during operation. No output may also be due to failure of the plate-voltage supply.

Reduced or Unstable Output. A change in value of almost any of the circuit components, due to age or partial failure, may contribute to a reduced output. If the capacitance of input coupling capacitor Cl changed or the resistance of grid resistor RI changed, the output would be affected. If the cathode bypass capacitor (if one is used) became either open or shorted, the bias would be changed, resulting in either decreased output due to degeneration (if open) or distortion due to no bias (if shorted). If the circuit incorporates fixed cathode bias obtained through a voltage divider from the  $E_{bb}$  line, an open reSIStOr on the  $E_{bb}$  side of the cathode (R3 in the second circuit illustrated) would interrupt the fixed bias, and the circuit would operate with self-bias, which may produce distortion under high signal input conditions. A decrease in the voltage of the plate supply, due to faulty operation, would also be responsible for a reduced output.

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PART 5-9. OPERATIONAL AMPLIFIERS

# **OPERATIONAL AMPLIFIERS**

#### General.

The operational amplifier is a high-gain dc amplifier utilizing negative feedback to establish and control precise gain. An operational amplifier may be used to perform mathematical operations such as addition, subtraction, multiplication, and division, or to provide special waveforms or voltages. This type of amplifier is used especially for analog computation and instrumentation, and in special systems design. Analog computation differs from logic computation in the manner in which it is accomplished. The information applied to a digital computer is separated into and handled in discrete measurable steps (digits), whereas the information applied to an analog computer is usually slowly varying ac or dc voltages. For example, a sawtooth voltage could easily represent the acceleration of an airplane. The slope of the sawtooth could represent the magnitude of the acceleration; the starting level of the slope could represent the initial velocity, and the final level of the slope could represent the final velocity of the airplane. Thus, complex analog problems are solved by operational amplifiers, using resistive input and output networks and high-gain dc amplifiers.

Operational amplifiers are named for their function. For example, the summing amplifier produces an output voltage that is proportional or equal to the sum of the inputs. A difference amplifier acts as a subtracter, producing an output equal to the difference between the input voltages. Similarly, the exponential amplifier produces an exponential output, and the derivative amplifier produces the desired derivative. The logarithmic amplifier, in turn, produces a logarithmic output. Each of these mathematical types of operational amplifiers is fully discussed later in this section. The combining and coincidence amplifiers are considered as special nonmathematical operational circuits.

# COMBINING AMPLIFIER (ELECTRON TUBE)

## Application.

Combining amplifiers are used in transmitter modulation stages, or in combining circuits of television transmitters, where it is necessary to combine two or more signals to obtain an output proportional to each input.

## Characteristics.

Uses a common plate load resistor. Has two or more inputs. Uses a separate amplifier for each input. May be dc coupled or capacitively coupled. Uses **triode** electron tubes. Uses cathode bias.

#### Circuit Analysis.

**General.** The combining amplifier produces an output which is the result of two or more input signals not necessarily of the same shape, phase, or frequency. Each input signal is applied directly to the grid of a separate electron-tube amplifier through a resistive voltage-divider network. The amplified output of each tube is developed across a common plate-load resistor, resulting in an overall output which is the combination of all input signals.

**Circuit Operation. A schematic** of a typical combining circuit is shown in the accompanying illustration. Potentiometer RI and resistor R2 form a voltage driver which couples an input signal to the grid of triode V]. Potentiometer R4 and resistor R5 form a voltage divider which couples an input signal to the grid of triode V2. Resistor R3 is the cathode bias resistor for Vl, and capacitor C1 is the cathode bypass capacitor. Resistor R6 is the cathode bias resistor for triode V2 and capacitor C2 is the cathode

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bypass capacitor. Resistor R7 is the common plateload resistor used by both VI and V2.



**Combining Amplifier** 

The amplitude of the input signal applied to the grid of V1 is determined by the setting of potentiometer R1, and the input signrd applied to V2 is, likewise, determined by the setting of potentiometer R4. By using R2 in series with the grid of VI, and R5 in series with the grid of V2, the grid circuits are effectively held at a high impedance, and the shunting effect of R1 and R4 on the respective grid input circuit is minimized. At the same time, overdriving of the grids is limited, since any grid current flow through R2 or R5 will develop an opposing negative bias and reduce the drive.

Normally both tubes are biased so that they are operating at approximately the same plate current. Thus, equal changes of grid voltage produce equal plate current variations and maintain a linear inputoutput relationship. When the grid of VI is driven in a positive direction, plate current will increase and produce a negative swing across load resistor R7. Since R7 is common to both tubes, if the grid of V2  $\checkmark$  is also driven positive at the same time as V1, the total plate current will be equivalent to the combination of both input signals at that instant. In this example, the circuit is acting as an adder. On the other hand, if one input is decreasing while the other input is increasing, the total plate current and voltage swing across R7 will represent the difference between the two signals.

Since the output voltage is developed by the separate plate currents of VI and V2 flowing through a common load resistor, the output waveform at any instant is the combination of the two input signals. -Hence, applying a sawtooth waveform to one input, and a rectangular waveform to the other input, will produce an output waveform which contains both sawtooth and rectangular signal components, and will be the composite waveform produced by both signals. Because of the normal phase inversion or polarity change produced by the tube amplifier, the combined output will be out-of-phase with respect to the input. Where an output of the same phase or polarity as the input is desired, an additional stage of linear application will be required. The combining circuit is used when it is desired to combine the outputs of two separate channels to control a third channel.

## Failure Analysis.

**No Output. Loss of output** can result from a defective plate supply voltage source, Ebb, or if resistor R7 is shorted or open. Loss of output can also occur if a failure exists in each of the individual amplifiers. Both triodes VI and V2 can be defective, both cathode bias resistors or both grid resistors can be open, or both input potentiometers maybe open.

Output voltage can not be developed if plate load resistor R7 is open or shorted. If the plate supply voltage source is defective, triodes V1 and V2 will not be supplied with either plate voltage or plate current to develop an output.

If plate load resistor R7 and the plate supply voltage source are not defective, there must be a defective component in both amplifier circuits. Consider first the circuitry associated with electron tube V 1; if the correct signal voltage is present at the grid of VI and no output is obtained from VI, cathode bias resistor R3 may be open, or tube V1 itself maybe defective. If potentiometer RI is defective, no sighai will appear at the grid of V 1 and no output will be obtained from  $\checkmark$ this stage. By the same reasoning, if resistor R4 is

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open, no signal will appear at the grid of V2, and no output will be obtained from V2.

An open grid resistor R5 or cathode resistor R6 will prevent an output signal from being obtained from V2. If the proper signals and proper voltages are available on the elements of V2, but no output is developed, the electron tube is probably defective.

Low or Distorted Output. A low or distorted output will be developed if the plate supply voltage is not the proper value, or if plate load resistor R7 is not the correct value. If either or both bypass capacitors C 1 and C2 are defective, or cathode resistors R3 or R6 are shorted, the output may be distorted. Defective electron tubes may also beat fault.

A lower than normal plate supply voltage or improper bias will cause the triodes to be operated over the nonlinear portion of their plate current-grid voltage characteristic curve. This will result in distortion of the output waveform. Shorted grid resistors R2 or R5 will allow a greater signal amplitude to appear at the grid of V1 or V2. This may drive the tube into saturation.

If one of the tubes is weaker than the other, a low output will be obtained, even though the voltages and parts of each amplifier stage test normal.

# COMBINING AMPLIFIER (SEMICONDUCTOR)

## Application.

Combining amplifiers are used to provide a single output which is equal to the combination of two or more input signals not necessarily of the same waveshape or frequency. The combining amplifier is used in transmitter modulator stages or in the combining circuits of television transmitters.

## Characteristics.

Two transistor amplifiers are connected provide a common output.

Output signal is developed across a common load resistor.

Two or more simultaneous inputs are necessary.

## Circuit Analysis.

**General.** Two or more input signals not necessarily of the same shape, phase, or frequency, are combined to produce an output which is the result of these signals. Each input signal is applied directly to the base of individually grounded emitter PNP transistor amplifiers. The output of each amplifier is developed across a common collector resistor. The resulting output is then the combination of all input signals.

**Circuit Operation.** A typical schematic of a combining amplifier using the common-emitter arrangement is shown in the accompanying illustration. In the circuit, **Q1** and Q2 are two identical PNP type transistors. The output impedance of the preceding stage is used to develop forward base bias for Q1 and Q2. The emitters of both transistors are grounded, and the collectors of both transistors are comected to the same end of common load resistor RI.





Assume that a positive-going rectangular input waveform is applied to the base of Q1, and a negative rectangular input waveform of one half the frequency, but with the same amplitude as the input to Ql, is applied to the base of Q2. The output which is produced across the collector load resistor contains the amplified resultant voltages of the two waveforms.

For ease of circuit explanation refer to the accompanying input and output waveform chart. At time \*O, both transistors have equal forward bias and no input voltage applied, and are in their quiescent or resting condition. At this time, the total of both collector currents produces a positive' voltage drop across common load resistor R1, and reduces the collector voltage applied to Q1 and Q2 to its normal resting value. At time '1, the positive-going leading edge of the pulse applied to the base of Q1 drives it

more positive and reduces the forward bias. The collector current of Q1 is correspondingly reduced, and the collector voltage tries to rise toward the negative supply value. At the same time, the negative leading edge of the input pulse applied to Q2 increases the forward bias, and the collector current of Q2 increases. Assuming equal amplitude inputs and matched transistors, the opposing changes in collector current through common collector resistor R1 balance each other out, so there is no effective change in current flow and voltage across RI. This condition occurs continuously from time <sup>t</sup> 1 to time '2. During this time, the output remains at its normal resting level as shown in the waveform chart.



Input and Output Waveform Relationships

At time '2, the input pulse on Q] reaches its trailing edge, driving the base of Q1 in a negative direction and increasing the forward bias. The collector current of Q1 now increases, and adds to the collector current drawn by Q2 which still has a negative – pulse (forward bias) applied. With twice the normal collector current flowing through RI, the total collector voltage is decreased, and a positive-going output spike of voltage is produced. This positive output voltage continues for the duration of the negative portion of both input pulses from time '2 to time '3.

At time '3, both input pulses end and the trailing edges both drive the bases of Q 1 and Q2 positive, reducing the forward bias on both transistors. Consequently, the collector current of Q1 and Q2 flowing through R1 is reduced to twice the normal value, producing a negative-going output voltage swing as the collector voltage rises toward the supply value. This negative output voltage continues during the steady-state condition of the input pulses between times '3 and '4. At time '4, the trailing edge of Q1 input pulse drives the base of QI negative, increasing the forward bias. The collector current of Q1 increases, and the output voltage tends to rise in a positive direction as the collector voltage of Q1 decreases. However, the positive pulse applied to Q2 base still continues to keep the forward bias reduced, dropping the collector current of Q1. At this time, the increase of collector current through Q1 exactly balances out the decrease of collector current through Q2, and the opposing currents cancel so that no output is produced. Thus, the total output voltage returns to its normal resting value (the zero output level) between times '4 and '5 (the input voltages are again canceling each other in the output). At time <sup>t</sup>5, the positive pulse applied to Q2 ends, and the trailing edge of the pulse drives O2 base is a negative direction until the collector current of Q2 is returned to its normal resting value. At the same time, the leading edge of the input pulse applied to the base of Q] drives the base positive, reduces forward bias, and reduces Q2 collector current. During the interval from <sup>t</sup>5 to <sup>t</sup>6, Q2 collector current remains at the resting value, and Q 1 collector current is less than normal. Thus, the collector voltage of Q 1 increases negatively toward the supply value. Because Q2 is resting in its quiescent condition and only the current in Q 1 is reduced, the negative output voltage is only half the amplitude produced when both transistors are operating. At time <sup>t</sup>6, the positive input pulse on Q1 base ends, and the negative trailing edge of the pulse increases the forward base bias and returns Q1 to its normal forward-biased condition. Hence, normal collector current of Q 1 occurs, and, since no

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input pulse is applied to Q2, both transistors rest in the quiescent condition, effectively producing no output. At time '7, if the pulses are continued, the cycle of operation described above repeats.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low vrdues of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

**No Output. No** output may be the result of defective supply voltage, a defective output resistor, or a defective transistor. With no collector voltage available for either transistor, no output can be produced. This lack of collector voltage may be the result of a faulty collector supply voltage source ( $V_{CC}$ ), or a shorted or open collector resistor RI. If neither  $V_{ec}$  nor RI is defective, both QI and Q2 must be defective in order to produce no output.

Low and Distorted Output. Since there are only four components which make up this circuit, and two of them (R1 and  $V_{ce}$ ) would not produce an output if either were defective, a low and distored output will result if either Q1 or Q2 is defective. In this case, the output of the good transistor alone would produce the total output voltage of the circuit, and no combining action would occur.

#### COINCIDENCE AMPLIFIER (ELECTRON TUBE)

#### Application.

The coincidence amplifier is mainly used in analog and digital computers. It is used to control the repetition frequency and pulse duration of a given signal by producing an output only when two simultaneous input signals are present.

## Characteristics.

Requires a multigrid type of tube such as a pentode.

Simultaneous inputs are applied to the control grid and the suppressor grid.

Tube is normally held at plate current cutoff by a large negative bias voltage.

A clipping circuit within the amplifier clamps the output to a constant amplitude.

#### Circuit Analysis.

**General. The** coincidence amplifier uses a pentode operated below plate current cutoff. An input signal applied to the control grid does not drive the tube above cutoff unless another signal is applied to the suppressor grid at the same time. When both signals are present, the tube conducts and the output is held at a constant level by a clipping circuit within the amplifier. In effect, the coincidence amplifier functions as a gated amplifier, which only operates when switched on by simultaneous input signals.

**Circuit Operation. The** schematic of a coincidence amplifier is shown in the accompanying illustration. Input signals are applied to the suppressor and control grids of pentode VI through resistors RI and R2. Resistor R5 is the cathode-biasing resistor, and capacitor Cl is the cathode bypass capacitor.



#### coincidence Amplifier

Resistor R4 is a clamping resistor, which limits the output to a certain level. The highly negative bias voltage ( $E_{cc}$ ) is applied to the control grid of VI through isolating resistor R3. The screen grid and plate of V1 are furnished with positive dc supply voltage from a common source. Plate load resistor R6 drops the plate voltage to a lower positive value than the screen grid supply voltage. The output voltage is obtained between the plate of VI and ground, developed by plate current flow through R6.

The primary input signal (input-1) is applied to the control grid of V1 through resistor R2. This voltage can not by itself raise the tube grid out of the cutoff

region. The output voltage thus remains at a value slightly less the plate supply voltage. The second input signal (input-2) provides a large positive gating potential on the suppressor grid and overcomes the fixed negative grid bias. When the primary input signal occurs at the same time that the second input signal is applied to the suppressor grid, the pentode conducts.

As shown in the following illustration, an output will be present only at those times when both input no. 1 and input no. 2 are positive at the same time (in coincidence). As the conduction and plate current through R6 increases, the plate voltage decreases by the drop across R6. Plate current is prevented from increasing above a certain level by a suppressor gridto-cathode feedback voltage. This voltage is developed across resistor R4 when the peak input to the suppressor is large enough to cause the suppressor grid to draw current. (Electron flow from the cathode to the suppressor grid of V1 and ground through R4 develops a negative voltage, which opposes the applied suppressor signal voltage.) The flow of suppressor current also causes the cathode to become more positive, thus increasing the cathode bias voltage and retarding tube conduction. The amplitude of the plate output voltages is then held constant by the combined effect of the retarding suppressor and cathode bias voltages, regardless of the amplitude of the input pulses.



#### Failure Analysis.

**No Output.** Lack of filament supply, screen grid or plate supply voltage, a defective electron tube, an open input or output circuit, as well as improper bias, can produce a no-output condition.

A lack of plate voltage, measured between plate and ground, can be caused by open plate load resistor R6. In this case, the screen grid will also glow red, due to an overload, since the electron flow is attracted to the screen. If there is no plate or screen voltage, the plate supply voltage source is probably defective.

When no output exists, but there is a higher than normal plate voltage, plate load resistor R6 may be shorted or tube V1 may be defective.

An open cathode circuit will result if cathode resistor R5 is open. Check the resistance of R5. No filament voltage will also cause a loss of output. This condition can result from a defective filament supply source or defective tube.

An open control gain or screen grid resistor (RI or R2) will prevent a signal from being applied to the supressor grid or control grid. Check RI and R2.

If none of the components is open or shorted and voltages present on the elements of the electron tube are of the proper value, pentode V1 is probably defective.

Low or Distorted Output. Defective grid, bias or plate supply resistors, or an open or shorted cathode capacitor Cl can cause low or distorted output voltage.

An improper voltage on the control grid of V1 indicates that control grid resistor R2 may be open, or that biasing resistor R3 may be open or shorted. A shorted suppressor grid resistor, RI, or an open or shorted clamping resistor, R4, will be indicated by improper voltage on the suppressor grid of V]. If RI <sup>-</sup> were shorted, only the output would be lowered, but if R4 were shorted, the output would not be clamped at a specific level, and would depend on the input level.

The cathode VI may measure an incorrect potential because cathode biasing resistor R5 is defective, or because cathode bypass capacitor C 1 is open or shorted. A shorted bypass capacitor is indicated by

**no** voltage at the cathode. An open cathode resistor will usually indicate above normal voltage, since the meter multiplier will act as the cathode resistor.

## DERIVATIVE AMPLIFIER (ELECTRON TUBE)

#### Application.

The derivative or differentiation amplifier is used in analog computers and control circuits to develop an output voltage which varies negatively as the derivative of the amplified input voltage.

#### Characteristics.

Has a low input and low output impedance.

Uses a capacitive input network.

Uses negative feedback.

Operation of the amplifier is based on resistancecapacitance time constant relationship.

Output is 180° out of phase with input.

## Circuit Analysis.

**General.** The derivative amplifier develops an output which is the differentiated value of the input voltage. This output is developed by the relationship between the input capacitor and a feedback resistor of a triode operational amplifier. The r-c time constant, which determines the exponential decrease of current, is the product of the capacitor and the feedback resistor. The exponentially varying current flows through the capacitor, the triode, and the feedback resistor value equals the output voltage value at any given time. The output voltage, then, varies exponentially as the current varies.

**Circuit Operation. The** one-line diagram of a derivative amplifier is shown in the accompanying illustration. It shows a derivative amplifier in simplified form. The triangle represents the basic operational amplifier circuitry, so that only a capacitive input and a resistive feedback network are needed to complete the functional diagram of the derivative amplifier. This type of diagram makes it easy to recognize the circuit function, particularly in complex illustrations where many operational amplifiers are used.



**Derivative Amplifier** 

The schematic of a derivative amplifier is shown in the accompanying illustration. Capacitor Cl is an input capacitor which couples the input signal to the grid of triode V1.

Together with feedback resistor R1, C 1 forms an R-C time constant network which determines the output waveform at any given time. Resistor R2 and bypass capacitor C1 form the cathode-biasing network for triode VI. Resistor R3 is the plate load resistor from which the output is taken.



**Derivate Amplifier Schematic Diagram** 

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When a positive-going pulse input signal is applied to the grid of VI through capacitor Cl, the grid of V1 is driven positive. This causes maximum plate current flow, which develops a maximum negative output, and the current through feedback resistor R1 is also at a maximum. The large feedback current through R1 produces a voltage drop across RI, which slightly decreases the total input voltage. Capacitor Cl charges at a rate determined by the time constant of Cl and R1. The voltage applied to the grid of VI then decreases at the rate that Cl charges. Plate conduction is decreased by an amount proportional to the decrease in grid signal voltage, and the positivegoing output voltage increase is proportional to the decrease in plate current. The resulting output voltage varies directly with the charge on capacitor C 1. This output voltage is the negative derivative of the positive input voltage. The charging of Cl during the flat top portion of the input signal continues until the input signal abruptly switches polarity. The negativegoing input signal now causes the charge on capacitor Cl to discharge abruptly. The full negative input voltage swing now is applied to the grid of VI and triode V1 is driven into cutoff. The internal resistance of V1 is now greater than the resistance of R1, permitting the capacitive discharge to flow directly through RI to the output. At this point, the positive output vohage reaches a maximum positive value. Once discharged, capacitor C 1 again charges through resistor R1 at a rate equal to the value of capacitor C 1 times resistor RI. As the capacitor charges in a positive direction, the grid of V1 becomes more positive, and rises above cutoff. This causes plate current to flow, and produces a decreased plate output voltage (negative swing), at the rate that capacitor C 1 charges. The decreasing positive output voltage represents the negative derivative of the negative input signal.

#### Failure Analysis.

**No Output.** A defective electron tube, an open input or output circuit, an open biasing network, or a defective plate supply voltage can result in loss of output voltage.

The input signal can not be applied to the grid of V1 if capacitor Cl is open. If cathode-biasing resistor R2 is open-circuited, the output and tube current flow will be prevented. An open plate load resistor, R3, will prevent plate voltage from being applied to the plate of VI. Similarly, if R3 were short circuited, no output voltage variations could be developed. With

a defective plate supply voltage source, no voltage would be available for the plate of V1. If no output occurs, and the proper potentials appear at the electron tube elements, electron tube V1 is probably defective.

Low or Distorted Output. A shorted input, a defective feedback network, a defective triode V1, or a diminished plate supply voltage value can cause the output to be low or distorted.

A diminished plate supply voltage will cause low plate voltage and the output to be lower than normal. If capacitor Cl is shorted, no charging action will occur, resulting in an output which is not the derivative of the input. A shorted or open feedback resistor R1 will cause the same effect as a shorted input capacitor. If cathode biasing resistor R2 is defective, V1 will be improperly biased and a lower, or higher, than normal plate current will produce an improper output.

If cathode bias capacitor C2 is shorted, it will produce an abnormally large and distorted output. An open capacitor will produce degenerative feedback, and a reduced output will occur.

#### DERIVATIVE AMPLIFIER (SEMICONDUCTOR)

#### Application.

**Same** application as electron tube version.

#### Characteristics.

Essentially the same characteristics as electron tube version, except it uses a transistor instead of an electron tube.

## **Circuit Analysis.**

**General.** An output which is the differentiated – value of the input voltage is generated by the derivative amplifier. The relationship between the input capacitor and feedback resistor of a PNP transistor operational amplifier develops the differentiated output. The r-c time constant, which determines the exponential decrease of current, is formed by the product of the input capacitor and feedback resistor. The exponentially varying current flows through the capacitor, the transistor, and the feedback resistor. The product of the current and the ohmic valve of the feedback resistor equals the output voltage value at any given time. The output voltage, then, varies 4 exponentially as the capacitor current varies. **Circuit Operation.** The one line diagram for the semiconductor version of the derivative amplifier is the same as the electron tube version, and therefore is not shown here.

The schematic of a derivative amplifier is shown in the accompanying illustration. Capacitor Cl couples the input signal to the base of transistor Ql. Capacitor C 1 and resistor Rl form an r-c network which determines the output waveform at any given time. Resistor Rl also provides base bias to transistor Ql. Resistor R2 is the collector loadresistor.





#### Waveform Chart

**Derivative Amplifier** 

Assuming a square wave signal is applied to the input, and a positive-going input pulse is applied to the base of Q1 through Cl, the transistor forward bias is decreased. Emitter and collector currents are decreased because of the decreased forward bias. The collector current decrease produces a more negative voltage at the collector of Q1 as the collector voltage rises toward the supply value (time t 1 on the wave-form chart).

Simultaneously, feedback current flows through resistor RI from collector to base, producing a voltage drop across R1, which slightly reduces negative collector voltage fed back to the base, which simultaneously reduces the input voltage. Capactor Cl charges at a rate determined by the time constant of Cl times R1. The input voltage at the base of Q1 decreases at the rate that Cl charges (during time '1 to '2). This charging action increases the forward bias of Q1, creating increased emitter to collector current. As the collector current is increased toward its quiescent value at '2, the voltage at the collector becomes less negative (more positive) at the same rate. The resulting positive-going voltages swing varies directly

with the charge on C 1. The negative output voltage spike produced from '1 to '2 is the inverted derivative of the applied positive input voltage. The charging of Cl, during the flat-top portion of the input signal during time t1 to t2 produces the curved trailing edge of the negative output signal, and continues until the input signal changes polarity at time t2. The negative-going trailing edge of the input signal causes Cl to discharge abruptly. The full negative input voltage is now applied to the base of O1 at time t2. This produces a large increase in forward bias, which increases the emitter to collector current. The increase of collector current results in a less negative (more positive) voltage at the collector of Q1 (developed by the larger IR drop across collector resistor R2). A feedback current also flows through RI from collector to base, and develops a feedback voltage which detracts slightly from the input voltage. Capacitor Cl again charges at the rate determined by Cl times RI during time '2 to '3. The charge is now in a positive direction and the voltage at the base of Q1 again increases during time t2 to '3 at the rate that Cl charges. This decreases the forward bias of Ql, creating decreased emitter to collector current. As the collector current is decreased, the voltage at the collector rises towards the supply value and becomes more negative at the same rate, since there is less current flowing through collector resistor R2. The resulting output voltage during time '2 to '3 varies directly with the charge on Cl. This output voltage is the inverted derivative of the applied negative input. Again C 1 charges during the flat portion of the input signal '2 to '3). When the signal changes polarity at time '3, Cl is immediately discharged and the same action occurs as described above for the first positive-going input pulse at time '5.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a flase low-resistance reading.

No **Output**. An open input, a defective collector load, a defective collector supply, or a defective transistor can cause a lack of output to occur.

If capacitor Cl is open, no input will be applied to the base, resulting in no putput variations. An open or shorted resistor R2, or a defective collector supply voltage source will prevent voltage from being available at the collector of Q1. If none of these components is found defective, transistor Q1 is probably defective.

Low or Distorted Output. The output may be low or distorted if the input is shorted the feedback resistor is open or shorted, the collector supply is defective, or transistor Q1 is defective.

With input capacitor Cl shorted, no charging time constant can be developed, and the output becomes an inverted form of the input voltage. Likewise, with resistor R1 open, no time constant is developed by which Cl can charge. If R1 is shorted, the transistor effectively becomes a diode and the output is not influenced by the input. A low or high collector supply voltage, produced by a defective collector supply source, results in a distorted output. If none of these faulty conditions exists, but there is a low or distorted output, Q1 is probably defective.

#### DIFFERENTIAL AMPLIFIER (ELECTRON TUBE)

## Application.

**The** differential amplifier is used in control and analog circuits to provide an output which represents the difference between two input voltages.

#### Characteristics.

**Uses** dual triodes with a common cathode resistor.

Degenerative feedback is used.

Output is taken from between the plates instead of between plate and ground.

Symmetrical grid and plate circuits are used.

## Circuit Analysis.

**General.** The differential amplifier (sometimes referred to as a difference amplifier) uses two triodes connected to a common cathode resistor. Plate current flow through the triodes develops a common cathode bias. Since the plate and grid circuits of each tube are symmetrical, equal grid input voltages produce equal plate output voltages. Since the output is taken between the plates of the two tubes, there is no potential difference and, effectively, no output. Hence, the output is the effective difference between

the two input signals. Unequal input voltages produce unequal plate voltages. The output voltage is now the difference between the input signals. If opposite polarity input signals are applied, the output will represent the algebraic difference between the input signals.

**Circuit Operation.** The schematic of a typical difference amplifier is shown in the accompanying illustration.



**Differential Amplifier** 

Resistors RI and R5 are the respective grid return resistors for V 1 and V2, while R2 and R3 are the respective plate resistors. Cathode resistor R4 is unby passed, and provides an instantaneous bias which varies with the signal, providing degenerative feedback. The output is taken between the plates of VI and V2.

For ease of circuit explanation, the operation of each tube will be discussed separately and then the two will be combined. When examined individually, the effect of two simple amplifiers with degenerative "feedback in the cathode will be clearly understood. Thus, when V1 grid is driven in a positive direction, increased plate current flows through R2 and produces a negative voltage drop or output. At the same time, the flow of current through cathode resistor R4 develops a cathode bias which determines the grid operating point, plate current flow, and effective amplification factor. The larger the input signal, the greater is the bias developed across the cathode resistor. Thus, a degenerative form of feedback is developed which reduces the range of amplification, helps to make the operation more linear, and reduces the effects of changes in variation of gain with different tubes. When a negative input signal is applied to VI grid, plate current flow through R2 is reduced. Consequently, the output voltage increases and produces a positive output swing. At the same time, the cathode bias voltage developed across R4 is less.

If we now consider the operation of V2, it can be seen that it operates identically, except that when the input is applied to the grid of V2, plate current increases or decreases through plate resistor R3. For identical input signals, equal outputs of the same polarity are developed across both plate resistors.

Consider, now, the combined operation of both tubes through the common cathode connection. When the grids of VI and V2 are both driven equally in a positive direction, equal plate currents flow through R2 and R3, developing equal plate voltage drops. Since the output is taken between both plates, there is no potential difference and zero output. This represents complete subtraction of both input signals. With both plate currents flowing through cathode resistor R4, the grid to cathode potentials are practically identical and the tube currents are balanced.

On the other hand, when one input signal is larger than the other input signal, different plate currents flow through the plate resistors. Similarly, the cathode current flow is less and the total effective bias is reduced. Since the grids are returned to ground through grid resistors R1 and R5, the effective gridcathode voltage is also changed. If V 1 is the more heavily driven tube, the plate current of V2 is reduced, while Vi's plate current through R2 is increased. Hence, the voltage drops across R2 and R3 no longer are equal, and an output voltage will appear between the plates of V1 and V2. This output is proportional to the difference between the two input signals.

When opposite polarity input signals are applied to the grids of the tubes, the plate outputs are also opposite in polarity, and the effect is similar to normal push-pull amplifier operation. In this instance, the output represents the algebraic difference between the input signals. It should be realized that, because of the degenerative feedback afforded by the unbypassed cathode resistor, maximum tube gain is not obtained. Hence, push-pull inputs are not normally applied to the difference amplifier, except where the effect of the difference between two different polarity input signals is desired to control another

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circuit, motor, relays, or to produce a direct meter indication.

#### Failure Analysis.

No Output. An open input or output circuit, lack of supply voltage, an open cathode circuit, or a defective tube can cause a loss of output. Since the output is taken between the plate circuits of two tubes, both tubes or circuits must be inoperative to cause a loss of output; otherwise, there will be some kind of output from one of the circuits. Normally, an open cathode bias resistor will prevent an output from either tube, and lack of plate supply voltage due to a blown fuse or defective supply will also inactivate both circuits. If there is supply voltage, but no plate voltage on both tubes VI and V2, plate load resistors R2 and R3 are probably defective. If both grid resistors Rl and R5 are open, or no input signals are applied, there will probably be a loss of output. In the special case where VI and V2 grids are connected across a common load resistor, open RI or R5 grid resistors may not prevent an output. If all resistors are satisfactory and plate voltage is present on both tubes, the tubes may be at fault. In the case where equal input signals are simultaneously supplied, the circuit will be zerobalanced, and although operating normally, no output will be obtained.

Low Output. A low plate or supply voltage, a small difference between input sigmls, too high a cathode bias, or defective tubes can produce a low output. If the plate supply voltage is normal, but the plate voltage on either or both tubes is not normal (with no grid input applied) plate resistor R2 or R3 may have changed value, or the tube showing abnormal plate voltage may be defective. If the plate voltage of both tubes with no input signal is low, or high, cathode bias resistor R4 may have changed value. If the plate voltage of one tube is lower than that of the other tube, with equal grid input voltages, either the grid or plate resistors are changed in value, or one of the tubes is drawing more plate current than the other. Compare the resistance values of RI and R4, and R2 and R3, as well as the plate currents of VI and V2.

**Distorted Output.** An output which does not vary in accordance with the difference between the input signals is distorted. Usually such a result occurs when only one of the amplifier circuits is operating properly. In such case, it will be necessary to check each circuit individually for proper resistance and voltage values, and for defective tubes.

# DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

## Characteristics.

Emitters are coupled together.

Output is obtained between the collectors of the transistors rather than between the collector and ground.

Symmetrical base and collector circuits are used.

## Circuit Amlysis.

General. The differential amplifier uses two transistors connected to a common stabilizing resistor through separate emitter resistors. Current flow through both transistors develops a common bias. Since the collector and base circuits of each transistor are symmetrical, equal input signals produce equal collector output voltages. Since the output is taken between the collectors of the two transistors, with equal input signals, there is no potential difference, and effectively no output. Hence, the output is the difference between two input signals. Unequal input signal voltages produce unequal collector voltages. The output voltage is now the difference between the two collector voltages and represents the difference between the input signals. If opposite polarity input signals are applied, the output represents the algebraic difference (or mathematical sum) between input signals.

**Circuit Operation.** The schematic of a typical transistordifferential amplifier is shown in the accompanying illustration. Resistors RI and R7 are equivalent base input resistors. Resistors R3 and R5 are equivalent emitter resistors. Resistors R3 and R5 in conjunction with common emitter resistor R4 help to establish equal bias voltage for Q1 and Q2. Resistors R2 and R6 are equivalent collector load resistors, which are connected to a common collector supply voltage source.

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**Differential Amplifier** 

This Circuit is, in effect, two grounded emitter amplifiers using degenerative feedback in the emitter circuit. For ease of explanation, one amplifier will be discussed and then the combined action of both amplifiers will discussed. When a positive-going voltage is applied to the base of Qi, the forward bias is reduced. The decreased forward bias between the emitter and base of Q1 reduces emitter-to-collector current flow. Consequently, collector current flow through collector load resistor R2 is also reduced. The voltage drop across the collector load resistor is thereby reduced, and the voltage at the collector rises toward the negative collector supply voltage. When a negative-going voltage is applied to the base of Q1, forward bias is increased. The increased forward bias and base of O1 increases the emitter-to+ ollector current flow and the collector current through R2. The voltage drop across R2 now increases and makes the collector of Q1 more positive and develops a positive output swing.

Since the amplifier consisting of Q2, R5, R6 and R7 is identical to the amplifier just discussed, with the same input pulses applied to the base, operation is identical. When equal amplitude positive pulses are applied to the bases of both transistors, equal negative voltage drops are produced at the collectors of both transistors. Hence, no output is produced in this case, since the output is the difference between the two collector voltages. When a positive pulse is applied to the base of Q1 and a negative pulse is applied to the base of Q2, a negative voltage is produced on

the collector of Q1 and a positive voltage is produced on the collector of Q2. The output is now the algebraic difference between these voltages or the mathematical sum of these voltages. By the same reasoning, when a negative pulse is applied to the base of QI and a positive pulse is applied to the base of Q2, a positive voltage is produced on the collector of Q1 and a negative voltage is produced on the collector of Q2. The output again is the algebraic difference between these voltages, or the mathematical sum of these voltages.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier shunting resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful, also, to observe proper polarity when check-ing continuity or making resistance measurements since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** A lack of output can result from an open common cathode circuit, a defective plate supply voltage source, or a defective component in both amplifiers.

With resistor R4 open, current is prevented from flowing through any part of the circuit. If collector SUpply voltage source  $V_{ee}$  is defective, no voltage is supplied to the collector of either transistor.

An output cannot be produced by either amplifier if the input resistor (Rl or R7) is open, the collector load (R2 or R6) is defective, the emitter bias resistor (R3 or R5) is open, or if the transistor (Ql or Q2) is defective.

When the input resistor (Rl or R7) is open, the input signal can not be applied to the base of the transitor. If the collector load resistor (R2 or R6) is open, no collector voltage will appear on Q1 or Q2. An open emitter resistor (R3 or R5) prevents current flow through the amplifier containing this resistor. If proper voltages are present on the electrodes of the transistor, and the collector voltage does not respond to the signal voltage variations, transistor Q1 or Q2 is probably defective.

Low or Distorted Output. A shorted input, a shorted emitter resistance, a defective collector supply voltage, or a defective transistor may cause, the output to be low or distorted.

If resistors R1, R7 or both R1 and R7 are shorted, the signal voltage applied to the base of Q1 and/or Q2

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will not be attenuated, the base bias will be less, and the output will probably be distorted. If resistor R3, R4, or R5 is shorted, the emitter biasing of transistors Q1 or Q2 will be incorrect and a low or distorted output will occur. If the collector supply voltage source is defective the output voltage will be either higher or lower than the required voltage. If none of these conditions exists and the output is low or distorted, either transistor Q1 or Q2 may be defective.

# BALANCED DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

## Application.

**The** balanced differential amplifier is used in CRT deflection circuits and in instrumentation and control circuitry where a balanced input and output are required.

## Characteristics.

Produces an output which is in proportion to the difference between two inputs.

Output and input are balanced with respect to ground.

Output is taken between the collector elements instead of from collector to ground.

May be used as an ac or dc amplifier.

## Circuit Analysis.

**General. The** balanced differential amplifier uses two similar amplifier circuits arranged to be driven by separate base inputs, and the emitters are coupled together through a common emitter-resistor. Identical input signals produce identical output signals. Since the output is taken between the two output loads, instead of to ground, there is no potential difference between identical outputs. Thus, an output exists only when there is difference between input signals. Consequently, common noise inputs tend to cancel each other so that the signal-to-noise ratio is usurdly improved by the differential amplifier.

**Circuit Operation.** A schematic diagram of a balanced differential amplifier is shown in the accompanying schematic diagram.



**Balanced Differential Amplifier** 

Fixed base bias is applied to Q1 by bias voltage divider R1 and R5 connected between the negative supply and ground. Resistor R4 together with R7 forms an identical base bias voltage divider for Q2. Resistor R2 is the collector resistor for Ol, and R3 is the collector resistor for Q2; both collector resistors are also the load resistors across which the output is developed. Potentiometer R6 couples the emitter of Q1 to Q2, with the ground return being made through a common-emitter resistor, R8. Potentiometer R6 also permits adjusting Q 1 and Q2 for zero balance, and R8 also provides emitter temperature stabilization. Any change in transistor current-flow due to temperature effect produces an opposing bias across R8 which returns the current flow to normal. Emitter stabilization is thus obtained.

Both Q1 and Q2 are symmetrical common-emitter amplifier circuits. When a forward bias is applied to the base of Ql, increased collector current flows through collector load resistor R2, reduces the applied collector voltage to a more positive vrdue, and produces a positive output voltage swing. At the same time that collector current increases, emitter current also increases. The voltage drop produced by current flow through emitter resistors R6 and R8 reduces forward bias slightly, and provides a slight amount of

degenerative feedback which improves output linearity. Since R6 is connected to the emitters of Q1 and Q2, any change appearing on QI emitter also appears on Q2. Hence, R6 can be adjusted with equal driving input signals to produce equal conduction through each transistor. This provides an effective zero-balance arrangement to compensate for slight production variations in transistors.

Transistor Q2 operates similarly to Q1. Thus, an increase of forward bias on the base of Q2 produces an increased collector current flow through collector resistor R3, and a positive-going output voltage. With equal amplitude input voltages applied to the base of Q1 and Q2, equal output voltages are produced. Since the output is taken between the collector resistors, instead of to ground, equal output voltages produce no difference of potential between them, and there is no effective output across the output terminals. When one input is larger than the other, an output is produced which is the difference between the two collector outputs.

When the forward bias on either **Q1** or Q2 is reduced, less collector current flows through R2 and R3, and the collector voltage increases toward the supply value, producing a negative-going output swing. Again, for equal inputs, no output is produced. For different amplitude signals, the output is proportional to the difference between the applied input signals.

When signals of opposite polarity are applied, the output polarities are opposite, since the collector current of one transistor increases while that of the other transistor decreases. Thus, push-pull operation is obtained, and the output represents the sum, or algebraic difference between the two input signals.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** An open input, output, emitter circuit, or defective transistors, as well as a loss of supply voltage can produce a no-output condition. In most instances, both circuits must be affected, since

if only one of the circuits is operative, some kind of output will be obtained. Lack of supply voltage will cause both circuits to be inoperative. An open emitter resistor, R8, will also prevent both circuits from operating. Two input signals of equal polarity and amplitude will also cause lack of output indication, but in this instance the circuit is operating normally. Where the bias, emitter, and collector voltages appear normal, but there is still no output with unequal input signals, the possibility exists that both transistors Q1 and Q2 are defective.

Low Output. Lower than normal bias, emitter, collector, or supply voltages can cause a loss of output. With a normal supply voltage, low bias can be caused by a change in the value of bias voltage-divider resistors R1 and R5, or R4 and R7. Low collector voltage can be caused by a change in collector resistor values of R2 or R3, or by a change of characteristics in either transistor Q1 and Q2. If emitter resistor R6 or R8 increase in value, a low output will also occur. There is also the possibility that an unbalance caused by a change in values in the parts of one amplifier can be compensated for by readjustment of zero balance potentiometer R6. In most cases, a resistance analysis of the individual parts will indicate the defective component.

**Distorted Output.** An output which does not vary proportionally with the difference between input signals can be considered as operating in a distorted mode. In most instances of this type, one of the amplifiers will be operating normally while the other amplifier is defective. If the individual outputs are observed against ground with the same input signal applied, the unequal output may be easily determined. Do not neglect the possibility that zero balance control R6 is incorrectly adjusted, since unequal outputs will occur if the circuit is not balanced properly.

# SINGLE-ENDED OUTPUT DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

#### Application.

The single-ended output differential amplifier is used in control circuitry and data handling equipment where the difference between two input signals is used to control an output which is not balanced to ground.

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#### AMPLIFIERS

## Characteristics.

Uses two transistor amplifiers with a common emitter-coupling resistor.

Two inputs are required to produce an output proportional to their difference.

The output is unbalanced with respect to ground. May be used as a dc or an ac amplifier.

## Circuit Analysis.

General. The single-ended output differential amplifier can be considered as an emitter-follower amplifier driving a common-base output amplifier. One input controls the emitter-follower amplifier, which is direct connected to the emitter of the common-base amplifier. The output is thus controlled by the emitter bias. Simultaneously, an input is applied to the base of the output amplifier which also controls the output. When the inputs are of different polarity, the output to ground represents the algebraic difference between the two signals. When the inputs are of the same polarity, the output represents the mathematical difference between these signals. Inputs of equal amplitude and polarity effectively cancel and prevent any change of circuit operation, producing on effective zero output. For unequal amplitude inputs, the larger signal controls operation.

**Circuit Operation.** The schematic of a typical single-ended output differential amplifier is shown in the accompanying illustration.



Single-Ended Output Differential Amplifier

Resistor R1 is the base input and bias resistor for Q1. Potentiometer R3 is the common emittercoupling resistor and zero-balance control for Q1 and Q2, with R4 acting as the emitter stabilizing resistor. Resistor R2 is the collector load and output resistor for Q2, and R5 is the base input and biasing resistor. The output is taken from the collector of Q2, and the separate inputs are applied to the base of Q1 and Q2.

Since there is no collector resistor for Q1, the collector bias supply filter capacitor effectively grounds the collector for ac. The output is taken from the emitter of Q1 and applied through R3 to the emitter of Q2; therefore, transistor Q1 can be considered an emitter-follower circuit. Likewise, since the inputs of Q2 are between emitter and base of QI, and between base and emitter for Q2, transistor Q2 can be considered a common-base amplifier. For ease of circuit explanation, each stage is considered separately and their operation combined in a common output.

in the schematic, Q1 and Q2 are fixed-biased by a separate emitter bias supply, so that the base of both transistors are normally forward-biased and the collectors are reverse-biased. When a positive input signal is applied through input-1 to the base of OI, the forward bias is reduced; thus, the emitter current is reduced. As the emitter current reduces, the output voltage across R4 and R3 increases positively. Thus, a positive increase in emitter voltage is applied directly through R3 to the emitter of Q2, and the emitter current of Q2 tends to increase. When the emitter current of O2 increases, the collector current also increases, and a positive-going voltage drop is produced across collector resistor R2 of Q2, producing a positive output. However, at the same time that the emitter of Q2 is driven positive, input 2 (which is also positive) is simultaneously applied to the base of Q2. Normally, "this will decrease the forward bias on Q2 and cause the collector voltage to rise toward the source and produce a negative output. Since a positive input to the emitter of Q2 effectively cancels the positive input to the base of Q2, the total resultant forward (or decreased) bias depends upon the relative amplitudes of the input voltages. If input 1 predominates, a positive output is produced. If input 2 predominates, a negative output is produced. In either case, the relative output is proportional to the difference between the two input voltages. When both inputs are of the same amplitude, the negative

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and positive drops acfoss R2 are equal, and no output results. When inputs of opposite polarity are applied, they bias Q2 in the same direction, so the output actually is the sum of the two signals, or the algebraic difference. Emitter-coupling resistor R3 is a potentiometer, and permits R4 to be connected as a voltage divider to produce an emitter input to Q2 which is equal in amplitude to the base input. Hence, by applying equal input signals and adjusting R3, the output voltage from Q2 may be balanced to zero.

> Other circuit variations may be found in other technical manuals, such as using fixed or voltage divider base bias, or even self bias. The circuit arrangement is always such that the output developed by Q1 opposes the input applied to Q2, and results in the difference between the input signals producing the output.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low value of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe the proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** Open input circuits, open emitter circuits, open output circuits or defective transistors can cause loss of output. If base resistors R1 and R5 open, the base to emitter circuit will be offered a high impedance path through the input signal source, and operation will probably be blocked. If either R3 or R4 opens, the emitter circuits of the transistors will be incomplete and no bias voltage will be measured between emitter and ground. If R2 opens, there will be no collector load for Q2 and no output can be developed. If the emitter, collector, and base voltages are normal, but still no output is obtained, transistors Q1 and Q2 are defective. If no collector voltage appears on both transistors, the supply source is at fault.

Low Output. If any of the resistors change in value, if the supply source is low, or improper bias is applied, or if one or both transistors are not normal, the output will be lower than normal. If the voltage on Q2 collector is normal, and both R2 and the supply source voltage are normal, but the collector voltage of Q2 is low, improper bias can be the cause. Check R3 and R4 and the emitter supply voltage. If

RI or R5 changes in value, the input signal amplitudes will be affected, and an improper output will be obtained. Similarly, if Q1 or Q2 characteristics change, an improper output will be obtained.

**Distorted Output.** If the output of Q2 varies other than as the difference between the input signals, one or both transistor circuits are operating improperly, and distortion is occurring. The output of Q1 should produce a waveform identical in shape and polarity to input-1 and of slightly less amplitude. The output of Q2 should always be proportional to the difference between the waveform on the emitter of Q2 and input-2.

# BALANCED SUPER-ALPHA DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

#### Application.

The balanced super-alpha differential amplifier is used in analog computers and control circuitry where higher gain than that obtained by the conventional balanced differential amplifier is required.

#### Characteristics.

Uses super-alpha circuit to provide high gain.

Circuit is balanced with respect to ground.

Output is taken between emitters instead of to ground.

Either self- or fixed-bias can be used.

### Circuit Analysis.

General. The super-alpha differential amplifier uses two NPN and two PNP transistors. Through use of the complementary transistors, the same power source may be used for both stages and a super-alpha circuit can be employed. The super-alpha circuit connection uses two direct-coupled transistors in a feedback circuit which is equivalent to a single transistor with superhigh gain. This gain is usually so high that it can never be equalled by a single transistor. Both input and output circuits are blanced, and identical outputs are obtained. Since the output is taken between the emitters instead of to ground, equal outputs effectively cancel; an output is only obtained when the input signals are different in amplitude, resulting in an amplifier which responds only to the difference between the input signals.

**Circuit Operation.** The accompanying schematic illustrates a typical balanced super-alpha differential amplifier.



Super-Alpha Differential Amplifier

Simplified Super-Alpha Circuit

Resistor RI is the emitter-coupling resistor for transistors Q1 and Q3, while R2 is the common emitter-stabilizing resistor. Resistor RI also provides a zero-balance arrangement for the circuit. Transistors Q1 and Q3 are the complementary input amplifiers, while Q2 and Q4 are the complementary output amplifiers. Resistors R3 and R4 from the emitter and output loads for Q2 and Q4, respectively.

Since the emitters of Q1 and Q3 are connected to a negative source, forward+x-nitter bias is produced for these NPN transistors. Since the collectors of Q2 and Q4 are connected to the same negative source, the collectors are reverse-biased, as is usual for PNP transistors.

Basic operation can be more easily understood if the super-alpha circuit is simplified to a single NPN transistor as shown in the accompanying illustration. In this case Q1 and Q2 are replaced with single NPN transistor QIA, while Q2 and Q4 are also replaced with a single NPN transistor, Q2A. Even though simplified, current flow is the same as in the original circuit, and because of this the emitter and collector elements are drawn reversed. Hence, when a positive input signal is applied to NPN transistor QIA, the forward bias on the NPN transistor is increased, a larger emitter current flows through R2 and R1, and back through the collector of QIA and load R3 to the supply. Similarly, when a negative input is applied to the base of Q2A, an increased emitter current flows through R2 and R1, and through the emitter to the collector of Q2A and R4 to the supply source. Thus, negative-going voltage drops are produced across R3 and R4, and the output taken between the

collectors of QIA and Q2A is zero (for equal input amplitudes) when R1 is set for zero balance with no inputs. For unequal inputs, the output is the difference between the collector voltages, which is proportional to the difference between the inputs.

Now consider the original super-alpha circuit, remembering that current flow is in the same direction, but that the output emitter and collector elements are reversed in a PNP configuration. When a positive input is applied to the base of Q1, the emitter and collector current of Q1 increases. Current flow is through R2, R1, and the emitter and collector of Q1 to the base of Q2. An increased current flow into the base of Q2 increases the emitter and collector current of Q2, and an increased current flows from the emitter to the collector of Q2 and through emitter-load resistor R3 to the supply. Thus, a negative-going voltage is produced by Q2. In a similar manner, when a positive input is applied to the base of Q3, the emitter and collector current of increases, and current flows through R2, RI, and from the emitter to the collector of O3. Since the collector of Q3 is connected to the base of Q4, an increased base current flows. As a result, the emitter and collector current of Q4 increases and an increased current flows through Q4 and back through R4 to the supply source. Thus, a negative-going output voltage is developed across the output of O4. With equal amplitude inputs, equal negative outputs are developed, and no difference in potential exists across the output when the circuit currents are balanced.

When the input to Q1 or Q2 is changed to a  $\_$  negative input, the reverse action occurs; the PNP

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transistor currents are reduced, and the drop across the output load is in a positive direction. Again, with equal inputs and outputs, there is no potential difference across the output and effectively no output occurs. Unequal inputs produce an output proportional to the difference between the input signals.

Since the input emitters of QI and Q3 are connected together through RI, it is also possible to apply a single input to Q3 and ground the input to Q1. In this special case, the emitter of Q3 will have an opposing signal applied and a balanced output will still be obtained. If, however, the output is taken against ground, the output of Q4 will be in-phase with the input, while the output of Q2 to ground is out-of-phase with the input. When different polarity inputs are applied, the output will act as a push-pull amplifier and the sum of the input, or algebraic difference, will produce the output.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. Lack of supply voltage, open emitter resistors, or collector resistors, as well as defective transistors can cause a loss of output. If there is no supply voltage, if R2 is open, or if both transistors Q1, Q3, or Q2, Q4 are defective, no output can occur. If potentiometer R1 is open on only one side, or if only Q1 or Q2, or Q3 or Q4 is open, or if output resistor R3 or R4 is open, a partial output will occur. It is necessary for both R3 and R4, Q1 and Q3, or Q2 and Q4, or both sides of RI to be open to produce no output, since both circuits must be rendered inoperative simultaneously for no output to occur.

Low or Distorted Output. If the supply source is low, if any transistor changes characteristics, if improper bias exists, or if R2, R3, or R4 changes in value, a low or distorted output can occur. If the supply source measures low, low bias and output current will produce a low output. If one half of the circuit operates properly and the other half does not, a distorted and low output will probably occur. A change in the value of currents drawn by the transistors will produce different voltage drops across R1, R2, R3 and R4, and produce unequal output. If the currents decrease, or the resistor values decrease, a low output will occur. If the currents increase, or the resistor values increase, a higher than normal output will probably occur. Where the waveforms appear normal at the inputs, and the outputs are distorted but voltages appear to be within tolerance, the transistors are probably at fault. A resistance check will usually indicate if any parts are defective.

# DIRECT-COUPLED CASCADED DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

## Application.

The direct-coupled cascaded differential amplifier is used in computers, cathode-ray tube circuits, and in control circuits **v**'here a low-drift and high-gain dc amplifier is required.

#### Characteristics.

Direct coupling is used.

Both amplifiers are balanced with respect to ground.

Output is taken from between the collectors instead of to ground.

Fixed bias is employed.

## Circuit Analysis.

General. The direct-coupled cascaded differential amplifier uses two differential amplifier connected in series, that is, the collector output of the input stage is directly connected to drive the base of the output stage. Both input and output stages can also be direct-coupled to the input or output loads, if desired. Since the differential amplifier is balanced, and inherently stabilized by a common-emitter resistor against temperature effects, it has very little drift (output level does not change with temperature). Therefore, with a minimum of drift, direct coupling is used to obtain a relatively stable high-gain amplifier. When an input signal is applied to both input stages, it either increases or decreases the base bias of the output stage. Consequently, either a negative or a positive output swing is developed across the output load. Since both outputs are of the same polarity when similar inputs are applied, the output is produced by the difference between the two input signals. Equal amplitude imputs will produce equal outputs, and there will be no potential difference between them. Thus, the effective output will be zero

if the circuit is correctly balanced. With unequal polarity inputs applied, the circuits will operate as push-pull amplifiers and produce the algebraic dif-

ference or sum of the input signals. Since each stage inverts the input and two stages are used, the output will always be the same polarity as the input.

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**Circuit Operation.** The schematic of a typical cascaded direct-coupled differential amplifier is shown in the accompanying illustration.



Cascaded Direct-Coupled Differential Amplifier

Resistor RI couples the emitters of input transistors Q 1 and Q2 together, and R2 is an emitterstabilizing resistor which is common to both input stages. Resistors R3 and R4 are the collector resistors and loads for Q1 and Q2, respectively. They also act as the base input resistors for Q3 and Q4. Potentiometer R5 couples the emitter of Q3 and Q4, and acts as a zero-balance control for the output circuit. Resistor R6 is an emitter-stabilizing resistor which is common to both Q3 and Q4. Resistors R7 and R8 are the collector and load resistors for output transistors Q3 and Q4 respectively. The inputs are applied to the base of Q1 and Q2, while the output is taken between the collectors of Q3 and Q4.

Normally, Q1 and Q2 are base-biased by the input circuit, or by voltage divider bias (not shown in the schematic). The bias is such that equal input swings are possible without biasing the transistors to cutoff (Class A operation). Transistors Q1 and Q3 operate as conventional common+ mitter amplifiers. The direct coupling between the collector of Q 1 and the base of Q3 places a reverse collector bias on Q1 and a forward base bias on Q3. Operation normally is such that the reverse leakage collector current of Q1 and the collector resistor value produce a bias which places Q3 at the desired operating point. If necessary,

separate bias can be applied to the emitter to obtain the desired operating point. When a positive input is applied to the base of Q1, forward bias is reduced and less collector current flows. The collector voltage on Q1 then increases and a larger negative bias is applied to the base of Q3, producing an increased forward bias. Consequently, Q3 collector current increases, and the increased current flow through collector resistor R7 decreases the collector voltage. Thus, a positive-going output voltage swing is created, and the output is in phase with the input.

In a similar manner, when a positive signal is applied to the base of Q2, reduced collector current flows through R4 and the collector voltage on Q2 increases. This negative increase of voltage is applied to the base of transistor Q4, and causes an increased collector current flow through R8. Hence, the output of Q4 is positive-going, and is in phase with the input. Since the output is taken across the collectors, equal output swings of equal polarity will produce an effective zero output. As log as the output swings are different, there will be a proportionate output which varies as the difference between the outputs. Since a difference in outputs can only be produced (in a balanced circuit) if there is a difference between the input signals, any output represents the difference between the input signals. By connecting the emitters of Q1 and Q2 together with potentiometer R 1, emitter-stabilizing resistor R2, which is common to both stages, provides the same temperature compensation for each transistor. Also, the different resistance paths through R1 to both emitters cause an emitter bias to be produced, which compensates for any differences in emitter current resulting from production variations. Thus, RI is adjusted for zerobalance with no input signal applied, so that approximately equal output currents are developed by equal input signals. Potentiometer R5 connects the emitters of Q3 and Q4 together and operates similarity to zero-balance the output stage, while resistor R6 operates as the common stabilizing emitter-resistor for O3 and O4. With both input and output circuits properly zero-balanced, equal outputs are always developed for equal inputs.

In normal design, transistors Q3 and Q4 are usually power-type transistors. Thus, with conventional driving transistors used for Q1 and Q2, a highcurrent gain can be realized from cascaded directcoupled stages, and a large output is developed.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional **volt-ohmmeters**. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. Lack of supply voltage, an open input or output circuit, or defective transistors can result in a 10ss of output. If emitter-stabilizing resistor R2 or R8 opens, the associated amplifier circuits will not operate. If collector resistors R3 and R4, or R7 and R8 are open, no collector voltage will appear on the collectors of Q1 and Q2, or Q3 and Q4, respectively, and no output will occur. Note that both resistors must be open, or alternate resistors in cascaded stages must be open, to cause a complete loss of output. Likewise, if the transistors are defective, it is necessary that one in each channel be defective; otherwise, a single unbalanced output could occur.

Low or Distorted Output. If the supply voltage is low, if improper bias exists, if the collector resistors change in value, or the emitter resistors change, a low output or a distorted output can occur. If the transistor characteristics change, of if the circuit is not zero-balanced, a low and distorted output can occur. If emitter coupling resistors RI and R5 open, the circuits cannot be zero-balanced and the output will be somewhat distorted. If collector resistors R3, R4, R7 or R8 change in value sufficiently that zero balance cannot be obtained, unsymmetrical outputs will be obtained, and a low or distorted output will occur.

# DIRECT-COUPLED CASCADED, COMPLEMENTARY-SYMMETRY DIFFERENTIAL AMPLIFIER (SEMICONDUCTOR)

## Application.

Same application as direct-coupled cascaded differential amplifier.

#### Characteristics.

Same characteristics as direct-coupled cascaded differential amplifier.

#### Circuit Analysis.

General. The direct-coupled cascaded, complementary-symmetry differential amplifier uses two complementary-symmetry differential amplifiers connected in series (cascaded). The output of the input amplifier is directly connected to drive the base of the output amplifier. Both input and output stages can also be direct coupled to the input or output loads, if desired. Since the differential amplifier is balanced, and inherently stabilized by a common emitter resistor against temperature effects, this type of amplifier has very little drift (the output level does not change with temperature). When minimum drift exists, direct coupling can be used to obtain a relatively stable high-gain amplifier. By using cascaded complementary-symmetry stages, the small amount of drift which normally exists is reduced still further, and extremely higher than normal gain may be obtained.

When an imput signal is applied to both input stages, it either increases or decreases the base bias of the output stages. Consequently, either a negative or a positive output swing is developed across the output

load. With similar input polarity signals applied, similar output signals are produced. Since the output is taken between the collectors, equal outputs produce no potential difference between them, and for equal inputs there is effectively no output. With unequal inputs, the output represents the difference between the input signals. When the input signals are of opposite polarity, the output operates as a push-pull amplifier and produces difference between the input signals. Since each stage inverts the input, and two stages are used, the output is always of the same polarity as the input.

**Circuit Operation.** The schematic of a typical cascaded complementary-symmetry differential amplifier is shown in the accompanying illustration.



Cascaded Direct-Coupled Complementary-Symmetry Differential Amplifier

Potentiometer RI couples the emitters of NPN input resistors Q1 and Q2 together, and R2 is an emitter stabilizing resistor common to both input stages. By adjusting the emitter bias applied through RI and R2, the output may be adjusted for zero balance (with no input signals applied) to ensure that both stages are properly balanced. Resistors R3 and R5 are the collector resistors and loads for Q1 and Q2, respectively. They also act as base input resistors for PNP transistors Q3 and Q4. Resistors R6 and R7 couple the emitters of Q3 and Q4, and act as balancing and stabilizing resistors. Resistor R4 is an emitter bias and stabilizing resistor which is common to both

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Q3 and Q4. Resistors R8 and R9 are the collector and load resistors for output transistors Q3 and Q4, respectively. The inputs are applied to the bases of Q1 and Q2, while the output is taken between the collectors of Q3 and Q4. Normally Q1 and Q2 are basebiased by the input circuit, or by a voltage divider bias (not shown on the schematic). The bias is such that equal input swings are possible (class A operation). Transistors Q1 and Q3 operate as conventional cascaded common-emitter amplifiers. Transistor Q1 is an NPN type, while Q3 is a PNP type. The direct coupling between the collector of Q1 and the base of Q3 places a reverse collector bias on Ql, and indirectly, a forward bias on the base of Q3. As connected, the emitter of Q3 is forward-biased through R4 and R6 from the same supply which biases the collector of Q 1 and the base of Q3. Collector resistor R3 for Q1 is larger in value than emitter resistors R4 and R6 combined. Thus, the drop through R3 by normal (quiescent) collector current flow throu-gh Q1 produces a steady negative voltage drop, so that the base of O3 is always more negative than the emitter. The emitter is more positive than either the base or collector of Q3, since the collector of Q3 is reversebiased. Thus, Q3 base is effectively forward-biased by the direct coupling circuit, even though a positive voltage exists on the collector of Q1 and the base of Q3. That is, the base of Q3 is less positive (more negative) than the emitter of Q3, and the operating bias is effectively a negative (forward bias) voltage with respect to its emitter. Design is such that the stage operates at the center of its linear Class A range, so that equal positive or negative bias swings are possible without creating excessive distortion.

When a positive input signal is applied to the base of Q1, the forward bias is increased and more collector current flows through R3, driving the base of Q3 negatively and increasing the forward bias on Q3. Hence, the **collector** current of Q3 increases and the voltage drop produced across the collector resistor R8 is positive-going, producing a positive output (less negative voltage) at the collector.

In a similar manner, when a positive input signal is applied to the base of Q2, forward bias is increased, and the increased collector current flow through R5 produces a negative-going voltage at the base of Q4, and increases the forward bias. With an increased forward bias on Q4, an increased collector current flows through R9, reduces the collector voltage, and produces a positive-going output swing. Since the output of the total circuit is taken between the collectors, equal amplitude output swings of the same polarity produce an effective zero output. If the output voltage swings are different in amplitudes, there will exist a proportionate output which varies as the difference between the output of Q3 and Q4. A difference in outputs can only be produced in a balanced circuit when there is a difference between the input signals. Since the emitters of Q1 and Q2 are connected together by potentiometer R1, emitter stabilizing resistor R2, which is common to both stages, provides the same temperature compensation for each transistor. By varying the position of R2 along potentiometer RI, different resistance paths are provided through R1 to each emitter, and allow an emitter bias to be produced which compensates for any differences in emitter currents caused by production variations. Thus, R1 is adjusted for zero balance (no output with no input signal applied), so that approximately equal output currents are developed by equal input signals. Resistors R6 and R7 connect the emitters of Q3 and Q4 together, and are temperature-stabilized through common emitter resistor R4, which operates similarly to R2. Since resistors R3 and R5 are equal, as are R6 and R7, and R8 and R9, only the single zero-balance potentiometer RI is needed for proper adjustment of circuit balance.

When negative inputs are applied to Q1 and Q2, the collector-current flow through R3 and R5 is reduced by the decreased forward bias, and the collector voltage of Q1 and Q2 becomes positive-going, rising toward the source value. In turn, the base bias of Q3 and Q4 is reduced, and less collector current flows through resistors R8 and R9. Thus, the collectors of Q3 and Q4 rise toward the negative source voltage, and produce an effective negative-going output. Again, for equal inputs, equal outputs are produced, and there is no effective difference in potential between them. Hence, the total output is effectively zero. For different amplitude signals, the output is again proportional to the input and the polarity is reversed.

## Failure Analysis.

**Generel.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional ohmmeters. Be careful, also, to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any

of the transistor junctions will cause a false lowresistance reading.

No **Output.** Lack of supply voltage, an open input or output circuit, or defective transistors can result in a loss of output. If emitter-stabilizing resistor R2 or R4 is open, the associated amplifier circuits will not operate. If collector resistors R3 and R5, or R8 and R9 are open, no collector voltage will appear on the collectors of Q1 and Q2, or Q3 and Q4, respectively, and no output will occur. Note that both resistors of balanced stages must be open, or alternate resistors of cascaded stages must be open, to cause a complete loss of output. Likewise, if the transistors are defective, it is necessary that one in each channel be defective, otherwise, a single unbalanced output could occur.

Low or Distorted Output. If the supply voltage is low, if improper bias exists, if the collector resistors change in value, or the emitter resistors change, a low output or a distorted output could occur. If the transistor characteristics change in value, or if the circuit is not zero-balanced, a low or distorted output could occur. If emitter resistors R1, R6, or R7 open, or change to a high value, the circuits cannot be zerobalanced and the output will be somewhat distorted. If collector resistors R3, R5, R8 or R9 change in value sufficiently that zero-balance cannot be obtained, unsymmetrical outputs will occur, and a low or distorted output will result.

#### EXPONENTIAL AMPLIFIER (ELECTRON TUBE)

## Application.

The exponential amplifier is used in analog corn-puters and cathode-ray tube circuits to develop an output voltage proportional to the desired exponential of input voltage.

### Characteristics.

Uses a variable-mu pentode.

Unbypassed cathode resistor is used to provide degenerative feedback.

The tube is operated at a non-linear portion of the plate current-grid voltage characteristic curve.

The desired multiple of the input (exponent) to which the output is raised is determined by plate and cathode resistance, and plate voltage.

## Circuit Analysis.

**General.** The exponential amplifier produces an output signal equivalent to an exponentially increased (squared, cubed, etc ...) input signal. This is accomplished by operating only over a selected portion of the tube plate current-grid voltage characteristic curve. The plate current (and output voltage) is, made to vary proportionally with the grid voltage raised to between the 2/2 power and the 2.5/2 power. The desired exponent by which the input is to be raised is obtained by the proper selection of plate load resistance, cathode resistance, and plate voltage for a specific value of internal tube plate resistance.

**Circuit Operation.** The schematic of a typical exponential amplifier is shown in the accompanying illustration.



**Exponential Amplifier** 

The input is applied across grid resistor RI. This resistor is also used to apply fixed bias from a separate bias supply voltage (Ecc); self-bias is also supplied by unbypassed cathode resistor R2. Electron tube V1 is a variable-mu pentode. Resistor R3 is the screen grid voltage-dropping resistor. Capacitor Cl is the screen grid bypass capacitor. Resistor R4 is the plate load resistor.

The cathode resistance, R2, plate supply voltage, Ebb, plate load resistor R4, and the internal resistance of electron tube V1 are chosen to provide an amplified output which varies as the square of the input voltage. By operating variable-mu pentode VI along a nonlinear portion of the grid voltage-plate current characteristic curve, the desired exponential relationship between input and output is obtained.

When a positive-going sine wave is applied across resistor R1 to the grid of V1, it effectively decreases the fixed negative bias voltage, and produces increased plate conduction of VI. The plate current rate increase is slight for a small applied grid voltage, and is not proportional to the signal voltage increase. When a positive l-volt signal is applied, conduction is directly proportional to the input; when the signal increases above 1-volt, the conduction rate becomes proportional to the product of the signal voltage value squared. The increased rate of conduction is enhanced by negative feedback voltage developed at the cathode of V1 through unbypassed resistor R2. The increased plate current of V1 caused by the reduced bias produces a proportional reduction in plate and output voltage.

As the sine wave decreases it causes the grid bias voltage effectively to increase. Plate conduction then decreases at the same rate it increased, until the signal voltage reaches zero. Here the conduction rate of VI is at a quiescent (static) value. When the input signal voltage swings negative, the plate conduction also decreases at a rate proportional to the square of the input signal voltage. The output voltage developed across plate resistor R4 then increases at a rate proportional to the increase of plate current.

#### Failure Analysis.

**No Output.** A loss of output voltage may be caused by an open output circuit, a defective tube, an open cathode resistor, or lack of plate supply voltage.

If plate load resistor R4 is open, no output voltage can be developed since no plate voltage will be applied to VI. A defective plate supply voltage source has the same effect. An open cathode resistor, R2, will produce an open output circuit. If the proper voltages are present on the elements of V1 and there is no output, tube VI is probably defective.

Low or Distorted Output. A defective input, a defective cathode circuit, a defective screen circuit, or defective supply voltages can result in an output which is low or distorted.

If resistor R1 is defective, improper bias voltage will be applied to the grid of V1, thus providing the incorrect amount of plate conduction for a given signal. A shorted cathode bias resistor, R2, or a defective bias supply voltage Ecc will produce the same effect. If screen resistor R3 is defective, improper

screen voltage will be applied to the screen grid of VI. A defective supply voltage source, Ebb, will cause low plate and screen voltages. A defective screen bypass capacitor, Cl, will cause output voltage variations to be coupled back to the screen grid of V1, resulting in a distorted output. If none of these conditions exists and proper potentials exist at the elements of V1, the tube is probably defective.

#### **EXPONENTIAL AMPLIFIER (SEMICONDUCTOR)**

## Application.

**The** exponential amplifier is used to develop an output voltage proportional to the desired exponential of input voltage. The amplifier is used in analog computers and control circuits.

#### Characteristics.

Uses common-emitter transistor amplifier configuration.

Uses emitter stabilization for temperature compensation.

Transistor is selected to give an exponential response.

## **Circuit Analysis.**

**General.** A transistorized exponential amplifier uses a circuit configuration which is essentially the same as a basic transistor amplifier. The distinction between the two types of amplifiers is with the transistor, and, the biasing potentials used. The exponential amplifier uses a transistor and bias combination that produces a collector current variation which is the input voltage raised by a desired exponential. The collector current variation, in turn, produces similar collector and output voltage variations. **Circuit Operation.** The circuit of a typical transistorized exponential amplifier is shown in the corresponding illustration. Resistor RI is a series base resistor. It attenuates the input signal before being applied to the base and reduces base current. Resistors R2 and R4 form a fixed-bias voltage divider for the base of Q1. Resistor R5 is an emitter stabilization resistor, and resistor R3 is the collector load resistor.



**Exponential Amplifier** 

The positive portion of an imput waveform is applied to the input, where it is attenuated by resistor R1 before being applied to the base of Q1. The positive-going input voltage decreases the forward bias of C 1. A decrease in base bias causes a decrease in emitter-to-collector current, which, in this case, is proportional to the square of the input signal variation. This is shown in the accompanying illustration of the "Transistor Transfer Characteristic Curve". The decreasing collector current of Q1 causes the IR drop across resistor R3 to decrease at the same rate. -The collector, and output voltage then decrease toward the negative collector supply voltage.





**Transistor Transfer Characteristic Curve** 

As the input waveform passes its positive peak and begins its negative swing, the negative-going input voltage (after being attenuated by Rl) is applied to the base of Q1. The forward bias of the transistor is increased by the negative-going input. An increase in bias causes an increase in emitter-to-collector current, which is proportional to the square of the input signal variation. The exponentially increasing collector current of Q1 causes the IR drop across R3 to increase at the same rate. In some circuit variations, a capacitor is placed from the collector to ground to produce an exponential charging waveform.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeter. Be careful to observe proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

**No Output.** There will be no output voltage if the input is open, the collector load is defective, the bias resistor is open, the collector supply source is defective, or transistor Q1 is defective.

An open base resistor, Rl, prevents output signal variations from being developed. If R3 were open, no collector supply voltage would be applied to the collector of Q1. No collector supply voltage would be present on Q1 if the collector supply voltage source  $V_{CC}$  were defective. An open emitter resistor, R5, prevents any current from flowing in the circuit. If none of these components is defective, and there is no output, transistor Q1 is defective.

Low or Distorted Output. The output becomes low or distorted if the input is shorted, the bias resistor is shorted, the collector supply sources is defective, or if the transistor is defective.

If base input resistor R1 is shorted, the input signals will not be attenuated and a distorted output will occur. A shorted emitter resistor, R5, will slightly lower the output and no temperature compensation will be produced. A defective collector supply source,  $V_{CC}$  may provide a higher or lower collector supply voltage than is necessary. If none of these components is defective and the output is low or distorted, transistor Q1 is probably defective.

#### INTEGRATING AMPLIFIER (ELECTRON TUBE)

## Application.

**The** integrating operational amplifier is used in analog computer and control circuitry to develop an output voltage that is the integral of the input voltage.

#### Characteristics.

Uses a resistive input network.

Uses a capacitive feedback.

Uses a triode electron tube.

A square-wave input produces a triangular output waveform.

Usually operated near zero bias.

## **Circuit Analysis.**

**General. This** intergrating operational amplifier, sometimes referred to as a "Miller" integrator, uses a resistive input network and capacitive feedback to produce the integrating effect. The capacitive feedback is essential to circuit operation. The output is developed by the charge and discharge of the capacitive feedback network during the pulse width and the time between pulses of a square wave input. The capacitor also makes the output more linear by controlling plate voltage variations with corresponding smaller and opposite grid voltage (feedback) variations. The output always represents the integral of the input.

**Circuit Operation. The** schematic of a typical integrating amplifier is shown in the accompanying illustration. Resistor RI is the grid resistor for electron tube V1. Capacitor Cl is the feedback capacitor, and resistor R2 is the plate load resistor.



**Integrating Amplifier** 

When a positive-going square wave is applied to the grid of VI, it causes increased plate conduction. A corresponding plate voltage decrease (negative swing) is developed across R2. This decrease in voltage (negative swing) is coupled back to the grid through Cl. The sum of this voltage and the square wave input pulse results in a decreased grid signal for the moment.

For ease of understanding, refer to the accompanying waveform chart, which shows the grid and plate waveforms and their relationship slightly exaggerated for the purpose of illustration. At time t. there is not input, approximately zero bias is applied, and the average plate voltage is 150 volts with no output voltage existing. At time T<sub>1</sub>, the positivegoing leading edge of the input signal produces a positive grid bias, which drives the plate into heavy conduction and produces a negative feedback voltage spike. This feedback voltage is applied from plate to grid through Cl and is shown as  $e_{pg}$  on the chart. The negative feedback cancels a portion of the positive input signal, and the grid signal is instantaneously reduced to a small value. As a result, plate current decreases and develops a positive feedback voltage, which drives the grid further positive and increases

plate current. The corresponding negative plate feedback signal again cancels a portion of the square wave input, which is constantly applied at full amplitude, for the duration of the input pulse. During time  $t_1$  to t, feedback capacitor Cl is constantly being charged by the effect of negative feedback voltage and the positive input voltage. The addition of these two voltages produces an effectively positive linear grid signal. The positive grid voltage would normally rise exponentially with the charge, as long as the input amplitude remained constant. Since the feedback voltage is constantly affecting the input voltage, the charge occurs nearly linearly. The effect is to produce an average plate current which constantly increases to a maximum at time t<sub>2</sub>, when the trailing edge of the input signal appears. At the same time, the voltage constantly drops, reaching a minimum at 140 volts. Thus, there is a 10-volt negative triangular voltage produced.



#### Grid and Plate Waveforms

When the negative trailing edge appears at the input (at  $t_2$ ), the grid is instantly driven negative, and a large positive plate feedback pulse is created by the decreased plate current. This positive feedback causes an increase in plate current, which produces a negative feedback voltage swing. The negative swing

applied to the grid through Cl reduces the positive voltage on the capacitor, and discharges it a slight amount. Plate current is again decreased, and a positive swing is fed back to the grid. Thus, instead of decreasing exponentially between times  $t_1$  and  $t_3$ , the grid charge voltage on Cl is reduced linearly. As the positive grid bias is reduced to zero between pulses by the discharge of Cl, the plate voltage constantly rises. At time t<sub>2</sub>, it again reaches its starting value of 150 volts, the leading edge of the next input pulse arrives, and now drives the grid in a positive direction. From time  $t_3$  to  $t_4$  the cycle of action described above occurs again. The square wave input thus creates a 10-volt triangular output, and represents the integral of the input signal. By selecting the proper time constants and applied voltages, the output voltage and waveshape may be varied for the desired design characteristics. For this reason, the integrator circuit is sometimes used with a switching tube and amplifier to provide a linear sawtooth sweep voltage.

#### Failure Analysis.

**No Output.** A defective plate supply source, a defective plate resistance, an open input or a defective electron tube can cause a loss of output.

If no voltage is present on the plate of V1, either the plate supply voltage source or plate load resistor R2 is defective. Check R2 for proper value. If resistor **P1** is open, no input will be applied to the grid of V1 and thus no output will be obtained. If all voltages on the electrodes of V1 are proper and no output exists, tube V1 is probably defective.

Low or Distorted Output. The output of this circuit can be made low or distorted by a shorted grid resistor, R1, a defective feedback capacitor, Cl, a defective tube, Vl, or a defective plate supply voltage source.

If resistor R1 is shorted, the correct charging time constant of Cl will not be obtained, and the output will be something other than the integral of the input. Likewise, if feedback capacitor Cl is open, no charging action will occur, and the output will more closely resemble the input. If Cl were shorted, no charging action would occur and in addition V1 would be connected between grid and plate, acting as a diode. This would produce an output waveform independent of the input voltage. The output will become distorted if the plate supply voltage source provides voltage higher or lower than the desired plate supply voltage. If proper voltages are supplied to all the elements of

#### ORIGINAL

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VI, and the component parts of this circuit are normal, triode VI is probably defective.

#### INTEGRATING AMPLIFIER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

## Characteristics.

Same characteristics as electron tube version except it uses transistor with self-bias.

#### **Circuit Analysis.**

**General.** An integrating operational amplifier uses a resistive input network and capacitive feedback to produce the integrating effect. The output is developed by the charge and discharge of the capacitive feedback network during the pulse width and the time between pulses of a square-wave input. The capacitor also makes the output more linear by applying feedback to the base to control collector voltage variations. The output always represents the integral of the input voltage.

**Circuit Operation. The** schematic of a typical integrating amplifier is shown in the accompanying illustration. Resistor R1 is the base input resistor. Capacitor Cl is the feedback capacitor connected between the collector and base of transistor Q1. Resistor R2 is the collector load resistor.

The accompanying waveform chart shows the relationship of collector, base, and capacitor feedback waveforms. At time t. there is no input and the collector voltage rests at some negative value. At time t a positive-going square wave is applied to the base of Q1, causing a decrease in forward bias. The collector voltage increases negatively and approaches the collector supply voltage, since the current through the collector load resistor is decreased. The negativegoing change in collector voltage is capacitively coupled uack to the base by Cl. This feedback voltage is designated as ech in the waveform illustration. The base voltage is now lower than the applied input voltage by the amount of the feedback voltage. The forward bias is then increased by this amount resulting in a slight emitter and collector current increase, and a slight drop in voltage across R2 to some more positive value. This positive change in voltage is coupled through Cl to the base of Q1, where it cancels some of the effect of the previously negative-going feedback. The current is decreased slightly between the emitter and collector, and collector voltage again approaches the collector supply voltage, but not nearly as much as it did with the original signal application. This effect continues during the signal pulse



Integrating Amplifier



**Base and Collector Waveforms** 

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**ELECTRONIC CIRCUITS** 

between  $t_1$  and  $t_2$ , but becomes less significant with each feedback pulse. This sawtooth effect is exaggerated in the  $e_{cb}$  waveform illustration. During time  $t_1$ to t<sub>2</sub> capacitor Cl is charged by the effect of the negative feedback and the positive input voltage. The addition of these two voltages produces an effectively linear positive base signal. The positive base voltage will normally rise exponentially with the capacitor charge, as long as the input amplitude remains constant. Since the feedback voltage is constantly affecting the input voltage, the charging action occurs nearly linearly. The effect is to produce an average emitter and collector current which constantly decreases to a maximum at time t<sub>2</sub>, when the trailing edge of the input signal appears. At the same time, the collector voltage constantly approaches the negative collector supply voltage. Thus, a nearly linear decreasing negative output is produced.

At time t<sub>2</sub>, the base is instantly driven negative by the negative trailing edge of the input signal. The forward bias is now increased, and produces a larger emitter and collector current, causing greater current flow through R2. The collector current flowing through R2 produces a larger voltage drop across R2, and a more positive (less negative) voltage on the collector of Q1. The increased positive collector voltage is fed back to the base, and causes a decrease in emitter and collector current, producing a negative collector voltage swing. This negative swing is fed back to the base through Cl and reduces the positive voltage on the capacitor, discharging it a slight amount. Emitter and collector current is again increased, and a positive swing is again fed back to the base. Thus, instead of decreasing exponentially between time t, and t<sub>3</sub>, the base charge voltage on Cl is reduced linearly. As the forward bias is increased between pulses by the discharge of Cl, the collector voltage constantly rises. At time t<sub>a</sub>, it again reaches its initial value, the leading edge of the next input pulse arrives, and applies a positive-going voltage to the base of Q1. From time t<sub>a</sub> to t<sub>4</sub> the cycle of action described above occurs again. The square-wave input thus creates a triangular output, which is the integral of the square-wave input. The output voltage and wave shape may be changed somewhat be selecting the proper time constant and changing the input voltage shape and duration.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional voh-ohmeters. Be careful also to observe proper polarity when checking continuity, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** An output cannot be produced if the collector supply is defective, or transistor Q1 is defective.

If collector load resistor R2 is defective, input variations will not produce output variations. If resistor RI is open, no signal can be applied to the base of Q1. No collector voltage will be available if collector supply voltage source  $V_{\infty}$  is defective. If none of these components is defective and there is no output, transistor Q1 is probably defective.

Low or Distorted Output. A low or distorted output may be the result of a shorted base resistor, a defective feedback network, a defective collector supply, or a defective transistor, Q1.

A shorted base resistor will change the r-c time constant so that the base boltage of Q 1 will no longer vary linearly and cause an abrupt decrease in output. If feedback capacitor Cl is open, no collector to base feedback will occur and the output variations will duplicate the input variations. If this capacitor (Cl) was shorted the collector and base of Q1 will be tied together, causing Q1 to act as a diode. A defective collector supply voltage source may cause the collector voltage to be higher or lower than the required voltage. If none of the previously mentioned components is found defective and the output is low or distorted, transistor Q1 is defective.

#### LOGARITHMIC AMPLIFIER (ELECTRON TUBE)

#### Application.

The logarithmic amplifier is used in analog computers and cathode-ray tube circuits to produce an output voltage which varies as the logarithm of the input voltage.

## Characteristics.

Circuit uses two electron tubes; a variablemu pentode and a constant-current pentode.

AMPLIFIERS

Plate of the constant-current pentode is connected directly to the cathode of the variable-mu pentode.

Control grid of the variable-mu pentode is maintained at a constant potential by **fixed** bias.

Output voltage is taken between the cathode and control grid of the variable-mu pentode.

## **Circuit Analysis.**

General. The logarithmic amplifier uses two pentodes in a circuit configuration where the plate of a constant-current pentode is directly connected to the cathode of a variable-mu pentode. The variable-mu pentode has a natural logarithmic relationship from the input to the output, where the output voltage and plate current are normally proportional to the natural logarith base e raised to a power equal to the input voltage. In this circuit, however, the output is taken from between the cathode and grid instead of the plate, and the input is applied directly to the cathode. Regardless of the output connection, the output voltage stiU varies proportionally to the tube plate current, and the plate current varies logarithmically with the cathode input voltage. The input voltage applied to the cathode is the plate voltage of the constantcurrent tube, which varies directly in relation to the signal voltage applied to the grid of the constantcurrent tube. Thus, the final output voltage varies in relation to the natural logarithm (loge) of the input voltage.

**Circuit Operation.** The schematic of a typical logarithmic amplifier is shown in the accompanying illustration. The input signals is applied across resistor R1 to the grid of Vl, a constant-current, sharp cutoff pentode. Resistors R1 and R2 develop a bias potential between the grid of Vl, and the cathode. Resistor R3 is a screen grid voltage-dropping resistor, and capacitor C 1 is the screen grid bypass capacitor. Electron tube V2 is a variable-mu pentode, which has a constant control grid voltage ( $E_{x}$ ) applied.



Logarithmic Amplifier

When the positive-going portion of a sinusoidally **varying** input voltage is applied across resistor RI to the control grid of Vl, it produces a corresponding increase in plate current conduction. Plate voltage is reduced as plate current increases. The reduced plate voltage causes a reduction in the voltage applied to the cathode of V2. This reduced cathode voltage is equivalent to a decrease in the grid voltage of V2, although the grid voltage is maintained at a fixed negative bias value by a separate supply. As a result, the plate conduction of V2 is increased and the plate voltage of V2 is decreased proportionally. Tube V2 is — operated along the nonlinear portion of the (grid voltage-plate voltage) transfer characteristic curve of the variable-mu pentode. The resultant plate voltage

decrease causes the grid-to-cathode bias voltage to be decreased by an amount equal to the natural logarithm of the plate voltage. A bias decrease produces a more positive grid-to-cathode voltage, which is the output voltage. Since the input voltage variations cause corresponding variations in the plate currents and plate voltage of V1 and V2, the relation between the input signal and plate voltage of V2 is linear. However, the grid-to-cathode voltage (output voltage) varies at a rate equal to the natural logarithm of the plate voltage of V2. The positive-going output voltage is then proportional to the natural logarith of the positive-going input signal.

As the negative-going portion of the signal is applied to the grid of VI, the conduction of V1 is decreased and the plate voltage is increased. The increased plate voltage of V1 results in increased voltage applied at the cathode V2. The higher cathode voltage causes a decreased plate current and a proportional increase in plate voltage of V2. The plate voltage increase causes the grid-to-cathode voltage of V2 to become more negative by an amount equal to the natural logarithm of the plate voltage. The negative-going input voltage then causes a negative-going output proportional to the logarithm of the input signal.

## Failure Analysis.

**No Output.** An open cathode resistor, a defective pentode VI or V2, or a defective plate supply voltage source can result in a loss of output.

Cathode resistor R2, if open, will prevent any current flow in the circuit. If pentode V1 were defective, no voltage would be applied to the cathode of V2 and thus, no voltage would appear at the output. If the proper voltages appear on the elements of V1 and there is no output, V1 is defective. If the proper voltage on the plate of V1, pentode V2 is defective. No voltage on the plate of V1, pentode V2 is defective. No voltage on the plate of V2 (and the screen grid of VI) indicates that plate supply voltage source  $E_{bb}$  is defective.

**Low Output.** Low Output can result from low plate supply voltage, low V2 grid bias, or from a defective screen voltage-dropping resistor.

Low plate supply voltage causes the conduction of V1 and V2 to be lower than desirable and makes a lower voltage appear at the cathode of V2. Low bias voltage on the control grid of V2 also Iowers the potential existing between the grid and cathode of V2. If screen grid dropping resistor R3 is open, or

larger than it should be, the conduction of V1 will not be sufficient to produce a normal output.

**Distorted Output.** If grid resistor RI is defective, cathode resistor R2 is shorted, bypass capacitor C 1 is defective, or pentodes VI or V2 are defective, the output voltage may be distorted.

A shorted or open grid resistor Rl, or shorted cathode resistor R2, produces a reduced bias on V1 and causes VI to be operated on a different portion of the pentode characteristic curve. This, in turn, causes the output to vary improperly with an input signal. An open screen grid bypass capacitor Cl will allow the screen grid voltage to vary with signal current variations in the plate circuit and produce distortion in V1. If none of these conditions exists and proper **voltages** are available on the elements of VI, pentode VI is probably defective. If the plate supply voltage of V1 is incorrect and the voltages on the elements of V2 are correct, pentode V2 is probably defective.

#### LOGARITHMIC AMPLIFIER (SEMICONDUCTOR)

#### Application.

The logarithmic amplifier produces an output which is proportional to the logarithm of the input. The logarithmic amplifier is used in analog computers and cathode-ray circuits.

#### Characteristics.

**The** logarithmic amplifier consists of three stages– a dc amplifier, an emitter follower, and a logarithmic circuit.

Two crystal diodes produce an output proportional to the logarithm of the applied signal.

The amplifier provides low-voltage gain.

#### Circuit Analysis.

**General.** This amplifier is especially useful in controlling and maintaining the output of an exponentially increasing input to a linear output. The amplifier, however, can be used to produce an output which is the logarithm of any input. The operation of this circuit is based on the inherent characteristic of silicon semi-conductor diodes to" develop a current which is the logarithm of the signal applied to these diodes. The driving circuit for the diodes consists of an operational amplifier and an emitter-follower circuit connected in series with the collector and supply source. The operatiomd amplifier increases signal

strength so that the logarithmic compression of the signal by the diode will not reduce the output to the point where it is unusable. The emitter-follower circuit maintains a high output impedance for the operational amplifier and prevents any load changes from greatly affecting the output impedance of the operational amplifier.

**Circuit Operation.** The schematic of a typical transistor logarithmic amplifier is shown in the **accom**panying illustration. In the circuit, resistors Rl, R2, and R3 provide voltage divider base bias voltage for transistor Q1. Resistors R2 and R4 also attenuate the input voltage before applying it to the base of transistor Q1. Transistor Q1 and emitter resistor R6 corm prise a series load for transistor Q2. Capacitor C1 couples the output of transistor Q1 to the logarithmic output network consisting of the parallel diode combination of CR1 and CR2.



### Logarithmic Amplifier

As the positive portion of a sinusoidally varying signal is applied to the input, the bases of both Q1 and Q2 are driven positive. The base of Q1 is driven to a less positive potential than the base of Q2, since the input voltage is attenuated by resistors R2 and R4. The positive-going input voltage decreases the forward bias of both transistors, and the emitter-to-collector current of both transistors decreases. As a result of decreased collector current, the collector voltage of Q2 attempts to increase (rise negatively).

Since the collector voltage of Q1 remains at the negative collector supply voltage value, the decreased emitter current increases the internal resistance of Q2 and causes the emitter of Q1 to become more positive. The voltage at the collector of Q2 then decreases. This, in effect, helps to decrease the total collector voltage swing of Q2 without lowering the supply impedance. The reduced collector current of Q2, however, tends to allow more current to be shunted around Q1 through CR2 without decreasing the supply impedance. The output voltage produced across CR2 is proportional to the natural logarithm of the current flowing through CR2.

As the sine wave reaches its positive peak and swings negative, the input voltage applied to the bases of Q1 and Q2 goes negative. Thus, the forward bias of both transistors increases, and the forward bias of Q1 is somewhat less than the forward bias of Q2 as a result of the attenuation provided by resistors R2 and R4. The current flowing from emitter to collector of each transistor now increases. The current increase of Q2 would normally be much greater than the current increase of Q1. The collector voltage of Q2 becomes more positive by the increased voltage drop across resistor R6. However, the internal impedance of Q1 is lowered, reducing the drop across Ql, and the effective supply voltage at the input to R6 increases. Thus, the collector voltage swing of Q2 is reduced. The collector output voltage swing is coupled through capacitor Cl to the diodes, and since it is positive-going, CR1 now conducts and CR2 ceases to conduct. The output voltage produced across CRI is proportional to the natural logarithm of the current flowing through it.

Semiconductor diodes provide a good logarithmic range when the current flowing through the diode is larger than the saturation current of the diode. The output voltage is then proportional to the natural logarithm of the quantity formed by the instantaneous forward current through the diode (,F) plus the saturation current value (Is), divided by the saturation current. This quantity is added to the diode voltage drop which is the product of the current through the diode (iF) and the actual resistance of the diode (Rd). This proportionality is expressed mathematically as:

$$V = \log_e \frac{(iF + Is)}{Is} + iFRd$$

Hence a logarithmic output is produced.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of a conventional volt-ohmmeter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** An output may not be produced if the collector supply is defective, if either transistor is defective, if the collector load resistor, or emitter bias resistor is open, if the coupling capacitor if open, or if both diodes are defective.

A defective collector supply source ( $V_{CC}$ ) prevents any voltage from being available on the collectors of either transistor. If either transistor **Q1** or Q2 is defective, no current carI flow in the circuit. Likewise, current cannot flow in the circuit if the collector load resistor of Q2 (R6) or emitter bias resistor (R5) is open. An open coupling capacitor, C 1 prevents current from flowing through either diode. If there is no output developed and if none of the previously mentioned components is defective, both diodes CR1 and CR2 are probably defective.

Low or Distorted Output. A low or distorted output may be produced if any of the biasing resistors is defective, the coupling capacitor Cl is shorted, either diode is defective, or if the collector supply voltage source is defective.

If any of the bias resistors Rl, R2, R3, R4 is shorted, the bias voltage available for **Q1** and **Q2** is incorrect. If resistor R2 or R4 is open, the input signal will not be applied to Q1. A shorted coupling capacitor Cl allows the dc voltage on the collector of Q2 to be applied to the crystrd diodes. If either diode CR1 or CR2 is defective, a logarithmic output will **only** be produced for one half of the input signal. A low supply voltage will prevent the correct supply voltage from being applied to either collector and produce a lower than normal output.

#### SUMMING AMPLIFIER (ELECTRON TUBE)

### Application.

**The** summing amplifier is an operational amplifier used in analog computer circuitry to develop an output voltage which is the sum of two or more input voltages of the same polarity and phase.

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#### Characteristics.

**High** stabilized gain. Negative feedback is employed. Fixed or self bias maybe employed. Input and output networks are resistive. Amplifier stages are directly coupled.

## Circuit Analysis.

**General.** A summing amplifier is a direct-coupled amplifier with high stabilized gain. It produces an output voltage that is equal or proportional to the sum of the applied input voltages, which are **usually** of the same phase and polarity. The input voltages are applied to the grid of an electron tube through equal input resistors forming a summing network. The corn bined input voltages are inverted and amplified by the tube. A portion of this voltage is fed back to the input of the amplifier through a resistive feedback network. This feedback voltage stabilizes the output and maintains a relatively constant gain.

**Circuit Operation.** The accompanying illustration shows a summing amplifier in symbolic one-line form. Using this type of circuit representation, the amplifier is indicated by an isosceles triangle. The base of the triangle represents the input of the amplifier and the vertex represents the output of the amplifier. Resistors RI, R2, and R3 form the summing network which provides the input signal to the input of the amplifier. Resistor R4 forms the feedback network for the amplifier. The one-line type of diagram may use a vacuum tube, transistor, or integrated circuit as the amplifier. The symbolic representation is used to show the relation among the input, the output, the feedback network, and the amplifier in simplified form.



**Summing Amplifier Circuit Representation** 

In the following schematic diagram, the operational amplifier uses triode VI, Resistors RI, R2,

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R3, and R6 form a resistive summing network which provides the input signal to the grid of V1. Resistor R8 is a cathode bias resistor bypassed by capacitor C 1. Resistor R7 is the plate load resistor from which the output voltage is obtained. Resistor R4 is the feedback resistor which returns a portion of the output voltage to the input to prevent distortion and drift. Fixed negative bias voltage is applied through grid-isolating and voltage-dropping resistor R5. Resistor R6 forms a bias bleeder network with R5 to stabilize the **fixed** bias voltage on the grid of VI and completes the summing network path to ground.



**Summing Amplifier Circuit** 

Voltages of the same polarity and phase are applied to each input simultaneously. The total value of the added input voltages appears at the grid of VI, and produces an increased plate current, which is proportional to the summed input voltage. The plate (and output) voltage decreases in relation to the plate current increase, creating a negative voltage swing. A portion of this negative plate voltage swing is returned to the grid of V1 through feedback resistor R4. This ensures that any distortion or drift existing in the input signal at the grid is canceled by feedback 180° out of phase with the input. The positive plate voltage fed back to the grid of V1 through R4 requires that a fized negative bias voltage be applied to the grid to prevent the grid from going positive and driving V1 to saturation. A negative voltage source supplies the added bias to the grid of VI through

resistor R5. Resistor R6 prevents a grid-current initiated voltage drop across R5 from changing the bias voltage at the grid of V1.

When the input voltage swings in a negative direction or reduces, the plate current also decreases. The decrease in plate current causes the plate (output) voltage to rise toward the supply value, creating a positive swing. A portion of the increasing plate voltage swing is fed back to the grid to cancel again any input signal distortion or drift.

The summing amplifier depends upon the feedback network to provide a constant gain despite any variation in tube characteristics. Although a high gain is produced by the tube, the feedback connection reduces the overall gain obtained by the amount of feedback. When an input voltage is applied to either Rl, R2, or R3 it will cause a current to flow through the respective resistor and a voltage wiU be applied to the grid of VI. When this input signal increases, the first small change in voltage is amplified by V1 and appears in the output circuit. In turn, a portion of this output voltage is fed back through R4, and being out of phase with the input, decreases the total input voltage at the grid. The decrease in input is amplified and fed back again to increase the amplitude of the input voltage. This process continues until the amplifier reaches a point of stable operation. If the input resistance is equal to the feedback resistance, the output voltage is equal to the input voltage, except that the output polarity is reversed (provided that an odd number of stages is used). Hence, if the input voltage is doubled, the output voltage will double. The amount of feedback used determines whether or not the output signal will be equal to, greather than, or less than the actual value of input voltage. So, depending upon design, the summing amplifier may not actually. amplify the total signal, but it will produce an output which does represent the sum of the applied input voltages.

## Failure Analysis.

**No Output.** Lack of plate voltage, a defective tube, an open input circuit, or lack of input signal can cause a loss of output. If plate load resistor R7 is open, no voltage will appear on the plate of V1. An open cathode resistor, R8, will prevent the tube from operating. Excessive bias caused by a shorted R5 can produce plate current cutoff and no output. Conversely, if R5 is open, a high positive bias voltage will be fed back from the plate of V1 to the grid and cause heavy plate current flow. In this case, the final value of plate current will be determined by cathode resistor R8, the plate voltage of VI will be extremely low, and a large voltage drop will occur across plate load resistor R7, In this instance, although an apparent output will be obtained, it will be constant, and the circuit will no longer act as an adder. If bias and plate voltages measure normal and input voltage is present on the grid of VI, but there is no output, the tube is probably defective. For the input circuit to be open, resistors R1, R2, and R3 must simultaneously be open. Check for the proper resistance value and continuity.

Low Output. A low output is an inaccurate output, and can be caused by a defective input circuit, improper bias and plate voltages, as well as a defective tube. Check Rl, R2, R3, and R6 for continuity and resistance. Measure the cathode, grid, and plate voltages with no input applied. No cathode voltage indicates the possibility that capacitor Cl is shorted or V1 is defective. Improper grid bias voltage indicates that R4, R5, or R6 are defective, or that the bias supply is at fault. Improper plate voltage indicates that R4, R7, or V1 can be defective.

**Distorted Output.** In the summing amplifier, am inaccurate output can be considered as a distorted output. Usually a change in feedback resistor R4, or a change in the values of input resistors R1, R2, or R3 are the cause, or the tube is defective. Check the values of the resistors to make certain that they are normal. Also check the bias and plate voltage sources to make certain that the external circuits are not at fault.

#### SUMMING AMPLIFIER (SEMICONDUCTOR)

#### Application.

The summing amplifier produces an output voltage which is the sum of two or more input voltages of the same polarity and phase. The summing amplifier is primarily used in analog computers, and in control and instrumentation circuitry.

#### Characteristics.

A number of input signals are applied to produce a single output.

Resistive input summing networks are used. Negative feedback is used.

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Circuit Analysis.

**General.** A summing amplifier uses a directcoupled amplifier with high stabilized gain. It produces an output voltage that is proportional to the sum of the applied input voltages. Each input voltage has the same phase and polarity as the other input. The input voltages are applied to the base of a transistor through a summing network. The combined signals are inverted and amplified across a common load resistor. A portion of this output voltage is fed back to the base of the transistor as negative feedback. The feedback voltage stabilizes the output and maintains a relatively constant gain.

**Circuit Operation.** The schematic diagram of a typicrd transistorized summing amplifier is shown in the accompanying illustration. Resistor Rl, R2, and R3 **together** with R6, form a resistive summing network, which provides the total input signal to the base of transistor Q1. Resistor R4 is the collector-to-base feedback resistor and together with R6 supplies base bias to Q1. Resistor R5 is the collector load resistor.



**Summing Amplifier** 

Separate positive signal voltages of the same phase and frequency are applied to resistors Rl, R2, and R3. The total sum of these voltages appears across R6 (which completes the path to ground) at the base of Ql, and reduces the normal forward bias of the transistor. The emitter and collector currents are thereby reduced, allowing the collector voltage to rise and

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approach the negative supply voltage value. A portion of this negative voltage swing is returned to the base of **Q1** through feedback resistor R4. This negative feedback voltage cancels any distortion or drift existing in the combined input voltage since it is  $180^{\circ}$  out of phase with the input signal.

When the input voltage swings negative, the **com**bined voltages at the base of Q1 develop an increased forward bias. As a result, the emitter and collector currents increase. The increased collector current flow through resistor R5 causes an increased voltage drop across the load. The collector of Q1 is thus driven to a less negative potential (more positive). A portion of this positive collector voltage swing is fedback to the base of Q1 through R4 where it again cancels any input signal distortion or drift. The output voltage taken between collector and ground is the amplified output which is proportional to the sum of all of the inputs.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** A lack of output may result if all inputs are open, the collector load is defective, the collector supply is defective, or if transistor Q1 is defective or improperly biased.

If input resistors, R1, R2, and R3 are all open, no input voltage can be applied to the base of Q1. An open collector load resistor, R5, will prevent any collector supply voltage from appearing at the collector of Q1. If the collector supply voltage source,  $V_{\infty}$  is defective, no voltage will appear at the collector of Q1. If none of these components is found to be defective and there is no output, transistor Q1 is probably defective; or R4 may be open, causing loss of forward bias.

Low or Distorted Output. The output of the summing amplifier is low or distorted if any of the inputs is defective, if the feedback network is defective, if the collector supply is defective, or the transistor is defective.

If one or two of the input resistors are open, only the signals applied to the remaining input resistors will be applied to the base of Q1 across R6. If any or all of these resistors are shorted, the input signals will not be properly summed before being applied to the base of Q1. If feedback resistor R4 is open, any distortion of the input signal will not be corrected before being applied to the base. Transistor Q1 will act as a diode if resistor R4 becomes shorted. The input variations will then be rectified and appear as an average steady output voltage. The collector voltage may be higher or lower than the required voltage, If collector supply voltage source  $V_{ee}$  is defective. If **the** components are not found to be defective with abnormal output, transistor Q1 is probably defective.

## **RING-BRIDGE AMPLIFIER (SEMICONDUCTOR)**

## Application.

The ring-bridge amplifier is used to detect and amplify a double-sideband suppressed-carrier signal or a single-sideband **signal**.

## Characteristics.

Requires a ring-bridge detector and a transistor amplifier.

Two stages are needed to provide the dual function of this circuit.

Transformer coupling is used between stages, but the output stage is direct-coupled to the load.

A reference oscillator input is required to produce an output.

### Circuit Analysis.

General. The ring-bridge amplifier is a two-state circuit consisting of a ring-type rectifier or detector, transformer-coupled into a dc operational amplifier circuit. The ring-type detector appears in the form of a bridge rectifier, from which the circuit name is derived. A reference oscillator provides a simulated carrier which is transformer-coupled between the center taps of the input and output transformers of the detector bridge, so that an in-phase signal may be coupled to each pair of diodes. No output is obtained as long as the simulated carrier signal alone is applied, since in the balanced bridge circuit equal conduction between opposite diodes occurs, and equal current flowing in opposite directions in the two halves of the same transformer effectively cancels any output. The applied sideband input signal beats with the simulated carrier, and results in the addition to and subtraction

of the input signal from the oscillator signal, causing each diode to conduct alternately on opposite half cycles. The output produced by the bridge diodes is coupled through the output transformer of the detector to the input of the second stage, where the detected signal is inverted and amplified.

**Circuit Operation.** A typical ring-bridge amplifier schematic is shown in the accompanying illustration. Transformer T1 is the r-f (or subcarrier) input transformer while T2 is the reference oscillator transformer. Transformer T2 is connected between the center taps of T1 and T3. Transformer T3 is the output transformer of the detector stage. Diodes CR1 and CR3 form one group of bridge rectifiers and CR2 and CR4 form the other group. The diode pairs conduct simultaneously for in-phase signals and alternately for push-pull signals. Resistor R1 is an emitter stabilization resistor for Q1. Resistor R2 is the collector load resistor of Q1. The collector supply voltage is  $V_{CC}$  and  $V_{EB}$  is a separate emitter bias voltage source.



**Ring-Bridga Amplifier** 

When no input signal is applied, except the reference signal from the oscillator, the center tap of T3 is driven positive, and the center tap of T1 is driven negative. Diodes CR2 and CR4 conduct because of the positive voltage applied to the anodes. Electron flow is from the negative terminal of T2 through the lower half of T1 secondary and the cathode to anode of CR4, back through the lower half of T3 primary to the positive terminal of T2. Current also flows through the top half of the secondary of T1 to the

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junction of CR2 and CR1. Diode CR2 is forwardbiased and conducts, causing current to flow through the top of T3 primary winding back to the positive end of T2. Because of the equal and opposite currents flowing through each half of the secondary of'Tl and the primary of T3, the transformer windings cancel, preventing any voltage from being induced into either the primary of T1 or the secondary of T3. As a result, no input is applied to the operational amplifier and no output is produced. When the polarity on the secondary of T2 reverses, a similar situation arises with diodes CR1 and CR3 conducting. In this case, current flows from the center tap of T3 to the cathodes of CR1 and CR3, and to the plates of CR2 and CR4. CR1 and CR3 conduct, causing equal currents to flow through opposite ends of T 1 to the center tap. The currents through both halves of the primary of T3 are equal, but opposite in polarity, which again causes the opposing induction fields set up in T3 to cancel, resulting in no output from the detector and no output from the amplifier.

Since the reference oscillator amplitude is stronger than that of the incoming r-f sideband signals, the polarity of the reference oscillator on the diodes controls conduction. Assume that a push-pull r-f signal is applied to the input of Tl, developing a voltage across the secondary of T1 which is negative at the top and positive at the bottom. The reference oscillator also assumed to be applying a signal which normally keeps diodes CR2 and CR4 conducting; when both signals add instantaneously, CR2 then conducts more and CR4 conducts less, developing unequal currents flowing from each end of T3 to the center tap. In this case, a greater current flows from the top of T3 to the center tap as a result of the greater conduction of **CR2.** At the same time, less current flows from the bottom of T3 to the center tap as a result of the lesser conduction of CR4. The result of these unbalanced currents is that the top of T3 becomes more negative with respect to the bottom of T3. The induced voltage in the secondary of T3 is positive at the top of the winding with respect to the bottom. Since the top of the secondary of T3 is connected directly to the base of Ql, the positive input voltage reduces the forward bias of Q1. Q1 conducts less as a result of this reduced forward bias. The smaller emitter-to-coflector current of QI results in less collector currently flowing through R2, producing a smaller IR drop across R2. The smaller IR drop across

R2 causes the voltage on the collector of Q1 to rise toward the collector supply voltage value.

The result of a positive-going input signal riding on a reference carrier input is a negative-going output, which is amplified. The reference carrier is automatically canceled so that it does not appear in the output.

A negative-going input signal riding on a reference carrier input produces the opposite action. Thus, diode CR4 conducts more, while diode CR2 conducts less.

The potential across the primary of T3 now reverses, inducing a voltage across the secondary of T3 which is 180° out of phase with the primary voltage. Hence, a negative voltage is now applied to the base of Q1, producing a greater forward bias; consequently, the greater emitter-to-collector current produces a greater IR drop across R2, and a positivegoing collector and output voltage. Again, the reference carrier signal is automatically removed by the canceling action in T3, previously described.

#### Failure Analysis.

General. When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of conventional volt-ohmmeters. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false lowresistance reading.

No Output. The output may be lacking if transformer T1 and T3 is defective, if the collector load resistor is defective, if the emitter stabilizing resistor is open, if the bias voltage source is open, if the collector supply source is defective, if any of the four diodes is defective, or if transistor Q1 is defective.

If transformer T1 is completely open or completely shorted, the input signal will not be

coupled to the detector circuit and no input will be applied to the amplifier circuit. If transformer T3 is completely open or completely shorted, the detected signal can not be applied to the amplifier. A shorted or open collector load resistor, R2 prevents any sup ply voltage from being applied to the collector of Q1. Collector voltage is prevented from being applied to the collector also, if collector supply voltage source V is defective. If emitter stabilization resistor R1 is open, the transistor amplifier circuit sees an open emitter circuit and no current will flow through Q1. will also prevent current flow in the amplifier circuit. If diodes CR1, CR2, CR3, and CR4 are defective, no potentird difference can be developed across T3, and thus no input will be applied to the base of Q1. If one of these components is defective, and there still is no output developed, transistor Q1 is probably at fault.

Low or Distorted Output. A low or distorted output can result from a defective reference carrier oscillator transformer T2, a defective diode, a defective transformer T1 or T3, a defective collector supply voltage source, a defective emitter bias source voltage, or a defective transistor.

If reference carrier oscillator transformer T2 is defective, the reference carrier signal will be absent and prevent the detector bridge from being properly balanced. If any of the diodes in the bridge is shorted or open, proper current will not flow through the diode and the proper potential difference will not be developed across the primary of T3. If either transformer T1 or T3 is partially shorted, improper voltage will be applied to the detector bridge circuit or to the amplifier circuit. A defective emitter bias source will cause improper bias to be developed and produce distortion. If collector supply source V<sub>c</sub> is defective, improper voltage will be applied to the collector of Q1. If these components are not found to be defective and a low or distorted output is developed, transistor Q1 is probably defective.

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## SECTION 6 OSCILLATORS

#### PART 6-1. ELECTRONIC

## ARMSTRONG (TICKLER-COIL) OSCILLATOR (ELECTRON TUBE)

#### Application.

The Armstrong oscillator is used to produce a sine-wave output of constant amplitude and fairly constant frequency within the r-f range. The circuit is generally used as a local oscillator in receivers, as a single source in signal generators, and as a variable-frequency oscillator over the medium- and high-frequency ranges.

#### Characteristics.

Utilizes an L-C tuned grid circuit to establish the frequency of oscillation. Feedback is accomplished by mutual inductive coupling between the tickler coil and the L-C tuned grid circuit.

Operates Class C with automatic self-bias. Frequency stability is fair.

Output amplitude is relatively constant.

#### Circuit Analysis.

**General.** Oscillations of a tuned circuit will tend to die out at an exponential rate and will finally cease, unless energy is replaced at regular intervals. For oscillations to be sustained, sufficient energy must be supplied to overcome circuit losses. The use of an electron tube as an amplifier provides the additional energy necessary to sustain oscillations. The energy applied to the tuned circuit must be of the correct phase relationship to aid the initial oscillations and of sufficient amplitude to overcome circuit losses in the tuned circuit.

The circuit used to provide this type of feedback is called a *regenerative circuit, and* the *energy* supplied

is called *positive feedback*. In the accompanying circuit schematic the tuned L-C circuit is designated as L1, C 1; the tickler (feedback) coil is designated as L2.

**Circuit Operation. The** accompanying circuit schematic illustrates a triode electron tube in an L-C Armstrong oscillator circuit. Inductance L1 and capacitor Cl form the resonant grid circuit. Inductance L2 is the plate, or tickler, coil and is mutually coupled to L1, to couple a feedback voltage to inductance L1 by transformer action. Capacitor C2 and resistor R1 form an R-C circuit which is used to develop the operating bias. Capacitor C3 functions as an r-f bypass to place the B+ terminal of tickler coil L2 at signal ground potential. Resistor R2 isolates the B+ line from the r-f signal and also serves to reduce the input voltage applied to the oscillator circuit. Capacitor  $C_c$  is the output coupling capacitor.



L-C Armstrong (Tickler-Coil) Oscillator

For the following discussion of circuit operation, refer to the accompanying illustration of oscillator grid-signal voltage and plate-current waveforms.



Theoretical Grid-Voltage and Plate-Current Waveforms

Initially, the tube is at zero bias (t. on waveform illustration) to permit the circuit to be self-starting. When input power is applied to the circuit, the tube conducts because of the lack of operating bias. As the plate current increases through tickler coil L2, an expanding magnetic field is built up around the tickler coil. This expanding field causes an increasing voltage to be induced in inductance L1 of the tuned circuit, and this voltage is of such polarity that the grid of V1 is made positive with respect to the cathode. The positive grid condition increases the flow of plate current, which further increases the field about tickler coil L2; consequently, the voltage induced in inductance L1 increases and the grid is drawn further in the positive direction. This process continues until saturation is reached, at which time no further increase in plate current can take place (point *a* on waveforms).

During the period of time that a charging voltage is induced in inductance L1, capacitor C 1 changes to maximum; also, capacitor C2 receives a charge as the result of grid-current flow through the low internal cathode-to-grid resistance of the tube.

When the plate current reaches saturation, a steady (unchanging) magnetic field is produced about tickler coil L2, and, as a result, a voltage is no longer induced

in inductance L1. With no induced voltage present, capacitor Cl begins to discharge through inductance Ll, and capacitor C2 begins to discharge through resistor R1 (and L1). The positive voltage on the grid of V1 decreases as capacitor C1 discharges through inductance L1, and this decrease in the grid voltage causes the plate current to decrease below the saturation value. The decrease in plate current through tickler coil L2 causes the magnetic field about the tickler coil to decrease and start to collapse, and thus causes an increasing voltage to be induced in inductance L1. However, the polarity of the induced voltage is reversed from that originally inducted in L1 when the magnetic field about tickler coil L2 was expanding. Hence, the induced voltage causes the grid of V1 to be driven negative with respect to the cathode, and the plate current is further decreased, causing the magnetic field about tickler coil L2 to collapse completely. As this occurs, the grid of V1 becomes increasingly negative until a voltage is reached which prevents any further decrease in plate current (point **b** on waveforms). (The voltage induced in L1 during this time also aids the discharge of Cl.)

At this instant, capacitor C2 starts to discharge through resistor RI (and Ll), decreasing slightly the negative potential existing between the grid and cathode of VI. Also, capacitor C 1 discharges through inductance LI, producing an expanding magnetic field about inductance L1; when capacitor Cl is completely discharged, the magnetic field begins to collapse. The collapsing magnetic field about inductance L1 again produces a voltage across the inductance which charges capacitor Cl and also drives the grid of V1 in a positive direction. As the grid of VI becomes positive with respect to the cathode, plate current begins to flow through tickler coil L2. -The magnetic field produced about tickler coil L2 again increases and induces a voltage in inductance Ll, which drives the grid still further into the positive condition. Grid current again flows through the internal cathode-to-grid resistance of the tube to produce a negative charge on capacitor C2. Plate current again rises to maximum, at which time no further increase in plate current can take place (point c on waveforms).

The entire process repeats as described above, with the bias voltage continuing to build up across capacitor C2 until a steady value of Class C bias, effectively across resistor RI, is reached. The interchange of energy at the resonant-frequency rate between inductance L1 and capacitor Cl of the tank circuit maintains the oscillations during the period of time that plate current is cut off and no energy is supplied to the tuned circuit through the tickler-coil feedback circuit.

As oscillations build up, the maximum signal across the resonant circuit becomes increasingly greater. Note that the grid-leak-and-capacitor combination, R1 and C2, is used to develop the operating bias, to permit Class C operation of the tube. When the circuit is placed in operation, a stable operating point is quickly reached where the positive signal peaks are of sufficient amplitude to cause grid current to flow and to charge the grid capacitor, C2. Momentarily, when the signal is less positive, grid current ceases to flow, and capacitor C2 discharges slowly through grid-leak resistor R1. Since the value of R1 is large, only a small amount of charge is lost by capacitor C2 before the signal again is sufficiently positive to cause the grid to again draw current. As a result of this automatic charge-discharge action, an average value of negative bias, approximately the value to which capacitor C2 is being charged, is developed across R1, between the grid and cathode. Whenever the signal amplitude tends to increase, additional grid current flows through the internal cathode-to-grid resistance of the tube, and, therefore, capacitor C2 is charged to a higher value. Consequently, the bias voltage also increases, and the resulting effect is to decrease the gain of the tube. As the gain of the tube decreases, the output-signal level also decreases and returns to approximately its original amplitude. Similarly, when the signal amplitude tends to decrease, there is a decrease in bias voltage and an accompanying increase in the gain of the tube. As the gain of the tube increases, the output-signal level also increases and returns to its original amplitude. Thus, through the regulating action of grid-leak bias, the circuit operation is stabilized, and the amplitude of the output is held essentially constant.

The oscillator output frequency is determined primarily by the values of inductance L1 and capacitance Cl at resonance

(f. = 
$$\frac{1}{2\pi\sqrt{LC}}$$
),

although interelectrode capacitances of the electron tube and distributed capacitances and inductances of

the circuit also have an effect upon the oscillator frequency. In most circuits a variable capacitor is used to change the frequency; however a variable inductance can be used with a fixed capacitor to accomplish the same purpose.

The oscillator output, which is taken from the tuned circuit, is generally capacitively coupled (Cc) to the associated load circuit; however, inductive coupling may also be used with the output coupling coil being mutually coupled to Ll near its ground end.

Tuned-Plate Version. The proceeding circuit description covered the basic Armstrong circuit, in which the tank coil is in the grid circuit (tuned grid) and the tickler coil is in the plate circuit. Another circuit version in which these conditions are reversed in called the tuned-plate circuit. In this circuit, the tank is in the plate circuit and the tickler (feedback) coil is in the grid circuit. The operation of this oscillator is identical to that of the tuned-grid circuit, except for limitations imposed by coupling between the plate and grid. This coupling limits the range of oscillation in the tuned-grid version, but not in the tuned-plate version. Actually, the tuned-plated oscillator is considered less susceptible to frequency changes caused by power supply voltage changes than the tuned-grid oscillator. The schematic of the tuned-plate circuit is shown in the following illustration.



**Tuned-Plate Armstrong Oscillator** 

The parts in the tuned-plate oscillator are labeled the same as in the illustration of the tuned-grid oscillator, for comparison. The differences are the use of shunt plate feed in the tuned-plate circuit instead of

what is essentially series plate feed in the tuned-grid circuit and the use of series grid-leak bias instead of. shunt grid-leak bias. Actually, the use of shunt or series feed does not change the method of operation; it merely illustrates possible circuit variations. Gridleak components R1 and C2 operate in the same manner as described for the tuned-grid version, and C3 is a plate blocking and coupling capacitor instead of an r-f bypass. Note that plate dropping resistor R2 is replaced by radio-frequency choke RFC, which keeps the r-f from being shunted to ground via the power supply falter capacitors. When the circuit is energized, the flow of plate current produces tank circuit variations through L2, and an in-phase voltage is fed back through grid (tickler) coil L1 to sustain feedback exactly as described under L-C circuit operation for the tuned-grid circuit previously discussed. The grid leak formed by RI and C2 controls the amplitude and grid bias.

**Detailad Analysis.** Since the oscillator is considered to be a Class C amplifier with a feedback loop, a rigorous mathematics analysis is complex because the circuit operation is inherently non-linear. The analysis can be greatly simplified by using the equivalent plate circuit, together with a few assumptions. This method of amlysis is helped in determining the conditions necessary to produce sustained oscillations and in determining the basic frequency of oscillation. With this approach, it is customary to neglect the flow of grid current, but to bear in mind that its effect must be considered and the final results modified to take the grid current into account. Actually, losses due to grid current can be treated as an equivalent loss in the tuned circuit.

The ac equivalent circuit for the tuned plate oscillator is shown in the following illustration. Assuming that the currents are sinusoidal and neglecting grid current flow, Kirchhoff's laws and Thevenin's theorem can be applied to this circuit to obtain the limiting parameters that determine oscillation and frequency.



**Tuned Plate Equivalent Circuit** 

Mathematics analysis of the equivalent circuit for the tuned-plate oscillator shows that the critical value of coupling is:

$$M \cdot \frac{{}^{\circ}P + CRr_{p}}{\mu}$$
(1)

which gives the minimum value that M can have and still allow the circuit to oscillate. To satisfy this condition, M must be posaible and:

$$g_{m} = \frac{RC}{M} + \frac{L_{p}}{M_{rp}}$$
(2)

Thus, the coupling between grid and plate coils must exceed the minimum value indicated in equation (1), and must have the sign to produce a positive grid **voltage component** when  $I_{Lp}$  is increasing (this is the condition required for regenerative feedback). The  $\_$  frequency of oscillation is determined by:

$$\omega = \sqrt{\frac{\mathbf{R} + \mathbf{r_p}}{\mathbf{L_p} \, \mathrm{Cr_p}}} = \omega_0 \sqrt{1 + \frac{\mathbf{R}}{\mathbf{r_p}}} \text{ or } \mathbf{f} = \frac{1}{2\pi\sqrt{\mathrm{LC}}} \sqrt{\frac{\mathbf{R} + \mathbf{r_p}}{\mathbf{r_p}}}$$

It is evident from (3) that the frequency of oscillation is affected to some extent by the resistance of the load, as well as the plate resistance of the tube. With  $\mathbf{r}_{\mathbf{p}} >> \mathbf{R}$  to provide better frequency stability (which condition normally exists), we can say that for all practical purposes, or

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$$f = \frac{1}{2\pi\sqrt{LC}},$$

where C includes all of the stray and distributed capacitance that tunes  $L_{\mbox{\tiny P}}.$ 

A similar analysis of the tuned-grid circuit can **also** be made by using the following equivalent circuit.



Tuned-Grid Equivalent Circuit

In this instance it can be demonstrated that the requirement for oscillation is:

$$\mathbf{g}_{\mathbf{m}} = \frac{\mathbf{RC}}{\mathbf{M}} + \frac{\mathbf{M}}{\mathbf{L}_{\mathbf{p}}\mathbf{r}_{\mathbf{p}}} \tag{4}$$

Since the quantity M appears in the denominator of one term and in the numerator of the other, the value of  $g_m$  is large for both high and low values of M, with a minimum value existing somewhere between. This is to say that in the tuned-plate circuit, while there is a critical value of coupling below which oscillation will not occur, there is no limit to the maximum value of coupling; although plate current and output may be reduced as a consequence, oscillation will still occur. For the tuned-grid circuit there exists both a lower and an upper limit; thus if the value of coupling is too low or too high, the circuit will not oscillate. This upper limit on M could be a practical disadvantage;

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however, it appears to be of academic interest, since  
it is only true for large values of 
$$L_p$$
 and C. That is, it  
actually applied only to low r-f or audio frequencies.  
At the higher radio frequencies the effect of tube  
capacitance and distributed circuit capacitance makes  
the value of M required to satisfy this condition so  
high that it is impractical or impossible to obtain.  
Thus, although there is a difference between the  
plate and grid-tuned circuits, theoretically, it is of no  
practical consequence.

The frequency of oscillation for the tuned-grid oscillator is given as:

$$\mathbf{f} = \frac{1}{2\pi \sqrt{\mathbf{C} \left(\mathbf{L}_{g}\mathbf{r}_{p} + \mathbf{L}_{p}\mathbf{R}_{g}\right)}}}{\frac{\mathbf{P}}{\mathbf{P}}}$$
(5)

From this expression it maybe seen that if  $\mathbf{R}_{\mathbf{g}}$  is very small as compared with  $\mathbf{r}_{\mathbf{p}}$ , the quantity ( $\mathbf{L}_{g}\mathbf{r}_{p}$ +  $\mathbf{L}_{p}RJ$  is nearly identical with  $\mathbf{L}_{\mathbf{g}}\mathbf{r}_{\mathbf{p}}$ . Equation (5) may then be rewritten as:

f= f. 
$$\sqrt[l]{2\pi L_g C}$$
 (6)

The tuned-grid circuit is similar to the tuned-plate version in that the ratio rp/R should be as large as possible for good frequency stability. One other fact may readily be seen if equation (5) is rewritten as:

$$\mathbf{f} = \frac{\mathbf{f}.}{\sqrt{1 + \frac{\mathbf{L}_{\mathbf{p}} \mathbf{R}_{\mathbf{g}}}{\mathbf{L}_{\mathbf{g}} \mathbf{r}_{\mathbf{p}}}}}$$
(7)

where f. is the same as in equation (6).

Since the operating frequency of the oscillator is equal to the tank resonant frequency divided by a number slightly greater than unity, the operating frequency is slightly less than the natural resonant frequency of the tank circuit. On the other hand, the tuned-plate version has a higher frequency of oscillation than its tank circuit, as shown by equation (3). Thus, at the operating frequency, the tuned-grid tank appears as an inductive reactance, and the tuned-plate tank appears as a capacitive reactance (neglecting the effect of resistance, which is of academic interest only).

**Vector Diagram.** It is sometimes "more helpful to use vectors to show the relationships of the various currents and voltages in the circuit. The following figure shows the vector diagram for the tuned-plate circuit. In this figure, The voltage  $-\mu e_g$  is used as a reference.  $\mathbf{e}_{g}$  is about 180° out of phase with  $-\mu \mathbf{e}_{g}$ , as indicated by the negative sign preceding the real quantity  $-\mu e_{g}$ . The direction of  $i_{LP}$  may be established from the fact that  $e_g$  (the voltage induced in  $L_g$ ) equals  $-j\omega Mi_{LP}$ , and must lag i<sub>I</sub> p by 900 because of the -j coefficient. Similarly, it can be seen from the ac equivalent circuit, that iLp will  $\log e_p$  by something less than 90° because of the resistance R in series with the coil. The amount of phase difference between  $e_p$  and  $i_{Lp}$  will depend on the Q of the coil, being closer to 90° with higher values of Q (uL/R). This makes  $e_p \log -\mu e_g$  by some small angle, which is dependent on the circuit Q.  $i_c$  since it is considered purely capacitive, will lead  $\mathbf{e_p}$  by 90°. The vector sum of  $\mathbf{i_p r_p}$  and  $\mathbf{e_p}$  must equal  $-\mu e_g$ . For this to be true,  $i_p r_p$  must lead  $-\mu e_g$  by some small amount, and since the current through a resistance is in phase with the voltage drop across it,  $i_p$  may be shown as leading  $-\mu e_g$ . Thus with  $i_p$  having a leading phase angle, the tuned plate circuit is shown to be capacitive as was also proven in the mathematical analysis. Note that  $i_p$  is the ventor sum of  $i_C$ and iLp; therefore,  $i_{C}$  must be the larger quantity.



**Tuned-Plate Vector Diagram** 

The tuned grid circuit may be similarly represented by means of the following vector diagram.



**Tuned-Grid Vector Diagram** 

As with the tuned-plate oscillator, the vector representing the voltage  $-pe_{g}$  is used as a reference;  $e_{g}$ is again shown displaced 180° from  $-\mu e_g$ . Since the plate circuit is inductive and resistive in nature, plate current  $i_p$  will lag  $-\mu e_g$  by a small angle, 6. This angle will be small because  $r_p >> j\omega L_p$ . The voltage induced in the secondary circuit, e  $_{ind}$ , will lag  $i_p$  by 90° since  $e_{ind}$  equals \_@.  $\omega Mi_{LP}$ . The voltage  $e_{ind}$  may be represented by a generator in series with the grid circuit. It was shown in the mathematical analysis that the oscillator operates slightly below the tank frequency; therefore, the capacitive reactance of C will be slightly larger than the inductive reactance of  $L_{p}$ . Viewing the grid circuit as a series circuit in relation to e<sub>ind</sub>, it is seen that the secondary current  $(i_s)$  is slightly capacitive and will lead  $e_{ind}$  by a small angle. Since grid voltage  $\mathbf{e}_{\mathbf{g}}$  is the same as capacitor voltage  $e_{e}$ , it will lag current  $i_{s}$  through the capacitor by 90°. From inspection of the vector diagram, it can be seen that angle  $\theta$  is the same as the angular difference between  $e_{ind}$  and  $i_s$ . Higher values of circuit Q will tend to diminish this angular difference, thus diminishing angle  $-\theta$  and improving the stability of the oscillator.

#### Failure Analysis.

**No Output.** If the circuit is in a non-oscillating condition, negative grid bias will not be developed; as a result, the applied plate voltage will be below normal because of the passage of additional current through the dropping resistor, R2. Excessive circuit losses present in the resonant circuit or the tickler (feedback) coil will prevent sustained oscillations. Reduced tube gain will also affect stage regeneration; changing values of the grid-leak bias components, R1

and C2, will directly **affect** the operating bias and, hence, the Class C operation and gain of the tube.

**Reduced or Unstable Output.** A relative indication of oscillator output is provided by the amount of bias voltage developed across RI. This negative bias voltage is normally from 2 to 40 volts, depending upon circuit design and the applied plate voltage.

A reduction in the applied plate voltage will cause the output to be reduced. An unstable voltage source will cause the output to be unstable in amplitude and may also produce some frequency instability. Losses in the tickler (feedback) coil, due to shorted turns or poor soldered connections, can cause reduced output or unstable operation resulting from changes in amplitude of the feedback signal coupled into the resonant circuit (Ll, Cl).

Incorrect Output Frequency. Normally, a small change in output frequency can be compensated for by realigning or adjusting the variable component of ,the L-c resonant circuit, assuming that all component parts of the circuit are known to be satisfactory. Since L1 and L2 are mutually coupled, any change in inductance of one coil will have an effect upon the inductance of the other. Thus, if several turns of tickler coil L2 should become shorted, the resonant frequency of Ll, Cl will likely be affected and the output frequency will change. This condition is also likely to reduce the oscillator output, since L2 is the means by which feedback or regeneration is accomplished. Furthermore, changes in distributed circuit capacitance, changes in the value of output coupling capacitor C4 and its associated circuit load, or changes in the value of r-f bypass C3 will produce a change in the resonant frequency of L1, Cl; thus, the output frequency will depend upon the amount of reactance reflected into the tuned circuit (L1, Cl).

# ARMSTRONG (TICKLER-COIL) OSCILLATOR (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Uses an L-C parallel tuned circuit to establish the frequency of oscillation, with feedback being

provided by a separate tickler coil of proper polarity to sustain oscillation.

Operates Class C with stabilized bias for applications where linearity of waveform is not important, and Class A where linearity of waveform is important.

Frequency stability is fair (generally comparable to that of the Armstrong vacuum-tube oscillator).

#### Circuit Analysis.

General. A sine-wave output may be obtained from an oscillator utilizing a tuned L-C circuit, especially when the transistor is operating over the linear portion of its transfer characteristic curve. The L-C circuit (commonly called a tank circuit) determines the frequency of oscillation. The tank circuit can be located in either the base or the collector circuits to produce two versions of this circuit known as the tuned-base and tuned-collector circuits, respectively; these are similar to the tuned-grid and tuned-plate electron tube oscillators. Although three basic transistor configurations (common base, common emitter, and common collector) can be used, generally, only two, the common emitter and common base, are used in practice. A trend is developing towards the use of the common-emitter arrangement in preference to the others, since it so nearly parallels the electron tube and has input and output impedances that are more easily matched. In the CE circuit, since the input and output are 180 degrees out-of-phase (opposite polarity), it is necessary to provide a 180-degree phase shift (reverse polarity) to bring the output in-phase (of proper polarity) so that oscillation may be sustained. However, in the common-base and common-collector arrangements, the input and output are already in-phase (identically polarized); therefore, no phase shift (polarity reversal) is required (at extremely low frequencies excessive phase shift may prove troublesome). The basic advantage of the Armstrong oscillator, however, is that since the feedback is developed by a separate (tickler) coil, the amount and polarity of the feedback are easily adjusted at the time of manufacture by changing the number of turns or direction of the winding.

**Circuit Operation.** The three basic transistor configurations of the Armstrong oscillator circuit are shown in the following illustration.

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#### **Basic Armstrong Configurations**

Bias and plate feed arrangements are omitted for the sake of simplicity, but will be discussed later. It is assumed that forward bias is applied to the emitterbase junction and that reverse bias is applied to the collector-base junction. Only junction transistors are discussed, since point-contact transistors require slightly different considerations and their use is constantly diminishing, except for special applications which will be discussed elsewhere in this technical manual when applicable.

The common-base circuit is usually preferred at the higher frequencies because the collector-emitter capacitance,  $C_{ce}$ , helps feed back an in-phase (properly polarized) voltage independently of tickler coil L1, and oscillation is more easily obtained. In the common-emitter circuit this capacitance feeds back an out-of-phase (oppositely polarized) voltage which requires additional feedback from the tickler coil to overcome it. In both the CB and CE circuits, since feedback is primarily provided by voltage induced through the manual induction between L1 and L2, and since the voltage gain of these circuits is greater than unity, oscillation is easily sustained. In the common-collector circuit, the voltage gain is always less than unity; therefore, feedback tends to be insufficient for stable oscillation at the lower frequencies, while at the higher frequencies it is assisted by Ccc. In some instances, an **external** capacitor is added between the collector and emitter to provide additional feedback, but when this is done the oscillator can no longer be considered an Armstrong circuit; consequently, the CC circuit is not often employed for this type of oscillator.

The CB circuit with the tuned collector permits convenient matching of input and output impedances, since the low input resistance is easily matched with the tickler coil, and the high output impedance is matched by the tuned parallel-resonant tank circuit. Moreover, the collector-base internal capacitance is swamped by the high-C tank circuit.

In the common-emitter circuit, the moderate input and output impedances are more easily matched, and the tank may be placed in either the base or collector circuits without noticeably affecting the performance.

The operation of the L-C circuit is identical to that of the L-C circuit for the Armstrong electron tube oscillator circuit described in the beginning of this section. The transistor action is as follows: As the oscillator is switched on, current flows through the transistor as determined by the biasing circuit. Internal noise or thermal variations (initial current) produce a feedback voltage between the collector and the emitter which is in-phase with the input circuit. Thus, as the emitter current increases, the collector current also increases, and additional feedback between L1 and L2 further increases the emitter current until it reaches the saturation region, where the emitter current no longer increases. When the current stops changing, the induced feedback voltage is reduced until there is no longer any voltage fed back into the emitter circuit. At this time the collapsing field around the tank and tickler coils induces a reverse voltage into the emitter circuit which causes a decrease in the emitter current, and hence a decrease in the collector current. The decreasing current then induces a greater reverse voltage in the feedback loop, driving the emitter current to zero or cutoff. Although the emitter current is cut off, a small reverse saturation current  $(I_{CEO})$  flows; this current has essentially no effect on the operation of the circuit, but

d

it does represent a loss which lowers the overall efficiency. In this respect, the transistor differs from the electron tube, which has zero current flow at cutoff.

The discharge of the tank capacitor through L2 will cause the voltage applied to the emitter to rise from a reverse-bias value through zero to a forwardbias value. Emitter and collector current will flow, and the previous described action will repeat itself, resulting in sustained oscillations. Actually, the shunting action of the transistor parameters provides both a resistive and capacitive effect, which causes the frequency of operation to be slightly lower than the tank circuit resonant frequency, but the frequency decrease is so small that the basic frequency of operation is considered, for all practical purposes, to be the tank frequency that is,

$$\mathbf{F_r} = \frac{1}{27r\mathbf{V}\mathbf{LC}}$$

where L and C are the values of L2 and C at resonance.

**Tuned-Base Oscillator. The** tuned-base (tuned-grid) Armstrong oscillator using the common-emitter configuration is shown in the accompanying illustration. One voltage supply is used, with fixed bias being supplied by voltage-dividing resistors RI and  $R_{\rm B}$  (see the introduction to the amplifier section of this handbook for bias explanation). Emitter swamping resistor  $R_E$  bypassed by Cl, is used for temperature stabilization.



**Tuned-Base Armstrong Oscillator** 

The collector is shunt-fed through  $R_c$ , with C2 serving as the coupling (and blocking) capacitor for the tickler coil, to prevent shunting of the dc collector voltage to ground. The tuned tank consists of L2 and tuning capacitor C, coupled to the base of transistor Q1 by capacitor C3, which prevents short-circuiting of the base bias to ground through the tank inductor.

When the circuit is energized, the initial bias is determined by RI and  $R_{\rm B}$ , and oscillation is built Up by feedback from L1 to L2. Besides acting as a thermal stabilizer and swamping resistor, the combination of  $R_{\rm E}$  and Cl acts similarly to a grid leak in an electron tube circuit and builds up a degenerative bias which places operation in the Class C region. That is, while  $R_{\rm B}$  and R1 produce a forward bias,  $R_{\rm E}$  produces a reverse bias, with the algebraic sum of the two biases providing the operating bias. Circuit constants can be adjusted by changing the values of parts to produce practically any of bias between Class A and C. The r-f output is taken from the collector through CCC. The output frequency is determined by the resonant frequency of the tank.

**Tuned-Collector Oscillator. The** tuned-collector (tuned-plate) Armstrong oscillator using the common-emitter configuration is shown schematically in the accompanying illustration. One voltage supply is used, with fixed base bias being supplied by voltage-dividing resistors R1 and  $R_{B}$  as in the tuned-base oscillator shown previously. The arrangement below uses series base feed, together with series collector feed through the tank inductor, although parallel feed may be used equally well.



**Tuned-Collector Armstrong Oscillator** 

Since the collector is series fed through L2, tuning capacitor C is above ground and will be subject to hand-capacitance effects. In some circuit variations a radio-frequency choke may be used in series with the tank and bypassed to chassis to shunt any remaining rf around the power supply. Base bias resistor  $R_{B}$  is shunted by C<sub>B</sub>, to prevent signal variations from affecting the fixed base bias. Emitter-swamping and base-biasing arrangements operate exactly the same as in the tuned-base oscillator previously discussed. The r-f output, however, is taken through inductive coupling to the tank circuit. Use of series collector and base bias feeds eliminates the need for coupling and blocking capacitors, and thus eliminates any dead spots caused by unwanted resonances of these parts with stray circuit or internal transistor capacitance. The feedback polarity is arranged to provide a 180-degree phase shift, in order to produce positive (regenerative) feedback similar to that obtained in the tuned-base oscillator. Placing the tank in the collector circuit provides an effective swamping capacitance across the collector and emitter, to minimize effects due to the variations of  $C_{CE}$ . Although this circuit appears to be more stable from a frequency standpoint than the tuned-base oscillator, it is not so stable thermally. Since the series feed arrangement is used in both the collector and base, there is a dc path of relatively low resistance for reverse saturation current  $I_{CBO}$ , which flows during cutoff. The path is from the negative collector supply through the low resistance of L2, through the collector to the base of Q1, and through the low dc resistance of Ll, then through the high base bias resistance  $R_{\rm B}$  to the positive supply terminal. Thus the relatively high resistance of collector resistor  $\mathbf{R}_{\mathbf{C}}$  of the tuned-base oscillator circuit is replaced by the very low dc resistance of the windings of L1 and L2. As a result, the individual transistor ICBO current determines how large a current will flow through the tank and feedback inductances to decrease the effective circuit Q and reduce the over-all efficiency of the oscillator. Where battery power supplies are used, such leakage current will provide a small but constant drain on the battery, an effect not possible with electron tubes.

#### Failure Analysis.

**No Output. As** in a vacuum-tube counterpart, loss of gain in the transistor can result in lack of oscillation through loss of feedback. It should be kept in mind that, unlike the electron tube, the transistor

d cannot lose gain through loss of emission. Failures of the transistor mostly result in short- or open-circuit conditions rather than deteriorated operation. An excessive time contant in the emitter bias circuit, produced by an increase in the resistance of  $R_{\rm e}$ , could cause blocking effects. A change in the value of emitter bias capacitor Cl will affect the operating bias, will be rather unlikely to completely stop oscillation unless the change is large. Once oscillations have started, loss of forward bias through an open in the base circuit will not necessarily stop oscillations because the feedback signal swinging both positive and negative (on a reference of zero or the established self-bias) will apply on the negative or positive half cycle, depending on the circuit configuration and the type of transistor used, a forward bias and cause emitter collector current to flow (while possible, this condition is not very common). Particular care should be taken not to aggravate troubles by applying potentials greater than the rated voltages (or of the wrong polarity) to the transistor elements when checking the resistance of bias elements and circuit continuity. Failure of the tank and tickler blocking capacitors in the parallel-fed circuit will cause the shorting of bias or supply potentials and stop oscillation; however, at the low voltages used such failure is not very likely. Shorted tickler or tank inductor turns or poorly soldered connections may produce sufficient shunting (or high resistance) to stop feedback, although the tank inductor change would probably be indicated by frequency change rather than loss of oscillation. A short in the tuning capacitor can cause loss of oscillation, and it may be detected by a continuity check unless the tank coil is disconnected.

Reduced or Unstable Output. Instability should be resolved into one of two types-frequency or amplitude. If temperature variations are the cause of frequency instability, the trouble is most likely in the biasing circuit or the emitter swamping circuit. Opening of the bias voltage divider or shorting of one of its resistors will provide less stability, but such a condition is easily found by checking for proper bias with a high-resistance voltmeter, preferably of the electronic type. It is important, in the case of the electronic voltmeter, to make certain that its chassis does not have an above-ground voltage which could be accidentally applied to the transistor under test. Frequency instability can also result from poor connections or changes of L and C values. Mechanical, electrical, and thermal considerations affecting the tank circuit

should be considered. Lack of regulated supply voltage for bias and operation is important. In. general, the percentage of regulation in the supply voltage must be better for transistor oscillators than for vacuum tube oscillators. If external to the equipment, power supply regulation effects can sometimes be easily corrected by appropriate use of Zener diodes at the points affected.

Instability in the amplitude can be traced in most cases to variations in the supply voltage or to component failure in limiting diodes placed in the circuit for the sole purposes of maintaining amplitude stability.

While reduced output can result from loss of gain in the transistor, this condition is not as common as it is with electron tubes; therefore, it is more logical to investigate supply and bias voltages first before changing transistors. Excessive bias, rather than lack of bias, is more likely to reduce output.

Incorrect Output Frequency. Normally, a small change in output frequency can be compensated for by realigning or adjusting the variable component of the LC resonant tank circuit, assuming that all corm ponent parts of the circuit are shown to be satisfactory. Changes in distributed capacitance or reflected load reactance will also affect the frequency of operation. Additional capacitance will lower the frequency and less capacitance will increase the frequency; corresponding changes in inductance will produce the same effect. A change in transistor parameters will also affect the frequency; for example, an increase in the collector voltage will reduce the collector-base capacitance, while an increase in the emitter current will increase the collector-base capacitance. Power supply regulation effects can, therefore, be suspected when temporary frequency changes occur. Comparison of actual indications with those of the operational standard will generally indicate the area at fault, It may normally be assumed that major frequency changes will involve the transistor elements and components associated with the tank circuit, since they constitute the major frequencydetermining portion of the circuit.

#### HARTLEY OSCILLATOR (ELECTRON TUBE)

#### Application.

The Hartley oscillator is used to produce a sine wave output of constant amplitude and fairly constant frequency within the r-f (and sometimes audio) range. The circuit is generally used as a local oscillator in receivers, as a signal source in signal generators and as a variable-frequency oscillator over the medium and high-frequency ranges.

#### Characteristics.

Uses an L-C parallel-tuned circuit to establish frequency of oscillation, with the inductance connected as an auto-transformer between grid, cathode, and plate to provide the feedback needed for oscillation.

Operates Class C with automatic self-bias for ordinary, or power, operation and Class A when output waveform linearity is important.

Frequency stability is only fair, but better than that of the Armstrong oscillator.

#### Circuit Analysis.

General. A sine-wave output may be obtained from an oscillator utilizing a tuned L-C circuit. The L-C circuit (commonly called a tank circuit) determines the frequency at which oscillation will take place. At any particular instant of time, the opposite ends of a tuned inductance are at different polarities, or 180 degrees out of phase. Likewise, the grid and plate of a triode are 180 degrees out of phase. Therefore, connecting the tuned circuit to the grid and plate of the triode will not affect the polarity of operation. When the cathode is tapped to the inductance of the tuned circuit and cathode current flows, a magnetic field will be produced between the cathode-toplate turns of the inductor. A voltage will be induced in the turns of the inductor connected between the cathode and grid by the cathode current flow, and the polarity of the induced voltage will be in the proper direction to cause an increase of cathode current. Thus, a positive regenerative action is produced by the tapped, tuned-tank circuit connected between

the electron-tube elements. As long as feedback is sufficient to supply the losses in the tuned circuit, continuous, undamped oscillations are produced.

**Circuit Operation. The** basic Hartley oscillator circuit is shown schematically in the following illustration.



#### **Basic Hartley Circuit**

Bias and plate feed arrangements will be discussed later. The tuned (tank) circuit consists of the  $L_g$  and L<sub>p</sub> portions of inductance L, which is parallelconnected with capacitor C. Feedback is usually accomplished by transformer action between L<sub>p</sub> and  $L_{\sigma}$  operating essentially as an autotransformer, with the turns ratio (from about 0.6 to 1) determining the feedback amplitude. (Electrostatic coupling through the tank capacitor can also provide the feedback for oscillation.) Tapping the cathode closer to the plate increases the feedback when the feedback is primarily accomplished by electrostatic coupling through the tank circuit capacitance, with the size of the plate load, L<sub>p</sub>, determining the feedback amplitude. Tapping the cathode closer to the plate reduces the plate load and the feedback amplitude. The manner of feedback is determined by the basic construction of the tank circuit inductance.

**Shunt-Fed Harley.** The circuit for the shunt-fed Hartley oscillator is shown in the following illustration. Grid bias is developed by  $R_g$  and  $C_g$ , connected in series between the tuned circuit and the grid of the triode tube. Shunt plate feed is accomplished by connecting the tuned circuit to the plate through  $C_P$ , which isolates the tank for dc, but connects it to the plate for r-f current flow. Radio-frequency choke RFC offers a high impedance to the rf, which flows through the tank circuit and not through the power supply, but it permits the dc to flow to the plate.



#### **Shunt-Fed Hartley Circuit**

The manner in which oscillations occur and the automatic amplitude regulation by grid-leak bias are identical for both the Hartley and the Armstrong oscillators. Refer to the previous discussion of the L-C tickler coil oscillator for an explanation of this action, and assume that the  $L_p$  portion of inductor L is the tickler coil.

The use of a high-C tank circuit, consisting of C and L comected between the grid and plate of the electron tube, effectively swamps the tube electrode capacitances and produces better frequency stability. The operating frequency is determined by the values of L and C at resonance

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

where L is equal to  $(L_g + L_p + 2M)$ .

Inductive coupling to the load through  $L_1$  at the grouped end of the tank is usually used, but it does not preclude the use of capacitive coupling to the tank circuit where desired.

**Series-Fed Hartley.** The shunt-fed circuit may be easily modified to a commonly used series plate feed arrangement, by moving the ground connection from the cathode to the bottom end of  $L_p$ , and connecting the cathode to the top end of  $L_p$ . Thus plate current

will flow directly through  $L_p$ . Plate capacitor  $C_p$ , in conjunction with radio-frequency choke RFC, then serves only to bypass the rf around the plate voltage supply. The operation of the circuit is otherwise identical to that of the shunt-fed circuit previously described.

Detailed **Analysis. The** analysis of the Hartley oscillator is similar to that of the tuned-plate Armstrong oscillator previously discussed. The following equivalent circuit is labelled exactly as in the previous example. Since the tank coil is now tapped, the total tank inductance, L, is  $L_p + L_g + 2M$ . Resistors R and  $R_1$  are equal to the r-f resistance of  $L_p$  and  $L_g$ , respectively.



Hartley Equivalent Circuit

Analysis of the Hartley circuit shows that the angular frequency is:

$$\omega = \omega_{o} \sqrt{\frac{R + r_{p}}{r_{p} + R(\mu + 1)}}$$
(1)  
where  $\omega_{o} = \sqrt{\frac{1}{L_{T}C}}$ 

As in the case of the tuned-plate oscillator, when no power is taken from the circuit, the frequency is practically given by:

$$f = \frac{1}{277 \sqrt{L_T C}}$$
(2)

## ORIGINAL

where  $\mathbf{L_T} = \mathbf{L_p} + 2\mathbf{M}$ , or the resonant frequency of the tank circuit. Thus while the oscillation frequency is slightly lower than the tank frequency, if a high  $\mathbf{r_p}$  and a small R are used, the tank will govern the frequency.

The criteria for oscillation is that:

$$g_{m}^{*}(\frac{\mu(R + RI) CL_{T}}{(L_{p} + M)}(\mu(L_{g} + M))$$
 (3)

Examination of equation (3) indicates that even with M at zero the equation will be satisfied; therefore, oscillation can occur even when there is no inductive coupling between the plate and grid circuits, the feedback being capacitively coupled through C. As might be suspected, since the criterion for oscillation is not critical, the Hartley circuit oscillates easily.

**Vector Diagram. The** relationships between the currents and voltages in the circuit are shown in the following vector diagram. Refer to the equivalent circuit drawing for easier understanding of the development of the vector diagram.



Hartley Vector Diagram

The voltage  $-\mu e_g$  is used as a reference vector, and  $e_g$  is 180° out of phase. It was pointed out in the mathematical analysis that the Hartley circuit operates slightl<sub>y</sub> below tank resonance;. therefore, the tank circuit will appear resistive and inductive, causin<sub>g</sub> i<sub>p</sub> to lag  $-\mu e_g$  by a small angle, and  $e_p$ , the voltage across the tank, to lead by a small angle. The current  $i_{LP}$  will lage  $e_p$  by some angle less than 90° dependent on the Q of that branch. The current  $i_c$  will lead

 $\mathbf{e_p}$  by some angle less than 90° since that branch is largely capacitive. The voltage induced in the grid coil,  $-j\omega Mi_{LP}$ , lags  $i_{LP}$  by 900 as indicated by its -j coefficient, while the positive component  $(+j\omega i_c L_g)$ , will lead  $\mathbf{i_c}$  by 90°. Grid voltage  $\mathbf{e_g}$  is the vector sum of the voltages developed across the grid coil Lg. Note that with higher values of circuit Q the voltages developed across the grid coil will more closely approach in-phase quantities, and the angle between  $\mathbf{i_p}$  and  $\mathbf{e_p}$ will also diminish, thereby improving oscillator stability.

#### Failure Analysis.

No Output. If the circuit is in a non-oscillating condition, negative grid bias cannot be developed; as a result, the applied plate voltage may be below normal because of the additional current drain unless the power supply is well regulated. For this condition, the plate current will be much higher than normal. Excessive circuit losses in the resonant tank circuit will prevent sustained oscillations. Reduced tube gain (if sufficient) will also affect oscillation. Changes in value of the grid-leak bias components, Cg and R<sub>e</sub>, will directly affect the operating bias, and hence the class of operation and overall gain of the tube. Such changes, if sufficient, may cause a loss of oscillation. Too htgh a value of grid leak resistance may cause intermittent operation or "motor-boating". Shorted turns of the oscillator coil (s), in addition to affecting output amplitude and frequency, may cause loss of oscillation because of loading effects. A leaky plate capacitor  $C_p$  may also load the oscillator sufficiently to stop operation. In the shuntfed circuit, a defective radio-frequency choke RFC or coupling capacitor C<sub>c</sub> may stop oscillation since the oscillator is dependent on these components for development and application of feed-back voltages.

**Reduced or Unstable Output.** A relative indication of oscillator output is provided by the amount of bias voltage developed across  $R_g$ . Variation from the manufacturer's rated value is indicative of abnormal operation.

A reduction in applied plate voltage will cause a reduced output. Therefore, an unregulated voltage source will produce output amplitude variations and probably frequency changes or instability. Losses in feedback, due to shorted turns or poor soldered connections, can cause reduced output or unstable operation. A leaky plate capacitor,  $C_{\rm P}$ , may cause reduced or unstable output by loading the oscillator or by

reducing plate voltage by adding to the normal current flow through a series resistance. Care should be used in selecting a replacement for a defective r-f choke, since an improper replacement choke may cause unwanted oscillations by resonating with distributed circuit capacitance or with the distributed capacitances of its own windings. Similar care should be exercised in replacing a defective tube in those oscillators operating in the higher frequency ranges where interelectrode capacitances may consitute a considerable portion of the tuned circuits. Variations of this physical capacitance from one tube to another may, in addition to affecting output frequency, cause the oscillator to shift from one mode of operation to another as the oscillator is tuned through its frequency range. For example, a Hartley oscillator could shift to Colpitts operation under the right conditions. This shifting may cause frequency jumps and/or dead spots in the tuning range of the oscillator. At the higher frequencies it is good practice to try more than one replacement tube if the first substitution does not achieve the desired results in frequency of operation and stability. Realignment of circuit components to compensate for a tube substitution should be avoided wherever possible.

Incorrect Output Frequency. Normally, a small change in output frequency can be compensated for by realigning or adjusting the variable component of the L-C resonant tank circuit, assuming that all component parts of the circuit are known to be satisfactory. Changes in distributed circuit capacitance or reflected load reactance will affect the frequency to some extent. Thus, an increase in capacitance will lower the frequency, and a decrease in capacitance will increase the frequency. Therefore, care must be used in the removal and replacement of parts in order not to disturb the distributed capacitance of the circuit which is inherent in the placement of physical parts and the wiring of the circuits. Large changes in ambient temperature may affect the operating frequency of the oscillator. Such changes could come about through failure of an oscillator oven, changes in filament supply voltage, etc. The effects of tube substitution on oscillator frequency were discussed above.

## HARTLEY OSCILLATOR (SEMICONDUCTOR)

## Application.

Same application as electron tube version.

## Characteristics.

Same characteristics as electron tube version, except inductance is connected as an autotransformer between emitter, collector, and base to provide the feedback needed for oscillations.

#### Circuit Analysis.

General. A sine-wave output may be obtained from an oscillator utilizing a tuned L-C circuit, especially when the transistor is operating over the linear portion of its transfer characteristic curve. The L-C circuit (commonly called a tank circuit) determines the frequency of oscillation. By using a tapped inductor for the tank inductance, a portion of the tank voltage can be fed back to provide positive feedback and sustain oscillation. The tapped inductor tank circuit may be used as either an autotransformer or a phase shifter, depending on the type of feedback needed for the specific circuit configuration. Unlike the Armstrong oscillator where feedback can be shifted in phase 180° by reversing the tickler coil, the Hartley oscillator will operate only in a commonemitter arrangement since the feedback is always shifted in phase 180°.

**Circuit Operation.** The basic transistor configuration of the Hartley oscillator circuit is shown in the following illustration. Bias and collector feed arrangements are not shown, but will be discussed later. It is assumed that forward bias is initially applied to the emitter-base junction and that reverse bias is applied to the collector junction. This discussion concerns junction transistors only; however, point-contact transistors operate in a somewhat similar manner.



**Basic Hartley Configuration** 

The common+ **mitter** circuit is similar to an electron tube oscillator in that it requires a 180-degree phase shift from collector to base to produce positive (regenerative) feedback. Grounding the emitter tap (see following illustration for grounding points) **pro**duces the effect of inverting the windings and thus provides the desired 180-degree Phase shift. The resonant frequency is determined by the tuning of the tank capacitor, C, and is given by the formula:

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2 + {}_2M)C}}$$

The figure shows three different arrangements of the common-emitter configuration for grounding the transistor elements. These circuits provide a convenient method for grounding the rotor of the tuning capacitor to eliminate hand-capacitance tuning effects and to obtain proper feedback phasing. Note that the three configurations in the illustration are all *common-emitter* arrangements and that the only difference from the basic schematic is the grounding point. In some texts, these configurations are referred to as *common base, common emitter*, and *common collector*, respectively. In all three grounding arrangements of the figure, the feedback is fed from collector to base, and the emitter is the common element.



C E Hartley Oscillator Grounding Points

The discussion under the Armstrong circuit concerning the relative merits of the various configurations and the transistor action are applicable to this oscillator. Operation of the L-C circuit is similar to that of the tickler coil electron tube oscillator circuit discussed at the beginning of this Section. In fact, the operation of the Hartley circuit can be considered

exactly the same as that of the Armstrong circuit, with the tickler coil being an integral portion of the tuned tank circuit. The frequency stability of the Hartley oscillator is slightly better than that of the Armstrong oscillator because the tank tuning capacitor tunes the entire coil and feedback loop, and a high C-to-L ratio provides effective capacitance swamping.

**Shunt-Fed Hartley.** The shunt-fed Hartley oscillator using the common-emitter configuration is shown in the following figure. One voltage supply is used, with fixed base bias being supplied by voltagedividing resistors **R1** and  $R_B$  (see the introduction to the Amplifier Section of this handbook for an explanation of biasing). Emitter swamping resistor  $R_E$ , bypassed by Cl, is used for temperature stabilization.



Shunt-Fed Hartley CE Oscillator

The collector is shunt fed through radio-frequency choke RFC, with C3 serving as the dc blocking and r-f coupling capacitor to keep the tank coil from shorting the collector. Similarly, C2 serves as the base blocking and coupling capacitor to prevent shorting of the base to ground through the tank inductor.

When the shunt-fed circuit is energized, the initial bias is determined by RI and  $R_{\rm B}$ , and oscillation is built up by feedback supplied from the collector to the base through sections  $L_{\rm e}$  and  $L_{\rm B}$  of the tank inductor. Note that an ac path exists from the emitter through the  $L_{\rm c}$  portion of the tank and coupling capacitor C3 to the collector, and that a similar path exists through  $L_{\rm B}$  and C2 to the base. As oscillation occurs, a degenerative bias is developed across  $R_{\rm e}$ (if Cl is of the correct value) similar to that of the gridleak-capacitor combination used in electron tube oscillators, and this bias places operation somewhere between Class A and Class C depending on the parts values. Usually the values of voltage divider R1 and  $R_{\rm B}$  are chosen to provide Class A bias for easy starting, and the values of  $R_{\rm e}$  and C 1 are chosen to provide Class B or C bias for the desired efficiency of operation, with thermal stabilization. The output may be taken from a capacitor connected to the collector or from an inductor coupled to the tank.

**Series-Fed Hartley.** The series-fed Hartley oscillator is shown in the following illustration. The base circuit is voltage-divider biased and emitter stabilized as in the shunt-fed version. The collector voltage is applied through the tap on the tank inductor, the voltage source being shunted for rf by C3. Operation of the series-fed circuit is identical to that of the shunt-fed circuit discussed previously. Since a dc current flows through a portion of the tank circuit, the Q is lowered and the frequency stability is not as great as that of the shunt-fed circuit.



Series-Fed Hartley CE Oscillator

**Detailed Analysis.** Like the vacuum tube oscillator, the transistor oscillator can be converted to an equivalent circuit and analyzed mathematically to determine the conditions required for oscillation and the frequency of operation, using the h-parameters of the transistor. A typical common-emitter equivalent circuit for the Hartley oscillator is illustrated below. Since the mathematical analysis is complex and beyond the scope of this text, and exact only for low audio frequencies, the interested reader is referred to standard text books for this data.



Hartley Semiconductor Equivalent Circuit

The accompanying vector diagram may be more helpful to a better understanding of circuit operation, since it shows the voltage and current relationships. The common-emitter circuit is illustrated.



The voltage  $e_{gen}$  is used as a reference vector. Since the Hartley circuit operates slightly below resonance, the tank circuit appears resistive and inductive, causing  $i_1$  to lag  $e_{gen}$ , and the voltage across the tank  $E_2$  to lead by a small **angle**. Current  $i_y$  leads  $E_2$  by some angle less than 90 degrees since that branch is largely capacitive. Current  $i_x$  lags  $E_2$  by some angle less than 90 degrees, depending upon the Q of that branch. The voltage induced in the base coil- $j_m Mix_{Lc}$  lags  $i_x$  by **90** degrees as indicated by its—j coefficient, while the positive component  $+_{j\sqrt{i_y}L_b}$  leads  $i_y$  by 90 degrees. The base voltage,  $E_i$ , is the vector sum of the voltages induced in base coil Lb. Note that with higher values of circuit Q the voltages developed across the grid coil more closely approach in-phase quantities, and the angle between  $i_1$  and  $E_2$  also diminishes, thereby improving the oscillator stability.

## Failure Analysis.

No Output. Lack of oscillation may be due to a shorted or open-circuited transistor. Deterioration with age causing lack of gain may result under hightemperature conditions. Unlike vacuum tubes, however, transistors have operated for years without noticeable deterioration under proper operating conditions. Failure of the collector and base blocking capacitors will short-circuit the biasing arrangement through the tank coil and prevent operation. Opencircuit conditions of the biasing resistors may stop oscillation, though it is more likely that reduced output will result rather than no output. Where radiofrequency chokes are used to keep rf out of the supply or bias circuits, failure of these components may shunt the rf to gound through power supply capacitors. A more likely condition is an open circuit in the RFC caused by poorly soldered connections. A shorted condition of the tuning capacitor will stop oscillation, and it cannot be detected by a continuity check unless the tank coil is disconnected. When trouble-shooting with test equipment containing line filter capacitors, care should be exercised to prevent application of excessive voltage to the transistor by using a common ground on both the transistor and test chassis. Use high-impedance meters to avoid placing a dc shunt or return path in the circuit and causing improper current flow or voltage distribution.

Reduced or Unstable Output. Instability should be resolved into one of two types - frequency or amplitude. Frequency instability will most likely result from poor tank circuit connections, poor insulation between turns, or changes in L and C values. Also, changes in the supply voltage will produce changes in frequency because of changes in the operating point and changes in the internal capacitance of the transistor with different applied voltages. Excessive bias will probably cause a reduction in the output and will most likely be produced by an increase in value of the bias resistor or opening of the bias bypass capacitors with the consequent production of degeneration. Temperature changes are usually evidenced by increased current in the collector circuit and can be caused by a shorted emitter swamping resistor.

Incorrect Output Frequency. Normally, a small change in output frequency can be compensated for by realigning or readjusting the variable component of the L-C resonant tank circuit, assuming that all parts of the circuit are known to be satisfactory. A change of transistor parameters will also affect frequency; for example, increased collector voltages will reduce the collector-base capacitance, and increased emitter current will increase the collector-base capacitance, but these effects are not equal and therefore do not compensate each other. Reflected load reactance can cause a change of frequency depending on the tightness of coupling between the oscillator and the load. Changes in distributed circuit capacitance or in the tank inductor will also cause frequency changes. A comparison of operational indications against operational standard values will generally indicate the area at fault. For example, frequency changes that vary with power supply voltage fluctuations indicate that supply regulation is necessary and trouble is not in the equipment. Major frequency changes will involve the transistor elements and components associated with the tank circuit, since they constitute the major frequency-determining portion of the circuit.

## CO LPITTS OSCILLATOR (ELECTRON TUBE)

#### Application.

The Colpitts oscillator is used to produce a sinewave output of constant amplitude and fairly constant frequency within the r-f range. The circuit is generally used as a local oscillator in receivers, as a signal source in signal generators, and as a variablefrequency oscillator over the low- and very-highfrequency ranges, especially where inductive tuning is desired.

#### Characteristics.

Uses an L-C parallel tuned circuit to establish frequency of operation.

Features inductive tuning rather than capacitive. Feedback is obtained through a capacitance-type voltage divider.

Operates Class C where wave form linearity is not important, and Class A where linearity of waveform is important. Frequency stability is good (considered better than that of the Hartley at the lower and medium frequencies).

Oscillates easily at high frequencies, where inductive feedback types have difficulty securing sufficient feedback.

#### Circuit Analysis.

General. When a tuned LC (tank) circuit is connected between the grid and plate of an electron tube, the phasing is of the correct polarity to sustain oscillation. The capacitor of a tuned tank circuit may be a single capacitor, or it can be two seriesconnected capacitors with a total capacitance equivalent to that of the single capacitor. In either case, the frequency of oscillation is the same. The two seriesconnected capacitors will form a capacitance voltage divider across the tank circuit. Tapping the cathode of the tube to this voltage divider provides a convenient electrical (and mechanical) connection, and a means of controlling feedback between the grid, cathode, and plate elements. The ratio of the capacitances used will determine the amount of feedback, and the total capacitance value will determine the resonant frequency for any particular value of tank inductance. Varying the inductance is a convenient method for tuning the tank over a range of frequencies with a fixed amount of feedback. The use of capacitive tuning involves the simultaneous tuning of both capacitors to maintain the proper ratio of feedback. For tuning over a limited range, capacitive tuning is sometimes employed.

**Circuit Operation.** The basic Colpitts oscillator circuit is shown schematically in the following illustration. The tuned tank circuit consists of  $C_g$  and  $C_p$ , in series, and the parallel-connected inductor, L. Feedback is accomplished by the capacitive voltage-divider action of  $C_g$  and  $C_p$  (or by the use of a variable capacitor shunting  $C_g$  and  $C_p$ ). The feedback ration varies as

thus, increasing the value of  $\boldsymbol{C}_{\boldsymbol{g}}$  decreases the feedback.

## **ELECTRONIC CIRCUITS**



**Basic Coipitts Circuit** 



Shunt-Fed Colpitts Oscillator

The capacitive ratios vary with circuit design and frequency, from about a 1:1 ratio to a 1:4 ratio, with the larger capacitor being  $C_{p}$ . For high-frequency use, the capacitance voltage divider may consist of ordy the interelectrode capacitances of the electron tube. The circuit may be arranged for grounded grid, cathode, or plate operation without affecting performance; the grounded-cathode configuration is probably the most frequently used circuit.

For simplicity, biasing and plate-voltage feed methods are not shown in the basic circuit, but are discussed where applicable in the following circuit variations.

**Shunt-Fed Colpitts.** The circuit for the shunt-fed Colpitts oscillator is shown in the following schematic. Grid bias is developed by  $\mathbf{R_g}$  and  $\mathbf{C_g}$  in the shunt grid-leak bias arrangement. Shunt plate feed is also used, with  $\mathbf{C_e}$  serving as the plate blocking and coupling capacitor, and RFC as the r-f isolating choke. The tank circuit consists of inductor L and capacitor C, which are parallel-connected between the grid and plate of the electron tube. Capacitor C consists of two series-connected capacitors,  $\mathbf{C_1}$  and  $\mathbf{C_2}$ , which are external to the tube and form a feedback voltage divider to which the cathode is connected.

The manner in which oscillations occur, as well as the automatic regulation of amplitude by grid-leak bias, is the same as explained in the previous discussion of the L-C tickler coil oscillator, except that feedback is obtained from a capacitive voltage divider instead of an inductive voltage divider. Assume that the tank circuit consists of L and C where C represents  $C_1$  and  $C_2$  in series. The tank circuit then is identical with the tuned grid circuit of the tickler-coil oscillator previously described. Since the tank is connected between the plate and grid of the electron tube, and  $C_1$  and  $C_2$  form a capacitive voltage divider, it is evident that there will be a division of feedback voltage in inverse ratio to their capacitance. For a specific frequency the large capacitor will have the lowest impedance, and the smaller capacitor the highest impedance. For equal capacitors, the voltages across the capacitors will be equal. Thus, with the cathode connected to the common connection of the capacitors, the tank voltage will be divided between cathode-and-grid and cathode-and-plate in accordance with the ratio of  $C_2$  and  $C_1$ . Any voltage change in

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the plate circuit will appear across  $C_1$  and be fed back through  $C_2$  in the correct phase to drive the grid in that direction to increase the initial change. That is, if the plate voltage is increasing, the grid change will cause a further increase, and if decreasing, a further decrease. This is exactly the same result that is achieved by the plate-grid coils of the Armstrong circuit or the tapped inductor of the Hartley circuit, as discussed previously, and sustained oscillations will occur.

Since the tank capacitance is composed of seriesconnected capacitors, each capacitor will be larger than the total capacitance that is effective in tuning the circuit. Since these series capacitors are connected in parallel with the grid-to-cathode and plate-tocathode tube capacitances, they will swamp out the interelectrode capacitance variations and thereby increase the frequency stability. Note, however, that as the capacitance of the feedback capacitors approaches the value of the tube element capacitance, this swamping effect is decreased. Stability therefore, is at a maximum at the lower frequencies. The gridplate capacitance, which is usually larger than the other element capacitance, remains in shunt with the tank inductor and will not be compensated for. If desired, capacitive tuning can be achieved by using a shunt tuning capacitor across L and leaving the feedback capacitors fixed. The advantage of the Colpitts circuit, however, is in the use of large variable inductors and fixed feedback-tank capacitors for operation in the low- and medium-frequency r-f ranges, where the greatest stability is obtained.

For high-frequency use, the Colpitts can be employed as an oscillator controlled mainly by the capacitance between the tube elements, so that inductance alone is needed to achieve oscillation. This arrangement results in higher frequencies of operation than with other L-C circuits, and is exemplified by the series-fed version of the Colpitts known as the ultraudion circuit, which is discussed as a separate circuit later in this section. The output coupling may be either inductive or capacitive, as desired.

**Detailed Analysis.** The equivalent plate circuit for the shunt-fed Colpitts oscillator is shown in the following illustration. Assuming that the RFC has infinite reactance, neglecting the grid capacitor reactance, and assuming that the circuit has an infinite grid leak with no grid current, it can be seen that:

$$ip = i1 + i2$$

$$e_{gk} = \frac{i_2}{j\omega C_2}$$

$$e_{pk} = \frac{i_1}{j\omega C_1} \cdot i_2 (R + j\omega L) + \frac{i_2}{j\omega C_2}$$

$$\mu_{egk} = \overline{r}_p \cdot i_p + \frac{i_1}{j\omega C_1}$$



**Colpitts Equivalent Circuit** 

The analysis of the Colpitts oscillator is similar to that of the Hartley, except that the capacitive reactance of capacitors Cl and C2 is substituted for  $L_p$  and L, and the inductive reactance for C. The angular **frequency** is:

$$\omega = \omega_{0} \sqrt{1 + \frac{R}{r_{p}}} \cdot \left(\frac{C_{2}}{C_{1} + C_{2}}\right)$$

For all practical purposes, the frequency is:

$$f = \frac{1}{2\pi \sqrt{L \frac{e_1 c_2}{C_1 + C_2}}}$$

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The criteria for oscillation is that:

$$\mu = \frac{C_2}{\epsilon_1} + \frac{r_p R(C_1 + C_2)}{L}$$

Capacitors Cl and C2 form a capacitive voltage divider across L, causing the grid excitation voltage to be proportional to

$$\overline{C_1 + C^*}$$

**Vector Diagram.** The relationships between the currents and voltages are shown in the following vector diagram. Refer to the illustration of the equivalent circuit for development of the vector quantities.



**Colpitts Vector Diagram** 

The voltage generator  $-\mu e_g$  is the reference voltage,  $e_g$  being 180° out of phase. It was shown that the Colpitts oscillator operates above the tank frequency. Therefore, the tank circuit appears slightly capacitive, and  $i_p$  leads  $-\mu e_g$  by a small angle while  $e_p$  lags 'Peg. The current  $i_1$  through capacitor Cl will lead  $e_p$  by 90°. Current  $i_2$  through the branch containing L and  $C_2$  is primarily inductive and will lag  $e_p$  by an angle less than 90° determined largely by the Q of L. The voltage  $e_g$ , since it appears across capacitor  $C_2$ , will lag  $i_2$  by 90°, thereby satisfying the conditions for oscillation. It can be seen that with higher values of circuit Q, the phase difference between  $i_p$  and  $e_p$  will be diminished.

#### Failure Analysis.

**No Output.** If the circuit is in a non-oscillating condition, the negative grid bias will be much less

than it is in the oscillating condition, because it will consist of contact-potential bias only, which will allow the tube to operate at approximately zero instead of at cutoff or higher. Thus the plate current will be much higher than normal. Excessive losses present in the resonant tank circuit will prevent sustained oscillations. Reduced tube gain, if sufficient, will also affect oscillation, but will not be as noticeable as in the inductive feedback circuits. Changed values of grid-leak bias components  $R_g$  and  $C_g$  will directly affect the operating bias and change the amplitude of the oscillations; if the change is large, oscillation may even be prevented; if small, the effect may not be noticeable. A defective radio-frequency choke RFC or coupling capacitor C may cause loss of oscillation since the circuit depends on these components for the development and application of the feedback voltage.

Reduced or Unstable Output. A relative indication of oscillator output is provided by the amount of bias voltage developed across  $\mathbf{R}_{\mathbf{g}}$ . Variation from the standard operating value is an indication of abnormal operation. A reduction of applied plate voltage will cause a reduced output. Therefore, an unregulated voltage source will produce output amplitude variations and probably some frequency change or instability. Losses in feedback due to shorted turns, poor soldered connections, or changing values of feedback capacitance can also cause reduced output or unstable operation. Care should be used in selecting a replacement for a defective r-f choke, since an improper replacement may cause unwanted oscillation by resonating with the capacitance of its own windings or with distributed circuit capacitances.

**Incorrect Output Frequency.** Normally, a small change in output frequency can be corrected by adjusting the variable **component** of the L-C resonant tank circuit, provided that all component parts of the circuit are known to be satisfactory. Changes in distributed circuit capacitance or reflected load reactance will affect the frequency of operation to some extent, being most noticeable on the higher-frequency ranges. Changes in stray capacitance which parallels the tank circuit will have a greater effect in changing the frequency than grid-cathode or plate-cathode capacitance changes (provided that they are large enough to overcome the tank swamping effect). Care should be used in replacing a defective tube, particularly in oscillator circuits operating in the higher frequency

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ranges. It is good practice to try more than one replacement tube if the first substitution does not achieve the desired results in frequency of operation and stability. Realignment of circuit components to compensate for a tube substitution should be avoided wherever possible. Large changes in ambient temperature may affect the operating frequency of the oscillator. Such changes could come about through failure of an oscillator oven, changes in filament supply voltage, etc.

## COLPITTS OSCILLATOR (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version.

#### **Circuit Analysis**

General. A sine-wave output may be obtained from a transistor oscillator using a tuned L-C circuit, particularly when the transistor is operating in the linear region of its transfer characteristics. The L-C (tank) circuit determines the frequency of oscillation. The tank circuit consists of two series-connected capacitors in parallel with the inductor. The two series capacitors will act as a capacitance voltage divider across the inductor (in addition to tuning the coil to resonance) with the larger voltage appearing across the smaller capacitor. The capacitance feedback voltage divider may be connected so as to provide either an in-phase voltage or an out-of-phase voltage, to suit the various transistor configurations used. The reactance ratio of the two series capacitors is usually chosen to match the input-output resistances of the transistor used. Mathematical analysis predicts a larger ratio between them than is employed in electron tube practice. The large ratio between capacitor values makes it practical to employ fixed capacitors and tune the inductance over the desired frequency range. The use of capacitance (separate or ganged) tuning over small ranges is occasionally encountered. The frequency of operation is the same as the resonant frequency of the tank circuit, which is given by:

$$f = \frac{1}{2 \pi \sqrt{L \frac{c_1 C_2}{C_1 + C_2}}}$$

**Circuit Operation.** The basic configuration of the Colpitts transistor oscillator is shown in the figure below. For simplicity, bias and collector feed arrangements are not shown, but are discussed later. It is assumed that forward bias is initially applied to the emitter-base junction and that reverse bias is applied to the collector-base junction. Only junction transistors are considered since point-contact transistors operate somewhat differently.



**Basic Colpetts CE Configuration** 

Since in the common-emitter circuit the base and collector elements are out-of-phase, it is necessary to provide a 180-degree phase shift to obtain the positive (regenerative) feedback needed to sustain oscillation. This phase shift is achieved by grounding the common capacitor connection, to make the instantaneous polarity of the capacitor supplying the feedback to the emitter opposite to that of the collector. The discussions of transistor action and the relative merits of the various configurations of L-C oscillators made previously are also generally applicable to this oscillator. The frequency stability is better than that of the Hartley oscillator and the Armstrong oscillator, because the lumped tank capacitors effectively swamp out any slight capacitance changes that occur between the emitter and collector and between the emitter and base of the transistor.

The following simplified schematics of grounding points show three different arrangements of the common-emitter configuration for grounding the transistor elements. These circuits provide a convenient method of grounding the tuning-capacitor rotor to eliminate hand-capacitance tuning effects and to achieve the proper phasing for the feedback. Note that the three gounding point configurations are all *common-emitter* arrangements and that the only difference from the basic oscillator is the grounding - point. In some texts these configurations are referred to as *common base, common emitter*, and *common collector*, respectively.



**CE Colpitts Oscillator Grounding Points** 

**Shunt-Fed Colpitts.** The shunt-fed Colpitts oscillator arranged in the common-emitter transistor configuration is shown schematically in the accompanying illustration. One voltage supply is used, with fixed bias being supplied by voltage-dividing resistors R1 and  $R_{\rm B}$  (see the introduction to the Amplifier Section of this handbook for an explanation of biasing). Emitter swamping resistor  $R_{\rm E}$ , bypassed by Cl, is used for temperature stabilization.



Shunt-Fed Colpitts GE Osallator

The collector is shunt-fed through radio-frequency choke RFC to keep the rf out of the supply circuit, with capacitor C2 acting as a coupling capacitor for the tank circuit. Capacitor C2 also serves as a blocking capacitor, preventing the dc supply from entering the tank circuit and shunting (actually shorting) R1 through the tank inductance.

When the circuit is energized, the initial bias is determined by R1 and R<sub>B</sub>, and oscillation is built up by feedback from the tank circuit through divider capacitor C4. Since the divider is grounded at the common connection, opposite polarities exist across capacitors C3 and C4 in respect to ground, with the voltages across these capacitors being determined by the capacitive reactance ratio. Thus a voltage that is out-of-phase with the collector is applied between the emitter and base to supply a positive feedback and sustain oscillation. The combination of  $\mathbf{R}_{\mathbf{F}}$  and Cl provides an emitter swamping resistor for thermal stabilization, with sufficient capacitance as a bypass to permit degenerative voltage buildup to occur and bias the transistor into the Class B or C operating region after a few initial oscillations. The values of R1 and R<sub>n</sub> are usually chosen to provide Class A bias for easy starting. The amplitude of oscillation is essentially regulated by driving the transistor to saturation on one portion of the cycle and to cutoff on the other portion. Although such action normally would cause abrupt changes and distort the waveform, the tank circuit effectively smoothes out the pulsations in Class C operation to provide oscillations that are essentially sine waves. In the linear Class A region, the circuit provides satisfactory sine-wave output for test equipment use. The oscillator output is normally taken inductively by a coil coupled to the tank inductor, although a capacitive tap may be used if necessary.

**Detailed Analysis.** A typical common-emitter equivalent circuit for the Colpitts oscillator is shown in the following illustration. As in the Hartley circuit, the mathematical analysis of the equivalent circuit is too involved for this text, but can be found in standard texts. With both the Hartley and C.olpitts equivalent circuits it is possible, with slight modifications, to represent most of the other oscillator circuits now in use. Thus, the interested reader will find these two circuits most useful.

## OSCILLATORS



**Colpitts Semiconductor Equivalent Circuit** 

One interesting fact develops from the Colpitts analysis; that is, the starting conditions are found to be:

$$\frac{h_{fe}}{\Delta_{he}} = \frac{C_1}{C_2}$$

Where  $Ah_e = h_{ie} hoe -h_{re} h_{fe}$ .

Thus, when  $h_{fe}$  is large and  $Ah_e$  is small, capacitors  $C_1$  and  $C_2$  will have large differences of values (from 10 to 100 times), which is not the case with the electron tube counterpart.

The accompanying vector diagram shows the current and voltage relationships for the Colpitts oscillator equivalent circuit above.



**Colpitts Vector Diagram** 

Note that the Colpitts is exactly the inverse of the  $\checkmark$ Hartley. The reference vector is  $e_{gen}$ , with the induced base voltage, El, directed 180 degrees out of phase. Since the Colpitts oscillator operates above the tank frequency, the tank circuit appears slightly capacitive. Thus i leads egen by a small angle, while  $E_2$  lags. Current  $i_x$  through capacitor  $C_2$  leads  $E_2$  by 90 degrees. Current  $i_v$  through the branch containing the tank inductance and C<sub>1</sub> is primarily inductive and lags E, by an angle less than 90 degrees depending largely upon the Q of the tank inductance. Since the induced base voltage,  $E_{i}$ , appears across capacitor  $C_{1}$ , it lags iv by 90 degrees, thereby satisfying the condi-tions for oscillation. It can be seen that with higher values of circuit Q the phase difference between i and E<sub>2</sub> will diminish.

#### Failure Analysis.

**No Output.** Although oscillation may fail because of a shorted or open-circuited transistor, deterioration with age similar to the decrease of emission in electron tubes does not normally occur. Hightemperature operation may cause premature failure or drop-off in performance of the transistor; however, this can normally be obviated by proper ventilation of the equipment. Reflected reactance from heavy loading due to tight coupling may occur and prevent oscillation, but it should not occur with proper design. Failure of collector blocking capacitor C2 will place a dc short circuit across the collector and base of transistor Q1 through the tank inductance and stop oscillation; it may also ruin the emitter-base junction. Changes in value of the bias resistors will probably reduce the output rather than prevent oscillation completely. Shorting of either of the tuning capacitors will prevent oscillation. In making continuity checks of these tuning capacitors with an ohmmeter, it is important to connect the ohmmeter with the correct polarity because, since the emitterbase junction is in parallel, use of the incorrect polarity would apply a forward bias and possibly damage the transistor.

**Reduced or Unstable Output.** As in the oscillators discussed previously, it is important to determine whether the instability is associated with frequency or amplitude. If amplitude instability is caused by temperature effects, the bias divider and emitter stabilizing resistors are probably at fault. Reduced output will most likely be due to excessive biasing caused

by changes in value of the bias resistors, or to excessive degeneration caused by an open capacitor (or a reduced value of capacitance) in the emitter bypass circuit. A leaky collector coupling capacitor will cause a change in bias by reflecting, through the tank inductarrce, a parallel resistance between the base and collector elements of the transistor. Frequency instability will indicate that the tank circuit or supply voltage is at fault. Although this circuit provides capacitance swamping of the elements to minimize transistor capacitance changes with supply voltage changes, it should be noted that a varying supply voltage also changes the transistor operating point and may therefore affect the frequency to some extent. As in the other oscillators, poor mechanical connections and shorted turns or deteriorated insulation in the tank circuit may cause unstable operation.

**Incorrect Output Frequency.** As in the other oscillators discussed previously, small changes in frequency can be corected by adjusting the tuning capacitor, assuming that all parts are in good condition. Variations of frequency with supply voltage changes indicate the need for external supply regulation. Major frequency changes will most likely indicate trouble in the tank circuit since it is the primary frequency-determining circuit. Although a change in transistor parameters may change the frequency to some extent, a major parameter change will most likely result in reduced output or unstable operation. Too tight coupling of the load is indicated if the frequency changes noticeably with changes in loading (a slight change is normal).

## CLAPP OSCILLATOR (ELECTRON TUBE)

## Application.

The Clapp oscillator is used to produce a sine-wave output of constant amplitude and fairly constant frequency within the r-f range. The circuit is used as a beat frequency oscillator in receivers, as a master oscillator in transmitters, and generally as a variablefrequency oscillator over the high- and very-high frequency ranges. It is also employed as a crystal controlled oscillator in frequency meters and in signal generators.

#### Characteristics.

Uses a separate series tuned L-C circuit to determine the frequency of oscillation, with a capacitance voltage divider form of feedback to control oscillation.

Operates as Class B or C with automatic self-bias for ordinary or power operation, and as Class A where output waveform linearity is important.

Frequency stability is good. The circuit is considered to have better stability than the Colpitts circuit.

## Circuit Analysis.

**General.** The Clapp circuit is considered to be a variation of the Colpitts circuit discussed previously. It uses the stabilizing effect of a series tuned tank circuit, coupled loosely to the tube feedback loop, to provide better frequency stability. It incorporates capacitive tuning which require the use of only one tuning capacitor. It also offers a convenient method of tuning over a small band of frequencies where band-spread or vernier-type tuning is desired.

**Circuit Operation.** The basic Clapp oscillator circuit is shown in the following schematic. The tuned tank circuit consists of series-connected components L and Cl in parallel with the basic capacitance feedback voltage divider,  $C_g$  and  $C_p$ . For simplicity, the biasing and plate feeds are not shown in this basic circuit, but are discussed as necessary in the following circuit discussion.



**Basic Clapp Circuit** 

The capacitance ratio for the voltage divider which provides the basic feedback (as in the Colpitts circuit) may vary with the circuit design and the frequency. Usually it is 1:1 with Cl being smaller (about one-tenth  $C_g$  for high-frequency operation).

The circuit may be arranged for grounded grid, cathode, or plate operation without affecting performance; the grounded-plate configuration is the most frequently used.

The frequency of operation is dependent upon the values of the three capacitors and inductor as follows:

$$F = \frac{1}{\sqrt{2\pi L C_1}} \qquad \sqrt{1 + \frac{C1}{C_g} + \frac{C1}{C_p}}$$

Thus it is evident that when the **ratios** of  $C_1/C_g$  and  $C_1/C_p$  are very small, the resonant frequency will be primarily determined by the values of L and C<sub>1</sub> alone. This is the condition usually desired.

Since the resonant frequency is primarily determined by L and  $C_1$  when  $C_p$  and  $C_g$  are comparatively large, the Clapp circuit may employ much larger values of capacitance in the feedback voltage divider than can the equivalent Colpitts. The larger values of capacitance much more effectively swamp interelectrode capacitances; it has been estimated that as much as a 400 to 1 reduction of change in capacitance by temperature or tube variations may be obtained.

As in the other L-C circuits, the most stable operation is obtained with a high loaded Q, which is produced for a series resonant circuit by a high L to C (not C to L ratio. Thus, for a given frequency, the tank inductance is larger than that used for the previously discussed circuits. Since it is easier to produce a high-Q coil when the inductance is greater than the usual high-C tank affords, the Clapp oscillator benefits from the 10wK tank. While the capacitance voltage divider consisting of  $\boldsymbol{C}_{\boldsymbol{g}}$  and  $\boldsymbol{C}_{\scriptscriptstyle P}$  does not offer any greater stability in this Clapp circuit than in the Colpitts, the ratio of  $\mathbf{C}_{\mathbf{g}}$  to  $\mathbf{C}_{\mathbf{p}}$  is chosen to afford the greatest possible stability in conjunction with the higher Q offered by the series tuned tank. Tuning capacitor Cl is chosen to have the desired tuning range, with sufficient capacitance to sustain the feedback loop at the higher frequency (feedback increases with decrease of frequency).

Since the basic frequency-determining portion of the Clapp circuit is the tank inductor (Cl merely tunes over the desired range), which is coupled capacitively through Cl to the tube, the Clapp tank is generally considered to be more loosely coupled than the tank circuit of the other oscillator configurations. Thus tank circuit changes are normally minimized. This factor, in combination with the higher circuit Q obtainable, provides the Clapp oscillator with very high stability in the presence of supply voltage variations, the frequency changing only a few parts per million for a supply voltage variation of 15 percent.

Variations of the Clapp oscillator circuit may be encountered. For example, an RFC may be inserted between cathode and ground to keep the cathode at a high impedance above ground, and offer a dc return path to the cathode. Usually this choke is chosen to resonate with its distributed capacitance at the fundamental frequency, and occasionally a trimmer is included to adjust the parallel resonant choke circuit for proper impedance. In special circuit versions, the **cathode** tank may be used for frequency doubling. These circuit variations, however, are not a part of the basic Clapp oscillator circuit design.

**Shunt-Fed Clapp.** The complete schematic for a shunt-fed Clapp oscillator is shown in the accompanying illustration. Series plate feed is never used in this circuit and will not be discussed. Shunt grid-leak bias is used ( $R_{e}$  and C,J, with shunt plate feed. Capacitor  $C_{e}$  is the plate blocking and coupling capacitor, and inductor RFC is the r-f choke. The combination of  $C_{c}$  and RFC provide an r-f bypass to isolate the power supply from r-f. The plate is grounded to r-f, and L and Cl form the tank circuit, which is connected across the feedback divider consisting of C2 and C3. The cathode RFC provides a dc return path to ground for the cathode, and offers a high impedance to r-f to prevent any shunting of divider capacitor C3.



Shunt-Fed Clapp Osallator
Operation of the circuit and automatic regulation of the amplitude by grid bias are the same as described in previous oscillator discussions. Oscillation is caused by feedback through the capacitance voltage divider, C2-C3, as in the Colpitts oscillator, but the ratio of the capacitors is chosen for the best frequency stability. The output coupling is usually inductive, but it may be capacitive.

## Failure Analysis.

No Output. High plate current will be indicative of non-oscillation and consequent loss of operating bias, with the tube operating at essentially zero (contact) bias. Reduced tube gain, if sufficient, will also affect oscillation. Changes in the value of the bias resistor and capacitor will directly affect the operating bias and the amplitude of oscillating - if the changes are large, oscillation may be prevented; if small, the effect may not be noticeable. Shorted turns of oscillator coil, in addition to affecting output amplitude and frequency, may cause loss of oscillation because of loading effects. A defective radio-frequency choke (RFC) or coupling capacitor (Cc) may stop oscillation since the oscillator is dependent on these components for the development and application of feedback voltages.

**Reduced or Unstable Output.** A relative indication of oscillator output is provided by the amount of bias voltage developed across  $\mathbf{R}_{\mathbf{g}}$ . Variation from the standard operating value is an indication of abnormal operation. A reduction of plate voltage will decrease the output amplitude. Therefore, an unregulated voltage source will produce output amplitude variations and possibly some frequency change, although the Clapp circuit is considered to be less affected in this manner than the Colpitts (a change of only a few parts in a million for a 15 per cent plate supply fluctuation is claimed). A partially open plate blocking capacitor will reduce the grid-to-plate coupling and feedback and thus affect the output or oscillation. At the higher frequencies it is possible for weak feedback to occur through the grid-to-plate tube capacitance and sustain oscillation even though the plate blocking capacitor is faulty. A leaky plate capacitor may cause reduced or unstable output by loading the oscillator or by reducing plate voltage by adding to the normal current flow through a series resistance. Care should be exercised in selecting a replacement for a defective r-f choke since an improper replacement choke may cause unwanted oscillation by resonating with distributed circuit capacitances or with the distributed capacitances of its own windings.

**Incorrect Output Frequency.** Changes in distributed circuit capacitance or reflected load reactance will affect the frequency of operation to some extent, although the design of this circuit provides fixed swamping capacitances to eliminate such changes. The largest change will be produced by a change of the tank circuit Q caused by shorted turns or poor soldered connections in the tank circuit. An incorrect output frequency resulting from a change of tube transconductance with age is normally corrected by slight readjustment of the tuning capacitor. Large changes in ambient temperature may affect the operating frequency of the oscillator. Such changes could occur through failure of an oscillator oven, changes in filament supply voltage, etc.

#### CLAPP OSCILLATOR (SEMICONDUCTOR)

# Application.

The Clapp oscillator is used to produce **a** sine-wave output of constant amplitude and frequency within the r-f range. The circuit is generally used as a signal source in signal generators and as a variable-frequency oscillator for general use over the high- and veryhigh-frequency ranges.

#### Characteristics.

Uses a series-resonant L-C circuit to determine the frequency of oscillation.

Feedback is obtained through a capacitance-type voltage divider.

Frequency of operation is relatively independent of transistor parameters.

Operates Class C where wave form linearity is not important, and Class A where a linear waveform is required.

Frequency stability is good (better than that of the Colpitts oscillator).

#### Circuit Analysis.

**General.** The Clapp circuit is considered to be a variation of the Colpitts circuit discussed previously. It uses the stabilizing effect of a series-resonant tuned tank circuit, loosely coupled to the feedback loop, to provide good stability relatively independent of transistor parameters. It also offers capacitive tuning, using only one capacitor, without affecting the feedback ratio.

**Circuit Operation.** The basic transistor configuration of the Clapp oscillator is shown schematically in the accompanying figure. For simplicity bias and collector feed arrangements are not shown, but are discussed later. It is assumed that forward bias is initially applied to the emitter-base junction and that reverse bias is applied to the collector junction. Only junction transistors are considered because point-contact transistors operate somewhat differently. the figure are all common-emitter arrangements and that the only difference from the basic schematic is the grounding point In some texts these configurations are referred to as *common base, common emitter*, and *common collector*, respectively.



**Basic Clapp CE Configuration** 

In the resonant tank circuit, the inductor is tuned by a capaictor which is essentially the sum of series capacitors C 1, C2, and C3. Since the total value of a string of capacitors in series is always less then the value of the smallest capacitor, it can be seen that when Cl and C2 are much larger than C3 the effective tuning capacitance is essentially the capacitance of C3 alone. Thus the series tuned resonant circuit consisting of L and C3 is the basic frequencydetermining element, and the frequency is given by:

$$f = \frac{1}{277 \sqrt{LC_3}}$$

Since the tank circuit is controlled by L and C3, it is clear that the feedback voltage divider consisting of Cl and C2 provides the feedback essentially alone, so that any changes of parts values in the tank circuit have negligible effect on the oscillation amplitude. The tuned tank is designed to have a high Q under loaded conditions (low C for series resonance) similar to the tank circuit of the electron tube counterpart. Thus the Clapp circuit has greater stability than the basic Colpitts oscillator from which it is derived. The following figure shows three different arrangements of the common-emitter transistor configuration for grounding the elements to achieve a particular result. Note that the three grounding point configurations in



**CE Clapp Oscillator Grounding Points** 

**Shunt-Fed Clapp.** The shunt-fed Clapp transistor oscillator is shown in the common-emitter and grounded-emitter configuration in the following schematic. One voltage supply is used, with fixed bias being supplied by resistors RI and  $R_B$  (see Section 3, paragraph 3.4.1, for bias explanation). Emitter swamping resistor  $R_{\rm e}$ , bypassed by C 1, is used for temperature stabilization.



Shunt-Fed Clapp CE Oscillator

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The collector is shunt-fed through radio-frequency choke RFC to keep r-f out of the power supply and avoid power supply shunting effects. Note that series feed cannot be used with the Clapp circuit because tuning capacitor C is in series with tank inductance. Thus a blocking capacitor in either the base or the collector lead is not required for this circuit. When the circuit is energized, Class A bias is supplied for starting by the bias voltage divider consisting of R1 and R<sub>B</sub>, and feedback to the base is applied through feedback divider capacitor C3. Grounding the common connection between the feedback divider capacitors provides the 180-degree phase reversal necessary to provide positive feedback from collector to base. The emitter resistor and capacitor combination acts in the same manner as an electron-tube grid-lead to provide essentially Class C bias after a few oscillations. R<sub>E</sub> aiso acts as a dc thermal stabilizer for collector-current temperature variations. In a properly designed circuit, the proper feedback voltage divider capacitor ratio for stable feedback with the transistor used may be selected, independently of tank circuit design considerations, to provide oscillation over the desired range of operation. The output may be taken capacitively or by inductance coupling to the tuned tank circuit. With loose inductive coupling, the output obtained is very stable and relatively free of the detuning effects of loading, since the tank circuit is loosely coupled to the feedback loop and relatively independent of any change in transistor parameters.

#### Failure Analysis.

**No Output.** Since no blocking capacitors are employed and since the tank circuit is essentially unaffected by changes in transistor parameters, lack of output is usually limited to lack of feedback or improper bias voltages. An open or shorted transistor or an open or shorted feedback capacitor will stop oscillation. A shorted tuning capacitor C will also stop oscillator because it will permit the collector voltage on tank "coil L to be shorted to the base. Poorly soldered connections may produce circuit losses sufficient to prevent oscillation, while changes in value or open bias resistors will probably reduce rather than stop oscillation completely.

**Reduced or Unstable Output.** Reduced output would most likely indicate a change in bias resistor values or a defective emitter bypass capacitor. An open or paritally open emitter bypass would produce excessive degeneration and perhaps complete cutoff, though the latter is very unlikely, whereas a shorted emitter bypass would probably be indicated by thermal instability. Frequency instability would be directly traceable to the tank circuit components and connections. An unstable output amplitude could be caused by an intermittent open or short in the bias circuitry or by a poor connection to the transistor or supply voltage. Lack of supply voltage regulation would normally be indicated by amplitude changes rather than by frequency changes.

**Incorrect Output Frequency.** Changes in distributed circuit capacitance or reflected load reactance will affect the frequency of operation to some extent, but can normally be corrected by resetting or adjusting the tuning capacitor. Large frequency changes will be produced by changes of tank circuit inductance caused by shorted turns or poorly soldered connections. At first glance it might appear that a shorted tuning capacitor would cause the frequency of oscillation to be determined by the inductance of the tank circuit alone (plus some distributed capacitance); however, for this condition oscillation could not occur because the shorted capacitor would short the collector voltage through the tank coil L to the base.

# TUNED-PLATE TUNED-GRID OSCILLATOR

#### Application.

**The** tuned-plate tuned-grid (TPTG) oscillator is used to produce a sine-wave output of constant amplitude and fairly constant frequency within the r-f range. This circuit is generally used as a variable frequency oscillator over the high- and very-highfrequency r-f ranges. It is not often encountered in Navy electronic equipment.

#### Characteristics.

Contains two parallel-tuned L-C circuits-one in the grid circuit and the other in the plate circuit of the electron tube-and uses the internal grid-plate tube capacitance for feedback.

Operates as Class C with automatic self-bias for ordinary, or power, operation and is seldom used for linear waveform applications.

Frequency stability is good when properly adjusted.

# Circuit Analysis.

General. When a tuned L-C tank circuit is connected between the grid and cathode of an electron tube and a similar tank circuit is connected between the plate and cathode of the tube with coupling existing between them, sustained oscillation will occur when these tuned circuits are resonated to the same frequency. The amplitude of the oscillation is determined by the amount of feedback from plate to grid, and is also affected by the tuning of the two circuits. To provide the proper phase to sustain oscillation, both the grid tank and the plate tank are tuned to a slightly higher frequency than the resonant frequency at which operation is desired. At the operating frequency both tanks then offer an inductive reactance, and the phase shift through the grid-plate tube capacitance is of the proper polarity to sustain oscillation. The condition for proper phasing is that the inductive reactance of the grid tank circuit be less than the capacitive reactance of the grid-plate interelectrode capacitance at the operating frequency. To sustain oscillation, it is only necessary to supply the losses in the grid circuit, which because of the high-Q grid tank are relatively small. Consequently, only a small capacitance is needed to supply sufficient feedback, and the grid-plate interelectrode capacitance of the triode tube is adequate for this purpose. When a pentode is employed in the circuit, it is usually necessary to supply an external capacitor to provide the feedback, because of the low electrode capacitance inherent in the pentode.

**Circuit Operation.** The basic tuned-plate tunedgrid oscillator circuit is shown schematically in the following illustration. The grid tank consists of Cl and Ll, while the plate tank consists of C2 and L2, no mutual inductance existing between L1 and L2. Feedback occurs through the plate-grid capacitance,  $C_{gp}$  (shown in dotted lines), when both tanks are tuned to the same frequency. The feedback amplitude can be controlled by detuning the grid tank with Cl. Thus, differences in interelectrode capacitance between tubes can be accommodated with no adverse effects.





For simplicity, biasing and plate voltage feeds are not shown in the basic circuit, but are discussed when applicable in the following discussion. Since capacitive feedback determines oscillation, this circuit is a better oscillator at the higher frequencies and is not often used in the low or medium-frequency ranges. Although other configurations may be used, this circuit lends itself conveniently to grounded-cathode operation. The grid tank basically controls the excitation and operating stability, and the grid-cathode tube capacitance is in parallel with the tank, being effectively swamped by the tank capacitance. Likewise, the plate tank capacitor effectively swamps the plate-cathode tube capacitance, and the plate tank is primarily used to determine the operating frequency. Once oscillation occurs near the desired frequency, the plate tank is tuned to set this frequency to the desired value, while the grid tank is adjusted for proper excitation and maximum stability.

Upon examination of the shunt-fed tuned-plate tuned-grid oscillator circuit (following illustration), it is evident that shunt grid-leak bias  $(C_s, R_g)$  and shunt plate feed are used, with  $C_c$  serving as the plate coupling and blocking capacitor. The radio-frequency choke, RFC, keeps the rf out of the plate supply. Ll,

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#### **ELECTRONIC CIRCUITS**

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Cl is the grid tank and L2, C2 is the plate tank. The grounded-cathode connection is shown since it permits grounding the tuning-capacitor rotors to eliminate any body capacitance effects on tuning. Theme of shunt grid-leak bias isolates the grid tank as far as dc is concerned and reduces circulating grid current, although series grid bias could be used as well. Sometimes a series resistor is included between cathode and ground, to provide protective bias in the event of non-oscillation. Both the plate and grid capacitors are sufficiently large so that the tank circuits are affectively coupled to the grid and plate for r-f, yet isolated as far as dc is concerned. Grid-leak bias action and automatic amplitude regulation are the same as described previously in other oscillator discussions. The feedback action takes place as described above, making use of the coupling between the plate and grid tanks provided by the grid-plate tube capacitance. At radio frequencies which require the use of relatively large inductors and when appreciable power is used, it is important for the tanks to be shielded or turned at right angles to each other, to prevent possible inductive coupling effects which would deteriorate circuit performance.

Output is obtained by inductive coupling to the plate tank, although a capacitive connection may be made if desired.



Shunt- Fed Tuned-Plate Tuned-Grid Oscillator

**Detailed Analysis.** The equivalent circuit of the tuned-plate, tuned-grid oscillator is shown in the following illustration.



**Basic TPTG Equivalent Circuit** 

Since the oscillator operates below the resonant frequency of the **tank** circuits, both the plate tank and the grid tank will appear resistive and inductive to the signal source-peg.

The following figure shows the tank circuits replaced by their equivalent values of modified equivalent resistance and inductance at the operating frequency. Notice that this equivalent circuit closely resembles that of the Hartley oscillator which was shown previously.



Modified Tuned-Plate, Tuned-Grid Equivalent Circuit

Therefore, the operation of the TPTG oscillator, at the operating frequency, is basically that of a Hartley

oscillator without the benefit of mutual inductance. However, adjustment of the tuned circuits to meet this condition is rather critical. Note from the equivalent circuits that the basis frequency-determining components are the plate tank and the plate to-grid capacitance of the tube,  $C_{gp}$ . The plate tank, therefore, is tuned to establish the frequency of operation, while the grid tank is tuned to establish the proper phasing and amount of feedback voltage for grid excitation.

**Vector Diagram.** The relationship between the current and voltages in the. circuit is shown by the following vector diagram.



**Tuned-Plate Tuned-Grid Vector Diagram** 

The constant voltage generator output pe, is the reference voltage. It is assumed that there is no inductive coupling between the plate and grid tank circuits and that the frequency of oscillation is slightly lower than the resonant frequency of the tanks. Since the tank circuits are tuned to a higher frequency than the oscillation frequency, they offer an inductive reactance. Also, since the feedback must occur through the grid-plate inter-electrode capacitance, the grid tank must offer a lower inductive reactance than the capacitive reactance of the electrodes (the gridcathode and plate-cathode capacitance is assumed to be a part of the tuned circuits). Therefore, the inductive plate tank causes  $e_p$  to lead  $\mu e_g$  by some angle dependent on the circuit values, and iprp lags. The inductive plate tank current  $i_2$  also lags  $e_p$  somewhat less than 90 degrees. Since the reactance of  $C_{gp}$  is greater than the grid tank reactance,  $i_1$  leads  $e_p^{BP}$  by almost 90 degrees. Voltage  $e_{gk}$  is developed across the inductive grid coil (tank) and, therefore, leads  $i_1$ 

by almost 90 degrees. This voltage is exactly 180 degrees out of phase with  $\mu e_g$ , satisfyin, the requirement for oscillation.

#### Failure Analysis.

No Output. If something happens to either of the tank circuits so as to cause a large enough shift in that tank's resonant frequency, the circuit will not oscillate, and only contact bias will be developed. Plate current, therefore, will be higher than normal and the standard operating value of grid bias will not be obtained. Excessive losses if present in the tank circuit will prevent sustained oscillation. Changes in the values of grid-bias components  $R_g$  and  $C_g$  will affect the operating bias and change the amplitude of oscillation. A large change may prevent oscillation, whereas a small change may not have any noticeable effect. Although loss of tube gain will reduce the amount of feedback, the TPTG circuit is a vigorous oscillator when properly adjusted, so that considerable reduction in tube amplification is necessary to reduce oscillation. Too close coupling of the output circuit to the plate tank will produce the same effect as a lossy tank circuit, and reflected reactance may cause sufficient detuning to prevent oscillation. In the shunt-fed circuit, a defective radio-frequency choke RFC or coupling capacitor C<sub>c</sub> may cause loss of oscillation since the oscillator depends on these components for isolation from the low a-c impedance of the plate supply and for coupling of the a-c signal to the tuned plate tank.

Reduced or Unstable Output. A relative indication of oscillator output is provided by the amount of bias voltage developed across  $R_g$ . Variation from the standard operating value is an indication of abnormal operation. A reduction of applied plate voltage will decrease the output. Therefore, an unregulated voltage source will produce output amplitude variations and probably some frequency change or instability. In this respect, the tuning of the grid tank is important, as is has a great effect on the stability of operation. A leaky coupling capacitor C may cause reduced or unstable output by loading the oscillator or by reducing plate voltage by adding to the normal current flow through a series voltage dropping resistance. Care should be used in selecting a replacement part for a defective r-f choke, since an improper replacement may cause unwanted oscillation by resonating with distributed circuit capacitances or with the distributed capacitances of its own windings.

Similar care should be exercised in replacement of a defective tube since the oscillator depends on interelectrode capacitances as a part of the tuned circuits. Variations of this physical capacitance from one tube to another may be enough to seriously detune the oscillator. It is good practice to try more than one replacement tube if the first substitution does not achieve the desired results in frequency of operation and stability. Realignment of circuit components to compensate for tube substitution should not ordinarily be necessary.

Incorrect Output Frequency. Assuming that all component parts of the circuit are known to be satisfactory, changes in output frequency can be compensated for by realigning or tuning the tank circuits. Detuning effects caused by reflected load reactance will affect the frequency of operation to some extent, being most noticeable on the very-high-frequency ranges. Changes in tank inductance caused by shorted turns, particularly in the grid circuit, will result in a different frequency of operation, if oscillation still occurs. Large changes in ambient temperature, such as may occur through failure of an oscillator oven or changes in filament supply voltage, may affect the operating frequency of the oscillator. Changes in distributed circuit capacitances will also affect the operating frequency. Therefore, care should be used in the removal and replacement of parts, in order not to disturb the distributed capacitance inherent in the physical parts and wiring of the circuit. The effects of tube substitution were discussed above.

# Series-Fed Tuned-Plate Tuned-Grid.

**Series** plate feed is easily accomplished with the tuned-plate tuned-grid circuit by connecting B + and the RFC in place of the ground to L2 (refer to shunt-fed schematic), connecting the plate directly to the top of L2, and bypassing the bottom end of L2 to ground with Cc. Circuit operation and failure analysis are exactly the same as for the shunt-fed circuit with two exceptions: (1) With the series .connection, unwanted low-frequency (or high-frequency) parasitic oscillations caused by resonances of RFC and C<sub>c</sub> or of RFC and C<sub>pk</sub> are eliminated. (2) The effect of dc in the tank circuit must be considered; since the capacitor and inductor must withstand both d-c and r-f voltages, their insulation to ground becomes an important factor.

# EL ECTRON-CO UPLEO OSCILLATOR (ELECTRON TUBE)

### Application.

**The** electron-coupled oscillator is used to produce an r-f output of constant amplitude and extremely constant frequency, usually within the r-f range. The circuit is generally used in any type of electronic equipment where stability is required, and the output waveform need not be a sine wave, as some distortion of waveform is normal.

# Characteristics.

Uses the shielding effect between the plate and screen grid in a tetrode or pentode to isolate the plate load from the oscillator, and employs the electron stream between the screen grid and plate to couple the oscillator output to the plate load.

Operates with practically any circuit configuration of the L-C or R-C type, but is mostly used with L-C circuits.

Frequency stability of circuit is very good-better than that of the previously discussed types of oscillators.

# **Circuit Analysis.**

General. In the triode-type oscillator, variation of the plate supply voltage and reflected load reactance causes slight frequency variations because the plate is involved in the feedback loop. By using the cathode, grid, and screen grid of a tetrode or pentode as the oscillator, the plate is eliminated from the feedback loop. Since the plate current in the tetrode or pentode is relatively independent of plate voltage changes and remains nearly constant for a specific value of screen voltage, variations in the plate load circuit have practically no effect on the other elements. Connecting the screen grid as the plate of the triode oscillator electrostatically shields the plate of the pentode or tetrode, and couples the output of the oscillator to the load through the plate electron stream.

Any of the previously discussed oscillator circuits may be used for the oscillating portion of the electron-coupled oscillator circuit, and the electron tube can be either a tetrode, a pentode, or a beampower tube.

The tetrode is a four-element tube, which uses a screen grid to accelerate the flow of electrons from the cathode to the plate under control of the control grid. As the electrons pass through the screen grid to the more positive plate, some of them impinge on the screen grid and produce a screen-grid current, which amounts to about one tenth of the plate current. Secondary electrons are emitted by the portion of the electron stream striking the screen grid and by the stream striking the plate. Normally, when the plate voltage is higher than the screen-grid voltage, these secondary electrons are attracted to the nearest element, plate or screen, and merely increase their respective currents. When the plate voltage is near or below the screen-grid voltage, space charge forms a virtual cathode between the screen grid and plate and thus nullifies the effect of electron coupling. Therefore, the screen grid is usually supplied from the plate source through a series voltage-dropping resistor, and it is bypassed to ground with a capacitor to provide an electrostatic shield. The beam-power tetrode uses special construction and beamforming plates connected to its cathode to provide the same effect. The pentode utilizes a fifth element (the suppressor grid), usually connected to the cathode internally and 1 ocated between the screen grid and plate, to eliminate secondary-emission effects. In some tubes the suppressor grid connection is brought out externally, and may be connected to ground, screen grid, or plate as desired. In the electron-coupled oscillator, it is always connected to provide an effective electrostatic shield between the screen grid and plate, in order to eliminate coupling of load variations back to the oscillator circuit. When a pentode with an internally comected suppressor is used in the electron-coupled circuit, the cathode is always grounded; otherwise, full electron coupling is not obtained and a less stable circuit results.

The electron-coupled plate load may be another tuned tank circuit, a radio- frequency choke, or a resistor. The tuned plate tank may be operated on the same frequency as the grid tank, or it may be tuned to a harmonic, operating as a frequency multiplier. In test-equipment applications, a choke or a resistor (instead of a tank circuit) is usually used with tight loading to assure maximum frequency stability. A properly designed electron-coupled oscillator provides the stability of a master oscillator-power amplifier circuit combination with ordy one tube, and it has the power output of an equivalent triode operating at the

same plate voltage and current.

When a resistor or choke is used in the output circuit, the waveform is not exactly sinusoidal because the plate current does not vary linearly with the screen-grid current. Although the control grid varies the screen-grid current linearly, and these oscillations effectively modulate the electron stream between the screen grid and plate, not all of the current controlled by the grid reaches the plate. Some of the electrons in the screen-plate region are attracted back to the screen grid, while others are shunted to the cathode by the suppressor electrode. Therefore, at any particular instant when the screen-grid current is being slightly increased, the plate current may or may not be increased by the same amount-in fact, it may actually decrease. Hence, the output waveform, which is the result of plate current flow through the load resistance, will not be exactly like the screen-grid waveform; it will be similar, but distorted. If a plate tank or an L-C filter is employed, the distortion will be corrected and a nearly sinusoidal waveform will result.

Circuit Operation. The schematic of an electroncoupled oscillator using a pentode tube is shown in the following illustration. The oscillator section utilizes the basic Hartley shunt-fed circuit, with a series grid leak as discussed previously in the Hartley oscillator circuit, and with the screen of the pentode acting as the troide plate.



Pentode Electron-Coupled Oscillator

The E.C.O. load is taken from the plate circuit of the pentode. Operation of the oscillator portion is identical to that of the previously discussed Hartley oscillater. In the electron-coupled version, however, plate

voltage is applied to the pentode through RFC2 to keep r-f out of the power supply, and the output is capacitively coupled to the load (usually the next r-f amplifier stage). To insure that the screen of the pentode remains at a lower minimum dc potential than the plate, a dropping resistor, RI, is generally used, but may be omitted in some versions of this circuit. Since the screen is above ground at r-f potential, RFC1 is necessary to block the rf from the power supply. If R1 is a high-vahre resistor of say 5000 ohms or more, RFC1 may be omitted, because the high resistance of RI is comparable to the reactance offered by the r-f choke. Note that the suppressor element is connected to the cathode, which is grounded. If the cathode were above ground, the sup pressor could not be connected to the cathode or it would capacitively couple the oscillator into the plate circuit and destroy the shielding effect of electron coupling. Since in this instance the cathode is grounded, the suppressor performs its normal function of eliminating secondaiy emission and isolating the plate and the screen grid.

The oscillator normally operates Class C, and for each pulse of oscillation a corresponding pulse is produced in the plate circuit through modulation of the electron stream. Thus electron coupling exists between the screen grid and plate. Plate load variations produce plate voltage and current changes, but, since a change of pentode plate voltage has little effect on plate current, these changes have negligible effect on the screen-grid voltage and current. Hence, the stability of the oscillator remains relatively unaffected by load variations. It should be noted that, although the pentode is considered to be unaffected by supply voltage variations, only the tetrode circuit can be **de**signed by selection of proper plate and screen voltages to be completely independent of supply variations. The advantage of the pentode arrangement is that grounded-cathode operation can be used to provide an electrostatic shield between plate and grid or screen, and secondary emission effects need not be considered.

The tetrode version of the electron-coupled oscillator which is particularly applicable to beam-power tubes is the grounded-screen circuit shown in the following illustration.



**Tetrode Electron-Coupled Oscillator** 

In this circuit, the shunt-fed Hartley is used; the operation and components of the circuit are the same as just described for the pentode E.C.O. illustrated in the accompanying figures, with the following exceptions.

Since there is no suppressor element in a tetrode tube, secondary emission effects are encountered. Therefore, RI is needed to keep the plate voltage always higher than the screen-grid voltage, in order to avoid formation of a virtual cathode within the space-charge region between the screen grid and plate. Because the screen is grounded by Cc, an electrostatic shield is provided between the oscillator and output sections. Since the cathode is above ground and cathode current flows through the  $L_p$  portion of the tank, the full current of the tube is utilized to provide feedback through the tank inductor. Actually, this is a series platefed connection. Since the plate current of the tetrode is independent of plate voltage, being controlled by the potentials on the screen and control grids, no undesired coupling results from the flow of cathode current through L<sub>p</sub>. The original derivation of this circuit utilized a variable resistor as R1, and the screen-grid voltage was adjusted for maximum stability. Since a slight increase of screen voltage (caused by supply or load variations) decreases the frequency,

while a similar change of plate voltage increases the frequency, RI can be adjusted for specific screen voltage where a frequency change in one direction will cancel a corresponding change in the other direction and result in freedom from frequency changes due to supply voltage variations.

It should be noted that, if a pentode is used in the tetrode circuit, the suppressor should not be connected to the above-ground cathode, or capacitance coupling will exist between the suppressor and ground and inject an undesired coupling between the oscillator and output sections. Instead, the suppressor grid should be tied to the screen or the plate, making the tube effectively into a tetrode; a pentode with an internally connected suppressor is not usable in this circuit.

A number of electron-coupled-oscillator variations using the oscillators previously discussed are also **illus**trated. These circuits are drawn in their most usually encountered form; namely, with a plate output tank which may be operated either on the fundamental or a harmonic. Circuit operation is the same as discussed for the basic oscillator with the addition of the electron-coupled circuit theory just completed. The tuned-plate tuned-grid version is not shown because it is usually in the form of a crystal-controlled **electron**coupled oscillator, in which the grid tank is replaced by the crystal and the plate tank is the output of the oscillator. This circuit version is discussed later in this section.









# Failure Analysis.

**No Output.** Failure of oscillation would cause no output, and could result from the same effects described in the failure analysis section of the Hartley oscillator. In addition, lack of supply voltage caused by open components or a short from plate to ground would effectively stop output. ActuaMy, in this type of circuit tube emission could drop to the point where there is sufficient current for the oscillator section, but practically none for the plate. Therefore,

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the circuit should be considered as basically a twosection tube, and checked for oscillator output first and then for continuity through the plate circuit. If the plate output circuit is known to be complete with all components in good operating condition, and the oscillator is operating, lack of plate output indicates a faulty tube.

Reduced or Unstable Output. In addition to those causes indicated for the basic oscillator in the Hartley oscillator circuit discussion, the following should be considered: If the basic oscillator is unstable or has a reduced output, then, with all other conditions equal, the plate output will also be unstable or reduced. Thus the oscillator should first be investigated for proper operation. Since the screen voltage determines the amount of plate current drawn by the tube, a reduction of screen voltage would have a more noticeable effect on the output before it dropped below the point where oscillation could be sustained. An increase in resistance of the screen dropping resistor, if used, is a primary cause of reduced output. Where the plate voltage is supplied through a load resistor, it is common for a high resistance to develop, reducing both the plate voltage and the output. This condition can result in instability if the plate voltage becomes lower than the screen voltage. If the output circuit of the plate includes a tuned tank circuit, a normal increase of output is to be expected when the tank is tuned to the same frequency as the oscillator or to a low-order harmonic. Therefore, any effects causing tank detuning will immediately result in a reduced output. When instability is produced by load variations, it can immediately be assumed that the electron coupling is involved; in this case, the circuit should be checked for capacitive coupling between screen and plate or for a change in voltage ratios d"ue to an excessive voltage drop or a short circuit in either the screen or plate. When the screen current increases abnormally, secondary emission effects or a defective (open) plate circuit can be suspected.

Incorrect **Output Frequency**. Since the output frequency is determined basically by the oscillator portion of the tube, any change in frequency with normal output amplitude indications would indicate that a change of oscillator components or voltages is the most probable cause. If the oscillator frequency change is not due to components in the oscillator itself, the electrostatic shielding between the plate and screen sections has probably deteriorated because of open or shorted bypass capacitors, changes in tube voltages, or the presence of stray capacitive coupling from other causes.

# ULTRA-AUDION OSCILLATOR (ELECTRON TUBE)

#### Application.

The ultra-aud ion oscillator is used to produce a sine-wave output of constant amplitude and fairly constant frequency wit hin the r-f range. It is generally used as a variable-frequency osc illator on the very-high and ultra-high-frequency ranges.

#### Characteristics.

Uses a parallel tuned L-C circuit to determine the frequency of oscillation, with a capacitive voltage divider form of feedback to control oscillation.

Operates Class C with automatic self-bias for ordinary operation.

Frequency stability is fair-similar to that of the Colpitts operating at high frequencies.

Oscillates easily at frequencies which are too high for other types of oscillators, or at which they are very unstable.

Has only one tuning control, and requires only two leads for connections between the tank and the tube.

#### Circuit Analysis.

**General.** The ultra-aud ion circuit is essentially a series-fed Colpitts oIC illator with a parallel-tuned tank c ircu it for determining the frequency of operat ion. The previous discussion of the Colpitts osc il lator circuit is generally applicable to the ultra-aud ion oscillator. The following discussion will be 1 **imited** to pointing out the basic differences of operat ion between the two circuits and any special cons iderat ions necessary for highfrequency operation.

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# **Circuit Operation.**

The ultra-aud ion circuit is shown schematically in the following illustration. The tuned tank circuit consits of L and Cl, connected between the plate and grid of the tube. Shunt grid-leak bias is used ( $C_{o}$  and  $R_{g}$ ) because of the series plate feed.



# Ultra-audion Circuit

The radio-frequency choke shown in dotted lines in the cathode circuit is sometimes inserted (open cathode lead at x), to minimize the effects of stray wiring capacitance; it is usually self-resonant at the frequency of operation. Although the frequency is determined by the tank circuit, the feedback is controlled by the ratio of grid-cathode and plate-cathode electrode capacitance plus any stray wiring capacitance. Operation is exactly the same as previously discussed for the Colpitts oscillator circuit. To visualize the circuit operation and component relationships, refer to the equivalent circuits shown in the illustrations. Figure A shows the basic u1 tra-aud ion without the cathode RFC, and figure B shows the arrangement when the cathode choke is used; each circuit will be discussed separately.



Simplified Equivalent of Ultraaudi on Circuit

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Since this oscillator is designed for extremely high-frequency operation, assume that the tank inductor L is merely a single wire loop of small diameter connected between the grid and plate, so that the inductor includes the leads to the tube as part of the tank. For the moment neglect Cl; since the inductor is connected between the plate and grid, it is evident that the grid-plate tube capacitance is in shunt with the inductor and forms a part of the tuned circuit, as shown in A. The grid-cathode and plate-cathode tube capacitances form a voltage divider between grid and plate, with the cathode at ground potential. Likewise, the distributed wiring capacitances  $C_{d1}$  and  $C_{d2}$  are in parallel with the voltage divider and, since the tube-element capacitances are small, they form a major portion of the capacitance in the voltage divider. Referring to the Colpitts theory, it is seen that  $C_{gk}$  and  $C_{pk}$  in series form the capacitance across the tank inductor. The tube-element (interelectrode) capacitance is usually small, with the grid-plate capacitance being larger than either  $C_{gk}$  or C<sub>pk</sub>. Therefore, the grid-plate capacitance acts as a swamping capacitor across the tank, being equal to, and in most instances greater than, the total seties grid-cathode and plate-cathode capacitances. Thus, when C<sub>1</sub> is added across the tank inductor, the tank circuit is relatively independent of the feedback capacitors and is the primary frequency-determining component. Where the stray wiring capacitance is large, it assumes more control over frequency than the tube capacitance does; therefore, disturbing the wiring may cause extreme detuning of the circuit.

To eliminate this stray capacitance effect and allow the tube capacitance alone to control feedback, the arrangement of B is used. In this case the cathode is above ground, as the RFC is chosen to resonate with its self-capacitance somewhere within the tuning range. Wiring and stray capacitances to ground effectively form a balanced capacitive divider across the tank circuit, but have no effect on the feedback circuit. Thus the stray wiring capacitance affects the frequency of operation to some extent, but it does not affect feedback; consequently, the tube that is most effective for the frequency of operation desired can be used.

# Failure Analysis.

No Output. Loss of, or improper, feedback will result in non-oscillation, as evidenced by a lack of grid voltage across grid leak  $R_g$  and by a high plate

current because of operation near zero bias. Since the capacitance to ground of the measuring probe will change the feedback capacitance ratio at the frequencies used, a grid voltage measurement to detect non-oscillation is not as effective as at lower frequencies and in other oscillator circuits. High plate current is usually a more positive indication. At extremely critical frequencies, change of lead dress can produce stray-distributed-capacitance swamping in the unbalanced circuit. Loss of tube gain will also reduce output and, if sufficient, will cause a lack of oscillation. Tank circuit losses are more serious at the very high frequencies because the resistance introduced will prevent operation. Thus poor soldering or shorted turns will have a greater effect than at lower frequencies. Changes in the grid-leak resistance or grid blocking capacitor will also affect operation, and small changes will easily stop oscillation at the higher frequencies. An open or high-resistance connection in the cathode RFC (when used) or the plate RFC will also result in a lack of output.

Reduced or Unstable Output. Low plate voltage or too high a value of grid-leak resistance will reduce the output. Poor soldered connections or high-resistance joints will also reduce the output. Unstable operation will occur if the grid-leak time constant changes because of a change in the component values of  $C_{p}$  or  $\mathbf{R}_{\mathbf{g}}$ . If present in a sufficient amount, stray capacitance which affects the feedback voltage will also produce instability. A reduction of filament emission will affect both the output and stability. Large changes in ambient temperature may affect output, as well as operating frequency. Tube substitutions may be critical, particularly at the higher frequencies, because of minor variations in interelectrode capacitance from one tube to another. More than one replacement tube should be tried if the first substitution does not achieve the desired results in output frequency and stability.

**Incorrect Output Frequency. Any change in** wiring-to-ground capacitance or lead length will affect the frequency. Changes in the tank circuit will have the greatest effect, and changes in the grid-plate capacitance and the grid- or plate-to-ground stray capacitance will have less effect, with the gridcathode and plate-cathode variations having the least effect. Changes in the plate voltage will produce a greater frequency change at the higher frequencies than at the lower frequencies. The effects of tube substitution and ambient temperatures on output frequency were discussed above.

# **R-C PHASE-SHIFT OSCILLATOR (ELECTRON TUBE)**

# Application.

**The** R-C phase-shift oscillator is used to produce a constant-amplitude, constant-frequency, sine-wave output.

# Characteristics.

Utilizes a single-stage amplifier with resistancecapacitance network to provide in-phase feedback.

Output frequency in audio range; usually fixed-frequency, but may be variable for certain applications.

Frequency stability good.

Operated Class A to obtain a sinusoidal output.

# **Circuit Analysis.**

**General.** In the basic circuit shown in the accompanying illustration, a sharp cutoff, pentode-type tube is used as the amplifier tube; however, a triode tube can be employed in a similar circuit. Bias voltage is developed across cathode resistor R4. Cathode bypass capacitor C4, by virtue of its filtering action, keeps the bias voltage relatively constant and places the cathode at signal-ground potential. The sine-wave voltage is developed across plate-load resistor R6; capacitor C6 is the output coupling capacitor. Any variation in plate current will cause a corresponding change in plate volatage. These plate volatage variations will also be present at the grid of the tube, since the plate is coupled to grid through the phase-shift network, ZI.



Figure A-465

#### **R-C Oscillator Circuit**

The operating condition for oscillation is a function of the amount of bias established by the cathode bias resistor, R4. The use of degenerative feedback (cancellation) and regenerative feedback (reinforcement) in the circuit simultaneously for undesired and desired frequencies is made possible by the action of the phase-shift network, Z1. The phase-shifting network is comprised of three separate R-C sections; each section is effectively a series R-C circuit. The three **R-C** sections are designated as Cl, R1; C2, R2; and C3, R3. The discussion given in the following **paragraphs** describes the action of only one series **R-C** circuit, but applies to all three sections.

**Phase-Shift Network.** It is the property of a capacitor that an a-c voltage applied across the capacitor

lags the current through the capacitor by 90 degrees. In a series circuit containing both resistance and capacitance, however, the voltage lags the current by some angle less than 90 degrees. A series resistancecapacitance circuit is shown in the accompanying illustration, together with its vector diagram.



Vactor Analysis of R-C Circuit

The values of capacitive reactance (Xc) and resistance (R), chosen for each section of the phase-shift network, are such as to cause a total impedance (Z). Assuming that this impedance represents the first section of the phase-shift network, it is across this section that plate-voltage variations are applied. The applied voltage is represented in the vector diagram as Ea. The circuit current passes through resistor R and, since this current leads the applied voltage  $\mathbf{E}_{\mathbf{a}}$  by 60 degrees, the voltage drop  $E_R$  across resistor R leads the applied voltage  $E_a by$  60 degrees. The voltage,  $E_R$ , developed across resistor R is applied to the second section and is shifted another 60 degrees in phase, so that the output voltage of the second series R-C section leads  $\mathbf{E}_{\mathbf{a}}$  by 120 degrees. The output voltage of the second R-C section is applied to a third section, and is again shifted an additional 60 degrees to lead the applied voltage  $E_a$  by a total of 180 degrees. The output of the third R-C section is applied to the grid of the tube.

Referring to the vector diagram, it is apparent that, since the capacitive reactance (XC) varies with frequency, the frequencies above or below the frequency for which the circuit is designed will be shifted more or less than 60 degrees by each section of the network, so that the total phase shift contributed by all three sections will be something more or less than exactly 180 degrees. In this **manner**, the circuit is caused to oscillate at only one frequency; that is, the frequency which is shifted exactly 180 degrees by the phase-shift network, Z 1.

By increasing the number of phase-shift sections comprising the network, the losses of the total network can be decreased; this means that the additional sections will each be required to have a lesser degree of phase shift per section so that the over-all phase shift of the network remains at 180 degrees for the desired frequency of oscillation. Assuming that the values of R and C are equal in all sections, networks consisting of four, five, and six sections are designed to produce phase shifts per section of 45, 36, and 30 degrees, respectively.

**Circuit Oparation.** Oscillations are initially started in this circuit by small changes in the B-supply voltage or by random noise. If it were not for the action of the phase-shift network, ZI, the voltage variations fed from the plate back to the grid of the tube would cancel the plate-current variations, since the tube introduces a polarity inversion between the grid and plate signals. For example, if the plate-voltage variation at any instant of time was positive, the positive variation would be present on the grid. This positivegoing grid voltage would then cause the plate current to increase, in turn causing the plate-voltage variation to go negative and, thus, canceling out the original grid-voltage variation.

Assuming that the plate-voltage variations are applied to the grid 180 degrees out-of-phase with respect to the initial grid-signal voltage, maximum degeneration (or cancellation) will occur. However, if the plate-voltage variations fed back to the grid approach zero-degree phase difference, minimum degeneration will occur. Therefore, if the phase difference between the plate-voltage variations and the initial grid-signal voltage is exactly zero (in phase), the plate-voltage variations will reinforce the grid-signal voltage at any instant of time, causing regeneration; furthermore, these variations will be amplified by the tube and reapplied to the grid, amplified again, and so on, until a point of stage equilibrium is reached and no further amplification takes place. The phase-shift network provides the required phase shift of 180 degrees to bring the voltage fed back to the grid in phase with the initial gridsignal voltage and cause regeneration. The circuit then oscillates under these conditions with relatively constant amplitude.

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The phase-shift oscillator is designed primarily for freed-frequency operation; however, the operating frequency can be made variable by using variable resistors or capacitors in the phase-shift network. An increase in the value of resistance or capacitance will decrease the operating frequency; a decrease in the value of resistance or capacitance will increase the operating frequency. In several practical applications of this circuit, three or more fixed R-C sections are employed together with a variable section to provide a limited range of output frequencies which are determined by the setting of a variable capacitor. In this circuit variation, the fixed R-C sections use values of R and C which will provide a phase shift somewhat less than 180 degrees at the operating frequency desired, and the last (variable) R-C section completes the required phase shift to exactly 180 degrees. The operating frequency is then determined by the setting of the variable capacitor.

# Failure Analysis.

**No Output.** Assuming that the applied voltages are correct, the lack of output results from two possible conditions; either the gain of the tube has decreased to a point where gain is insufficient to overcome the losses inherent in the phase-shift network, or one or more sections of the phase-shift network is possibly defective and does not provide proper phase shift of the plate-to-grid feedback signal.

In some cases, the phase-shift network must be replaced as an assembly if found defective. In cases where the phase-shift network is composed of individual resistors and capacitors, the individual components may be checked and replaced if found defective.

**Reduced Output.** Reduced output is generally caused by decreased stage gain; however, a small reduction in gain may cause oscillations to cease before any appreciable decrease in output can be detected.

**Nonsinusoidal Output.** Nonsinusoidal output results when the tube is operating on the nonlinear portion of its characteristic curve. Such operation results from a change in B-supply voltage or bias voltage which causes partial or complete clipping of the output waveform.

**Output Frequency Incorrect.** Since the values of resistance and capacitance that form the phase-shift network determine the operating frequency of the oscillator, any change in component values will be reflected as a change in the frequency of socillation.

# R-C PHASE-SHIFT OSCILLATOR (SEMICONDUCTOR)

## Application.

**The** R-C phase-shift oscillator is used to produce a sine-wave output of relatively constant amplitude and frequency.

# Characteristics.

Utilizes R-C network to provide feedback.

Eliminates need for inductors in resonant circuit. Output frequency is usually fixed within the range of 15 Hz to 200 kHz per second, although the circuit can be arranged to provide an output which can be varied over a wide range of frequencies by changing R or **C**.

#### Circuit Analysis.

General. A sine-wave output may be obtained from an oscillator using an R-C network in lieu of an L-C network. The R-C network determines the frequency of oscillation and provides regenerative feedback from the output circuit to the input. In the common-emitter circuit configuration for transistors, the signal between the base and collector is shifted in phase by 180 degrees; therefore, an additional 180-degree phase shift is necessary to provide the correct feedback signal when returned from the output circuit to the input in order to sustain oscilla-. tions. The feedback signal of proper phase relationship is obtained using a network consisting of three equal R-C sections; each section produces a 60-degree phase shift at the desired frequency of operation. In the accompanying circuit schematic, the three R-C sections are designated as Cl, RI, C2, R2; and C3, R3.



**R-C Phase-Shift Oscillator Using PNP Transistor** 

**Phase-Shift Network. The** current in a series circuit comprised of resistance and capacitance is determined by the applied voltage divided by the series impedance of the components

$$(I=\frac{E}{Z}).$$

Since a series R-C circuit exhibits capacitive reactance, the current leads the applied voltage by a specific phase angle. The phase angle is determined by the relationship of resistance and capacitance. The voltage drop produced across the resistance is determined by the current through the resistance and therefore leads the applied voltage by a given phase angle.

For a vector analysis of the phase-shift network, refer to the discussion given for the electron tube **R-C phase-shift** oscillator.

At least three R-C sections are required to provide the **180-degree** phase shift needed to produce a positive (in-phase) feedback voltage. The values of resistance and capacitance for a three-section network are chosen so that each section of the network will provide a **60-degree** phase shift at the desired frequency.

The R-C phase-shift oscillator is normally fixed in frequency, but the output frequency can be made variable over a range of frequencies by providing ganged variable capacitors or resistors in the phase-shift network. An increase in the value of either R or

C will produce a decrease in the output frequency; conversely, a decrease in the value of either R or C will produce an increase in the output frequency.

By increasing the number of phase-shift sections comprising the network, the losses of the total network can be decreased; this means that the additional sections will each be required to have a lesser degree of phase shift per section so that the over-all phase shift of the network remains at 180 degrees for the desired frequency of oscillation. Since the loss per section is decreased as the amount of phase shift (per section) is reduced, many oscillators employ networks consisting of four, five, and six section; assuming that the values of R and C are equal for each section, the individual sections are designed to produce phase shifts per section of 45, 36, and 30 degrees, respectively.

**Circuit Operation.** The previous circuit schematic illustrates a PNP transistor in a commonemitter configuration. Resistors RI, R2, and R3 and capacitors Cl, C2, and C3 comprise the feedback and phase-shift network. Resistors R3 and R4 establish base bias for the PNP transistor. Resistor R5 is the emitter swamping iesistor, which prevents large increases in emitter current and causes the variation of emitter-base junction resistance to be a small percentage of the total emitter swamping resistor, R5, and effectively places the emitter at signal ground potentird. Resistor R6 is the collector load resistance across which the output signal is developed. Capacitor C5 is the output coupling capacitor.

Oscillations are started by any random noise in the power source or the transistor when input power is **first** applied to the circuit. A change in the base current results in an amplified change in collector current which is shifted in phase 180 degrees. The output signal developed across the collector load resistance, R6, is returned to the transistor base as an input signal inverted 180 degrees by the action of the feedback and phase-shift network, making the circuit regenerative.

The output waveform is essentially a sine wave; the output frequency is a fixed frequency. When fixed values of resistance and capacitance are used for the feedback network, the 180-degree phase shift occurs at only one frequency. At all other. frequencies, the capacitive reactance either increases or decreases, causing a variation in phase relationship;

thus, the feedback is no longer in phase and is therefore degenerative. Note, however, that if the components comprising the phase-shift network should change value, the frequency of oscillation will change to the frequency at which a phase shift of 180 degrees **will occur** to sustain oscillations.

# Failure Analysis.

**No Output. All** input voltages should be measured with an electronic voltmeter to determine whether the input voltage is present and whether the biasing voltages applied to the transistor are within correct operating limits. If it has been established that all voltages are correct, it is likely that circuit losses are present in the phase-shift network or that degeneration in the emitter circuit is preventing oscillation.

**Reduced or Distorted Output.** All voltages should be measured with an electronic voltmeter to determine whether the rnput voltage is present and whether the biasing voltages applied to the transistor are within correct operating limits. A change in base bias or load impedance or degeneration in the emitter circuit will cause reduced output and possible distortion; however, the output frequency will remain substantially correct.

**Incorrect Output Frequency.** The correct operating frequency of the R-C oscillator is determined by the circuit constants comprising the phase-shift network; therefore, if the output frequency is incorrect, it is likely that the phase-shift network components have changed vahre in such a manner as to permit a **180-degree** phase shift to occur and sustain oscillations at the incorrect output frequency.

#### WI EN-BRIDGE OSCILLATOR (ELECTRON TUBE)

#### Application.

The Wien-bridge oscillator is used as a variablefrequency oscillator for test equipment and laboratory equipment to supply a sinusoidal output of practically constant amplitude and exceptional stability over the audio-frequency and low-radio-frequency ranges.

# Characteristics.

It uses a bridge circuit to supply positive feedback

voltage at the **R-C** frequency to produce oscillation. It operates as a Class A linear amplifier and employs negative feedback to produce an almost perfect sine-wave output.

It also uses negative feedback to provide a practically constant output amplitude.

Frequency stability is excellent (2 to 3 parts per million).

Operates over a wide frequency range (10 Hz to 200 kHz or higher).

#### Circuit Analysis.

General. When the output of a linear amplifier is applied to its input, a feedback loop is produced. If the feedback is out-of-phase with the input, or negative, the amplifier output will be reduced. If the feedback is inphase, or positive, the amplifier will oscillate. The frequency of oscillation for positive feedback can be controlled by using a frequencyselective network in the feedback loop, such as the Wien bridge. When negative feedback is applied to the cathode circuit of an amplifier, it produces a degenerative effect which reduces the output and improves the amplifier response (this is called inverse feedback). By use of the impedance bridge circuit a differential input can be used to provide oscillation at the desired frequency, with amplitude and waveform control.

**Circuit Operation.** The basic bridge circuit and feedback loop are shown in the accompanying simplified diagram. In the actual circuit, R4 is a small incandescent lamp with a tungsten filament, and is normally operated at a temperature that produces a dull red or orange glow to give automatic control of amplitude (thermistors are also used). Resistors RI and R2 are of equal value, as are capacitors C 1 and C2, with R3 having twice the resistance of lamp R4 at the operating temperature. The bridge is balanced and the circuit oscillates at a frequency given by:

f. = 
$$\frac{i}{27r R1 Cl}$$

d

**ELECTRONIC CIRCUITS** 



Simplified Wien Bridge Oscillator

It can be seen by inspection that resistors R3 and R4 form a resistive voltage divider across which the output voltage of V<sub>2</sub> is applied. Since these resistors are not frequency-responsive, the voltage at any instant from point B (and the cathode of VI) of the bridge with respect to ground is dependent upon the ratio of R3 to R4 for any frequency which the amplifier produces at its output. Components RI, Cl, and R2, form a reactive voltage divider, between the output of V2 and ground, which is frequency-responsive, with the grid of V1 connected at point A. Thus the voltage across R2 is applied to the input of the amplifier, between grid and ground. When the voltage between point A and ground is in phase with the output voltage of V2, maximum voltage will appear between the grid and ground; therefore, maximum amplification occurs and a large output voltage is produced by V2. Two amplifier stages, V1 and V2, are used to produce a total phase shift of 180 degrees x 2, or 360 degrees, to insure that the voltage at the output is in phase with the input. Thus reactive networks RI, C 1, and R2, C2, are not required to shift the phase to produce oscillation, but are used to control the frequency at which oscillation takes place.

The manner in which these various feedback voltages vary in amplitude and phase are best shown by the following graphic representation. The center (dotted) vertical line (ordinate) represents the frequency at which the oscillator operates. The left and right vertical lines represent a frequency much lower than the operating frequency, and a frequency much higher than the operating frequency, respectively.



Phasing Diagram

Curve A represents the negative feedback between point B of the simplified schematic and ground. Since it is the same at all frequencies, it is represented by the horizontal line covering the middle of the graph. Curve B represents the positive feedback voltage existing between the grid (point A) of VI and ground, or the voltage across R2. At frequencies below the operating frequency (f<sub>o</sub>), the series reactance of Cl is large, and the voltage across R2 is reduced. As the operating frequency is approached, the reactance diminishes, and the voltage across R2 reaches a maximum at f.. As the frequency is increased above f, the parallel reactance of C2 shunts R2, effectively reducing the voltage across R2. Thus, both above and below  $\mathbf{f}_{0}$  the voltage across R2 is reduced, and only at the operating frequency is it a maximum. At this frequency, the positive feedback voltage (at the grid) is exactly equal to (or very slightly greater than) the negative feedback voltage (at the cathode), amplification is at a maximum for VI and V2. Now consider the phase of the output voltage which is fed back to the input of V1; this is shown by curve C. Because of the phase shift produded by RI, Cl, a phase shift occurs above or below the operating frequency; at the operating frequency, however, the phase change is zero, and the output of V2 is exactly 360 degrees from the input voltage, because of the phase inversion through two stages of amplification. Thus, below  $f_0$ the phase angle leads and above f. it lags. The out-ofphase voltage above and below f, together with the

decrease in the regenerative feedback voltage applied to the grid as compared with the degenerative feedback voltage applied to the cathode of V1 effectively stops oscillation at all frequencies except the operating frequency, where RIC1 equals R2C2.

The schematic of the Wien bridge oscillator is shown in the accompanying illustration. Operation is the same as previously discussed. Amplitude regulation is provided by the use of resistor R4, which is an incandescent lamp (DS 1) with a tungsten filament. The current through this lamp consists of the cathode current of V1 plus the ac current at the oscillating frequency through R3 and R4. The design is such that the lamp is operated at a temperature-sensitive point (where the resistance of the lamp changes rapidly with temperature). When the amplitude of oscillation tends to increase, the ac component of the current through the cathode and through the lamp increases. The resistance of R4 (DS1) increases in value because of its higher temperature, and, being in the inverse feedback circuit causes an increase of degenerative feedback. Thus, the amplitude of oscillation is automatically reduced back toward the original level.

In the schematic, resistors Rl, R2, R3, and DS1 and capacitors Cl and C2 from the arms of the Wien bridge.



Wien Bridge Osallator

Tube VI is R-C-coupled through C3 to the grid of V2. R5 is the plate resistor of VI, which produces a 180degree phase inversion. Resistor R6 is the grid resistor for V2 across which the output of V1 is applied. The circuit design is such that the phase shift

through the coupling network consisting of R5, C3, and R6 is kept to a minimum. The cathode of V2 is biased by R7, which is left unbypassed to provide degeneration and help keep the output waveform linear. The sinusoidal output waveform is developed across R8 and applied through C4 from the plate of V2 to the input of the Wien bridge as a 360-degree phase-shifted signal, which is now in-phase with the original signal. An output is also taken from the plate of V2 through capacitor C5 for external use. The values R8, C4, and C5 are also chosen to provide an absolute minimum of phase shift, so that the bridge circuit alone determines the feedback frequency. The operation of this circuit is similar to that of the basic circuit described above, with the oscillation frequency being at the frequency where R1 Cl equals R2 C2 and with waveform linearity retained by inverse feedback through R3 and R4. Biasing is a combination of cathode and contact bias, with a larger amount of degeneration (inverse feedback) being provided by the unbypassed cathode bias circuits; the output waveform is extremely linear. The output amplitude is small because of the large amount of degeneration employed, and circuit stability is excellent with a minimum of phase shift or frequency variation.

#### Failure Analysis.

**No Output.** Since the feedback loop involves two tubes and a bridge network, it is apparent that an open circuit in the coupling capacitors or bias resistors will stop oscillation immediately. An excessive phase shift caused by the change of coupling network values due to aging may also cause stopping of oscillation at the lower frequencies. It is rather improbable that changes due to the aging of would result in the stoppage of oscillation, although failure of one tube due to lack of emission or loss of gain could prevent operation. A defective lamp would produce an open cathode circuit in V1 and stop oscillation. Usually a resistance check will quickly isolate the trouble in this circuit.

**Reduced or Unstable Output.** The principal components to suspect in the case of reduced output are the electron tubes and the degenerative feedback components. An increase of cathode bias resistance with age or leaky capacitors which place improper bias on the grids not only will reduce the output, but will probably distort the waveform. Poor connections and soldered joints will also cause either condition. tubes -

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Following the signal path from grid to plate with an oscilloscope will quickly show lack of amplitude and any waveform distortion. Motorboating at low frequencies may occur through common impedance coupling in the power supply, and should be suspected if oscillations are produced at more than one frequency simultaneously.

Incorrect **Frequency**. Since the frequency is primarily under control of the reactive portion of the bridge network, these components should be suspected when the frequency is incorrect. Where band switching and tuning arrangements are included in the design, faulty switches, poor contacts, and bad connections would be the primary causes of frequency shift.

#### WIEN-BRIDGE OSCILLATOR (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version.

#### **Circuit Analysis.**

General. The Wien-bridge circuit consists of a resistive element and a reactive element arranged in a bridge. The resistive element supplies an inverse (negative) feedback voltage to the emitter, and the reactive network supplies a regenerative (positive) feedback voltage to the base of the same transistor. When the bridge is balanced (at the operating frequency), the positive feedback is slightly greater than the negative feedback and oscillation occurs. The operating frequency is determined by the R-C networks employed in the reactive bridge arm. To obtain the feedback, two transistor amplifiers are used, each producing a 180degree phase shift, or the total 360degree phase shift necessary for positive feedback to the base circuit. The negative feedback is obtained by inserting a portion of the feedback into the emitter circuit of the input transistor to produce an out-of-phase or negative feedback. The operation of the bridge circuit and the development of the positive and negative feedback voltages are the same as described for the electron tube counterpart.

Circuit **Operation.** The semiconductor Wien-bridge oscillator is shown schematically in the following

figure. Except for bias arrangement, it is practically identical to the electron-tube Wien-bridge oscillator.



Wien Bridge Oscillator Using PNP Transistor

Voltage divider base bias is used, with R2 and R5 biasing Ql, and R7 and R8 biasing Q2. Temperature stabilization is provided by series emitter (swamping) resistors R4 and R9 (see Section 3, paragraph 3.4, for an explanation of this action).

Resistors R3 and R4 form the resistive arm of the bridge across which the output of Q2 is applied; a portion of this voltage appears across R4 (DS-1) as a negative feedback, being in-phase with the emitter voltage. Resistor R4 (or DS-I or RT-1) is either an incandescent lamp or a thermistor with a positive temperature coefficient. When a lamp is used, it is operated at a current which produces a temperaturesensitive point (where resistance varies rapidly with temperature); when a thermistor is used, it is selected to have the desired temperature-current characteristic. In either case, the bias developed across this resistor is in opposition to the normal (forward) bias, and produces a degenerative effect. The feedback voltage is of the same polarity as the degenerative bias and increases the degeneration. However, since the output of the voltage divider is not frequencysensitive, the feedback voltage is always constant

regardless of the frequency of operation. At frequencies other than the frequency of operation the degenerative feedback predominates and prevents oscillation. At the frequency of operation, which is controlled by the bridge reactive arms consisting of R1, Cl, and R2, C2, the positive feedback is a maximum. This in-phase feedback signal is applied to the base and is slightly greater than the negative feedback at the balance point or frequency of operation which is given by:

f. 
$$\frac{1}{2rr R1 Cl}$$

where R1 is equal to R2, C2 is equal to C1, and R3 is slightly greater than twice R4.

The amplified output of Q1 is developed across collector resistor R6, and it is applied by capacitor C3 and base resistor R7 which form a conventional resistance coupling network (designed for minimum phase shift), to the input (base) of transistor Q2. The signal is further amplified by Q2, and the voltage developed across collector resistor R1 O is supplied as an output through capacitor C5, and, as a positive feedback through C4 to the bridge network. Note that the Q2 emitter resistor, R9, is not bypassed and that the circuit of Q2 is therefore degenerative. Note also that R1O, C4, and C5 are designed to provide a minimum amount of phase shift. Thus, with a highly degenerative two-stage amplifier and Class A bias, the output signal is essentially a pure sine wave. Since the coupling networks are arranged for minimum phase shift, the phase shift required for regeneration is obtained from the inverting action of the commonemitter configuration, with each amplifier stage providing a 180-degree shift. The feedback input signal is thus shifted 360 degrees in phase to produce a regenerative (positive) feedback independent of circuit parameters. The reactive portion of the bridge (Cl, C2 and R1, R2) determines the frequency at which maximum amplification (and feedback) occurs. Resistor R4 (DS-1) controls the degenerative feedback and also the output amplitude; that is, when the input signal to Q1 increases, more emitter current flows through R4 (DS-1), and the lamp or thermistor resistance increases, producing a degenerative voltage which opposes the input signal, and tends to restore it to the original operating vahre by reducing the amount of amplification through the feedback loop.

This oscillator then, with amplitude stability, temperature stabilization, and degenerative feedback to control the waveform, and with an R-C frequencyselective circuit to determine the frequency of operation provides a signal of excellent stability and pure waveshape for test applications. In order to control the frequency, either resistors R1 and R2 or capacitors C 1 and C2 are changed in value or made variable. With a two-gang variable capacitor and a selector switch (or fixed and variable resistors), a continuous range of frequencies over a number of bands may be obtained.

# Failure Analysis.

No Output. If the feedback loop or the coupling network between stages is open because of a defective (open) component or if the supply voltage is too low the circuit will not oscillate. Also, if the coupling capacitors are short circuited, the circuit will not oscillate because the bias circuits will apply an abnormal bias to Q1 and Q2. For example, with C4 shorted the emitter of Q1 will be negatively biased and stop oscillation; with C3 shorted the bias will be provided by the parallel combination of R6 and R8 in series with R7 and most likely will be too large to permit operation. If the R4 bridge arm opens, the emitter will be disconnected from the circuit and the transistor will not operate. A resistance analysis and continuity check of the circuit with a high-impedance voltohmmeter should quickly determine the defective component.

Reduced or Unstable Output. An intermittent open or short in any of the bridge reactive network parts will change the frequency of operation and cause instability. Poor contacts in band switches will also cause instability. When the output is reduced, it is logical to suspect that a defective component in the positive feedback loop is permitting the degenerative action to predominate. Since some positive feedback is required to maintain even a weak oscillation, the reduced output would most likely be caused by increased series resistance in the positive feedback loop, because an open in this loop would stop oscillation. Failure of the transistors with age or reduced output because of lack of emission as in an electron tube would be the least likely cause of reduced output. Normal aging of the transistor will have little effect on oscillation since operation is over only a small

d

range of amplitude and only small currents are involved. In the event of damage to the transistor, by the application of improper bias or by the application of ohmmeter voltages and polarities that exceed the transistor rating (through poor testing techniques) reduced or no output will occur, but this type of trouble is due to factors external to the circuit and normally should not happen. The supply voltage should be checked for the rated output voltage because a low supply voltage could readily affect the oscillator output.

**Incorrect Frequency. Where** the frequency of operation differs from the original calibration, the cause might be the aging of circuit parts such as changes in value of R and C in the reactive arm of the bridge or possibly poor switch contacts. Any large change of frequency which cannot be compensated for by retrimming or recalibration is most likely due to defective parts in the frequency arm of the bridge (Cl, C2, RI, R2). If the frequency change is linear, the resistive parts should be suspected; if it is non-linear, the capacitive parts should be suspected. The circuits of **Q1** and Q2 would not effect any frequency changes.

# **MAGNETOSTRICTION** OSCILLATORS

# Application.

The magnetostriction type oscillator is usually used at audio, supersonic, or low radio frequencies to provide an extremely stable sine-wave output. This circuit is employed in preference to the crystal type of oscillator at the very low frequencies because of its simplicity, ease of construction, and economy due to the lack of suitable quartz crystals. If finds particular application in laboratory test equipment and low-frequency standards.

#### Characteristics.

Uses a nickel-steel alloy rod to control the frequency of oscillation.

Feedback is through magnetostriction effects and not through externally coupled inductors.

Provides frequency stability of less than one Hertz at audio frequencies.

Produces an approximate sine wave of relatively constant amplitude.

Circuit Analysis.

**General. The** magnetostriction effect is similar to the piezoelectric effect found in crystal oscillators.

Instead of using electric charges, however, it operates by the effect of a changing magnetic field. When an iron-alloy rod is placed within a magnetic field, there is a change in length due to the strain placed on the rod by the magnetic field. This compressional strain, in effect, squeezes the rod and makes it longer; when the field is removed, the rod return to nearly its former length. Similarly, when a rod located within a magnetic field changes its length, it also includes a change in the magnetic field, increasing or decreasing the field. The induced change is dependent upon the original direction of the magnetic field and the polarization of the metal rod and its composition. When the change in length of the bar is performed at the resonant (mechanical) frequency of the bar, and the induced change is properly phased to enhance the field that produces the strain, mechanical oscillations are set up at the fundamental frequency of the bar. When clamped in a fixed position at the middle, the bar will vibrate with a flexural motion similar to a tuning fork. The metal composition of the bar determines its efficiency and effectiveness as a resonator. A pure iron rod will oscillate very feebly if at all, and a nickel rod will vibrate strongly, but has poor stability. A combination of nickel and iron, such as Invar or Stoic metal, oscillates strongly but has a poor temperature coefficient. With the addition of a small amount of chromium to the nickel alloy, one of the strongest vibrators and most readily available metals (Nichrome) is produced. A coupper-nickel alloy (Monel) has too little residual magnetism to operate without an external field, but when a permanent magnet is held nearby it oscillates strongly. Temperature effects will cause changes in the bar length and thus affect the frequency of operation; hence, for extreme stability, the alloy must have a small temperature coefficient or temperature control must be used. Operation in this respect is similar to the

The change in length at fundamental longitudinal (mechanical) vibrations is on the order of one part in one million (of an inch) for a field of one gauss, using a nickel rod as an example, but when the rod is resonant, the change in length is multiplied one hundred times or more. Thus, at the resonant frequency the mechanical change in length is sufficient to produce a substantial change of field, and control the operation of the oscillator. At the lower audio frequencies, it is desirable to use an oscillator phased to oscillate very feebly, if at all, without the rod. At

operation of crystal oscillators.

supersonic and low r-f frequencies of from 25 to 300 kHz, the **oscillator** is not very greatly affected if the basic electronic circuit oscillates strongly without the bar. The stability of the bar prevails in either case. By utilizing nickel tubing with a negative temperature coefficient and filling the tubing with Stoic metal which has a positive temperature coefficient, temperature compensation may be achieved to produce a nearly zero-temperature-coefficient bar.

Although operation is possible at 2 MHz and higher, the oscillation is usually feeble and not nearly so strong as that of the conventional quartz crystal; therefore, operation of this type of oscillator is usually restricted to the lower frequencies.

Circuit Operation. The basic circuit of the magnetostriction oscillator is shown in the accompanying illustration. Grid bias is obtained conventionally through gridleak operation  $(C_g R_g)$ , and series plate feed is used. The coils are wound so as to produce the same flux at the plate end of the bar for an increasing plate current or an increasing grid current (they are in-phase). This condition, which is opposite to that of the normal feedback oscillator, produces degenerative feedback, rather than regenerative feedback. In addition, these plate and grid coils have no coupling or only very loose coupling. Thus, the oscillator will normally not oscillate at all, or oscillate only feebly, as a result of feedback between the interelectrode capacitances. Capacitor Cl is the tuning capacitor, and is connected so as to tune both the plate and grid coils (either one along may be tuned if desired). For a single frequency or frequencies within a narrow range of operation, Cl may be fixed and different lengths



Magnetostriction Oscillator

of rod may be inserted in the coils (similar to crystal plug-in operation) for the different frequencies.

Assume that plate voltage is applied and that the plate current is producing a steady strain on the rod. If a noise pulse occurs and produces an increase of flux in the plate coil, a compressional wave will be started at the plate end of the bar and will travel to the left toward the grid end. This compressional wave due to magnetostriction will travel through the bar in a manner similar to the propagation of sound waves through a metal bar. When the compressional wave reaches the grid coil,  $L_g$ , the lengthening of the bar induces a positive voltage in the grid coil, which is applied to the grid and causes the plate current to increase. The increased plate current induces a stronger field around the plate coil, inducing another compressional wave into the bar. The compressional waves in the bar are reflected from the grid end and travel back to the plate end, where they again are reflected back toward the grid end. When the compressional wave which is reflected from the grid or left end of the bar reaches the right or plate end, a voltage is induced in plate coil L<sub>p</sub> by the lengthening of the bar. This voltage, by induction, creates a stronger field around the plate coil. Consequently, the motion of the plate end of the bar is further reinforced, causing it to vibrate more strongly. As a result, another compressional wave is started and the cycle repeats. When the induced and reflected are in phase, the grid-reflected wave arriving at the plate end will always reinforce the induced wave at the plate end, producing at stronger oscillation. Therefore, the length of time it takes for the wave to travel from one end of the bar to the other and return will determine the phasing of the reflected and induced waves. For each length of bar, there will be a specific time taken for a wave to travel to the end and return; if the length is made equivalent to an electrical half-wavelength, each wave will reinforce the other. When the frequency of the tuned circuit (as adjusted by Cl) is approximately the same as the resonant frequency of the bar, maximum reinforcement will occur and maximum mechanical vibration will be produced. With the bar initially unpolarized, operation will occur at the second harmonic. Therefore, the bar is usually permanently magnetized and inserted into the coils so that the field of the plate coil increases the polarization. Operation then takes place at the fundamental frequency (f = v/21 where v is the velocity of sound and 1 is the length of the bar). Adjusting

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tuning capacitor Cl for maximum plate current tunes the oscillator to the bar frequency, and feedback is provided mainly through magnetostriction action. Even though there may be some coupling to produce oscillation without the bar, with the bar in place oscillation is strengthened and maintained, being controlled by the mechanical vibration of the bar.

When the bar vibrates at an audio frequency, the sound is audible close to the bar. The operation is similar to the operation of an ac driven tuning fork. The difference is that the tuning fork is actually driven by an ac signal (audio) from an oscillator operating at the frequency of the tuning fork. The tuning fork vibrations induce a magnetic change in a pickup coil around one leg of the fork, thus inducing a stable mechanically controlled sigml back into the driving oscillator. The output of the magnetostriction oscillator is usually capacitively coupled from the plate circuit into an amplifier, operating as a buffer on either the fundamental or the desired harmonic frequency.

#### Failure Analysis.

**No Output.** If the bar (or tube) is mechanically defective or the tuned circuit is not adjusted to the bar frequency, no output will result. A plate milliammeter connected in the plate circuit will abruptly indicate a two or three times increase of current when tuning capacitor Cl is adjusted to the bar frequency. Otherwise, the circuit is probably open and should be checked with an ohmmeter.

Low Output. A low supply voltage or poor soldered connections which introduce high resistance into the circuit can cause a reduction of developed signal. Excessive bias developed by an RC grid-leak combination which has too large a time constant can cause blocking of the grid and motorboating. Normal resistance and voltage checks will quickly isolate the defective portion of the circuit.

**Incorrect Frequency.** Since feedback occurs at the bar frequency and is practically independent of the tuned circuit, only a free-running oscillator operating considerably away from the fundamental bar frequency can produce an incorrect frequency. Actually, once the bar starts oscillating the tuned circuit can be varied over quite a noticeable tuning range before oscillations cease. Thus, small changes in the LC circuit will affect only the output amplitude. The use-fulness of this circuit as a frequency stabilizer stems from the fact that only the mechanical vibration of

the bar determines the frequency of oscillation. Therefore, at low audio frequencies it will be practically impossible to obtain a different frequency. At r-f frequencies, however, it is possible for spurious oscillations to occur at a frequency not related to the bar frequency because of operation of the electron tube circuit as another form of self-excited oscillator. The frequency of operation should indicate the relative values of components involved, so that the circuit can be examined for lumped capacitance and inductance which could resonate at the undesired oscillating frequency.

# NEGATIVE RESISTANCE OSCILLATORS

#### General.

The negative resistance type of oscillator includes the dynatron, which operates by virtue of secondary emission effects in a screen grid tube, the negative transconductance pentode (or transitron) circuit, and the push-pull (or kallitron) circuit. There is also a possible fourth class, that is, the negative grid resistance type (better known as the tuned grid oscillator with capacitive feedback inherent within the tube); however, this oscillator is not used very much at present. Since it is sometimes included in the negative resistance group, however, it is mentioned here; the interested reader is referred to standard texts for this data.

Negative resistance is a somewhat vague term, which is not very well understood by the layman, or even by many engineers. Actually, it is a term used to describe an imaginary property dealt with in the mathematical analysis of oscillators (and also in amplifiers to a limited extent). It is often erroneously defined as the opposite of positive resistance, which is considered as conventional, or real, resistance. This definition is based on the fact that positive resistance manifests itself by an increasing voltage drop as the current is increased. Negative resistance, on the other hand, manifests itself by a decreasing current as the voltage applied to the device exhibiting the negative resistance is increased, or by a decrease in voltage as the current is increased. While these physical effects are real, the derivation and meaning of the term is purely artifical.

In the mathematical analysis of oscillators, a series of terms have been developed to describe the properties of the circuit; they are then added and equated

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to zero. One of these terms is always positive resistance, which is real: it exists in the dc and ac resistance of the coils and leads, and is always assigned a positive value. Therefore, to be equated to zero, the series must contain certain other terms that are of equal, but negative, value. It is this negative resistance which, when it equals the positive resistance mathematically, permits oscillation. With any type of oscillator, both the positive and negative resistance concepts apply. In the oscillators considered previously, the negative resistance is created by an external circuit, such as an inductive or capactive feedback arrangement. In the true negative resistance type of oscillator, however, the negative resistance is an inherent property within the tube or device which exhibits it. There is no circuitry involved other than the requirements to supply a tank circuit or inductor in parallel (or sometimes in series) with the negative resistance. The basic simplicity of this type of circuit makes it useful if its inherent defects do not nullify the advantage of its simplicity.

A more effective way to understand *negative resistance* is to visualize it as a generator of energy. In contrast to positive resistance, which *dissipates* energy at a rate proportional to the square of the impressed voltage or current, negative resistance *generates* energy at a rate proportional to the square of the impressed voltage or current.

Negative resistance may be either voltagecontrolled or current-controlled; the accompanying figure illustrates the volt-ampere characteristics of these two types of control. As can be seen, each type is the exact inverse of the other. In the voltagecontrolled device, as the voltage is increased the current rises to a peak, and then drops to a low value from A to B (this is the negative resistance region) and then increases to a new peak value thus the voltage is a single-valued function of the current. In the current-controlled type, the voltage varies similarly as the current is increased, and the current is a single-valued function of the voltage. Note the characteristic "lazy S" pattern of these curves, which makes them easily identifiable. The oscillators described in the following discussions are all of the voltage-controlled type.

When either a parallel resonant or a series resonant tank circuit is connected across a negative resistance device, it can be mathematically demonstrated that oscillation will occur if certain conditions are satisfied. The basic equivalent circuit of a negative resistance oscillator is shown in the accompanying illustration. L, C and r in the figure represent the tank inductor, capacitor, and tank resistance respectively, and p represents the negative resistance.





# Basic Negative Resistance Oscillator Equivalent Circuit

It can be shown mathematically that when p is smaller than the ratio L/rC the amplitude of oscillations will build up. On the other hand, when p is greater than the ratio of L/rC, the oscillations will diminish in amplitude and eventually cease. The criterion for constant oscillation with no change in amplitude is that p be just equal to L/rC. Thus for oscillation to occur, p must be less than, or equal to, L/rC.

If a generator is substituted for p in the basic figure, it can be understood how the basic concept of negative resistance applies. The region where the device exhibits a negative resistance normally covers a limited range, and is never associated with positive resistance. That is to say, when the device is operated as a conventional feedback oscillator, the operating region is beyond that portion associated with the negative resistance properties. Thus, devices which exhibit negative resistance can also be employed in circuits involving the positive resistance region of operation without any conflict with their negative resistance characteristics. For example, the same type of tube which is particularly useful in the dynatron oscillator (because of its inherent secondary emission at plate voltages lower than the screen voltage) may also be used in conventional LC feedback oscillator circuits operating at higher plate and screen voltages in the so-called positive region. For good waveform, it is important that large capacitance values be used in the tank circuit of the negative resistance oscillator, as small capacitance will cause distorted output waveform.

# DYNATRON OSCILLATOR

### Application.

**The** dynatron oscillator is used to produce a stable sinsonidal output over the low, medium, and highfrequency r-f ranges (and sometimes the audiofrequency ranges). It is used mostly as a signal generator for laboratory or test equipment purposes or as a bent-frequency oscillator in receivers.

#### Characteristics.

Uses the negative resistance of a screen-grid tetrode to produce oscillation.

Provides very good stability, but at a low output amplitube.

Uses a two-terminal tuned circuit to determine the frequency of operation.

#### Circuit Analysis.

General. The dynatron circuit was originally based upon the use of the type 24 screen-grid tube, which exhibited considerable negative resistance at low plate voltages. The negative resistance was due to secondary emission from the tube plate. Present day tube manufacturing and design methods have minimized the undesired secondary emission, but it still exists at very low plate voltages in most tetrodes. Secondary emission occurs when the plate is much lower than the screen voltage, because of bombardment of the plate by electrons which have passed the screen grid. With high or normal plate voltage these electrons are attracted back to the plate and have no effect. With low plate voltage, however, the field of the grid extends into the plate region and attracts the secondary emitted electrons knocked out of the plate. Thus, the plate current is reduced by the amount of secondary electrons captured by the screen grid, and the screen current is increased. The accompanying figure illustrates typical plate and screen currents for a type 24 tube. These curves have the distorted "lazy S" shape characteristics of negative resistance as explained previously in the general discussion. When the tube is operated in the region of negative slope with a tank circuit connected to either the screen or the plate, oscillation will occur. Maximum screen current flows when the plate current is minimum (point B on the curve). Useful oscillation is

**ORIGINAL** 491-044 0-73 -41 possible between points A and B, with the oscillator adjusted to work at the midpoint of this negative resistance region. From points B to C and beyond is the positive resistance region, which cannot be used for dynatron operation. It can be clearly seen that the plate of the dynatron must be operated at extremely low voltages; therefore, the amplitude of oscillation is limited and the circuit is capable of a only a small output. The output amplitude is controlled by adjusting the grid voltage, which varies the slope of the negative resistance region.



Plate and Screen Current Relationships

One of the advantages of this type of oscillator is that it requires only a single coil with tuning capacitor, instead of a tapped coil or an additional tickler winding. Thus its extreme simplicity made it popular. On the other hand, since secondary emission varies with the age and emission of the tube, and since tubes of the same type and manufacture have widely different secondary emissions, it is necessary to have a plate voltage control to permit adjustment for stability with tube aging and the use of different tubes. Because of the low output and the variation of secondary emission from tube, this circuit is not very widely used today.



#### **Dynatron Oscillator**

The grid is biased by means of potentiometer  $R_k$  when cathode current flows. Adjustment of the grid arm of the potentiometer effectively places the grid at a more negative potential with respect to the cathode in one direction of rotation, and at a less negative potential in the other direction of rotation. The screen is connected to the high side of the plate supply and bypassed by  $C_{sc}$ , and the plate is connected to a voltage divider consisting of **R1** and **R2**. Thus, the plate voltage is reduced below the screen voltage. Capacitor  $C_p$  is the conventional series-feed bypass. The tuned tank, consisting of L and C, is placed in the plate circuit, although it could also be placed in the screen circuit. The output is taken capacitively from the plate by Cc.

The inherent stability in this type of oscillator is based upon the action of the tank circuit primarily, as in other types of the LC oscillator. Although operation at a low plate voltage limits the output to a low value, it also contributes some stability, because

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load changes are a smaller percentage variation than in other self-excited power type oscillators. Since the feedback is inherent in the tube, rather than being provided by an external circuit, changes in tube element capacitances are not as effective in causing frequency changes, thus contributing to the stability of this type of oscillator. Therefore, a dynatron which is properly adjusted for the correct operating point and plate voltage is practicrdly equivalent to the electron-coupled LC oscillator, as far as frequency stability is concerned.

Operation at a low amplitude insures better linearity and less harmonic content in the output, accounting for the relatively pure output waveform of this type of oscillator. Variation of the grid voltage changes the slope of the negative resistance characteristic and thus governs the operating amplitude.

Detailed Analysis. Mathematically it can be demonstrated that when an LC tank circuit is connected to a negative resistance element oscillations will start and continue, with the negative resistance supplying the losses caused by the positive resistance of the tank. In the conventional external feedback oscillator, this same action is obtained by the feeding back of output voltage in-phase with the input voltage. In the dynatron it is inherent within the electron tube. Thus, in the conventional feedback oscillator, as the plate voltage is increased, the plate current is also increased and the amplitude of oscillation is primarily limited by the power supply voltage. In the dynatron, with the plate operating at a lower voltage than the screen, as the plate voltage increases the plate current decreases. As the plate current decreases, since the supply voltage remains substantially the same (considering a regulated supply), there is more voltage available for the load. Thus, as the tube current becomes smaller, the voltage across the load builds up. In effect, the tube is releasing energy from the power supply instead of absorbing it. Therefore, the tube can be considered as a generator which supplies power to the tank circuit. The generated energy is used to overcome the losses in the tank circuit, and the oscillation builds up until an amplitude is reached where a state of equilibrium is obtained, and continuous oscillations are produced without any external feedback circuitry. All that is required is to shock excite the tank circuit into oscillation, and once started the action continues. Starting is produced by turning the circuit on. The initial rush of current to the plate produces a transient oscillation in

the tank circuit, at the approximate frequency to which it is tuned. In the absence of negative resistance, this oscillation would quickly die out, being damped by the positive resistance of the tank. The inherent negative resistance of the tube, however, provides an effective in-phase feedback. Consider the tank circuit and its operation. In an oscillator condition, the coil and capacitor are interchanging energy. First the capacitor tends to charge as the transient increases, and the charging current flows through the inductor in a direction which increases its magnetic field. As the transient reaches its peak and drops, the magnetic field about the coil collapses and induces a reverse voltage in the coil, which is in the direction of capacitor discharge. Consider now the instantaneous ac component of plate voltage. As the transient increases in amplitude, the total effective plate voltage is increased and the instantaneous plate current is reduced. With a lowered current the plate voltage tends to rise, and this constitutes a higher effective plate voltage. Thus, the action within the tube is such as to aid the transient, and the tube is quickly driven to its saturation region (point Bon the plate and screen curves shown previously). At saturation the plate current does not change, so the inductor field collapses and the reverse cycle occurs. Since the voltage is decreasing, the plate current increases; this in turn, reduces the available plate voltage, and the tube absorbs the power. The transient is now falling and effectively subtracts from the total applied plate voltage. Thus the plate voltage is driven in a negative direction (a peculiarity of the dynatron region), whereupon the plate current change reverses itself. At this time the capacitor, which is discharged, proceeds to charge again and the cycle is repeated. The limits of operation are set by the applied grid bias, which determines the operating point, and the static plate voltage.

Unfortunately, the effects of secondary emission are not completely controllable, and the setting for optimum amplitude and efficiency for each tube of the same type varies. The negative resistance oscillator circuits which follow are considered to be better from the standpoint of stability and criticalness of adjustment than the dynatron circuit. When the tank tuning capacitance is reduced to that of the tube elements and leads, the output waveform is considerably distorted, and operation approaches that of the relaxation oscillator with the frequency of operation being set by the time constant of the resistance

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and capacitance in the circuit, With the turned tank, however, the angular frequency of oscillation is approximately

$$\omega = \sqrt{\frac{r+p}{p} \frac{1}{LC}}$$

Since r, which represents the ac resistance of the coil and leads, is usually only a few ohms, whereas the negative resistance p is seldom less than two or three thousand ohms, the frequency of oscillation is practically equal to

$$f_o = \frac{1}{2\pi \sqrt{LC}}$$

As a result, small changes in p which result from changes in the supply voltage have negligible effect on the frequency of oscillation at the threshold value, where p is equal to or less than L/rC.

# Failure Analysis.

No Output. A no output indication will be caused by lack of supply voltage, or by a plate voltage which exceeds the screen voltage and places operation in the positive resistance region, producing a non-oscillatory condition. An increase in coil resistance due to poor contacts or soldered joints can place operation in the non-starting region; such resistance will be so high that it will be revealed by a resistance analysis. With normal voltages applied and no oscillation, either the tank circuit is short circuited, or the secondary emission has changed and requires an adjustment of plate, screen, and grid voltages or a change of tubes. A change of load can change the negative resistance values and place the circuit in the nonoperative region. In this case, removing the load will restore normal operation and indicate the source of trouble.

**Reduced Output.** A primary cause of reduced output, which is common in this circuit, is for a change to occur in secondary emission, requiring a readjustment of operating voltages or the selection of another tube. A change in grid voltage to an operating **region** of small slope will also cause an amplitude change and reduced output. Such a condition will be evident by a grid voltage check. The reduction of applied plate voltage through a defective voltage divider can also cause the same condition. Thus, voltage and resistance checks should quickly reveal any defective components.

**Incorrect Frequency.** Changes in load or changes in applied screen and plate voltages will change the frequency slightly, but the effect is usually negligible. Since the tank circuit is the primary frequencydetermining portion of the circuit, any large frequency change will be due to a change in tank circuit parameters. Usually the tuning range is sufficient to adjust the circuit to the desired frequency. Once properly set, any noticeable frequency change indicates either ambient temperature effects or poor contact resistances (soldered joints) in the tank circuit.

# TRANSITRON (NEGATIVE GM) OSCILLATOR

# Application.

**The** transitron, or negative transconductance  $(g_m)$ , oscillator is used to supply a stable sinusoidal waveform at audio and low or medium radio frequencies. It is used mainly in test equipment, receivers, and laboratory instruments that require a simple band-switching oscillator.

# Characteristics.

Uses the negative transconductance effects of a pentode to provide negative resistance type of oscillation.

Uses an external capacitor coupled between the suppressor and screen to obtain negative transconductance.

Utilizes a two-terminal tank circuit to determine the frequency of operation.

# Circuit Analysis.

**General.** When a negative voltage is applied to the suppressor grid of a pentode, it will cause electrons that have passed through the screen grid to return to the screen grid. If the negative suppressor voltage is decreased (made more positive), more electrons will be attracted to the plate, and the screen-grid current will be reduced. Thus, the screen-to-suppressor transconductance is negative. With proper voltages and circuit arrangements, the screen current will decrease with a small positive voltage increases on the suppressor, even when the screen voltage is also increased an equal amount. The accompanying figure shows a typical screen current versus screen voltage characteristic curve of a pentode which has its suppressor coupled to the screen through a capacitor. The

typical distorted "lazy S" pattern indicates that there is a negative slope. There, oscillation will occur if an LC tank circuit is connected in the screen circuit.



Negative Transconductance Characteristic

If the control grid is biased negatively, the bias may be adjusted to control the amount of negative resistance developed. With the negative transconductance arrangement, the control and development of the negative resistance effect is by electrode voltages and circuit parameters. Thus, the transitron oscillator does not depend upon secondary emission for its operation; therefore, it does not have the undesirable features of the dynatron oscillator, although the circuit is somewhat more complicated.

**Circuit Operation. The schematic** of the basic transitron oscillator is shown in the accompanying figure. In this circuit, the LC tank is inserted in the screen grid circuit, and the screen is capacitively



Basic Transitron oscillator

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coupled to the suppressor through capacitor Cc. The output is taken capacitively from the screen circuit through Cl.

Cathode bias is employed, and the grid is returned to potentiometer  $\mathbf{R}_{\mathbf{k}}$ . Variation of the negative grid bias permits the slope of the negative transconductance region to be controlled. Thus, both output and linearity control are effected. Note that the plate is placed at a reduced potential with respect to the screen grid by means of the voltage divider consisting of RI and R2. The basic arrangement is the same as in the dynatron oscillator, except that the pentode has an additional element, the suppressor. Since the suppressor is located between the screen and plate, it will control the current between these elements when properly biased. To produce the negative transconductance, the screen is capacitively coupled through C<sub>c</sub> to the suppressor, and the suppressor is returned to ground through  $\mathbf{R}_{\mathbf{c}}$ . As a result of these connections, instantaneous ac variations of the screen voltages are effectively applied to the suppressor, and dc variations are effected through the RC network in accordance with the time constant. For proper operation, it is imperative that the reactance of C<sub>e</sub> at the operating frequency be very small as compared with the resistance of R. This is necessary to ensure that practically all of the feedback voltage appears across  $\mathbf{R}_{\mathbf{c}}$  and that very little voltage divider action occurs, as when C<sub>c</sub> has a large value of reactance. The effect of the voltage divider action is to reduce the feedback and produce a higher negative resistance, which is not desired.

In a pentode, the movement of electrons from the cathode to the screen and plate constitutes the screen  $(i_{sc})$  and plate currents  $(i_p)$ , respectively. Variations in suppressor voltage  $(e_{sv})$  have negligible effect on the total number of electrons leaving the cathode because of the shielding effect of the screen and control grids. The suppressor grid voltage, however, does control the division of the space current between the screen and plate. Making the suppressor voltage Icss negative results in a greater number of electrons passing through to the plate; consequently, the plate current,  $i_{p}$ , increases while the screen current,  $i_{sc}$ , decreases. On the other hand, making the suppressor voltage more negative results in fewer electrons being passed through to the plate, and a decrease of i<sub>n</sub>, with an increase  $\dot{m} i_{sc}$ . Typical variations of the screen and plate currents with changes in the suppressor voltage are shown in the accompanying graph. A decrease of  $i_{sc}$  with an increase of  $e_{su}$  indicates the existence of a negative transconductance between the screen suppressor grids. Since the reactance of C<sub>c</sub> is negligible at the frequency of oscillation, the alternating components of the screen voltage and the suppressor voltage are of the same polarity. Therefore, an increase in screen voltage instantaneously increases the suppressor voltage and, because of the negative transconductance, decreases the screen current. Thus, the negative transconductance of the tube produces, in effect, a negative resistance between the screen grid and cathode.



Plate and Screen Currents vs. Suppressor Voltage

When the transitron oscillator is adjusted so that the negative resistance is smaller than the vrdue needed to produce continuous oscillations, any brief oscillation or transient caused by closing of the plate switch is amplified. As a result, the operating range on the screen current versus suppressor voltage characteristic curve is increased, and, because of the curvature of the characteristic, the average slope of the part used is decreased. Since this is the same as increasing the value of the negative resistance, the amplitude of oscillation increases until the value of the negative resistance is such that it maintains a constant amplitude of oscillation.

**Detailed Analysis.** For oscillations to be sustained, the losses in the tuned circuit must be replaced by energy supplied from the electron tube. The losses produced by the circuit resistances are best illustrated in the accompanying transitron equivalent circuit.

The negative resistance presented by the tube to the tuned circuit is represented by  $R_{s}$ , and the tank circuit losses by  $R_i$  in parallel with the LC tank. The shunt resistance of suppressor return resistor  $R_{su}$  and load resistor  $R_L$  are effectively in **parallel** with the negative resistance and the tank loss resistance. The sum of  $R_L$ ,  $R_{su}$ , and 1\$ is the effective positive resistance. The current in  $R_N$  must be equal and opposite to the total current through this positive resistance. If  $R_N$  is larger than the positive resistance, the current through  $R_N$  is too small and the oscillations die out. If  $R_N$  is smaller, the current is too large and the oscillations increase in amplitude. When the current through  $R_N$  is just sufficient to sustain oscillations, the circuit is the equivalent of a simple LC combination, and the frequency of operation is:

$$f = \frac{1}{2\pi\sqrt{LC}}$$



**Transitron Equivalent Circuit** 

# Failure Analysis.

No Output. The loss of plate voltage due to defective divider resistors, the lack of screen voltage due to an open tank coil or a defective supply source, or a defective tube will cause loss of output. A change in the value of the feedback capacitor can reduce the feedback below the amount required for oscillation, depending upon the frequency of operation. High resistance coil contacts (poor solder joints) will also cause circuit losses high enough to stop operation. Since there are relatively few components, trouble should easily be isolated by a voltage check to determine proper operating conditions, and by a resistance analysis if the voltage are apparently correct. It should not be necessary to select tubes to produce oscillation, because, unlike the dynatron, the circuit is operable regardless of secondary emission.

Restoring oscillation by the selection of tubes indicates insufficient feedback between the screen and suppressor due to incorrect or changed values of  $R_c$  or Cc.

**Reduced Output.** Excessive reactance in the suppressor-screen feedback circuit can change the negative resistance value and reduce the amplitude of oscillation. However, reduction of output is more likely to be caused by excessive bias on the control grid, which will restrict operation to a very limited range of negative slope. Also, excessively low screen and plate voltages will cause a reduction in over-all amplitude, even though the tank circuit at resonance will provide an increase of output. In oscillators covering a wide frequency range where the feedback capacitor value is changed by a switching arrangement to produce optimum feedback, difficulties with switch contacts may cause loss of amplitude on some of the ranges.

**Incorrect Frequency or Instability.** Since the tank circuit is the primary frequency-determining element, normal variations of frequency due to aging of components should be easily compensated for by adjustment of the tuning capacitor. After the capacitor is adjusted, if the frequency varies it is probably due to the effect of ambient temperature changes or r-f heating on the tank inductance and distributed capacitance.

# KALLITRON (PUSH-PULL) OSCILLATOR (ELECTRON TUBE)

#### Application.

The push-pull negative resistance type of oscillator, known as the *Kallitron*, is used to produce pure audio-frequency waveforms, with low harmonic content. Its use is mostly confined to laboratory type audio generators and test equipment.

#### Characteristics.

Uses two tubes in a push-pull feedback arrangement.

Uses a tuned LC tank to determine frequency of operation.

Produces a sinusoidal output waveform, with low harmonic content.

#### Circuit Analysis.

General. In a balanced push-pull circuit with no input voltage applied, the quiescent plate currents

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and voltages are equal. When an input is applied, first one tube conducts, and then the other conducts. Assuming a sine wave input, as tube 1 goes through a positive grid excursion, it develops an inverted polarity output across its plate load resistor. If this inverted output is applied to the grid of tube 2, a positive output will be developed in the plate load of tube 2. If the plate output of tube 2 is fed back to the grid of tube 1, the positive input excursion will be enhanced, and the tubes will be driven in opposite directions equally. As the input waveform changes polarity the opposite action occurs, with grid 2 now being driven positive and grid 1 negative. If a tank circuit is connected between the plates of these tubes, oscillation will occur because of current flow in the external circuit, and the frequency will be determined mainly by the tank circuit resonant frequency. The accompanying figure shows an elementary oscillator circuit of this type, with the tank connected between points A and B (bias voltage is not shown for simplicity).



**Elementary Push-Pull Oscillator** 

As can be seen, the circuit is basically a simple multivibrator. However, in a multivibrator the current (and voltage) changes abruptly from one value to another and is determined mainly by the values of R and C in the circuit. In the Kallitron oscillator, however, the oscillation is controlled by the tuned tank circuit, and there are no abrupt changes, the transition from one state to another or conduction being smoothly sinusoidal. Because the plate voltage of each tube increases when the plate current decreases, there is in effect a negative resistance between the two plates. The second harmonic output is effectively reduced by the push-pull action, and the third harmonic content is reduced by the tuned circuit. Therefore, the output waveform is relatively pure, having a minimal amount of harmonic distortion.

**Circuit Operation. The** schematic of a typical Kallitron oscillator is shown in the accompanying illustration. Usually a dual triode in one envelope with its accompanying circuitry is used to provide, in effect, a single tube oscillator. To keep the push-pull relationships in balance, the output is generally taken inductively, but it may be taken capacitively.



# Kallitron (Push-Pull) Oscillator

Cathode bias is provided by  $R_k$ . Since the tubes operate in push-pull through a common cathode bias resistor, it can be seen that as the plate current of tube 1 increases the bias also increases, and, being applied to the V2 cathode, it reduces the plate current of tube 2. On the other half cycle, the operation is reversed, with the VI current decreasing and the V2 current increasing. The net result is a negligible change in cathode current. Feedback is obtained by cross-connecting the grids and plates through CC. Thus as the grid of V1 rises, the plate current increases, causing the voltage on V2 grid to fall, which increases the plate voltage of V2 and feeds back a rising grid voltage to VI grid, Likewise, on the opposite cycle the conditions reverse. The output amplitude is controlled by proportioning the grid resistors,  $\mathbf{R}_{\mathbf{g}}$ , and the grid coupling capacitors, Cc. The amplitude is also affected to some extent by the applied plate voltage and the values of the plate load resistors. However, the most effective method is to adjust the bias by means of  $R_{\mu}$  to obtain the desired amplitude. Actually,  $C_c$  and  $R_g$  operate essentially as grid leaks. When the reactance of the grid coupling capacitor is small in comparison with the grid leak resistance at the lowest operating frequency, the feedback is at a maximum, and the tank circuit can be connected in either the grid or plate circuits.

A typical curve showing plate voltage change versus external current flow between points A and B exhibits a continuous negative slope over most of its range, indicating typical negative resistance characteristics, as illustrated in the accompanying figure.



#### **Typical Current-Voltage Characteristics**

With the feedback action now understood, it can be clearly seen that when the LC tank is connected between points A and B it is alternately charged and discharged at its natural resonant frequency. Since the voltage on one plate is increasing when the voltage on the other tube plate is decreasing, points A and B are always of opposite potential. With a lowresistance tank circuit in place, the negative resistance action, produced by the tube operating at reduced conduction, effectively supplies energy to **the** tank circuit to overcome its positive resistance losses, so that continuous oscillation is maintained.

# Failure Analysis.

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No Output. Lack of plate voltage due to an increase in external load resistance or short-circuiting of the supply will cause lack of output. Since the negative resistance primarily depends on the amplifying action of the tube, insufficient amplification may also result in no output. Any change in the feedback circuit which reduces the feedback below the critical point can also stop oscillation. Since these conditions are generally produced only by an open- or shortcircuited component, resistance and voltage checks should quickly isolate the defective component. Tank circuit losses resulting from shorted turns or from increased resistance due to poor contacts (poor solder joints) can also be a contributing cause. Shorted turns will show up as a change in frequency if the circuit oscillates at all, and excessive resistance will cause reduced amplitude if it does not entirely stop oscillation.

**Reduced Output.** Excessive bias resistance will cause a reduction of amplitude. A reduction of applied plate voltage will also reduce the amplitude, but it can easily be detected by a voltage check. Changes in the feedback capacitors or the grid-leak resistors will also reduce the amplitude. Checking the capacitor with an in-circuit capacitor analyzer will quickly determine whether the capacitance is correct, and a resistance analysis will determine whether a grid-leak resistor has changed value. A decrease in the amplification factor of the tube with aging can also reduce the output.

**Incorrect Frequency or Instability.** Since the tank circuit is the primary frequency-determining element, major frequency change would indicate the possibility of shorted turns or a reduction of capacitance. The nature of the trouble is indicated by the direction of the frequency change. That is, an increase in frequency indicates shorted turns or a reduction of capacitance, and a decrease in frequency indicates an increase of capacitance, since the number of turns cannot increase.

Usually minor frequency changes, which may be produced by slight changes in plate voltage with changes in load or line voltage, can be compensated for by retuning the tank circuit. Since the stability of this circuit is normally better than that of either the dynatron or transitron, small frequency changes will require the use of a reliable secondary frequency standard to determine them. At the frequencies used, changes in tube element capacitance with temperature is rather unlikely to affect the frequency. Unstable operation might possibly be caused by a reduction of the tank capacitance to a minimal value, due to such trouble as defective bearing contacts in the tuning capacitor. This could produce a distorted waveshape and possibly result in the relaxation type of oscillation. Such operation would be evidenced by abrupt changes in current and voltage from one value to another, and the frequency would, no doubt, be out of the frequency range for which the circuit was designed.

#### PART 6-2. CRYSTAL OSCILLATORS

# **CRYSTAL OSCILLATORS**

#### General.

The crystal type of oscillator uses natural or synthetic nonconducting crystals excited by the piezoelectric effect and vibrating at or near their natural frequency to control the frequency of oscillation. The electrical excitation of the mechanical device at or near its fundamental, harmonic, or subharmonic frequency produces stable mechanical oscillations; these are converted into electrical impulses of the same frequency are are fed back into the oscillation circuit to sustain highly stable oscillations at the desired frequency of operation. The most popular, economical, and plentiful kind is the quartz crystal (shown in the following illustration), which in its natural (alpha) state only requires cutting, grinding, and polishing to size. The frequency of oscillation is determined mainly by the thickness (or length for very low frequencies) of the crystal slab. The crystal cannot be made to vibrate too strongly or it will shatter. Tourmaline crystals were once popular for the higher frequencies since they are more rugged and thicker for a given frequency. Because of the expense and scarcity of large-sized crystal prisms, and since tourmaline has a negative temperature coefficient which prevents a zero-temperature-coefficient cut from being obtained, tourmaiine crystals are not in common use today, although they may occasionally be encountered.





Natural Quartz Crystal, Showing the X, Y, and Z Axes

A quartz prism has three basic axes, X, Y, and Z. The Z axis is the optical axis, the Y axis is considered the mechanical axis, and the X axis is considered the electrical axis (see quartz crystal previously illustrated). No piezolectric effects are directly associated with the Z axis; an electric field applied in this direction produces no piezoelectric effect on the crystal, nor will a mechanical stress along the Z axis produce a difference of potential. A simple compressional or tensional mechanical stress applied along the Y axes will cause a change of polarization of the X axis, but not the Y axis; however, if a shearing or flexural strain is applied along the Y axis a change of polarization will occur. When the crystal is stretched along the X axis, a positive charge will appear on one end of the crystal, and when the crystal is compressed along the X asix, a negative charge will appear. Thus, piezoelectric effects are produced for either X- or Y-cut crystals, as shown in the accompanying illustration.

The piezoelectric effect is defined as that effect which produces a potential across the parallel faces of a crystal-line dielectric substance when pressure or torsional forces are applied between the faces, or, conversely, that effect which causes the crystal to distort itself when a voltage is applied between the faces. Thus, when alternating voltages are applied between the crystal faces, it will oscillate (vibrate mechanically) at a specific frequency, which is determined mainly by the thickness of the crystal.

When loosely coupled to a suitable oscillator circuit and excited at the proper frequency, the crystal will stabilize the frequency of oscillation. If the circuit is arranged to provide self-oscillation at the natural frequency of vibration of the crystal and will not oscillate without the crystal, it is a crystalcontrolled oscillator. Normally, a crystal has two frequencies or modes of operation: the resonant (fundamental) frequency, or series mode, and the anti-resonant frequency, or parallel mode. The series and parallel modes are similar to the equivalent types of resonance. In the series mode, the crystal presents a low impedance and provides a maximum of stability. In the parallel mode, it presents a high impedance (usually considered infinite), since the crystal is used as a high-Q inductor which is resonated with the crystal circuit shunt capacitance (including crystal and holder capacitances), to form a highly stable *parallel-resonant circuit* operating at the antiresonant frequency of the crystal. The arrtiresonant crystal frequency is always slightly higher than the natural, or series-resonant, frequency.

The variation with frequency of the series reactance  $(X_s)$  of a typical quartz crystal is shown qualitatively in the accompanying figure. The solid line represents the condition where the resistance R is equal to zero (which is only theoretically possible); the dotted line represents the true conditions where R has some finite value. Thus, where R is equal to zero, the series reactance is equal to zero at

$$f_{o} = \frac{1}{2\pi\sqrt{LC}}$$

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and changes from + infinity to – infinity at the frequency  $f_{po}$  (the solid line on the graph). When **R** is greater than zero, the dotted line indicates that the series crystal reactance has a finite maximum and minimum, and that it actually has a zero value at both  $f_s$  and  $f_p$ , the series- and parallel-resonance frequencies. For a resonably small **R**, the frequency difference between  $f_s$  and  $f_p$  is approximately the same as that between f. and  $f_{po}$  (they are quite close). In practice, the frequency difference between series and parallel resonance varies with the type of crystal and its cut. For example, a GT-cut quartz crystal can have a difference as low as 0.08 percent of the resonant frequency, and an AT-cut crystal can be as great as 2 percent.

the circuit is that specified in the Standard. For commercial crystals the schematic of the circuit used for calibration is generally supplied with the unit, or is otherwise specified. When used in a *nonstandard* circuit, the crystal will operate at a slightly different frequency from the calibration obtained in the standard circuit (±3 MHz maximum), depending upon the tolerance to which it is ground, the holder capacitance, and stray inductance and capacitance effects of wiring. The following figure shows the basic flexural vibra-

operation in a *standard* circuit. For MIL STD crystals

tion modes for fundamental, second overtone, third overtone, and fourth overtone operation of a crystal bar. These modes are used at low frequencies, where a bar producing lengthwise vibrations instead of a plate is used.



## Variation of Series Raactence of Crystal With Fraquancy

The series mode of operation is usually used for wave-filter circuits where a specific frequency is to be absorbed, or **for** *overtone* oscillators operating at high frequencies. A brief discussion of the basic principles of an overtone crystal is given in the next paragraph. The parallel mode is usually used in oscillator circuits where it is extremely high Q produces stable operation not normally possible with the ordinary inductor or LC tank circuit. As issued, the antiresonant (parallel-resonant) frequency is marked on the holder unless otherwise specified on the nameplate (overtone crystals are stamped at the overtone frequency). Crystal calibration and rating are for a specified shunt capacitance and holder, and for

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Crystal Flexural Vibration Diagrams for Lengthwise Vibrations

Part A of the figure shows the basic mode of operation as the fundamental frequency with the bar bending in the middle, and parts B, C, and D show second, third, and fourth overtone operation. In part B, note that the second harmonic flexing is of opposite direction, or phase, and that with a single plate extending the length of the crystal the bar cannot easily oscillate. On the other **hand**, the third overtone has the same motion or phase at both ends with the middle free to flex. In practice, the output on the third overtone is strong with a single plate, but the output of the second overtone, if not completely canceled, is so weak that it is unusuable (the bar has practically no piezoelectric effect). By plating a **single** 

electrode and then dissolving the plating between nodes, it is possible to get free flexing and piezolectric effect from even overtones, either separately through each set of plates, or by using one or the other of the end plates for excitation as shown in part D of the figure.

In the high-frequency crystal a different condition exists. Here the thickness shear mode is the mode of interest, and it is illustrated in the following figure. It is clearly seen that the vibrations in this mode are as if the crystal were squeezed with a shearing motion, distorting it somewhat as shown. Since this motion is essentially lateral, the crystal may be clamped at the edges, without being appreciably affected by the spring pressure between the plates; that is, the mechanical friction is negligible. When operating on an overtone, the high-frequency crystal appears to be formed of layers with the motions occurring in opposite directions. It should be understood, of course, that the illustrations are exaggerated to convey the idea. Basically, a crystal does not oscillate on one frequency; it has numerous nodes and modes, which can be affected by changes in temperature and excitation. For example, it is possible to heat the crystal by overexcitation, and cause it to change from a mode of **operation** at one temperature to another mode of operation at a higher temperature. It is also possible to cut and grind it so that it oscillates most vigorously on a particular frequency for *fundamental* crystals, and overtone frequency for overtone crystals.



**Thickness Shear Vibration Diagrams** 

Overtone operation is normally restricted to the odd harmonics on high-frequency thickness shear type crystals. In the circuit to be discussed, the crystal will operate only at the overtone frequency if ground for overtone operation. The circuit, however, will also operate at an overtone of a fundamental type crystal (which is some odd multiple of the fundamental frequency), but it will not operate at the fundamental frequency. It is possible to operate up to the third or fifth overtone with fundamental crystals and up to the ninth or higher overtone with overtone crystals.

As a matter of academic interest, it should be noted that crystals have been made which will operate on even harmonics, but this is the exception rather than the rule; only crystals which operate on odd overtones are of practical interest.

Since the overtone crystal is usually very thin, its ' mounting is very important. Therefore, it is usually plated and connected to wire electrodes in a sealed container. It is also very sensitive to surface imperfections; for example, scratches that would not affect the operation of the fundamental crystal can prevent operation of the overtone crystal. Therefore, extra care should be observed in handling and cleaning operations.

Generally speaking, the series-resonant crystal oscillator has greater frequency stability and can generate higher frequencies, whereas the parallelresonant type oscillator is more economical to construct, can operate over a wider frequency range (by substitution of different crystals), and can generate greater output. However, there are a number of exceptions to this general rule. The parallel- resonant oscillator is primarily used with fundamental-mode crystals at frequencies below 20 MHz. In conventional circuits of this type, the crystal must operate between its resonant (series-resonant) and antiresonant (parallel-resonant) frequencies, thereby behaving as an inductor. Under these conditions, the circuit will not oscillate if the crystal becomes defective and the oscillator is a true crystal-controlled type. Maximum stability is achieved with a low crystal drive and with operation in the class A to class B range. For maximum power output, the oscillator is operated class C. With normal voltages the electromechanical coupling in the parallel mode of operation tends to become too weak to sustain oscillation at the

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higher frequencies. This reduction in coupling, plus the shunting effects of tube and crystal capacitances, makes increased drive and plate voltage necessary to produce oscillation, thus leading to crystal fracture or instability; hence, it is impracticrd to use the parallel mode at the higher frequencies. It is possible though, by frequency multiplication in a number of subsequent stages, to obtain high-frequency operation with a parallel mode basic crystal.

The *series-resonant oscillator* is almost always used with *overtone* crystals. Because the output is lower than that of the parallel-resonant type, the operating range is restricted, and more parts are required. The series-resonant crystal oscillator is usually used only for high frequencies, or for low and medium frequencies where special design considerations make its use justifiable (mostly for frequency standards and laboratory and test equipment).

The inertia of the mechanical equivalent of the crystal oscillator provides a stable oscillatory action that is little affected by the varying parameters of the electron tube circuit (and for which crystal-controlled oscillators are noted) so that changes of tube capacitance or line voltage have little effect on the frequency of operation. In fact, the change of crystal dimensions with temperature usually has a greater effect. In this respect, the X-cut crystal has a negative temperature coefficient of 20 to 25 parts per million per degree centigrade (a 10"C rise in temperature of a 5000-kHz crystal produces a lowering in frequency of 1000 to 1250 Hz), and the Y-cut crystal has a positive temperature coefficient of 75 to 125 parts per million per degree centigrade. Thus, it can be understood that various crystal cuts provide different temperature coefficients, each suitable for different ranges of operation, with each different cut designed for zero temperature coefficient (see previous illustrations for typical cuts and typical temperaturefrequency variations) or as near thereto as possible. (The CT cut is the only one which covers a large range of temperatures.) For exact frequency operation, as needed in frequency standards or for special uses, temperature compensation is utilized, with the crystal ground and cut for a zero temperature coefficient over a temperature range easily sustained by the thermostatically controlled oven.

The effect of the crystal holder and the shape of the crystal have a slight effect on the resonant frequency, which varies with the cut. For example, a Y-cut crystal may be clamped at the edges without affecting operation (see accompanying illustration), whereas an X-cut crystal will oscillate only if all edges are free. Since the crystal is mounted between two metal plates and is a dielectric, there is an equivalent capacitance for the crystal determined by its dimensions, plus a capacitive effect due to the plates of the holder. Thus air gap holders, provided with a variable top plate adjustment, are sometimes used. Changing the effective capacitance by adjusting the gap changes the frequency of operation slightly (from 500 Hz to 3000 Hz maximum).



**Typical Mountings** 

The electrical equivalent circuit of the crystal and holder is illustrated in the following figure, to show

the parameters and components needed to stimulate a single quartz crystal. The inductance, L, is on the order of henries (for low-frequency crystals) with a Q of 100,000 or better. The series resistance, R, varies from unit to unit but is usually less than 500 ohms (the lower the better since it represents a loss of power). The capacitance of the crystal without a holder is represented by C and is on the order of a few picofarad. Where an air gap holder is used, the capacitance of the holder air gap is in series with the crystal, as indicated by  $C_g$ . The holder capacitance (with no air gap) appears in shunt with the crystal and also includes any wiring, stray, and distributed capacitance plus the grid interelectrode capacitance of the tube, all of which are lumped together as  $C_d$ . For the parallel-resonant mode of crystal operation, this capacitance is fixed at 32 picofarads for Military Standard crystals.



**Crystal Equivalent Circuit** 

The discussion of electron-tube crystal oscillators is also generally applicable to semiconductor crystal oscillators. However, the basic semiconductor is less frequency stable than an electron tube, mostly because of its inherent ability to act as a variable capacitor with a change of collector voltage. In an LC oscillator the *tank circuit* is the frequencydetermining and stabilizing element, but in the crystal oscillator, it is the *crystal* itself, because the crystal operates essentially as a parallel tuned tank or series tuned tank depending on the mode of operation. Therefore, whether semiconductors or electron tubes are used, the basic principles of operation of the resulting crystal oscillators are identical. The chief differences in operation are the effects on feedback and the circuitry used for the effective feedback control.

Like the self-excited semiconductor oscillator, the crystal-controlled semiconductor oscillator also has circuit configurations similar to those in the electrontube field, but none so well known by name as the Miller and Pierce circuits. Therefore, the circuit discussions are identified primarily from a functional standpoint rather than by name. By the principle of *duality*, most of the electron-tube circuit configurations have duals in the semiconductor field. Since — there are numerous circuit variations now in use and the state of the art in such that changes occur constantly, the circuits have been classified into three arbitrary groups and a circuit typical of each group will be discussed.

The first group, known as the transformer-coupled group, includes those oscillators using mutually coupled separate coils to provide feedback. The oscillators in this group have the advantage of extreme flexibility. They can be used in either CB, **CE**, or CC configurations, since polarities and impedances can be completely controlled by the number of turns and directions of the windings. The second group uses a capacitive voltage divider and is called the Colpitts-type crystal oscillator. The third group is the overtone group, which generally uses a tuned tank with a tapped coil in a Hartley type feedback arrangement operating at a desired harmonic or overtone. In any of these circuits, series or parallel resonance of the crystal may be employed. However, since the transistor is a low-impedance device, operating with relatively low voltage and high current, it conveniently lends itself to the use of series mode crystal operation, using only one stage instead of two stages as is necessary in the electron-tube circuit.

Because the transistor is basically a low-power device, it minimizes problems of heating and over excitation, which often cause crystal shattering in the power-tube oscillator. Thus, frequency changes due to thermal effects within the crystal are usually negligible, and ambient temperature changes are more important. For extreme stability, temperature compensation is necessary, particularly since the transistor itself is temperature sensitive and generally requires compensation. At normal room temperatures \_ (or lower), and with average low-temperature or zero-temperature coefficient crystals, the transistor

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crystal oscillator is stable enough for average use without compensation. At higher temperatures, compensation of the transistor, if not the crystal, is necessary in most cases.

Dc stabilization (biasing) methods as discussed in the Amplifier Section of this handbook are used in crystal oscillators, as well as self-excited oscillators, to insure that variations of emitter and collector voltages and currents do not cause parameter changes. The use of the form of stabilization generally results in more power being consumed in the biasing circuits than in the basic oscillator.

In considering output requirements, the load is generally in shunt with the crystal or the tuned tank circuit; as a result, increased power output usually affects the frequency stability by degrading the Q of the resonator or increasing the effective coupling impedance between crystal and feedback circuit. Or, as in **self-excited** oscillators, the less the output required, the more stable the frequency, and the less load changes affect the circuit. For all ordinary purposes, the good mechanical stability of the crystal resonator makes it almost free from the effects of load changes, particularly if the collector voltage is regulated.

Good crystal oscillator desigrr requires the use of low impedance coupling between the oscillator and resonator, the use of either resistance stabilization (in the form of series resistance in the emitter and collector circuits) or reactance stabilization, regulation of supply and bias voltages through the use of Zener diodes, the temperature control of both the transistor and the crystal.

In the following circuit discussions, the external feedback type of oscillator is discussed. However, it is possible to use the inherent negative resistance of a transistor to provide oscillation. In this case, a tuned or high-impedance circuit is employed in the baseemitter circuit, and the crystal provides a lowimpedance (series) feedback connection resembling the Miller and Pierce electron-tube circuits, as shown in the accompanying illustration. These types of oscillators (primarily used with point-contact transistors), however, are dependent entirely upon the transistor parameters since the feedback is entirely within the transistor and varies with each one. Such circuits are considered undesirable, except for special applications; they have been mentioned only for general information and will not be discussed further.





# GRID-CATHODE (MILLER) CRYSTAL OSCILLATOR. (ELECTRON TUBE)

#### Application.

The Miller crystal oscillator circuit is used to supply a constant-frequency sine-wave output at a relatively constant amplitude, usually within the r-f range. This circuit is used wherever a highly stable specific frequency is needed, such as the basic oscillator in a transmitter, receiver, frequency standard, or test equipment.

#### Characteristics.

Utilizes piezoelectric effect of a natural or synthetic crystal to control frequency of oscillation.

Crystal is connected between grid and cathode of an electron tube.

R-F feedback occurs only through grid-to-plate inter-electrode tube capacitance.

Operates normally with class B or C automatic self-bias, but may be operated class A or with combination freed and self-bias for special designs.

Frequency stability is excellent, with or without temperature compensation.

Output amplitude is relatively constant.

### Circuit Analysis.

General. The Miller-type crystal oscillator uses the crystal connected between the grid and cathode tube elements. Because of its popular usage, it is sometimes considered the basic crystal oscillator. However, the Pierce-type crystal oscillator which uses the crystal connected between the grid and anode tube elements, and is discussed later in this section, is also a basic type of crystal oscillator. In some other texts the Miller oscillator may be called the Pierce-Miller oscillator. However, to avoid confusion in this Handbook, the grid-cathode-connected crystal is called the Miller oscillator, while the grid-plate-comected crystal is called the Pierce oscillator. The Miller circuit is popularly used because, for a given amount of crystal excitation, it provides a greater output than any other circuit arrangement; the output is greater because the basic feedback occurs between the grid and plate of the electron tube, and not through the crystal. This also prevents the crystal from being subjected to sufficient strain to cause fracture of the crystrd, and the tube may be driven harder.

**Circuit Operation.** The basic Miller oscillator is shown in the accompanying illustration. The crystal is located between the grid and cathode, and grid-leak bias is obtained through Rl, with the shunt capacitance of the crystal, together with that of the holder, acting as the grid-leak capacitor. The tuned tank circuit, LC, is located in the plate-to+ **athode** circuit. As shown, the rfc and Cl form a conventional series plate-feed decoupling circuit, but the tank may be shunt-fed, if desired.



Basic Crystal (Miller) Oscillator

Crystal action in controlling oscillation can be explained as follows: Assume that the tank circuit in the basic oscillator is tuned to a higher frequency than the anti-resonant (parallel-resonant) crystal frequency, so that the plate circuit appears inductive. Assume also that filament and plate potentials are applied and the crystal is not vibrating. A positive voltage is present between plate and ground, and a negative voltage is present between grid and ground (due to contact potential). By piezoelectric action, the negative grid voltage will cause the crystal to be deformed slightly. Assume that a noise pulse occurs and causes the grid to go more negative, thus further deforming the crystal. The deforming of the crystal produces a piezoelectric action, increasing the charge on the grid in the same direction, and drives it further negative. When plate current cutoff is reached, the feedback becomes zero, and the accumulated grid voltage discharges through grid leak resistor R1. As the grid voltage is reduced, the deformation of the crystal is reduced, and the negative piezoelectric charge on the grid is also reduced by a corresponding positive induced piezoelectric voltage until plate current again flows. This cumulative action causes the crystal to vibrate mechanically near its parallelresonant frequency. Once started the vibrations continue and induce in the grid circuit an ac voltage of a frequency almost equal to the vibration frequency of the crystal. As long as the plate tank is tuned to present an inductive reactance, the proper phase for feedback is maintained. When the tank is tuned on the capacitive side of the frequency of oscillation (to a lower frequency), the phase of the crystal oscillation opposes the plate-to-grid feedback, and oscillation is reduced and eventually stopped. Tuning the tank circuit allows the feedback to be controlled from minimum to maximum with a corresponding output. To produce the proper phase relationship, tuning is approached from the high capacitance side of resonance. Plate current varies in a similar manner from a high value to a low value at the optimum point, then suddenly increases and abruptly reaches its normal static (non-oscillating) value as the seriesresonant frequency is approached. The action described, although slightly exaggerated for ease of understanding, happens very quickly. That is, the tube reaches its class B or C operating condition in one or two cycles of operation.

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Since the crystal is essentially the equivalent of a high-Q circuit, it resonates only over a very narrow range of frequencies (tuning is very sharp). Therefore, slight changes in tube parameters and supply voltages have a minimal effect, about 100 to 200 times less than in the conventional LC oscillator.

Biasing Considerations. In the basic Miller oscillator shown above, the bias is supplied by means of grid-leak action, as in the conventional LC feedback oscillator. Since the crystal represents a very high-Q circuit (a Q of 100 times or more than that of the conventional LC tank), it is evident that grid leak resistor RI effectively acts as a shunt for the voltage generated by the vibrating crystal. Therefore, an r-f choke is sometimes placed in series with the grid leak to reduce the load on the crystal and help it start oscillating more easily. When a bias battery replaces the grid leak and the series-connected r-f choke is also used, the grid operating point is freed by the battery bias, and the circuit can be adjusted for maximum power output, with minimum crystal excitation and good output waveform. The combination of battery bias and r-f choke, however, does not make for easy starting. The use of cathode bias, together with the r-f choke and with or without the grid resistor, normally provides the most effective starting, and is used where keyed oscillator operation is required (maximum stability dictates that keyed operation be avoided).

As the bias is increased, the crystal current increases, because more excitation is needed to swing the operation into the cutoff region and overcome the bias. The increased bias also increases the mechanical distortion of the crystal and causes it to vibrate harder. If driven excessively, the crystrd will shatter.

**Other Considerations.** The plate voltage applied to the crystal oscillator is limited to a value lower than that applied to the standard LC oscillator, because as the power increases with an increase of plate voltage, so does the feedback voltage, which in turn increases the current through the crystal. The increase of crystal current has two effects: (1) it may exceed the value where it causes the crystal to vibrate so strongly that it shatters; (2) since the temperature of the crystal depends upon the current flow through it among other things, unless the crystal has a zero temperature coefficient over a wide enough range, the frequency of operation will vary, either increasing or decreasing, depending upon whether the temperature coefficient is positive or negative.

Temperature changes external to the crystal will change the grid-to-plate interelectrode capacitance of the tube, and supply voltage changes will change the plate impedance and affect the frequency of operation. This frequency change occurs in parallelresonant csystal operation because either a **change** in the feedback capacitance or the plate load impedance will affect the phase shift in the feedback loop, and cause the crystal to operate at a frequency somewhat nearer to or farther from the antiresonant frequency, to **satisfy** the conditions for sustaining oscillation.

The Miller oscillator provides an average frequency deviation of approximately 1.5 times that of the Pierce oscillator (to be discussed later) and is therefore less stable than the latter circuit. On the other hand, it will give the same output (or slightly more) with only half the grid excitation and crystal current. Thus, with the same excitation, the Miller oscillator can supply twice the power of the Pierce oscillator and effectively obviate the need for an additional stage of amplification to bring its output up to the value needed to drive a following power amplifier. (The high output power largely accounts for the popularity of the Miller circuit and its almost universal used.) When used with a pentode, the Miller circuit provides maximum output with minimum crystal strain and excitation, and also greater stability (see the Electron-Coupled Crystal Oscillator circuit discussion given later in this section).

**Detailed Analysis.** The basic Miller oscillator is considered to be a variation of the tuned-grid, tuned-plate oscillator, in which the feedback occurs solely through the grid-plate interelectrode capacitance. The equivalent circuit of the Miller oscillator is shown below with bias and plate voltages omitted for simplicity. The crystal tank (tuned-grid) circuit is represented by  $L_1$ ,  $R_1$ ,  $C_3$ , tuned by interelectrode capacitance  $C_{gk}$ , and the plate tank by  $L_2$ ,  $R_2$ , tuned by variable capacitor  $C_2$ . The two circuits are coupled by the internal plate-grid capacitance,  $C_{pg}$ , for feedback purposes.

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**Basic Miller Equivalent Circuit** 

The plate circuit must appear inductive so that the correct phase shift will be produced in the developed r-f plate voltage to compensate for the effect of the resistance in the feedback loop; this resistance prevents the necessary 180-degree phase rotation of the equivalent generator voltage of the amplifier from occurring entirely in the feedback circuit. Since the load capacitance is a function of frequency, the Miller oscillator cannot be operated at more than one frequency and still present the same load capacitance to each crystal unit, unless provision is made for adjustment of the circuit parameters. Hence, the tuned tank circuit is required so that the plate circuit will appear inductive when the tank is tuned to the high-frequency side of crystal resonance.

Now examine the means by which the proper phase relationships between the grid and plate voltages are maintained to produce oscillation. In the conventionrd electron tube, the grid and plate voltages are always 180 degrees out of phase. When the grid voltage is positive, it causes the plate current to increase. Consequently, the voltage drop across the plate load impedance produces a negative-going output voltage. If this output were fed back to the grid, it would oppose the grid voltage and reduce or prevent any possible oscillation. To produce oscillation it is necessary to shift this phase another 180 degrees. Thus, a positive-going grid voltage must be reinforced and enhanced by a positive-going (feedback) voltage from the plate circuit. If the feedback voltage is **suffi**-\_\_ cient to replace any losses in the feedback circuit, continuous oscillation will occur. Now consider the crystal oscillator equivrdent circuit which follows:



#### **Crystal Oscillator Equivalent Circuit**

The equivalent generator voltage is  $-\mu E_g$ , where  $\mu$  is the amplificator factor of the tube and  $E_g$  is the excitation voltage on the grid.  $R_p$  is the plate resistance of the tube, and  $Z_p^{i_s-the}$ -plate impedance from plate to cathode, with  $Z_g$  as the grid impedance from grid to cathode. These impedances are reactive, and must always have the same sign for oscillation to be produced. Considering an ideal circuit with no feedback losses, the plate-to-grid impedance,  $Z_{p_s}$ , is the dominant impedance in the feedback circuit, and is always opposite in sign to  $Z_p$  and  $Z_g$ . If  $Z_p$  and  $Z_g$ are positive,  $Z_{p_s}$  is negative; thus the current,  $i_g$  leads  $e_p$  and  $-\mu E_g$  by 90 degrees. If  $Z_p$  and  $Z_g$  are negative,  $Z_{p_s}$  is positive; thus  $i_g$  lags  $e_p$  90 degrees. The voltage across  $Z_{pg}$ , of course, is in phase with  $e_p$  in both instances. Since  $Z_g$  is opposite to sign to  $Z_{p_s}$ ,  $e_s$ is thus opposite in sign to  $e_p$ , and the required phase reversal takes place. Note that  $i_g$  is first rotated in phase with respect to  $e_p$ ; next,  $e_g$  is rotated in the same direction with respect to  $i_g$ .

**ELECTRONIC CIRCUITS** 

In a practical circuit, the feedback losses cannot be zero; thus an exact 180-degree reversal cannot be obtained in the feedback circuit alone. This means that  $\mathbf{e}_{\mathbf{p}}$  must first be rotated by an amount exactly sufficient to make up the losses in the feedback circuit. To do this, the plate tank is tuned to a higher frequency than the antiresonant crystal frequency. Therefore, Z<sub>p</sub> appears as an inductive reactance, and  $\mathbf{e}_{\mathbf{p}}$  is rotated in a leading direction. The smaller the value of  $R_{p}$ , the more nearly will  $Z_{p}$  control the phase of  $\mathbf{i}_{\mathbf{p}}$ , and the more detuned must the tank circuit become in order to produce the necessary rotation of  $\mathbf{e}_{\mathbf{p}}$ . If practically all the resistance in the feedback arm is between the grid and the cathode, as is normally the case when  $\mathbf{e}_{\mathbf{g}}$  is developed directly across the crystal unit,  $e_p$  must be rotated through a larger angle than otherwise, thereby requiring the tank circuit to be detuned to a greater degree.

In a conventional parallel-resonant crystal oscillator having an ideal feedback arm, the frequency would be entirely determined by the resonance of the tank circuit; thus fluctuations in  $R_p$ , although effective in changing the activity, would not affect the frequency. In practical circuits, changes in both  $R_p$ and  $Z_p$  will slightly shift the phase of  $E_p$  and, consequently, the frequency. The basic amount of frequency shift is **fixed** by the crystal used, varying directly with the Q and the shunt capacitance of the crystal. This is the **reason** for using a standard value of 32 **picofarads** for crystrd capacitance; the Q depends upon crystal processing and composition, and thus varies somewhat.

In the Miller circuit, the maximum permissible voltage across the crystal unit is (k + 1) times the maximum voltage, where k is the gain of the stage and is equal to  $\mathbf{e_p}/\mathbf{e_g}$ , as shown in the crystal equivalent circuit. Theoretically, this gain can approach the mu of the tube as a limit when the load impedance,  $Z_{\text{L}}$ , is large as compared With the plate resistance,  $\mathbf{r_p}$  (as shown by the following simple electron tube amplifier equivalent circuit); this explains the large output obtainable from this circuit when used with hi-mu tubes.



**Electron Tube Amplifier Equivalent Circuit** 

When a pentode, instead of a triode, is used as the oscillator **tube**, it is usually necessary to insert a small feedback capacitance between plate and grid, because of the small value of interelectrode capacitance present in the pentode. The output waveform is also improved by using a tuned tank circuit with a low L/C ratio. Since the tuning must be such that the tank impedance appears inductive, the tank circuit provides an effectively high-Q plate load when the tank capacitor is set for the proper load capacitance.

#### Failure Analysis.

No Output. Since the crystal controls oscillation, the crystal will not oscillate and no output will be obtained if the crystal is removed, if poor or loose holder connections cause an open or high-resistance circuit, if the plate circuit is detuned sufficiently, or if no plate voltage is present because of open- or short-circuit conditions. When sustained arcing (caused by too high a crystal r-f excitation current) produces burnt spots on the holder or crystal, it will not oscillate until cleaned (this condition normally does not occur in pressure type holders, but may occur in unloaded or air gap holders). Navy policy is to return defective crystals to the crystal laboratory for repair. Do not attempt to clean crystals. An open r-f choke or a short-circuited plate bypass capacitor will remove plate voltage from the tube, and the

crystal will not oscillate. Poor soldered connections on the tank coil in a series-fed circuit will produce a similar result. An open-circuited grid RFC in a circuit using no grid or cathode bias resistor will open the grid circuit and prevent oscillation unless the crystal is defective and has a low resistance. Insufficient feedback capacitance between tube elements (most likely to be associated with pentodes) will cause the crystal to stop oscillating (This condition will not occur in an oscillator which has previously oscillated unless the tube becomes defective).

**Reduced Output.** Low "plate voltage, a detuned plate tank circuit, or a crystal of low activity will result in reduced output. An open-circuited tank capacitor will allow the circuit to act as an untuned plate oscillator and, if the feedback is not too greatly out-of-phase, may permit weak oscillation; this trouble may be easily located because the tuning of the tank will not affect the plate current, and the plate current will be high, near its normal nonoscillating value. Increased resistance in the feedback arm due to poorly soldered connections will cause less phase rotation and, if excessive, will result in weak oscillation or entirely prevent operation.

**Unstable Output.** Any instability as far as oscillation is concerned would be associated with the feedback circuit and the crystal. A defective crystal, due to a partial fracture, may cause instability of amplitude and frequency. A defect causing the output to change from one mode of crystal operation to another could also cause instability, but in most instances it would be easily discovered because it would also change the operating frequency. An intermittent open, short-circuited, or partially open bypass capacitor may also cause a similar condition, although it is more likely to result in either no output or reduced output.

**Incorrect Frequency.** Since frequency is primarily determined by the crystal and tank circuit tuning, either a defective crystal or tank circuit may cause a change of frequency. The most probable trouble would be a defective, burnt, dirty, or fractured crystal. Changes of frequency on the order of only a few cycles per second may be due to tank detuning or temperature effects; changes greater than a few cycles per second indicate a change of crystal parameters. Temperature variations are generally indicated by a slow change of frequency in one direction with an increase of temperatures; such variations may occur if the ambient temperature is above the range of

thermal compensation provided. A slight change in frequency, due to aging or a change in drive level, can normally be compensated for by a slight change or tank tuning; otherwise, the crystal must be replaced.

# GRID-PLATE (PIERCE) CRYSTAL OSCILLATOR (ELECTRON TUBE)

# Application.

The Pierce crystal oscillator circuit is used to supply approximatley a sine-wave output of relatively constant frequency, usually within (although not restricted to) the r-f range. This circuit is used whereever a specific frequency of extreme stability and of moderate power output is needed, such as the basic oscillator in multistage transmitters, test equipment, receiver-converters, etc. It is usually interchangeable with the Miller oscillator in low- and mediumfrequency applications, but it is not often used in high-frequency applications, mostly because of its low output.

# Characteristics.

Utilizes piezoelectric effect of a natural or synthetic crystal to control frequency of oscillation.

Crystal is connected between grid and plate (or any other element acting as an anode) of an electron tube.

Does not require an LC tank circuit for fundamental mode operation.

R-F feedback occurs only through crystal.

Operates normally with class B or C automatic self-bias, but may be operated class A or with combination freed and self-bias for special design.

Frequency stability is excellent, with or without temperature compensation.

Output amplitude is relatively constant.

#### Circuit Analysis.

**General.** The generalities applicable to the basic crystal oscillator in the discussion of the Miller circuit are also applicable to the Pierce circuit. The simplicity of the Pierce oscillator, with its lack of tuned plate tank and its ability to oscillate easily over a broad range of frequencies with different crystals, makes it popular for use in crystal calibrators, receivers, and test equipment, and in transmitters not requiring much drive. The Pierce circuit is sometimes considered as the inverse of the Miller circuit since it exhibits opposite effects. Thus, instead of operating

as an inductive reactance **as** the Miller circuit does, the Pierce circuit operates as a capacitive reactance (when a tank circuit is employed, it is always tuned for a lower frequency). The crystal excitation voltage for the Pierce is approximately half that permissible with the Miller circuit. The plate load of the Pierce oscillator is resistive and is usually large enough in vahre that minor fluctuations in the tube plate resistance have much less effect on the frequency of operation than in the Miller circuit. This is used to best advantage when a pentode is employed, since its inherently high plate resistance and low grid-plate capacitance permit a greater range of plate load with the use of an external capacitor to fix the amount of excitation.

Circuit Operation. The basic Pierce oscillator circuit is shown in the accompanying illustration. Conventional grid-leak bias is obtained through  $C_g$  and  $\mathbf{R}_{\mathbf{g}}$ , which operate as described previously in the Amplifier Section of this handbook, and in the LC Tickler Coil Oscillator Circuit discussion given previously in this section. The crystal, which is connected between grid and plate, offers a high Q. The inductive reactance of the crystal, together with the capacitive reactance of Cl (which consists of tube and stray wiring capacitance), provides the final phase rotation required to produce the 180-degree shift in the feedback voltage in order to sustain oscillation. The plate load is resistor R1. C2 is the conventional plate bypass capacitor used in series plate feed arrangements. The use of resistor RI in the plate circuit provides a relatively flat response over a wide range of frequencies, so that various crystals may be substituted for operation on other frequencies without any tuning being required. In some instances, however, when it is desired to operate on a single frequency or over a narrow range of frequencies, with increased output, an r-f choke is substituted for R1. This choke eliminates the dc power loss in the resistor and provides a high r-f impedance for proper operation; since the plate voltage is increased, the (resistor voltage drop is eliminated) output is also increased.



**Pierce Crystal Oscillator Circuits** 

Now consider one cycle of operation. Assume that crystal Y is at rest and that the circuit as illustrated above is inoperative, with no plate voltage applied. At rest, the crystal is unstressed and there is no charge on either plate. When the plate voltage is applied, since no bias exists initially, heavy plate and grid current flows. Simultaneously, the crystal is stressed by this plate potential, and a peizoelectric charge appears" across the crystal. The sudden shock of applied plate voltage causes the crystal to start oscillating at its parallel-resonant frequency. Assume also that the plate voltage stress induces a positive piezoelectric charge on the grid, which tends to increase plate current and grid current flow. The plate current quickly reaches saturation at some low plate voltage, caused by the drop through plate resistor R1. Meanwhile, grid current flow is producing a negative voltage drop across  $R_g$ , thus charging  $C_g$ . As the crystal vibrates in the opposite direction, it induces a negative charge which adds to the negative grid voltage produced by the charging of  $C_g$ . As a result, plate current is now reduced by the increasing grid bias, and the plate voltage rises. The rising plate voltage again induces a positive charge on the grid. The crystal now flexes in the opposite direction, and the plate voltage again induces a positive charge on the grid by piezoelectric effect. Grid current flow again tends to charge  $C_g$ , and the cycle is repeated.

For oscillations to occur, the crystal must be effectively synchronized in its vibration, so that the piezoelectric effect does not oppose oscillation by reducing the feedback between grid and plate. The proper phasing is accomplished by connection of the crystal between grid and plate. The inherently high Q of the crystal makes it act as a large inductor to shift the phase of the feedback voltage in the proper direction to cause oscillation. Capacitance Cl provides a ddi tionrd phase shift to complete the 1?30-degree rotation needed.

Bias **Considerations.** As in the conventional LC oscillator, grid-leak bias may be employed for selfbias and amplitude stabilization, but unlike the gridleak circuit in the Miller oscillator previously discussed, it usually employs a grid capacitor (CJ because the crystal is connected between grid and plate and cannot provide the necessary grid-leak capacitance.

During operation, grid bias is produced by the grid leak and capacitor combination of  $\mathbf{R_g}$ ,  $\mathbf{C_g}$ . As grid current is drawn the capacitor charges, and in the absence of grid current it discharges. After a few cycles of operation an equilibrium state is reached where the slight amount that leaks off during the negative cycle **just** equals the amount of charge during the positive cycle; thus a steady bias is maintained. This action is similar in all respects to that of the conventional grid leak in other forms of oscillator circuits.

Since the excitation in a Pierce oscillator is low, it is common to use a higher value of grid-leak resistance than in the Miller oscillator (grid bias is equal to  $I_g R_g$ ). Fixed bias can be used in place of grid-leak bias to stabilize the operating point; however, fixedbias operation normally requires that starting provisions be made, particularly if the bias voltage is at or below cutoff. When a power-type oscillator is required, a combination of cathode bias and grid-leak bias is sometimes employed. Use of the cathode bias provides a protective bias voltage in the absence of excitation and allows the use of a lower value of gridleak resistance. However, the use of the combination bias also reduces the starting sensitivity and may be objectionable for keyed oscillators.

**Other Considerations.** Although the Pierce oscillator is normally used without a plate tank circuit, this is not always so. Where the output waveform is important, use of a selective tuned circuit in the plate circuit minimizes the harmonic content in the output

and thus provides a purer waveform than is produced by a resistive plate load, which is not frequency responsive and provides a high harmonic content. Selection of the circuit with a resistor plate load for use in a crystal calibrator to supply harmonics of 200 to 300 times that of the fundamental proves particularly advantageous. On the other hand, when overtone operation is desired, the Pierce circuit *must* use a tuned tank circuit to select the desired overtone if a useful and practical output is to be obtained.

Since this circuit is a vigorous oscillator, it lends itself to use as a multifrequency oscillator which permits mumerous crystals to be switched into the circuit to obtain operation over a wide range of frequencies, as shown in the following illustration. A particular advantage of the Pierce oscillator is that, since **crystal** activity varies considerably from crystal to crystal, it will operate with a weak crystal as well as a strong one. **Since** the Pierce oscillator is normally operated at a low output than that of the Miller oscillator, an additional amplifier stage can bring the output up to the same level. Such operation can be accomplished conveniently by using a single dualtriode tube as oscillator and amplifier.



Multifrequency Crystal Oscillator with Plate Tank

Lack of a tuned output circuit sometimes causes difficulty when a crystal is used which has a strong overtone activity as compared with the fundamental, because the Pierce circuit tends to respond at the frequency of strongest activity. However, this is a fault of the crystal rather than the circuit, as a fundamental-ground crystal has its greatest activity at the fundamental frequency. Because the plate impedance is resistive and of a high order, fluctuations in the plate resistance of the tube (which are only a small percentage of the totrd plate resistance) because of varying supply voltages or loads have less effect on the output frequency, so that this circuit is basically more stable than the Miller type oscillator.

Because the crystal is in series with the feedback from plate to grid and has full plate voltage across it, caution must always be observed to keep the fixed plate voltage below that which could cause excessive feedback and produce shattering of the crystal, or a frequency change due to heating of the crystal.

**Circuit Modifications.** Some typical circuit modifications made to improve the operation of the Pierce circuit or to overcome an inherent defect as shown in the following illustrations and are accompanied by a brief explanation. There are many variations of the basic Pierce circuit, because as long as the crystal is connected between the grid and any element other than the cathode, the resulting oscillator is basically a Pierce circuit.

used, C3 is also eliminated). It might appear that, with no cathode choke and no plate load, the shunting effects of Cl and the power supply capacitor would effectively short-circuit the crystal output; however, since the output is taken directly between the crystal and ground, the shunting has little effect, and maximum crystal output is obtained.

The operation of this circuit is practically identical with that of the basic Pierce oscillator. Even though the schematic of the grounded-plate Pierce circuit shows that C2 prevents the dc plate voltage from straining the crystal, it does not prevent the plate voltage changes from appearing on the crystal. Furthermore, C2 is charged and discharged through the crystal capacitance. Therefore, the crystal is initially shocked into oscillation by the ac or r-f voltage changes occurring in the plate and grid circuits. Once oscillations are started, the operation is identical with that previously described for the basic circuit.

Another variation, using combination cathode and grid-leak bias, is shown in the following figure.



#### Grounded-Plate Pierce Circuit

The grounded-plate version of the Pierce circuit uses a capacitor, C2, to block the plate supply from the crystal and thus minimize the electrostatic strain on the crystal. Sometimes an r-f choke is placed in series with the cathode to reduce the shunting effect of Cl; however, this choke is unnecessary if the other components are properly chosen. The plate load resistor,  $R_t$ , may or may not be used (when it is not  $\begin{array}{c} C_{c} \\ C_{c} \\ C_{d} \\ C_{k} \\$ 

**Combination Bias Arrangement** 

In the circuit above,  $R_k$  is a low-value resistor (Say 200 ohms) and furnishes cathode bias, being bypassed by  $C_k$ . Grid-leak bias is supplied by  $R_g$  (resistance on the order of 100,000 ohms) and  $C_g$ . The grid capacitor is made variable to provide a slight amount of tuning for the crystal, in order to permit operation with crystals of different frequencies. Actually, it has the same effect as  $C_i$  in the basic Pierce circuit,

shown previously; that is, it provides the proper phasing for the predominantly inductive crystal to ensure oscillation. Capacitor C2 effectively reduces the strain on the crystal though it does not isolate it from the plate supply. In this respect, both this circuit and the preceding circuit show two variations of using a blocking capacitor in series with the crystal to reduce the crystal strain. This is done to protect the crystal; with a constant d-c potential applied to the crystal, it would be permanently strained in one direction, and could be shattered by the excessive strain produced when the oscillations are in the same direction as the applied plate voltage, causing it to vibrate greater in one direction than the other. In the circuit above, the plate load resistor is replaced by inductor L1 to avoid the d-c losses in a resistive load. The inductor also makes it desirable to have  $C_{\sigma}$  variable to compensate for the phase-shifting of LI (it is assumed that the distributed capacitance of L1 in this case does not tune the inductor to the frequency of oscillation). Resistor R1 is a voltage-dropping resistor which is used to reduce the plate supply voltage to the desired plate voltage level; it is not required if the correct voltage is provided by the power supply. Capacitor Cl is the conventional series-feed decoupling capacitor.

Another method of connecting the crystal to avoid the strain produced by the plate voltage is to ground the crystal directly and to ground the plate through a capacitor, as shown in the following illustration. With this arrangement, the cathode must operate above ground, and an r-f choke is used to provide the necessary isolation. Capacitor C3 effectively grounds the plate so that the crystal is connected between grid and plate, but is unstrained by the d-c supply potential Resistor R, and capacitor C2, together with RFC and  $\mathbf{R}_{\mathbf{k}}$ , provide combination grid-leak and cathode bias, and C 1 and C2 form a typical Colpitts type capacitive feedback voltage divider. Capacitor C<sub>1</sub>represents the total grid tuning capacitance (both the interelectrode and stray wiring) which is the effective tuning capacitance across the crystal (32 picofarads with MIL-STD types). In this case, it is clearly seen that the crystal acts as the tank circuit (see Ultraudion Oscillator equivalent circuit shown in the following illustration), but that it is shunted by the grid leak, which effectively reduces its Q. The output is taken from across the crystal through coupling capacitor Cc.



Grounded-Crystal Circuit Variation

Again, the circuit operation of the groundedcrystal stage illustrated above is practically identical with that of the basic Pierce oscillator previously described. The crystal is shocked-excited into vibration by the a-c plate and grid voltage changes. In addition, the capacitive voltage divider formed by Cl and C2 provides additional feedback to overcome the shunting effect on the crystal caused by grid leak  $R_g$ . Their value is such that the circuit will not oscillate with the crystal removed. Their use makes the circuit easier to start, and permits the use of crystals with much weaker activity than normal.

**Detailed Analysis.** The Pierce oscillator is considered to be the ultraudion version of the Colpitts <sup>-</sup> type of **L-C** oscillator circuit, with the crystal taking the place of the plate tank as illustrated in the accompanying illustrations.

The Pierce circuit operates at a frequency which places it on the inductive side of parallel resonance in the crystal. When a plate tank circuit is used, it is always tuned to a lower frequency to make it appear as a capacitive reactance. Thus, the crystal operates somewhere between its series- and parallel-resonant frequencies. The tube grid-plate interelectrode capacitance,  $C_{gp}$ , is in shunt with the crystal, and the effective tank tuning capacitance of the inductive crystal is

**ELECTRONIC CIRCUITS** 

the electrostatic crystal capacitance (represented by C in the Ultraudion equivalent illustration) in parallel with grid-plate tube capacitance  $C_{gk}$ , together with the series-parallel combination of grid+ athode capacitance,  $C_{gk}$ , and plate-cathode capacitance,  $C_{pk}$ (which includes the distributed wiring capacitances). For Military Standard crystals, this capacitance is always held to 32 picofarads total. Since the plate circuit is predominantly resistive, consisting of R<sub>1</sub> only, as shown in the Pierce equivalent circuit above, any small fluctuation in any of these capacitances is minimized; as a result, the circuit has a more stable frequency of operation than the Miller oscillator. Capacitor C, previously illustrated in the basic Pierce oscillator circuit, is usually inserted to ensure that the circuit will oscillate with many different types of crystals. Although the crystal (tank circuit L,R, C in the illustration) is comected between plate and grid, and feedback occurs through the crystal, it is the basic piezoelectric charge applied to the grid-cathode interelectrode capacitance,  $\mathbf{C}_{gk},$  that couples the crystal into the circuit electrically, as is evident from examination of the Pierce equivalent circuit shown previously. Because the plate circuit is predominantly resistive, small fluctuations in tube plate resistance due to changes in operating voltages are a smaller percentage of the over-all total plate resistance; therefore, greater frequency stability is obtained than in the tuned plate oscillator, in which plate resistance changes are a much greater percentage of the total load resistance. The higher plate resistance and lower grid-plate capacitance of the screen grid tube are particularly advantageous in the Pierce oscillator. Since the crystal is effectively the tank circuit and represents the highest impedance in the circuit, it is evident that the largest voltage is developed across the crystal, but it is limited by the maximum voltage and power dissipation that the crystal can withstand without shattering. Thus, the maximum output from this type of circuit is limited by the crystal powerhandling capability (area), rather than by circuit components. (Modem, 1/2-inch-square, crystals have only 1/4 the power-handing ability of the old l-inchsquare type.)







**Ultraudion Equivalent** Circuit

**Pierce Equivalent Circuit** 

Ultraudion Equivalent Circuit

Ultraudion as Compared with Pierce Crystal Equivalent Circuit

# Failure Analysis.

No Output. If the crystal is removed or if poor or defective holder connections cause an open (or highresistance) circuit, the crystal will not oscillate, and no output will be obtained. Also, if the plate load resistor is open or if a short circuit lowers the plate voltage sufficiently, the crystal will not oscillate. In the case of over+ xcitation when unloaded or air gap holders are used, the crystal may be burnt because of r-f arcs between the crystal and mounting plates, and it will not operate until cleaned. (Return crystal to repair center; do not attempt to clean it yourself.) In a poorly sealed holder, dust accumulation or moisture from condensation may also make crystal cleaning necessary. Normally, with the sealed, pressure-type holder, cleaning is unnecessary. An open series blocking capacitor will disconnect the crystal and stop operation.

Insufficient feedback capacitance between electron tube elements (most likely with pentodes) will prevent the crystal from oscillating, but this condition will not occur with a tube which has previously **oscillated** unless the tube becomes defective. An open grid resistor or capacitor will probably prevent operation, but may result in reduced output. Usually, only open-circuited or short-circuited conditions will prevent the circuit from operating. In the case of overtone operation, excessive detuning of the plate tank can cause a stoppage of oscillation, which will resume after the circuit is properly tuned.

Reduced Output. Since the Pierce crystal oscillator operates vigorously when excited, any reduction in output will result from lack of excitation or low plate voltage, rather than from high resistance or poorly soldered contacts. An open or shorted grid capacitor or grid-leak resistor will change the bias conditions and result in either reduced output or no output. When the grid-leak bias is combined with cathode bias, failure of the grid-leak bias will cause reduced output and perhaps hard starting. A dirty crystal may not oscillate at all or only weakly, and could be the cause of reduced output. With unsealed crystal holders a reduction in output, hard starting, or stoppage of oscillation was a signal for possible cleaning; however, with modern sealed holders the possibility of crystal contamination is not very likely, but should be kept in mind. (Return crystal to repair center; do not attempt to clean it yourself.)

**Unstable Output. Instability** may be due to an intermittent or poor (high-resistance) connection in the feedback circuit, but it is more likely to be due to a defective crystal which has been partially fractured by over-excitation. A crystal which normally operates satisfactorily in a tuned Miller oscillator may be defective and have a spurious frequency which is produced alternately with the desired frequency, when the crystal is used in a Pierce circuit, and thus cause an unstable output. Such a condition is evidenced by changes in frequency, due to erratic jumping from one frequency to the other.

**Incorrect Frequency.** Since the crystal frequency is primarily determined by its own constants, an incorrect frequency is probably the result of a change in the crystal itself or in the holder and associated wiring capacitances. Normally these changes are very small. If the crystal is not temperature-controlled, over-excitation can cause sufficient heating of the crystal to change the frequency; this condition is normally indicated by a continuous drift in one direction as the crystal is heated. A zero-temperaturecoefficient crystal operating within its range of compensation will not be affected by minor temperature changes. Since a tuning adjustment is usually not provided, a noticeable change in crystal frequency indicates a circuit or crystal parameter change which should be checked. With the few parts concerned in this type of oscillator, it should not be too difficult to determine the defective component. Crystal or tube aging effects may also cause a change in frequency, which would be indicated by a slow change over a long time. Any decrease in grid circuit resistance may cause an increase in frequency, and an increase in the grid resistance due to high-resistance contacts may decrease the frequency. Cleaning the crystal sometimes restores it to its normal frequency of operation. However, do not attempt this yourself. Return it to the repair center. Actual aging of the crystal may cause a change of frequency, which is not correctable except by grinding or plating (at the repair center) to restore the proper thickness. Such aging usually does not occur quickly, but is cumulative over a long period of time. It should be noted that frequency is based upon time and that time is controlled astronomically and does vary in very minute parts. Thus, primary frequency standards are only accurate to 2 or 3 parts per 100 million for short

time operation, but this accuracy decreases as the time interval is lengthened. Therefore, crystal frequencies should not be expected to be absolutely accurate. However, they should be as accurate as their rated tolerance, and should normally require a stable secondary frequency standard to determine their error. Where crystal-controlled receiving and transmitting frequencies are involved, it may sometimes be suspected that either one or the other is in error when, in fact, both could be in error.

# ELECTRON-COUPLED CRYSTAL OSCILLATOR (ELECTRON TUBE)

#### Application.

The electron<oupled crystal oscillator is used almost universally to provide an approximate sine wave rf output over the low-, medium, and high-frequency rf ranges. It utilizes a screen grid or pentode tube to provide extreme stability and greater output than is possible with a basic triode-crystal oscillator, and is widely used in transmitters, receivers, test equipment, and other equipments which require crystal frequency control. Its widest application is for frequency **multiplication** in the plate circuit.

### Characteristics.

Utilizes piezoelectric effect of a natural or synthetic crystal to control frequency of oscillation.

Uses electron coupling to the load to reduce strain on crystal, to minimize load variations, and to provide extra stability.

Normally operates with automatic self-bias and class C, but may be operated with combination fixed and self-bias and class A or B for special design purposes.

Frequency stability is better than frequency stability of triode crystal oscillator, and power output is also greater.

Output waveform is a relatively constant amplitude sine wave, but if output is primary consideration it may be a distorted sine wave.

Uses a tuned plate tank for harmonic operation.

# **Circuit Analysis.**

**General.** The discussion on the Electron<oupled LC Oscillator given earlier in this Section is generally applicable to this circuit. The basic crystal-controlled

circuit employs either a Miller or Pierce oscillator which utilizes the screen grid of a tetrode or pentode tube as the anode. Either grounded-cathode or grounded-plate circuits may be used, with the grounded cathode being used mostly with a basic Miller oscillator, and the grounded plate being used mostly with the basic Pierce oscillator. The basic Miller oscillator is usually used for single-frequency operation, and always incorporates a tuned tank circuit. The Pierce oscillator is used where a number of frequencies are to be covered by changing of crystals, with no tuning adjustment being provided; however, plate tuning is required if harmonic operation (frequency multiplication) is desired.

Circuit Operation. A typical electron-coupled Pierce type oscillator is shown schematically in the following illustration. The grounded-plate version of the basic circuit is used to minimize the electrostatic strain on the crystal. The illustration shows a pentode tube rather than a tetrode because better electron coupling, or looser coupling, between load and crystal oscillator is possible because of the effect of the suppressor element. The looser coupling results from the fact that the screen grid completely surrounds the control grid and effectively isolates it from the plate circuit, and from the fact that the suppressor, if grounded or properly biased, minimized capacitance coupling between screen and plate. Thus, the coupling between oscillator and load circuit is provided by the electron stream alone, and any reflected load changes have negligible effects. Although the circuit shown may at first glance appear to be a Miller oscillator, it can be seen that the cathode is effectively above ground and that the oscillator plate (the screen grid) is grounded for ac by capacitor C4; hence, the crystal is connected (as in the typical Pierce circuit) between grid and plate (screen). This type of comection prevents the supply voltage from placing permanent electrostatic strain on the crystal, ans is preferred for that reason.

I n the schematic, the suppressor is shown grounded through C5, and it is held effectively at zero bias with respect to the plate by its connection to B+ through R2 (an internally connected suppressor type tube should **not** be used in this circuit). Thus, by construction, the grid is effectively shielded from the plate, and the coupling effects of plate-cathode capacitance are therefore reduced. Since the oscillator plate (the screen) is grounded, the RFC is used to keep the cathode above ground for rf. The output is

taken from across plate load resistor  $R_{I}$  through capacitive coupling. Actually, the plate load can be an r-f choke or a tuned LC circuit when the circuit is operating on the fundamental frequency. When it is desired to double or triple the frequency, it is necessary to tune the plate circuit to the desired harmonic, or overtone, for maximum output. Combination freed-bias (from voltage divider  $R_1$  and  $R_k$ ) and selfbias (from  $\mathbf{R}_{\mathbf{k}}$ ) is used to stabilize the circuit against frequency changes caused by bias variations because the excitation changes for various crystals and frequencies of operation. Therefore, with a fixed oscillator anode (screen) voltage which is relatively unaffected by load variations caused by supply changes or tuning, plus a stable operating point established by the fixed bias, usually only temperature effects need be considered with evaluating the short-time frequency stability of the circuit. In a typical circuit of this type, changes in resistor values of 20% result in a frequency change of only 1 part per million (ppm), and capacitance changes of up to 10% produce frequency changes of less than 8 ppm, whereas changes in temperature of the crystal and other circuit parts produce frequency changes as high as 35 ppm per degree centigrade above ambient room temperature.



Grounded-Plate Pierce Electron-Coupled Oscillator

Use of a crystal with a better temperature coefficient and with temperature control can reduce this to a short-time frequency variation of only 2 to 3 ppm.

Electron coupling also affords greater output because the circuit employs the equivalent of two tubes, the triode section operating as a low-voltage oscillator with low grid excitation and low crystal strain, and the pentode section operating as an amplifier loosely coupled to the oscillator by the electron stream between screen and plate. Thus, the amplifier portion may be operated at high voltages, which if used in the basic oscillator would normally shatter the crystal; consequently, the power output from the amplifier plate is greater than that from the basic unit. The over-all result is a stable crystal oscillator operating with crystal excitation on the order of a few milliwatts and providing a power output on the order of watts. In most cases, the output is equal to or greater than the output available from the basic Miller type power oscillator, and has a greater frequency stability.

Now consider one cycle of operation. When B+ voltage is applied, the fixed cathode bias produced by voltage divider R1 and R<sub>1</sub> permits a heavy flow of screen and plate current. Since the plate is isolated from the oscillator portion of the circuit by the zerobiased suppressor grid, and is coupled only through the electron stream in the tube, plate current flow has no effect on oscillator operation. Since the grid is located between cathode and screen, electrons will be intercepted from the space current, causing a small grid current to flow. Grid current flow through  $R_{\sigma}$ develops a negative bias on the grid, which tends to charge Cl. Thus  $R_g$  and C 1 act as a grid leak and grid capacitor, respectively. Simultaneously, the crystal is shock-excited into oscillation by the changing grid and screen voltages. The crystal vibrations produce a piezoelectric voltage across the crystal, and between grid and ground (the screen is bypassed by C4, and acts as the oscillator anode). The crystal oscillates in synchronism with the grid and plate voltage changes. On the negative swing, the crystal-generated voltage adds to increase the bias and reduce the anode (screen) current. On the positive half-cycle, the total bias is decreased. Consequently, the screen current (and thus the electron stream through the tube from cathode to plate) is caused to alternately decrease and increase at the oscillator frequency. The capacitive voltage divider (C2 and C3), connected between grid

and cathode, and plate and cathode, fixes the minimum amount of feedback. Thus it helps stabilize the circuit and overcome any tendency toward hard starting because of the initial fixed cathode bias. The cathode is kept above ground potential by the rfc; otherwise, oscillation would not occur (screen and cathode would be short-circuited for r-f).

The electron stream between screen and plate varies in accordance with the crystal oscillation frequency. Since the plate voltage and current are greater than the screen voltage and current, the r-f output voltage developed across load resistor  $R_L$  is larger than the voltage developed across the crystal. Since the plate is isolated from the screen and oscillator section of the tube by the zero suppressor bias, any load variations or supply voltage changes have little or no effect on the oscillator. Thus, a more stable and higher-powered output is taken from the plate circuit of the electron-coupled crystal oscillator. The dc power dissipated in  $R_L$ , of course, appears as a loss of efficiency, since it is wasted in heating the resistor.

The accompanying circuit schematic shows the Miller version of the electron+ **oupled** crystal oscillator. Although this circuit requires two tank circuits, it has the advantage that doubling (or tripling) can be accomplished in the final tank, while the basic stability of the fundamental frequency is retained.



Miller Electron-Coupled Oscillator

Note that in this circuit the cathode is grounded; hence, even though the suppressor is shown externally connected, an internally connected suppressor type of tube could be used without impairing the electron coupling. Actually the second tank circuit (C4, L2) need not be used; a resistor or RFC could be used in its place, but tuning the plate circuit ensures that the proper output frequency is selected and reduces the harmonic content to a minimum. From the illustration it is evident that the basic oscillator circuit is connected between the cathode, grid, and screen (anode) tube elements, just as in the Pierce electron-coupled oscillator. However, the crystal is connected between grid and cathode, and the operation of the oscillator is as descrived previously (see Grid-Cathode (Miller) Crystal Oscillator discussion at the beginning of this section of the Handbook). Electrostatic isolation of the plate by means of the grounded suppressor limits the coupling to the electron stream alone, thus providing increased stability because of freedom from the effects of load variations on the oscillator.

#### Failure Analysis.

No Output. Lack of output from this type of oscillator may be due to a fault in either the oscillator portion or the amplifier portion of the circuit. Thus, it should first be determined whether the crystal oscillator is oscillating, using the failure analysis discussion of the basic oscillator as a guide. If the oscillator is operating, then lack of output is caused by lack of plate voltage due to an open or short-circuited condition. An open suppressor bypass capacitor may cause a virtual cathode to be formed between screen and plate and reduce the output almost completely. A defective electron tube may oscillate, but have insufficient emission to supply any appreciable output in the plate circuit. Usually, the cause of a no output condition can be quickly localized to a particular part by a resistance check of the few components involved.

**Reduced Output.** This condition is more likely than no output and may be caused by low plate voltage, by the presence of a high resistance in the plate load circuit due to poor connections, particularly in tuned tank circuits, and by excessive bias. Shortcircuiting of the cathode bias voltage-dropping resistor connected to the supply source ( $R_i$  in Pierce circuit) would produce cutoff-bias conditions and the

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tube would not operate; an increase in this resistance would minimize the fixed bias and allow the cathode bias alone to prevail, causing class A operation of the plate section, so that reduced output and a reduction of harmonic content would occur.

**Incorrect Frequency.** Since the frequency is determined by crystal operation, any basic frequency changes will occur solely in the oscillator section, except when the circuit employs a plate output tank. If this tank becomes tuned (either accidentally or by component faihrre) to the wrong harmonic of the crystal frequency, the circuit" will produce an output of incorrect frequency. Any changes caused by load fluctuations or supply voltage fluctuations will be so small that they may go unnoticed unless precision measuring equipment is available.

# OVERTONE CATHODE-COUPLED (BUTLER) CRYSTAL OSCILLATOR (ELECTRON TUBE)

#### Application.

The cathode-coupled (Butler) crystal oscillator is used primarily for overtone crystal operation on high or very high radio frequencies. It is used in receivers, transmitters, test equipment, and other equipment which requires the use of a stable crystal-controlled high-frequency oscillator.

#### Characteristics.

Uses an overtone crystal to provide operation on frequencies which are not integral harmonics of the fundamental crystal frequency.

Employs two triodes coupled by the crystal operating all series resonance.

Normally operates class A, but may be operated class C for greater power output.

Provides an approximate sine-wave output of relatively constant amplitude.

#### Circuit Analysis.

**General.** The Butler cathode-coupled two-stage oscillator is one of the most widely used of the *series mode* oscillators because of its simplicity, versatility, frequency stability, and comparatively high reliability. This circuit seems to be the least critical to

design and adjust for operation at a given harmonic with any type crystal. The balanced circuit, plus the fact that twin triodes within a single envelope can be used, contributes to a saving in space and cost and provides for short leads. The cathode-coupled circuit can also be used for operation on the lower radio frequencies, provided that the resistance of the crystal unit is not greater than a few hundred ohms. However, the power output is less than that of the Miller circuit for the same crystal power, and the broad bandwidth of operation without tuning as provided by the Pierce circuit is not possible.

At series resonance, the crystal element appears as a resistance, so that in the normal circuit it can be short-circuited or replaced with a comparable resistor without stopping oscillations. Although circuit operation of the series-mode oscillator is less complicated than that of the parallel-mode oscillator, the circuit design becomes increasingly critical at the high frequencies and higher overtones. It is vitally important to keep stray capacitance at a minimum, and all leads must be as short as possible to eliminate unwanted resonances. It is sometimes necessary to nullify the shunt crystal capacitance by paralleling the crystal with an inductor which is antiresonant with the shunt crystal capacitance at the operating frequency. It may also be desireable to connect a capacitor in series with the crystal to tune out the stray inductance of the crystal leads, and tuned output circuits must be provided to select the proper overtone. For maximum frequency stability, the effective resistance of the circuit facing the crystal unit should be as small as possible. At the higher frequencies, stray capacitances limit the impedances obtainable with tuned circuits, making them more selective, and more effective in influencing the frequency and increasing instability. -

Usually, the output is taken from the plate or cathode of either tube. Sometimes the cathode follower is a pentode tube utilizing the cathode, screen, and grid elements as the basic oscillator, which is electron+ **oupled** to the plate load. This provides greater stability and affords the possibility of tuning the plate circuit to a higher harmonic.

**Circuit Operation.** The accompanying illustration shows the basic cathode+ **oupled** circuit using triodes.



**Basic Cathode-Coupled Crystal Oscillator** 

Tube V2 is a grounded-grid amplifier whose output is fed back to the cathode (input circuit) through cathode follower VI and the series-connected crystal. Cathode bias is supplied through RI and R2, and VI Normally conducts more heavily than V2 (both tubes are identical triodes). The feedback voltage is coupled capacitively through  $C_f$  to the grid of V1, and grid resistor  $R_g$  provides conventional grid-drive bias which varies with the excitation supplied. When operated class A, no grid current is drawn, and there is no grid-drive bias produced across  $R_g$ . In this instance  $R_g$  acts solely as the grid-return resistor in a conventional R-C coupling network, and the bias is produced by R1 alone. In class C operation, grid current is drawn, and grid drive bias is produced exactly as in the conventional r-f driven amplifier. In this case, the total bias consists of the self-bias produced through cathode resistor RI, plus the drive bias in the grid circuit. The tuned tank circuit ( $L_1$  and  $C_3$ ) in the plate of V2 offers maximum impedance at the frequency to which it is tuned. The maximum output voltage (and feedback) occurs at this point, neglecting crystal operation. The crystal is normally an overtone type, and is ground for maximum acitvity at the overtone frequency (fundamental frequency crystals are occasionally used with this circuit, but this fact does not materially affect the theory of operation of the circuit). Usually the circuit will oscillate when the

crystal is short-circuited or replaced with an equivalent resistance, operating at the frequency of the tank circuit. Resistor R4 and capacitor C2 are a conventional plate voltage dropping and decoupling network provided for series plate feed of V2. Resistor R3 and Cl perform a similar function for V1 with sufficient capacitance to effectively ground the plate of VI for rf at the frequency of operation. The output is taken from the plate of V2 through coupling capacitor Cc, but it **could** also be taken from VI or from the cathode without materially changing operation.

Off resonance, the crystal exhibits a high resistance, which effectively reduces the feedback and prevents oscillation. At the series resonant frequency, the crystal exhibits a low resistance and the circuit oscillates vigorously. Since the gain of the cathode follower tube cannot exceed unity, there is partial control of excitation because V] cannot amplify the feedback from V2; as a result, greater feedback is provided for a weak crystal than for a strong crystal. This action enhances overtone operation, since the strongest oscillations are at the fundamental frequency, with successively weaker oscillations being obtained as the numerical value of the overtone increases.

Now consider one cycle of operation. When plate voltage is applied to V1 and V2, since no initial bias exists there is a heavy flow of plate current. The flow of plate current through RI and R2 produces a cathode bias on each tube which reduces the plate current flow. At the same time, the flow of plate current in V1 through plate resistor R3 drops the supply voltage to the proper value. Any a-c variations in voltage produced by changing plate current through R3 are bypassed to ground by C 1, and tube V1 operates as a cathode follower. The initial flow of current shockexcites the crystal so that it vibrates at its seriesresonant frequency. At resonance the drystal appears as a low value of resistance, while on either side of resonance it appears as a large resistance. In the offresonance, high-resistance state, the crystal attenuates any feedback from the plate of V2 through V1 and thus prevents oscillation. In the series-resonant state, the low crystal resistance permits practically all the feedback to be applied across R2. (The crystal resistance, R, and the cathode bias resistor, R2, form a voltage divider connected in parallel with R 1.)

With the crystal oscillating on the positive halfcycle, assume that a positive voltage produced by

piezoelectric effect is applied to R2, and increases the bias. The plate current of V2, therefore, is reduced. Since the output voltage is developed across the impedance of the plate tank circuit, a reduction in plate current produces less drop across the tank, and the plate voltage approaches the source (goes positive). Thus, a positive-going voltage is fed through coupling capacitor  $C_r$  to the grid of VI. The positive-swinging grid voltage produces an increase of plate current in V1 and a positive increase across cathode bias resistor RI. Since the gain through cathode follower V1 is less than unity, no amplification of the signal occurs through V1. Sufficient feedback occurs, however, to replace the small circuit losses; thus oscillation is sustained.

On the negative half-cycle of operation the crystal develops a negative voltage which is applied to R2. The bias on V2 is thus reduced, and the plate current increases. The output voltage produced across the tank circuit is now negative-going, and is fed back to the grid of V1 to reduce plate current flow. Consequently, the voltage drop across cathode resistor R1 is decreased, and a negative-going voltage is applied through the crystal to maintain oscillation.

Although it might appear that the feedback voltage is such as to oppose crystal oscillation, it must be realized that this circuit will operate with the crystal removed if the equivalent resistance (or an ohmic connection) is placed across the crystal terminals. Operation without the crystal, however, is never as stable as with the crystal.

**Circuit Modifications.** As with all other oscillator circuits, there are numerous variations of the basic circuit. A typical variation is shown in the accompanying illustration.



Frequency Multiplying Overtone Oscillator

This circuit is essentially identical with the basic Butler overtone **oscillator**, except for the insertion of a tuned tank in the plate circuit of the cathode follower. Thus, the cathode follower stage becomes a cathode-coupled stage. The effect on over-all operation is to make available an output which can be tuned to a harmonic of the overtone frequency (instead of being bypassed to ground as in the basic circuit) and provide effective frequency multiplication.

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As far as the basic oscillator is concerned, the operation is the same as described for the basic circuit. Although amplification occurs in the plate circuit, since the plate load of VI is tuned to a different frequency, any coupling effects through the plate-grid capacitance do not affect the basic frequency.

An electron-coupled version is formed by connecting VI as a conventional pentode amplifier which is resistance-capacitance coupled to V2, with the frequency multiplying tank in the plate circuit of Vl, shown in the following illustration. This version is identical with the basic Butler circuit except that the screen of V1 acts as the anode of the cathodefollower stage. With the screen ac grounded through C2 and the suppressor tied back to the cathode, the plate is coupled solely through the electron stream between screen and plate. The rfc and C3 form a conventional series plate feed decoupling network, and  $\mathbf{R}_{sc}$  is the screen resistor. All other components function as in the basic oscillator. In this circuit VI is usually operated class C, and has a high applied plate voltage. Thus, the plate output is considerably higher than in the previous triode type of frequencymultiplying circuit, and the tank L and C may be tuned to either the second or third harmonic of the oscillator frequency. The basic tank  $C_4L_2$  is tuned to the fundamental frequency.



**Electron-Coupled Overtone Oscillator** 

Although other versions of the Butler circuit exist, they are similar to the versions described above. The identifying feature of the Butler oscillator is the connection of the crystal as a series feedback arm between two cathode-coupled stages. Overtone oscillators with grid-cathode or grid-plate comected crystals are special versions of the Miller and Pierce circuits.

## Failure Analysis.

No Output. A primary cause of inoperation is a defective crystal or poor holder connections; the crystal and holder resistance should not exceed 500 ohms for proper operation. Since two tubes are involved, a defective tube is also a possible cause of no output. An open circuit in the feedback path, either in the coupling capacitor or crystal holder, will rdso stop operation. In addition, short-circuited components will cause the affected tube to draw greater than normal current and stop oscillation. A short circuit across the crystal will not stop oscillation; depending on the design, it is possible for oscillation to continue at the tank frequency. Lack of supply voltage will also stop operation, but low supply voltage will primarily affect only the output amplitude. Because of the few components involved, a quick voltage and resistance check should isolate the defective part. If all parts and voltages appear normal, the cause of trouble is in the crystal, or the tank tuning capacitor is shorted or tuned' to the wrong frequency. If other crystals oscillate in the circuit, cleaning the defective crystal may restore activity. (Return crystal to repair activity for cleaning.)

Low or Unstable Output. Excessive bias on one or both tubes will reduce the output. Such bias could be caused by heavy current through the cathode bias resistors due to defective tubes or short-circuited components in the plate circuits. A change in the grid-leak resistor and in the coupling capacitor constants may cause blocking and motorboating or intermittent operation. A weak or dirty crystal may also produce low output. (Replace the crystal.) Too low or too hi&a plate voltage can cause instability.

**Incorrect Frequency.** The series-resonant **crystal** oscillator is the most stable kind. Therefore, a change in frequency will probably be due to crystal caused effects. Cleaning the **crystal** should restore proper operation (cleaning to be done only at repair activity); if not, there is a possibility that changes in stray capacitance between cathode and ground (perhaps

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from a change of lead dress) have caused a slight detuning. Though operation at a frequency above the series frequency can occur, it is rather unlikely because the limits of series resonance do not permit as much detuning as those of parallel resonance.

# OVERTONE CRYSTAL OSCILLATOR (SEMICONDUCTOR)

### Application.

The overtone type oscillator is used as an oscillator in receivers, converters, frequency synthesizers, and test equipment, and as an exciter in low-power transmitters. Its use is restricted to the high-frequency ranges (above 20 mc) where fundamental mode crystal operation is not practicable.

#### Characteristics.

Uses piezoelectric effect of a quartz crystal operating on an odd overtone to provide stable high-frequency oscillations.

Has at least one tuned circuit at overtone frequency and may have two; it is never untuned.

Operates class C to help produce harmonic operation.

Regenerative feedback is usually provided through a tapped coil (Hartley principle).

Always operates as a crystal-controlled oscillator to avoid spurious frequencies.

# **Circuit Analysis.**

**General.** Overtone circuits are basically of two types: one type uses. a crystal which is ground for fundamental frequency operation, and the other uses an overtone ground crystal. Since the circuits that use overtone crystals are usually designed for specific types of crystals, this discussion will be restricted to circuits which can use either type of crystal.

Basically, the overtone crystal oscillator uses an inductive form of feedback, but it is not necessarily limited to that type. It just happens that at the present state of the art the inductive type is more popular. Although the tapped coil is primarily a Hartley feedback arrangement, it is closely similar to the tickler coil feedback arrangement. At the frequencies used, the tighter coupling of the Hartley arrangement and the ease of construction make it a more natural choice.

For operation of an overtone circuit, regenerative feedback must be provided to assist in the starting of

oscillations, but the feedback must not be strong enough to cause free-running oscillations. Most circuits of this type are first designed to operate as freerunning oscillators, and the amount of feedback is then reduced by the manufacturer until only the crystal controls the oscillation. Oscillation is usually vigorous, and the output at the third and fifth overtones (using a fundamental crystal) is almost as large as that at the fundamental; at higher overtones, the output falls off quickly. The output depends so much upon the processing and manufacture of the crystal, however, that the highest overtone at which practical operation is possible is rather indefinite. Designers have produced satisfactory outputs on overtones above the 11th, but mostly with patented circuits and special components. In the transistor crystal oscillator, for example, overtone operation has been improved by the use of special transistors designed to minimize phase shift at very high frequencies. When this type of transistor is combined with an overtone crystal or a specially processed crystal, the results equal or surpass similar electron-circuit tube achievements, but the power output is less.

Circuit Operation. A simplified schematic of the basic overtone semiconductor oscillator, using the common-emitter configuration, is shown in the accompanying illustration, It can be seen at a glance that this is the basic Hartley Oscillator circuit with a crystal in series with the emitter feedback connection. For simplicity, bias and supply arrangements are not shown. It is assumed that the collector is reversebiased and the base forward-biased, and that PNP junction transistors are used. The crystal can be either a fundamental or an overtone type. The tank circuit, consisting of L and C, is tuned to the overtone frequency desired. The principle of operation is exactly the same as the principle of operation of the basic Hartley oscillator, with proper polarity of feedback between the oppositely polarized collector and base being obtained by means of the tapped-coil arrangement. The difference in operation is primarily in the amount of feedback, with the portion of the coil between emitter and base producing just enough feedback for easy starting with the crystal in place. In the self-excited Hartley, the tap on the inductor is normally at or near the center of the coil, the number of turns between emitter and base being selected for strong and stable feedback. In the overtone oscillator the feedback coil usually consists of a few turns (no more than 3 or 4), approximately 10% of the total

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number of tank coil ,turns. This corresponds very closely to the tickler coil oscillator arrangement used in regenerative receivers, where it is possible to just produce oscillation with the regeneration control all the way on. The overtone oscillator regeneration, however, is adjusted so that the circuit will not quite oscillate with the crystal out of the circuit, but will produce, strong stable oscillation at the crystal frequency only (no spurious self-oscillation) with the crystal in the circuit.



**Simplified Overtone Circuit** 

A typical overtone circuit with bias and supply connections is shown in the accompanying figure. The common-emitter circuit is used, and the crystal is in series with the feedback loop as in the basic schematic. Voltage divider bias is obtained through R1 and  $R_B$ , and the base resistor is bypassed for rf by C<sub>B</sub>. An unbypassed emitter swamping resistor (R<sub>e</sub>) is used for stabilization. Actually, at the high frequencies used, it is probable that the distributed capacitance (shown in dotted lines in the schematic) across R<sub>E</sub> and the resistor itself form a grid-leak bias arrangement for amplitude control, and that some designs may use a bypassed emitter. In the circuit shown, the collector supply is bypassed by  $C_2$ , with the RFC connected in series between the negative collector supply terminal and  $L_1$ , as a conventional series-feed arrangement.



**Overtone Crystal Oscillator** 

Now consider one cycle of operation. When collector voltage is applied, bias divider  $R_{I}R_{B}$  supplies class A bias to the base, and collector current flows as in a conventional amplifier circuit. Assume that a noise pulse causes the collector current to increase and that a voltage is developed across the tank circuit  $(L_1C_1)$ , which offers a high impedance at the resonant frequency. The voltage developed across the tank is positive with respect to the supply end. The crystal offers a low-impedance path to the emitter at series resonance. With the crystal connected near the supply end, that electrode is negative, and the electrode connected to the emitter is positive. Therefore, a voltage exists across the crystal, causing it to deform in one direction. The base of the transistor is connected for rf through  $C_B$  and  $C_2$  to the supply end of the tank coil. Thus the tank is essentially connected between collector and base, with the emitter

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tapped to the tank. This is equivalent to a typical Hartley-type of grounded-base feedback oscillator, which is effective only for the series-resonant frequency of the crystal. On either side of resonance the increasing crystal impedance quickly stops any feedback, and the circuit will not oscillate.

As the noise pulse causes the collector current to increase, the feedback to the emitter is positive and the base end of the coil becomes more negative. Both the more negative base and the more positive emitter cause an increase in forward bias and a greater I. The collector current increases until the supply voltage bottoms (cannot go any lower). During this time the tank capacitor, Cl, is charging. The tank circuit now discharges and the polarity of the base and emitter feedback voltages change to produce a reduced forward bias and a lowering of Ic. This causes the collector voltage to rise toward the supply voltage and become more negative. At the same time, since the polarity across the crystal changes, the crystal flexes in the opposite direction as a result of piezoelectric action. This state of operation continues until the collector current cutoff point is reached; at this time a small flow of  $I_{CEO}$  (reverse current) occurs, but it has no effect on operation other than to cause a lowering of efficiency. When the feedback ceases, the crystal flexes back toward its original resting condition and generates a piezoelectric charge that starts collector current flowing again, and the cycle repeats. Emitter resistor  $\mathbf{R}_{\mathbf{E}}$  is affected only by the dc current flow, and operates as a simple swamping resistor for thermal compensation and stabilization. In some circuits the distributed capacitance across R<sub>n</sub> is considered to cause it to operate in a manner similar to that of the electron-tube grid leak. That is, the charge across this capacitance holds the circuit inoperative until the charge leaks off; too large a capacitance will effectively short the crystal. The capacitance is shown in dotted lines in the above illustration because it is not considered necessary for operation. The output is taken capacitively through Ccc between collector and ground, or, if desired, by inductive coupling to the tank circuit. The tank circuit is tuned to the overtone

frequency, and the crystal also operates at the overtone frequency.

Circuit Variations. A typical practical operating design used in a satellite transmitter is shown in the following figure. The grounded-base arrangement is employed. The tank circuit is connected between base and collector, and the emitter is connected to the tap on the tank coil through the series crystal and capacitor  $C_4$ . Separate bias supplies are shown because their use provides almost perfect stabilization; however, voltage divider bias can be used if only one supply is available. RFC 1, in the emitter circuit, is used to keep the emitter above ground, and  $R_{_{\rm E}}$ ,  $\_$ which is bypassed by C 1, provides emitter swamping (and also controls output). Forward bias is applied between the emitter and base by battery supply  $V_{\text{\tiny EF}}$ . Conventional series collector feed is provided through RFC2, which is bypassed for rf by C6. The output is taken capacitively from the collector through C7, which is adjustable to match of 50-ohm load. Capacitor C3 is a base blocking and coupling capacitor (it also affords a reduced tuning range for C2); it connects the base to the tank circuit for rf and isolates it from the dc collector supply; otherwise, the supply would be short-circuited. Capacitor C5 is a trimmer across the tank, and variable capacitor C2 is the tank tuning capacitor. Feedback is obtained from the tap on L2, and applied through C4 and the series crystal to the emitter. In this circuit, C4 adjusts the phasing to ensure feedback of the proper polarity and to compensate for the phase lag in the transistor at high frequencies. It acts as a variable regeneration control to permit the use of various types of crystals and replacement transistors. Inductor L1 is used to resonate out the effects of excessive crystal holder shunt capacitance at the frequency of operation. At the series resonant overtone the crystal offers minimum inpedance and supplies maximum feedback from collector to emitter. Although the emitter and collector are of the same polairty, or phase, L2 and C4 provide the necessary phase rotation to insure oscillation, since the feedback is taken from the end of the tank coil opposite the collector.

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Grounded-Base Overtone Oscillator

Now consider one cycle of operation. When voltage is applied, the fixed bias, which is less than cutoff, permits collector current to flow. Assume a noise pulse which causes an increased I<sub>c</sub>. Since the tank is connected between collector and base, with the emitter tapped onto the coil, it is basically a Hartley-type oscillator. In this circuit L2 acts as an autoformer, with the emitter-base turns coupled to the emittercollector turns. However, the emitter is not directly connected to the coil; it is connected through crystal Y and capacitor C4 in series. The capacitor offers only a small capacitive reactance to the oscillator frequency; the crystal offers a high impedance offfrequency, and a low inpedance at its series-resonant frequency. Thus, feedback is permitted at the seriesresonant frequency, but is stopped on either side of resonance.

The increased collector current induces a feedback pulse in the emitter-base portion of L2 in a direction which increases the forward bias, and, hence, the collector current. Capacitor C4 provides a phase-delay adjustment which can reduce the amount of feedback (or increase it, as desired) so that various types of crystals and transistors may be used. For the purpose of this discussion it carI be considered as shortcircuited, since it is only a production type or compensator, and is not necessary to basic operation. Since the feedback action is regenerative, the collector current continues to increase until the collector saturates and no further change can occur. At this

time the crystal, which was initially deformed by the feedback potential between the emitter and collector, flexes in the opposite direction. The polarity across the crystal produced by piezoelectric action also reverses, and the flow of emitter current is reduced; since the collector current is also reduced, and the feedback is regenerative, the collector is driven to cutoff. At this time a small  $I_{CEO}$  (reverse current) flows, but it has no effect on operation except to lower the over-all efficiency. At this time C 1, which was charging during the conduction period, now discharges through  $\mathbf{R}_{\mathbf{F}}$ . When the bias drops below cutoff, current again flows and the cycle repeats. During the reducing collector current period, the crystal is flexed in a direction opposite the initially caused deformation, and at cutoff it again flexes oppositely and resumes its original shape. Thus, the crystal is caused to oscillate, and in oscillating it provides a lowimpedance path for the feedback. Because of its inherent stability, the crystal controls the frequency by permitting operation to occur at only one frequency. The basic tank circuit (L2, C2) functions in the conventional manner to supply energy during the nonconducting half-cycle, so that the negative output alternation may be completed. This flywheel effect provides a sine-wave output through coupling capacitor C7, instead of the distorted pulse which otherwise would occur.

The circuit described above is capable of providing an output of 15 to 30 milliwatts at an efficiency of 30 to 35% to a 50-ohm load, and a maximum output of 100 milliwatts at an efficiency of 40 to 45%. Under constant loading and controlled temperature, the short time frequency stability is plus or minus one part in one hundred million. The circuit uses a fifth overtone crystal operating on 108 MHz and a diffused base transistor.

### Failure Analysis.

No Output. Loss of output will result from the loss of bias or supply voltage due to an open- or short-circuited component; this condition is easily determined by checking for the presence of voltage. An incorrectly tuned tank circuit will prevent the crystal from operating and could result from shorted turns or a shorted tuning capacitor, but at low voltages used, troubles of this kind are rather unlikely with ordinary components. In miniaturized circuits where the current-carrying capacity is low, there is the possibility that an overload can cause the inductor or leads to open. It is important, therefore, to use a meter having a very low full-scale current requirement, preferably in the microampere region. A VTVM is preferable to the standard **20,000-ohms**per-volt meter, although with care both can be used interchangeably. A check of the forward and reverse resistances of the transistor will quickly determine whether it is at fault. Because of the low potentials involved, a high resistance or poor soldered joint can introduce excessive resistance and stop the circuit from oscillating. A defective, partially fractured, or dirty crystal can also prevent oscillation.

Reduced Output. Since the output amplitude is primarily controlled by the emitter swamping resistor and bias voltage, changes in these parameters can cause reduced output. Opening of the bias ground return resistor will place a higher bias voltage on the transistor, and, depending upon the internal base-toemitter resistance of the transistor, oscillations may be blocked entirely or hard starting may result. Hard starting is usually a clear indication of a dirty or defective crystal. The value of the emitter resistance and its bypass capacitor will determine the output amplitude to a great extent; therefore, a partially shorted capacitor or increased resistance in the emitter circuit will reduce the amplitude. Such troubles can be easily located by making a resistance check of the few components in the circuit. A reduction of output may also be caused by short circuiting of the transistor elements or by mismatching of the transistor due to a change in the circuit values. This too is easily checked by making a resistance analysis and by measuring the forward and reverse resistances of the transistor. A combination of low foreward resistance and high reverse resistance indicates a satisfactory transistor. If the forward resistance is high or nearly the same value as the reverse resistance, the transistor is defective. If both resistances are zero, the transistor is shortcircuited.

**Incorrect Frequency. Since the** crystal is the frequency-determining component, an appreciable change in frequency indicates a defect or a change in the crystal, except where the tuned circuit is actually tuned to another overtone. Under normal conditions it is practically impossible to tune the tank to **reso**nance at a different overtone unless the tank circuit components are defective. Although a fimdamentrd type crystal will operate within the tolerances marked on the holder, it must be kept in mind that for overtone generation of the crystal the tolerances will be

multiplied by the overtone number (1, 2, 3, etc); hence, the tolerance range at the overtone will be much larger. Oscillation will occur, not over the entire range of tolerances, but at a specific frequency within the range. On the other hand, overtone crystals are rated for their actual tolerance at the overtone frequency; therefore, operation outside this range indicates a defective crystal or spurious oscillations. As a result of changes in circuit components and transistor parameters with age, excessive feedback may occur at certain resonant frequencies and produce free-running oscillations. Usually these sig- nals have a much rougher or more raspy sound and are less stable than the controlled oscillations. In the case where calibration capacitors or feedback controls are provided, it is normal for them to control the frequency slightly so as to permit the crystal to be operated on its exact frequency. When no controls are provided, a change in ambient temperature can place the crystal in another class of temperature compensation and change the actual overtone frequency. The temperature tolerance is shown on the crystal holder and is stan&rd for a MIL type crystal. Minute imperfections or partial fractures can also cause the crystal to operate at another frequency. Return defective or dirty crystals to the crystal repair activity for servicing.

# TICKER COIL FE EOBACK CRYSTAL OSCILLATOR (SEMICONDUCTOR)

#### Application.

This oscillator is used to provide an approximate sine-wave r-f output that is extremely stable under crystal control, and operable over the low-, medium-, and high-frequency r-f ranges. It is universally used where a transistor oscillator is required; typical applications are local oscillators in receivers and heterodyne converters and oscillators in test equipment.

#### Characteristics.

Uses piezoelectric effect of a quartz crystal to control oscillator frequency.

Uses a feedback (tickler) coil to provide the proper phasing for oscillation and control of regeneration.

Usually has the primary coil tuned to the crystal fundamental frequency, with the secondary (tickler) \_\_\_\_\_\_ coil being untuned. Not restricted to a particular configuration; may be **CE**, **CB**, or CC as desired.

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Can operate on a fundamental, harmonic, or overtone frequency if proper tuned circuit and crystal are selected.

# **Circuit Analysis.**

General. The semiconductor tickler coil crystal oscillator is basicrdly a transformer< oupled oscillator. It may be either tuned or untuned, or partially tuned by stray and distributed capacitance. When the circuit is tuned, it is possible to operate the crystal on a fundamental frequency and tune the tank circuit to a harmonic, thus obtaining frequency multiplication, or to use overtone crystals for the same result. Like the electron-tube crystal oscillator, it may be crystalstabilized or crystal-controlled. However, this circuit discussion will be restricted to the crystal-controlled type of oscillator. The ease of obtaining the feedback and controlling it makes the tickler coil feedback circuit popular. Since the polarity of each coil with respect to the other is easily changed by reversing the windings (at the time of manufacture), and since the coupling may be made tight by spacing the coils close together, or loose by spacing them apart, it is easy to obtain the proper amount and polarity (or phasing) of feedback. With the use of inductors to provide a low dc resistance, the dc resistance losses are minimized, and more output is obtained from the circuit with better efficiency. Since the transistor requires a certain amount of stabilization against bias and temperature changes, it is usually necessary to add stabilization resistors or reactance.

The use of a crystal operating in the seriesresonant mode is more common with transistor oscillators because the crystal serves as a convenient means of permitting feedback at the resonant frequency by virtue of its low impedance series resonant circuit, but offers a hi@ impedance to feedback at all other frequencies. When placed in series with the feedback loop, the crystal effectively controls the feedback. Use of the parallel-resonant mode is not obviated, however, since sufficient flexibility exists in the placement of the crystal in either the collector, base, or emitter circuit to match circuit conditions. For example, since the common-base circuit has a high output impedance, the crystal could be placed in the collector-to-base (or ground) loop and operated effectively as a parallel resonator. Actually, the possibility of three different basic circuit configurations,

together with placement of the crystal in either the input or output circuits, poses a problem in the circuit discussion because of the numerous circuit variations that can be formed. The discussion will, therefore, be limited to a typical circuit considered most likely to represent present day use. It is assumed that placement of the crystal or choice of circuit configuration does not materially change the basic stability, but that it does affect the power output and efficiency of operation to some extent.

Since the **crystal** power oscillator practically does not exist in the semiconductor field (most outputs are on the order of milliwatts), the crystal is not restricted in its placement by power requirements or heat dissipation, but it may be placed so as to **pro**duce the best performance.

Circuit Operation. The basic common-emitter circuit configuration for the tickler coil crystal oscillator is shown in the accompanying illustration. For the sake of simplicity, bias and collector supply voltages are not shown and will be discussed later. It is assumed that forward bias is applied to the emitter-base junction and that reverse bias is applied to the collector junction. The discussion is based upon the use of PNP junction transistors, although the basic principles also apply to point-contact transistors. From the discussion of basic transistor operation in the Amplifier Section of this Handbook, it will be recalled that the inputs and outputs of the common-collector and common-base circuits are of the same polarity, or inphase, and that those of the common-emitter circuit are oppositely polarized, or out-of-phase. Thus, to ob tain the desired polarity (phase) of feedback in the common-emitter circuit, the two coils are oppositely phased. In the illustration the feedback is from collector to base, with the input being considered from base to emitter. Since the polarity is reversed in the transistor collector circuit, the tickler coil, L2, is connected so that it also reversed the polarity, and feedback through the crystal (series-mode operation) arrives at the base properly polarized (or phased) to produce regeneration. Removal of the crystal, which is in series with the feedback loop, will prevent the occurrence of feedback; therefore, the circuit will not oscillate with the crystal removed. However, the circuit is normally designed to operate as a self-excited oscillator with the crystal short< ircuited.



Basic Tickler Coil Crystal Oscillator, Common-Emitter Circuit

The operation of the circuit is similar to the operation of the electron-tube Tickler Coil LC Oscillator described earlier in this section. When the oscillator is switched on, current flows through the transistor as determined by the biasing circuit. Initial noise or thermal variations (initial current) produce a feedback voltage from collector to base through the crystal which is in-phase with the initial noise pulse. Thus, as the emitter current increases, the collector current also increases, and additional feedback through L1 and L2 further increases the emitter current, until it reaches saturation (or the collector voltage bottoms) and can no longer increase. When the current stops changing, the induced feedback voltage is reduced until there is no longer any voltage fed back into the base-emitter circuit. At this time, the collapsing field around the tank and tickler coils induces a reverse voltage into the base-emitter circuit which causes a decrease in the emitter current, and hence a decrease in the collector current. The decreasing current then induces a reverse voltage into the feedback loop, driving the emitter current to zero or cutoff. At this time a small reverse saturation current (I<sub>CEO</sub>) flows, representing a loss of efficiency, but having no other effect on circuit operation. The discharge of tank capacitor C through  $L_1$  then causes the voltage applied to the base-emitter circuit to rise from a reverse-bias value through zero to a forwardbias value. Emitter and collector currents flow, and the previous action repeats itself, resulting in sustained oscillations.

While this oscillatory action is going on, **piezo**electric action occurs in the crystal; that is, as the feedback voltage is increased, the strain on the crystal is increased with maximum strain (and maximum crystal deformation) occurring at the peak of the

cycle. Upon reversal of the feedback voltage the strain on the crystal is reduced; since the crystal is now changing shape back to its original form, a piezoelectric charge (potential) is produced across the crystal. This charge is opposite to that which produced the deformation of the crystal. For example, if the original charge which caused the deformation was positive, the crystal causes a negative potential to appear across itself when the strain is released. This potential is in the direction of the feedback (decreasing) so that alternate positive and negative charges are induced across the crystal as it vibrates. These potentials add to the feedback voltage; as a result, the crystal enhances the feedback, and the feedback increases the strength of the mechanical vibrations.

Since the feedback and **piezoelectric** action are regenerative the transistor quickly reaches its saturation and cutoff points. By correctly proportioning the turns and coupling between the tank circuit and the tickler coil, it is easy to obtain the proper amount of feedback, although with the low potentials involved there is no danger of fracturing the crystal as in the vacuum-tube oscillator. The amount of feedback is adjusted to produce maximum stability. The crystal current is not nearly as great as the crystal current in an electron-tube circuit; in fact, the total transistor collector current is **usually** less (depending on the type of transistor) than the electron-tube crystal current.

Although the collector-emitter capacitance of the transistor is in parallel with the tank circuit, the use of a low L/C ratio (high-C) produces effective capacitance swamping so that variations in the collector supply voltage, which produce a change in this capacitance, have a minimal effect. For good stabilization, a Zener diode placed across the supply provides excellent regulation. By careful design, the short time stability of the semiconductor crystal oscillator can be made as high as 2 or 3 parts in ten million, which is better than the stability of the equivalent electron tube oscillator. The power output is, of course, very small; however, this fact increases the stability since any change of output load or tuning results in a smaller over-all change. **Thus,** the frequency stability of the circuit is less affected by load changes than that of the electron-tube (triode) circuit. The output may be taken from the emitter or collector, or even the base circuit, by means of either capacitive or inductive coupling.

The circuit operates at the natural or fundamental frequency of the crystal for the series mode; hence, the operating frequency is slightly lower than the tank resonant frequency. It is also possible to operate this circuit using the parallel mode (antiresonant operation) of the crystal by proper choice of circuit parameters. Although the crystal offers a high impedance at the antiresonant frequency, sufficient feedback can be obtained to sustain oscillation in this mode. In this case, the crystal appears as a high-Q inductor which is tuned by the total shunt capacitance (self, stray, and distributed) across it, and the tank is tuned to a higher frequency. This type of operation is particularly applicable to the higher frequencies, where the shunt crystal capacitance is appreciable. For operation in the parallel mode, the frequency stability is slightly degraded and the output is slightly less than the output in the series mode. Both types of operation are in use.

**Bias and Stabilization.** In practical circuits, bias and stabilization are usually combined. Bias is usually provided by a freed voltage divider (RI and RB), as shown in the accompanying illustration of a typical tickler coil crystal oscillator. Note that the base in this case is not bypassed for rf, although in some circuits it may be. When it is unbypassed, there is presumed to be a slight amount of degeneration, which enhances the circuit stability.



**Tickler Coil Tuned Collector Crystal Oscillator** 

Collector resistor  $R_C$  serves two purposes, to drop the collector voltage and to provide resistance stabilization. If the dc losses are serious, the resistor can sometimes be replaced by an r-f choke. Emitter resis-

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tor  $\mathbf{R}_{\mathbf{F}}$ , which is bypassed by capacitor  $C_2$ , provides the major stabilization by emitter swamping action, as explained in the Amplifier Section of this handbook. The tank circuit consists of L1 tuned by Cl, with tickler coil L2 untuned, and is coupled to the collector through C3 in a shunt-feed arrangement. The crystal is in series with the feedback circuit with the tickler coil polarized so as to produce regenerative feedback. In similar circuits of this type using the tuned base configuration, the crystal is connected directly between base and collector, and the tank between base and ground. In this case, the operation is identical to the operation of the circuit described above; however, the feedback is basically controlled by the capacitance between base and collector, thus making the circuit more suitable for the parallel mode of operation.

Taking the output across the tank through capacitor Ccc effectively places the load across the tank and reduces the operating Q, but provides a good waveform because of the smoothing action of the tank circuit. Without the tank circuit, since the oscillations consist essentially of clipped pulses, the waveform would be quite distorted unless the circuit were operated with class A bias. The class of operation is usually class C, with the emitter resistor and capacitor  $R_{E}C2$ ) acting similar to a grid leak in tube oscillators. In the circuit shown, the initial bias is class A for easy starting, with the operating bias being determined by the values of the emitter RC circuit. With large values of capacitance for C2 fixed bias alone is provided, but as the capacitance is reduced to a small value the self-bias developed across  $\mathbf{R}_{\mathbf{F}}$  increases.

#### Failure Analysis.

**No Output.** In addition to failure of the transistor, no collector voltage or excessive bias can cause a nooutput condition. Transistor failure is not very likely under normal conditions, and the transistor should be replaced only after all other checks have been made. Lack of collector voltage can occur because of opening of the series collector resistor or short-circuiting of the tank coupling capacitor, which-provides a path to ground through the tank inductor. An open emitter resistor will also cause lack of output. A shortcircuited coupling capacitor will place the output load directly across the tank and could change the resonant frequency sufficiently to prevent feedback at the crystal frequency, and stop oscillation.

Reduced Output. Although aging of the crystal may cause a change in the resonant frequency, it is more likely to cause a drop in output as the crystal becomes less active. This condition usually results in a gradual change over a long period of time and is most easily determined by comparison with a known good crystal operating in the same circuit. A change in bias conditions or in the emitter RC network will probably reduce the output because of the amplitude regulating effects of these components. This condition could be caused by an increase in emitter resistance value or by a reduction in capacitance of the emitter bypass capacitor. These conditions are most likely to occur in miniaturized circuits where new component fabrication techniques have not been perfected. If a resistance analysis shows all circuit values normal, there is a possibility that the crystal is dirty and requires cleaning; however, this condition is not very likely to occur in sealed holders, and certainly will not occur in evacuated holders. Do not attempt to clean the crystal yourself. Return it to the crystal laboratory for servicing.

Incorrect or Unstable Frequency. Placement of the equipment so that it is subjected to a change in ambient temperature will cause a change in frequency if the change is not within the range of the temperature characteristic for which the crystal is cut. Likewise, small capacitance changes in the crystal circuit (particularly when the crystal is operated in the parallel resonant mode) will cause slight changes in frequency. Detuning of the tank circuit, if sufficient, may cause the crystal to pop in and out of oscillation with a slight change in frequency. Voltage variations will produce a change in the collector capacitance and cause a slight change in the operating frequency. At very low audio frequencies or at high frequencies near  $f_{max}$ , phase shift within the transistor csused by transit time effects may produce instabilities (such trouble is not encountered in properly designed circuits). In the crystal-stabilized circuit (which is not used in the Navy), changes in component values may cause oscillation at undesired frequencies outside the range of the crystal, but in the crystal-controlled circuit they cannot cause this effect because the circuit can oscillate only over a very narrow range about the resonant frequency or at an overtone. This can easily be determined by observing whether the circuit oscillates with the crystal removed. If the crystal is shortcircuited, it is possible in the series mode of operation for the circuit to oscillate at the tank frequency, but

not in the parallel mode of operation. Frequency changes can sometimes be traced to a defective crystal, but more often to varying supply voltages. If a crystal oven is used to keep the crystal temperature stabilized, a defective oven may cause the frequency to shift.

# COLPITTS CRYSTAL OSCILLATOR (SEMICONDUCTOR)

# Application.

The Colpitts crystal oscillator is used mostly at the higher radio frequencies as an extremely stable oscillater in receivers, transmitters, and test equipment. However, it may also be used at low and medium radio frequencies.

#### Characteristics.

Uses piezoelectric effect of a quartz crystal to control oscillator frequency.

Feedback is provided through a capacitive voltage divider arrangement, which is usually external, but it may be provided through the transistor element capacitances.

Normally does not use a tuned tank circuit adjusted to the crystal fundamental frequency (but may employ a tuned circuit for special applications).

Operates class C if waveform is not important, and class A if good waveform is required.

#### Circuit Analysis.

General. The Colpitts type crystal oscillator is usually used at the higher radio frequencies where the difficulty of tightly coupling the inductors in the inductive feedback circuits makes their use problematical. Actually, the so-called Colpitts version uses three basic feedback arrangements: (1) the external capacitive voltage divider with the crystal in shunt (or in series) (2) the crystal acting as a high-Q tank inductor similar to that in an ultraudion arrangement (parallel mode operation), and (3) the in-phase capacitive feedback arrangement, which is included in the Colpitts group solely becuase the feedback is capacitive (some texts may not regard this as a Colpitts, but as a special type of its own). The basic circuits of each type are shown in the accompanying illustration. Part A of the illustration employs the common-emitter configuration, and parts B and C use the commonbase configuration. Actually, the circuit of part B can also use the CE configuration, and that of part C can use only the CB or CC arrangements, because the

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feedback must be between elements of the same phase of polarity. In the case of part C, the circuit is unique with semiconductors, since in electron tubes there is always a polarity inversion between input and output (except when used as cathode followers). The circuit of part B is analogous to the Pierce electron tube crystal oscillator.



External Voltage Divider Arrangement (Parallel Mode)



U1 tra-audion Arrangement



**Basic Capacitive Feedback Circuits** 

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For maximum power output, the input and output closely as possible; this requirement accounts to a great extent for the numerous variations in circuitry, since it is usually possible to sue any of the three basic circuit configurations and to ground any element. With the crystal determining the frequency stability of the circuit it is only necessary to arrange the proper polarity of feedback and provide a small amount of excitation to start the crystal oscillating. Although in a few cases the phase relationships within the transistor may require tight coupling to provide oscillation, it is usually easier to obtain stable crystal oscillations than to obtain stable self-excited oscillations, because of the assistance of the piezoelectric effect. The Colpitts semiconductor crystal oscillator, like its electron-tube counterpart, is usually a vigorous oscillator in the high-frequency range. However, the use of a quartz crystal does not extend the maximum frequency of oscillation, although it sometimes does provide better performance in the region between the alpha cutoff frequency and  $f_{max}$ . Thus good design makes it mandatory to use a transistor capable of oscillating strongly m the desired radiofrequency region of operation regardless of crystal control, Although there are a number of circuits in use, there is not much evidence at the present state of the art that the Colpitts is much (if any) more stable than the tickler coil crystal oscillator. Its main use is to improve operation at the higher frequencies.

Circuit Operation. A typical common-emitter Colpits circuits using the external capacitive divider feedback method is shown in the accompanying schematic. Voltage divider bias is used for easy starting and is supplied by RI and  $R_{\rm R}$ , with  $R_{\rm E}$  providing emitter swamping resistance for stabilization of the transistor. Feedback is provided from collector to ground. With the base effectively bypassed by C3, the capacitive voltage divider consisting of C 1 and C2 is effectively connected between collector and base for rf. Both feedback divider capacitors are variable to permit adjustment and control of feedback. Capacitor Cl also serves to bypass rf around emitter swamping resistor  $R_{\rm F}$ . Capacitor C2 is the primary feedback control, and is usually made variable to facilitate operation with more than one type of transistor and crystal. The crystal is connected between the collector and ground and operates in the parallel mode. The collector is series-fed through the RFC and conventional bypass capacitor C4. The output is taken capacitively through Ccc from the collector.

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Untuned Colpitts Crystal Oscillator

The operation of the Colpitts type of oscillator basicaMy depends upon the action of the voltage divider consisting of Cl and C2. Assume that the oscillator is first turned on. With fixed class A bias supplied by bias voltage divider R1, R<sub>B</sub>, collector current flows, and a voltage appears across the Cl, C2 divider. The voltage appearing across Cl is in parallel with emitter resistor  $R_{E}$ . Assume that a noise pulse caused by thermal action in the transistor causes the collector current to increase. A portion of the noise pulse voltage is then fed back through C2 to the emitter, causing the collector current ot increase further (this is a regenerative action). At the same time, this increase in noise voltage at the collector also appears across crystal Y. Thus, the crystal is slightly strained mechanically by piezoelectric action. When the collector current reaches satr.tration, no further change in  $I_c$  occurs, and the regenerative action ceases. At this time, the electrostatic strain across the crystal begins to reduce as capacitor C2 discharges (the heavy current flow from collector to emitter effectively shunts the capacitor). Thus, the emitter to ground voltage is reduced, the forward bias is reduced, and the collector current starts to fall. This action is also regenerative, and the transistor quickly reaches cutoff. As the collector current reduces, the voltage across the crystal approaches that of the supply (becomes more negative), and the crystal is now strained in the opposite direction. As a result, as each cycle of this action co..tinues, the crystal oscillates at its parallel-resonant frequency. Since oscillation of the crystal produces a voltage across it, once started into vibration, the crystal continues to oscillate Since the crystal is connected in shunt from collector to ground, it effec-

tively functions as a parallel-resonant tank circuit, and smooths out the pulses of oscillations into \_ approximate sine wave-forms. On the conducting portion of the transistor operating cycle, it is effectively reinforced by the ensuing pulse of collector current, and during the nonconducting portion of the cycle, it supplies what would otherwise be the missing halfcycle of oscillation by flexing in the reverse direction. Emitter resistor  $R_E$  and capacitor Cl form an amplitude limiting device similar to that of the electron tube grid leak. The output is taken from across the crystal, with CCC acting as a dc blocking and ac coupling capacitor. It is evident that the crystal must be capable of handling the power developed, since if driven too hard it will fracture. However, at the norreally low milliwatt outputs obtained with transistors, this is no problem. It does indicate, however, that the transistor crystal oscillator requires additional stages of amplification to produce the same r-f drive as an electron tube crystal oscillator.

A typical Colpitts crystal oscillator of the ultraudion form is shown in the following illustration and may be compared with the basic version. This circuit is analogous to the Pierce type crystal oscillator, and is more easily **recongnizable** because the crystal is connected directly between collector and base. The common-emitter configuration is also used in this version, and feedback is provided directly through the crystal. Voltage divider class A bias is obtained by , means of **R1** and **R**<sub>B</sub> for easy starting, with emitter swamping being provided by  $R_{\rm F}$ , bypassed by C2.



Ultra-audion Colpitts Crystal Osci11 ator

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The output is taken capacitively from the collector circuit through Ccc. In this instance, c3 is avariable control which permits adjustment for feedback and transistor variations. Both this circuit and the Pierce electron-tube circuit operate almost identically. The feedback capacitive divider in this case consists of the total shunt capacitance across the crystal (including holder and stray wiring capacitance, plus the internal collector-base capacitance, shown dotted as Cl) and external capacitor C3 to ground. In this circuit version, the crystal and feedback network appear to be in the base circuit, rather than the collector circuit as in the other version. The difference is that, like the ultraudion electron-tube oscillator, the crystal is considered to be a tank circuit operating in the parallel mode, and since the capacitance of Cl and C3 is usually less than that of Cl and C2 in the previous circuit version (the emitter-collector capacitances is much larger than the base-collector capacitance), the ultraudion circuit tends to be operable at higher frequencies than the external capacitive-divider circuit. Also, phase shifts within the transistor due to transit time effects are such that they aid in producing the correct feedback polarity.

Now consider one cycle of operation. Assume that crystal Y at rest and the circuit, as illustrated above, is inoperative with no collector voltage applied. At rest, the crystal is unstressed and there is no charge on either plate. When the collector voltage is applied, since the circuit is fixed biased for class A operation by voltage divider Rl,  $\mathbf{R}_{\mathbf{B}}$ , collector current flows similarly to that in a conventional amplifier. With the base connected to one plate of the crystal and the collector connected to the other plate, when one plate is negative the other plate will be positive. This is the same condition as when the crystal produces a piezoelectric voltage; it is also the same as the polarity for base-collector operation in the common emitter circuit (base polarity is opposite to collector polarity). Therefore, the instant the collector appears negative at turn-on time, the piezoelectric voltage across the crystal causes the base electrode to be positive; this small positive voltage, in turn, causes a reduction in  $I_c$ , producing a decrease in collector current. Thus, the collector voltage (of a PNP transistor) becomes more negative. This action is regenerative, and quickly drives the collector to cutoff. During this

time the crystal is being deformed in the same direction. During cutoff a small  $I_{CEO}$  current flows which only affects the efficiency of the circuit. Since the value of  $l_{CEO}$  is steady, there is no change in feedback from the collector. Meanwhile, the small charge developed on C2 by the flow of emitter current through  $R_E$  leaks off, reducing the emitter bias and permitting the class A bias to again cause normal current flow. The increase in collector current now causes a reduction in collector voltage, in effect producing a positive swing. The crystal now changes polarity and flexes back toward its original shape. As a result of piezoelectric action, a negative charge now appears on the base electrode. This causes a further swing of collector voltage in the positive direction (this action is also regenerative), and at full current flow the crystal is equally deformed in the opposite direction. At this time the flow of  $I_c$  is again steady (corresponds to saturation current flow with selfbias). Since the emitter current flow through  $R_F$  produces a bias voltage, C2 now charges and the emitter bias is added to the fixed bias. Once again the collector current is reduced by the increasing bias, and the cycle repeats. Thus, in flexing back and forth in accordance with the changes in collector voltage, the crystal is caused to oscillate; in turn, it produces an in-phase piezoelectric voltage which enhances circuit action. The crystal oscillates at some frequency between that of series and parallel resonance. Actually, the phase shift of the feedback voltage from collector to base, which is necessary to produce oscillation, is produced by the crystal acting as a high-Q inductor which produces an initial 90-degree shift. An additional phase shift is caused by the base-emitter capacitance, which is sufficient to cause an effective feedback large enough to overcome any of the resistive losses in the circuit. Thus, continuous oscillation under control of the crystal is assumed. Although the basic oscillation consists of distorted pulses of collector current, the effective tank circuit action of the crystal helps smooth out these pulses into approximate sine-wave oscillations. The output is taken through coupling capacitor Ccc, and appears as a resistive load in shunt from collector to ground.

The common-base arrangement of the Colpitts crystal oscillator using in-phase capacitive feedback is shown in the following illustration. Voltage divider



Colpitts Common-Base Crystal Oscillator

bias is supplied by  $R_1$  and  $R_B$ , and the base resistor is bypassed for rf by C2. Emitter resistor  $R_E$ , which is bypassed by  $C_E$ , provides conventional swamping of the emitter circuit, and  $R_C$  provides resistance stabilization in the collector circuit. The crystal is connected between collector and ground, but is effectively connected between the collector and base for rf by means of C2. The output is taken capacitively from the collector (across the crystal) through Ccc.

Since the emitter and collector in the commonbase circuit are of the same polarity (in-phase), feedback is obtained by using Cl to apply a portion of the collector voltage to the emitter.

Now consider one cycle of operation. Fixed class A bias is supplied by voltage divider Rl,  $R_{B}$ . When collector voltage is applied, Q1 conducts as in a conventional amplifier. Assume that a noise pulse occurs in the base circuit, which causes the collector current to increase. The voltage drop across collector resistor **R**<sub>c</sub> appears as a positive-going puke, which is applied through Cl to the emitter. This increase in emitter bias is in the forward direction, causing a larger flow of collector current. Thus, a regenerative in-phase feedback exists. The positive-going noise pulse is applied to crystal Y, which is in shunt from collector to ground, causing the crystal to be distorted in one direction by piezoelectric action. When the collector voltage bottoms (becomes almost zero), no further feedback occurs and the crystal flexes in the opposite direction. By piezoelectric action the crystal polarity is now reversed and a negative charge appears at the grounded electrode. Since the base is connected to

ground through C2, the base now has a negative voltage applied and thus operates to reduce  $I_c$ . As the collector current reduces, the drop across  $R_C$  becomes negative-going and approaches the source voltage.

The feedback through capacitor Cl is also negative and reduces the forward emitter bias, causing a still smaller I to flow. This action is also regenerative and continues until cutoff is reached. At this point a small flow of reverse current  $(I_{CEO})$  exists, but it has no effect other than to reduce the over-all efficiency of the circuit. Once the feedback stops, there is no further change in current, and  $C_E$  (which was charged negatively during this half-cycIe) starts to discharge through emitter resistance R<sub>E</sub>. When the emitter voltage drops to a value which again starts I flowing, a positive-going voltage is produced across  $R_{C}$ , and a positive voltage is again fed back through Cl, and the cycle repeats. During this time the crystal is now flexing in the opposite direction and the polarity across it again changes, so that the crystal-induced piezoelectric voltage is in phase with the collector-base voltage. Actually, the crystal acts as a tank circuit, smoothing out the rough pulses of current into approximate sine-wave variations. By appearing as a high-O inductance, the crystal insures that the proper feedback phase relationship is maintained, and, since it is a low-loss tank, the feedback through Cl need only be sufficient to supply the small tank losses to sustain oscillation.

By properly proportioning  $C_E$  and  $R_E$ , the bias can be made to reach the region of class C operation for best efficiency, as in regular gridleak operation, while the fixed class A bias makes certain that starting occurs easily. The output is taken from across the crystal through coupling capacitor Ccc. Therefore, the load is in shunt with the crystal and tends to reduce the output somewhat as in the electron-tube Pierce circuit.

**Circuit Variations. Because** the Colpitts crystal circuit has so many variations, a few representative circuits are shown in the following illustrations to facilitate identification of this type of circuit. Parts are labeled as in previous illustrations where they serve the same function, and the discussion is limited to the basic differences between these circuits and those considered previously.


**Tapped Cdleetor Crystal Oscillator** 



Grounded-Collector Colpitts Crystal Oscillator

In this circuit version, conventional voltage divider bias and emitter swamping are used for stabilization. The crystal is series-connected between the emitter and the collector by the voltage divider, consisting of Cl and C2, connected across L1. The operation of this circuit is based on a combined matching of impedances and a feedback connection. Connecting the crystal to the emitter through the capacitive voltage divider provides the proper feedback polarity, and the capacitances of Cl and C2 together with L1 form a tuned tank circuit which is resonant to the crystal fundamental (series-resomnt) frequency. The input and output impedances of the transistor are matched by the proper capacitance ratios, producing the same effect as though the collector were tapped across L1. The output is taken between the tap and ground, that is, across the crystal. This type of circuit is usually used at the lower r-f frequencies. The use of a tuned tank helps provide a good waveform and permits frequency doubling or the use of an overtone crystal.

A grounded-collector common-emitter version in which the voltage divider and crystal are located in the base circuit shown previously. Conventional voltage divider biasing and emitter swamping are used for stabilization. The collector is grounded for rf by C3. Thus in effect the crystal is connected between base and collector similar to the Pierce grounded-plate electron-tube version. However, the crystal, although isolated from collector voltage, is still subject to the small bias voltage from base to ground. Feedback is provided through capacitive divider Cl and C2, with primary control of feedback being provided by C2. Capacitor Cl is used to tune (match) the output, which is taken between the tap and ground. This type of connection offers a low output impedance suitable for coaxial line matching. The RFC is used to keep the emitter above ground; otherwise, the load or output would be short-circuited through  $C_{E}$ . No particular claims are made for this version other than its output matching feature.

The inverse feedback type of crystal oscillator shown in the following illustration, utilizes a conventional Colpitts with an external feedback capacitive voltage divider and with the crystal in the collector circuit. Bias is obtained by a conventional voltage divider, and emitter swamping is used for stabili-The bias is provided in conjunction with zation. feedback by tapping  $R_F$  on L1. Thus, dc bias is obtained through  $R_F$  and  $R_B$ , r-f feedback is obtained through R<sub>F</sub> and L<sub>1</sub>. The basic feedback path is through the capacitive divider, Cl and C2, and the secondary feedback path is through  $L_1$ Placing the tap at the lower end of via R<sub>E</sub>.  $L_1$  produces regenerative feedback, and placing it at the upper end produces degenerative feedback, because the polarization of the collector is opposite that of the base. Thus, by placement of the tap, the feedback can either enhance oscillation by regenerative action or stabilize operation by degenerative action. The possibility that unwanted resonances of parts in this circuit may tend to cause free-running operation makes this version of dubious value. With the output being taken from the collector, it is more likely that the feedback tap provides better input and output matching to the transistor, similar to the tapped collector circuit previously mentioned.



Inverse Feedback Crystal Oscillator

#### Failure Analysis.

**No Output.** In tuned circuit oscillators, the loss of output can be due to improper tuning. Also, a defective crystal will prevent operation, in either tuned or untuned circuits. A suspected crystal can easily be checked by the substitution of a crystal known to be good. A simple resistance check will indicate continuity and general parts condition. A defective bias

resistor producing a high bias voltage (in the divider arrangement) can prevent starting, and will be made evident by a resistance or voltage check. An open bias arrangement can prevent operation by causing a lack of bias, or by causing excessive internal bias due to feedback within the transistor. An open r-f choke, collector resistor, or coil will also stop operation. A shorted coil in the tuned circuit can stop oscillation, but the short will not be revealed by a resistance check. This condition is checked (after all other components have been eliminated from suspicion and a crystal known to be good has been substituted) by grid-dipping the tank for resonance. A defective transistor should be suspected only if all other parts check satisfactory and bias and supply voltages are normal.

Reduced Output. A low supply voltage or increased collector resistance can cause a reduction of output. A reduction of bias from class B or C to class A will also result in reduced output. Both of these conditions can be determined by a simple voltage check, preferably with a vacuum-tube voltmeter or a high-resistance voltohmmeter. Reduced crystal activity, due to aging or semi-fracture, or a dirty crystal can also be a prime cause. In this case, substitution of a crystal known to be good will restore normal operation. A change in the value of the emitter swamping resistor or bypass capacitor can cause excessive bias, and consequent squegging or motorboating due to intermittent blocking of oscillations. In circuits designed for the higher frequencies, changing the lead dress or parts wiring during repair may change the distributed wiring capacitance sufficiently to detune the circuit and cause a reduced output. In the tuned tank versions of this circuit, reduced output can also be caused by a high-resistance tank circuit connection or a shorted turn.

**Incorrect Frequency.** A defective or dirty crystal can cause an abrupt change from one frequency to another; this can sometimes be corrected by adjusting the tank tuning, if an adjustment is provided. Aging of the crystal can also cause a slow change over a long period of time; this change can sometimes be compensated for by means of a small trimmer capacitor, if the frequency is higher than normal. (Do not add an unauthorized modification to accomplish this. In most circuits a trimmer is included to permit calibration to the exact frequency for which the crystal is ground.) Failure of the collector supply regulation (as well as the bias supply regulation) can cause the effective element capacitance of the transistor to change

#### **ELECTRONIC CIRCUITS**

and cause slight off-frequency operation. In this case, check the supply voltage with a high-resistance voltmeter and observe whether there are occasional fluctuations of the voltage when the crystal is suddenly removed from its socket and reinserted into its socket or when the load is suddenly removed and replaced. If all components check normal and trouble is still present, the crystal is probably defective.

# PART 6-3. TUNED-LINE OSCILLATORS

### **TUNED-LINE OSCILLATORS**

### General.

As the frequency of operation extends into the VHF and UHF regions and into the microwaves, it becomes more and more difficult to produce oscillations using conventional electron tubes. At the extremely high frequencies even the best oscillators are not very efficient. The difficulties of highfrequency operation involve the construction of the electron tube. As the frequency increases, the transit time between electrodes must be considered. Also, the tube electrodes have capacitance between each other and ground, and their leads have inductance. At the lower frequencies these capacitances and inductances are negligible as compared with the other lumped circuit components, but at the very high frequencies they become the major part of the circuit, and often must be minimized to extend the upper frequency limit. To minimize lead inductance, electron tubes are debased (no base is used), they use large leads to minimize skin effect, and sometimes have their grids or plates brought out through the envelopes. To reduce interelectrode capacitance, tubes are miniaturized to make their elements smaller (this also reduces their power-handling capability), and special construction in the form of a planar triode or tetrode is used. (The planar type of construction uses a single flat grid (or plate) through which the electron stream passes, instead of grids or plates made up of wires or screens, which are "wrapped" around the emitter as in conventional tube construction.) The original derivation of the planar tube was the well known lighthouse tube (also called *disc seal* tube), which is so named because of its physical resemblance (three or more stepped cylinders) to a lighthouse. These tubes utilize coaxial and

planar elements, or rings, with direct physical connection to the electrodes themselves. There are two forms of oscillator used. One form, which operates in the VHF region, uses a special socket and its operation is similar to that of a conventional LC oscillator. The other, which is used in the UHF region, incorporates a series of coaxial cylinders into which the lighthouse tube fits as an integral part, forming a tuned line coaxial oscillator. Tubes used for low power and receiving purpose are usually provided with conventional pin type sockets, and those used for transmitting are either provided with a special socket and plate cooling fins or are inserted into the cavities or lines to form a compact unit. The construction of a typical tube is illustrated in the accompanying figure.



#### Lighthouse Tube

In addition to the coaxial line oscillators, tuned transmission line, or Lecher line, oscillators are also used. The tuned lines in these oscillators are arranged parallel to each other, instead of being arranged coaxially. At the lower frequencies the lines are used as inductances and are tuned with a shorting capacitor. At the higher frequencies they are tuned with a

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shorting bar and operate essentially as a quarter wave transmission line.

The tuned line can be substituted for an LC tank circuit because it possesses the same properties as the tuned tank. When the line is exactly a quarter wavelength long electrically, and is shorted at the far end with the input open, it presents a high impedance at the input and a low impedance at the far end. When it is coupled to a source of energy, a heavy current will flow in the line at the shorted end, but only a small current (or no current) will flow at the open or input end, because of the high input impedance. This effect is exactly the same as that produced by the conventional LC tank; therefore, the quarter-wave line can be substituted in its place.

Use of the transmission line tuned circuit provides a higher Q and lower losses than is possible with conventional lumped inductance and capacitance. The higher Q is obtained because the resistance of the line is low for a given value of reactance, since Q is equal to XL/R. The low resistance is obtained by using relatively large diameter tubing, since at radio frequencies current flows on the outside of the conductor because of skin effect. For UHF applications this loss is made even less by silverplating the outside of the conductor, so that the r-f current flows through a highly conductive path of silver. For single-tube oscillators the concentric type line is frequently used, and for push-pull circuits a balanced two-wire line offers a convenient arrangement (two concentric lines may also be used). The concentric line has the additional advantage that the outer conductor shields the inner conductor and thus reduces unwanted radiation from the tank to a minimum.

An incidental feature of the quarter-wave transmission line tank **results** from the use of the highimpedance property at the open (input) end and the low-impedance property at the output end to insulate the line as far as rf is concerned. Thus the shorted end of the line may actually be attached to the chassis without affecting the operation. This helps to reduce dielectric losses, which otherwise would be introduced if an actual insulator were used. Unfortunately, this feature cannot be used where dc is applied to the line as in series plate feed arrangements, but it can be used in shunt-feed arrangements.

The tuned lines and circuits discussed in this section are confined to negative grid oscillators; that is, to oscillators where the average grid voltage is always negative, since there are other special oscillators (such as the Barkhausen-Kurz and Gill-Morrell oscillators) which use positive grid operation to obtain UHF oscillations. This classification is necessary to avoid confusion, as both groups appear to be identical schematically at first glance, since both employ tuned lines. The positive grid voltage is the major identifying feature of the positive grid oscillator and the circuit operation is entirely different from the operation described below.

Because the reactance of the tube interelectrode capacitance and distributed circuit capacitance is small at ultra high frequencies, the circulating (or charging) current in these capacitances is large. It is on the order of many amperes for large power tubes. This high current adds nothing to performance, and may cause damage. Because of skin effect, the current follows the surface of the metal electrodes of the electron tube, and causes localized heating of the seals, sometimes causing cracks and tube failure. Thus, in UHF oscillators the tuned circuit is designed to have a high inductance and the minimum capacitance that will resonate the tank to the operating frequency. Tuned-line tanks provide the required high inductance with a minimum of capacitance. The trend in present day tube manufacturing is to employ ceramics instead of glass as dielectrics, because of their better heat resistance and easy machining properties, in addition to the reduction of inter-electrode capacitances. The push-pull circuit effectively reduces these capacitances to half their normal value since they are in series in push-pull operation. Although an open transmission line has some eddy current and radiation losses, close spacing to less than one hundredth of a wavelength (a few inches) causes the field around one conductor to neutralize the field around the other, Radiation and eddy current losses are thereby minimized, but not as completely as with the shielded coaxial line.

The Q of the quarter-wave short-circuited section of line is much higher than that of the conventional tank circuit because larger diameter conductors can be used than in the conventional coil, making the skin effect less. Specially constructed (planar) tubes extend the transmission line as a part of the tube leads. Thus, the interelectrode capacitances and lead inductances of the tube are all incorporated as a part of the tuned circuit.

Transit time produces two different effects at UHF. (1) it causes the plate current to lag the grid voltage by a small angle, so that the phase difference

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between the plate current and plate voltage is greater than 180 degrees. As a result, the power output is decreased and the plate dissipation is increased. (2) The transit time permits an accumulation of electrons on the grid and causes grid current flow, even when the grid is negative. This produces a grid loss which is similar to the loss incurred by shunting the grid with a resistor. At extremely high frequencies this loss is so great that the effect is as though the shunting resistor produced a short circuit between grid and cathode and prevented proper excitation of the tube. The grid loss also results in the development of heat, which can exceed the tube ratings.

Therefore, while tuned lines, together with special tube construction, offer a partial solution to the transit time problem, a different kind of generator other than the simple ultraudion feedback arrangement is required to operate at UHF with resonable power output. The lighthouse tube provides efficiencies on the order of 48% at 500 MHz to 10% at 2100 MHz for CW operation, and 52% to 35%, respectively, for pulsed emissions. The present day trend is to use klystron generators for UHF, plannar tubes for VHF, and either klystron or magnetron generators for microwaves and beyond.

#### LIGHTHOUSE-TUBE OSCILLATOR

#### Application.

The lighthouse tube oscillator is used as an r-f source in the UHF range for recievers, test equipment, and low-power oscillators or transmitters. The planar type triode or tetrode is used for transmitters where more than a few watts are needed.

### Characteristics.

**Use** special tube construction to overcome high-frequency limitations.

At frequencies of 300 to 1500 MHz uses external lines, and at frequencies of 1500 to 2500 MHz uses coaxial cylinders, into which the tube is inserted as an integral part.

Tuning is accomplished by means of shorting bars or plungers.

Has low output and low efficiency (10-30%).

### **Circuit Analysis.**

Generel. The so-called lighthouse tube oscillator is operable over a large range of frequencies, and the frequency of operation basically determines the final form of the oscillator. At frequencies up to about 1500 MHz, the size of the coaxial elements that would be required is so great that external open-wire line or tubing must be used. When the frequency approaches 2500 MHz, however, coaxial elements become small enough for practical use, and the tube itself can be inserted into them to form part of the line. Since the design of the lighthouse tube provided the necessary means of overcoming the difficulty of obtaining oscillations at the high frequencies above 300 MHz, there have been a number of similar designs. Thus, the basic lighthouse tube evolved into the co-planar type of triode and pentode. In this tube the elements are coaxial cylinders, with the outside of the rign forming the electrode contact. Planar tubes using plane rings instead of coaxial cylinders can be used in coaxial lines, or separately with a special socket. The receiving type (or low-power type) has a conventional octal socket using only cathode and heater pins. The transmitting type requires the special socket and is usually equipped with radiation type cooling fins connected to the plate and normally requires forced air cooling. Where coaxial construction is used, the coaxial line itself acts as the heat radiator. Since the basic lighthouse coaxial unit is representative of this type of design, all discussion will be confined to the original type of lighthouse tube. Although now replaced by tubes of planar design, the original lighthouse tube may still be encountered.

**Circuit Operetion.** The construction of a typical self-contained lighthouse tube oscillator is shown in the accompanying illustration. The tuner assembly consists of three concentric tubes, or coaxial lines. The inner tubing is connected to the plate, the center tubing to the control grid, and the outer tubing to the shell or base envelope of the tube. The outer tube is effectively shorted to the cathode for rf by a built-in mica capacitor connected between the metal envelope and the cathode.



**Coaxial Cavity Tuned Oscillator** 

The cathode (outer) and control grid cylinders form a coaxial cathode line which is effectively short-circuited by a capacitive non-conducting plunger at a point approximately 3/4 of a wavelength from the point of connection to the tube elements. The position of this plunger is adjusted for the proper amount of feedback. The capacitance between the plunger dielectric and the grid conductor of the coaxial line effectively shunts the rf to the cathode, but does not short-circuit it for dc. The dc path between the cathode and control grid is provided by grid-leak resistor 1\$, bypassed by grid capacitor C, which produces grid-leak operating bias. A shorting plunger is inserted into the plate line 1/4 wavelength from the open end (3/4 wave from plate end) to tune the plate circuit. Plate voltage is supplied by connecting B+ to the plunger. The short circuit provided by the shorting plunger offers a high impedance to r-f energy a quarter wavelength away, so that no rfc is needed to isolate the plate supply. Since the grid is located approximately one wavelength from the open end of the line and a high impedance is reflected there by the plate tuning plunger, the grid is also placed at a point of high impedance with respect to plate. Thus the open wavelength-long plate conductor and the shorted three-quarter-wavelength cathode conductor both act as parallel resonant tank circuits. The tuning of the plate circuit determines the operating frequency of the oscillator, and the tuning of the cathode circuit determines the proper amount of

feed-back for stable oscillation. Since there is a certain amount of interaction between the plate and cathode circuits, it is necessary when changing frequency to adjust both plungers for optimum operation.

**Detailed Analysis.** The r-f equivalent circuit of the lighthouse tube oscillator is shown in the accompanning illustration.



### Lighthouse Equivalent Circuit

The interelectrode capacitance of the lighthouse tube, plus the capacitive effect of the open ends of the grid conductor, is represented in the diagram as C<sub>pk</sub>. The net reactance of the parallel tuned circuit containing  $C_k$  and  $L_k$ , shunted by  $C_{gk}$ , must be capacitive to ensure that the voltage divider which they form with  $C_{g^p}$  supplies alternating voltage of the proper polarity to the grid. This means that the frequency of the cathode tank circuit must be lower than the output frequency of the oscillator. The operating frequency of the oscillator is determined primarily by the resonant tank in the plate circuit  $(C_p, L_p)$ , which is in parallel with  $C_{gp}$ , and the effective input capacitance of the voltage divider network; consequently, it is lower than the resonant frequency of the plate tank alone, and slightly higher than the frequency of the cathode tank. To provide the proper feedback to sustain oscillation, it is necessary that the resonant frequency of the cathode tank circuit be less than the resonant frequency of the plate tank circuit. This is accomplished by careful tuning of the lines. Particular care is necessary in adjusting the cathode line; if the line is too short, it appears inductive and

oscillation stops. On the other hand, if the line is too long, the effective feedback divider capacitance is increased, and the amplitude of the feedback voltage becomes too low to sustain oscillation. Consider now one cycle of operation. When the plate voltage is applied, heavy current tends to flow in the plate circuit since the tube is self-biased and the initial bias is zero. The initial rush of current shock+ xcites both plate-grid and grid-cathode tanks into oscillation. Since the grid-cathode tank  $(C_k L_k)$  is tuned to a lower frequency than the oscillator output, it appears as a capacitive reactance shunting the grid-cathode interelectrode capacity, C.&. Neglecting the plate tank for the moment, it is seen that C<sub>ap</sub> will charge due to momentary grid current flow, since  $C_{g^p}$  and C<sub>gk</sub> form a capacitive voltage divider between plate and cathode, or ground. Assuming that the charge is in such a direction as to make the grid more positive a momentary and amplified increase in plate current will occur. This action is regenerative. Since the plate tank is tuned to a higher frequency than the r-f output, it appears as an inductive reactance shunting C<sub>gP</sub>. The result is to produce a negative grid input resistance which overcomes grid circuit losses and permits oscillation to occur. This negative resistance occurs primarily from the tank circuit which, in effect, returns energy to the circuit through its flywheel effect. When the grid pulse reaches its maximum, the plate tank appears as a high inductive impedance across which the plate voltage is dropped. During this time the tank absorbs energy from the circuit. As the grid swings negative plate current is reduced and eventually cut off. During this time the tank is returning energy to the circuit. The feedback is now in an opposite direction to the initial charging current (C<sub>en</sub> is discharging), is likewise regenerative, and quickly drives the tube to cutoff. Once oscillatory action is started it continues until the plate voltage is removed, or until the grid tank is detuned too far from resonance to retain the proper phasing. If tuned too high in frequency it appears inductive and the feedback is opposed and oscillation stops. Conversely, if tuned too low in frequency it acts as a heavy capacitive shunt from grid to cathode and also stops oscillation.

Grid bias is provided by grid-leak resistor  $R_g$  and capacitor  $C_g$ , which are connected between the open (high-impedance) end of the grid line and ground. After a few oscillations are built up, a small charge is put on  $C_g$  each time the lower end of the tank circuit swings positive. During the time the grid is not posi-

tive with respect to the cathode part of the charge leaks off through grid leak  $R_g$ . The voltage to which the grid capacitor is charged ultimately makes the grid sufficiently negative so that only a small amount of charge is added to the capacitor at the peak of each cycle, and all of this small increase of charge leaks off through  $R_g$  during the remaining time of the cycle. Thus the grid is maintained at the proper bias for good operation. If the high negative bias required for proper operation were applied at the time the oscillator was turned on, the tube would be completely cut off and oscillations could not start. It can be seen from the schematic that this circuit is essentially a simple tuned-plate, tuned-grid oscillator with the basic feedback being supplied through the plateto-grid capacitance.

## Failure Analysis.

No Output. Since the unit is of integral construction, loss of output may be caused by failure of the cavity to tune properly, a defective tube, or an open or shorted supply. Where contact fingers are used for the shorting plunger, as in the plate line, poor contact will cause improper tuning and lack of oscillation. Also, poor contact will cause a reduction or complete lack of plate voltage, and produce 10ss of oscillation. The presence of voltage maybe determined by a voltmeter. Poor contacts will be indicated by fluctuations of the plate current as the plunger is tuned, and sometimes by burnt spots on the lines. A defective tube is usually indicated by lack of normal plate current when due to lack of emission, or by abnormal plate current when short-circuited. Because of the inherent solid construction of the coaxial tuner, poor contacts or tube failure are the most common troubles. At radio frequencies any additional resistance in contacts produces losses which are serious in the UHF range. Therefore, effects which are not very noticeable at the lower frequencies can produce complete lack of oscillation at UHF. Since the inner cavities are inaccessible until disassembled, the only practical check is a test for voltage on the heaters and plate, and between grid leak and ground, if accessible. Observation of the plate current while tuning and a check of the voltages should be made first. The unit should then be disassembled and the tube and coaxial tuner checked.

**Reduced Output.** Reduced output is usually due to low plate voltage or improper tuning. Low plate voltage can be the result of poor contact resistance in

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the tuner or a **defective supply**, which can be easily located by making a voltage **test**. Improper tuning can be quickly verified by slight readjustment of the controls to see whether the output **improves**. With normal plate voltage and correct **tuning**, if the output remains **low**, either the tube or the grid leak is probably **defective**.

Incorrect Frequency. Since the frequency is determined by the adjustment of the plate tank, small frequency changes can be corrected by tuning. Platevoltage and load changes will also affect the frequency to a small extent; these can be checked by changing the load and measuring the supply voltage. Normally the high Q tank afforded by the coaxial cavity results in a highly stable frequency. In cases of high ambient temperature, however, the line and cavity dimensions may change and produce a drift in frequency, depending upon the metal used. For temperature-caused changes, adequate ventilation by means of forced-air cooling is necessary. If the cavities and lines are made from temperaturecompensated alloys, the cause of frequency changes will be limited to supply or tube defects.

**Instability.** Unstable oscillations may be caused by erratic plate supply voltage, lack of regulation, or improper tuning.

# LECHER-WIRE OSCILLATOR

### Applications.

Lecher-wire oscillators are used in the VHF and UHF regions to generate **rf** for the receiver **oscillators**, test **equipment**, and **transmitters**.

### Characteristics

Uses a pair of lecher wires, or tuned lines, in place of conventional LC tanks.

Frequency of operation is such that use of quarter-wave or half-wave lines are practical.

Has better stability and efficiency than a conventional LC circuit.

Usually used with the planar type of high-frequency tube, but not restricted to any type (can be used with any tube that will oscillate).

# Circuit Analysis.

**General.** The lecher-wire, or transmission-line, oscillator is derived from the lecher wire wavelength measuring principle and the application of transmis-

sion line theory. The lecher-wire principle is shown in the accompanying illustration, in which two parallel wires a few inches apart are capacitively coupled to an r-f source. Assuming that the coupling is loose, the wires are in effect open-circuited. The length of the wires should be at least one full wavelength at frequency of the r-f source. When a shorting bar is series with a current indicator, such as a lamp or r-f ammeter, is placed across the lines, it will be observed that at a point 1/4 wavelength from the source maximum current is obtained. If the shorting bar is left at that spot and another one is moved along the line, an identical maximum indication (but not the same value) will be obtained at a point 1/2 wavelength from the first indication (3/4 wavelength from the source). This demonstrates that standing waves exist on the line. Such a device can be used to measure the frequency of operation in wavelengths. When the lecher wire is coupled through a single-turn loop to the r-f source, the line is considered closed at both ends; in this case, the first indication will be obtained at the half wavelength point.



#### Lecher Line

Transmission line theory predicts that a half-wave line repeats, or reflects, the input conditions at the output.

If a transmission line is open-circuited, it will have maximum impedance at the half-wave points, as shown in the preceding figure. If the transmission line is shorted, it will have the lowest impedance at the half-wave points as shown in the following figure. Conversely, a quarter-wave line (if open) will see a high imput impedance (at its source) when shorted at a point a quarter wave from the input end, and if



**Open-End Line** 



**Closed-End Lines** 

shorted at the input, will have a maximum impedance one quarter wave from the short as shown in the preceding illustrations of open and closed lines.

When standing waves exist on the transmission line, the current and voltage are out of phase. That is, at a



**Relationships of Standing Waves** 

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point of maximum current, the voltage is at a minimum and, conversely, at the point of maximum voltage, the current is at a minimum as shown in the accompanying illustration. Thus either voltage or current indications may be used in the lecher wire.

If the lecher line is attached to the grid and cathode of an electron tube and ground, and is tuned to a quarter wavelength, the current through the line will be heavy since it is limited only by the resistance in the line at the short; this is the equivalent of a series resonant circuit formed by an LC tank. At the grid and cathode (one quarter wavelength away), the impedance will be high and only a minimum current will flow between cathode and grid. Thus the line simulates a parallel resonant circuit, with a heavy circulating line current and minimum external current as shown in the following illustration.



Shorted Line Equivalents

**Circuit Operation.** When the lecher line is connected between the grid and plate of an electron tube, a simple ultraudion oscillator results, with the line forming the tank connected between grid and plate of the tube, as shown in the following illustration. In the illustration a capacitive shorting bar is employed; since plate voltage is present on the plate bar, it would be applied to the grid if a direct shorting bar were used. At the frequencies used, the capacitor has such a low reactance that it is effectively a short circuit for rf, but it will block dc. Grid-leak bias is obtained through the action of  $\mathbf{R}_{g}$ , and the total effective grid-cathode circuit capacitance acts as the grid-leak capacitor. The r-f output can be taken from

## OSCILLATORS

the circuit with a hairpin coupling loop or capacitively from the grid or plate bar. Tuning is accomplished by moving the shorting bar along the lecher line. The amplitude is controlled by the grid-leak value and the applied plate voltage, by the spacing



Simple Lecher Line Oscillator

between the bars, and by the tube electrode capacitance. See the ultraudion oscillator circuit discussion in another part of this section for an explanation of the feedback operation of this type of circuit.

Although the simple oscillator just discussed is operable, it has been found advantageous at UHF to utilize circuits which minimize the circuit capacitance. This allows the lecher lines to act more like lumped components, and thereby serve as the controlling factor in the circuit, permitting tube replacement with minimum effect on circuit operation. The tubes may be any type that will operate at the desired frequency of operation. In this circuit all elements are balanced. Since the interelectrode capacitances are in series in a push-pull oscillator, the effective capacitance shunting the circuit is half that for a single tube. (See following illustration,) Thus, the charging current for this amount of capacitance is reduced with a consequent reduction of capacitive circulating currents. As a result, tube seal heating effects and circuit losses are also reduced. Since the tubes operate alternately and the currents are opposite, losses resulting

from eddy currents and radiation from the lecher lines are reduced. Such reduction is due to the complete balance in the circuit and the close line spacing which causes the electromagnetic field around one line to almost completely cancel that around the other. Since the same voltages are present on both grid bars and on both plate bars, shorting bars can be used.



**Push-Pull Lecher Line Oscillator** 

For best efficiency and stability at ultra high frequencies, not only the tube losses but also the losses in associated circuits must be kept as low as possible. On the other hand, both the loaded Q and the unloaded Q must be kept high as possible. For this reason, the tuned circuits associated with UHF oscillators use resonant sections of transmission line, rather than coil and capacitor tank combinations.

Since the coaxial line is a form of transmission line, it has properties similar to the open-wire type. At high frequencies it has the further advantage of shielding the line, because the center conductor is entirely surrounded by the shield. As a result, coaxial lines reduce radiation and eddy current losses to an absolute minimum, and for this reason are used extensively. A typical coaxial type of lecher line oscillator is shown in the following illustration.



Coaxial Line Oscillator

In this type of oscillator, the grid and plate coaxial lines are shorted by small capacitors, Cl and C2, and have an effective length of one quarter wave each. This oscillator corresponds to a tuned-plate, tunedgrid LC oscillator with series plate feed and grid-leak bias. The filament type of tube shown utilizes the transforming action of a half-wave line section to bypass the filament to ground. At low frequencies the filament would be directly bypassed to ground with a capacitor. At the UHF region, however, this method of bypassing proves ineffective because the filament leads are long enough to offer a large inductive reactance. As a result of the transformer action in the half-wave line, connecting C3 and C4 to the far end of the line provides an effective shunt at the filament inside the tube, which ordinarily is inaccessible. Since the length of the line includes the filament leads, the physical length of the external line is slightly shorter than a half-wavelength.

### Failure Analysis.

**No Output.** Lack of supply voltage, a defective tube, an open circuit, or improper tuning can cause loss of output. Resistance and voltage checks will quickly reveal lack of circuit continuity or incorrect voltage conditions. The trouble then may be either in the tube or tuning. If the circuit will not tune and the plate current is excessively high or low, the tube is defective. Lack of contact in the shorting bar is then most probable, since it is possible to have a low dc resistance or continuity indication and a high r-f resistance which will not show on an ohmmeter. The usual troubles in this type of unit are open or highresistance circuits due to poor solder joints or defective components. Most line sections are mechanically and electrically of excellent construction. It is possible, however, for silver-plated components to develop a heavy oxide film which effectively opencircuits them at UHF, particularly in areas where corrosive vaports react with the silver. In this case, frequent cleaning is necessary, or gold plating may be required.

Low Output. Low plate supply voltage, together with reduced tube emission, is the primary cause of low output. A check of voltages will detect this type of trouble. Improper tuning can also result in reduced output; it can be eliminated by a slight readjustment of the shorting bars for maximum output. Defective contacts in the shorting bars are usually obvious, causing erratic indications as the bars are moved slightly back and forth. A high-resistance grid leak can also reduce the amplitude of oscillations, but it is easily located by a resistance check. In the open-wire unshielded line, it is also possible for nearby objects to produce capacitive unbalance and mistuning. If this effect is present, the plate meter will show a change in current as the hands or other objects are moved near the tuning controls.

Incorrect Frequency. This type of oscillator is adjustable over a sufficiently broad range that normal plate voltage changes or slight emission changes may be compensated for by tuning. Since the stability is determined by the tuned lines, any large frequency change indicates a defect in the tuning of the lines. This can be caused by poor contact resistance of the shorting bar and by defective shorting capacitors. Reflected load reactance can also affect the circuit operation; this condition is normally indicated by a return of the frequency to original value as the load is adjusted. A lecher line circuit is usually so stable that calibration markings ruled on the line itself can be used to accurately determine the line frequency. Normally, a resistance analysis and voltage checks should quickly reveal the component at fault.

# MAGNETRON OSCILLATOR

#### Applications.

The magnetron oscillator is used in the region of 100 MHz to 30 GHz and beyond, to develop r-f energy. It is used in test equipment, in low-power CW transmitters, in beacons, and particularly in radar equipment, as a source of high-power pulsed r-f energy.

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# Characteristics.

Utilizes a specially constructed tube with a resonator surrounded by a permanent magnetic field to produce the r-f energy.

Operates with grounded anode.

**Is** usually operated by a negative pulse applied to the cathode.

Has either coaxial or waveguide output, depending upon the frequency of operation.

# Circuit Analysis.

General. There are, generally speaking, two types of magnetrons: the split-anode negative resistance (or dynatron) type, and the transit-time (or electronic) type. The negative resistance type uses the principle of negative resistance between the two anodes to produce oscillation, and operates only at frequencies which are low with respect to the transit-time frequency (on the order of 100 MHz to 1000 MHz). The efficiency is low in comparison with the efficiency obtainable with transit-time operation; therefore, it is not very popular, being more or less supplanted by the power type klystron at these frequencies. The frequency of oscillation in this type of magnetron is controlled entirely by the resonator with which it is used, as in conventional LC oscillator On the other hand, the transit-time type of magnetron depends entirely upon the transit time to determine the frequency, with the resonator(s) providing greater efficiency and proper phasing for maximum output. A short treatment of the negative resistance type of magnetron is given below for the sake of completeness, with the remainder of the discussion devoted to transit-time magnetrons, which are in greater use.

**Circuit Operation.** Before discussing the two types of circuits, it is necessary to establish the fundamentals of operation. The accompanying figure shows

a simple magnetron. As can be seen, the tube is a diode with a cylindrical plate surrounding a coaxial



## **Elementary Magnetron**

cathode or filament. A negative voltage is applied to the cathode, in addition to the heater voltage needed for fdament emission or heating of the cathode, depending upon whether direct or indirect heating (fdament) is used. Because the plate is positive with respect to the cathode, an electrical field exists between cathode and plate (anode); an external dc magnetic field is placed perpendicular to the electric field, and is produced by a strong permanent magnet. See the following illustration. (While an electromagnet could be used and the magnetic field could be alternating, as well, this is done only on the low frequencies for special effects, and will not be discussed further.) In these discussions it is assumed that the magnetic field is produced by a permanent magnet. The tuned tank circuit in which the oscillations take place is connected between the plate and the cathode. This can be a tuned LC circuit, a coaxial cavity, or a special cavity resonator built into the tube.



Motion of Electron in Electric and Magnetic Fields

Consider now the effect of the electric field on the electrons emitted from the cathode. In the absence of the permanent magnet field there would be a continuous electron flow in all directions, radially, direct from the cathode to the plate. But with the magnetic field applied, as the electrons are attracted toward the plate they encounter a force (due to the magnetic field) that tends to push them in a direction perpendicular to the forces applied. Since two fields are involved, the plate-to-cathode-voltage induced electric field and the permanent magnet field, and since they are at right angles with respect to each other, the electrons are affected by the vector sum of these forces; with a strong enough field the electrons are deflected in a cycloidal path as shown in the above illustration. Thus they are effectively bent back toward the cathode. The following illustration shows the path followed by a single electron as the external magnetic field is increased. At some low value of field (A in the figure), the electron travels in a slightly curved path, but reaches the ancde. At the critical value of field (B in the figure), the electron just grazea the plate and returns to the cathode. When the field exceeds the critical value (C in the figure), the electron follows a smaller-diameter circular path and returns to the cathode without getting near the plate.



Electron Path with Increasing Magnetic Field

The current flow of the magnetron for the previous conditions is shown, perhaps more clearly, by the following graph. With the low value field a constant flow of current occurs between anode and cathode until the critical field value is reached, whereupon the current abruptly ceases and drops off to zero, since the electron can no longer reach the plate. The useful point of operation is where the electron is just prevented from reaching the plate by the critical

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field value. Oscillation is then produced by the current induced in the cavity or resonator by the electron movement. on the other half-plate is decreased by an equal amount. This results in a different electron trajectory.



**Plate Current vs Field Strength** 



Split-Anode Magnetron

While the actual electron flow in a magnetron is complicated, it is evident that since an electron is basically a negative charge of electricity, as it approaches an electrode it will change the field **distribu**tion around the electrode, inducing a **positive** charge and causing current flow within or on the electrode by electrostatic induction. As it recedes, a negative change will be induced. If the electron reaches the electrode it will be absorbed, and current will cease. When positive and negative charges are induced in a resonator, current flows alternately back and forth within the resonator, at the frequency to which it is tuned (resonant), and r-f oscillations are thereby produced. This is the simple basic principle by virtue of which the magnetron operates.

**Negative Resistance Magnetron.** The negative resistance magnetron is a variation of the basic magnetron using a split anode. It is capable of operating at a higher frequency (than the single plate magnetron) and with higher output. Its general construction is similar to the basic magnetron, except that it has a split plate, as shown in the accompanying figure. These half-plates are operated at different potentials by connecting them to opposite ends of a tuned tank circuit (or cavity). When the tank circuit is oscillating, the voltage on one half-plate is increased, while that

A graph of the plate current versus plate voltage characteristics of one segment of a two-segment magnetron, showing four different vahres of voltage applied to the other segment, is shown in the accompanying figure. Note that for each voltage there is a negative slope to the curve where the current is reducing as the voltage applied to the segment is increasing. Likewise, a curve of the difference current to the two segments of a split-anode magnetron as a function of the difference in the potential of the two segments when the voltage on one segment is raised as the other segment potential is lowered a like amount shows the same effect, that is, a negative slope. From the earlier discussion on negative resistance oscillators (see contents list under Electronic Oscillators for location), it can be seen that this curve bears a resemblance to the typical lazy "S" type curve that indicates negative resistance. Therefore this tube will produce oscillations of the negative resistance type if a parallel-tuned tank is series connected, either from one segment to the cathode or between the two segments. A schematic showing the tank connected between the two segments is shown in the following figure; this is a typical so-called push-pull nrugnetron circuit (from its resemblance to the push-pull type electron tube circuit.)

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Consider now the effect of the different potential fields between the segments and the cathode. In the quiesent or static condition, since the plate potential is applied equally through the tank coil, as shown in the following illustration, the dc field



**Push-Pull Magnetron Circuit** 

between the cathode and either segment is of equal strength. Once shock-excited (by application of B+), a transient oscillation is produced to increase the potential on one segment and decrease the potential on the other segment by a like amount. Thus the field is stronger in one half of the area around the cathode than in the other half. By applying the external permanent magnet field so that it is perpendicular to the cathode, a cycloidal motion is **imparted** to the single electron in a manner similar to that described in the basic magnetron discussion. The effect of the distorted field, however, is to cause the electron to make a number of revolutions before eventually being attacted to the segment with the lower potential as explained below. This action occurs because after the initial deflection by the field in a particular path of motion, the electron passes the split between the two plates and enters the electrostatic **field** set up by the lower-potential plate. Here the magnetic field has a stronger effect on the electron (since the electric field is weaker), and causes it to be deflected with a smaller radius of curvature. As the split is passed again (on the opposite side of the cathode) and the electron once again enters the higher-potential field area, it is again caused to deflect with a change in the radius of **curvature**. Thus the electron continues to make a series of loops through the magnetic and electric fields until it finally hits the low-potential plate and is absorbed. The following figure shows the effects of different potentials on the motion.



Electron Transit Paths

In part A the fields are equal, with the permanent magnetic field below the critical value. In B and C the field is above the critical value and current flows because of the action just discussed. Two different electron paths are shown for clarity. Actually, it has been found that optimum efficiency is obtained when the electron makes approximately 10 revolutions before contacting the anode. Since oscillation is produced by the negative resistance effect, the tank frequency governs the path of the electron and transit time is maximized. Naturally, this can happen only at the lower frequencies. As the frequency of operation is increased, the transit time eventually becomes the important limiting parameter, and the negative resistance oscillation is ineffective. Since a very concentrated field is required for the negative-resistance magnetron oscillator, the length of the tube plate is limited to a few centimeters for a magnet of reasonable dimensions. In addition, a small-size tube is required to make the magnetron operate efficiently at

UHF. Therefore, the plate size (area) is limited, and produces a serious limitation on the permissible plate heat dissipation. For this reason, heavy-walled plates are necessary to increase the heat radiating properties, and artificrd air or water cooling is necessary for high-power operation. These parameters, in effect, are the limitations which restrict its use to the lowfrequency end of the UHF spectrum and cause the transit-time magnetron to be in greater demand.

With the electrons traveling in numerous loops, there are bound to be collisions between electrons and bombarding of the filament (or cathode), producing secondary emission and in some cases even destruction of the fdament or cathode. This action is cumulative, and sometimes results in fdament burnout before the current can be reduced to a safe value. To minimize this effect, and to prevent unstable operation, the tubes are operated with reduced plate and filament voltage. In some tubes it is possible to use the electron bombardment of the cathode element to provide the heat for emission, once oscillation is started.

**Transit Time Magnetron.** In this type of magnetron the plate or anode block is usually constructed so that it functions as a tank circuit resonant to a particular **frequency**. The construction may be that of a simple shorted quarter-wave line resonator, as shown in the accompanying illustration, or as a multicavity resonator also illustrated.



#### Magnetron Tank Circuits

In either case there are no external tank circuits to be tuned, and the output of the magnetron is picked up by a transmission line with coupling loop (or aperture for waveguide) built into the tube. Usually, the anode is composed of more than two segments; as

many as eight or more are often used (while as many as 64 cavities have been used). While this type of magnetron has a reasonably high efficiency (30 to 60 percent) and large output, it is limited in that the frequency of oscillation is fixed by the resonator. Thus it tends to be supplied as a single-frequency unit which usually has provisions for tuning over a limited range (on the order of 1% at 9 GHz), and is operated at a fixed frequency. The average power is limited by the fdament emission, and the peak power is limited by the maximum voltage it can safely withstand without damage. Actually, during initial operation the high-power magnetron arcs from plate to cathode, \_ and must be properly adjusted by a process known as seasoning, after which it can handle the high voltage properly without damage (within limitations).

New magnetrons require an initial break-in period or seasoning because violent internal arcing occurs when they are first put into operation. Actually, arcing or sparking in small magnetrons, and in high power magnetrons is very common. It occurs with a new tube or after long periods of idleness once a tube has been seasoned. One of the prime causes is the liberation of gas from the tube elements during idle periods. Arcs are also caused by the presence of sharp surfaces in the tube, mode shifting, and by overworking the cathode (drawing excessive current). While the cathode can withstand considerable arcing for short periods of time, if continued excessively it will shorten the useful life of the magnetron and can quickly destroy it. Hence each time the excessive arcing occurs, the tube must be seasoned again until the arcing ceases and the tube is stabilized.

The seasoning procedure is relatively simple. The magnetron voltage is raised from a low value unit until arcing occurs several times a second. The voltage is left at that value until the arcing dies out. Then the voltage is raised further until arcing again occurs, and is left at the value until the arcing again dies out. Whenever the arcing becomes very violent and reassembles a continuous arc the applied voltage is excessive and is reduced to permit the magnetron to recover. Once recovered the procedure is again continued. When normal rated voltage is reached and the magnetron remains stable at the rated current value, the seasoning is completed. It is good maintenance practice to season magnetrons left idle either in the equipment, or held as spares, when long periods of non-operating time have accumulated. Follow the

recommended procedures and times for seasoning specified in the equipment technical manuals. The preceding information is general and of an informational nature only.

The outputs of pulsed magnetrons are on the order of megawatts, with an average power of not much more than 1000 to 2000 watts being usable for CW operation (a typical 3-megawatt pulsed radar has a 6-kw average rating). However, as the state of the art changes, these limitations also change; thus where 50 kw was once high power, 5 to 10 megawatts now represents high power.

The construction of transit-time magnetrons is varied; they operate in the VHF, UHF, and SHF regions. Some are not tunable, while others are voltage tunable (anode potential is varied), mechanically tunable by hand or by motor, or are fixed-tuned. They provide power outputs of 50 to 100 milliwatts for receiver operation, and in the megawatt region for high-power radars, with all ranges of in-between powers. They are provided with integral built-in permanent magnets or with external magnets. They are supplied with transmission line outputs or wave-guide outputs, or with transition type coaxial-to-wave-guide outputs. They are of glass-metal or ceramic-metal construction, with advantages claimed for each. Cooling is achieved directly by natural air draft for low powers, by forced air or liquid air-convection, or by heat exchangers for the high-powered types. It is evident, therefore, that the subject or magnetrons covers a large field, with a complexity far beyond the scope of this technical manual. Thus, in the following discussion sufficient detail is provided to insure a basic understanding of the general principles of operation, with the important principles emphasized or expanded as needed. For details on a specific type of magnetron, consult the manufacturer's specifications, and refer to a more comprehensive text for further information.

**Detailed Analysis.** The magnetron, while capable of generating continuous-wave oscillations, is particularly suited for pulsed power applications, as in radar. That is, the magnetron is capable of producing pulsed powers of more than 1000 times greater than the best c-w output at the same frequency. Basically, there are three factors which produce the favorable conditions for pulsed powers; the magnetron is more efficient at very high levels of power and voltage; an oxide cathode under pulsed operation produces currents over 100 times greater than that obtainable

under dc (non-pulsed or **CW**) conditions; and finally, by pulsing with small duty cycles, anode heat dissipation is less of a problem, so that greater powers can be handled. On the other hand, a new problem is posed, where the build-up of oscillations from noise to full power must occur reliably for every pulse in a time that may be as short as one-hundredth of a microsecond. Failure of this build-up produces misfiring or mode changing, and often occurs under the proper conditions.

From the preceding discussion it is clearly seen that the understanding of pulsed operation involves new concepts, some entirely different from those in CW operation. Since the magnetron consists basically of an emission system involving electron flow, plus resonators (or cavities) which modify the electron flow, and a means of extracting the r-f output, a discussion of the functioning of each of these items logically leads to a better understanding of the magne tron oscillator.

First consider the emission system, which may be a straight filament, a coiled filament, or an oxidecoated cathode cylinder. Magnetrons using thoriated tungsten or pure tungsten filaments are generally operated at high temperature; because of their ruggedness, these filaments are suitable for c-w type tubes, but consume considerable fdament power. The low-temperature, oxide-coated filaments operate best for pulsed-type tubes, producing much larger emissions than the high-temperature type (for a given filament power). However, since they are not as rugged, they are more susceptible to damage from electron bombardment and deterioration effects. The oxide coated cathode cylinder provides the most practical construction for low-temperature operation; keeping the heater fdament independent of the operating circuit avoids any fdament inductance effects which might adversely affect the frequency of operation. Another type of operation is also possible with the cathode sleeve, namely, cold-cathode operation. Because of the extremely high secondary emission produced by electron bombardment of the cathode by electrons out of the useful orbit, once started by heated-cathode operation, cold-cathode operation may be obtained by lowering the heater voltage or by removing it entirely. Such operation is commonly used in high-powered magnetrons, operating with extremely high plate voltages and heavy electron bombardment of the cathode.

Since it is desired that the electrons travel in the interspace area between the anode and cathode of the cavity block and thus contribute to the excitation of the various cavities, end shields are placed at the ends of the cathode. These shields, which are of various designs (some may be only small protuberances at the ends of the cathode), minimize the electron leakage paths at the ends of the cathode. These cathode end shields are considered to operate by producing a retarding electrostatic field at the ends of the interspacial area. By distorting the equipotential lines at this point in such a way as to produce an inwardly directed force upon the electrons attempting to leak out of the area, they simply urge the electrons toward the center plane of the anode block. While in some cases secondary electrons may also be emitted from the end shields, through bombardment by partially controlled electrons in orbit, the useful electron emission is usually restricted to the cathode alone. An exaggerated illustration of end shields and the retarding field they produce is shown in the following illustration.



**Cathode End Shields** 

With the cathode emitting a stream of electrons into the interaction space, let us examine the method by which the electrons produce oscillation. A halfsection of a typical eight-cavity anode is shown in the following illustration, with the fields and current flow as indicated.

Assume for the initial operation that the cavities have been excited by an r-f field so that each cavity is oscillating. In the capacitive space between the walls of the entrance to the cavity (slot) a charge exists, with one wall negative and the other wall positive. By construction, the segments are placed 180 degrees apart electrically (pi mode), so that when traveling from one cavity to the other in the interaction space, each cavity is oppositely polarized. Thus the original negative-to-positive charge in cavity 1 is now a positive-to-negative charge in cavity 2, and likewise for the other cavities around the interaction space. A complete cycle of rotation around the anode block is produced in 360 degrees of rotation or some multiple thereof. In the case illustrated, since there are eight cavities (only half are shown) and the phase shift between the cavities is 180 degrees, there is a total of 8 pi radians shift which, when divided by 2 pi (for one full 360° of rotation), gives a number of 4. This arbitrary number is called a mode number. As might be surmised, magnetrons can be constructed so that they will operate at a different number of modes for the same frequency.



**Development of Internal Fields** 

Examine the illustration and observe the effect of the fields produced. First the r-f field at the entrance to the cavity is strong at the lip but weaker as it -extends into the interaction space, as shown by the widely separated lines. Arrows indicate field direction. The straight lines between the anode and cathode represent the dc field produced electrostatically by the anode-to-cathode potential. The dc field is steady except where reinforced or reduced by the changing r-f field. The permanent magnet field is at right angles to it (into the page), and is not shown. Thus two fields are always present in the cavity, and the resulting field affecting the electrons is the vector sum of the two.

Recalling from basic magnetron theory that when an electron approaches an anode it induces a positive

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### **ELECTRONIC CIRCUITS**

charge, and as it recedes from the anode it induces a negative charge. It is evident that as an electron approaches an anode which is going positive (because of the r-f cavity field), that segment is made more positive, aiding cavity oscillations. If the electron recedes from the anode as it is going negative, oscillations also will be aided. On the other hand, if the electron approaches the anode as it is swinging negative, or recedes as it swings positive, the electron tends to oppose oscillations. If sufficient electrons were so phased, oscillation would stop. Therefore, to sustain oscillation the phasing must be such as to produce more aiding than opposing electrons, or to remove those that oppose the oscillation, retaining only those that aid.

In addition to the r-f fields existing because of cavity resonance, assume that the magnetic field is just slightly greater than the cutoff value. Therefore, if the r-f oscillating field did not exist, or were zero at a point in the interaction space, the electron emitted at the cathode would be returned by the effect of the dc magnetic field. On the other hand, when r-f field is going positive, the electric field is enhanced, and an electron emitted at a point affected by this field would be attracted toward the anode. Because of the effects of the two fields, the electron is forced to travel in a cycloidal path instead of straight, and around the interaction space in a clockwise or counterclockwise direction (depending on the polarity of the magnet). If the distance between the cavity segments is such that the electron traverses the space between adjacent slots in a time equal to one-half cycle of r-f oscillation, when the second slot is reached the electric field will be reversed (the next half-cycle of r-f oscillation is now starting) and will be in an aiding direction. Because of the curved path, however, the *working* electron is traveling in a long path and through a decreasing potential (since the potential through which it falls is less as it approaches the anode). The result is a change in phase of such a mture that by the time the electron approaches the third slot the polarity is opposing and repels the electron. Thus the electron is forced to curve back upon itself, and, by the time it is traveling towards the direction from whence it started, the field in segment 2 is again attracting it, and it again curves toward the



#### **Electron Path**

anode. Likewise, because of the curved path it enters the number 1 segment field when the field is in a direction that pushes it back toward the number 2 and 3 segments. In this way the working electron follows a series of looped paths between two segments, as shown in the preceding figure until it reaches the anode. During the time it is being attracted by the field, it effectively aids oscillation in that cavity just as if an additional charge were induced into it. Because of the curved path it is in an aiding condition longer than it is in a position where it removes energy from the cavity; therefore, the net result is to enhance the oscillations. Since the distance traversed between segments is effectively 180 degrees, the electron is operating in the pi mode. Thus in an eightcavity magnetron, four pairs of segments are operating simultaneously, and the effect is the same as that existing in a polyphase motor; that is, an effective traveling field is produced which rotates around the circumference of the interaction space, and oscillation is successively enhanced in each cavity as the field rotates past the slot. The effect is as though a wheel of four spokes were being rotated, as shown in the following figure.

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### OSCILLATORS

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**Rotating Electron Field** 

Conversely, the non-working electron is emitted at a time during which the r-f field opposes it and is quickly directed back to the cathode. This is a harmful electron in that it strikes the cathode with considerable force and tends to destroy it. Since the back radiation cannot be eliminated, it is used to produce secondary electrons and economize on filament heating.

Since there are electrons emitted from all points on the cathode, there are electrons which start at intermediate points of changing field, and are not attracted or repelled as strongly as the working electron; therefore, their paths are of different orbits. However, since the r-f field varies sinusoidally with time, the result is that the electron emitted before the working electron is retarded until the electron emitted after the working electron catches up. For this reason there is an effective electron density grouping (or bunching) about the working electron, or a *velocity* modulation effect similar to that in the klystron. Thus standard waves similar to those on traveling wave tubes are caused to exist in the inter-action space.

While the r-f filed was initially assumed, it is produced by application of the anode voltage or negative cathode driving pulse, which is sufficient to shockexcite the cavities, and with the proper phasing oscillations are built up. This proper phasing is produced  $\checkmark$  through construction and by the proper selection of anode voltages and field strength. Since the phasing of magnetrons is a highly technical subject and of concern only to the designer, it is beyond the scope of this technical manual and will not be discussed.

**Types of Cavities and Modes.** There are basically, three different types of cavities used in unstraped resonant systems; these are the slot, the vane, and the hole-and-slot types of side resonators shown in the following figure.





Regardless of the type of resonator used, it is primarily the simple equivalent of a parallel LC tuned circuit, which can be represented schematically by a series of tank, as shown in the following illustration, the interaction space is represented by capacitance between the anode and cathode; inductive effects are neglected for simplicity.



**Resonator Equivalent Schematic** 

While the resonators are shown connected in series, actually each one is independent and is dimensioned and shaped so that all are resonant to the same frequency (identically shaped resonators are used). They are coupled together by the interaction space between the cathode and anode. The spacing of the cavity entrances is approximately a half-wave at the desired frequency of operation (assuming the pi mode of operation). Therefore, the smallest number of cavities that are operable is two (2x 180 equals 360 degrees), corresponding to split-plate usage. The maximum number of cavities is limited only by construction since multiplication by two produces the same result (2, 4, 8, 16, 24, and up to 64 as a practical limit).

Consider now the mode of operation. Assume a basic six-cavity magnetron, as shown in the following illustration; operation is possible in three types of modes, as shown.



Examples of Various Modes

In part A of the figure there is a phasing of 60 degrees between adjacent segments. Therefore, six segments must be traversed before a total phase rotation of 360 degrees (one cycle) is obtained. Since there are 2 Pi radians in 360 degrees by angular measure, this represents a rotation of 2 Pi radians divided by 2 Pi, or mode 1. In part B of the figure the segments are separated 120 degrees, and only one-half as many segments (three segments) need be traversed to produce a complete cycle of operation. When the complete cycle around the magnetron is traversed, a total of 720 degrees of ratation is completed (two complete cycles of operation), or 4 Pi, giving mode 2. In part C of the figure adjacent segments are oppositely polarized, so that only two segments need by traversed to complete a cycle. Therefore, in a complete rotation of the magnetron cavity, 1080 degrees

of rotation is produced, or 6 Pi radians divided by 2 Pi, giving mode 3.

Since a six-cavity magnetron can operate in at least three modes (with either leading or lagging phase, this represents 2 x 3 modes, or a total of 1 mode for each cavity), there is a frequency for each of these modes at which the output is a maximum. Thus the magnetron generates a series of discrete frequencies arranged symmetrically (in the ideal case) around a center frequency of maximum amplidude for each mode. A typical plct of wavelength variation with mode for typical magnetron is shown in the following graph.



Wavelength vs Mode Variations

The c-w magnetron provides a different output from that of the pulsed magnetron, in that a steady anode voltage is supplied, and the output is mainly concentrated at the mode chosen by the plate voltage and current applied. It still does not consist of a single frequency, however, since the cavity at microwave frequencies can support a number of different types of oscillation. This concept is diametrically op posed to the normal concept of a tuned tank being responsive to only one frequency. It is true, however, because the magnetron consists not of a single cavity, but of a number of cavities, each coupled to the other. As in coupled circuits at the lower frequencies, it is possible to achieve a response curve having a main lobe with numerous side lobes, depending upon the interaction and amount of coupling between the

### **ELECTRONIC CIRCUITS**

cavities. This condition is further complicated by the possibility of phased bunching of electrons in the interaction space; thus it can be clearly seen that a single pure frequency output is rather unlikely. In the tunable types of magnetrons, the main spectrum can be shifted to the desired frequency by tuning. In the fixed-tuned magnetron, operation consists mainly of operating at the proper current, which for a pulse of a particular shape produces the desired main lobe at the proper frequency with a minimum of side lobes (other modes). A typical output spectrum for a pulsed magnetron is shown in the accompanying figure.





Microwave Magnetrons, from which much of this – material was selected.

Since the unstrapped magnetron presents a number of modes of nearly equal outputs, it has been discarded for the sfrapped type, and for a special type known as the rising sun magnetron because of the design of the cavity. Strapping consists of connecting together alternate segments with short, heavy conductors, as shown in the accompanying figure. Thus



**Double Ring Strapping** 

The broad spectrum shown is caused mainly by pulsing. Because the pulse is a rectangle with steeply sloping sides, it approximates a square wave with a similar harmonic content. Thus, in effect, many frequencies are induced into the cavities, and all those to which it responds will be present. The shape of the anode pulse is important, since it can cause a distorted output and place the main output energy in an unwanted portion of the spectrum. It should also be understood that this discussion is necessarily general since it concerns actions mostly of interest to the designer. The technician is concerned with making the magnetron perform as designed. He can control only the voltages applied and the currents at which it is operated, plus any cavity tuning which may be possible. Therefore, the preceding discussion of modes and spectrum effects is intended to indicate, in a very limited manner, internal operation effects which are highly complex and beyond the scope of this circuit analysis. The interested reader is referred to standard texts such as the Radiation Laboratory volume on

strapping favors mode 3, the Pi mode, and places alternate segments at the same potential (which corresponds to a shift of 2 Pi radians). Operation at mode 2 is impossible, since it would require a shift of 4/3 Pi radians between alternate segments, and cannot occur with the segments short-circuited. While the straps are essentially simple short circuits, at the frequencies used they have inductance; moreover, since the straps pass near the segments which they connect, they also have capacitance. As a result, the -frequency of the mode of operation is slightly altered. At the Pi mode the straps are at the same potentirds at the ends, and carry no current (except for a slight capacitive current between them); therefore, the inductance is negligible and the capacitive effect predominates, lowering the basic frequency of the Pi mode. When the magnetron is excited in a different mode, there is a difference in potential between the segments, causing the straps to carry more current between them because of the difference in potentials. Thus both inductive and capacitive

effects operate on the other modes, changing their operating frequency. The result is to further separate the modes and eliminate the possibility of simultaneous operation on two closely spaced modes. Suppression of the unwanted modes increases the over-all efficiency of the magnetron. While it might appear that the symmetry of strapping is essential, this is not so in practice. Actually, by omitting certain straps (usually the ones at the output resonator and adjacent to the input cathode), even greater discrimination is obtained.

The rising sun magnetron design evolved from the fact that symmetry is not required for best results in strapping. The typical design of alternate cavities of the same shape, with adjacent cavities of dissimilar shape, produced the so-called "rising sun" des'ign. Since the sizes of the cavities in the two groups are different, the mode frequencies of this type of magnetron tends to form into two groups as though there were only two resonators. Thus the respective mode frequencies are well separated from the Pi mode, and this unit is suitable for Pi mode operation without the use of strapping. The rising sun design is used at the higher frequencies (above 10 GHz), while strapping with the conventional design is used at the lower frequencies to provide a smaller assembly. A typical rising sun design is shown in the following illustration.



**Rising Sun Magnetron** 

**Coupling Methods.** F-R energy is usually removed from the magnetron by means of a coupling loop. At frequencies lower than 3 cm the coupling loop is made by bending the inner conductor of a coaxial line into a loop (center-fed coupling) and soldering the end to the outer conductor, so that the loop projects into the cavity, as shown in the following figure.



Coaxial (canter-fed) Coupling Loop

At the higher frequencies to obtain sufficient pickup the loop is located at the end of the cavity (halo loop), as shown in the accompanying illustration.



External (halo) Coupling Loop

Other forms of inductive couplings are shown in the following illustration.

In the segment-fed loop it is presumed to intercept the flux passing between cavities, while the strap-fed loop intercepts the energy picked up between the strap and the segment. On the output side, the coaxial line feeds another coax line directly, or it feeds a **waveguide** through a choke joint, with the vacuum seal at the inner conductor helping to support the

line. Direct waveguide connection is usually through a slot in the back of the cavity, with an iris feeding into the waveguide connector through a window.



Segment-Fed Coupling Strap-Fed Coupling

**Tuning. The** magnetron is basically fixed-tuned. It is pretuned by adjusting the straps, pressing them in or out to resonate with a test voltage inserted into the cavity from a klystron at the desired operating frequency; the adjustment is made for maximum response on a detector-indicator. Some magnetrons have a flexible plate arranged to move in or out by means of a screw adjustment. Still other magnetrons have pins or rods that screw in or out of the cavities (as in the klystron), and some low-powered types are voltage-tuned. Usually, pretuning is necessary before the magnetron is placed in operation; therefore, some form of mechanical tuning which can be externally performed over a small range tuning which can be

adjust it to the desired operating frequency. (Of course, this frequency must be within a specified band of frequencies over which the magnetron is designed to be operable.) Thus in most cases the magnetron output frequency is essentially fixed, with the receiver having its bandpass and frequency automatically centered and maintained in synchronism with the transmitting magnetron.

### Failure Analysis.

No Output. Lack of output can be caused by nonoscillation of the magnetron, or by oscillation on an undesired mode which will not couple to the output circuit; it can also be caused by a short circuit or an open circuit. Use of the ammeters and voltmeters supplied with the equipment will usually pinpoint the trouble. A steady high current with low applied anode voltage usually indicates a loss of magnetism which allows the electrons to pass directly from cathode to anode. In this case, remagnetization or replacement of the magnets will generally restore operation. (Sometimes insertion and reinsertion of the small soft iron bar placed between the magnet poles during storage, known as the keeper, a few times will restore the magnet.) An anode-to-cathode short will produce heavy plate current and blow fuses or operate protective circuits immediately after the plate voltage is applied. Such a condition will be indicated by a simple ohmmeter check between the anode and cathode, with the voltages removed.

An erratic heavy plate current, usually accompanied by noise and internal flashes within the magnetron (seen through the coupling ports or at visible portions of the glass envelope), particularly in highpower magnetrons, indicates arcing. This is a common occurrence after periods of long idleness or after exceeding the permissible ratings; it can also be caused by land changes or discontinuities in choke or rotating joints, producing excessive r-f reflections. Immediate reduction of plate voltage is imperative to prevent damage to the magnetron or modulator equipment. Then, by following the normal seasoning process, the arcing should occur less frequently until the magnetron stabilizes and resumes normal operation.

If there is no output until a number of starting attempts have been made and the output then builds up slowly, this is a possible indication of an open **filament**. Particularly with extremely high-powered tubes using very high voltages, the phenomenon of cold cathode operation can occur through the back bombardment effect. Checking the filament for continuity with the plate voltage removed will quickly determine whether this condition exists.

Since magnetrons are expensive and usually do not plug in as conveniently as common receiving tubes, replacement of the magnetron should be resorted to only after all other checks have been made. Where the current meter indicates zero, it is most probably an open circuit caused by cathode burnout, an open anode or cathode lead, or failure of the modulator or power supply. Checking with the voltmeters provided on the equipment will quickly determine whether the power supply and modulator are normal; if they are, the open must be between these units or within the magnetron. A resistance check for continuity of connections will indicate whether the condition is external to, or within, the magnetron. Do not overlook resetting any overload relays or replacing open fuses in the search.

Reduced Output. Reduction of output below normal is usually more difficult to analyze than lack of output, since the magnetron is very susceptible to variations in the strength of its magnetic field, anode voltage, and load impedance. Such variations cause a loss of output power and efficiency to a large extent, and usually affect the frequency of operation. A shift in the mode of operation can usually be caused by any of the previously mentioned items, and, since the magnetron is normally designed to operate at a particular frequency with maximum output, reduced output may indicate such a condition. Perhaps the best method of trouble shooting is to use a spectrum analyzer such as the echo box, detector, and meter, or by direct observation of the r-f envelope on an oscilloscope. Since the shape of the high-voltage modulator pulse is important, using a portable spectrum analyzer connected via a directional coupler to the magnetron output will save time. Double moding will be indicated by the presence of two or more maximum lobes. A jittering pulse which changes in amplitude or wiggles back and forth is immediately apparent. Changes in load can be made and the effect observed and evaluated. Likewise, the anode voltage can be varied and its effects observed; any frequency instability will be evident. The effect of reduced output will be obvious from local meter indications in the case of c-w magnetron type of operation, but they are not as accurate and are sometimes actually

misleading in pulsed operation. A change in current or voltage will show immediately in the steady voltage type of c-w operation. However, in pulsed operation, where the pulse width and duty cycle govern the average value of the current and voltage, a change in pulse width may compensate for a change in duty cycle (or vice versa); thus the pulsed indications may appear normal, when actually there is a reduction in efficiency and output power. Low power output usually results from a weak magnetron or low modulator output. If the modulator pulse is normal, the trouble lies in the magnetron. A weak magnet will cause a loss of power, by reducing the efficiency of operation, and also a change in the spectrum, which is usually obvious on the oscilloscope. For further information, test, and typical waveforms, refer to Test Methods and Practics, NAVSHIPS 0967-000-0130, of the EIMB.

Incorrect Frequency. While magnetron troubles may be divided into three general classifications, namely, wrong frequency, poor spectrum, and low output, they are usually interlinked. For example, a magnetron operating off frequency will most probably show a poor spectrum and produce a lower output, as compared with previously recorded data obtained when the magnetron was known to be operating correctly. In the case of wrong frequency operation for fixed-tuned magnetrons, there are three possible causes. The magnetron may be defective, or frequency pulling or pushing may be present. Frequency pulling may be present because of some fault in the r-f system, such as varying impedance, faulty rotating joints, or be caused by a strong reflection from a nearby object. A change in magnetron frequency due to a change in load impedance is known as "pulling". The effect of pulling is greatest at high output powers. The operating point of a magnetron is usually a compromise between high output power and good frequency stability, and is usually chosen for a matched load condition. Magnetron performance is often summed up in what is called the pulling figure. This figure is the total change in frequency (usually in MHz) which occurs when the load is adjusted to produce a voltage-standing-wave ratio of 1.5: 1, and the phase of the reflection is varied through 360 degrees.

When off-frequency operation occurs and another magnetron is substituted, satisfactory operation of the replacement does not necessarily indicate that the

original magnetron is defective. In some cases a magnetron may be in good condition, but because of individual difference it may be more easily pulled outside the operating band by externrd conditions (such as a change in load impedance) than another magnetron of the same type number. Blind replacement of the magnetron when off-frequency operation occurs, therefore may result in the discarding of a perfectly good tube. The VSWR of the r-f system should first be checked to determine whether it is high or low. With a low VSWR, normal operation of the r-f system is indicated, and the fault is most likely the magnetron. Sometimes the effects of pulling are not noticed if the frequency is within the operating band, so that occasional off-frequency operation is possible without any visible external indications. Frequency pushing (indicated by waveform distortion) may be present because of improper anode or filament voltage. Magnetron pushing, caused by a change in dc anode voltage, is frequently indicated by a poor spectrum shape; this condition results from improper modulator pulse amplitude or shape. The frequency of operation may be slightly altered, or may change from pulse to pulse. Although such operation maybe indicated by a changing anode current, a more definite check can be made by use of an oscilloscope.

Magnetron pushing is usually produced by a change of input conditions. The pushing figure is usually expressed in terms of megacycles per second per ampere. In most cases pushing can be neglected for the longer wavelengths where it is slight. It cannot, however, be neglected at the shorter wavelengths. Regardless of the cause of the frequency change, in the case of the tunable magnetron, only a slight adjustment of the tuning control to establish the desired frequency may be all that is required.

When frequencies appear and disappear in the spectrum, the cause is usually arcing, which produces temporary transients. If this condition occurs frequently, seasoning is necessary; there is also the possibility that the magnetron is becoming unstable and approaching the end of its useful life. If it occurs infrequently, operation can be considered normal, but there is the possibility of incipient magnetron failure.

### **REFLEX KLYSTRON OSCILLATOR**

#### Applications,

The reflex klystron is used as a low-power r-f oscillator in the microwave region (from 1000 MHz to 10,000 MHz) in receivers, test equipment, and lowpower transmitters.

#### Characteristics.

Uses special tube construction to produce r-f feedback and oscillation.

Operates as a positive grid oscillator.

Uses a tuned cavity, either integral (built-in) or external, to determine the basic range of operation. Uses negative anode (repeller-plate) voltage.

### Circuit Analysis.

General. A klystron tube is a specially constructed electron tube using the properties of transit time and velocity modulation of the electron beam to produce microwave frequency operation. It can be used as an oscillator or an amplifier. The amplifier employs two or more cavities to produce the proper bunching of electrons, upon which its function and amplifying properties are based. The amplifier type of klystron can produce a large amount of power (up to megawatts) and can be used as an oscillator if proper feedback arrangements are made. However, the reflex klystron offers a simple type of feedback arrangement and performs specifically as a special tube designed for oscillator operation alone. Although the power output of the reflex klystron is limited, it is adequate for receiving and test equipment functions and for low-power transmitters. Where high power is required, it can be achieved by using the reflex klystron as a master oscillator and the conventional amplifier type klystron as a power amplifier. Since microwave radiation is limited to line-of-sight distances, the reflex klystron usually furnishes sufficient power for these relatively short rf transmission paths.

Generally speaking, although the efficiency of the klystron is low as compared with efficiencies obtainable with conventional tubes at the lower frequencies (on the order of 30% as compared with 60%), it is more efficient than the other types of high-frequency generators in the microwave region. The negative grid tetrode provides approximately the same efficiency at 500 MHz, but its output drops to zero around 1500 MHz; similarly, the lighthouse tube covers a range of from 800 MHz to 2500 or 3000 MHz with comparable efficiencies and then its output drops off; the multicavity klystron, however, is operable up to 10,000 MHz and beyond with efficiencies not less than 1 0%. In this respect, the reflex klystron offers the lowest efficiency (on the order of 2 or 3 percent) mostly because of its simplicity of construction. For example, the use of more cavities to provide better bunching would give higher efficiency. Actually, the klystron is the only device other than the magnetron (and perhaps the traveling wave tube) which offers practical operation on the microwave frequencies; it is simpler and cheaper than the magnetron (or TWT) and more flexible in its applications, which is the reason for its popular use. Present trends indicate that the reflex klystron will be replaced for high-power operation by the two- or three-cavity klystron, but for simplicity and economy for low-power applications the reflex klystron is more practical.

The klystron has a large power gain than the negative grid tube at the higher frequencies because the tetrode primarily has a smaller cathode area, is limited in the amount of plate voltage that can be applied, and has greater r-f losses. The advantages of the klystron accrue because the cathode is not limited in size but can be made as large as necessary, and, being outside the rf field in the tube, it is unaffected by radio-frequency bombardment or other deleterious effects. Although the negative grid tube has a closely spaced grid and plate (to reduce transit time effects), and distance between the anode and the cathode in the klystron is large (on the order of one inch), permitting larger applied plate voltage before breakdown occurs. Since there is no grid structure in the klystron to heat and cause losses (actually, grids are sometimes used, but are very rugged) and the collector is located outside the r-f field and designed solely to dissipate heat, better efficiency results. The major loss in the klystron is dielectric loss (such as the loss produced by windows in cavities for waveguide couplings), as well as wall absorption. Thus, the r-f gain is limited only by the small r-f input cavity loss and by beam loading of the output cavity. Normally there is no negative feedback to be overcome by virtue of interelectrode couplings, as in the

negative grid tube, since the input and output cavities are isolated. In the case of the reflex klystron, positive feedback is obtained by the use of a repeller electrode so that only one cavity is required.

In the preceding discussion, a number of generalities were made to bring out the inherent differences between negative grid tubes and the klystron. Since the subject of klystrons and their design considerations cover a large field, which is beyond the scope of this text, and since there are so many variations between different products, it is possible that exceptions to some of the generalities can be made. In fact, considering reflex klystrons alone as a small branch of a large family of klystron tubes, there are a number of variations in design from type to type. Therefore, the interested reader is referred to other texts for specific data on a particular type or design, and the generalities made herein should be viewed broadly. The discussion that follows will be restricted to basic principles which can be applied to any type of tube.

The operation of the klystron is predicated upon the development of velocity modulation of the electron beam; that is, the velocity of the electron beam is controlled to produce a grouping or bunching of electrons. These bunches of electrons are then passed through grids or cavities to produce oscillations at the desired frequency by direct excitation of the cavities. A basic klystron (not reflex type) is shown in the following illustration to establish the fundamental principle of operation. As shown in the figure, a



Basic Klystron

heater is used to produce electron emission from a cathode. The electrons from the cathode are attracted to the accelerator grid (No. 1), which is at a postive

potential with respect to the cathode. The accelerator grid may be a flat grid structure or an annular ring (cylinder or sleeve) through which the electrons pass unhindered. Assume that this attraction produces a constant-velocity electron beam, which is further attracted to the next electrode, the buncher grids (or cavity), and then to the next electrode, the catcher grids (or cavity), also at a higher positive potential. If the output from the catcher is fed back to the buncher, and if the proper phase and energy relations are maintained between the buncher and the catcher, the tube will operate as an oscillator. The collector plate, which is also at a positive potential, serves only to collect the electrons which pass the catcher. Successful operation requires that the energy needed for bunching be less than that delivered to the catcher. Amplifying action is obtained because the electrons pass through the buncher in a continuous stream and are effectively grouped so that they pass through the catcher in definite bunches or groups as explained in the following paragraphs.

Bunching is produced by applying an alternating voltage to the buncher grids (produced by excitation of the buncher resonator by the passing electron beam). Assuming that a sine-wave voltage is produced and applied between the buncher grids, it is evident that on the positive alternation the buncher grid nearest the catcher effectively has its positive potential increased, and therefore further accelerates the electron flow. On the negative alternation, the same buncher grid voltage is made less positive and the electron stream is slowed down. Since a continuous stream of electron enters the bunching grids, the number of electrons accelerated by the alternating field between the buncher grids on one half-cycle of operation is equalled almost exactly by the number of electrons decelerated on the negative half-cycle. Therefore, the net energy exchange between the electron stream and the buncher is zero over a complete cycle of alternation, except for the losses that occur in the tuned circuit (cavity) of the buncher.

After passing through the buncher grids, the electrons move through the drift space in the tube with velocities which have been determined by their transit through the buncher grids. Since in a conventional klystron the drift space is free of any fields, at some point in this drift space the electrons which were accelerated will catch up with these which were previously decelerated (in a prior passage) to form a bunch. The catcher grids are placed at this point of bunching (determined by frequency and transit time), to extract r-f energy from the bunched electrons.

At the catcher a different situation exists. Since the electrons are traveling in bunches, spaced so that they enter the catcher field only when the oscillating circuit is in its decelerating half cycle, more energy is delivered to the catcher than is taken from it. The remaining electrons in the beam pass through the grid and travel to the collector plate, where they are absorbed.

In the *reflex* klystron, the catcher grids are replaced by a repeller plate, to which a negative potential is applied, as illustrated in the accompanying figure.



Reflex Klystron

In this type of klystron, the electron beam is also velocity-modulated, and, by proper adjustment of the negative voltage on the repeller plate, the electrons which have passed the bunching field may be made to pass through the resonator again (in the reverse direction) at the proper time to deliver energy to this circuit. Thus, the feedback necessary to produce oscillation is obtained and the tube construction is simplified. Spent electrons are removed from the tube by the positive accelerator grid (when used) or by the grids of the positive buncher cavity. Energy is coupled out of the cavity by means of a one-turn hairpin coupling loop. The operating frequency can be varied over a small range by changing the negative potential applied to the repeller, because this potential determines the transit time of the electrons between their first and second passages through the resonator. Since maximum output depends upon the fact that the electrons must return through the resonator at just the time when they are bunched and at exactly the decelerating half-cycle of oscillating resonator grid voltage, the output is more dependent

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than the frequency upon the repeller potential; therefore, the amount of tuning provided by varying the repeller voltage is limited. Usually the volume of the resonator cavity is changed (by mechanical tuning) to make a coarse adjustment of the oscillator frequency, and the repeller voltage is varied over a narrow range to make a fine adjustment of the frequency (electronic tuning) consistent with good output. Since the same grids perform the dual function of bunching and catching in the reflex klystron, they are frequently referred to as the buncher-catcher grids. Because of the variation of frequency with accelerating voltage, it is difficult to achieve linear amplitude modulation with a klystron. Frequency modulation may be readily accomplished, however, by introducing a small modulating voltage at the cathode or repeller. The tuned circuit used in the reflex klystron is a cavity resonator, which has a very high Q. Depending upon the tube type, the cavity may be an integral cavity (built into the tube) or an external cavity (clamped around the tube). Several methods are used to tune cavity resonators. Capacitive tuning is provided by mechanical varying the grid gap spacing; inductive tuning is provided by moving screw plugs in or out of the cavity (this changes the volume, making it either smaller and tuned to a higher frequency, or larger and tuned to a lower frequency). In some instances thermal tuning is used by applying heat to grid gap to produce capacitive variations. Several types of output couplings are used, but the coupling loop is the most popular type. Capacitive probe coupling is often used with the external type of cavity because construction difficulties do not readily permit the use of coupling loops with this type of cavity. At frequencies above 10,000 MHz waveguides are employed, and the output is coupled to the waveguide through a window or aperture.

**Detailed Analysis.** In the practical klystron, the function of the accelerating grid is provided by the cavity, which is maintained at a postive potential sufficiently strong to produce the initial effect of accelerating the electrons to a constant velocity. A focus electrode, in the form of a cyclinder connected to the cathode, is also provided to confine and effectively focus the electrons into a narrow beam. Focusing is achieved electrostatically without any external control. Any electrons which travel outside the beam are intercepted and removed, while those within the beam are attracted by the strong positive cavity field and accelerated uniformly. A typical

reflex klystron, showing the focusing electrode and the cavity structure, is illustrated in the accompanying figure.



Practical Reflex Klystron

Note the particular shape of the cavity, which has a post-shaped center hole. As a result of this construction, the cavity is very narrow at the point (the gap) where the electrons pass through it. The narrow gap is necessary for proper operation since the transit time through the cavity must be much less than the time for a complete cycle at the frequency of operation. Beyond the center hole the cavity is much larger. The portion of the cavity at the gap where the ends are close together may be considered capacitive in effect, and the remaining portions, where the capacitance is small, may be considered inductive in effect. Consider now the operation of velocity modulation. Since the cavity is developed as a quarter wave coaxial resonator, the input and output ends are at opposite polarities. Also, the current distribution is approximately uniform at the center, where the beam passage takes place. Hence, in the gap a uniform electric field is produced. The passage of the electron beam through this field will distort the field and cause energy to be absorbed from the beam. Thus, the cavity is excited, and it oscillates at a frequency determined by its dimensions. These oscillations produce opposite polarities at the entrance (grid 1) and exit (grid 2) grids, because the sides of the cavity are exactly one quarter wavelength apart at the operating frequency. By virtue of resonance and the use of a high-Q cavity, the r-f oscillations develop a large

instantaneous voltage, which on the positive alternation places the exit grid at a more positive potential than the entrance grid. As a result, the exit grid is polarized in the proper direction to attract the electron beam and increase the electron beam velocity. See the following illustration for a representation of the cavity action.

, EXIT GRID , EXI which were accelerated meeting those which were not accelerated, but which passed through the gap at a later time, and also by those decelerated electrons which passed through at a still later time. A typical Appfegate diagram illustrating the bunching effect is shown in the accompanying figure.



### **Applegate Diagram**

On the negative alternation the beam is opposed and effectively slowed down. At and near the changeover points, the ac oscillation voltage is practically zero so that the beam is not affected and it passes through with the initial velocity. The alternate acceleration and deceleration of the beam, together with the ineffective period of no change produces a bunching of the electrons. (In effect, the bunches of electrons occur at a period equal to the frequency of oscillation. Thus, actual density modulation is produced, resulting in an alternating current varying in strength at the frequency of operation, which when absorbed by a resonant cavity will cause rf oscillations.)

Before the electrons with different accelerations are completely bunched, they enter into the repellerplate field, which is negative and repels the electrons. An electron which was accelerated by the field at the cavity grids will penetrate the electric field at the repeller plate to a greater depth than one which was accelerated less or not at all, and will require a longer time to return to the cavity. Thus, bunching can be achieved by adjustment of the repeller plate voltage to the optimum value. When the voltage is optimized, bunches are formed at the cavity by those electrons

To more clearly understand buncher and catcher operation, we shall review the operation of the twocavity type of tube. Action is based upon the fact that electrons will give up energy when slowed down, and absorb energy when accelerated. In order for an electron to give up the greatest amount of energy to the catcher, it is necessary that the electron arrive at the center of the catcher at the instant when the electric field at the center of the catcher has its maximum negative (retarding) value. Similarly, in order for a symmetrical group of electrons to deliver as much energy as possible, the center of the group must arrive at the center of the catcher when the catcher field has its maximum negative value. Since the electron at the center of the group is the one that passed the center of the buncher at the instant when the buncher field was changing from negative to positive, the time  $s/v_0$  required by this electron to move through the distances from the center of the buncher to the center of the catcher, must be equal to the time interval between the zero of the buncher fields and a negative maximum of the catcher field, as shown in the following figure. It is evident from

# OSCILLATORS

examination of the illustration that for maximum energy transfer, the catcher field must lag the buncher field by the angle

$$\frac{S}{V_{c}} \times \frac{2\pi}{T} + 2\pi (\frac{1}{4} - n),$$

where T is the period of the field and n is any integer.



**Buncher-Catcher Phase Relationships** 

Up to this point nothing has been said regarding the means by which the catcher is kept in oscillation. The motion of an electron through a cavity resonator sets up an electromagnetic field within the resonator. In a klystron the electrons pass through the catcher in bunches; therefore, the fields resulting from individual electrons will, for the most part, reinforce each other and thus produce a resultant field of appreciable magnitude. Because the bunches pass through the catcher at time intervals equal to the natural period of oscillation of the catcher, the catcher is set into oscillation. Since the amplitude of oscillation can build up only if the catcher gains energy, the oscillation automatically tends to assume the proper phase relative to the cycle of arrival of electron bunches to result in maximum transfer of energy from the electrons to the catcher. Since the cavity of the reflex klystron acts both as a buncher and a catcher, if an output is to be obtained, the returning electrons must be phased so as to impart energy to the cavity and be absorbed. It is necessary that they approach the cavity when the buncher voltage originally induced is opposing them, or producing deceleration. Therefore, the time taken for a bunch to return to the cavity must be 3/4 of a cycle of the operating frequency to supply energy by feedback and satisfy the requirements for oscillation. The phasing must be such that

the electrons add energy to the cavity. Therefore, during the first quarter cycle they have not yet returned, and during the second quarter cycle they are in phase opposition ( $180^{\circ}$  apart), but at the 3/4 cycle they are in phase and will add energy to the cavity. A bunch of electrons which returns to the cavity at a time equal to 3/4 of a cycle, or any whole number of cycles plus 3/4 cycle, will supply energy of the proper phase for sustaining oscillations. Thus, oscillations may be obtained at a number of repeller plate voltages for a given frequency setting of the resonator cavity.

Oscillations of maximum amplitude are obtained when the frequency of operation, as determined by the return time of the reflected electrons forming a bunch, coincides with the frequency to which the resonator is tuned. Since only one resonator is used, the tuning of the reflex klystron is relatively simple. Although the frequency of operation for fixed cavity tuning may be varied by changing the repeller voltage, the power output drops off on either side of the cavity frequency because the field of the gap does not provide optimum retardation. The various values of repeller voltage which produce oscillation result in what is known as different modes of operation. The most negative repeller voltage for which oscillation results is known as mode 1. Lower values of repeller voltage successively produce the higher modes (2, 3, 4, etc) of operation. A typical output response with repeller voltage variation is illustrated in the following figure.

TRANSIT TIME WAVELENGTHS



Power Output vs Repeller Voltage

Since the bunching of the electrons for the highernumbered modes is not so well defined, the net

energy given up by the beam to the resonator field is less, and the output power is smaller, as illustrated. On the other hand, because the bunching is not so well defined, the modes of higher number are tunable over a greater range of frequencies (by adjustment of the repeller voltage). The accompanying illustration of electronic tuning ranges verses modes indicates that for the lower repeller voltages (mode 3) the range of electronic tuning increases but the output decreases.



#### **Tuning Ranges vs Modes of Oparation**

The variation of frequency with changes in the repeller voltage permits the reflex klystron to be used with an automatic- frequency-control circuit, which controls the klystron frequency by lowering (or by increasing) the repeller voltage in the proper direction to compensate for any frequency change. Thus, the circuit can be made self-tuning and provide reasonably good frequency stability, particularly in pulsed operation where voltages and pulse amplitudes change drastically. (See the Special Circuits Section of this handbook for a discussion of the various types of AFC circuits.)

**Tuning Methods.** The method used for tuning the resonator has an important bearing on the performance of a reflex klystron. Tuning is commonly accomplished by varying the length of the r-f gap, to adjust the capacitive portion of the resonator, although in some tubes the inductive portion is altered. Capacitive tuning requires small motions for large frequency shifts, particularly near the low-frequency end of the tuning range. This extra sensitivity can be either an advantage or a disadvantage depending upon the application. Generally speaking, it creates a problem when temperature compensation

is attempted because there must be considerable reduction of motion by a mechanical linkage between the control knob and the gap itself.

The use of capacitive tuning reduces the range over which reasonable efficiency is obtained. As the frequency is raised by lengthening the gap, the transit angle through the gap increases rapidly because the electrons have farther to go and less time to make the trip. The beam coupling coefficient also drops rapidly at the high frequencies so that the output drops quickly. On the low-frequency side of resonance, a similar drop-off occurs, but it is not so rapid. Since the resonator must incorporate a flexible diaphragm to permit capacitive tuning, problems arise in providing the proper vacuum seal; also, the tube is susceptible to changes cause by strong sound waves impinging on the diaphragm, and to changes in barometric pressure, which cause problems in aeronautical applications.

On the other hand, inductive tuning is usually less sensitive because larger mechanical motions are required to produce the same effect. In radial cavities, screw plugs are used (as many as four to six) for tuning. This method of tuning usually results in a **fixed-tuned** arrangement because of the mechanical difficulties in providing remote control of a number of plugs. However, since the transit time varies directly with the phase angle, rather than the 3/2 power as in capacitive tuning, much larger tuning ranges are available with inductive tuning. The largest tuning range (approximately 2 to 1) is provided by a coaxial cavity, but at greatly reduced efficiency (capacitive tuning range is about 0.7 to 1).

Mechanical tuning is usually employed in preference to thermal tuning because of the complexity of the frequency control circuit. Since the thermal motion is usually small, capacitive tuning is practically always used for thermal control. The main drawback of thermal control is thermal inertia, which prevents a rapid response to sudden frequency changes; as a result, overshoot becomes a major problem. In general, thermal tuning is used only for special applications where the simpler types of tuning are inadequate.

**Output Coupling.** Tubes with integral resonators usually have built-in output circuits that consist basically of a coupling device and an output transmission line. The most common pickup device is an inductive loop formed on the end of a coaxial line and inserted in a region of the cavity where the magnetic field is high. Aperture coupling, sometimes called iris coupling, is also used, but to a lesser extent than the pickup loop. In waveguide applications, the aperture is usually used for simplicity and convenience. For external cavity tubes employing coaxial-line tuners, a capacitive probe is sometimes used.

### Failure Analysis.

No Output. Incorrect or no plate voltage can prevent oscillation. An incorrect repeller voltage can usually be re-adjusted (within range of the control) to the proper value, or output frequency may be adjusted by tuning the cavity until the tube operates on some other frequency. Lack of oscillation for all values of repeller voltage and cavity tuning indicates an open circuit, loss of accelerator anode voltage, or a defective tube. With an external cavity klystron, poor electrode contacts can also cause lack of output. A voltage check will quickly indicate whether the potentials are normal. Note: Although low voltages are used, the cavity is positive while the repeller is negative so both supplies in series provide a possibility of dangerous shock. Observe safety precautions when testing. A tube with decreasing emission indicates incipient failure by a gradual reduction of plate current, and failure to oscillate at the usual repeller control settings. Such a condition becomes progressively worse over a period of time, and complete failure can be anticipated. Loss of output when automatic frequency control is used can result from failure of the AFC circuits; this type of trouble can be determined by switching to manual and noting whether normal tuning occurs. Since the reflex klystron is an integral unit with only output and supply connections, complete loss of oscillation is usually due to mistuning, loss of supply" voltage, or a defective unit.

**Reduced Output.** In the majority of cases, reduced output is caused by mistuning or lack of proper electrode voltages. Mistuning can usually be corrected by a slight readjustment of the repeller voltage and the cavity tuning unless the tube or supply is defective. There is also a possibility that the output load has changed, requiring a readjustment of the controls. Where stub tuners are employed in the output circuit, reduced output may be caused by improper stub tuning. In either case, a slight readjustment of each of the tuning controls should quickly indicate which is

at fault. Operation on a lower mode due to incorrect supply voltage can be detected by a voltage check; this condition is usually indicated when the controls must be set to a position other than normal for maximum output, or when reduced output is obtained at the optimum adjustment point. If the supply voltages and load are normal, reduced output usually indicates incipient tube failure.

Incorrect Frequency. Slight changes in frequency can usually be corrected by making slight repeller voltage changes and by tuning the cavity. Normally a rough frequency setting is obtained by adjusting the cavity tuning, and a fine frequency setting with optimum output is obtained by adjusting the repeller control. A simple voltage check should indicate whether the repeller and cavity voltages are correct. If the cavity tuning is operable and the repeller voltage is correct, incorrect frequency operation can be caused only by load changes or by a change in the tube cavity mechanism with age. It should be possible to restore the frequency by proper load adjustment. Changes in the mode of operation can be detected by noting whether the tuning range is greater and the output is less. Where AFC circuits are used to maintain the frequency, a shift to manual control will quickly determine whether they are at fault.

Changes in frequency resulting from changes in temperature are usually compensated for by adjustment of the tuning controls; such changes may be caused by localized heating due to improper operation when power type klystrons are used, or by greater than normal ambient temperature changes. When proper operation and normal temperature are restored, the unit should again stabilize at the proper frequency. Unless thermal compensation circuits or devices are provided, it will be necessary to compensate by the use of manual tuning. It continued drift is observed, the tube ratings are probably being exceeded. Where a stable frequency is important, an AFC circuit is usually incorporated. Improper operation of the AFC can be checked by switching to manual operation and observing whether operation is normal.

# BACKWARD WAVE (CARCINOTRON) OSCILLATOR

#### Application.

The carcinotron oscillator is used to supply ultrahigh frequency and microwave frequency outputs for transmitting applications.

### Characteristics.

Frequency reange is from approximately 200 MHz to over 100 GHz.

Output is from a few milliwatts to 150 watts or more.

Efficiency is low, from about 10 to 30 percent.

Output frequency is determined by applied voltage.

An electron gun and magnetic field are used to produce electron bunching.

#### Circuit Analysis.

General. There are two general types of carcinotron in use, the "O" type and the "M" type. The first type uses an electric field to impart kinetic energy to electrons. The kinetic energy of the electron is then extracted by a traveling wave; in the second type, a combination of electric and magnetic fields are used to extract potential energy from the dc field, utilizing electrons as the pivot for this action. Since the O-type is simpler and easier to understand, discussion will be limited to that type. The backward-wave tube is similar to the traveling-wave tube except that basically it is an oscillator rather than an amplifier, and it is the backward component of the traveling wave which produces the action. The typical backward wave oscillator consists of a folded transmission line or waveguide operating in the TE<sub>1</sub>, O mode, constructed so that the waveguide winds back and forth across a center line which produces an axial component of the electric field. The total path length from one end of the tube to the other is on the order of 12 wavelengths, and in a typical tube it will cross the axis about 50 times. An electron beam is directed along the axis through holes in the structure. When this beam has suitable velocity, an interaction occurs between the electron stream traveling from left to right and the backward wave traveling from right to left. This infraction causes energy to be delivered to the backward wave by the electron beam, producing an r-f output.

**Circuit Operation.** The schematic of a typical backward oscillator of the folded type is shown in the accompanying illustration.



Folded-Line Backward Wave oscillator

As can be seen from the illustration, a beam of electrons from an electron gun is directed through a hole in the center of a series of rectangularly folded waveguide sections. The collector electrode is placed at the end opposite the accelerating anode, and a non-reflecting termination is also placed at this end of the waveguide (if it were used as an amplifier this would be the input end). The output is at the electron gun end of the tube. The electron gun is a typical Pierce type, using a filament connected to **a** cathode and a separate cylindrical accelerating grid or anode. The collector and accelerating anode are connected to a source of positive voltage to attract the electrons from the cathode. Changing this voltage over a ten to one range produces a two to one frequency change which is about the maximum tuning range possible. Backward wave oscillation may also be obtained from a tube using a helix instead of a folded waveguide; in this instance, the circumference of a single turn must be between a quarter and a half wavelength.

Although the Pierce electron gun produces a series of essentially parallel-path electrons, in some tubes there is a tendency for the parallel electrons to be deflected or to stray from the parallel path. This is overcome by adding a solenoid around the envelope of the tube whose axis is in a longitudinal direction.

# ELECTRONIC CIRCUITS

The focusing field of the solenoid deflects any stray electrons back into the electron steam so that they must travel through the center of the holes in the wave guide. The accelerating anode creates the initial electric field which attracts the electrons from the cathode, while the collector serves to collect the spent electrons after they pass through the wave-guide, and return them to the power source. The r-f output is coupled from the waveguide through a probe or an aperture in the end of the waveguide.

Normally, thermal noise produced by current variations in the electron beam produces a noise signal in the waveguide to initiate oscillation. The purpose of the waveguide is to provide a path for the r-f oscillations in proximity to the electron beam, so that interaction can occur between the beam field and the signal field. When a noise signal is generated within the waveguide it is offered a conduction path from the collector back to the cathode end of the tube through which the r-f output current flows. While the electron beam and r-f oscillation (backward wave) signal both travel at the speed of light, and path through the waveguide is longer. Therefore, the backward wave oscillations pass through the waveguide at a much slower speed than the electron, which passes through the center of the waveguide and follows the shorter direct path between cathode and collector. Note that while the electrons flow from left to right, the backward wave travels in the opposite direction from right to left.

When the backward wave oscillation field opposes the field of the electrons passing through the gap at the center of the waveguide, the electrons are decelerated, and are overtaken by other electrons. During the time the beam electrons are decelerated they relinquish kinetic energy to the r-f field which causes them to form in bunches. When the backward oscillation field increases at the gap it enhances the electron field and accelerates the beam electrons, and energy is transferred from the r-f field to the electron beam field. As the oscillating field and electron beam progress in opposite directions through the tube, more bunching occurs. Thus, more beam electrons are available to give up kinetic energy while passing through a decelerating field. Since more time is spent by a beam electron in a decelerating field than in an accelerating field, it gives up more energy to the r-f field than it receives. To ensure the proper phase relationship between the field at the gap and the electron beam, the electron velocity is chosen so that

the total phase difference at the collector end of the tube is approximately one half cycle. Therefore, over most of the length of the tube, the beam electron bunches encounter relatively strong decelerating fields as they cross the gaps. These fields slow down the beam electrons and cause energy to be delivered to the backward wave. If the beam current is sufficiently great self-sustaining oscillations are developed. The amplitude of the backward wave builds up and becomes larger as it progresses from the collector to the gun end of the tube, and passes more and more bunches of beam electrons from which it receives energy. Simultaneously, the beam electron bunching becomes greater as the electrons progress toward the collector. Actually, the backward wave oscillator is a special type of traveling wave tube which characteristically contains a built-in feedback mechanism. In this mechanism, the power generated by a travelingwave type of interaction is used to supply the signal required at the gun end of the tube to produce bunching of the electron stream.

### Failure Analysis.

General. The carcinotron is manufactured as an integral unit and cannot be repaired or altered by the electronic technician. Usually the filament may be observed visually to see if it is illuminated, and the high voltage and beam current may be measured. WARNING-be certain to employ all safety precautions since highly dangerous voltages are employed. Always disconnect the power and discharge the circuit with a shorting stick before attaching the voltmeter or ammeter test prods. If normal voltages and currents are obtained but the unit does not oscillate, a higher than normal voltage and beam current may be employed to determine if the tube will oscillate at all. Usually, if normal voltage and current will not produce an output, or produce a much lower than normal output, the tube may be defective. If the tube operates but not on the desired frequency it is possible to increase the frequency by applying higher voltage, or to lower it by reducing the voltage. Such a condition indicates a change in tube characteristics and may be a preliminary indication of incipient failure. Other other possibility of trouble could exist; this would be a poor match to the load or a shorting of the load. This possibility can be checked by using a dummy load of the proper value and observing if the output and voltages return to normal.

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# PART 6-4 BLOCKING AND SHOCK EXCITED

# FREE-RUNNING PRF GENERATOR (ELECTRON TUBE)

### Application.

The free-running prf generator is a basic blocking oscillator. It produces short-time-duration, largeamplitude pukes for use as timing, synchronizing, or trigger pulses in radar modulators and display indicators.

#### Characteristics.

Output pulse is a single cycle of oscillation caused by tube conduction at the beginning of each **pulse**repetition period.

Pulse-repetition time is determined primarily by the R-C time constant of the grid circuit. The pulse repetition frequency is generally fixed within the range of 200 to 2000 Hz, although the circuit can be arranged to change the R-C time constant and provide for operation at other fixed pulse-repetition frequencies.

Frequency stability is  $\pm 5$  percent.

Pulse width and rise time of the output pulse are determined primarily by the transformer characteristics.

Output-pulse polarity is determined by the phasing of the transformer output-tertiary winding. With minor circuit changes, output can also be taken from the cathode circuit.

#### Circuit Analysis.

**General.** The free-running blocking oscillator (prf generator) is a special-type oscillator in that the oscillator completes one cycle of operation to produce a pulse and then becomes inactive (blocked) for a considerable period of time, whereupon the cycle of operation to produce a pulse is repeated and the oscillator again becomes inactive. This mode of operation continues, and thus produces a series of output pulses which are of short-time duration, separated by relatively long time intervals.

**Circuit Operation.** The following circuit schematic illustrates a triode electron tube in a basic freerunning blocking oscillator circuit. Transformer T1 provides the necessary coupling between the plate and grid of electron tube VI; terminals 1 and 2 of transformer T1 connect to the plate (primary) winding, terminals 3 and 4 connect to the grid (secondary) winding, and terminals 5 and 6 connect to the output (tertiary) winding. Capacitor Cl and resistor RI form an R-C circuit to determine the discharge time constant in the grid circuit circuit. The output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer T1.



Free-Running PRF Generator

On the circuit schematic, note the placement of small dots near winding terminals 1, 4, and 6 of transformer **T1**. These dots are used to indicate similar winding polarities. For example, if current flows through the plate windings and terminal 1 is negative, the voltage induced in each of the other windings is such that the dot end is also negative in each winding at the same time; therefore, at this same instant of time, terminals 3 and 5 are positive.

For the discussion of circuit operation which follows, refer to the following illustration of the blocking oscillator grid-signal, plate-signal, and output-voltage waveforms.


Theoretical Grid-, Plate-, and Output-Voltage Waveforms

When plate voltage is first applied to the circuit, the grid of VI is at zero bias and plate current starts to flow through the plate winding (terminals 1 and 2) of transformer T1. A magnetic field is set up about the plate winding and a voltage is induced (through transformer action) in the grid winding (terminals 3 and 4) of transformer T1. Because of the phasing of the plate and grid windings, the voltage produced across the grid winding is impressed on the grid of the tube through coupling capacitor Cl with such polarity as to drive the grid to a positive direction. This results in an increase in the tube plate current, and the action continues with the grid being driven further in the positive direction. When the grid is driven sufficiently positive, the tube begins to draw grid current and capacitor Cl begins to charge. Grid capacitor Cl is charged through the relatively low internal cathode-to-grid resistance of the tube, causing the plate of capacitor C 1, which is attached to the grid of V1, to accumulate a surplus of electrons. At this time, however, the plate current has reached its saturation value and the current through the plate winding of transformer T1 can no longer increase (change); as a result, the voltage induced in the grid winding of the transformer can no longer increase (point a on grid-voltage waveform). As a further result, since no induced voltage appears in the grid winding, capacitor C 1 starts to discharge through resistor R1 causing the grid potential of V1 to become slightly less positive. This causes the plate current in the plate winding to decrease slightly, accompanied by a decrease in the magnetic field about the plate winding. As the magnetic field begins to collapse, a voltage is induced in the grid winding of a polarity opposite that originally produced; thus, the grid is driven in a negative direction.

As the grid of V1 is driven negative, the plate current continues to decrease and the magnetic field about the plate winding collapses completely. This causes the grid to be driven still further in a negative direction until cutoff is reached (point b on waveform) at which time plate current no longer flows through transformer T1.

The highly negative charge existing on capacitor Cl places the grid of V1 below cutoff (point c on waveform); then the capacitor slowly discharges through resistor R1 and the grid winding of transformer T1. Since the resistance of the grid winding is low compared to that of the resistor, RI, the resistor is the determining factor in the discharge time of capacitor Cl. Furthermore, since the resistance of R1 is large compared to the internal cathode grid resistance of the tube when the grid of V1 is positive, resistor R1 does not affect the charging of capacitor c1.

After an elapsed period of time, as governed by the time constant of RI and Cl, capacitor Cl discharges through resistor R1 to a point near cutoff (point d on waveform), where the grid voltage allows the tube to conduct. As plate current once again starts to flow through the plate winding of transformer T1, the entire cycle of operation is repeated.

The changing magnetic field produced about the plate winding of transformer T1 also induces a changing voltage in the tertiary or output winding (terminals 5 and 6). Thus, an output-voltage waveform is produced across the tertiary winding which is similar to the plate-voltage waveform of the blocking oscillator. The pulse output can be of either polarity (with respect to ground) depending upon which terminal of the tertiary winding is grounded. As shown in the

circuit schematic, terminal 6 of T1 is grounded; therefore, the initial output pulse is positive with respect to ground. If desired, limiting or clipping techniques can be applied to the output signal to reduce or eliminate the overshoot (amplitude extreme) in the output waveform. In some instances the desired signal may actually be the overshoot and is used to provide a trigger pulse which is delayed in time by the width of the initial pulse.

The approximate time interval required for the capacitor voltage,  $E_e$ , to discharge from maximum to the cutoff value,  $E_{eo}$  (point c to point d on the grid-voltage waveform), may be determined by use of the following formula:

$$t \approx 2.30 \text{ RC } l_{\text{og}} \frac{E_{c}}{E_{\text{co}}}$$

Where:

t

	cutoff (seconds)
E <sub>c</sub>	= maximum voltage change
	across capacitor

= time interval to discharge to

E<sub>co</sub> = negative cutoff value for tube R = resistance of grid resistor (megohms)

c = capacitance of grid-coupling capacitor (µf)

Since the pulse width of the blocking oscillator is usually small compared with the capacitor discharge time, the pulse width may be neglected when approximating the natural operating frequency of the oscillator. The natural operating frequency (Hertz),  $f_o$ , can be expressed as the reciprocal of capacitor discharge time; thus, the blocking-oscillator frequency may be approximated using the following formula:

$$f_o \cong \frac{1}{t}$$

Where: t <sup>=</sup> capacitor discharge time (seconds)

The free-running blocking oscillator, with minor circuit changes, may be synchronized to an external trigger signal by chosing values of R1 and Cl so that the natural oscillating frequency of the blocking oscillator is slightly lower than the desired frequency. The synchronizing trigger signal, then, must be slightly above the natural oscillating frequency of the blocking oscillator. Under these conditions, when the tube is held below cutoff, the application of a positive synchronizing pulse will drive the tube into conduction somewhat earlier than the R-C time constant would normally permit. Thus, the oscillator **will** synchronize its frequency of operation with that of the trigger source and the repetition period of the blocking oscillator will be that of the trigger source.

In a practical blocking-oscillator circuit, resistance RI is usually made up of two resistors: a fixed resistance and a variable resistance connected in series. The variable resistance is then adjusted to provide operation at the desired pulse-repetition frequency. The operating frequency of the blocking oscillator can be changed by switching values of R, C, or both R and C, to alter the time constant. For example, a blocking oscillator designed to operate at 600 pps can be changed to a lower frequency, such as 300 pps, by switching a larger value of R, C, or both, into the circuit to lower the pulse-repetition frequency. Another method of shifting the operating frequency of the blocking oscillator, over a limited range, is to change the quiesent grid voltage of the tube. This method is unaffected by lead resistance, stray capacitance, etc, and is well adapted to remote-control operation.

Important factors affecting the frequency stability of the blocking oscillator are: the stability of grid resistor R1 and of capacitor C 1, the variation or changes in applied filament and plate voltages, and the changes occurring in the electron tube. The circuit is particularly sensitive to changes in filament voltage; a 10 percent decrease in filament voltage may change the oscillator frequency as much as 2 percent, while a 10 percent increase in filament voltage may change the frequency about 1 percent. A change in plate voltage of 10 percent will change the frequency about 1 percent.

# Failure Analysis.

**No Output.** In a nonoscillating condition, negative grid voltage will not be developed; the measured plate voltage at the plate of V1 will be below normal because of the steady value of plate current flowing through the plate winding of transformer T1 (assuming the plate winding is not open). Capacitor Cl and resistor R1 directly affect the pulse timing; a shorted capacitor will cause oscillations to cease and prevent development of oscillator grid voltage, and an open

resistor will prevent capacitor discharge. Sustained periodic oscillations of the blocking oscillator depend upon feedback obtained from transformer Tl as well as the action of capacitor C 1 and resistor R1. Therefore, any defect in the transformer, such as an open plate or grid winding or a number of shorted turns in either of these windings, will prevent the circuit from operating. A shorted output winding or shorted load impedance may also cause the circuit to stop oscillating, since the tertiary winding is coupled to the plate and grid windings of the transformer. In this case, the impedance reflected to the plate and grid windings may cause excessive losses which will prevent sustained oscillations. Note that if the tertiary winding should open, the circuit will continue to operate: however, no output will be obtained from the tertiary winding.

**Incorrect Frequency.** The value of oscillator R-C components should be within design tolerance in order to produce the desired operating frequency; where an adjustment is provided, a small change in operating frequency can be compensated for by adjustment of the variable resistance in the grid circuit. It is resonable to assume that any change in the R-C time constant of the blocking-oscillator grid circuit (change in value of resistance or capacitance, leaky capacitor, etc) will be accompanied by a change in operating frequency. Also, changes in applied filament and plate potentials will affect the operating frequency.

Indiscriminate substitution of tubes in the freerunning blocking-oscillator circuit can cause a frequency change because of differences in individual tube characteristics.

incorrect Pulse Width Or Unstable Output.Capacitor Cl affects the pulse width as well as the R-C discharge time; however, transformer T1 is of greatest influence in determining pulse width and the rise time of the output pulse. The rate of rise of the leading edge of the output pulse depends upon the transformer turns ratio between plate and grid windings and also upon the rate at which current may rise in the windings as determined by their inductance. (A transformer with high step-up ratio and low inductance will produce relatively short-duration pulses.) The pulse width normally obtained is approximately equal to the time of one-half cycle which would be produced at the natural oscillating frequency if the relative large grid-blocking capacitor Cl were not used in the circuit. Thus, a defect in the transformer,

T1, would be likely to cause a change in pulse width accompanied by unstable or erratic output.

The instantaneous blocking-oscillator grid-tocathode voltage is the difference between the instantaneous charge voltage on the capacitor and the instantaneous negative voltage produced across the grid winding of transformer T1. A rise in capacitor voltage causes the grid voltage to become less positive faster than if the action depended upon transformer voltage alone; thus, the initial pulse is effectively shortened. If either capacitor Cl or resistor R1 should change value, the effect would be more readily noticed as a change of frequency rather than a change of pulse width.

# FREE-RUNNING PRF GENERATOR (SEMICONDUCTOR)

### Application.

The free-running (prf generator) blocking oscillator is a basic blocking oscillator. It produces shorttime-duration, Iarge-amplitide pulses for use as timing, synchronizing, or trigger pulses.

### Characteristics.

Output pulse is a single cycle of oscillation caused by transistor (collector element) conduction at the beginning of each pulse-repetition period.

Pulse-repetition time is determined primarily by the R-C time constant in the base-emitter circuit. The pulse-repetition frequency is generally fixed within the range of 200 to 2000 pulses per second.

Pulse width and rise time of the output pulse are determined primarily by the transformer characteristics.

Output-pulse polarity is determined by the phasing of the transformer output-tertiary winding.

## Circuit Analysis.

**General.** The free-running blocking oscillator (prf generator) is a special-type oscillator in that the transistor conducts for a short period to produce a pulse and then becomes cut off (blocked) for a much longer period of time; then the cycle of operation to produce an output pulse is repeated and the oscillator again becomes inactive. This mode of operation continues and thus produces a series of output pulses which are of short-time duration, separated by relatively long time intervals.

**Circuit Operation.** The following circuit schematic illustrates a PNP transistor in a basic freerunning blocking oscillator circuit. (Note the similarity between the blocking oscillator circuit given here and the L-C tickler-Coil oscillator circuit given earlier in this section.



Free-Running PRF Generator Using PNP Transistor

Transformer T1 provides the necessary regenerative feedback coupling from the collector to the base of transistor Q1; terminals 1 and 2 of transformer T] connect to the collector (primary) winding, terminals 3 and 4 connect to the base (secondary) winding, and terminals 5 and 6 connect to the output (tertiary) winding. Capacitor Cl and resistor R1 form the R-C circuit which determines the time constant in the base-emitter circuit.

The output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer T1. Damping resistor R2 is connected across the tertiary winding to reduce the amplitude of the back voltage resulting from the collapse of the magnetic field about the transformer after the occurrence of the initial output pulse.

On the circuit schematic, note the placement of small dots near winding terminals 1,4, and 5 of transformer T1. These dots are used to indicate similar winding polarities. For example, if current flows through the collector winding and terminal 1 is positive, the voltage induced in each of the other windings is such that the dot end is also positive in each winding at the same time; therefore at this same instant of time, terminals 3 and 6 are negative.

Bias and stabilization techniques employed for a transistor oscillator are essentially the same as those employed for a transistor amplifier. The commonemitter circuit configuration illustrated utilizes a single-battery power source; this source directly produces the required reverse bias voltage in the collector-base circuit. Forward bias for the PNP transistor requires the base to be negative with respect to the emitter. Since the collector is at a negative potential and the emitter is at a positive potential, the two PN junctions within the transistor act as a voltage divider. The junction between collector and base represents a relatively high resistance and develops a large portion of the voltage drop. The junction between emitter and base represents a low resistance and develops a lower voltage drop. The base of the transistor is structurally between the collector and the emitter and assumes a potential which is between the two voltage extremes; therefore, the base can be considered to be less positive than the emitter, or negative with respect to the emitter. Thus, the correct polarity is established to produce a forward bias between the emitter and the base.

The blocking oscillator can be compared to an amplifier with feedback of the proper phase and amplitude to provide regeneration. In the accompanying circuit schematic a common-emitter configuration circuit schematic a common-emitter configuration is shown using a PNP transistor; the regenerative feedback signal must undergo a polarity reversal in passing from the collector to the base. If an NPN transistor is used, the polarity of the supply voltage must be opposite to that given on the schematic in order to maintain forward bias in the base-emitter circuit and reverse bias in the collector-base circuit; however, for either type of transistor the transformer must provide a **polarity reversal** when feedback is from collector to base.

For the discussion of circuit operation which follows, refer to the accompanying illustration of the blocking oscillator waveforms.



**Theoretical Waveforms for Blocking Oscillator** 

When dc power is first applied to the circuit, a small amount of collector current, i, will start to flow through the collector winding (terminals 1 and 2) of transformer TI. The current flow in the collector winding induces a voltage in the base winding (terminals 3 and 4) which is negative with respect to ground. The induced voltage causes capacitor Cl to charge through the relatively low forward resistance of the base-emitter junction, and the induced voltage appears across the forward resistance to increase the forward bias. The increase in forward bias, in turn, increases the collector current, and regeneration continues rapidly until the transistor becomes saturated. During the essentially flat-top portion of the collector voltage waveform, the collector current, i, increases at a slower rate, as determined by the amount of magnetizing current necessary to maintain the voltage drop across the collector winding of transformer T1. Also during this period of time, the base curent, i<sub>h</sub>, gradually falls off from its peak value as a result of the inability of the transistor to maintain the same

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rate of increase in magnetizing current as the transistor approaches saturation; further, at this same time a charge is accumulating on capacitor Cl which subtracts from the voltage supplied by the base winding of transformer T1. At saturation, the collector current, i, can no longer continue to increase, and thus becomes a constant value; therefore, there is no longer a voltage induced in the base winding, terminals 3 and 4. As a result, the magnetic field begins to collapse and induces a voltage across the winding which is of opposite polarity to the original voltage. At the same time, capacitor Cl starts to discharge through resistor R1 and the base winding (terminals 3 and 4). The discharge current of capacitor Cl produces a voltage drop across resistor RI which is of positive polarity at the base of the transistor, thereby driving the base in a positive direction to reduce the forward bias of the base-emitter junction. The reduction in forward bias causes the collector current, i, to decay rapidly, which further accelerates the process; thus reverse bias is rapidly achieved at the baseemitter junction. At this time the base and collector currents drop to zero.

Because of the reverse bias, the transistor remains held at cutoff until capacitor Cl discharges through resistor RI (and transformer Tl) to a point where the transistor returns to a forward-biased condition. When the forward-biased condition is reached, conduction begins and another cycle of operation is initiated.

The output pulse width depends principally on the inductance of the transformer, T1. The smaller the inductance, the more rapidly the collector current must increase to maintain magnetizing current, and the faster the collector current will reach saturation. Normally, capacitor Cl has relatively little effect on the pulse width; however, if it is made small enough that it approaches a value where the capacitor charge can change appreciably during the pulse time, there will be a noticeable decrease in pulse duration (width). As the capacitor is made still smaller, the effect will be more pronounced and the pulse duration will be further reduced.

The repetition rate of the free-running blocking oscillator is determined by the time constant of resistor R1 and capacitor Cl. Although the resistance of the base winding (terminals 3 and 4) of the pulse transformer also has an effect upon the discharge time constant, the resistance of the winding is low compared to that of resistor RI.

The output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer T1. Damping resistor R2 is connected across the tertiary winding of the transformer to reduce the amplitude of the back voltage (or overshoot) which results from the collapse of the magnetic field about the transformer at the termination of the desired output pulse. If it were not for the damping resistor, the amplitude of the backvoltage pulse could exceed the breakdown voltage of the transistor and cause damage to the transistor. Several modifications can be made to the basic circuit to further reduce the amplitude or to eliminate the undesirable back voltage. One such modification is to connect a clamping diode across the collector winding (terminals 1 and 2) of the transformer as shown on the circuit schematic by the dotted lines connecting diode CR1. Similarly, a clamping diode can be connected across the output winding (terminals 5 and 6) as shown on the circuit schematic by the dotted lines connecting diode CR2, to accomplish the same purpose. In either case, the diode (CR] or CR2) is connected in the circuit to conduct whenever the backvoltage pulse occurs and to effectively place a short circuit across the associated transformer winding for the duration of the inducted back-voltage pulse; thus it prevents the application of an excessive voltage between the collector and emitter.

The accompanying circuit schematic illustrates a variation of the basic free-running prf generator. In this circuit resistor RI is returned to the negative terminal of the supply voltage,  $V_{cc}$ . Resistor R1 not only limits the base current and establishes the initial condition of forward-bias, but also operates in conjunction with capacitor C1 to determine the operating frequency of the blocking oscillator.

The circuit operation is essentially the same as that previously described.



Variation of Basic Free-Running PRF Generator

## Failure Analysis.

**No Output.** Voltage measurements should be made with an electronic voltmeter to determine whether the input voltage is present and whether the correct bias voltages are applied to the collector and base of the transistor. It is possible that the base-emitter junction may change resistance and thereby change the forward bias on the base; such a condition may cause thermal runaway with subsequent damage to the transistor.

Any defect in transformer T1, such as an open collector or base winding or shorted turns in any of the windings, will prevent the circuit from operating properly, since oscillations depend upon regenerative feedback from the transformer. A shorted load impedance, reflected to the collector and base windings, may cause excessive losses which will prevent sustained oscillations. Note that if the output winding

should **open**, the circuit will continue to operate; however, no output will be obtained from the winding. Furthermore, if damping resistor R2 should open, the induced back-voltage could exceed the voltage breakdown of the collector-emitter junctions and result in damage to the transistor.

A shorted or open capacitor Cl will prevent oscillations, since the regenerative action of the circuit depends upon the charge and discharge of Cl. Also, if resistor R1 should open, the base-emitter current path will be broken and thereby prevent transistor operation.

Where the basic oscillator circuit illustrated has been modified to include a clamping diode (CR1 or CR2) across either the collector winding or the output winding, a defective diode with a low front-toback ratio may cause circuit losses and prevent oscillation. Furthermore, if damping resistor R2 should decrease in value or if the load impedance should drop to an extremely low value, oscillations may not occur because of induced circuit losses.

**Reduced Output.** The input supply voltage should be measured with an electronic voltmeter to determine whether the input voltage is the correct value. Voltages at the collector and the base of the transistor should also be measured to determine whether they are within tolerances. Where the basic oscillator circuit illustrated has been modified to include a clamping diode across either the collector winding or the output winding, or across each winding, a defective diode with low front-to-back ratio can cause cir**cuit** losses which can reduce the output. Moreover, if either clamping resistor R2 or the load impedance should decrease in value, the output amplitude will decrease. Note that if the circuit losses are excessive, the circuit may not oscillate at all.

**Incorrect Frequency. The** pulse-repetition frequency of the free-running blocking oscillator is determined by the R-C time constant of resistor RI and capacitor Cl; any change in the values of these components will cause a change in operating frequency. Also, any change in the supply voltage will probably affect the pulse-repetition frequency and may affect the amplitude of the output pulse.

# PARALLEL-TRIGGERED BLOCKING OSCILLATOR (ELECTRON TUBE)

## Application.

The parallel-triggered blocking oscillator is used to produce short-time duration, large-amplitude pulses for use as synchronizing or trigger pulses in radar modulators and display indicators.

## Characteristics.

Output pulse is a single cycle of oscillation caused by **trigger-amplifier** tube conduction which is, in turn, synchronized by a trigger pulse at the beginning of each pulse-repetition period. Some delay is introduced between the time of trigger application to the trigger amplifier and the development of the leading edge of the output pulse.

Pulse repetition time is determined by an external positive-trigger source in conjunction with the R-C time constant of the grid circuit. The pulse-repetition frequency is generally fixed within the range of 200 to 2000 pulses per second.

Trigger amplifier provides isolation and prevents blocking oscillator from reacting on trigger source; also, amplification of trigger pulse sharpens pulse somewhat.

Pulse width and rise time of the output pulse are determined primarily by the transformer characteristics.

Output-pulse polarity is determined by the phasing of the transformer output-tertiary winding. With minor circuit changes, the output can also be taken from the cathode circuit (positive pulse) or from the plate circuit (negative pulse).

#### Circuit Analysis.

**General. The** parallel-triggered blocking oscillator is similar to the free-running prf generator except that its pulse-repetition frequency is determined by a positive synchronizing trigger pulse which is applied to a trigger amplifier. The plates of the trigger-amplifier tube and the blocking-oscillator tube are in parallel

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and share a common plate winding of the blockingoscillator transformer. When the **trigger** amplifier receives a pulse from an external source, it amplifies the pulse and causes current to flow in the plate winding of the transformer; thus, a cycle of oscillation is initiated. Upon completion of the pulse cycle, the circuit becomes inactive until the amplifier receives another trigger pulse. Normal operation of the parallel-triggered blocking oscillator results in the generation of an output pulse each time a trigger pulse is applied to the trigger amplifier.

**Circuit Operation.** The following circuit schematic illustrates two triode electron tubes in a parallel-triggered blocking-oscillator circuit; one electron tube is the blocking oscillator and the other is the trigger amplifier. Although the schematic illustrates two separate triodes, VI and V2, a twin triode is frequently used in this circuit.



Parallel-Triggered Blocking Oscillator

Transformer TI provides the necessary coupling (inductive feedback) between plate and grid of electron tube V2; terminals 1 and 2 connect to the plate (primary) winding, which is common to bothVl and V2, terminals 3 and 4 connect to the grid (secondary) winding, and terminals 5 and 6 connect to the output (tertiary) winding. Capacitor Cl couples the input trigger pulse to the grid of V1; resistor RI is the grid-return resistor for V1. Resistors R2 and R3 form a voltage divider to provide cathode bias for the trigger-amplifier tube, V1; similarly, resistors R4 and R5 provide cathode bias for the blocking-oscillator tube, V2. Capacitors C2 and C3 are the cathode bypass capacitors for V1 and V2, respectively. Capacitor C4 and resistor R6 form an R-C circuit to determine the discharge time constant in the grid circuit of V2. Resistor R7 and capacitor C5 form a plate decoupling network.

The output pulse from the blocking oscillator is taken from the tertiary winding (terminals 5 and 6) of transformer TI.

For the following discussion of circuit operation, refer to the accompanying illustration which shows the input trigger and blocking-oscillator plate-signal, grid-signal, and output-voltage waveforms. Bias voltage for the trigger amplifier, V1, is developed by cathode resistor R2 as a result of the dc current through the series resistance of R2 and R3, connected as a voltage divider between the supply voltage and ground; also, bias is developed for the blocking oscillator, V2, by cathode resistor R4, which is in series with resistor R5 to form a similar voltage divider. The amount of bias developed by resistor R2 is sufficient to hold the grid of V1 near cutoff, whereas the bias developed by resistor R4 places the grid of V2 below cutoff.



Theoretical Trigger-, Plate-, Grid-, and Output-Voltage Waveforms

To start a single cycle of operation, a positive trigger pulse is applied to the input of trigger amplifier V1 across coupling capacitor C1 and grid-return resistor RI. The trigger pulse developed across resistor R1 is applied to the grid of VI and amplified by the trigger amplifier. As a result of the positive-going pulse on the grid of VI, the tube conducts and plate current flows through the plate winding (terminals 1 and 2) of the pulse transformer, TI. The voltage at the plates of V1 and V2 starts to drop as the current of the trigger amplifier increases in the plate winding; the increasing current through the plate winding sets up a magnetic field about the winding, and a voltage is induced (through transformer action) in the grid winding (terminals 3 and 4) of transformer TI. Since the trigger pulse is of short duration, the trigger amplifier returns to its initial condition at the end of the trigger pulse, and VI ceases to conduct because of the cathode bias developed by resistor R2. The

blocking-oscillator action which follows is similar to that which occurs during one cycle of operation for the free-running (**prf** generator) blocking oscillator.

When trigger-amplifier plate current flows through the plate winding, a grid-signal voltage is produced across the grid winding and is impressed on the grid of V2 through coupling capacitor C4 to drive the grid of V2 in a positive direction. (See grid-voltage waveform.) This causes the blocking-oscillator tube to start to conduct when the positive grid voltage exceeds the value of cathode bias; the regenerative action (feedback) which occurs to complete the cycle of operation is essentially the same as the action previously described for the free-running (prf generator) blocking oscillator. Near the end of the cycle of operation and after the trigger-amplifier tube returns to cutoff, the grid of the blocking oscillator is driven below cutoff as the result of the highly negative charge existing on capacitor C4. (See grid-voltage waveform.) Capacitor C4 slowly discharges through resistor R6 and the grid winding of T1. The time constant of R6 and C4 is chosen so that the grid is held below cutoff for a considerable period of time; thus, the grid gradually approaches the initial value of bias, at which time the circuit is ready to be triggered to initiate another cycle of operation. (The initial value of bias developed across R4 is sufficient to keep the blocking-oscillator tube at or below cutoff.) Under the conditions of operation described above, the blocking oscillator produces an output pulse each time a trigger pulse is applied to the input of the trigger amplifier, VI. The output pulse is delayed slightly, but has the same repetition frequency as the synchronizing trigger pulse.

With minor modification to change the time constant of R6C4, the parallel-triggered blocking oscillator circuit may be used as a pulse-frequency divider to produce output pulses at a submultiple of the trigger-pulse frequency.

The output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer TI in the same manner as that previously described for the freerunning (prf generator) blocking-oscillator circuit.

The parallel-triggered blocking oscillator is relatively insensitive to changes in filament and plate supply voltages. A change in plate voltage of 10 percent may reflect a change as great as 7 percent in pulse amplitude; however, there is little change in pulse width or rise time.

# Failure Analysis.

No Output. It is important to establish that the cathode bias voltage developed by each voltage divider (R2, R3, and R4, R5) is correct for the triggeramplifier and blocking-oscillator tubes, V1 and V2. Since the trigger-amplifier and blocking-oscillator tubes are normally biased at or below cutoff, it is also important to establish that a trigger pulse of correct polarity and amplitude is being supplied to the circuit. When the circuit is in a nonoscillating condition, assuming that the bias voltage is correct for both tubes, the voltage measured at the plates of V1 and V2 will approach the value of the supply voltage, provided that the plate winding of T1 and the decoupling filter (R7 and C5) are not defective. Any defect in the plate or grid windings of transformer T1 is likely to prevent the proper regenerative feedback from occurring; as a result, the circuit will not provide the proper output pulse or may not oscillate at all.

If the tertiary winding of transformer T1 should open, the circuit may still operate but no output will be obtained from the tertiary winding.

Unstable output. Whenever the output-puke repetition rate of the blocking oscillator becomes unstable or erratic, the trigger pulse should first be checked to determine whether the fault lies within the trigger-generator circuit. Since the stability of the blocking oscillator is dependent upon the repetitionfrequency and pulse-amplitude stability of the trigger source, it is entirely possible that an unstable trigger applied to the trigger amplifier will cause the blocking oscillator to produce output pulses which are synchronized to the faulty trigger. The time constant of R6 and C4 must allow the grid of V2 to return the initial value of bias before the blocking oscillator is triggered ;.otherwise, the blocking oscillator may not respond reliably to the amplified trigger pulse. Random pulsing of the blocking oscillator can also result if the cathode bias (derived from resistors R4 and R5) is reduced and approaches zero bias. In this case, although the trigger pulse will frequently initiate an operating cycle, the oscillator may attempt to become free-running because of the lack of correct bias. Leakage in capacitor C4 will cause a change in the R-C time constant of the blocking oscillator, and will result in an unstable output which is usually accompanied by a decrease in pulse amplitude.

Low Output. Reduced plate-supply voltage will affect the amplitude (and perhaps the pulse width and

rise time) of the output pulse. Also, if shorted turns should develop in the tertiary winding of T1 or if a decrease in load impedance should occur, the pulseoutput amplitude will be reduced not only because of the change in load impedance but also because of the impedance reflected into the plate and grid windings of transformer T1. If the load impedance should fall considerably below the normal value for the circuit, an increase in time delay will occur between the trigger pulse and the start of the output pulse; also, the rise time of the output pulse will increase and will be accompanied by a decrease in pulse amplitude.

# SERIES-TRIGGERED BLOCKING OSCILLATOR (ELECTRON TUBE)

## Application.

The series-triggered blocking oscillator is used to produce short-time-duration, large-amplitude pulses for use as synchronizing or trigger pulses in radar modulators and display indicators.

#### Characteristics.

Output pulse is a single cycle of oscillation caused by tube conduction which is initiated by synchronizing trigger pulse at the beginning of each **pulse**repetition period.

Pulse-repetition time is determined by an external positive-trigger source in conjunction with the R-C time constant of the grid circuit. The pulse-repetition frequency is generally fixed within the range of 200 to 2000 pulses per second, although the circuit can be arranged to change the R-C time constant and provide for operation at a submultiple of the trigger-pulse frequency; in this case, the triggered blocking oscillator operates as a pulse frequency divider.

Requires a low-impedance **trigger** source; there is considerable reaction on the trigger source even if a cathode follower is used for triggering the circuit.

Pulse width and rise time of the output pulse are determined primarily by the transformer characteristics.

Output-pulse polarity is determined by the phasing of the transformer output-tertiary winding. With minor circuit changes, the output can also be taken from the cathode circuit.

## Circuit Analysis.

**General.** The series-triggered blocking oscillator is similar to the free-running prf generator except that

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its pulse-repetition frequency is determined by a positive synchronizing trigger pulse. When the oscillator is triggered by a pulse from an external source, it completes one cycle of operation to produce an output pulse and then becomes inactive; the cycle of operation is repeated upon application of another trigger pulse. Normal operation of the series-triggered blocking oscillator results in the generation of an output puke each time a trigger pulse is applied to the circuit.

**Circuit Operation.** The following circuit schematic illustrates a triode electron tube in a seriestriggered blocking-oscillator circuit. Transformer T1 provides the necessary coupling (inductive feedback) between the plate and grid of electron tube V1; terminals 1 and 2 connect to the plate (primary) winding, terminals 3 and 4 connect to the grid (secondary) winding, and terminals 5 and 6 connect to the output

Series-Triggered Blocking Oscillator

(tertiary) winding. Capacitor Cl and resistor Rl, in conjunction with R4, form an R-C circuit to determine the discharge time constant in the grid circuit. Resistors R2 and R3 forma voltage divider to provide cathode bias for the tube; the voltage developed across R2 is sufficient to bias the tube at or below cutoff. Capacitor C2 is a cathode bypass capacitor. The synchronizing trigger pulse is applied across resistor R4, which is effectively in series with the grid signal. The value of resistor R4 is generally low; however as indicated previously, this resistance is a part of the total resistance which determines the R-C time constant of the circuit. Resistor R5 and capacitor C3 form a plate decoupling network.

The output pulse from the blocking oscillator is taken from the tertiary winding (terminals 5 and 6 of transformer T1.

For the brief discussion of circuit operation which follows, refer to the accompanying illustration which shows the blocking-oscillator-trigger, grid-signal, and output voltage waveforms.



Theoretical Trigger, Grid-Vcdtage, and Output-Voltage Waveforms

When voltage is first applied to the circuit, bias voltage for the tube is developed by cathode resistor R2 as a result of the dc current through the series resistance of R2 and R3 connected between the supply voltage and ground. The amount of bias developed is sufficient to hold the grid at or slightly below cutoff; thus, plate current does not flow at this time.

To start a single cycle of operation, a positive trigger pulse is applied across resistor R4. This pulse is applied through the grid winding of transformer T1 and capacitor Cl to the grid of V1, and raises the grid

voltage above cutoff. (The positive-going trigger pulse must be of sufficient amplitude to drive the grid out of the cutoff region to initiate the cycle.) At this time the tube starts to conduct, and the regenerative action which occurs during the cycle of operation is essentially the same as the action previously described for the free-running (prf generator) blocking oscillator. Near the end of the cycle, when the grid is driven below cutoff and plate current no longer flows through the plate winding of T1, the highly negative charge existing on capacitor Cl slowly discharges through resistors RI and R4 and the grid winding of transformer T]. Since the resistance of the grid winding is low in comparison with the combined resistance of R1 and R4, it has little effect on the discharge time of capacitor Cl. Furthermore, the resistance of R4 is low compared to that of R1; therefore, RI has the predominant effect on the discharge time of capacitor Cl.

After an elapsed period of time, as governed by the time constant of R1, R4, and Cl, capacitor Cl discharges and allows the grid potential to reach a point near cutoff. When a positive trigger pulse is again applied across resistor R4, another cycle of operation is initiated.

If it were not for the periodic application of the positive trigger pulse to resistor R4, the blocking oscillator would remain cut off because of the value of cathode bias developed across cathode resistor R2. Under these conditions, each time a trigger pulse is applied to the circuit, a complete cycle of the blocking oscillator produces an output pulse which is in synchronism with the trigger pulse and has the same repetition frequency. For synchronization to occur the values of R and C must be chosen so that the natural oscillating frequency of the blocking oscillator, in the absence of cathode bias, is **slightly** lower than the repetition frequency of the synchronizing trigger pulse.

The operating frequency of the triggered blocking oscillator can be conveniently changed to a submultiple of the trigger frequency by switching R-C values to alter the time constant. For example, an additional resistance could be switched into the circuit in series with resistor RI to increase the **R-C** time constant. In this case, if the time constant were at least doubled, the oscillator would respond to every other **trigger** pulse and, therefore, the blockingoscillator repetition frequency would be one-half that of the trigger source. The output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer T1 in the same manner as previously described for the free-running (prf generator) blocking-oscillator circuit.

In a practical series-triggered blocking-oscillator circuit, resistor R4 may actually be the cathode resistor for a cathode-follower circuit. In this case, the trigger is applied to the grid of the cathode-follower electron tube, and resistor R4, across which the trigger pulse is developed, represents a low-impedance trigger source to the blocking-oscillator circuit.

The series-triggered blocking oscillator is relatively insensitive to changes in filament and plate-supply voltages, although a change in plate voltage of 10 percent may produce a change as great as 10 percent in pulse amplitude and maybe accompanied by some change in pulse width. However, this effect is reduced to some extent by the change in the bias voltage developed across resistor R2 whenever the platesupply voltage changes.

#### Failure Analysis.

No Output. Since the oscillator is normally biased to cutoff, it is important that a trigger pulse of the correct polarity and amplitude be supplied to the oscillator circuit. When the circuit is in a nonoscillating condition, assuming that the developed cathode bias is normal, the voltage measured at the plate of V1 will approach the value of the supply voltage, provided that the plate winding of T1 and the decoupling filter (R5 and C3) are not defective. Any defect in the plate or grid windings of transformer T1 is likely to prevent the proper regenerative feedback from occurring; as a result, the circuit will not provide the proper output pulse or may not oscillate at all. If the tertiary winding of transformer Tl should open, the circuit may still operate but no output will be obtained from the tertiary winding.

**Unstabla Output.** Whenever the output-pulse repetition rate of the blocking oscillator becomes unstable or erratic, the trigger pulse whould first be checked to determine whether the fault lies within the trigger-generator circuit. Since the stability of the blocking oscillator is dependent upon the repetition-frequency and pulse-amplitude stability of the trigger source, it is entirely possible that an unstable trigger applied to the oscillator will cause the blocking **oscillator** to produce output pulses which are synchronized to the random triggering. Random pulsing of

the blocking oscillator can also result if the fixed bias (derived from resistors R2 and R3) should be reduced and approach zero bias. In this case, although the trigger pulse will frequently initiate an operating cycle, the oscillator may attempt to become freerunning because of the lack of corect bias. Leakage in capacitor C 1 will cause a change in the R-C time constant of the blocking oscillator, and will result in an unstable output which is usually accompanied by a decrease in pulse amplitude.

**Low Output.** Reduced plate-supply voltage will affect the amplitude (and perhaps pulse width) of the output pulse. Also, if shorted turns should develop in the tertiary winding or if a decrease in load impedance should occur, the output will be reduced not only because of the change in load impedance but also because of the impedance reflected into the plate and grid windings of transformer T1.

# TRIGGERED BLOCKING OSCILLATOR (SEMICONDUCTOR)

#### Application.

The basic triggered blocking oscillator is used to produce synchronized, large-amplitude pulses for use as timing, trigger, or control pulses in radar equipment, television sets, and similar electronic switching devices.

#### Characteristics.

Requires a negative input trigger pulse.

Output pulse is a single cycle of oscillation (positive and negative alternations).

Output-pulse-repetition frequency is determined by the input trigger frequency.

Output-pulse width and rise time are determined primarily by the transformer inductance, capacitance, and resistance characteristics.

Output-pulse polarity is determined by the transformer output (tertiary) winding phasing.

Fixed, Class B (cutoff) bias is employed.

#### Circuit Analysis.

**General.** The basic blocking oscillator produces an output pulse each time an input pulse is applied to activate the circuit. Between trigger pulses, the transistor remains cut off (non-conducting), and no output is produced until an input trigger pulse of sufficient amplitude to produce conduction is again applied. The circuit produces one output pulse and then

returns to the inactive (quiescent) state, awaiting the next trigger.

**Circuit Operation.** The accompanying circuit schematic illustrates a basic triggered blocking oscillator using a PNP transistor connected in the common-



**Basic Blocking Oscillator** 

emitter configuration. Transformer T1 provides the regenerative feedback necessary between the collector and the base of transistor Q1 to obtain oscillation. The primary winding (terminals 1 and 2) is connected in series with collector supply  $V_{\alpha}$  and the collector of transistor Q1. The secondary winding (terminals 3 and 4) supplies the feedback voltage, which is applied to the base of transistor Q1 through capacitor C2. Capacitor C2 is also a dc blocking capacitor used to isolate the base from the dc shunting effect of the secondary winding of transformer T1, preventing it from shorting to ground the fixed cutoff bias applied to transistor Q1 through base resistor R1. The negative input trigger is applied through coupling capacitor Cl to the base of transistor Q1, and the output pulse is taken from the tertiary winding (terminals 5 and 6) of transformer T1.

The collector of transistor Q1 is reverse-biased by the negative collector supply,  $V_{ec}$ ; the positive base bias supply,  $V_{BB}$ , furnishes fixed reverse bias to the base of transistor Q1 through base resistor R1. Thus, in the quiescent state with no input trigger applied, transistor Q1 is completely reverse-biased and cannot conduct. Hence, no output is produced.

When a negative trigger pulse, such as that shown at time  $t_1$  on the accompanying waveform



illustration, is applied through coupling capacitor Cl to the base of transistor QI, it forward-biases

Theoretical Waveforms for Basic Blocking Oscillator

the transistor, causing collector current to flow. The collector current, flowing from the collector supply through the collector (primary) winding of transformer T1 to the transistor, causes a magnetic field to be built up around the collector (primary) winding of the transformer. This increasing magnetic field induces into the base winding of the transformer a voltage of such polarity that the potential on terminals 3 of the winding is negative with respect to ground (terminal 4). This negative potential is applied to the base of transistor Q1 (through capacitor C2), and increases the forward bias on the transistor, causing the collector current to increase further. As the collector current flowing through the collector winding of transformer T1 increases. The magnetic field around the winding increases accordingly, inducing a larger voltage into the base winding of the transformer. The increasing induced voltage is fed back to the base of

transistor Q1, causing the forward bias on the transistor and hence the collector current, to increase still further. Thus, this regenerative feedback from the collector to the base of transistor Q1 causes the collector current to continue to increase until the transistor reaches saturation. When transistor Q1 reaches collector-current saturation (time toon the waveform illustration), the collector current flowing through the collector winding of transformer T1 can no longer increase. Therefore, the magnetic field around the collector winding no longer increases; consequently, no feedback voltage is induced into the secondary (base) winding of the transformer. As a result, the voltage across the base winding of transformer T1 decays at a rate determined by the inductance, capacitance, and resistance values of the transformer, causing the negative voltage on the base of transistor Q1 to decrease accordingly. At the same time, the decreasing voltage across the base winding of transformer T1 also induces into the collector winding a voltage of such polarity that it aids (adds to) the collector-supply voltage, effectively increasing the value of the collector-supply voltage. The effectively increased collector-supply voltage raises the saturation point of the transistor; consequently, the collector current increases slightly above the previous saturation value. When the voltage across the base winding of transformer TI decays to zero (time t, on the waveform illustration), no further forward bias is applied through capacitor C2 to the base of transistor Ql, and the transistor ceases to conduct. Since no further forward bias is supplied, the base bias supply resumes control and applied a positive bias voltage through resistor RI to the base of transistor Ol, reverse-biasing the transistor and holding it below cutoff until the next trigger pulse is applied. Meanwhile, as the transistor decreases in conduction from saturation to cutoff (at time  $t_{a}$ ) the collector curent flowing through the collector winding of transformer T1 decreases to zero, and the magnetic field around the winding collapses. This collapsing field induces into the collector winding a voltage of such polarity that it tends to keep current flowing in the same direction as the original current flow (that is, the induced voltage aids the collector-supply voltage). The result of adding these voltages is that the voltage on the collector of transistor Q1 momentarily becomes much more negative than the negative collector-supply value. This large negative voltage pulse is called overshoot (point A on the collector-voltage waveform). As the **mag** netic field around the collector winding of **trans** former T1 collapses completely, the induced voltage (overshoot) also decreases to zero, and the collector voltage returns to the quiescent value.

Any change of current in the collector winding of transformer T1 also induces a changing voltage into the tertiary, or output, winding of the transformer. The polarity of the output pulse is determined by which terminal of the output winding is grounded. As shown in the circuit schematic, terminal 6 is grounded, and a positive output pulse results (a negative output pulse would be obtained if terminal 5 were grounded instead).

## Failura Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias applied through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition maybe caused by an improper input trigger, a lack of supply voltage, or a defective circuit component. First, use an oscilloscope to observe the input trigger voltage waveform. Compare the observed waveform with one shown in the equipment instruction book to be certain that the proper input trigger is applied. Next, use a vacuum-tube voltmeter to measure the supply voltage and eliminate the possibility of a defective power supply. If the correct input trigger is applied and the normal supply voltage is present, further checks must be made to locate the defective component. Use an in-circuit capacitor checker to check capacitors Cl and C2 for opens and leakage, and an ohmmeter to check resistor R1 and transformer T1 for continuity and proper resistance vrdue. If these checks fail to locate a defective component, transistor Q1 is probably at fault.

Low or Distorted **Output. Low** supply voltage, a defective transistor (Ql), or a defective transformer

(Tl j may cause either low-amplitude or distorted output pulses. Measure the supply voltage with a vacuum-tube voltmeter. If the normal value of voltage is measured, the trouble is in the blocking oscillator and not in the power supply.

# FAST-RECOVERY BLOCKING OSCILLATOR (ELECTRON TUBE)

### Application.

The fast-recovery blocking oscillator produces short-time-duration, large-amplitude pulses for use as timing, synchronizing, or trigger pulses in radar modulators and display indicators.

### Characteristics.

Output is a single pulse caused by tube conduction and initiated by a trigger pulse at the beginning of each pulse repetition period.

Pulse repetition frequency is determined by an external trigger source.

Pulse repetition period is much shorter in the fastrecovery blocking oscillator than in other types of blocking oscillators.

Pulse width and rise time are determined primarily by the transformer characteristics.

Output pulse polarity is determined by the phasing of the transformer output (tertiary) winding.

#### Circuit Analysis.

**General.** The fast-recovery blocking oscillator is **similar** to other types of triggered blocking oscillators in that, when triggered, it supplies one output pulse and then becomes inactive. In the normal triggered blocking oscillator, the grid voltage must be allowed to return to a point near cutoff before the circuit is triggered again. This period of time, called *recovery* time, is normally much longer than the pulse width and limits the pulse repetition frequency. The fast-recovery blocking oscillator uses a number of methods to overcome the difficulty of long recovery time.

**Circuit Operation.** The accompanying circuit schematic illustrates one type of fast-recovery blocking



Fast-Recovery Blocking Oscillator

oscillator. With the exception of diode V2, it is identical to the series-triggered blocking oscillator discussed previously in this section of the Handbook. Transformer T] provides the necessary coupling (inductive feedback) between plate and grid of electron tube V1. Terminals 1 and 2 connect to the plate (primary) winding, terminals 3 and 4 connect to the grid (secondary) winding, and terminals 5 and 6 connect to the output (tertiary) winding. Resistors R1 and R2 form a voltage divider which provides cathode bias for triode V1. The voltage developed across cathode resistor R1 biases triode V1 to plate current cutoff. Capacitor Cl is the cathode bypass capacitor for triode V1, and resistor R3 is the grid return resistor. The positive trigger pulse is applied across resistor R4, which has a relatively low value of resistance. Grid capacitor C2 and resistors R3 and R4 normally determine the time constant of the grid circuit. However, when capacitor C2 discharges, diode V2 conducts, shunting grid resistor R3, and the discharge time for the circuit is greatly reduced. Resistor R5 and capacitor c3 forma conventional plate decoupling network. The output from the blocking oscillator is taken from the tertiary winding (terminals 5 and 6) of transformer T1.

The following illustration shows the trigger-, grid-, plate-, and output-voltage waveforms in their proper time relationship. When voltage is first applied to the circuit, dc current flows through voltage divider consisting ot resistor RI and R2. This current flow develops a bias voltage on the cathode of triode V1 which is sufficient to keep the tube biased to platecurrent cutoff. Hence, no current flows in the-plate circuit.





When a positive trigger pulse is applied to resistor R4, it passes through the grid winding of transformer T1 and is applied to grid capacitor C2. The positive potential on the transformer side of capacitor C2 causes an electron flow from ground through grid resistor R3 to the grid side of the capacitor. This current flow, which eventually charges the capacitor, develops a positive voltage across grid resistor R3 sufficient to raise the bias of triode V1 above cutoff and cause VI to conduct. As plate current increases and flows through the plate winding terminals 1 and 2) of transformer Tl, it produces a magnetic field around the winding. This increasing magnetic field induces a voltage into the grid winding of the transformer. The transformer phasing is such that the induced positive voltage increases the voltage across C2, causes more current to flow through grid resistor R3, increases the charge on grid capacitor C2, and drives the grid of V1 further positive. The increase in positive grid voltage, due to feedback, causes the plate current to increase still further. This regenerative action continues. That is a continual increase in grid voltage causes a continual increase in plate current which, in turn, causes a further increase in the grid

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## **ELECTRONIC CIRCUITS**

(feedback) voltage. Meanwhile, as the plate current rapidly increases toward plate-current saturation, the grid voltage becomes more positive until it reaches zero bias, and grid current flows, charging grid capacitor C2 to its maximum value.

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When the plate-current saturation point is reached (point A on the plate-voltage waveform), current flow in the plate winding of transformer T1 no longer increases. Since there is no longer a changing magnetic field around the plate winding of the transformer, no further voltage is induced into the grid winding. Grid capacitor C2 is now fully charged, and since there is no longer a voltage across the grid winding of transformer T1 to sustain this charge, the capacitor begins to discharge. Normally, the capacitor would discharge through grid resistor R3, resistor R4, and the grid winding of the transformer. However, the negatively charged side of grid capacitor C2 is connected to the cathode of diode V2. This negative potential on the cathode of the diode makes it conduct, shunting grid resistor R3. Capacitor C2 now discharges through diode V2, resistor R4, and the grid winding of transformer T1. Since the high resistance of grid resistor R3 is shunted by diode V2 and effectively removed from the circuit, resistor R4 alone determines the discharge time constant of the circuit. Since the value of R4 is low, the time constant is short, and capacitor C2 discharges very quickly. When capacitor C2 discharges, the grid voltage level drops until it reaches the fixed cathode bias (determined by resistors RI and R2) which keeps the triode biased to cutoff, and plate current ceases.

As plate current stops flowing in the plate winding of transformer T1, the magnetic field around the winding collapses. The collapsing field induces into the plate winding a voltage of a polarity which tends to keep current flowing in the same direction. (That is, the polarity of the induced voltage is series-aiding with that of the plate-supply voltage.) The result of adding these voltages is a momentary increase in plate voltage over and above the plate-supply voltage, called overshoot (point B on the plate-voltage waveform). As the magnetic field around transformer T1 decreases in intensity, the induced voltage (overshoot) decreases accordingly, and the plate voltage quickly returns to the normal quiescent value.

Any changes of current in the primary winding of transformer T1 also induce a changing voltage into the tertiary, or output, winding (terminals 5 and 6). The polarity of the output pulse from this winding is

determined by which terminal is comected to ground. As shown in the circuit schematic, terminal 6 is grounded. Therefore, in this case, a positive output pulse results (for a negative output it would be necessary to ground terminal 5 instead).

The fast-recovery blocking oscillator provides one output pulse each time a positive trigger pulse is applied. It is ready again almost immediately to receive another trigger pulse and produce another output pulse. Therefore, it is preferred for circuits operating at fast repetition rates.

#### Failure Analysis.

No Output. Since the oscillator depends on a positive trigger pulse to initiate operation, it is important to determine whether the input pulse is of the proper polarity and of sufficient amplitude to drive the grid of VI above cutoff. Use an oscilloscope to observe the input waveform. If the proper trigger pulses are present at the input, use the oscilloscope to observe the signal at the plate of VI. If pulses similar to those shown in the illustration of the plate-voltage waveform are observed, but still no output is obtained, the output (tertiary) winding of transformer T1 is either open or shorted. Use an ohmmeter to check the continuity of this winding; also check for a short to ground (indication of less than O.lohm). If no pulses are observed at the plate of V1, either no plate voltage is present or there is a defective feedback circuit or a defective cathode-bias circuit. Measure the voltage on the plate of V1 with a high-resistance voltmeter. If no voltage is measured at this point, a number of other possibilities exist: either an open in the plate winding of transformer TI, an open plate resistor R5, or a shorted bypass capacitor C3. Use an ohmmeter to check these components and isolate the trouble. If the proper voltage is measured at the plate of V1 but no plate pulses are seen on the oscilloscope, the trouble is in either the feedback of bias circuits. Use an ohmmeter to check for an open grid capacitor, C2, or for an open grid winding of transformer T1 to clear the feedback circuits. Then check for proper resistance values of resistors Rl, R2, R3, and R4 to clear the bias circuits. If these checks fail to locate the trouble, the tube is probably at fault.

**Unstable Output.** Since the output stability of the oscillator is dependent upon the input trigger pulse, it is important to be certain that the input trigger is of the proper amplitude and frequency. Use an oscilloscope to observe the input waveform. If the proper

input waveform is observed, the bias circuit or feedback circuit may be faulty. Use an ohmmeter to check capacitor C 1 for an open or a short, and to check bias resistors RI and R2 for proper resistance values. If these checks shown that the bias circuit is not defective, check the feedback circuit with an ohmmeter. First check grid capacitor C2 for a short, and then check resistors R3 and R4 for the proper resistance values. Also use the ohmmeter to check transformer T1 for continuity of the grid and plate windings, for shorts between the windings, and for shorts to ground (less than 1 ohm).

Low Output. Low output may be caused by weak emission in the triode, low plate-supply voltage, or excessive circuit loading. If substituting a good tube for triode V1 does not remedy the trouble, use a high-resistance voltmeter to measure the plate-supply voltage. If this voltage is low, the trouble is in the power supply. If the plate-supply voltage is normal, the transformer is probably defective.

# NONSATURATING DIODE-CLAMPED BLOCKING OSCILLATOR (SEMICONDUCTOR)

#### Application.

The nonsaturating, diode-clamped blocking oscillator is used to produce synchronized, large-amplitude pulses for use as timing or synchronizing pulses in radar, communications, and data-processing equipment.

#### Characteristics.

Requires a negative input trigger pulse. Output is a single square pulse caused by transistor conduction.

Output-pulse repetition frequency is determined by the input **trigger** frequency.

Output-pulse width and rise time are determined primarily by the transformer inductance, capacitance, and resistance characteristics.

Output-pulse polarity is determined by the transformer output (tertiary) winding phasing.

Fixed, class B (cutoff) bias is employed.

# Circuit Analysis.

**General. The** nonsaturating, diode-clamped blocking oscillator produces one output puke each time a trigger pulse is applied to activate the circuit. Between trigger pulses the circuit remains in the inactive (quiescent) state, and no output is produced. The operation of the onosaturating, diode-clamped **block**ing oscillator is similar to that of other types of blocking oscillators except that in this circuit, diode clamping is employed to prevent transistor saturation and to eliminate the normal overshoot which is present in the output of other types of blocking oscillators.

Circuit Operation. The accompanying circuit schematic illustrates a nonsaturating, diode-clamped blocking oscillator using a PNP transistor connected in the common-emitter configuration. Transformer T1 provides the regenerative feedback necessary between the collector and the base of transistor O1 to obtain oscillation. The primary winding (terminals 1 and 2) is connected in series with the collector supply (made Up of  $V_{CC_1}$  and  $V_{CC_2}$ ) and the collector of transistor Q1. The secondary winding (terminals 3 and 4) is connected from ground to the base of transistor QI through dc blocking capacitor C2. This capacitor prevents the base (secondary) winding of the transformer from acting as a dc shunt to ground for the fixed cutoff bias applied to transistor Q1 through base resistor R1. Clamping diodes CR1 and CR2 limit the collector voltage swing, and prevent transistor saturation and overshoot in the output pulse. The negative input trigger is applied through coupling capacitor C 1 to the base of transistor Ol. and the output pulse is taken from the tertiary or output winding (terminals 5 and 6) of transformer T1.



Nonsaturating, Diode-Clamped Blocking Oscillator

The collector of transistor Q1 is reverse-biased by the combined negative voltage of  $V_{CC1}$  and  $V_{CC2}$ .

The base of transistor Q1 is reverse-biased by the positive voltage applied from the bias supply ( $V_{\text{\tiny BB}}$ ) through base resistor R1. Thus, in the quiescent state with no input applied transistor Q1 is completely reverse-biased and cannot conduct. Diode CR1 is reverse-biased by  $V_{\text{cc2}}$ , which is connected across the diode through the collector (primary) winding of transformer T1, diode CR2 has no bias applied because there is no current flow through the collector winding of transformer T1, and hence no voltage drop occurs it to bias diode CR2. Consequently, neither diode conducts while the circuit is in the quiescent state.

When a negative trigger pulse (such as that shown at time t<sub>1</sub> on the accompanying waveform illustration) is applied through coupling capacitor Cl to the base of transistor Ql, it forward-biases the transistor, causing collector current to begin to flow.



Theoretical Waveforms for Nonsaturating, Diode-Clamped Blocking Oscillator

The collector current flowing from  $V_{CC2}$  through the collector winding of transformer T1 to the transistor causes a magnetic field to be built up around the collector winding. The increasing magnetic field induces into the base winding of the transformer a voltage of such polarity that the potential on terminal 3 of the winding is negative with respect to ground (terminal 4). This negative potential is applied through capacitor C2 to the base of transistor QI; it

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increases the forward bias on the transistor and causes the collector current to further increase. As the collector current flowing through the primary (collector) winding of transformer T1 increases, the magnetic field around the winding increases accordingly and induces a larger voltage into the base winding of the transformer. This increasing induced voltage is fed back to the base of transistor Q1, increasing the forward bias and causing the collector current to increase still further. Thus, the regenerative feedback from the collector to the base of transistor Q1 causes the collector current to continue to increase once the input trigger puke starts current flowing. As the collector current increases the voltage on the collector of transistor Q1 decreases from the negative (cutoff) value of  $V_{cc2}$  to the less negative value of  $V_{cc1}$ (time t<sub>2</sub> on the waveform illustration). When the collector voltage becomes less negative than the value of V<sub>cl</sub> diode CR1 becomes forward-biased and conducts. Since the forward-biased (conducting) diode has a very low resistance, the voltage drop across it is negligible and the voltage on the collector of transistor Q1 is held equal to the negative value of  $V_{ccl}$ . Thus, diode CR1 clamps the collector voltage to the negative value of  $V_{ccl}$ ; in other words, it prevents the collector voltage from becoming less negative (more positive) than  $V_{ccl}$ . Consequently, the collector current flowing through the collector winding of transformer T1, increases, as a result of the regenerative feedback, until the collector voltage drops to the value of V<sub>ccl</sub>. At this time, diode CR1 begins to conduct and shunts any additional collector current flow around the collector winding of the transformer. Since there is no longer an increasing current flow in the collector winding of transformer T1, the magnetic field around the winding ceases to increase and no further voltage is induced into the base winding. Since no further induced voltage is present, the voltage across the base winding of transformer T1 decays at a rate determined by the inductance, capacitance, and resistance values of the transformer. When the voltage across the base winding of the transformer decays to zero (time  $t_3$  on the waveform illustration), no further forward bias is applied to the base of transistor Q1 and the transistor ceases to conduct. The base bias supply  $(V_{BB})$  again furnishes reverse bias to the base of transistor Q1 to hold the transistor or below cutoff until the next input trigger is applied. Meanwhile, as the collector current flow through the collector winding of transformer T1 decreases to

zero, the magnetic field around the winding collapses; this induces into the collector winding a voltage of such polarity that it tends to keep current flowing in the direction of the original collector current flow. The induced voltage forward-biases diode CR2, and the diode conducts, allowing the induced current to flow through it. Thus, diode CR2 effectively shorts out the voltage induced into the collector winding of transformer T1, and prevents it from having any effect on the remainder of the circuit. Consequently, as the collector voltage increases from maximum to zero, the collector voltage increases in the negative direction from the negative value of  $V_{cc2}$ , and the circuit returns to the quiescent state.

Any change in current in the collector winding of transformer T1 also induces a changing voltage into the tertiary, or output, winding of the transformer. The polarity of this output voltage is determined by grounding the proper terminal of the output winding. As shown in the circuit schematic, terminal 6 is grounded. Therefore, in this case, a positive output pulse results (for a negative output pulse, terminal 5 is grounded instead).

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000-ohms-per-volt meter. Be careful to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A no-output condition maybe caused by an improper input trigger, a lack of supply voltage, or a defective circuit component. First, use an oscilloscope to observe the input trigger voltage waveform, and compare it with the one shown in the equipment instruction book to determine whether the proper input trigger is applied. Next, use a vacuum-tube voltmeter to measure the supply voltage and eliminate the possibility of a defective power supply. If the proper input trigger is applied and the normal supply voltage is present, further checks must be made to locate the defective circuit component. Use an incircuit capacitor checker to check capacitors Cl and C2 for open circuits and leakage. Use an ohmmeter to check resistor R1 and transformer T1 for continuity and proper resistance value. Also use the ohmmeter as

a diode tester, to check the forward and reverse resistance of diodes CR1 and CR2.

Low or Distorted Output. Low supply voltage, a defective diode (CR1 or CR2), a defective transistor (Q1) or a faulty transformer (T1) may cause either low-amplitude or distroted output pulses. Measure the supply voltage with a vacuum-tube voltmeter to be certain that the power supply is not at fault. If the normal supply voltage is present, use an ohmmeter or diode tester to check diodes CR1 and CR2 for an adequate front-to-back ratio. If neither diode is defective, the fault is probably in either transistor Q1 or transformer T1.

# PULSE-FREQUENCY DIVIDER (ELECTRON TUBE)

### Application.

**The** pulse-frequency divider is used to produce high-amplitude pulses at a submultiple of the input trigger pulse frequency for use as timing or synchronizing pulses in radar and communications equipment.

#### Characteristics.

Output pulse frequency is a submultiple of the input pulse frequency.

Frequency-division ratio can be adjusted within a small range.

Requires a high-impedance trigger source which produces positive **trigger** pulses.

Output pulse width and rise time are determined primarily by the transformer characteristics.

Output pulse polarity is determined by the phasing of the transformer output (tertiary) **winding.** 

# Circuit Analysis.

**General. The** operation of the pulse-frequency divider is similar to that of other types of triggered blocking oscillators. However, the pulse-frequency divider is designed so that, instead of producing output pulses at the same frequency as the input pulse frequency, it produces output pulses at a frequency which is only a fraction of the input pulse frequency. In other words, the circuit divides the input pulse frequency down to a lower frequency. **The** ratio of the input pulse frequency is called the division ratio. Although pulse-frequency divider circuits have been designed with

**division** ratios as high as 100:1, a low division ratio (less than 6:1) gives the best stability. Consequently, most pulse-frequency dividers are designed to operate at low division ratios.

**Circuit Operation. The** accompanying circuit schematic illustrates a pulse-frequency divider with a division ratio that can be adjusted between 2:1 and



**Pulse-Frequency Divider** 

grid resistor R2 and the grid winding of transformer T1 to the grid of V1 (time t. on the waveform illustration).



Output-Voltege Waveforms

5:1. Transformer T1 provides the coupling (inductive feed-back) between the plate and the grid of triode V1. Terminals 1 and 2 connect to the plate (primary) winding, terminals 3 and 4 comect to the grid (secondary) winding, and terminals 5 and 6 comect to the output (tertiary) winding. The positive trigger pulses are applied through coupling capacitor C1 to the grid of triode VI. Capacitor C2 and resistors R2 and R3 make up the grid R-C circuit. Resistor R2 is variable and allows the time constant of this R-C circuit to be adjusted for the desired division ratio. Resistors RI and R3 form a voltage-divider network which supplies fixed grid bias voltage for triode V1. Resistor R4 and capacitor C3 form a conventional plate decoupling network.

The following illustration shows the trigger-, grid-, plate-, and output-voltage waveforms in their proper time relationship.

In the quiescent condition (with no trigger pulse applied), VI is held at plate-current cutoff by the fixed negative bias taken from the voltage divider made up of resistors R1 and R3, and applied through

When the first positive trigger pulse is applied to the grid of triode V1 through coupling capacitor Cl, it drives the grid above cutoff and causes the tube to conduct (time ton the waveform illustration). The increasing plate current flowing through the plate winding (terminals 1 and 2) of transformer T1 produces a magnetic field in the transformer. The changing magnetic field induces a feedback voltage into the grid winding of transformer T1. The transformer phasing the polarity are such that the induced feedback voltage drives the grid of triode VI more positive, and the plate of capacitor C2 which is connected to the negative end of the grid winding more negative. Thus, the induced feedback voltage causes two things to occur simultaneously: the capacitor charges to a higher potential, and the tube is biased more positive. The increased positive bias causes the plate current of triode V1 to increase further. The increasing plate-current flow through the plate winding of transformer T1 causes the magnetic field in the transformer to increase accordingly, and induces a still larger voltage into the grid winding of

transformer T1. This continuous increase in feedback voltage, grid voltage, and plate current produces a regenerative-feedback action which quickly drives the tube toward plate-current saturation. As the grid of triode V1 is driven more and more positive, grid current eventually begins to flow. The flow of grid current through the grid winding of transformer T1 to capacitor C2 causes the capacitor to quickly charge to its maximum negative value.

When plate-current saturation is reached (point A on the plate-voltage waveform), the plate current can no longer increase. Consequently, the magnetic field in transformer T1 no longer increases, and no feedback voltage is now induced into the grid winding. The grid of triode VI is therefore driven negative by the large negative charge on capacitor C2. This negative grid voltage causes the triode plate current to decrease. As the plate current through the plate winding of transformer T1 decreases, the magnetic field in the transformer decreases accordingly, inducing a feedback voltage of opposite polarity into the grid winding of the transformer. This induced feedback voltage drives the grid of triode V1 further negative, increasing the negative grid bias, and causing plate< urrent flow through the plate winding of transformer T1 to decrease still further. As previously explained, the regenerative feedback from the plate to the grid of triode V1 produces a continuous cycle which causes the grid to be driven far below cutoff. As plate-current occurs, the plate current ceases to flow, and the magnetic field in the transformer collapses. The collapsing magnetic field induces into the plate winding of transformer T1 a voltage os such polarity that it tends to keep current flowing in the same direction as the original plate-current flow (that is, the induced voltage is series-aiding with the platesupply voltage). The result of adding these voltages is a momentary increase in plate voltage over and above the plate-supply voltage, called overshoot (point B on the plate-voltage waveform). As the magnetic field decreases to zero, the induced voltage (overshoot) decreases accordingly, and the plate voltage returns to the normal, quiescent value.

When plate current ceases, the charge on capacitor C2 is no longer sustained, and the capacitor discharges through resistors R2 and R3 towards the negative fixed-bias value. Since the time constant of

this R-C circuit is very large, capacitor C2 discharges very slowly, and its potential decreases only a small amount by the time the plate pulse and overshoot are completed. The discharge time of the circuit is, in fact, many times longer than the input pulse repetition period. Consequently, the next input trigger pulse (time  $t_2$  on the waveform illustration) occurs while capacitor C2 is still discharging and reducing the bias towards the fixed cutoff bias value. This positive trigger pulse (number 2), when combined with the negative grid voltage remaining on capacitor C2, is not of sufficient amplitude to raise the grid of triode V1 above cutoff. Therefore, trigger pulse number 2 has no effect on the operation of the circuit, and triode VI remains cut off with capacitor C2 still discharging. The same result occurs during the next three input trigger pulses (times  $t_3$ ,  $t_4$ , and  $t_5$  on the waveform illustration). However, when the next input trigger pulse (time  $t_6$  on the waveform illustration) occurs, capacitor C2 is now discharged to nearly the fixed negative bias voltage across resistor R3 (cutoff bias). Therefore, when trigger pulse number 6 is combined with the negative grid voltage remaining on capacitor C2, the resulting pulse is of sufficient amplitude to again drive the grid of triode V1 above cutoff and cause the tube to conduct. Thus, the sixth trigger pulse causes the circuit to begin another cycle of operation. The pulse-frequency divider produces an output pulse as previously explained, and then remains inactive for the next four input trigger pulses. It produces an output pulse for every fifth input pulse. Therefore, the circuit is said to have a division ratio of 5: 1.

The division ratio of the pulse-frequency divider is entirely dependent upon the discharge time of capacitor C2, which is determined by the time constant of the grid R-C circuit. Resistor R2 is made variable so "" that the time constant of the R-C circuit can be adjusted for the desired output frequency. If the value of resistor R2 is decreased, the time constant of the R-C circuit decreases and capacitor C2 discharges more quickly. Thus by proper adjustment of resistor R2, the circuit will operate on every fourth input trigger pulse, giving a division ratio of 4:1. As the value of resistor R2 is decreased still further, the division ratio decreases accordingly. The following illustration shows the trigger- and grid- voltage waveforms for two different frequency-division ratios.



Trigger- and Grid- Voltage Waveforms for Two Settings of Resistor R2

#### Failure Analysis.

**General.** Since the output signal of the pulsefrequency divider is dependent upon the input signal, it is important to be certain that the proper trigger pulses are applied. If the proper input **trigger** pulses are not applied, the output from the circuit, if present at all, will be unstable or of the wrong frequency. Therefore, the first step in trouble-shooting this circuit is to use an oscilloscope to observe the input waveform, and compare it with the waveform shown in the equipment instruction book to be certain that it si of the proper polarity, amplitude, and frequency.

No Output. In addition to an improper input signrd, a no-output condition may be caused by a lack of plate-supply voltage, a fault in the grid circuit, a fault in the plate circuit, a defective tube, or an open output winding of transformer T1. After checking the input signal with an oscilloscope (as explained in the previous paragraph), use the oscilloscope to observe the waveform at the grid of triode V1. If no signal appears at this point, capacitor Cl is open and must be replaced. If the proper grid-voltage waveform is observed, use the oscilloscope to observe the waveform on the plate of triode VI. A proper platevoltage waveform indicates that the output winding of transformer T1 is defective. If no signal is observed on the plate of triode V1, voltage and resistance checks must be made to isolate the defective com-

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ponent. Use a high-resistance voltmeter to measure the plate-supply voltage and determine whether the power supply is at fault. Next, use the voltmeter to measure the voltage on the plate of triode V1. If no plate voltage is present, plate circuit components T1 (primary winding), C3, or R4 are either open or shorted. Use an ohmmeter to check continuity and resistance, and isolate the defective component. If the proper plate voltage is present, either the tube is defective, transformer T1 (secondary winding) is open, resistors RI, R2, or R3 are open, or capacitors Cl or C2 are shorted. Use an ohmmeter to isolate the defective component.

**Improper Division Ratio or Unstable Output. An** improper input signal, an improper bias-supply voltage, a defective tube, an open or shorted grid circuit, or a defective transformer, T1, may cause either an improper division ratio or an unstable output. After checking the input signal with an oscilloscope (as **explained** previously), use a high-resistance voltmeter to measure the bias-supply voltage. If the bias-supply voltage is correct, the trouble is in the divider circuit and not in the power supply. Use an ohmmeter to check the grid circuit of the divider for open or shorted components (C 1, C2, R1, R2, R3). Triode VI may also be at fault. Replace the tube with one known to be good, and if this still does not correct the trouble, transformer TI is probable shorted.

Low Output. A low output may be caused by three conditions: low plate voltage, low tube emission, or excessive circuit loading. Use a highresistance voltmeter to measure the plate-supply voltage and eliminate the possibility of a faulty power supply. Since defects in capacitor C3 or resistor R4 may also cause low plate voltage, use an ohmmeter to check these components. The low output may also be caused by low emission in triode VI. If replacing the tube with a good one does not correct the trouble, the low output may be caused by excessive circuit loading. Such a dondition may be caused by shorted turns in transformer T1.

## DISTANCE-MARK DIVIDER (ELECTRON TUBE)

#### Application.

**The** distance-mark divider is used to produce short time duration pulses at a submultiple of the input trigger frequency for use as distance marks in radar display indicators.

## Characteristics.

Produces output pulses at a submultiple of the input trigger pulse frequency.

Requires a low-impedance trigger source which produces positive trigger pulses.

Output consists of positive pulses taken from the cathode of the tube.

Output pulse width and rise time are determined primarily by the transformer characteristics.

## **Circuit Analysis.**

General. The distance-mark divider is a specific application of the pulse-frequency divider discussed earlier in this section of the Handbook. Like the pulse-frequency divider, the distance-mark divider produces output pulses at a submultiple of the input pulse frequency. That is, it divides the input pulse frequency down to a lower frequency. The ratio of input pulse frequency to output pulse frequency is called the diviswn ratw of the circuit. While the division ratio of many pulse-frequency divider circuits is adjustable within a small range, the division ratio of the distance-mark divider is normally freed (usually 2:1 or 3:1). In this way, the circuit can be designed to give the desired characteristics in the output pulse. Moreover, taking the output from the cathode of the tube also helps to produce the desired output pulse shape and eliminates the overshoot present in other types of blocking oscillators.

**Circuit Operation.** The accompanying circuit schematic illustrates a distance-mark divider with a division ratio of 3: 1.



**Distana?-Mark Divider** 

Transformer T1 provides the coupling (inductive feedback) between the plate and the grid of triode V1. Terminals 1 and 2 connect to the plate (primary) winding, and terminals 3 and 4 connect to the grid (secondary) winding. The input trigger pulses are applied through grid capacitor Cl and the grid winding of transformer T1 to the grid of triode VI. The division ratio of the distance-mark divider is determined by the R-C circuit made up of capacitor Cl and resistors R1 and R2. Resistor RI is variable and allows the circuit to be adjusted to compensate for variations in component values, supply voltages, and input trigger pulse amplitude. Resistors R2 and R3 form a voltage divider which provides fixed negative grid bias for triode V1. Resistor R4 and capacitor C2 form a conventional plate decoupling network. The output is taken across resistor R5, which is the cathode resistor for triode V1.

The following illustration shows trigger-, grid-, plate and cathode-voltage waveforms in their proper time relationship.



# Trigger-, Grid-, Plate-, and Cathode-Voltage Waveforms

In the quiescent condition (with no trigger pulse applied), triode V1 is held at plate-current cutoff by the fixed negative bias taken from the voltage divider made up of resistors R2 and R3, and applied through grid resistor RI and the grid winding of transformer T1 to the grid of VI (time t. on the waveform illustration).

## **ELECTRONIC CIRCUITS**

When the first positive trigger pulse is applied through grid capacitor Cl and the grid winding of transformer T1 to the grid of triode V1, it drives the grid above cutoff and causes the tube to conduct (time  $t_1$  on the waveform illustration). The increasing current flowing through the plate winding of transformer T1 produces a magnetic field in the transformer. The changing magnetic filed induces a feedback voltage into the grid winding of transformer T1. The transformer phasing and polarity are such that the induced feedback voltage drives the grid of triode V1 more positive and the plate of capacitor Cl which is connected to the negative end of the grid winding more negative. Thus, the induced feedback voltage causes two things to occur simultaneously: the capacitor charges to a higher potential, and the tube is biased more positive. The increased positive bias causes the plate current of triode V1 to increase further. The increasing plate current flow through the plate winding of transformer T1 causes the magnetic field in the transformer to increase accordingly, and induce a still larger voltage into the grid winding. This continuous increase in feedback voltage, grid voltage, and plate current produces a regenerative feedback action which quickly drives the tube toward plate current saturation. As the grid of triode V1 is driven more and positive, grid current eventually begins to flow. The flow of grid current through the grid winding of transformer T1 to capacitor C1 causes the capacitor to quickly charge to its maximum negative value.

When plate-current saturation is reached (point A on the plate-voltage waveform), the plate current can no longer increase. Consequently, the magnetic field in transformer T1 no longer increases, and no feedback voltage is now induced into the grid winding. The grid of triode **V1** is therefore driven negative by the large negative charge on capacitor Cl. This negative grid voltage, and the positive cathode voltage caused by current flow through cathode resistor R5, cause the triode plate current to decrease. As the plate current through the plate winding of transformer T1 decreases, the magnetic field in the transformer decreases accordingly, inducing a feedback voltage of opposite polarity into the grid winding of the transformer. This induced feedback voltage drives the grid of triode V1 further negative, increasing the negative grid bias, and causing plate-current flow through the plate winding of transformer T1 to decrease still further. As previously explained, the

regenerative feedback from the plate to the grid of triode V1 produces a continuous cycle of operation which causes the grid to be driven far below cutoff. **As plate-current** cutoff occurs, the plate current ceases to flow and the magnetic field in the transformer collapses. The collapsing field induces a momentary surge of voltage called overshoot, into the plate winding of transformer T1 (point B on the plate-voltage waveform). However, since tiode V1 is cut off, no current can flow through cathode resistor R5, and the overshoot is not present in the output.

When plate current ceases to flow, the charge on capacitor Cl is no longer sustained, and the capacitor discharges through resistors **R1** and R2 twoard the fixed negative bias value. The time constant of this R-C circuit is very large, and the discharge time of capacitor C 1 is many times longer than the input trigger pulse repetition period. Consequently, the next input trigger pulse (time t<sub>2</sub> on the waveform illustration) occurs while capacitor Cl is still discharging and reducing the bias toward the fixed cutoff bias balue. This positive trigger pulse (number 2), when combined with the negative grid voltage remaining on capacitor C 1, is not of sufficient amplitude to raise the grid voltage of triode V1 above cutoff. Therefore, trigger pulse number 2 has no effect on the operation of the circuit, and triode V1 remains cut off with capacitor Cl still discharging. The same result occurs during the next input trigger pulse (time t<sub>2</sub> on the waveform illustration). However, when the next input trigger pulse (time t<sub>4</sub> on the waveform illustration) occurs, capacitor Cl is discharged to nearly the fixed negative bias voltage across register R2 (cutoff bias). Therefore, when trigger pulse number 4 is combined with the negative grid voltzge remaining on capacitor Cl, the resulting pulse is of sufficient amplitude to again drive the grid of triode V1 above cutoff and cause the tube to conduct. Thus, the fourth trigger pulse causes the circuit to begin another cycle of operation. The distance-mark divider produces an output pulse as previously explained, and then remains inactive for the next two input trigger pulses. It produces an output pulse for every third input pulse. Therefore, the circuit is said to have a division ratio of 3: 1.

The division ratio of the distance-mark divider is entirely dependent upon the discharge time of capacitor C 1, which is determined by the time constant of the grid R-C circuit. Thus, the distance-mark divider can be made to produce different division

ratios by using various component values in the grid R-C circuit. Although resistor RI is variable, and will change the time constant of the circuit somewhat, this range is not normally broad enough to change the division ratio. Normally, resistor R1 is used only to adjust the circuit to compensate for variations in trigger pulse amplitude and supply voltages.

# Failure Analysis.

No Output. A no-output condition maybe caused by an improper input signal, a lack of plate-supply voltage, a fault in the grid circuit, a fault in the plate circuit, a fault in the cathode circuit, or a defective tube. After checking the input signal with an oscilloscope to be certain that the proper input is applied, use the oscilloscope to observe the waveform at the grid of triode V1. If no signal appears at this point, either capacitor Cl or the grid winding of transformer T1 is open. Use an ohmmeter to make resistance checks and isolate the defective component. If the proper grid-voltage waveform is observed, further voltage and resistance checks must be made to isolate the defective component. Use a high-resistance voltmeter to measure the plate-supply voltage and determine whether the power supply is at fault. Next, measure the voltage on the plate of triode V1. If no plate voltage is present, plate components T1 (primary winding), R4, or C2 are either open or shorted. Use an ohmmeter to check continuity and resistance, and isolate the defective component. If the proper plate voltage is present, either the tube is defective, transformer T1 (secondary winding) is open, or resistors R1, R2, R3, or R5 are open or shorted. Use an ohmmeter to isolate the defective component.

Improper Division Ratio or Unstable Output. An improper input signal, an improper bias-supply voltage, a defective tube, an open or shorted grid circuit, or a defective transformer may cause either an improper division ratio or an unstable output. After checking the input signal with an oscilloscope to be certain that it is of the proper amplitude and frequency, use a high-resistance voltmeter to measure the bias-supply voltage. If the bias-supply voltage is correct, the trouble is in the divider circuit and not in the power supply. Use an ohmmeter to check the grid circuit of the divider for open or shorted components (Cl, Rl, R2, **R3**). Triode V1 may also be at fault. Replace the tube with one known to be good. If this still does not correct the trouble, transformer T1 is probably shorted.

**Low Output.** A low output is usually caused either by low plate voltage or by low tube emission. Use a high-resistance voltmeter to measure the plate-supply voltage and eliminate the possibility of a faulty power supply. Since defects in capacitor C2 or resistor R4 may also cause low plate voltage, use an ohmmeter to check these components. If these checks fail to **locate** the trouble, the low output is probably caused by low emission in triode V1.

# SHOCK-EXCITED RINGING OSCILLATOR (ELECTRON TUBE)

#### Application.

**The** shock-excited ringing oscillator produces a short series of r-f oscillations each time an input gate is applied. The r-f oscillations are normally used as distance marks in radar indicators.

# Characteristics.

Requires a high-impedance, negative input gate.

Produces an output only when gated.

R-F output pulse duration is equal to that of the input gate.

Uses a high-Q resonant tank circuit to produce an r-f output.

Output frequency is determined by the tankcircuit inductance and capacitance values.

# Circuit Analysis.

**General. The** shock-excited ringing oscillator uses a parallel-resonant L-C (tank) circuit to produce an r-f output. An electron tube is used as a switch to control (gate) the r-f oscillations. While the basic circuit discussed below serves to illustrate the principles of operation of the shock-excited ringing oscillator, it is not suitable for use in practiced circuits. A typical practical circuit is discussed after the basic circuit operation is established.

**Circuit Operation.** The accompanying circuit schematic illustrates a basic shock-excited ringing oscillator.



**Basic Shock-Excited Ringing Oscillator** 

In the quiescent state (with no negative gate applied), positive grid bias is applied from the plate supply through grid resistor RI to the grid of triode VI, and causes the tube to conduct heavily near plate-current saturation. Electron flow is from ground, through inductor L1 and the tube to the plate supply, building up a magnetic field around the inductor. So long as a negative gate is not applied, the circuit remains in this quiescent state (triode VI conducting heavily and no r-f output).

When a negative input-gate is applied through coupling capacitor Cl to the grid of triode V1, it instantaneously drives the grid below plate-current cutoff, and holds it at cutoff for the duration of the input gate. Plate-current flow through inductor L1 abruptly ceases, and the magnetic field around the inductor collapses. The collapsing magnetic field induces into the inductance a voltage of such polarity that it tends to keep current flowing in the same direction. This is, the induced voltage causes a current to flow from ground toward the cathode of triode V1. The triode, however, is biased below cutoff by the negative gate; therefore, no current will flow through the tube. Consequently, the induced current flows around the tank circuit and charges capacitor C2 negative with respect to ground. When the magnetic field has completely collapsed, no further voltage is induced into inductor L1, and the induced current ceases to flow in the tank circuit. Since there is no longer any induced voltage sustain the charge on capacitor C2, the capacitor discharges back through

# inductor L1. The capacitor discharge current flowing through inductor L1 builds up a magnetic field around the inductor which is of opposite polarity from the original magnetic field. When capacitor C2 is full discharged, current flow around the tank circuit again ceases, and the magnetic field around inductor L1 again collapses and induces into the inductance a voltage which tends to keep current flowing in the same direction. This induced voltage causes current to flow around the tank circuit and charges capacitor C2 positive with respect to ground. After the magnetic field completely collapses, the charge on the tank capacitor is no longer sustained, and the capacitor again discharges through inductor L1, once again building up a magnetic field around the inductor in the original direction. This cycle of charge and discharge continues to repeat, producing a *ringing* effect in the tank circuit. That is, the capacitor and inductor charge and discharge alternately, causing the tank circuit to oscillate at a radio-frequency rate. Since the tank circuit has a very high Q (low loss), the r-f oscillations continue for many cycles. Because of the loss in the tank circuit produced by the d-c resistance of the inductor, successive oscillations gradually decrease in amplitude as the energy in the tank circuit is dissipated by this resistance. The resulting output waveform across the tank circuit is a series of damped oscillations, as shown in the following illustration.



Input Gate and Output-Voltage Waveforms

The damped oscillations continue until the end of the input gate. When the negative input-gate ends, the positive bias supplied by grid resistor R1 resumes control and causes triode V1 to again conduct heavily

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near plate-current saturation. When the tube conducts, the heavy plate-current flow through inductor L] produces a magnetic field around the inductor in one unchanging direction, which effectively shunts the tank circuit and decreases the circuit Q. Consequently, the r-f oscillations are effectively damped out very quickly. The heavy plate current flowing through inductor L1 once again builds up a steady magnetic field around the inductor which effectively prevents any possibility of r-f oscillation, and the circuit remains in the quiescent (no-output) state until the next input gate is applied.

Since triode V1 is cut off while output oscillations are being produced, the frequency of the output oscillations is not affected by the tube. Thus, the output frequency is determined solely by the values of inductance and capacitance in the tank circuit. The duration of the train of r-f output oscillations is determined solely by the length of time triode V1 remains cut off, and is therefore controlled by the duration of the input gate.

The basic shock-excited ringing oscillator just discussed always produced damped oscillations when an input gate is applied. Since these oscillations decrease in amplitude, they are not suitable for many applications, particularly for producing distance marks. The following circuit schematic illustrates a practical type



Typical Shock-Excited Ringing Oscillator

of shock-excited ringing oscillator which produces r-f oscillations of a constant amplitude when the input gate is applied.

The two-tube shock-excited ringing oscillator shown in the illustration is actually a switched Hartley oscillator (see Section 7 of this Handbook for a detailed discussion of Hartley circuit operation). The circuit consisting of triode V2, capacitor C2, inductor L1, and Resistor R3 is a conventional seriesfed Hartley oscillator, consisting of triode V1, capacitor C1, and resistors R1 and R2 is a switching circuit which controls the operation of the Hartley oscillator.

In the quiescent state (with no negative gate applied), no bias is applied to the grid of triode V1 and the tube conducts heavily near plate-current saturation. The electron flow is from ground, through inductor L1, triode V1, and resistor R2 to the plate supply, building up a magnetic field around inductor L1. When triode V1 is conducting, the heavy plate-current flow through inductor L1 produces a steady magnetic field around the tank inductor which effectively shunts the tank circuit and prevents the oscillator from functioning. Consequently, no r-f output oscillations are produced and the circuit remains in this state.

When a negative input-gate is applied to the grid of triode V1 through coupling capacitor Cl, it drives the grid far below cutoff. As plate current ceases to flow through tank inductor L1, the magnetic field around it collapses, inducing a voltage into the inductor which tends to keep current flowing in the same direction as the original plate-current flow (that is, from ground thru the inductor to the cathode of triode V]). As in the basic circuit discussed previously, the induced current cannot flow through triode VI (which is cut off); consequently, it flows around the tank circuit, charging capacitor C2 and initiating a ringing effect. In this practical circuit, however, any potential across the tank is also applied to the grid of oscillator tube V2, and the oscillator section of the circuit functions as a normal Hartley oscillator, producing oscillations of a constant amplitude in the tank circuit. The oscillator portion of this circuit replaces the energy dissipated in the tank coil resistance so that the resulting oscillations are always of constant amplitude. Thus, as long as the negative gate is applied, triode V1 remains cut off, and the oscillator portion of the circuit operates, producing constant-amplitude r-f oscillations.

The oscillator operates until the end of the negative input gate. When the negative gate ends, the grid bias on triode VI returns to zero, and the triode again begins to conduct heavily near plate-current saturation. When the tube conducts, the heavy current flow through inductor L1 produces a steady magnetic field around the tank inductor, effectively damping out the r-f oscillations very quickly. Thus the circuit is once again operating in the quiescent state, with triode V1 conducting heavily near saturation, and no r-f output.

The practical shock-excited ringing oscillator produces r-f oscillations of constant amplitude when a negative input gate is applied. As in the basic shock-excited ringing oscillator, the output frequency is determined by the values of inductance and capacitance in the tank circuit, and the duration of the r-f output is determined by the length of the input gate. The output waveform is the same as that shown for the basic circuit, except that all the oscillations are of constant amplitude.

#### Failure Analysis.

No Output. Failure of the shock-excited ringing oscillator to produce an output when the gate is applied may be caused by a defective switching circuit, by a defective oscillator circuit, or by a lack of plate-supply voltage. To isolate the trouble to one portion of the circuit, temporarily remove triode V1. If continuous output oscillations are now produced, the trouble is in the switching section of the circuit. Use an ohmmeter to check capacitor Cl for a shorted condition, and resistors R1 and R2 for continuity and proper value. If none of these parts are defective, triode V1 is probably shorted. If continuous output oscillations are not produced when triode V1 is temporarily removed, the fault is either in the oscillator section of the circuit or due to a lack of platesupply voltage. Use a high-resistance voltmeter to check the supply voltage and the plate voltage of triode V2. Proper values of these voltages indicate that the trouble is in the oscillator section of the circuit and not in the power supply. Use an ohmmeter to check capacitor C2 and inductor L1 for a shorted condition, and to check resistor R3 for continuity and proper value. If the trouble still persists, triode V2 is probably at fault.

**Continuous R-F Output.** Defects in the switching portion of the **shock-excited** ringing oscillator may cause the circuit to produce output oscillations

whether or not the input gate is present. Use an ohmmeter to check capacitor Cl and resistors R1 and R2 for a shorted or open condition. If none of these parts are defective, triode VI is probably at fault.

Low Output. Defects in the oscillator portion of the circuit or a low plate-supply voltage may cause either low-amplitude output oscillations or damped (decreasing) output oscillations. First measure the plate-supply voltage with a high-resistance voltmeter to eliminate the possibility of low-supply voltage. If the plate-supply voltage is normal, the trouble is in the oscillator section of the circuit and not in the power supply. (If the output oscillations are damped, triode V2 is probably inoperative and should be replaced with a tube known to be good.) Use an ohmmeter to check inductor L1, capacitor Cl, and resistor R3 for continuity of shorts. If no defective parts are found, triode V2 is probably defective.

# SHOCK-EXCITED PEAKING OSCILLATOR (ELECTRON TUBE)

### Application.

The shock-excited peaking oscillator is used to produce very narrow positive pulses at the beginning of each input gate for use as trigger or synchronizing pulses in radar modulators, display indicators, and other electronic devices.

#### Characteristics.

Requires a high-impedance, negative input gate.

Produces one very sharp positive pulse at the beginning of each negative input gate.

Produces one relatively broad negative pulse at the end of each negative input gate.

Uses a critically damped tank circuit to produce an output.

Shape of positive output pulse is determined by tank inductance and capacitance valves.

### Circuit Analysis.

**General. The** shock-excited peaking oscillator uses a critically damped resonant **L-C** (tank) circuit to produce a peaked output. An electron tube is used as a switch to control (gate) the tank circuit.

**Circuit Operation. The** accompanying circuit schematic illustrates a typical shock-excited peaking oscillator.



### **Shock-Excited Peaking Oscillator**

Capacitor Cl and resistor R1 form a conventional R-C input circuit for triode Vl, and capacitor C2 and resistor R2 form a conventional cathode bias circuit for the tube. Inductor L1 and its distributed capacitance, C, form a parallel-resonant tank circuit. Since the distributor capacitance is small, the resonant frequency of the tank circuit is very high (approximately 2 me). This r-f tank is critically damped by resistor R3. That is, the value of resistor R3 is such that it allows the tank circuit to oscillate for only a half cycle after oscillation is started.

The following illustration shows the input-gate and plate-voltage (output) waveform in their proper time relationship.





In the quiescent state (with no negative input-gate applied), no bias is applied to the grid of triode VI, and the tube conducts heavily near plate-current saturation. The plate current is held constant by the cathode bias developed across cathode resistor R2. This constant plate current flowing through inductor LI builds up a steady magnetic field around the inductance. **So** long as a negative gate is not applied, the circuit remains in this quiescent state.

When a negative gate is applied through coupling capacitor Cl to the grid of triode VI (time t<sub>1</sub> on the waveform illustration), it instantaneously drives the grid far below cutoff, and holds it below cutoff for the duration of the input gate. Plate-current flow through inductor L] abruptly **ceases**, and the magnetic field around the inductor collapses. The collapsing magnetic field induces into the inductance a voltage of such polarity that it tends to keep current flowing in the same direction as the original plate-current flow. This induced current flowing in

the inductor charges the distributed (tank) capacitance, C, negative on the plate-supply side of the capacitance and positive on the triode side of the capacitance (polarity as shown in schematic). Since the charge time of the capacitance is determined by the resonant frequency of the tank circuit, and the resonant frequency is very high, the capacitance charges very quickly to its maximum value. The potential across the charged capacitance is seriesaiding with the plate-supply voltage, and the resultant voltage on the plate of triode V1 momentarily rises above the plate-supply voltage (point A on the plate-voltage waveform). When the magnetic field around the inductor completely collapses, there is no longer any induced voltage to sustain the charge on the distributed (tank) capacitance, the capacitance begins to discharge. Since the dc resistance or resistor R3 is much lower than the impedance of inductor L1 at the resonant frequency, the distributed capacitance discharges very quickly through the resistor, and the triode plate voltage quickly returns to the platesupply value. Thus, the shock-excited peaking oscillator produces one very sharp positive pulse at the beginning of the negative input gate.

Triode V1 remains cut off, and no further output is produced until the end of the negative input gate. When the input gate ends (time  $t_2$  on the waveform illustration), the grid bias on triode VI returns to zero, and the triode again begins to conduct heavily near plate-current saturation. As plate current flows through inductor Ll, a magnetic field builds up around the inductor. The increasing magnetic field induces into the inductance a voltage of such polarity that it tends to oppose the plate current flowing through the inductor. This induced voltage is seriesopposing with the plate-supply voltage, and the resulting voltage on the plate of triode VI momentarily drops below the plate-supply voltage (joint Bon the plate-voltage waveform). As the magnetic field around the inductance builds up to its maximum value and ceases to increase, the opposing induced voltage decreases to zero, and the triode plate voltage returns to the plate-supply value. Thus at the end of the negative input gate the shock-excited peaking oscillator produces a negative-going pulse and then returns to the quiescent state, with triode V1 conducting heavily near saturation and a steady unchanging magnetic field built up around inductor L1.

The output from the **shock-excited** peaking oscillator is a series of alternate positive- and negative-going pukes occurring respectively at the beginning and the end of the negative input gate. Since the positive output pulses are much sharper, and of greater amplitude, than the negative-going output pulses, the positive pulses are normally the desired portion of the output. The negative-going output pulses are usually eliminated with a clipping or limiting circuit which passes only the desired positive out-put pulses.

## Failure Analysis,

No Output. Failure of the shock-excited peaking oscillator to produce an output when the proper negative input gate is applied may be caused by a defective circuit component, a defective tube, or a lack of plate-supply voltage. After measuring the plate-supply voltage with a high-resistance voltmeter to be certain that the power supply is operating properly, use the voltmeter to measure the voltage on the cathode of triode V1. A lack of cathode voltage indicates that either resistor R2 or capacitor C2 is shorted, or the triode is faulty. If checking resistor R2 and capacitor C2 with an ohmmeter does not reveal a shorted component, triode VI is probably at fault and should be replaced with a tube known to be good. If the proper voltage is measured on the cathode of triode V1, inductor L1 may be open or shorted, capacitor Cl may be open, or resistor R1 or R3 may be open or shorted. Use an ohmmeter to check these components for continuity, shorts, and proper resistance values. If these checks fail to locate a defective component, triode V1 is probably defective.

Low Output. Output pulses of low amplitude may be caused by low plate-supply voltage, low tube emission, or a defective cathode bias circuit. First, measure the plate-supply voltage with a highresistance voltmeter to eliminate the possibility of a faulty power supply. If the proper plate-supply voltage is present, use an in-circuit capacitor checker to check cathode capacitor C2 for an open. If this capacitor is open, degenerative action in the cathode bias circuit will cause a low output. If both the platesupply voltage and capacitor C2 are normal, low emission in triode V1 is probably the cause of the low-output condition. Replace triode VI with a tube known to be good.

**Distorted Output.** Defeats in the plate circuit of triode V1 may cause a distorted output. Use an ohmmeter to check shunt resistor R3 for continuity and the proper resistance value. If resistor R3 is not defective, inductor L1 is probably at fault.

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# SECTION 7 MULTI VIBRATORS

## PART 7-1. ASTABLE

## ASTABLE (FREE-RUNNING) MULTI VIBRATORS I

## General.

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The term astable multivibrator refers to a class of multivibrator or relaxation-oscillator circuits that can function in either of two temporarily stable conditions and is capable of rapidly switching from one temporarily stable condition to the other. The astable multivibrator is frequently referred to as a freerunning multivibrator. It is basically an oscillator consisting of two stages coupled so that the input signal to each stage is taken from the output of the other. One stage conducts while the other is cut off until a point is reached at which the stages reverse their condition; that is, the stage which had been conducting cuts off, and the stage that had been cut off conducts. Thus, the circuit becomes free-running because of the regenerative feedback, and the frequency of operation is determined primarily by its couplingcircuit constants rather than by an external synchronizing pulse.

In electron tube circuits, the frequency of operation can be as low as one-sixtieth of a Hz or as high as 100 kHz; in semiconductor circuits, the frequency of operation ranges from 400 Hz to 200 kHz.

The output of the astable multivibrator is usually nearly rectangular in form. A symmetrical output results when the R-C time constants of the coupling circuits are made equal. Rectangular pulses of almost any desired width (time duration) can be obtained by proportioning the R-C time constants of the coupling circuits with respect to one another; the resulting pulse output is unsymmetrical since the R-C time constants of the coupling circuits are no longer equal.

The operating frequency of the astable multivibrator can be changed by switching values of R or C, or both R and C, in the coupling circuits to alter the time constants. For example, a multivibrator designed to operate at 800 pps can be changed to a lower frequency, such as 400 pps, by simply switching additional capacitors into the circuit in parallel with the existing coupling capacitors to lower the repetition frequency.

The frequency stability of the multivibrator is somewhat better than that of the typical blocking oscillator. However, a disadvantage of the multivibrator is that its output impedance is essentially equal to the plate-load resistance and this resistance must be relatively high in order to obtain good frequency stability. Also, the negative-going waveform is generated at a much lower impedance than the positivegoing waveform. Because a changing load will also affect the frequency stability, the output is sometimes fed to a cathode follower, in order to isolate the load from the multivibrator plate circuit. In some instances the desired output from the multivibrator is a differentiated waveform, and this waveform, in turn, is applied to the cathode follower; in this circuit configuration the load will have the least effect upon the multivibrator frequency stability.

# BASIC ASTABLE (FREE-RUNNING) MU LTIVIBRATOR (ELECTRON TUBE)

## Application.

The basic (plate-to-grid coupled) astable multivibrator produces a square-wave output for use as trigger or timing pulses.

#### Characteristics.

Free-running oscillator; does not require trigger pulse to produce oscillations.

Operating frequency is determined primarily by the R-C time constants in the feedback (plate-to-grid) coupling circuits and by applied voltage.

Frequency stability of 3 percent can be obtained. Input tirgger pulses may be applied to the circuit for synchronization to produce a stable output; it may be synchronized at the trigger-ulse frequency or integral submultiple thereof.

Symmetrical square- or rectangular-wave output is produced when the R-C time constants of the grid circuits are equal. Unsymmetrical output is produced when the R-C time constant of one grid circuit is purposely made several times greater than that of the other; for this condition the two tubes are cut off for unequal periods of time.

Output impedance is essentially equal to plate-load impedance.

## **Circuit Analysis.**

**General. The** free-running plate-to-grid coupled multivibrator is a basic astable multivibrator. The circuit is fundamentally a two-stage R-C coupled amplifier with the output of the second stage coupled to the input of the first stage! Thus the ouput signal is fed back in the proper phase to reinforce the input signal; as a result, sustained oscillations occur.

**Circuit Operation.** The following circuit schematic illustrates two triode electron tubes in a basic free-running rnultivibrator circuit. Electron tubes VI and V2 are identical-type triode tubes; although the accompanying schematic illustrates two separate triodes, a twin-triode is frequently used in this circuit. Capacitor Cl provides the coupling from the plate of V2 to the grid of V1; capacitor C2 provides the coupling from the plate of V1 to the grid of V2. Resistors RI and R2 are the grid resistors for V1 and V2, respectively; resistors R3 and R4 are the plate-load resistors for V1 and V2, respectively.



## Triode Plate-to-Grid Coupled Astable Multivibrator

Capacitor Cl and resistor RI form an R-C circuit to determine the discharge time constant in the grid circuit of V1; capacitor C2 and resistor R2 determine the discharge time constant in the grid circuit of V2. Output pulses can be taken from the plate of either or both electron tubes. Capacitors C3 and C4 are the output coupling capacitors for VI and V2, respectively.

When voltage is first applied to the circuit, the grids of both tubes are at zero bias and plate current

starts to flow through plate-load resistors R3 and R4. Also, capacitors Cl and C2 begin to charge when the applied voltage appears at the plate of each tube. If the constants of both stages of the circuit are alike, the currents through both tubes may at first be nearly equal. In practice, the symmetrical free-running multivibrator component values are held to close tolerances in order to obtain good frequency stability; the value of coupling capacitors Cl and C2 are at least 2 percent tolerance, grid resistors R1 and R2 are 1 percent tolerance, and plate-load resistors R3 and R4 are usually 5 percent tolerance. Hewer, in spite of the close tolerance of the components, there will always be some slight difference in the two currents. This small difference in tube currents will cause a further unbalance, resulting in a regenerative action which rapidly switches the circuit to a condition wherein one tube is conducting maximum current and the other is cut off.

For example, if initidly the current through tube V1 should be slightly greater than that through V2, the voltage drop across plate-load resistor R3 will be greater than the drop across resistor R4. This results in a lower plate voltage for VI. This decrease in plate voltage is coupled through coupling capacitor C2 to the grid of V2 as a negative-going instantaneous grid voltage which reduces the plate current of V2. When the current through V2 is decreased, the current through plate-load resistor R4 is also decreased; therefore, the voltage drop across resistor R4 decreases, resulting in a rise in the plate voltage of V2. This increase in plate voltage is coupled through coupling capacitor Cl to the grid of V1 as a positive-going instantaneous grid voltage which increases the plate current of VI. The drop across plate-load resistor R3 increases, the plate voltage of V1 decreases, and as before, the decrease in the plate voltage of V1 is coupled to the grid of V2 as a negative-going voltage. The regenerative switching action just described continues rapidly until V2 is cut off and V1 is at maximum conduction.

In order to cut off plate current in V2, the grid of v2 must be driven negative beyond the cutoff voltage. The negative grid voltage results from a charge on coupling capacitor C2. Since this charge leaks off through grid resistor R2, the grid voltage at V2 does not remain in a negative condition but starts to return to zero as C2 discharges through R2 and the cathode-to-plate conduction resistance of V1. When C2 discharges sufficiently and the grid voltage cutoff point

is reached, plate current once again starts to flow through V2, initiating another switching action similar to the first action described. However, this time as V2 conduts, coupling capacitor Cl discharges through grid resistor R1 to cut off the plate current in Vl, and the switching action ends with V1 cut off and V2 at maximum conduction. Here again, the negative charge existing on coupling capacitor Cl must discharge through grid resistor R1 and tube V2 before the grid voltage cut off point is reached and V1 can conduct to initiate another switching action. The switching action repeats continuously with first one tube and then the other tube conducting.

# Theoretical Waveforms for a Symmetrical Free-Running Multivibrator

For the following discussion of circuit operation, refer to the accompanying illustration which shows a simplified schematic and waveforms for a symmetrical free-running multivibrator.

At time t. (start of time interval a) on the waveform illustration, the grid of VI (e<sub>d</sub>) has been driven negative to cut off the tube, and, as a result, the plate voltage of V1 (e<sub>pl</sub>) has risen rapidly to approach the supply-voltage value (E<sub>bb</sub>). Coupling capacitor C2 is quickly charged through the low cathode-to-grid internal resistance of V2 and the plate-load resistor, R3. The voltage waveform at the plate of VI  $(e_{p})$  is rounded off, and the waveform at the grid of V2  $(e_{g2})$  has a small positive spike of the same time duration as a result of the charging of coupling capacitor C2. Since at this time the grid of V2 is slightly positive, V2 conducts heavily and the plate voltage of V2  $(e_{p_2})$  drops to a minimum. Note that the plate voltage waveform (e. ) exhibits a small negative spike of the same time uration as the positive spike on the grid waveform  $(e_{g2})$ .

While coupling capacitor C2 is being charged, coupling capacitor C1 (previously charged) discharges through grid resistor RI and through the conduction resistance of V2. Capacitor Cl cannot change its charge immediately; therefore, it produces a negative voltage ( $e_{gl}$ ) across grid resistor R1, which decays at an exponential rate (toward zero) as capacitor Cl discharges. The rate of discharge is determined primarily by the R-C time constant of RI and Cl. Although the conduction resistance of V2 is included in the discharge path of Cl, the resistance is small as compared with the resistance of R1, and can therefore be neglected.

When the negative voltage  $(e_g)$  produced across grid resistor R1 decreases near the end of time interval a and reaches cutoff, V1 immediately conducts and the plate voltage of V1  $(e_{P1})$  drops to a minimum; the circuit now switches to the other condition with V2 cut off by the discharge of capacitor C2 through grid resistor R2. This condition is shown on the waveform illustration as the start of time interval b. Coupling capacitor C2 discharges through grid resistor R2 and through the conduction resistance of V1. The rate of discharge is determined primarily by the R-C time constant of R2 and C2. (The conduction resistance of V1 is small and can be neglected.)

When the negative voltage  $(e_{g2})$  produced across grid resistor R2 decreases near the end of time interval b and reaches cutoff, V2 immediately conducts

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and the plate voltage of V2  $(e_{P2})$  drops to a minimum; the circuit now switches to the other condition with VI cut off by the discharge of capacitor Cl through grid resistor R1. This condition is shown on the waveform illustration as the termination of interval **b** at time  $t_1$ .

In the discussion of circuit operation given above, the multivibrator was assumed to be a symmetrical (or balanced) multivibrator; that is, coupling capacitors Cl and C2 are equal, reistors RI and R2 are equal, and plate-load resistors R3 and R4 are also equal. Therefore, the discharge time constants of RI and C 1 and of R2 and C2 are equal. Also, the time intervals (a, b, c, and d) between the switching actions are equal to one another. To obtain a pulse output which is unsymmetrical (asymmetrical or unbalanced), it is necessary to proportion the time constants in the coupling circuits so that one tube remains cut off for only a short period of time while the other is cut off for a much longer period. For example, if the time constant of R1 and Cl is made short compared to the time constant of R2 and C2, then V1 will be cut off for a short period of time while V2 will be cut off for a longer period. Thus, the time intervals a and c, shown on the waveform illustration will be short while time intervals b and d will be long.

The time interval for either output pulse may be approximated if the voltage change across the coupling capacitor, the R-C time constant of the discharge path, and the cutoff voltage of the tube are known. The approximate time interval, t, for the capacitor to discharge to cutoff may be determined by use of the following formula:

$$t \cong 2.30 \text{ RC} \log \frac{E_c}{E_{co}}$$

- where: t = time interval to discharge to cutoff (seconds)
  - **E**<sub>c</sub> = maximum voltage change across capacitor
  - $E_{co}$  = negative cutoff value for tube
  - $\mathbf{R}$  = resistance of grid resistor (megohms)
  - $C = capacitance of coupling capacitor (<math>\mu f$ )



If the grid resistor, R, is returned to a positive voltage source, such as the plate-supply voltage  $(E_{bb})$ , the formula becomes:

$$t \cong 2.30 \text{ RC } \log \frac{E_{bb} + E_c}{E_{bb} + c}$$

where:  $\mathbf{E}_{\mathbf{bb}}$  = plate-supply voltage

The natural operating frequency (Hertz) of the oscillator,  $f_o$ , may be calculated from the following formula:

f.. 
$$\frac{1}{t_1+t_2}$$

where:  $t_1$  = time interval to discharge to cutoff for V1 grid circuit.

> t<sub>2</sub> = time interval to discharge to cutoff for V2 grid circuit.

The free-running multivibrator may be synchronized with a stable external source to force the period of multivibrator action to be exactly the same as the synchronizing source. In this case the multivibrator is called a driven multivibrator. Synchronizing signals, when used, are applied to the grid of one multivibrator tube if the impedance of the synchronizing source is high, or to the cathode if the impedance of the source is low. In either case, the frequency of the synchronizing signal must be slightly higher than the natural operating frequency of the multivibrator so
that the synchronizing pulse occurs just prior to the time that normal switching action would occur.

The output of the multivibrator is taken from either or both plate circuits through an outputcoupling capacitor (C3 or C4). In cases where it is desired to minimize the effect of a varying load impedance on the multivibrator frequency stability, a cathode follower is used for isolation.

#### **Failure Analysis**

No Output. Assuming that the multivibrator is a free-running type and no synchronizing signal is applied, the applied plate and filament voltages should be measured to determine whether they are within specified values. If either coupling capacitor Cl and C2 should become leaky or shorted, a positive potential will be present on the grid of the associated tube and, as a result, the tube will conduct heavily; the other tube will also conduct heavily, since it will be at zero bias. A similar condition could exist if either coupling capacitor Cl or C2 should open; in this case the feedback necessary to sustain oscillations cannot. occur and both tubes will conduct heavily because the grids are at zero bias. If the circuit is in a nonoscillating condition, the voltage at each plate should be measured to determine whether plate-load resistor R3 or R4 is open. If either is open, there will be no plate voltage present on the associated plate; also, the other tube will donduct heavily because of zero bias, and its plate voltage will be low. If either output coupling capacitor (C3 or C4) should become leaky or shorted, the input resistor of the following stage can form a voltage divider which also includes the associated plate-load resistor (R3 or R4). If the input resistor of the foilowing stage is returned to ground or to a negative potential, voltagedivider action may reduce the voltage available at the plate of the multivibrator to the point where oscillations will cease; also, the additional current through the plateload resistor (R3 or R4) may cause the resistor to burn out.

**Incorrect Frequency or Pulse Width.** 'f'he critical components governing the frequency and pulse width of the multivibrator are those in the coupling circuits. Any change in components governing the R-C discharge time constant will directly affect frequency and pulse width; a change in capacitor Cl or C2 or resistor R1 or R2 will have the greatest effect. A change in the value of plate-load resistor R3 or R4

will affect the amplitude of the output, and it will also have an effect upon the frequency, but not nearly as much as the components mentioned above.

A drift in frequency of the free-running multivibrator will generally occur if the applied plate voltage should change approximately 10 percent from the specified value; also, some frequency drift may occur if the lament voltage should drop below the specified value.

In a practical circuit, where the muhivibrator is free-running and is not synchronized from an external source, means should be provided to adjust the applied plate voltage or to adjust the value of resistance in each grid circuit. This provision enables the circuit to be adjusted to the correct frequency and pulse width, and compensates for differences in individual tube characteristics when a tube substitution has been made.

If either output coupling capacitor (C3 or C4) should become leaky or shorted, the voltagedivider action which can occur may reduce the amplitude of the output waveform and cause the multivibrator to operate at a higher frequency, since the grid capacitor (Cl or C2) discharge time is dependent upon the amount of change in capacitor voltage. The operation of the following stage may also be affected by the change in grid-bias voltage resulting from the voltage-divider action.

# BASIC ASTABLE (FREE-RUNNING) MU LTIVIBRATORS (SEMICONDUCTOR)

#### Application.

The free-running astable multivibrator circuit is a basic circuit. It is normally used to produce a square-wave output for use as a trigger or timing pulse in electronic equipments; this basic curcuit, when modified for application to switching circuitry, is representative of a class of circuits which perform computer logical operations (counting, shift register, and memory circuits), control functions (relay driver circuits), and a variety of similar applications in radar and communications systems.

#### Characteristics.

Free-running oscillator; does not require a trigger pulse to produce oscillations.

Operating frequency is determined primarily by the time constants in the feedback (collector-to-base) coupling circuits and by the applied voltage.

Symmetrical square-wave or rectangular-wave output is produced when the time constants of the coupling circuits are equal. Unsymmetrical output is produced when the time constant of one coupling circuit is purposely made several times greater than that of the other; for this condition the transistors are cut off or conducting for unequal periods of time.

Output taken from collector of either transistor in common-emitter circuit configuration.

Output impedance is very low when transistor is in conducting (on) state; output impedance is approximately equal to collector load resistance when transistor is in cutoff (off) state.

### **Circuit Analysis.**

**General. The** free-running collector-coupled multivibrator is a basic astable mtdtivibrator. The circuit is fundamentally a two-stage, R-C-coupled, commonemitter amplifier, with the output of the second stage coupled to the input of the first stage. Since the signal in the collector circuit of a common-emitter amplifier is reversed in phase with respect to the input to the base, a portion of the collector output of each stage is fed to the base electrode of the other stage. Thus, the output signal from each stage is fed back in the proper phase to reinforce the input signal on the base electrode of the other stage; as a result of this regenerative feedback, sustained oscillations occur.

The collector-coupled, **common-emitter multivi**brator circuit described in the following paragraphs is analogous to the basic plate-to-grid-coupled electrontube mtdtivibrator circuit described earlier in this section of the handbook.

**Circuit Oparation. The** following circuit schematic illustrates two transistors in a basic freerunning multivibrator circuit.



Basic Free-Running Astable Multivibrator Using PNP Transistors

Transistors Q1 and Q2 are identical PNP transistors used in a common-emitter circuit configuration; either junction or point contack transistors may be used in this circuit. Resistors R1 and R4 are the collector load resistors for Q1 and Q2, respectively; R2 and R3 are the base-biasing resistors for Q1 and Q2, respectively. Capacitor C 1 provides the coupling from the collector of Q1 to the base of Q2; capacitor C2 provides the coupling from the collector of Q2 to the base of Q1. Capacitor Cl and resistor R3 form an R-C circuit to determine the discharge time constant for the base of O2; capacitor C2 and resistor R2 determine the discharge time constant for the base of Q1. Capacitors C3 and C4 are the output coupling capacitors for Q1 and Q2, respectively. An output waveform can be taken from the collector element of either transistor, or output waveforms can be taken from the collector elements of both transistors.

The common-emitter configuration illustrated uses a single-battery power source,  $V_{cc}$ . Forward bias for the base of transistor Q1 is obtained through the low-resistance emitter-base junction, which is in series with resistor R2 across the voltage source,  $V_{cc}$ ; since the base of Q1 is placed at a negative potential with respect to its emitter, the required forward bias for the PNP transistor is thereby established. In a like manner, forward bias for the base of transistor Q2 is obtained through the emitter-base junction and resistor R3. When voltage is first applied to the multivibrator, the current which flows in each collector load resistor, RI and R4, is determined by the effective resistance offered by transistors Q1 and Q2 for a given value of base-bias voltage.

The multvibrator circuit shown in the schematic appears to be a balanced (or symmetrical) circuit, since each **R-C-coupled** stage is identical to the other; however, in spite of the use of close-tolerance components, there will always be minor differences in circuit resistances ana in juncuon resistances within the transistors themselves. (A balanced circuit is assumed here and not necessarily a multivibrator designed for unsymmetrical output.) As a result of this inherent unbalance, the initial collector current (resulting from the forward-bias conditions set up by the emitter-base junction resistances and bias resistors R2 and R3) for each transistor is different, and the immediate effect produced by regenerative action between the coupled stages is that one transistor conducts while the other is cut off. For the purpose of this explanation, assume that initially more collector current flows through transistor Q1 than through transistor Q2; thus, as the collector current of Q1 increases, the voltage at the collector of Q1 decreases with respect to its emitter, or ground. In other words, the collector of Q1 becomes less negative and this, in effect, acts as a positive-going pulse, which is coupled through capacitor Cl to the base of transistor Q2. The positive-going pulse at the base of Q2 makes the base positive with respect to its emitter (ground) and, as a result, Q2 approaches cutoff. The collector current of Q2 decreases because of the revers-bias action, and the voltage at the collector of Q2 increases, and approaches the supply voltage,  $-V_{cc}$ . In other words, the collector of Q2 becomes more negative and this, in effect, acts as a negative-going pulse, which is coupled through capacitor C2 to the base of transistor Q1. The negative-going pulse at the base of QI places the base negative with respect to its emitter

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(ground), and the collector current of QI is further increased because of the forward-bias action. This regenerative process continues until Q1 is driven into saturation (as a result of increased forward-bias), and Q2 is cut off (as a result of the reverse-bias conditions).

For the following discussion of circuit operation, refer to the circuit schematic shown previously, and also to the waveforms shown in the following illustration.



# Theoretical Waveforms for a Symmetrical Free-Running Multivibrator (Using PNP Transistors]

Assume that transistor Q1 is conducting and has just reached saturation. When Q1 is at saturation, its collector current no longer increases but rather becomes a constant value (see Q1 collector waveform for period Tl); therfore, there is no further change in collector voltage to be coupled through capacitor C1 to the base of transistor Q2. The voltage at the base of Q1 is only a few tenths of a volt negative, and, as a result, capacitor C2 quickly charges (see Q1 base waveform for period Tl) through the low resistance of R4 to a potential which is approximately equal to  $-V_{cc}$ . Since the **collector** voltage at QI (Q1 is conducting heavily) is at nearly ground potential, capacitor Cl (previously charged) starts discharging (see Q2 base waveform for period Tl) at a rate which is equal to the time constant R3C1, through transistor Ql, the voltage source, and resistor R3.

As capacitor Cl discharges, the voltage at the base of Q2 becomes less and less positive (negative-going) until **a** point is reached where reverse bias is no longer applied and Q2 is able to conduct (as shown in the Q2 base waveform at the end of period Tl).

When the base of Q2 returns to a forward-bias condition, Q2 begins to conduct and its collector current begins to flow through load resistor R4. As the collector voltage at Q2 drops (see Q2 collector waveform for period T2), a changing (positive-going pulse) voltage is coupled through capacitor C2 to the base of transistor Q1. The voltage at the base of Q1 is only a few tenths of a volt negative, and, as a result of the charge on capacitor C2, reverse bias is applied to the base of Q1. Transistor Q1 is driven to cutoff, and the collector voltage of Q1 rises (see Q1 collector waveform for period T2). This rise, coupled through Cl, will drive the base of Q2 further into the forward-bias condition. The voltage at the base of Q2 is only a few tenths of a volt negative, and the collector voltage at Q1 is approximately  $-V_{cc}$ ; as a result, capacitor Cl quickly recharges (see Q2 base waveform for period T2) through the low resistance of RI to a potential which is approximately equal to -V<sub>cc</sub>. Since the collector voltage at Q2 (Q2 is conducting heavily) is at nearly ground potential (see Q2 collector waveform for period T2), capacitor C2 (previously charged) starts discharging at a rate which is equal to the time constant R2C2, through transistor Q2, the voltage source, and resistor R2.

As capacitor C2 discharges (see **Q1** base waveform for period T2), the voltage at the base of Q1 becomes less and less positive (negative-going) until a point is reached where reverse bias is no longer applied, and O1 is able to conduct.

When the base of Q1 begins to conduct, collector current begins to increase through load resistor R1. As the voltage drops at the collector of Q1 a changing (positive-going pulse) voltage is coupled through capacitor C 1 to the base of transistor Q2 to initiate another cycle of operation.

For each half-cycle of operation, whenever a changeover of the multivibrator takes place one of two actions occurs: in one case capacitor Cl recharges through load resistor R1 and the base-emitter junction of Q2 to the vrdue of the supply voltage,  $V_{cc}$ , while capacitor C2 discharges through the series circuit consisting of transistor Q2, the voltage source, and resistor R2; in the other case, capacitor C2 recharges through load resistor R4 and the base-emitter junction of Q1 to the value of the supply voltage,  $V_{cc}$ , while capacitor C1 discharges through the series circuit consisting of transistor Q4 and the base-emitter junction of Q1 to the value of the supply voltage,  $V_{cc}$ , while capacitor C1 discharges through the series circuit consisting of transistor Q1, the voltage source, and resistor R3.

The discharge times of capacitors Cl and C2 are relatively long as compared with their charge times; thus, the capacitor which is charging reaches its final potential long before the other capacitor has completely discharged. This action can be clearly seen if the Q1 and Q2 base waveforms in the illustration are compared for periods T1 and T2.

The waveforms shown in the preceding illustration are for a symmetrical multivibrator, and the output taken from the collector of either transistor is a square wave. The waveforms shown in the following illustration are for an unsymmetrical multivibrator, and the output waveforms have unequal time durations. The general circuit operation is identical with that of the symmetrical multivibrator; however, the on and off times, or charge and discharge times, are different since different R-C values are used.



# Theoretical Waveforms for an Unsymmetrical Fraa-Running Multivibrator (Using PNP Transistors)

#### Failure Analysis.

No Output. An open-circuited, short-circuited, or over-biased condition, as well as a defective transistor, can cause lack of output. The transistor element voltages can be checked against their proper values to determine the defective component. With the circuit in the non-oscillating condition, a check of the voltages at the collector of each transistor will reveal whether load resistor **R1** or R4 is open. If either resistor is open, there will be no collector voltage on the associated transistor; also, the other transistor will conduct heavily because of the reduced bais (the circuit is inoperative), and its collector voltage will be low, (In this case the collector resistor can burn out.) If coupling capacitor Cl or C2 is leaky or shorted, the collector resistor of one transistor will be shunted across the base resistor of the other transistor, and the fixed bias on the base of the transistor to which the defective capacitor is connected, will be increased. If the increase in bias is sufficient, the transistor will be rendered inoperative. (Under certain conditions, an unsymmetrical output can occur.) Also, if coupling capacitor Cl or C2 is open, or if resistor R3 or R4 is open, the circuit will be rendered inoperative, since the R-C circuit resistance will be infinite. If output capacitor C3 or C4 is open, the circuit will operate at a slightly different frequency because of load changes, but no output will be observed.

**Incorrect Frequency and Pulse Width. The** critical components governing the frequency and pulse width of the multivibrator are those in the coupling circuits. Any change in the components governing the **R-C** discharge time constant will directly affect the frequency and pulse width. A change in value of coupling capacitor C 1 or C2 or in the base resistance R2 or R3 will have the greatest effect. Although a change in the value of collector resistor RI or R4 will affect the frequency and pulse width, it will have a greater effect on the output amplitude of the waveform.

A 10 percent variation in the collector voltage may cause some frequency drift. However, in practical circuits where the multivibrator is unsynchronized and free-running, adjustments are usually provided to adjust the collector voltage or the base resistance (usually the latter). In this manner the circuit can be set to the correct frequency and pulse width, and can be compensated for the difference in transistor characteristics when a replacement is made.

If output coupling capacitor C3 or C4 is leaky or shorted, the voltage divider action which can occur through the base resistance of the next stage may reduce the amplitude of the output waveform and cause the multivibrator to operate at a higher frequency. This is true because the discharge time in the base circuit is dependent on the amount of change in the voltage applied to the capacitor. Another effect can be a change in the operation of the following stage caused by the bias voltage resulting from this voltage divider action.

If this following stage employs a PNP transistor, the forward bias on the transistor will be increased, with a resultant "increase in collector current. The excessive collector current may cause burnout of the collector resistor or the transistor, depending on the ratings of those parts. If the stage employs an NPN transistor the bias will be reversed and cutoff may occur.

# PENTODE ELECTRON-CO UPLEO ASTABLE MULTIVIBRATOR

#### Application.

The pentode electron-coupled astable multivibrator produces a square-wave output for use as trigger or timing pulses.

## Characteristics.

Essentially the same characteristics as the basic astable multivibrator discussed earlier in this section with following exceptions:

Operating frequency is determined primarily by the  $\mathbf{R}$ - $\mathbf{C}$  time constants in the feedback (screen-to-grid) coupling circuits and by the applied screen voltage.

Changes in load have minimum effect upon multivibrator frequency because load is isolated from pentode screen (multivibrator plate) circuit by electron-stream coupling and supressor-grid action of tube.

# Circuit Analysis.

General. The pentode electron-coupled multivibrator is basically a free-running (triode) plate-togrid-coupled multivibrator using the screen grids of sharp cutoff, pentode-type tubes as plates for the multivibrator switching function. The circuit is fundamentally a two-stage R-C amplifier with the output (screen grid) of the second stage coupled to the input of the first stage. The screen grid of each tube functions in the oscillator circuit as though it were the plate of a triode. Thus, the ouput signal from the screen grid is fed back in the proper phase to reinforce the input signal; as a result, sustained oscillations occur. The output, taken from the plate-load resistor, is coupled to the mr.dtivibrator oscillatory circuit through the electron stream of the pentode tube.

**Circuit Operation. The** following circuit schematic illustrates two pentode electron tubes in a basic free-running multivibrator circuit. Electron tubes VI or V2 are identical sharp cutoff, pentodetype tubes. Capacitor Cl provides the coupling from the screen grid of V2 to the grid of Vl; capacitor C2 provides the coupling from the screen grid of VI to the grid of V2. Resistors R1 and R2 are the grid resistors for V1 and V2, respectively; resistors R3 and R4 are the screen resistors for VI and V2. Resistors R5 and R6 are the plate-load resistors for V1 and V2, respectively. Resistor R7 is a series voltage-dropping resistor which is common to both screen-grid circuits.

Capacitor Cl and resistor R1 form an R-C circuit to determine the discharge time constant in the grid circuit of VI; capacitor C2 and resistor R2 determine the discharge time constant in the grid circuit of V2.

Output pulses can be taken from the plate of either or both electron tubes. Capacitors C3 and C4 are the output coupling capacitors for V1 and V2, respectively.



Pentode Electron-Coupled Astable Multivibrator

The switching action of the electron-coupled multivibrator is similar to that of the triode plate-togrid-coupled multivibrator circuit, previously described in this section.

When voltage is first applied to the circuit, the grids of both tubes are at zero bias and both plate and screen curents start to flow; the plate currents pass through plate-load resistors R5 and R6, and the screen currents pass through resistors R3 and R4 and through the common voltage-dropping resistor, R7. Also, capacitors Cl and C2 begin to charge when the applied voltage appears at the screen of each tube. The currents through both tubes may be equal at first; however, in spite of the close tolerances of the components in the control-grid and screen-grid circuits, there will always be some slight difference in the total currents will cause a further unbalance, resulting in a regenerative action which rapidly

switches the circuit to a condition wherein one tube is conducting maximum screen and plate currents and the other is cut off.

For example, if initially the total plate and screen current through tube VI should be slightly greater than that through V2, the voltage drop across screen resistor R3 will be greater than the drop across screen resistor R4. This results in a lower screen voltage for V1. This decrease in screen voltage is applied through coupling capacitor C2 to the grid of V2 as a negative going instantaneous grid voltage which reduces the plate and screen currents of V2. When the screen current of V2 is decreased, the current through screen resistor R4 (and resistor R7) is also decreased; therfore, the voltage drop across resistor R4 decreases, resulting in a rise in the screen voltage of V2. This increase in screen voltage is fed through coupling capacitor Cl to the grid of V1 as a positive-going instantaneous grid voltage which increases the screen current of V1. The voltage drop across screen resistor R3 increases as the screen current increases, the screen voltage of V1 decreases, and, as before, the decrease in the screen voltage of V1 is applied to the grid of V2 as a negative-going voltage. Note that as the screen current of V1 increases the screen current of V2 decreases. Since the screen currents of V1 and V2 flow through dropping resistor R7, the voltage (with respect to ground) at the junction of resistors R3, R4, and R7 remains essentially constant throughout the entire period of oscillation.

The regenerative switching action just described for the screen-grid to control-grid coupling of the pentode multivibrator circuit continues rapidly until V1 is cut off and VI is at maximum conduction. In order to cut off plate and screen current in V2, the grid of V2 must be driven negative beyond the cutoff voltage. The negative grid voltage results from a charge on coupling capacitor C2. Since this charge leaks off through grid resistor R2, the grid voltage of V2 does not remain in a negative condition but starts to return to zero as C2 discharges through resistor R2 and the conduction resistance (cathode to screen grid) of VI. When capacitor C2 discharges sufficiently and the grid voltage cutoff point is reached, the plate and screen currents once again start to flow through V2, initiating another switching action similar to the first action described. However, this time as V2 conducts, coupling capacitor Cl discharges through grid resistor R1 to cut off the plate and screen currents in

VI, and the switching ac tion ends with V1 cut off and V2 at maximum conduction. Here again, the charge existing on coupling capacitor C 1 must discharge through grid resistor R1 and tube V2 before the grid voltage cutoff point is reached and VI can conduct to initiate another switching action.

In a sharp cutoff pentode tube, as long as the plate voltage is greater than the applied screen voltage, the plate current in the tube depends largely upon the screen voltage rather than upon the value of the applied plate voltage. The screen grid is made positive with respect to the cathode and therefore attracts electrons from the cathode; however, most of the electrons attracted by the screen pass on through the screen grid and reach the plate. It is this flow of electrons to the plate that couples the multivibrator action to the plate circuit, from which the output waveform is obtained. The term electron coupled refers to this method of coupling within the tube.

The fact that plate current is largely independent of applied plate voltage makes it possible to produce the desired output waveform in the plate circuit since the positive potential existing on the screen will control the number of electrons arriving at the plate. Furthermore, the plate and screen currents are controlled by the action of the control grid; therefore, when the tube is at maximum conduction and plate current flows through the plate-load resistor, the voltage drop across the plate-load resistor is also maximum and the plate voltage of the tube is minimum. When the tube is cut off, the plate voltage is at maximum. Thus, the voltage at the plate of the tube is determined by the coupling of the electron stream to the plate circuit, and this, in turn, is governed by the switching action of the multivibrator oscillatory circuit (control and screen grids). The suppressor grid acts to shield the screen from the plate and prevents changes in loading from affecting the oscillatory circuit; therefore, the frequency of the multivibrator is reasonably independent of changes in output loading.

Like the triode plate-to-grid-coupled multivibrator, described previously in this section, the proportioning of the **R-C** time constants of the coupling circuits **(R1C1** and R2C2) determine whether the output waveform will be symmetrical or unsymmetrical.

The output waveform is taken from either or both plate circuits and coupled to the load through an output-coupling capacitor (C3 or C4).

## Failure Analysis.

No Output. Assuming that the multivibrator is a free-running type and no synchronizing signal is ap plied, the plate, screen, and filament voltages should be measured to determine whether they are within specified values. If either coupling capacitor Cl or C2 should become leaky or shorted, a positive potential will be present on the grid of the associated tube, and, as a result, the tube will conduct continuously; the other tube will also conduct, since it will be at zero bias. A similar condition could exist if either coupling capacitor Cl or C2 should open; in this case, the feedback necessary to sustain oscillations cannot occur, and both tubes will conduct continuously because the grids are at zero bias. If this circuit is in a nonoscillating conditon, the voltage at each screen grid should be measured to determine whether screen resistor R3 or R4 is open. If either is open, there will be no screen voltage present on the associated screen grid, and the tube will be cut off; also, the other tube will conduct continuously because of zero bias, and its plate and screen voltages will be low. Furthermore, if resistor R7 should open, there will be no voltage at either screen grid, and both tubes will be cut off.

Note that, if a plate load resistor (R5 or R6) should open, the multivibrator oscillatory circuit (control and screen grids) may function normally, but no output waveform will be obtained from the tube associated with the open plate-load resistor.

**Incorrect Frequency or Pulse Width.** The critical components governing the frequency and pulse width of the multivibrator are those in the coupling circuits. Any change in components governing the R-C discharge time constant will directly affect frequency and pulse width; a change in capacitor C1 or C2 or resistor R1 or R2 will have the greatest effect. A change in the value of screen resistor R3 or R4 or dropping resistor R7 will also have an effect upon the frequency and pulse width, but not nearly as much as the coupling components mentioned above.

In a practical circuit, where the multivibrator is free-running and is not synchronized from an external source, means may be provided to adjust the applied screen voltage or to adjust the value of resistance in each control-grid circuit. This provision enables the circuit to be adjusted to the correct frequency and pulse width and compensates for differences in individual tube characteristics when a tube substitution has been made. **Reclucad Output.** A reduction in ouput amplitude is generally caused by a defective tube; however, it can also be caused by a decrease in the applied plate voltage or an increase in the resistance of the **associ**ated plate-load resistor (R5 or R6). A similar condition can also result from a change in the value of the applied screen voltage; however, in this case the multivibrator frequency will probably be affected before a noticeable change in output occurs.

If either output coupling capacitor (C3 or C4) should become leaky or shorted, the input resistor of the following stage can form a voltage divider which - also includes the associated plate-load resistor (R5 or R6). If the input resistor of the following stage is returned to ground or to a negative potential, voltage-divider action may reduce the voltage available at the plate of the multivibrator and reduce the amplitude of the output waveform; also, the additional current through the plate-load resistor (R5 or R6) may cause the resistor to burn out. Furthermore, the operation of the following stage may also be affected by the change in grid-bias voltage resulting from the voltage-divider action.

# TRIODE CATHODE-COUPLED ASTABLE MULTI-VIBRATOR

#### Application.

The triode cathode-coupled astable multivibrator produces a square- or rectangular-wave output for use as trigger or timing pulses.

#### Characteristics.

Free-running oscillator; does not require trigger pulse to produce oscillations.

Operating frequency is determined primarily by the **R-C** time constant in the grid circuit and by the applied voltage.

Frequency stability is rather poor when unsynchronized; however, stability is good when synchronized by an external timing pulse.

Circuit may be synchronized at the timing-pulse frequency or integral submultiple thereof.

Either a symmetrical square- or rectangular-wave output or an unsymmetrical output maybe produced by changing circuit constants for voltages.

Output impedance is essentially equal to plate-load - impedance.

Circuit Analysis.

General. The triode cathode-coupled astable multivibrator is functionlly similar to the basic Triode Plate-to-Grid-Coupled Astable Multivibrator discussed at the beginning of this section of the handbook. R-C coupling is provided from the plate of V1 to the grid of V2, as in the basic plate-to-grid-coupled circuit, but in this instance the coupling from V2 to V2 is direct, being affected in the cathode circuit through a common cathode resistor; the R-C coupling (in the basic circuit) from the plate of V2 to the grid of VI, is therefore, omitted. A variation of this cathode coupled circuit uses separate cathode bias resistors, with V2 coupled to V1 through a capacitor rather than directly. Output signals can be taken from the plate of either or both electron tubes, as in the basic plate-to-grid-coupled circuit configuration.

**Circuit Operation.** The following circuit schematic illustrates two triode electron tubes in a basic cathode-coupled astable (free-running) multivibrator circuit employing direct coupling in the cathode circuit. Electron tubes V1 and V2 are identical-type triode tubes; although the schematic illustrates separate triodes, a twin-triode is frequently used in this circuit. Capacitor Cl provides the coupling from the plate of V1 to the grid of V2. Resistors R1 and R2 are the grid resistors of V1 and V2, respectively; resistors R3 and R4 are the plate-load resistors of V1 and V2, respectively. Resistor R5 is the common cathode-coupling and bias resistor coupling V2 to VI.



## Triode Cathode-Coupled Astabla Multivibrator (Direct Coupling)

Capacitors C2 and C3 are the output coupling capacitors for V1 and V2, respectively.

Capacitor Cl and resistor R2 form and R-C circuit establishing the time constant in the grid circuit of V2. The intial charge path for capacitor Cl is from its left side through V1 plate-load resistor R3 and the plate supply voltage to ground, then through cathode resistor R5 and the low (approximately IK) cathodeto-grid conduction resistance of V2 to the right side of Cl, as illustrated by the solid-line path in part A of the following simplified schematic diagram. When the conduction through V2 decreases, and the grid of V2 no longer draws current, the charge path for Cl is completed through grid resistor R2, as illustrated by the dotted-line path in the same diagram. For all practical purposes, Cl charge completely during the time that V2 conducts; the amount of charge via R2 is negligible. Part B of the diagram shows the discharge path for capacitor Cl to be through grid resistor R2, common cathode resistor R5, and the low cathodeto-plate conduction resistance of V1. The time constant of the charge path and the cutoff voltage level of V1 determine the length of time that V1 is cutoff; the time constant of the discharge path and the cutoff voltage level of V2 determine the length of time that V2 is cutoff.



Charge and Discharge paths for Capacitor C1

If the time constants for the charge and discharge of Cl are equal, a symmetrical square-wave output is produced by the circuit; by making the charge and discharge R-C time constants different, the circuit produces an asymmetrical, or unsymmetrical, rectangular-wave output. Although the conduction resistance of VI and the resistance of cathode resistor R5 are in the discharge path, their resistance value is small as compared with that of R2, and are, therefore, neglected in the discharge path time-constant calculations.

For the following discussion or circuit operation, refer to the preceding illustrations in addition to the following illustration which shows the theoretical waveforms for a symmetrical triode cathodecoupled a stable multivibrator employing direct coupling between the cathodes. When voltage is first applied, the grids of both tubes are at zero bias and plate current begins to flow through plate-load resistors R3 and R4. When voltage is applied to the plate of VI, capacitor Cl begins to charge along the path previously outlined. As Cl charges, the grid of V2 becomes positive. Since there is no coupling capacitor from the plate of V2 to the grid of VI, the voltage at the plate of V2 has no effect on the conduction of V1. The plate current of V2 flowing through cathode resistor R5 makes the voltage at the top of the resistor positive with respect to ground. This voltage is a bias voltage of sufficient amplitude to cut off conduction of V1 and still permit V2 to conduct, since at this time the grid of V1 is at ground (zero volts) and the grid of V2 is at a positive potential. Thus, the initial conditions fo circuit operation are established; that is, V2 is conducting and V1 is cut off.



## Theoretical Waveforms for Symmetrical Cathode-Coupled Astable Multivibrator (Direct Coupling)

The foregoing multivibrator action is summarized at time t. (start of time interval a) on the waveform

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illustration. Note that the grid of V2  $(e_{g2})$  is driven positive, causing heavy conduction through this tube. At the same instant, the plate voltage of V2  $(e_{P2})$ decreases (is negative-going) as a result of plate current through plate-load resistor R4. Also, the same plate current, flowing through common cathode resistor R5, produces a positive voltage  $(e_k)$  which provides a bias sufficient to cut off VI and cause the **plate** voltage  $(e_{Pl})$  of this tube to approach B+. The positive-going voltage at the plate of V1 is instantaneously coupled through capacitor Cl to the grid of V2, driving this grid still further positive. All of the action described is instantaneous and cumulative, so that the high positive potential on the grid of V2 causes this tube to conduct heavily, while VI is cut off.

With VI cut off, its plate voltage is at B+, and capacitor Cl charges toward this value. The waveform at the plate of V1 ( $e_{pl}$ ) is rounded off, and the waveform at the grid of V2 ( $e_{g2}$ ) has a small positive spike of the same time duration as a result of the charging of capacitor Cl. Since at this time V2 is conducting, its plate voltage ( $e_{p2}$ ) drops. Note that the plate-voltage waveform has a small negative spike of the same time duration as the positive spike on the grid waveform.

As capacitor Cl charges, electrons are accumulated on its right side; this accumulation of electrons is a negative charge which acts in opposition to the positive potential on the grid of V2, in effect causing this potential to decrease from its most positive excursion. This is illustrated during time interval a (betwe<sub>m</sub>t. and  $t_1$ ), where the rapid charging of C1 is represented by the steep portion of the V2 grid voltage  $(e_{g2})$  waveform. Note that during the rapid charge time of Cl the positive voltage on the grid of V2 decreases until, at  $t_1$ , it is equal to the voltage  $(e_k)$  across common cathode resistor R5. At this instant the grid of V2 ceases to draw current. However, Cl continues to charge, but at slower rate through grid resistor R2, which is much larger in value than the total resistance in the "fast" charge path. This change in the R-C time constants of the charging paths of Cl accounts for the abrupt change in the voltage waveforms at t1.

During time interval b (from  $t_1$  to  $t_2$ ), capacitor Cl continues to charge slowly and the grid voltage of V2 decreases slowly; this causes a reduction in the plate current of V2, which results in a decreasing volt-

age drop across common cathode resistor R5. This action continues until the voltage drop across resistor R5 decreases to the level where tube V1 is no longer held below cutoff. In other words, since the bias on tube V1 is determined by the cathode voltage  $(e_k)$ , VI remains cut off so long as the cathode voltage is positive with respect to ground by more than the cutoff voltage (bias) of V1. When the cathode voltage drops to the level of the V1 cutoff voltage, as at t<sub>2</sub> on the cathode voltage  $(e_k)$  waveform, V1 conducts and rapidly cuts off V2 because the large negativegoing signal at its plate is coupled through capacitor .-C1 to the grid of V2. Thus, the **first** switching action occurs; that is, V2 is cutoff and VI is conducting.

When tube VI is conducting, capacitor Cl discharges through grid resistor R2, common cathode resistor R5, and the plate resistance of VI. The grid voltage of V2 approaches cutoff as capacitor Cl discharges; this is illustrated by the V2 grid voltage  $(e_{\sigma 2})$ waveform during time interval c (between  $t_2$  and  $\bar{t}_3$ ). At t<sub>3</sub>the grid voltage of V2 just reaches the cutoff level, permitting this tube to conduct. When the plate current of V2 increases, the voltage across common cathode resistor R5 (waveform  $e_k$ ) also increases (goes positive); this increases the bias on V1 and thereby reduces the conduction of V1. The decreasing plate current of V1 produces a positive-going signal across its plate-load resistor, R3, which, in turn, is coupled through capacitor Cl to the grid of V2, causing this grid to become highly positive. In addition to increasing the plate current of V2, the positive grid voltage again causes grid current flow and charges capacitor Cl. Thus, the second switching action occurs and the cycle is now complete as the intitial conditions once again are reached; that is, V2 is conducting and VI is cutoff.

In the preceding discussion the multivibrator was considered to be a symmetrical type; that is, the periods for conduction and cutoff of the tubes are equal. An asymmetrical, or unbalanced, output can be obtained by having V2 cutoff for a longer period than V1. Adjusting the value of the cathode resistance will permit this to happen, since it is the bias voltage developed across the common cathode resistor that determines when VI begins conduction. In this case, the combined time intervals of a and b will be less than time interval c.

Another configuration of a triode cathode-coupled astable multivibrator is the circuit shown in the

**ELECTRONIC CIRCUITS** 

**MU LTIVIBRATORS** 

following schematic diagram. This circuit is identicd to the basic common-cathode-resistor-coupled circuit just discussed, except that the feedback from V2 to VI now is by capacitive coupling through C4 between the two cathodes. Although the same switching action occurs between the two tubes and the cutoff time of V2 is still determined by the discharging of capacitor Cl through grid resistor R2, the cutoff time of VI in this instance is determined by the charging of capacitor C4 through its cathode resistor, R5. (Note that this circuit differs from the basic common-cathode-resistor-coupled multivibrator in that, in addition to capacitive coupling between cathodes, separate cathode resistors are used.)



Triode Cathode-Coupled Astable Muitivibrator (Capacitive Coupling)

# **ELECTRONIC CIRCUITS**

The charge and discharge paths for capacitors Cl and C4 are depicted in the following illustration. Note that capacitor Cl (parts A and B of the illustration) the paths are the same as in the direct-coupled circuit just discussed, except that the cathode resistor through which capacitor Cl now charges initially is R6. The charge path for capacitor C4 (part C of the illustration) is from its right side through the low cathode-to-plate conduction resistance of V2, plate-

load resistor R4, and the plate-supply voltage to ground, then through V1 cathode resistor R5 to its left side. Part D of the illustration shows the discharge path for capacitor C4 to be from its left side through the low cathode-to-plate conduction resistance of V], plate-load resistor R3, and the plate-supply voltage to ground, then through V2 cathode resistor R6 to its right side.



A. CAPACITOR CI CHARGE PATHS



C. CAPACITOR C4 CHARGE PATH



B. CAPACITOR CI DISCHARGE PATH



D. CAPACITOR C4 DISCHARGE PATH

Charge and Discharge Paths for Capacitors CI and C4 of Capacitive-Coupled Muftivibrator The free-running frequency of the output signal is determined primarily by the values of R-C time constants R2-C 1 in the grid of V2 and R5-C4 in the cathode circuit, and by the value of the applied voltage. The symmetry of the square-wave output signals depends upon the degree of balance between the two tubes and their associated circuit components.

Consider now the operation of the astable multivibrator being discussed. When voltage is first applied to the circuit, the grids of both tubes are at zero bias, and plate current begins to flow through plate-load resistors R3 and R4. Also, capacitor Cl begins to charge by drawing grid current through resistor R2 and tube V2, making the grid of this tube positive. The plate current of V2 flowing through cathode resistor R6 makes the voltage at the top of the resistor more positive with respect to ground. This positive voltage swing is coupled through capacitor C4 to the cathode of V1, where it acts as a bias voltage to hold V1 cutoff. At this instant, capacitor C4 begins charging through resistor R5 toward the positive voltage at the top of resistor R6. The positive voltage at the top of R5 holds V1 cut off until C4 reaches the approximate potential across R6. At this time, the decrease in current through R5 decreases the bias on VI and allows it to conduct, thereby causing the multivibrator switching action. That is, conduction of VI caauses the voltage at the VI plate to decrease, and this negative-going voltage is coupled through capacitor Cl to the grid of V2, where it drives the grid negative and cuts off V2.

When V2 is cutoff, capacitor Cl discharges through R2, R5, and V1. Also, the voltage on the cathode of V2 decreases (becomes less positive); this negative going voltage is coupled through capacitor C4 to the cathode of V1. Since V1 is already conducting the negative-going signal merely aids its conduction. However, the plate current of V1 flowing through cathode resistor R5 produces a positive voltage at the top of this resistor. Capacitor C4 now discharges through Vl, plate-load resistor R3, and cathode resistor R6. As capacitor C4 discharges, the voltage at the top of resistor R6 decreases (becomes less positive) because of the accumulation of electrons on the right side of capacitor C4. When the combination of the voltage on the grid of V2 (becoming less negative as capacitor Cl discharges through resistor R2) and the voltage on its cathode (becoming less positive as capacitor C4 discharges through resistor R6) decreases sufficiently, V2 again conducts. The switching action repeats continuously with first one tube and then the other tube conducting.

The output of the multivibrator is taken from either or both plate circuits through output coupling capacitor C2 or C3. In cases where it is desired to minimize the effect of varying load impedance on the frequency stability of the multivibrator, a cathode follower is used for stability.

The triode cathode-coupled astable multivibrator, like the plate-to-grid-coupled type, may be synchronized with a stable external souce to force the period of the multivibrator action to be exactly the same as that of the synchronizing source. The frequency of the synchronizing signal must be slightly higher than the natural operating frequency of the multivibrator so that the synchronizing pulse occurs just prior to the time that normal switching action would occur.

#### Failure Analysis.

No Output. Assuming that the multivibrator is a free-running type and no synchronizing signals are applied, the plate and filament voltages should be measured to determine whether they are within the specified values. If coupling capacitor Cl should become leaky or shorted, a positive potential will be present on the grid of V2 and, as a result, tube V2 will conduct heavily; V1 will remain cutoff because of the high positive potential (bias) on its cathode as a result of the heavy conduction of V2. If the circuit does not oscillate, measure the voltage at each plate to determine whether plate-load resistor R3 or R4 is open. If either resistor is open, there will be no voltage on the associated plate; also, the other tube will conduct heavily and, as a result of the heavy conduction, its plate voltage will be low.

In the common-cathode-resistor-coupled circuit configuration, if cathode resistor R5 were to open there would be no output because neither tube would conduct, and the plate voltage of both tubes would be at B+. In the capacitive-coupled-cathode circuit configuration, if cathode resistor R5 or R6 were to open only the associated tube (V1 or V2, respectively) would not conduct. If coupling capacitor C4 were to open there would be no feedback from V2 to V1, and thus no output from the multivibrator.

**Reduced Output.** A reduction in the output amplitude is generally caused by a defective tube; however, it can also be caused by a decrease in the applied

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plate voltage or an increase in the resistance of the associated plate-load resistor, R3 or R4. If either output coupling capacitor, C2 or C3, should become leaky or shorted, the input resistor of the following stage can form a voltage divider which also includes the associated plate-load resistor, R3 or R4. If the input resistor of the following stage is returned to ground or to a negative potential, voltage-divider action may reduce the voltage available at the plate of the multivibrator and reduce the amplitude of the output waveform; also, the additional current through the plate-load resistor, R3 or R4, may cause the resistor to burn out. Furthermore, the operation of the following stage may also be affected by the change in grid-bias voltage resulting from the voltagedivider action.

**Incorract Frequency or Pulse Width. The** critical components governing the frequency and pulse width of the muhivibrator are those in the coupling circuits. Any change in the components governing the grid or cathode R-C time constants will directly affect the frequency and pulse width; a change in the R-C combinations of R2-C1 or R5-C4 will have the greatest effect. A change in the value of plate-load resistor R3 or R4 will affect the amplitude of the output; it will also have an effect on the frequency, but not nearly so much as the components mentioned above.

If the plate-supply voltage,  $+E_{bb}$ , should change approximately 10 percent from the specified value, a drift in frequency will generally occur; some frequency drift may also occur if the filament voltage should drop below the specified value.

In a practical circuit, where the multivibrator is free-running and not synchronized from an external source, a variable resistor may be provided to adjust the applied plate voltage or to adjust the value of resistance in each grid circuit. This provision enables the multivibrator to be adjusted to the correct frequency and pulse width, and permits adjustment to compensate for differences in individual tube characteristics when a tube substitution is made.

If either output coupling capacitor (C2 or C3) should become leaky or shorted, the voltage-divider action which can occur may reduce the amplitude of the output waveform and cause the multivibrator to operate at a higher frequency, since the grid capacitor (Cl) discharge time is dependent upon the amount of change in capacitor voltage.

# PART 7-2. BISTABLE

# BISTABLE (START-STOP) MULTIVIBRATORS General.

The term bistable *multivibrator* refers to one class of multivibrator or relaxation oscillator circuits that can function in either of two stable states and is capable of switching rapidly from one stable state to the other upon the application of a trigger pulse. In the strict sense of the word, the bistable multivibrator is not an oscillator; rather, it is a circuit having two conditions of stable (bistable) equilibrium and requiring two input triggers to complete a single cycle. The operation of the bistable multivibrator is dependent upon the timing-control action involved in the transfer of conduction from one tube to the other, initiated by an input trigger pulse of proper polarity and sufficient amplitude. Because there is a sudden reversal (or "flopping") from one stable state to the other, the bistable multivibrator is frequently referred to as a *flip-flop* circuit.

The bistable multivibrator produces an output pulse, more commonly called a "gate", having fast rise and fall times and extreme flatness on top. To generate this type of waveform the circuit requires one trigger pulse for turn-on (start) and another trigger pulse for turn-off (stop), thus generating a "step" function for each input trigger. When the trigger pulses are of constant frequency and are applied at long time intervals (low frequency), the gates generated are wide. On the other hand, when the trigger pulses are of constant frequency and are applied at short time intervals (high frequency), the gates generated are narrow. In all cases, however, two input trigger pulses are required to complete one cycle of operation, resulting in an output gate frequency one- half that of the input trigger frequency.

Although the turn-on and turn-off input trigger pulses (which can be applied from different sources as well) can be of either positive or negative polarity, a negative trigger is preferred. A reason for this requirement is that if a tube is biased far beyond cutoff, a high-amplitude positive pulse is required to drive the tube from cut off into conduction. On the other hand, a low-amplitude negative pulse will immediately cut off conduction of a tube. In addition, the circuit used to generate a low-amplitude pulse requires less power.

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When a transistor is operating in the saturation region, a phenomenon known as minon"ty carn"er storage occurs. Because the collector-base voltage is limited in its excursion by the resistance in the collector circuit, the collector cannot accept all of the minority carriers injected by the emitter, and, as a result, an excess of minority carriers is built up in the base region. In a PNP transistor that is in a state of saturation, an excess of holes is built up in the base; before the transistor can be turned off, this excess must be removed. Thus, the turn-off operation is a function of the amount of minority carrier storage. Minority carrier storage is one limiting factor in the switching speed of the multivibrator; other factors that limit the switching speed are the operating level of the transistors, collector capacitance, and external circuit elements.

Minority carrier storage can be prevented by limiting the excursion of the collector voltage of a switching stage to an area outside the saturation region of the transistor. In this case, the collector current is not limited by the collector circuit resistance, but rather by the maximum current limitation of the transistor. This is the basis of operation of the "nonsaturating multivibrator"; this circuit is discussed in detail later in this section, as are several other semiconductor bistable multivibrator circuits and bistable multivibrator triggering techniques.

The rectangular-gate output of the bistable multivibrator can be either positive or negative in polarity. Each gate is formed by the combination of positive and negative step functions produced by turning the multivibrator on and off. The negative-going step is inherently faster than the positive-going step. When connecting other circuits to the bistable multivibrator output, precautions should be taken so as to prevent the shunting capacitance from causing undesirable effects on the rise and fall times of the step function.

# BASIC FLIP-FLOP (ECCLES-JORDAN) MU LTIVIBRATOR (ELECTRON TUBE)

#### Application.

**The** basic flip-flop (Eccles-Jordan) multivibrator produces a square-or rectangular-wave output for use as gating or timing signals, or for on-off switching operations in binary counter circuits.

#### Characteristics.

Circuit assumes one of two stable states: one tube normally conducting with the other tube normally cut off, and vice versa.

Requires two input triggers to complete one cycle of operation; the circuit assumes a stable state upon completion of each half-cycle of operation.

For a constant-frequency input, the output frequency is one-half that of the input trigger frequency.

Input triggers can be either positive or negative; positive trigger affects normally cut-off tube, and negative trigger affects normally conducting tube.

Symmetrical triggering occurs when the same trigger pulse is applied simultaneously; unsymmetrical triggering occurs when triggers are applied separately.

Symmetrical or unsymmetrical output gate depends on timing sequence of input trigger pulses; input triggers from different sources (turn-on and turn-off triggers) produce unsymmetrical gate output.

Plate-to-grid feedback coupling is direct (through resistors), with bypass capacitors used to speed up switching from one stable state to the other.

Circuit can be made to assume the same stable state whenever voltages are applied by incorporating a definite imbalance within the circuit or by using a manually controlled "reset" signal.

Tubes can be grid-biased by connecting to negative supply, or cathode-biased by connecting cathodes through voltage divider to positive supply.

#### Circuit Analysis.

General. The basic flip-flop (Eccles-Jordan) Multivibrator is capable of producing a square- or rectangular-wave output pulse (gate) in response to two input triggers. This type of multivibrator has two stable (bistable) states - one tube is normally conducting while the other tube is normally held cut off - and will function for only one-half cycle upon the application of an input trigger. Feedback from the plate of one tube to the grid of the other is direct through a coupling resistor bypassed with a capacitor, whose function is to reduce or eliminate the effects of tube interelectrode capacitance. Because two input triggers (turn-on and turn-off) are required to complete one cycle of operation, the output-gate frequency of the bistable multivibrator is one-half the input trigger frequency. The output gate length is determined by the time interval of the turn-on and turn-off input trigger. Output signals can be taken from the plate of either or both electron tubes.

**Circuit Operation. The** accompanying circuit schematic illustrates two triode electron tubes in the basic



**Basic FlipFlop Multivibretor** 

multivibrator circuit. Electron tubes VI and V2 are identical-type triode tubes; although the accompanying schematic illustrates two separate triodes, a twintriode is frequently used in this circuit. Resistors R1 and R2 are the grid resistors for V1 and V2, respectively. Resistor R3 provides the direct coupling from the plate of V1 to the grid of V2, and resistor R4 provides the direct coupling from the plate of V2 to the grid of V1. Feedback resistors R3 and R4 are bypassed with capacitors C3 and C4, respectively. These capacitors permit faster switching action from one tube to the other by reducing the effects of tube interelectrode capacitance. Resistors R5 and R6 are the plate-load resistors for V1 and V2, respectively. Capacitors Cl and C2 are the input-trigger coupling capacitors for VI and V2, respectively; they provide symmetrical triggering. Capacitors C6 and C7 are the output-gate coupling capacitors for V1 and V2, respectively. Operating bias for this bistable multivibrator, which is cathode-biased, is determined by the combination of the cathode and respective grid circuit voltage dividers. The cathode circuit voltage divider consists of common cathode resistor R7, bypassed with capacitor C5, and resistor R8; the voltage divider for the grid circuit of V1 consists of resistors R1, R4, and R6, and the voltage divider for the grid circuit of V2 consists of resistors R2, R3, and R5.

Consider now the operation of the basic flip-flop multivibrator by referring to the preceding circuit illustration and the following illustration of the idealized theoretical waveforms. Also, in order to more fully analyze the timing sequence, assume that the circuit under consideration is for a radar application wherein it is desirable to have the gate length contolled by the display circuit. **Thus, the radar** sweep circuit provides the turn-off trigger to return the multivibrator to its initial stable state.



Theoretical Waveforms for Basic FlipFlop Multivibrator

When voltage is first applied to the circuit, there is a slight conduction through both tubes. Because of the inherent imbalance of the circuit, however, one tube will conduct slightly more than the other. For example, if initially the current through V1 should be slightly greater than that through V2, the voltage drop across plate-load resistor R5 will be greater than the drop across plate-load resistor R6. This results in a lower plate voltage for V1, which is applied through resistor R3 to the grid of V2, thus causing the voltage at this grid to become more negative and reduce the current through V2. When the plate current through V2 is reduced, the current through plate-load resistor R6 likewise is reduced; therefore, the voltage drop across resistor R6 decreases, resulting in a rise in the plate voltage of V2. The positive-going plate voltage of V2 is applied through resistor R4 to the grid of V1, making this grid more positive. The regenerative action just described continues rapidly until V2 is cut off and VI is at maximum conduction. Thus, the circuit is in one of its two stable states of equilibrium, as represented by time interval a on the waveform illustration. Note that the output at the plate of V1 is at its most negative excursion (V1 is conducting) while the output at the plate of V2 is positive (V2 is cut off). Since there is no internal R-C time constant timing circuit to drive the nonconducting tube out of cutoff, the circuit remains in this stable condition until an input trigger pulse is applied.

Assume now that a negative trigger pulse of sufficient amplitude is applied simultaneously to both grids through input capacitors Cl and C2. This trigger pulse, which is the turn-on input trigger from the radar timing circuits, is applied at t as illustrated on the waveform diagram. Because V2 is already cut off, the input trigger has little effect on this tube; however, the same negative trigger pulse drives the grid of V1 below cutoff, causing this normally conducting tube to decrease conduction. As soon as V1 reduces conduction, its plate voltage rises toward the platesupply voltage,  $+E_{bb}$ . The positive-going signal at the plate of V1 is now coupled through resistor R3 and applied to the grid of V2, driving V2 into conduction. Thus, at instant  $t_1$  a switching action occurs; V2 now conducts heavily, as indicated by the waveform at its plate, and V1 is cutoff. The multivibrator remains in this condition, which is its second stable state as depicted by time interval b, until another trigger is applied.

When the desired gate duration is attained, the negative turn-off trigger from the radar sweep circuits is applied (at  $t_2$ ) and the gate is terminated. The negative-going turn-off trigger cuts off conduction of V2 and causes a switching action that returns the multivibrator to its original stable state, in which VI is conducting and V2 is cut off. The circuit remains in this condition (time interval c) until another negative trigger from the radar timing circuits is applied at  $t_3$ .

Close examination of the waveform illustration reveals that the length of the output gates is determined by the time interval between the turn-on and turn-off triggers. if the frequency of the turn-off trigger is made lower, the time interval between the triggers will increase; hence, the gate length will likewise increase. Conversely, the gate length will decrease if the turn-off trigger frequency is increased. Thus, the bistable multivibrator provides a positive or negative gate output in response to a timing (turn-on) input trigger pulse, with the gate being terminated by a turn-off trigger pulse. If a single constant-frequency trigger is used for both the turn-on and turn-off functions, the circuit will produce a symmetrical squarewave output having a frequency one-half that of the input-trigger frequency.

In the symmetrical-input bistable multivibrator being considered, positive input trigger pulses of sufficient amplitude can also be used to initiate the switching action between tubes V1 and V2. When the positive trigger pulse is applied simultaneously to the grids of the tubes, there will be no effect on the operation of the conducting tube. However, the plate current of the cut-off tube will be increased, causing its plate voltage to fall. The fall in plate voltage, when coupled to the grid of the conducting tube, drives this tube into cutoff.

Although it is true that either negative or positive input trigger pulses can cause the switching action to occur, triggering with negative pulses is preferred. For example, if the cut-off tube is biased with a high negative potential, a high-amplitude positive pulse is required to drive the tube into conduction, and only the most positive portion of the pulse has any effect. On the other hand, a low-amplitude negative pulse applied to the conducting tube immediately drives

this tube into cutoff, causing an instantaneous switching action.

#### Failure Analysis.

**No Output. The** input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the grid of V1 or V2 can be due to an open coupling capacitor, C 1 or C2, or to failure of the external input-trigger source.

Failure of the plate voltage supply, +E<sub>bb</sub>, will disrupt the operation of the circuit, as will an open cathode circuit. With tubes (or a single twin-triode tube) installed in the circuit, the filament and plate voltages should be measured, as well as the bias voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether plate-load resistor R5 or R6 and cathode-bias resistor R7 or R8 is open. If coupling resistor R3 or R4 is open there will be no feedback signal to cause the muhivibrator switching action. If bypass capacitor C3 or C4 is open feedback will still occur, but the interelectrode capacitance of the tube may cause undesirable effects on the wavefront of the feedback signal. An open output coupling capacitor, C6 or C7, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective tube; however, it can also be caused by a decrease in the applied plate voltage or an increase in the resistance of the associated plateload resistor, R5 or R6. A leaky or shorted output coupling capacitor, C6 or C7, will form a voltage divider with the input resistor of the following stage. If the input resistor of this following stage is returned to ground or to a negative supply, the voltage at the plate of both VI and V2 will be reduced, and the operation of the following stage will be upset by the change in voltage applied to its grid. Also, the additional current through plate-load resistor R5 or R6 may cause the resistor to burn out.

**Incorrect Frequency or Gate Width.** The basic flip-flop multivibrator has no components governing the frequency or width of its output-gate signal; these are both governed by the input triggers applied to the circuit. Therefore, any change in the output-gate frequency or width is a result of improper operation of the turn-on and/or turn-off trigger generating circuits.

# BASIC FLIP-FLOP MULTI VIBRATOR (SEMICONDUCTOR)

## Application.

The basic flip-flop multivibrator produces a square-or rectangular-wave output for use as gating or timing signals in radar sets. It is also used in switching-circuit applications, and for computer logic operations which include counting, shift-registers, clock pulses, and memory circuitry. This circuit is often used for relay-control functions, and for a variety of similar applications in radar and communications systems.

#### Characteristics,

Circuit assumes one of two stable states: one transistor normally conducts while the other transistor is cut off, and vice versa.

Requires two input triggers to complete one cycle of operation; the circuit assumes a stable state upon completion of each half-cycle of operation.

For a constant-frequency input, the output frequency is one-half that of the input trigger frequency.

Input trigger can be either positive or negative (positive trigger may be applied to base of conducting transistor, and negative trigger may be applied to base of cut-off transistor in common-emitter circuit configuration).

Symmetrical triggering occurs when the same trigger pulse is applied simultaneously; unsymmetrical triggering occurs when triggers are applied separately.

Symmetrical or unsymmetrical output gate depends on timing sequence of input trigger pulses; input triggers from different sources (turn-on and turn-off triggers) produce unsymmetrical output gate.

Collector-to-base feedback coupling is direct (through resistors), with bypass capacitors used to speed up switching from one stable state to the other.

Circuit can be made to assume the same initial stable state whenever voltages are applied by incorporating a definite imbalance within the circuit, or by using a manually controlled "reset" signal.

Output is taken from collector of either transistor in common-emitter circuit configuration.

Output impedance is low when transistor is in conducting (on) state; output impedance is approximately equal to collector load resistance when transistor is in cutoff (off) state.

# Circuit Analysis.

**General. The** basic flip-flop multivibrator is capable of producing a square- or rectangular-wave output pulse (gate) in response to two input triggers. This type of multivibrator has two stable (bistable) states – one transistor is normally conducting while the other transistor is normally held cut off – each one functions for only one-half cycle when triggered. Feedback from the collector of one transistor to the base of the other is direct through a coupling resistor bypassed by a capacitor. The capacity shunts the high-frequency components of the pulse from collector to base around the coupling resistor so that the rapid change taking place at one collector is coupled,

with minimum attenuation, to the base of the other transistor. Because two input triggers (turn-on and turn-off) are required to complete one cycle of operation, the output gate frequency of the flip-flop multivibrator is one-half the input trigger frequency. The output gate length is determined by the time interval between the turn-on and turn-off triggers. Output signals are taken from the collector of either or both transistors in the common emitter circuit configuration.

**Circuit Operation.** The accompanying circuit schematic illustrates two transistors in a basic flip-flop multivibrator circuit. Transistors Q1 and Q2 are



Basic Flip-Flop Multivibrator Using PNP Transistors

CHANGE 1

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identical PNP transistors used in a common-emitter circuit configuration; either junction or point-contact transistors may be used in this circuit. Resistors RI and R2 are the base-biasing resistors for Q1 and Q2, respectively. Resistor R3 provides the direct coupling from the collector of Q1 to the base of Q2, and resistor R4 provides the direct coupling from the collector of Q2 to the base of QI. Feedback resistors R3 and R4 are bypassed with capacitors C3 and C4, respectively; these capacitors permit faster switching action from one transistor to the other. Resistors R5 and R6 are the collector-load and output resistors for Q1 and Q2, respectively. Capacitors Cl and C2 are the input trigger coupling capacitors for Q1 and Q2, respectively; they provide unsymmetrical triggering. Capacitors C5 and C6 are the output-gate coupling capacitors for Q] and Q2, respectively. An output waveform can be taken from the collector element of either transistor, or output waveforms can be taken from the collector elements of both transistors simultaneously.

Fixed bias for the PNP transistors of this flip-flop multivibrator is obtained from two separate d-c voltage sources via voltage-divider networks. Resistors R1, R4, and R6 form one voltage divider between the positive d-c  $(+V_{BB})$  and negative d-c  $(-V_{cc})$  supply voltages. The resistor values are selected so that the voltage at the top of RI is negative with respect to the grounded P-type emitter of Q1; thus, the emitter of Q1 is forward biased with respect to the N-type base. Another voltage divider, consisting of resistors R2, R3, and R5 between the positive and negative supply voltages, forward biases the emitter of Q2 in the same manner. That is, the voltage at the top of R2 (at the N-type base of Q2) is negative with respect to the P-type emitter of Q2. Because of the voltagedivider action, the voltage at the collector of each transistor is more negative than the voltage at its base; thus, the collector-base junction of each PNP transistor is reverse biased.

When voltage is first applied to the circuit, the current which flows in each collector load resistor (R5 and R6) is determined by the effective resistance offered by transistors Q1 and Q2 for a given value of base-bias voltage. Although the multivibrator shown in the schematic appears to be a balanced circuit, and in spite of the use of close-tolerance components, there is always minor differences in internal resistance within the transistors. As a result of this inherent imbalance, the initial collector current (resulting from

the forward-bias conditions set up by the emitter-base junction resistances and bias resistors R1 and R2) for each transistor is different, and the immediate effect produced by regenerative action between the coupled stages is that one transistor conducts while the other is cut off.

For the purpose of this explanation, assume initially that more collector current flows through transistor QI than through transistor Q2; thus, as the collector current of Q1 increases, the negative voltage at the collector of Q1 decreases with respect to its emitter, or ground. Thus, the collector of Q1 becomes less negative and this, in effect, acts as a positive -going pulse, which is directly coupled through resistor R3 to the base of transistor Q2. The , · positive-going pulse at the base of Q2 makes the base positive with respect to the emitter (ground) and, as a result, Q2 is reverse-biased and approaches cutoff. The collector current of Q2 decreases because of the reverse-bias action between its base and emitter, and the voltage at the collector of Q2 increases, rising towards the value of the supply voltage. In other words, as the collector of Q2 becomes more negative a negative-going pulse is developed across R6, which is directly coupled through resistor R4 to the base of transistor Q1. The negative-going pulse at the base of Q1 makes the base negative with respect to its emitter (ground), and increase the forward bias on the base, causing the collector current of Q1 to further increase. This regenerative process continues until O1 is driven into saturation (as a result of the increased forward-bias), and Q2 is cut off (as a result of the increased reverse-bias). Thus, with the initial application of dc power, one transistor is turned on while the other is cut off, and each transistor is then held in this particular state of operation by the feedback from the other transistor until the off-trigger arrives.

For the following discussion of basic flip-flop multivibrator circuit operation, refer to the preceding  $\smile$  circuit schematic and the following illustration of the idealized theoretical waveforms. Assume that transistor Q1 has been initially turned on and is conducting heavily in a saturated state, while transistor Q2 remains cut off. Thus, the circuit is resting in one of its two stable states of equilibrium as discussed 'above. The initial turn-on period is represented by time interval *a* on the waveform illustration, while the steady state conducting condition of Q1 is represented by time interval b. Therefore, the output at the collector of Q1 is at its most positive excursion,

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while the output at the collector of **Q2** is at its most negative excursion (Q2 is cutoff). Since there is no internal time constant circuit provided to permit the nonconducting transistor to be automatically raised above cutoff (the fixed bias network ensures that it is held below cutoff), the circuit remains in this stable condition until a positive off-trigger is applied Q1.



Theoretical Waveforms for Basic Flip-Flop Multivibrator (Using PNP Transistors)

At time t<sub>2</sub>, the positive turn-off trigger is applied to terminal B, and the base of Q1 is instantaneously driven below cutoff. Collector current flow through Q1 reduces, and heavy collector current flow through Q2 develops a positive-going output voltage across R6, which is also applied through R4 and C4 to re-

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verse bias the base of Q1. This additonal reverse-bias quickly causes O1 collector current to cease, and the collector voltages rises quickly towards the supply value producing a negative-going output through C5. At the same time, this negative-going collector voltage is fed back through R3 and C3 to the base of Q2 as a forward bias. This continuous feedback action of reverse bias on Q1 and forward bias on Q2 continues until the collector voltage on Q2 bottoms, or saturation is reached. The circuit now rests in its second stable state, (during time interval c) with Q1 nonconducting while Q2 conducts heavily. The switching action is speeded up by capacitors C3 and C4 which allow the instantaneous changes to be immediately applied to the associated base element to produce the steep leading and trailing edges of the waveform. The circuit remains in this condition (time interval c) until another turn-on trigger of positive polarity is applied to terminal A.

At time t<sub>3</sub>, the positive turn-on trigger is applied to C2 and the base of Q2 which is forward biased and heavily conducting. The instantaneous positive bias produced by the input signal cancels the existing forward bias and reverse-biases Q2, stopping collector current flow. As the collector current of Q2 ceases, the collector voltage of Q2 rises towards that of the supply and produces a negative-going output signal. Meanwhile, this negative output voltage is also fed back to the base of Q1 through feedback resistor R4 which is bypassed by C4. The instantaneous negative swing through C4 quickly drives the base of QI in a forward-biased direction, and causes Q1 to conduct. As Q1 conducts, an output voltage of positive-going polarity is developed across R5, and is fed back through R3, bypassed by C3, to the base of Q2 driving it still further towards cutoff. Thus Q2 is held cut off, while Q1 once again conducts heavily near saturation. This is the starting condition and the other stable "operating point (time interval d on the waveform).

Close examination of the waveform illustration reveals that the length of the output gates is determined by the time interval between the turn-on and turn-off triggers. If the frequency of the turn-off trigger is made lower, the time interval between the triggers will increase; hence, the gate length will decrease if the turn-off trigger frequency is increased. Thus, the bistable multivibrator provides a positive or negative output gate in response to a timing input (tumon) trigger pulse, with the gate being terminated by a turn-off trigger pulse. If a single constant-frequency trigger is used for both the turn-on and turn-off functions, the circuit produces a symmetn" cal square wave output, with a frequency one-half that of the trigger frequency. A single pulse can be used for triggering because either the leading or the trailing edge of the trigger can be used. When conducting, and the leading edge is applied, a positive trigger operates to reverse bias the conducting transistor while the feedback causes the nonconducting transistor to be turned on. Conversely, if the trailing edge of the trigger pulse is applied to the nonconducting transistor, it produces a forward-biased condition and starts the transistor conducting, while feedback from the transistor produces a reverse bias to stop the first transistor from operating. This action is true as long as the trigger is a sharp pulse of short duration. If of long duration, an unsymmetrical output will be produced.

In the symmetrical-input bistable multivibrator under discussion, negative trigger pulses of sufficient amplitude can also be used to initiate the switching action between transistors Q1 and Q2. When the negative pulse is applied simultaneously to the base of the transistors, there will be no effect on the operation of the conducting tube. However, the collector current on the cut-off transistor will be increased, causing the collector voltage to decrease. The decrease in collector voltage when coupled to the grid of the nonconducting transistor drives this transistor into full conduction. In turn, feedback through this newly turned on transistor biases off the originally conducting transistor.

Although it is true that either negative or positive input trigger pulses can cause the switching action to occur, triggering with positive pulses is preferred. For example, if the cut-off transistor is biased with a highly positive potential, a high-amplitude negative pulse is required to drive it into conduction, and only the most negative portion of the pulse has any effect. On the other hand, a low amplitude positive pulse applied to the conducting transistor immediately drives this transistor into cutoff, causing a relatively instantaneous switching action.

#### Failure Analysis.

**No Output. The** input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit, and whether it is of the proper amplitude and polarity. Lack of an input trigger at the base of Q1 or Q2 can be due to an open coupling  $\_$  capacitor, C 1 or C2, or to failure of the external input-trigger source. If the input signal does not appear on the base side of the capacitor use an incircuit capacitance checker to check C 1 or C2 for proper capacitance or an open circuit.

Failure of the base bias or collector bias supply will disrupt operation of the circuit as would an open feedback circuit. Use a voltmeter to check the base bias, collector, and supply voltages. Normal voltage indications on these elements also indicates that neither RI nor R2 is open and, likewise, R3 and R4 also. If either C3 or C4 is opened, the circuit will still operate as a direct-coupled unit and operation will be – somewhat slowed up, but an output will still be obtained. If normal signals appear on the collectors but not at the output, coupling capacitor C5 or C6 is probably open. Use an in-circuit capacitance checker to verify the capacitance value and to check for an open or shorted condition.

**Reduced Output.** A reduction of output is usually caused by low collector voltage, improper bias, or defective transistor. A change in the resistance of the associated collector load resistor R5 or R6 will also affect the output amplitude. Check the resistance with an ohmmeter. A leaky or shorted output coupling capacitor, C5 or C6, will form a voltage divider with the input resistor of the following stage. If the input resistor of the following stage is returned to ground or to a bias supply, the collector voltage on either Q1 or Q2 will be changed and operation of the following stage will be upset by the change in voltage on its grid. In addition, this may possibly cause additional collector current flow through collector resistor R5 or R6 and may cause the resistor to burn out.

Incorrect Frequency or Gate Width. The 'basic flip-flop multivibrator has no parts governing the frequency or width of the output gate signal; these are both governed by the input triggers applied to the circuit. Therefore, any change in the output-gate frequency or width is a direct result of improper operation of the turn-on and/or turn-off trigger generating circuits.

# PENTODE FLIP-FLOP (ECCLES-JORDAN) MU LTIVIBRATOR

#### Application.

Same application as basic flip-flop (Eccles-Jordan) multivibrator (electron tube).

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#### Characteristics.

Same characteristics as basic flip-flop (Eccles-Jordan) multivibrator (electron tube), except it uses plate-to-supressor grid feedback coupling instead of plate-to-grid feedback coupling.

#### **Circuit Analysis.**

General. The pentode Eccles-Jordan (flip-flop) multivibrator is capable of producing a square- or rectangular-wave output pulse (gate) in response to two input triggers. The circuit has two stable (bistable) states - one tube is normally conducting while the other tube is normally held cutoff. Like the triode Eccles-Jordan multivibrator, discussed earlier in this Section of the Handbook, the circuit operation is controlled by the application of an input trigger pulse which causes the conduction to switch from one tube to the other. Thus, the multivibrator will function for only one-half cycle upon the application of each input trigger. Feedback from the plate of one tube to the suppressor grid of the other is direct through a coupling resistor bypassed with a capacitor, whose function is to reduce or eliminate the effects of tube interelectrode capacitance.

The **feedback** connection to the opposite suppressor gird, instead of the control grid, frees the control grid for application of the trigger pulses. Because two input triggers (turn-on and turn-off) are required to complete on cycle of operation, the output-gate frequency of the bistable multivibrator is one-half the input trigger frequency. The output gate length is determined by the time interval of the turn-off input triggers. Output signals can be taken from the plate of either or both electron tubes.

**Circuit Operation. The** accompanying circuit schematic illustrates two pentode electron tubes in an Eccles-Jordan bistable multivibrator configuration.





Electron tubes VI and V2 are identical sharp cutoff pentode-type tubes. Resistor **R1** is a common grid resistor for both tubes. Resistors R2 and R3 are the suppressor grid resistors for V1 and V2, respectively. Resistor R4 provides direct-coupled feedback from the plate of V1 to the suppressor grid of V2; resistor R5 provides direct-coupled feedback from the plate of V2 to the suppressor grid of VI. Feedback resistors R4 and R5 are bypassed with capacitors CI and C2, respectively. These capacitors permit faster

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switching action from one tube to the other by reducing the effect of tube interelectrode capacitances, Resistors R6 and R7 are the plate-load resistors for VI and V2, respectively; the screen grids are tied directly to the supply voltage, +Ebb. Suppressor grid voltage for V1 is obtained from a voltage divider consisting of resistors R2, R5, and R7; suppressor grid voltage for V2 is obtained from a voltage divider consisting of resistors R3, R4, and R6. Capacitors C4 and C5 are the output coupling capacitors for V1 and V2, respectively. Operating bias for this bistable multivibrator, which is cathode-biased, is obtained from a voltage divider consisting of common cathode resistor R8, bypassed with capacitor C3, and resistor R9. A comparison of the pentode and triode Eccles-Jordan multivibrator circuits reveals their similarities and differences.

Consider now the operation of the pentode Eccles-Jordan multivibrator by referring to the preceding circuit illustration. Since the output-gate waveforms of the pentode circuit are similar to those of the triode Eccles-Jordan multivibrator presented earlier in this Section of the Handbook, reference to the triode circuit waveforms can be made for this pentode circuit as well. The waveforms are reproduced in the following figure for convenience.



# Theoretical Waveforms for Pentode Eccles-Jordan (Flip Flop) Multivibrator

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When voltage is first applied to the circuit, there is a slight conduction through both tubes. However, because of the inherent imbalance of the circuit, one tube will conduct slightly more than the other. For example, if initially the current through V1 should be slightly greater than that through V2, the voltage drop across plate-load resistor R6 will be greater than the drop across plate-load resistor R7. This results in a lower plate voltage for VI, which is applied through resistor R4 to the suppressor grid of V2. The negative-going signal on the V2 suppressor grid reduces the plate current of this tube, thus reducing the current through plate-load resistor R7 and causing a voltage rise at the plate of V2. This positive-going voltage is coupled through resistor R5 to the suppressor grid of V1, further increasing the plate current of V1. Suppressor grid current flows at a slight positive suppressor grid voltage, but decreases at a high positive suppressor grid voltage, such as when the positive-going signal is applied from the plate of V2. The plate current of V1 increases further, and a regenerative action occurs instantaneously to drive VI into heavy conduction and V2 into cutoff. Thus, the multivibrator is in one of its stable states, as depicted during time interval  $\boldsymbol{a}$  in the waveform illustration referenced previously. Since there is no internal R-C time constant timing circuit to drive the nonconducting tube out of cutoff, the circuit remains in this stable state until a timing pulse is applied to the control grids to cause the switching action.

Assume now that a negative trigger pulse of sufficient amplitude is applied simultaneously to both control grids. The trigger pulse, applied at t 1, has little effect on the operation of V2 since this tube is already cut off. However, the same negative trigger drives the grid of VI below cutoff, causing this tube to reduce conduction. As soon as V1 reduces conduction, its plate voltage rises toward the plate supply voltage,  $+E_{bb}$ . The positive-going signal at the plate of VI is now coupled through resistor R4 and applied to the suppressor of V2 driving V2 into conduction. Thus, at instant t<sub>i</sub>a switching action occurs, with the result that V2 now becomes the conducting tube and V1 is cut off. Thus, the circuit is in the second of its two stable states, as depicted during time interval b. The multivibrator remains in the condition wherein V2 is conducting and VI is cut off until the next negative trigger pulse is applied to cause another switching action.

When the desired gate duration is attained, the negative turn-off trigger is applied (at  $t_2$ ) and the gate is terminated. The negative-going turn-off trigger cuts off conduction of V2 and causes a switching action that returns the multivibrator to its original stable state wherein VI is conducting and V2 is cut off. The circuit remains in this condition (time interval c) until another negative trigger from the timing circuits, the turn-cm trigger, is applied at  $t_3$ .

As in the triode Eccles-Jordan multivibrator, the length of the output gates of the pentode configuration is determined by the time interval between the turn-on and turn-off triggers. The gate length will increase if the turn-off trigger frequency is decreased; conversely, the gate length will decrease if the turnoff trigger frequency is increased. If a single constant frequency trigger is used for both the turn-on and turn-off functions, the circuit will produce a symmetrical square-wave output having a frequency one-half that of the input-trigger frequency.

Although positive trigger pulses could be used to "drive" the pentode Eccles-Jordan bistable multivibrator, negative trigger pulses are preferred; a smallamplitude negative pulse when applied to the conducting tube will immediately drive this tube into cutoff to cause an instantaneous switching action. The output of the multivibrator is taken from either or both plate circuits through an output coupling capacitor (C4 or C5). A cathode follower should be used couple the positive gate output to a circuit that requires grid current, since the multivibrator may occasionally fail.

#### Failure Analysis.

**No Output. The** input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the grid of V1 or V2 can be due to failure of the external input-trigger source or to the coupling from the trigger source to the multivibrator.

Failure of the supply-voltage source,  $+E_{bb}$ , will disrupt the operation of the circuit, as will an open cathode circuit. With tubes installed in the circuit, the **filament**, plate, screen grid, and suppressor grid voltages should be measured, as well as the bias voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether any of the respective electrode resistors are

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open (resistors R2 through R9). If coupling resistor R4 or R5 is open, there will be no feedback signal to affect the multivibrator switching action; in addition, the dc operating **potential** from the associated sup pressor grid will be removed. If bypass capacitor Cl or C2 is open, feedback will still occur, but the interelectrode capacitance of the tube may cause undesirable effects on the wave front of the feedback signal. An open output coupling capacitor, C6 or C7, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective tube; however, it can also be caused by a decrease in the applied voltage or an increase in the resistance of the associated plate-load resistor, R6 or R7. A leaky or shorted output coupling capacitor, C4 or C5, will form a voltage divider with the input resistor of the following stage. If the input resistor of this following stage is returned to ground or to a negative supply, the voltage at the plate, screen grid, and suppressor grid of both V1 and V2 will be reduced, and the operation of the following stage applied to its grid. Also, the additional current through the resistors associated with the electrodes mentioned previously may cause the resistors to burn out.

Incorrect **Frequency and Gate Width.** The pentode **Eccles-Jordan** (flipflop) multivibrator has no components governing the frequency or width of its output-gate signals; these are both governed by the input triggers applied to the circuit. Therefore, any change in the output-gate frequency or width is a result of improper operation of the turn-on and-or turn-off trigger generating circuits.

# DIRECT COUPLED (OR BINARY) MU LTIVIBRATOR (SEMICONDUCTOR)

#### Application.

**The** direct-coupled (or binary) multivibrator produces a square or rectangular output waveform primarily for use in computer circuit and switching operations such as computer logic, counting and shift register operations, clock pulse generation and memory circuit. Because of its simplicity is also serves a variety of similar applications in radar and electronic equip ments.

# Characteristics.

Usually employs self bias.

Provides two outputs (one is the inverse of the other).

Requires a turn-off or reset trigger to change state. Requires a minimum number of parts.

Operates at low levels (10-15 millivolt input con. trols 200-300 millivolt output).

## Circuit Analysis.

General. The dc coupled or binary (count-by-two circuit) multivibrator offers design simplicity and a minimum of parts which leads to its frequent use in logic circuitry. It is basically, a bistable multivibrator with two states of stable operation. In the on-state, one transistor continuously conducts while the other remains cut off. In the off-state, the previously conducting transistor is cut off and the previously nonconducting transistor is switched on. The change of state is accomplished only by a separate trigger. There is no R-C timing network to permit automatic charge or discharge to control the switching rate. Design is usually such that the conducting transistor operates in a saturated condition. Thus the base voltage is higher than the emitter and the collector voltages, and all element voltages are low in value with only a fraction of a volt difference between them. Consequently, the conducting transistor has a low value of dissipation, and the output is also low. As a result, the dc multivibrator usually requires a stage of external amplification if other transistors are to be driven by it. When operated as a saturated flipflop it requires a higher turn-off power than that of the nonsaturating type (discussed later in this section of the Handbook). Since no emitter resistors are used, the circuit is somewhat sensitive to temperature changes. above 60 degrees Centigrade.

**Circuit Operation.** The following schematic illustrates a basic dc flip-flop. Note that only two resistors (R1 and R2) are used, which serve both as collector resistors and as feedback resistors, and

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across which the output is developed. For simplicity,

the control trigger circuitry is not shown.

**Basic PNP Direct-Coupled (Binary) Flip Flop** 

Initially a forward bias is applied to both transistors by connecting the base of Q1 and Q2 to R2, and Rl, respectively (the negative supply voltage through the resistor places a forward negative bias on the transistor). In the absence of a trigger pulse both transistors tend to conduct. However, the first one to establish a flow of collector current produces a positive-going collector swing which is applied to bias the opposite transistor below cutoff. Because of the inherent slight difference in base resistance between similar transistors, one transistor will always conduct more heavily than the other. Assume for the sake of discussion that Q1 is conducting and Q2 is driven to cutoff. Since this circuit operates at collector saturation, a heavy current flows from the supply through resistor Rl, and transistor QI to ground. The flow of i as shown on the schematic produces a positive voltage drop across R1. This positive-going voltage is fed back directly to the base of Q2 as a reverse bias which immediately stops conduction through Q2. The heavy flow of i drops the collector voltage of Q1 to almost zero (it is saturated). Meanwhile, since Q2 stops conducting its collector voltage rises to nearly the full negative supply value. Since the base of Q1 is connected to the collector end of R2, this negative-going feedback voltage is applied to the base of Q1 as a large forward bias. The base voltage on Q1 is now higher than that of the collector, and since the emit-

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ter is grounded and effectively at zero potential, the

base voltage is rdso higher than the emitter. Thus the base voltage is the dominating voltage which holds Q1 conducting until a turn-off trigger arrives. The circuit

is now operating between intervals tl and t2 as shown

on the following waveform illustration.

At time  $t_2$  the turn-off trigger arrives, and a negative input pulse is applied via input 2. Consequently, the negative input on the base drives Q2 in a forward direction (the small saturation voltage fed from the collector of Q1 is easily overcome by the negative input pulse), and Q2 conducts. Immediately, current flow through R2 causes a positive swinging voltage to be applied to the base of Q1, stopping conduction through R1. As conduction ceases through R1 the collector voltage of **Q1** rises towards the full negative supply value, and feeds back an increasing negative voltage to the base of Q2. Thus, Q2 is quickly switched into conduction while Q1 is turned-off. At time T<sub>2</sub> the second stable state is accomplished, and now the circuit awaits another turn-off trigger at time t<sub>3</sub>. This is merely a repeat of the sequence of operation at time t<sub>1</sub>. Namely, a negative trigger is applied to input 1 which drives the base of Q1 in a forward direction, causes collector current flow through R1 and feeds back a positive-going voltage to the base of Q2 causing it to stop conducting. Instantaneously, the collector voltage of Q2 rises towards the negative supply value, and drives the base of Q1 into heavy conduction. The circuit is now resting in the initial state, with Q1 conducting heavily and Q2 cut off.

The circuit schematic of a practical binary multivibrator is shown in the following illustration, with control circuitry. Except for the operation of transistors Q3 and Q4, circuit operation is identical and corresponding parts are labelled identically so that the previous discussion applies.



**Typical PNP Binary Multivibrator** 

Transistor Q3 and Q4 merely act as switches, when a negative trigger is applied to their base they conduct, and when no trigger is present they are held nonconducting. The control transistor connected to the conducting multivibrator transistor is held at cutoff by the low saturation voltage of the collector to which it is connected, while the other is held cutoff

by the high reverse bias at the non-conducting collector. Since their emitters are comected directly to ground, when triggered, they develop a shut-off pluse which stops the conducting transistor from operating and causes the switching. For example, assume Ql heavily conducting, with its base held negative by the feedback from R2. Q4 is resting reverse biased awaiting the control trigger. When the negative control trigger (input 2) arrives, the base of Q4 is driven negative and this forward bias causes the transistor to conduct through R2. Flow of collector current in Q4 develops a positive swinging pulse across R2 and drives the base of Q1 positive to cutoff. Thus Q1 is stopped from conducting. Transistor Q3 operates similarly, assuming Q2 conducting and Q1 cut off, the negative input to Q3 (input 1) causes collector conduction and produces a positive pulse across RI, thereby driving Q2 base positive to cutoff, and switching Q1 into conduction by the feedback developed as the collector of Q2 rises towards the negative supply at cutoff.

## Failure Analysis.

Partial or No Output. A no-output condition can only be caused by a lack of bias voltage because of a blown fuse or defect in the supply, or because both transistors Q1 and Q2 or load resistors R] and R2 are defective. If either Q1 or Q2 is operable and either R1 or R2 is not open, a single unstitched output will be obtained, since the circuit has two states of operation. First check the supply voltage with a high resistance voltmeter to ascertain that a blown fuse or defective power supply is not at fault. Then check the collector voltage to ground. Transistors Q1 and Q3 will show either a high negative voltage or practically zero voltage depending on whether or not Q1 is conducting, while Q2 and Q4 will produce exactly the opposite indication under normal operation. If both Q1 and Q2 indicate either a low voltage or a high voltage, one or both of the transistors is at fault. Use an in circuit transistor checker to locate the defective one. In the absence of a transistor checker use an ohmmeter, and check the forward and reverse resistance of the emitter and collector junctions with the bias removed. The forward resistance should be considerably lower than the reverse resistance. Replace any defective transistors with known good ones. Since control transistors Q3 and Q4 shunt the multivibrator transistors, if defective, the output will also be shunted to ground. If inoperative, there will still be a single output and the stage will not change state.

If they are simultaneously shorted, there will be no output and both Q1 and Q2 collector voltage will be almost zero. If only one is shorted there still will remain a single output which cannot be switched by application of an input trigger.

**Reduced Output.** A reduced output is usually caused by low collector voltage, improper bias, or a defective transistor. Any change in the resistance of collector load resistors RI or R2 will also affect the output amplitude. Use a high resistance voltmeter to check the supply and collector voltages, and measure the resistance of R1 and R2 with an ohmmeter. If the voltages are normal and both R1 and R2 are of proper value the transistors must be at fault. Check the beta of both transistors with an in-circuit checker to determine which has a loss of gain, or use an oscilloscope to locate the low output waveform and associated transistor.

**Incorrect Frequency or Gate Width. The** directcoupled multivibrator has no parts governing the internal frequency or width of the output gate signal; these are solely controlled by the input triggers applied to the circuit. Therefore, any change in output gate frequency or width can only be a direct result of improper operation of the turn-on or turnoff trigger generating circuits, not the multivibrator.

# SQUARING MU LTIVIBRATOR (SEMICONDUCTOR)

#### Application.

The squaring multivibrator, also known as the Schmitt trigger or emitter-coupled bistable multivibrator, is primarily used to supply a square or rectangular output when triggered by a sine-wave, sawtooth, or other irregularly shaped waveforms.

## Characteristics.

May be self or fixed biased.

Has two stable (bistable) states of operation (one transistor conducts while the other is cut off, and vice versa).

Provides a symmetrical output gate regardless of input waveform.

Collector to base feedback provides one switching path, while common emitter coupling feedback provides the other switching path. Use common emitter configuration.

#### Circuit Analysis.

**General. The** Schmitt circuit differs from the conventional bistable multivibrator circuit in that one of the coupling (feedback) networks is replaced by a common emitter resistor (the equivalent of cathode coupling in the electron tube). The additional regenerative feedback developed by the common emitter-feedback coupling arrangement provides quicker action and straighter leading and trailing edges on the out put waveform than in other mr.dtivibrators. Because of the relatively instantaneous switching action of this arrangement, the waveform of the input trigger has no effect on the output so that essentially square-wave output signals are rdways produced.

**Circuit Operation. The** schematic of a typical Schmitt type squaring circuit is shown in the following illustration.



**PNP Squaring Multivibrator** 

Transistor Q2 is the initially conducting transistor, which is supplied with forward base bias by resistor network R2, R3, and R5 connected as a voltage divider between the negative voltage supply and ground. Capacitor  $C_{cc}$  and base resistor RI form a conventional R-C input coupling circuit. Resistor R4 is the feedback (coupling) resistor which is common

## **ELECTRONIC CIRCUITS**

to both emitters, and R6 is the collector resistor of Q2 across which the output waveform is developed. Capacitor **£3** bypasses feedback resistor R3 to help speed up switching action.

Initially, transistor Q2 conducts heavily because of the large forward bias supplied by the voltage divider consisting of collector resistor R2, feedback resistor R3, and base resistor R5, series-connected between the negative supply and ground. A reverse collector bias is applied Q1 through R2, and a reverse ernitterbias is developed across the common emitter resistor R4 by Q2 current flow. Base current flow through R1 is rdso in a direction which produces a reverse base on Ql, so that Q1 cannot conduct until triggered. Thus, Q1 remains cutoff, while Q2 conducts. With Q2 conducting, a positive-going output voltage is developed across collector resistor R6 which lowers the effective collector voltage of Q2 to almost zero. No output coupling capacitor is shown since the circuit may be direct coupled to the following driver stage, if desired.

Assume now a sine-wave input signal is applied to c<sub>cc</sub>. During the positive half-cycle of operation the positive input voltage applied across R1 keeps Q1 reverse-biased so that it cannot conduct. Since in this condition the output is developing a positive signal similar to that through initial conduction, as explained previously, it is evident that the input and output are in phase. When the input signal swings negative during the opposite half-cycle of operation, a negative voltage appears across R1 as Ccc discharges. The case of Q1 is thereby driven negative and forward biased, starting collector current flow through R2. The direction of electron flow is such that the collector end of R2 becomes positive (as marked on the schematic), and this instantaneous positive swing is coupled through Cl to the base of Q2, appearing as a positive reverse bias which instantly stops current flow through Q2. The reduction of collector current flow through R6 produces a voltage of opposite polarity to that shown on the schematic, that is a

negative output voltage, as the collector of Q2 rises towards the supply voltage (time  $t_1$  to  $t_2$  on the following waveform illustration).



#### Typical Input and Output Waveforms

Although R3 connects the collector of Q1 to the base of Q2, and any voltage appearing on the collector of Q1 will also eventually appear on Q2 base, a speed up of this action is obtained by bypassing R3 with capacitor C1. Thus, the high frequency components of the collector signal are not slowed up by the resistance of R3 so that switching action is faster than without Cl.

Consider now the effect of the common coupling resistor (R4) in the emitter circuit. Initially the heavy current through Q2 produced a negative drop across R4, as marked on the schematic. This negative emitter bias which is degenerative, because no bypass capacitor is employed, also tends to prevent Q2 current flow. However, the base bias of Q2 is much larger and the degenerative emitter voltage produced across R4 has little effect on Q2 collector current flow. However, Q1 is already at cutoff, and this additional negative emitter bias ensures that it remains so until sufficient base input is applied (on the next half-cycle) to overcome this reverse bias.

With the collector current flow of Q2 reducing, the degenerative voltage developed across R4 also reduces, which is the same as applying an increasing positive voltage between emitter and ground. Thus, while the base of Q1 is driven in a forward-biased direction by the input signal, a regenerative feedback is developed in the emitter circuit by the reduction of Q2 current flow. Consequently, transistor Q1 is quickly driven into heavy conduction near saturation. The resulting instantaneous positive swing developed across R2 is instantly applied through Cl to the base of Q2, and quickly drives Q2 to cutoff. The circuit now rests in its second stable state (interval t  $_{1}$  to  $t_{2}$ ) until another trigger arrives to drive Q2 into conduction and cut off QI.

When the input signal again swings in a positive direction (time interval  $t_2$ ), the positive voltage appearing across R1 causes a reverse bias to be applied Q1 base and reduce collector current flow through R2; this produces a negative swinging voltage across R2, which is applied to the base of Q2 through capacitor Cl. The negative swing forward-biases Q2 and starts it conducting, and develops a positive-going voltage swing across R6 to provide an in-phase output voltage. Simultaneously, the increased negative emitter (reverse) bias developed across feedback resistor R4 further stops conduction in Q1. This regenerative feedback action quickly drives Q2 to collector saturation and Q1 to cutoff, whereupon the rising negative collector voltage of Q1 applied to the base of Q2 through Cl and ,R3 holds Q2 strongly conducting despite the degenerative emitter voltage developed across R4 (time interval  $t_1$  to  $t_3$ ). This is the initial order of conduction and the transistor awaits the next trigger (at time  $t_3$ ) to turn off Q2 and turn on OI. Because of the extreme regenerative action of the emitter-coupled circuit, once started, the switching action is quickly accomplished, and the shape of the input trigger has no effect in determining the output waveform. Cutoff and turn-on is sharp and the sides of the waveform are steep. The width of the output waveform like the other bistable multivibrators is controlled by the difference in time between the off and on pulses. When symmetrical and equal a true square wave is produced.

#### Failure Analysis.

Constant or No Output. Lack of supply voltage, an open common emitter resistor, or defective transistors are about the only three items which can cause a no output condition, since at least one steady output can always be obtained if any voltage is present. Check the supply voltage with a high resistance voltmeter to make certain that a blown fuse or defective supply are not at fault. Since R4 connects both transistors to ground and they are reverse collector biased, no conduction will occur if R4 is open, and a steady negative output will be obtained. A zero emitter to ground voltage reading will indicate that R4 should be replaced. If a steady positive, or near zero but constant voltage is obtained, O1 is probably defective. On the other hand if Q2 is shorted the same indication would occur. Likewise, if Q2 is open a steady negative output voltage would be obtained through R6. It is evident that it is rather difficult because of the feedback and direct connections in this type of circuit to obtain a specific indication which conclusively points to only one cause of trouble. Therefore, a simple voltage check plus a resistance analysis of the few parts involved should quickly locate the defective component. If the voltage and resistance are correct but an unswitchable steady output is still obtained, check that an input trigger is being received on both sides of coupling capacitor Ccc, using an oscilloscope.

**Reduced Output.** A reduced output can occur because of low supply voltages, improper bias voltage, or defective transistors. Check the supply and bias voltage with a high resistance voltmeter. Use an incircuit transistor checker, or check for a low forwardresistance and a high reverseresistance with an ohmmeter.

**Incorrect Pulse Width or Frequency. Like** the other bistable multivibrators, an effect on frequency or pulse width is controlled by the time difference between the on- and off-triggers. Thus any faulty operation of this type is due solely to defects in the trigger generating circuits and not the multivibrator.

# SATURATING MU LTIVIBRATOR (SEMICONDUCTOR)

#### Application.

The saturating multivibrator is used to supply **a** rectangular gate, or trigger, in radar and control applications, and irr the logic switching circuits of computers and similar devices.

#### Characteristics.

Usually uses fixed bias.

Provides two outputs simultaneously, one the inverse of the other. Requires a turn-on or turn-off trigger to change state.

Has two (bistable) stable states (one transistor conducts while the other remains cut off and vice versa).

Output power is considerable lower than that of the nonsaturating type.

Operating speed is slower than the non-saturating multivibrator.

#### Circuit Analysis.

General. In the saturating multivibrator, the emitter and collector voltages are lower than the base voltage and there is only a few tenths of a volt difference between them. Consequently, it takes more driving power in this saturating circuit, as compared with the nonsaturating circuit, to drive the stage out of saturation (a larger trigger is required). The output voltage is also less. Thus, while a certain amount of stability may be imparted by saturated operation the gain and speed suffer. The gain is limited by the low saturation voltages, and the speed by the amount of time required to obtain hold dispersion (the extremely heavy saturation current injects extra holes in the base, which require a finite recovery time to remove them). As a result, the saturated circuit is used where its simplicity makes it more economically feasible than the non-saturating type.

**Circuit Operation.** The schematic of a typical saturated multivibrator is shown in the accompanying illustration.





Fixed bias is applied by a voltage divider arrangement, consisting of RI, R3, and R6 for transistor Q2, and R2, R4, and R5 for Q1, connected between the negative supply and ground. Feedback resistors R3 and R4 are bypassed by capacitors Cl and C2, respectively, to speed up response. An output is taken from each collector, and the input trigger is applied across emitter resistor R7, which is common to both transistors. This circuit arrangement is that of the conventional bistable multivibrator arranged for common emitter triggering.

In the quiescent condition, with no trigger applied, both transistors conduct immediately when the supply voltage is applied, since they are both forward biased through voltage dividers to the negative sup ply. Although the circuit is symmetrical, that is, the collector, feedback, and base resistors are all of equal values to minimize any unbalance, there still exists a slight difference in base resistance between transistors of the same types. Thus, one transistor always tends to conduct more heavily than does its counterpart, and through feedback from the collector to the opposite base drives the associated transistor to cutoff, and itself to full conduction. Assume for the sake of discussion the normally-on transistor is Ql, while Q2 is the normally-off transistor. From time t. to  $t_i$  (as shown on the following waveform illustration) the initial conduction is established as previously explained, so that a time  $t_1$  transistor QI is conducting while Q2 is cutoff. Since the turn-off input trigger at this time is stopping Q2 there is no effect and the circuit rests in its initially-on state until time  $t_2$ .



Typical Waveforms

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During the interval from  $t_1$  to  $t_2$  a continuous positive (reverse) bias exists at the base of Q2 due to base current flow from ground through R6, producing a voltage drop of the polarity shown on the schematic (this current is actually produced by reverse collector current  $I_{cc0}$ ). Thus, with reverse base bias and a reverse collector bias, O2 remains cut off until the next turn-on trigger arrives. Since no collector current flows through R2 the collector of Q2 rises towards the value of the negative supply voltage and drives Q1 base in a forward-biased direction, causing heavy conduction through Q1. The heavy collector current drops the voltage across R1 to almost zero, and a positive-going output is produced at A, while a negative output from Q2 is produced at terminal B. Once saturated, the collector voltage of Q1 is less than the base voltage fed back from Q2. With high current but low voltage, the power dissipation of the transistor is well within ratings (one advantage of saturated operation is the low collector dissipation involved). They heavy emitter current flow through the common, emitter-coupling resistor R7 places a large degenerative voltage on the emitter of Q2 which effectively reverse-biases Q2. Thus Q2 is held in its off-state, regardless of whether or not the off period is long enough for Cl to discharge. The only effect on operation that Cl has is that of speeding up the switching operation by shunting the high frequency transients around R3 to help speed up turn-on, or turn-off, switching action.

When the negative trigger is applied at t, the emitter of Q1 is driven negative, which is the same as driving the base **positive** to reverse bias the transistor. Since transistor Q2 is already reverse-biased, this trigger has no effect on Q2, only on Q1. Consequently, the collector and emitter current of Q1 is reduced. This reduction of collector current produces a negative-swinging voltage across collect resistor R1, and through Cl to the base of Q2. The instantaneous negative swing applied to the base of Q2 drives Q2 in a forward-biased direction, and causes collector current flow through collector resistor R2. The voltage drop across R2 produced by the increasing collector current reduces the collector voltage, effectively producing a positive-swinging voltage at the collector, which is fed back through capacitor C2 to the base of Q1. The positive-swinging voltage drives the base of Q1 instantaneously in a reverse-biased direction and causes a further drop in collector current. The

regenerative feedback action continues smoothly and quickly until Q2 is driven into collector saturation (collector voltage bottoms), while QI is cut off. While this regenerative feedback and switching action occurs, a degenerative voltage is developed across common resistor R7 in the emitter circuits of both transistors. Although this degenerative emitter voltage normally is of such polarity as to oppose the increase of current, it is not of as great an amplitude as the feedback voltage developed across R5 which is driving Q1 to cutoff, or the feedback voltage developed across R1 which is driving Q2 into conduction. It does, however, aid in obtaining collector current cut off on Q1 since the transistor is already being driven in that direction, and eventually reaching saturation. Because the heavy collector saturation current of Q1 produces extra holes in the base of Q1, transistor Q1 does not stop conduction immediately when its base voltage is driven positive and base current flow is stopped. But instead, the collector current continues to flow for a finite interval, even though there is no forward bias on Ql, until the holes are removed from the base of O1 and cut-off prevails. With no collector current flow, the collector of Q1 rises in a negative direction towards the full supply voltage, and a negative output is produced at terminal A. Meanwhile, as O2 conducts heavily saturated, the collector current is ahnost zero, and a positive output voltage is produced at terminal B by the voltage drop across collector resistor R2 of Q2. Conditions are now exactly opposite the original state and Q2 rests in the on-state (interval  $t_2$  to  $t_3$ ), while Q1 rests in the cutoff state awaiting a negative turn-on trigger at time t<sub>3</sub>.

When the turn-on trigger arrives at time t3, the emitter of QI and Q2 is driven negative. Since Q1 is already in a non-conducting state the trigger cannot further stop conduction so it has no effect on the operation of Q1. However, the trigger does drive Q2 in a reverse-biased direction (a negative emitter trigger has the same effect as a positive base trigger), and causes a reduction of collector current flow through R12. Immediately a negative-swinging voltage is developed across R2 and applied through Cl to the base of Q1, which drives Q1 in a forward direction towards saturation. The increasing collector current flow through RI, again produces a positive-swinging collector voltage which is applied through Cl to the base of Q2, further driving Q2 in a reverse biased direction and further reducing collector current flow. This regenerative switching action is smooth, continuous and relatively fast so that except for a slight delay caused by hole storage, as explained previously for the opposite condition of conduction in Q1, the switching is considered to be almost instantaneous. When Q1 reaches saturation and Q2 is completely cutoff, minimize hole storage time and produce speedy operation, even as high as 20 MHz. Thus, the tendency is to use saturated circuity generally for its simplicity and economy. Non-saturated circuits are usually only used when output power requirements call for more power than can be produced with saturated circuits.

## Failure Analysis.

**General.** When making voltage checks use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

Partial or Steady Output. Failure of one half of the circuit to operate will produce a partial output in the form of a steady single polarity output. Failure of the supply voltage, or emitter resistor R7, are about the only two possibilities of obtaining no output at all. Because of the feedback connections it becomes rather difficult to isolate the trouble by symptom along. It is quicker to make a voltage check and determine if the supply voltage is present, and that no fuse or power supply is at fault. Then use an ohmmeter to the stage again rests in the original conducting state awaiting a turn-on trigger for Q2 to change operation (interval t3 to t4). Meanwhile, a positive output is developed across R2 and applied output terminal B, while a negative output is developed across RI and applied to terminal A.

Practically all the non-clamped multivibrators are of the saturated type, since clamping the waveform to operate within the normal operating region of the transistor when use as an amplifier is necessary. As long as the base drive is allowed to draw collector current until the transistor collector voltage bottoms, saturation will always occur. Therefore a produce the unchanging steady current represented by the flat top of the output pulse there must be no further change of collector current. In the simple multivibrator this is achieved by collector current saturation, and in the
# **ELECTRONIC CI RCUITS**

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more complicated types of multivibrators by clamp ing diodes. At the time transistors were first discovered and applied to this type of circuit, hole storage time effects caused a serious limitation in the **speed** of operation at which practical multivibrators could be made to operate. At the present state of the art, however, special switching transistors have been developed which check for continuity and proper resistance values to locate the defective part.

If either collector resistor R1 or R2 is open, no collector voltage will appear on the associated transistor, Q1 or Q2, respectively, and the bias voltage divider will be open. Therefore, the other transistor will be effectively cutoff biased by the floating base, and the normal reverse collector bias. With no conduction, a single negative output will be produced while the other output will be zero due to the open collector circuit. In the event emitter resistor R7 which is common to both transistors opens, there will be no flow of current through either transistor, but a negative output will appear at both output terminals since the transistors will, in effect, operate as if both were biased to cutoff. Thus, both collector voltages will rise to the full value of the supply. Therefore, if either transistor fails, or both fail, a negatime output will be produced.

Normal voltage indications on the base and collector elements of the transistors usually indicates that any associated series resistors have continuity and proper value. However, it is just as easy to check the **resistance** of each resistor with an ohmmeter because of the few parts involved, Since it is important to check that the proper polarity and amplitude of input trigger exists and that it is present, use an oscilloscope to observe the waveforms. When the waveforms are improper or missing it locates the general area of the trouble, which must then be further localized by voltage and resistance checks.

**Reduced Output.** A reduced output is usually caused by low collector voltage, improper bias, or a defective transistor. A change in the associated collector load resistor, R1 or R2, will also affect the output amplitude. Use an oscilloscope to observe the waveforms and determine where the reduced amplitude exists. Then check for proper bias and collector voltage in that portion of the circuit, and make certain that the collector resistance is normal. If normal voltages are present and the collector resistance is within tolerance, and a low output amplitude still exists, it must be because of reduced transistor current.

**Incorrect Frequency or Gate Width.** Since the multi-vibrator has no parts which govern the frequency or width of the output signal, these are both governed by the input triggers' applied to the circuit. Hence, any change in these parameters must be the direct result of improper operation of the turn-on or turn-off trigger generating circuits.

# NONSATURATING MU LTIVIBRATOR (SEMI-CONDUCTOR)

# Application.

The nonsaturating multivibrator is used to supply a rectangular gate or trigger in radar and control equipments, and in the logic switching circuits of computers and similar devices. Particularly where a large power output is required.

#### Characteristics.

Usually uses fixed bias.

Provides two simultaneous outputs, one is the inverse of the other.

Requires a turn-on or a turn-off trigger to change state.

Has two stable operating states (bistable).

Output frequency is one-half that of the trigger frequency.

Output power is greater than that of the saturating type.

Operating speed is faster than the saturating multivibrator.

Uses clamping diodes to prevent saturation effects.

#### Circuit Analysis.

**General.** The nonsaturating multivibrator uses clamping diodes to stop collector saturation, and steering diodes to make certain the proper trigger is received, thus avoiding false triggering. In the circuit discussed below breakdown diodes are also used to prevent forward biasing of the collector which would cause saturation. Consequently, the transistors operate in the normal operating region (over the linear portion of their transfer curve). Basically the circuit is that of a conventional emitter-coupled bistable multivibrator, with the steering, clamping, and breakdown diodes added.

**Circuit Operation.** The schematic of a typical nonsaturating multivibrator is shown in the accompanying illustration.

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NPN Nonsaturating Multivibrator

Resistors R1 and R2 are the collector resistors of Q1 and Q2, respectively. The collector to base feedback networks are C2 and R5, and C4 and R6, with the common coupling-emitter resistor R8, bypassed by C5 to prevent degeneration. Resistors R7 and R9 are the base return resistors. The clamping diodes are CR1 and CR2 which shunt R3 and R4. Diodes CR3 and CR'4 are the respective steering diodes of Q1 and Q2. Breakdown diodes CR5 and CR6 are saturation limiters which prevent the collector voltage of Q1 and O2 from being forward biased when conducting. Input triggering pulses are injected at input terminal I (connected for parallel triggering), while terminals A and B are the output terminals from which the square wave output is taken. Transistor Q2 is considered to be the normally-on transistor, while Q1 is normallyoff. When the negative input trigger is applied to the

base of Q2, these conditions are reversed and Q2 is turned off, while Q1 is turned on. When the next negative trigger is applied to the base of Q1, the circuit reverts back to the initial state of operation, with Q1 off, and Q2 on.

In the absence of an input signal, both transistors initially conduct. Although the multivibrator circuit is symmetrical (corresponding resistors have the same value), there is always a slight difference in collector resistivity between transistors of the same type, so that one transistor will conduct more heavily than the other. In turn, the heavier-conducting transistor produces a feedback voltage which cuts off the lightconducting transistor. Assume for the sake of discussion that Q1 is initially in the off-condition while Q2 is in the on-condition.

In the quiescent condition, then, Q1 is effectively at cutoff, or at its lowest limit of conduction held by a negative, reverse-bias feedback voltage from the collector of Q2 via R-C network R5, C2 (NPN transistors require a negative bias voltage for cutoff). With no collector current flowing through RI, the collector of Q1 is at a high positive voltage near the supply value (reverse-biased collector), and both steering diode CR3 and clamping diode CR1 are held in a reverse-biased condition. At the same time, the negative feedback voltage produced by collector current flow through R2, and applies through C2 and R5 holds breakdown diode CR5 in a forward-biased condition but cuts off the base of Q1. In a similar manner, the emitter bias developed across R8 and C5 holds the emitter-base junction of Q1 in a reversebiased condition preventing conduction. Meanwhile, a positive feedback voltage from the collector of Q1 is applied via C4 and R6 to the base of Q2 through breakdown diode CR6. Because of the high reverse voltage (collector of Q1 is near supply level), breakdown diode CR6 conducts in a reverse direction and maintains a constant forward bias on O2, which causes heavy current flow but not collector saturation. The heavy collector current flow through collector resistor R2 develops a negative-going voltage which is applied to terminal B as an output, simultaneously with the positive output from terminal A. As Q2 collector current increases, the voltage drop across R2 increases also, the collector voltage of Q2 reduces becoming less positive. Since steering diode CR4 is connected to the collector of Q2 through R4, when the collector voltage drops lower than the positive feedback voltage developed across RI (which is L

applied through R6 to the anode of diode CR4) the diode becomes forward-biased and conducts, and as the collector voltage drops further CR2 eventually conducts. The collector of Q2 is now connected through the two diodes to the cathode of breakdown diode CR6 and the junction of R6. As long as the breakdown diode maintains a constant potential between the base and collector of Q2, the collector voltage cannot fall lower than the base voltage. Therefore, the collector cannot be forward biased and saturation cannot occur. Although the collector current may still increase if additional base current drive is supplied, the collector potential remains constant at the freed minimum value. The operating range of Q2 (and later Ql) then, is from the minimum value of collector voltage to almost the full supply voltage at cutoff. The stage is now in its initial conducting or on-state with O2 conducting and O1 off, and rests in this condition until a turn-off trigger is received.



#### **Multivibrator Waveforms**

At time  $t_1$  in the preceding waveform illustration, a negative trigger is applied to steering diode CR4, but since it is already conducting the trigger has

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no effect and the stage rests in the initially-on condition (interval  $t_1$  to  $t_2$ ). At time  $t_2$ , the next negative trigger is applied through Cl to the cathode of diode CR3 and simultaneously to CR4 via C3. Since Q1 is nonconducting and the base is already negative, no effect is felt on Q1. However, when the negative pulse passes through CR4 and CR6 and appears on the base of Q2 it instantly partially reverse-biases the conducting transistor and causes a reduction in O2 collector current flow through R2. As the collector current decreases, the drop across R2 is reduced and collector voltage becomes more positive. This positive-going voltage is applied as feedback through C2 and R5, causing breakdown diode CR5 to conduct in a reverse direction, and driving the base of Q1 in a forwardbiased direction. Collector current now flows through R1 and produces a negative-going voltage which is applied through feedback network C4 and R6 to the base of Q2 through breakdown diode CR6. Thus Q2 is driven further in a reverse-biased direction, and a larger turn-on voltage is fed back again to the base of Q1 by the increasing collector current flow through RI. The regenerative feedback continues smoothly and rapidly until Q1 is fully conducting while Q2 is turned-off. The circuit now rests in its second stable state (interval t, to t,) until triggered off again at time t<sub>a</sub>. When Q1 conducts, diodes CR3 and CR] are activated similarly to diodes CR2 and CR4 in the discussion of Q2 operation, so that CR5, CR3, and CR1 continue to conduct, while a negative output pulse is produced at terminal A. With Q2 held at cutoff by feedback from Q1, a positive square-wave output pulse is obtained at terminal B as the collector voltage of O2 rises toward the full supply vrdue. In this instance, the emitter bias developed across R8 by conduction of Q1 keeps Q2 emitter reverse-biased, while breakdown diode CR5 maintains a constant difference in potential between the base and collector of Q1. Thus, while additional current may be drawn through Q1 if the base current drive increases, the collector voltage remains steady at its minimum clamped potential. If additional current is required, it is supplied through the shunt diode circuit from the cut-off side of the circuit via R2, and R5. Since any additional base current supplied at this time would cause only.. a- small increase of collector current this shunting action will not appreciably reduce the output voltage developed across R2. But what is more important, is that additional collector current through R1 cannot occur and drop the collector of

Q1 to zero and cause saturation. At time  $t_4$ , the next negative trigger is applied through Cl, and CR3, and CR5, to the base of Q1, reducing the flow of collector current because of the reverse bias it applies subsequently, the previously discussed cycle of feedback through C4 and R6 occurs, driving the base of Q2 into conduction, and produces additional feedback through C2 and R5 to drive the base of Q1 in the off-direction. Thus time  $t_4$  corresponds to the initial trigger at  $t_1$  which was previously considered ineffective, since Q2 was already assumed to be turned on.

When a positive trigger pulse is applied through Cl or C3, it reverse-biases the steering diodes and cannot reach a triggering point in the circuit. After the pulse ceases, the positive charge on the capacitor is quickly discharged through either CR1 or CR2. Any similar effect produced by the trailing edge of a negative trigger is also eliminated in this fashion providing a fast recovery time. Diodes CR7 and resistor RIO, shown in dotted lines in the schematic, are trigger shaping devices to allow speedy triggering, they are not necessarily a part of the multivibrator. Resistor R1O is used to slow up any positive trigger so that false triggering cannot occur. Diode CR7 acts as a gate for negative triggers and shunts them around R1O to avoid any attenuation, while forcing any positive excursions to travel through R1O. Feedback capacitors C2 and C4 function only to pass the high frequency component of the switching transients from collector to base without attenuation. Thus the switching action is speeded up, and the output waveform has steep leading and trailing edges rather than sloping sides produced by slow switching action.

Although clamping and steering diodes provide improved operation, it is possible to design nonsaturating multivibrators using the standard saturated multivibrator circuit with different values of component parts. In this case, parts values are chosen so that saturation does not occur. It is also of interest to note that, while the saturated circuits use heavy currents at very low voltages the dissipation is less than that involved in the nonsaturating circuit, which uses near-saturation currents at higher voltages with a consequent increase in average collector dissipation. Therefore, the nonsaturating circuit usually requires transistors with higher ratings. Failure Analysis.

**General. While** making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges. Be careful also to observe the proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junction will cause a false low-resistance reading.

Partial or No Output. It is necessary that the proper polarity and amplitude trigger be applied before the circuit will switch from one state to another. However, it will rest in one stable state and produce a single output if unable to respond to a trigger, or if disabled. Use an oscilloscope to determine that the proper trigger is applied, and then check the element voltages to determine if the circuit is otherwise normal. Check the supply voltage first to make certain the fault is not in a blown fuse or defective power supply. With the normal voltages present and a proper trigger at the input, if switching will not occur check steering diodes CR3 and CR4 to see if they pass the pulse. If not, replace the defective diode with a known good one. Should emitter resistor R8 which is common to both Q1 and Q2 open, neither will function but a dual positive output will be obtained from terminals A and B since they will rise to the full value of the supply voltage. Failure of breakdown diodes CR5 and CR6 will allow saturation to occur, but will not prevent obtaining an output. When the collector voltage is found to be lower than the base voltage the associated breakdown diode is inoperative and should be replaced with one known to be good.

Low Output. Low collector voltage, improper bias, failure of the breakdown diodes, or the transistors themselves can cause a low output. If emitter bypass capacitor C5 is open, degeneration will cause a reduction of output. Use an in-circuit capacitance checker for this test. A change in the associated collector load resistors, R1 or R2, will also effect the output amplitude. Use an oscilloscope to observe the output waveform and determine where the reduced amplitude exists. Then check for the proper bias and collector voltage in that portion of the circuit. If normal voltage is present and the collector resistor is within tolerance, but low output amplitude still exists it must be caused by reduced collector current.

**Incorrect Frequency or Gate Width.** Since the multivibrator has no parts which govern the frequency or width of the output signal, these are both governed by the input triggers applied to the circuit. Hence, any change in these parameters must be the direct result of improper operation of the turn-on or turn-on or turn-off trigger generating circuits.

# RELAY CONTROL MU LTIVIBRATOR (SEMICONDUCTOR)

#### Application

The relay control multivibrator is used in computers and electronic switching circuits to control a relay or similar electromechanical device where the ratio of the on-off currents is 10 or more.

# Characteristics.

Usually uses fixed bias.

Requires a turn-on and a turn-off trigger to change state.

Has two stable states (bistable).

Operates at a frequency of one half the trigger pulse frequency.

Is a saturating type of multivibrator.

Uses steering diodes for stability.

Inductive kickback from the relay coil is prevented by a diode clipper.

Operating speed is limited by the relay operating speed.

# **Circuit Analysis.**

**General.** In the relay control multivibrator, one transistor is used to operate the relay, with a pull-in to drop-out current ratio of approximately 15 to 1. A rectangular output is simultaneously obtained from the other transistor; a positive output is obtained with the relay closed, and a negative output with the relay open. Steering diodes are provided to prevent false triggering and a protective diode is placed across the relay operating coil to prevent inductive operating transients from affecting the transistor to which the relay is connected.

**Circuit Operation.** The schematic of a typical relay control multivibrator is shown in the following illustration. As can be seen from the schematic, relay K1 is operated by transistor Q1, while Q2 provides a rectangular output voltage. The negative input trigger is applied through attenuating resistors R9 or R10

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and capacitors C3 or C4 to turn off the conducting transistor. Resistor R4 is the collector resistor for Q2, while the relay coil of K1 functions similarly for Q1. The feedback network for Q1 consists of C2 and R3, while Q2 is held in conduction by a voltage divider arrangement of R1 and R2 together with bias resistor R7. Diode CR2 prevents the collector voltage swing of Q1 across relay coil K1 from supplying the feedback to operate Q2. Resistors R6 and R7 are the base bias resistors. Note that fixed bias is supplied from a separate base bias source, and that two different collector supplies are used, with that of Q1 (Vcc<sub>1</sub>) being the lowest.



NPN Ralay Control Multivibrator

Normally, transistor Q2 is the conducting transistor while Q] is cut off. Initially both transistors will conduct, but with bias voltage divider R1, R2, and R7 connected between the high positive voltage of  $V_{CC_2}$  and negative base bias supply Vbb, a positive (forward) bias exists on Q2 base. Therefore, Q2 conducts heavily and develops a negative-going voltage

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across collector resistor R4, which is fed back through C2 and R3 to the base of QI, driving it into cutoff. As the voltage across K1 coil rises to the supply value of Vcc<sub>1</sub>, diode CR2 is reverse biased and prevents any feedback from the collector of Q1 to the base of Q2. The negative feedback voltage on Q1 base holds NPN transistor Q1 is a non-conducting condition with only a small reverse-collector current flow through K1 relay coil. At this time, any voltage drop across K1 places a positive bias on protective diode CRI to keep it reverse-biased and nonconducting. As long as the cathode of diode CR2 remains at the positive level of  $Vcc_1$ , and as long as the voltage drop across RI keeps the anode lower than the cathode voltage, CR2 also remains in a nonconducting condition.

When a negative trigger is applied to the reset input terminal through R10 and C4, the base of Q2 is momentarily driven negative by the conduction of steering diode CR4, and causes Q2 to stop conducting. Thus, as the forward bias on Q2 is reduced by the input trigger, the collector current voltage drop across R4 reduces (becomes positive-going).

The feedback of the positive-swinging collector voltage through C2 and R3 to the base of Q1 produces a forward bias which causes Q1 collector current to increase. The flow of Q] collector current through the relay coil of K1 is of a polarity which keeps CR] reverse-biased. CR2 also remains reverse biased, until the collector potential of Q1 drops below the anode potential applied through R1 and R2. As Q2 collector current decreases and Q1 collector current increases the base of QI is further driven towards saturation by the feedback from R4. Eventually, relay K1 pulls in, and transistor QI is in saturation, while transistor Q2 is cut off. At this time a positive voltage is developed at the output terminal of Q2 as the collector voltage of Q2 rises to the supply value of VCC<sub>2</sub>. At saturation the collector voltage of Q1 is less than the base voltage (only a few tenths of a volt) and CR2 is forward-biased. Electron current flow from ground through Q1 and CR2 to R1, and voltage supply VCC<sub>2</sub> produces a negative reverse bias voltage which is fed back through R2 to Q2 base to hold Q2 in a nonconducting state. This is the second stable state, with Q1 on and Q2 off.

When a negative trigger is applied through R9 and C3 from the set-input of Q1, sterring diode CR3 temporarily conducts and produces a momentary reverse bias on the base of Q1, causing Q1 collector current

to reduce. The reducing collector current allows the voltage on the cathode of CR2 to rise in a positive direction towards supply voltage Vcc, and eventually reverse-biases the diode. The positive voltage fed back to the base of Q2 through R1 and R2 now causes Q2 to again conduct. Thus Q2 quickly reaches the initial stable conducting state with QI cut off by the negative feedback through C2 and R3. When the collector current flowing through relay coil of K1 is reduced to zero, the inductive field about the coil collapses and causes CR1 to momentarily conduct when a negative trasient appears on the cathode. The negative inductive kick is thereby effectively clipped off, protecting Q1 from the inductive surge voltage.

Steering diodes CR3 and CR4 will now' allow a positive trigger pulse to appear on the base of either Q1 or Q2, thus false triggering is prevented. Resistors R9 and R1O are not always required, in fact, they are really not a part of the multivibrator. They are used to provide a high impedance input instead of the approximate 300 ohm impedance offered by the coupling capacitors alone. These resistors also prolong the discharge time of the trigger, ensuring that the switching action occurs before the trigger is removed. With the steering diode cathodes connected back to their associated collector through R5 and R8, the conducting transistor maintains the diode in an almost forward biased condition (in saturation the collector is almost the same value as the base voltage – within tenths of a volt). Thus the large trigger pulse instantly turns the diode on and triggers the conducting transistor off. If a negative trigger pulse was accidentally applied to the nonconducting transistor, the large collector to base reverse bias would prevent the diode from being forward biased, and the trigger would be ineffective.

Since the output voltage is in-phase with the closing of the relay it may be used to signal the position of the relay or to trigger an associated circuit. The prime purpose of this multivibrator circuit, however, is to control the relay. Since the relay is a mechanical device, it operates at slower speeds than the electronic circuit; thus the relay operating speed determines the maximum switching speed.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges. Be careful to observe proper polarity when

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checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output or Partial Output. Total loss of output could only result from lack of supply voltage, since an output will be produced even if both transistors are inoperative. Although the relay will not operate if Q1 is defective or has a defective circuit part, a positive voltage equal to the VCC, supply will still be obtained from Q2, if inoperative, or a negative output if operable. Use an oscilloscope to determine that the proper input trigger exists and passes through the correct steering diode (an open diode can prevent triggering). Then measure the supply voltage and check the collector voltage on both transistors. With the correct collector bias supply voltage and base bias voltage present, the collector of the conducting transistor should measure very low (a few tenths of a volt), while the cut off transistor will have a high collector voltage almost the same as that of the supply voltage. If both collector voltages are low, either relay coil K1 or collector resistor R4 is open, or the transistor(s) are shorted. Check the resistance of R4 and K1 coil.

Where an output is obtained but no switching occurs, in addition to defective steering diodes, either R9, R1O, C3 or C4 can be open. Hence the necessity to use the oscilloscope to determine if the input trigger appears at the transistor base terminal. The circuit will operate without feedback capacitors Cl and C2 but will be somewhat slowed down, and will most probably cause sloping leading and trailing edges on the output waveform at high switching speeds.

**Erratic Operation. Since** the circuit is controlled by an external trigger it is important to observe the trigger with an oscilloscope to be certain that the trigger itself is not erratic. If the **trigger** appears normal in shape and amplitude, check operation of the steering diodes and the resistance of R5 and R8. If the resistance of R5 or R8 increases with age, or they become open, the biasing of the steering diodes and the discharge **time** of R9, C3 or R1O, C4 will be changed. Such condition might also be caused by defective transistors. Check the resistors with an ohmmeter, and the diodes and transistors with an incircuit checker, if possible.

**Incorrect Frequency or Gate Width.** Since the multivibrator has no parts which govern the frequency or width of the output signal, these are both governed by the input triggers applied to the circuit. Hence, any change in these parameters must be the direct result of improper operation of the turn-on or turnoff trigger generating circuits.

Low Output. Low collector voltage, improper bias, or defective transistors can cause a low output voltage. A change in collector resistor R4 will also affect the output amplitude. Use an oscilloscope to check the output wavefrom and determine where the reduced amplitude exists. Then check for the proper bias and collector voltages in that portion of the circuit. If normal voltages are present and the collector resistor is within tolerance, but low output amplitude still exists, it can only be because of reduced collector current.

### PART 7-3. MONOSTABLE

#### MONOSTABLE (ONE-SHOT) MULTI VIBRATORS

#### General.

The term monostable multivibrator refers to one class of multivibrator or relaxation oscillator circuits that function in a stable condition until the application of a trigger pulse. At this time the circuit switches rapidly and goes through one complete cycle of operation, after which it reverts to its original stable condition, in which it remains until the application of another trigger pulse. The monostable (or one-shot) multivibrator is essentially a two-stage resistance-capacitance-coupled amplifier, and not an oscillator in the strict sense of the word, with one stage normally cut off and the other stage normally conducting. The one shot multivibrator operates in much the same manner as the free-running, or astable, type discussed earlier in this Section of the Handbook, except that this circuit requires an input trigger to initiate the multivibrator action and produce the output signal.

The monostable multivibrator produces a squareor rectangular-wave output pulse, more commonly called a "gate", having fast rise and fall times and extreme flatness on top; the pulse is produced only in response to an input trigger. The output frequency is determined by the frequency of the input trigger, and the duration of the gate length is determined by the circuit design. The one-shot multivibrator can be used at pulse-repetition rates from zero to maximum which is determined by the gate length and the R-C time constant of the circuit. A nominal range of gate time duration is from 30 to 2500 microseconds,

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which will accommodate trigger pulses in the range of 200 to 2000 pps.

In applications requirng different gate lengths, the gatedeterrnining components can be switched in value to produce the desired gate length. Also, the monostable multivibrator may supply both positive and negative gates to as many as four branches. A precaution is that the positive-gate output should not be applied to a circuit requiring grid current as the multivibrator may occasionally fail; the use of a cathode follower or buffer circuit will eliminate this disadvantage. Because the monostable multivibrator is not well suited for controlling the gate length with a turn-off trigger pulse, a bistable multivibrator should be used when this type of control is desired.

Although the output from the monostable multivibrator is sometimes differentiated to provide a pulse either at the leading edge or the trailing edge of the gate waveform, in most cases only the leading edge of the waveform must be extremely fast; the trailing edge is usually not used for critical timing applications. A negative-going leading edge is used whenever possible since such a gate can be obtained rather easily from any tube electrode except the cathode. In addition, a negative gate at the plate of a multivibrator tube will always be generated at a lower impedance than a positive gate at the same plate.

# **TRIODE PLATE-TO-G RIO-COUPLED** MONOSTABLE MU LTIVIBRATOR

# Application.

The triode plate-to-grid-coupled monostable multivibrator produces a square-wave or rectangular-wave output for use as gating or timing signals.

#### Characteristics.

Circuit assumes a stable state in which one tube normally conducts and the other tube is normally cut off.

Requires an input trigger to cause circuit operation; circuit returns to stable state upon completion of one cycle of operation.

Input trigger can be either negative or positive; negative trigger affects tube that is normally conducting, and positive trigger affects tube that is normally cut off.

Produces square-wave or rectangular-wave output gates for both positive and negative polarity in response to an input trigger.

Output gate length is determined by R-C time constant in grid circuit and by the applied voltage; output frequency is determined by input trigger frequency.

# **Circuit Analysis.**

General. The triode plate-to-grid-coupled monostable multi vibrator is a two-stage resistancecapacitance-coupled amplifier capable of producing a square-wave or rectangular-wave output pulse (gate) in response to an input trigger The monostable multivibrator has only one stable state, in which one tube normally conducts while the other tube is normally cut off, and will function for only one complete cycle upon the application of the input trigger. To achieve the stable condition, the grid of the normally conducting tube is usually returned to B+, while the grid of the tube that is normally cut off is returned to ground or to a negative voltage source. Feedback from the plate of one tube to grid of the opposite tube is through R-C coupling. Because the monostable multivibrator operates for only one cycle in response to an input-trigger pulse, the output frequency of this circuit is dependent upon the input trigger frequency; the output gate length is determined by the R-C time constant of the plate-to-grid feedback network and the applied voltage. Output signals can be taken from the plate of either or both electron tubes.

Circuit Operation. The following circuit schematic illustrates two triode electron tubes in a plate-to-grid-coupled monostable multivibrator configuration. Electron tubes V1 and V2 are identicaltype triode tubes; although the accompanying schematic illustrates two separate triodes, a twintriode is frequently used in this circuit. Capacitor Cl provides coupling from the plate of V2 to the grid of V1, and capacitor C2 provides coupling from the plate of V1 to the grid of V2. Resistor R1 returns the grid of V1 to the negative voltage (bias) supply, -Ecc, and resistor R2 returns the grid of V2 to the positive voltage supply, +Ebb. Resistors R3 and R4 are the plate-load resistors for V1 and V2, respectively. Capacitors C3 and C4 are the output coupling capacitors for V1 and V2, respectively. The tube that

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is normally cut off is VI, and the tube that is normally conducting is V2.



Triode Plate-to-Grid-Coupled Monostable Multivibrator

The following simplified schematic diagram illustrates the charge and discharge paths for feedback capacitor C2. The cutoff time of V2 is determined by the discharge of capacitor C2 through resistor R2 toward the positive voltage supply, +Ebb. Although the conduction resistance of V1 is included in the discharge path of C2, it is small as compared with the resistance of R2, and can therefore be neglected. The cutoff time of VI is determined by the period of the input trigger pulse. If the R2-C2 time constant is made exactly one-half the period of the trigger pulse, the multivibrator produces a symmetrical square-wave output; if the R2-C2 time constant is made longer or shorter than one-half the trigger pulse period, an asymmetrical rectangular-wave output is produced.



Charge and Discharge Paths for Capacitor C2

Consider now the operation of the triode plate-togrid-coupled monostable multivibrator by referring to the preceding circuit illustrations and the following illustration to the idealized theoretical waveforms. When voltage is first applied, V2 goes into conduction and VI cuts off. This action results from the fact that the grid of V2 is returned through resistor R2 to a positive voltage, while the grid of V1 is returned through resistor R1 to a negative voltage. Thus, at time t. (start of time interval a) on the waveform illustration, the grid voltage of V2  $(eg_2)$  is slightly positive, causing conduction through V2, and a decrease in its plate voltage (ep<sub>2</sub>). The negativegoing voltage at the plate of V2 is coupled through capacitor Cl to the grid of V1, thus aiding in cutting off this tube (waveform eg1). Also, at to, coupling capacitor C2 charges through the low cathode-to-grid internal resistance of V2 (approximately 1K) and the V1 plate-load resistor, R3. The voltage at the plate of

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VI is represented by the **ep1** waveform. At to, **then**, the plate-to-grid-coupled monostable multivibrator assumes its stable state, in which V2 normally conducts and V1 is normally cut off; the circuit remains in this condition until a trigger pulse is applied.



# Theoretical Waveforms for Triode Plata-to-Grid Coupled Monosteble Multivibrator

Assume now that a negative trigger pulse of sufficient amplitude to cut off the tube is applied directly to the grid of V2. The effect of this trigger pulse ( $e_{in}$ , applied at  $t_1$ ) is to drive V2 into cutoff. As a result of the decreased conduction through V2, the **plate** voltage of v2 (ep<sub>2</sub>) rises toward the **supply** voltage, and the positive-going signal is coupled through capacitor Cl to the grid of V1, thus raising the grid voltage (eg<sub>1</sub>) above cutoff and driving V1 into conduction. The plate voltage of V1 (ep<sub>1</sub>) decreases, and the negative-going signal is coupled through capacitor C2 to the grid of V2 to drive V2 further into cutoff. Thus, at **t**<sub>1</sub> a switching action

occurs and the multivibrator is in a "temporary" stable state in which V1 conducts and V2 is cutoff.

During this temporary stable state (time interval b), capacitor C2 discharges through resistor R2 toward the potential of the positive voltage supply. This causes the grid voltage of V2 (eg<sub>2</sub>) O to rise toward the potential of the positive voltage supply until the point is reached where the grid voltage of V2 can no longer hold the tube cut off. At that instant,  $t_2$ , V2 once again conducts and the negative-going signal at its plate is coupled through capacitor Cl to the grid of VI which again cuts off V1. The voltage waveform at the plate of V1 (ep<sub>1</sub>) is rounded off, and the waveform at the grid of V2  $(eg_2)$  has a small positive spike of the same time duration as a result of the charging of coupling capacitor C2 when V2 again conducts. The plate voltage waveform of V2 (ep<sub>2</sub>) has a small negative spike at the same time duration as the positive spike on the V2 grid voltage waveform  $(eg_2)$ . Hence, at t<sub>2</sub>, the multivibrator reverts to its original stable condition, in which V2 conducts and V1 is cut off; the circuit remains in this condition (time interval c) until another negative trigger pulse is applied at  $t_3$ .

Close examination of the waveforms reveals that the monostable multivibrator goes through one complete cycle of operation for each input trigger pulse. Also, the time of application of the trigger pulse determines when V1 is driven into conduction, and the R-C time constant of R2-C2 and the applied voltage determines when V2 is driven into conduction. Thus, the monostable multivibrator output frequency is determined by the input trigger frequency, and the output gate width is determined by the discharging of capacitor C2 through resistor R2 toward the potential of the positive voltage supply.

A negative trigger pulse applied to the grid of the normally conducting tube, as was done in this case, is not the only method by which the multivibrator circuit can be **triggered**. A negative trigger pulse applied directly to the plate of VI and coupled through capacitor C2 to the grid of V2 serves the same purpose. A positive trigger pr.dse applied directly to the plate of V2 or to the grid of V1 will also trigger the circuit. In some practical-circuit applications, a positive trigger is applied to the grid of a "trigger-inverter" stage whose plate is comected in parallel with the plate of VI; the inverted trigger is then coupled through capacitor C2 to the grid of V2 as a negative trigger pulse. In any event, a cycle of

multivibrator operation is initiated by diving the normally conducting tube into cutoff, or by driving the tube that is normally cut off into conduction.

# Failure Analysis.

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**No Output. The** input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the grid of V2 can be due to failure of the externrd input-trigger source.

Failure of the positive voltage supply, +Ebb, will disrupt the operation of the circuit, as will an open cathode circuit. With tubes (or a single twin-triode tube) installed in the circuit, the filament and plate voltages should be measured, as well as the grid bias voltage, to determine whether the applied voltages are within tolerance and whether plate-load resistor R3 or R4 or grid-bias resistor R1 or R2 is open. If coupling capacitor Cl or C2 opens, there will be no feedback signal to effect the multivibrator switching action. An open output coupling capacitor, C3 or C4, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective tube; however, it can also be caused by a decrease in the applied plate voltage or an increase in the resistance of the associated plate-load resistor, R3 or R4. A leaky or shorted output coupling capacitor, C3 or C4, will form a voltage divider with the input resistor of the following stage. In this input resistor is returned to ground or to a negative voltage supply, the voltage at the plate of both VI and V2 will be reduced, and the operation of the following stage will be upset by the change in voltage applied to its grid. Also, the additional current through plate-load resistor R3 or R4 may cause the resistor to bum out.

**Incorrect Frequency or Gate Width.** The plate-togrid-coupled monostable multivibrator has no components governing the frequency of its output-gate signal; this frequency is governed by the input trigger applied to the circuit. Therefore, any change in the output-gate frequency is a result of improper operation of the trigger generating circuits. A change in the output-gate width, however, will result if there is a change in the value of either resistor R2, capacitor C2, or the applied voltage. A change in the resistance or capacitance of the R2-C2 timing control circuit will have the greatest effect on the gate width; changes in the applied voltage will affect the gate width to a lesser **degree**.

# TRIODE COMMON-CATHODE-RESISTOR-COUPLED MONOSTABLE MULTI VIBRATOR

#### Application.

The triode common-cathode-resistor-coupled monostable multivibrator produces a square-wave or rectangular-wave output for use as gating or timing signals.

# Characteristics.

Circuit assumes a stable state, in which one tube normally conducts and the other tube is normally cut off.

Requires an input trigger to cause circuit operation; circuit returns to stable state upon completion of one cycle of operation.

Input trigger can be either negative or positive; negative trigger affects tube that is normally conducting, and positive trigger affects tube that is normally cut off.

Produces square-wave or rectangular-wave output gates of both positive and negative polarity in response to an input trigger.

Output gate length is determined by R-C time constant in grid circuit and by the applied voltage; output frequency is determined by input trigger frequency.

#### Circuit Analysis.

General. The triode common-cathode-resistorcoupled monostable multivibrator is functionally similar to the Triode Plate-to-Grid-Coupled Monostable Multivibrator discussed previously in this Section of the Handbook. The circuit has only one stable state, in which one tube normally conducts while the other tube is normally cut off, and will function for only one complete cycle upon the application of an input trigger pulse. To achieve the stable condition, the grid of the normally conducting tube is usually returned to its cathode or to B+ while the grid of the tube that is normally cut off is returned to ground or to a negative voltage (bias) supply. R-C coupling is provided from the plate of V1 to the grid of V2, but the coupling from V2 to V1 is effected across a common cathode resistor. Because the monostable multivibrator operates for only one

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cycle in response to an input trigger pulse, the output frequency of this circuit is dependent upon the input trigger time constant of the grid circuit and by the applied voltage. Output signals can be taken from the plate of either or both electron tubes.

Circuit Operation. The following circuit schematic illustrates two triode electron tubes in a common-cathode-resistor-coupled monostable multivibrator configuration. Electron tubes VI and V2 are identical-type triode tubes; although the accompanying schematic illustrates two separate triodes, a twin-triode is frequently used in this circuit. Capacitor Cl is the input coupling capacitor for application of a positive trigger to the grid of VI. Capacitor C2 provides coupling from the plate of V1 to the grid of V2. Resistor R1 returns the grid of V1 to ground, and resistor R2 returns the grid of V2 to the common cathode connection. Resistors R3 and R4 are the plate-load resistors for V1 and V2, respectively. Resistor R5 is the common cathode bias and coupling resistor for coupling from V2 to V1. Capacitors C3 and C4 are the output coupling capacitors for V1 and V2, respectively. The tube that is normally cut off is V1, and the tube that is normally conducting is V2.





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The following simplified schematic diagram illustrates the charge and discharge paths for capacitor C2. The cut-off time of V2 is determined by the discharge of capacitor C2 through resistor R2. Although the conduction resistance of VI is included in the discharge path of C2, it is frequency; the output gate length is determined by the R-C small as compared with the resistance of R2, and can therefore be neglected. The cutoff time of V1 is determined by the period of the input trigger pulse. If the R2-C2 time constant is made exactly one-half the period of the trigger pulse, the multivibrator produces a symmetrical square-wave output; if the R2-C2 time constant is made longer or shorter than one-half the trigger pulse period, an asymmetrical rectangularwave output is produced.



Charga and Dischargs Paths for Capacitor C2

Consider now the operation of the triode common-cathode-resistor-coupled monostable multivibrator by referring to the preceding circuit illustrations and the following illustration of the idealized theoretical waveforms. When voltage is first applied, V2 goes into conduction and VI cuts off. This action results from the fact that the grid of V2 is returned through resistor R2 to the cathode, initially placing this grid at the same potential as the cathode, and thus allowing V2 to conduct heavily. The plate current flow of V2 through common cathode resistor R5 makes the voltage at the top of the resistor positive with respect to ground, producing a bias voltage of sufficient amplitude to hold V1 cut off (since its grid is returned to ground through resistor RI), and still permit V2 to conduct. Thus, at time t. (start of time interval a) on the waveform illustration, the grid voltage of V2 (eg<sub>2</sub>) is slightly positive, causing conduction through V2; as a result, the plate voltage (ep<sub>2</sub>) of V2 decreases because of plate current flow through plate-load resistor R4. Also, as a result of V2 plate current, there is a positive voltage (ek) developed across common cathode resistor R5, which provides the bias to cut off VI. The positive-going voltage at the plate of VI (ep<sub>1</sub>) is coupled through capacitor C2 to the grid of V2, driving the grid further positive. Also, at to, coupling capacitor C2 charges through the low cathode-to-grid internal resistance of V2 (approximately 1 K) and the plate-Ioad resistor, R3, of V1. At to, then the commoncathode-resistor-coupled monostable multivibrator assumes its stable state, in which V2 normally conducts and V1 is normally cut off; the circuit remains in this condition until a trigger pulse is applied.





Assume now that a positive trigger pulse of sufficient amplitude to cause the tube to conduct is applied to the grid of V1 through coupling capacitor Cl. The effect of this trigger pulse  $(e_{in}, applied at t_i)$ is to drive V1 into conduction, thus causing an increase in current through V1 and a decrease in the plate voltage  $(ep_1)$  of VI. This negative-going voltage is applied instantaneously through capacitor C2 to the grid of V2, driving the grid voltage of V2  $(eg_2)$ below cutoff. When the V2 plate current ceases, the voltage drop (ek) across cathode resistor R5 decreases to the level where it decreases the bias on VI, permitting this tube to conduct more heavily. Thus, at t<sub>1</sub>, a switching action occurs and the multivibrator is in a "temporary" stable state, in which V1 conducts and V2 is cut off.

During this temporary stable state (time interval b), capacitor C2 begins to discharge, causing the grid voltage of V2 (eg<sub>2</sub>) to become less negative. The discharge path of C2 is downward through grid resistor R2 and then upward through the low cathode-toplate conduction resistance of V1. At this time VI alone is conducting; its plate current is limited by its own cathode bias, which is not sufficient to cut off VI. As the voltage  $(eg_2)$  on the grid of V2 becomes less negative, because of the discharging of capacitor C2, it soon reaches the point, at t<sub>a</sub>, where is is no longer of sufficient amplitude to hold V2 in cutoff. Consequently, V2 once again conducts, and the flow of V2 plate current through common cathode resistor R5 increases the voltage drop (ek) across this resistor, again increasing the bias of VI and reducing the flow of plate current through V1. As the conduction through VI decreases, the plate voltage (ep<sub>1</sub>) of VI rises toward the potential of the positive voltage, supply, +Ebb. The positive-going signal at the plate of VI is coupled through capacitor C2 to the grid of V2, driving this grid positive (waveform  $e_{2}$ , at  $t_{2}$ ). Thus, capacitor C2 stops discharging and again begins charging. The voltage waveform at the grid of V2 (eg<sub>2</sub>) has a' small positive spike of the same time duration, as a result of the charging of coupling capacitor C2 when V2 again conducts. The plate voltage waveform of V2 (ep<sub>2</sub>) has a small negative spike, and the voltage waveform across common cathode resistor R5 (ek) has a small positive spike of the same time duration as the positive spike on the V2 grid voltage waveform (eg<sub>2</sub>). Hence, at t<sub>2</sub>, the multivibrator reverts to its original stable condition in which V2 conducts and VI is cut off; the circuit remains in this condition (time interval c) until another positive trigger pulse is applied at t<sub>3</sub>.

Close examination of the waveforms reveals that the monostable multivibrator goes through one complete cycle of operation for each input trigger pulse. Also, the time of application of the trigger pulse determines when V1 is driven into conduction, and the R-C time constant of R2-C2 and the applied voltage determine when V2 is driven into conduction. Thus, the monostable multivibrator output frequency is determined by the input trigger frequency, and the output gate width is determined by the discharging of capacitor C2 through resistor R2 toward the potential of the positive voltage supply.

A positive trigger pulse applied to the grid of the tube that is normally cutoff, as was done in this case, is not the only method by which the multivibrator circuit can be triggered. A negative trigger pulse applied directly to the cathode of V1 or applied to the grid of V2 and coupled to the cathode of V1 through the cathod-follower action of R5 serves the same purpose. In some practical-circuit applications, a positive trigger is applied to the grid of a "triggerinverter" stage whose plate is connected in parallel with the plate of V1; the inverted trigger is then coupled through capacitor C2 to the grid of V2 as a negative trigger pulse. In any event, a cycle of multivibrator operation is initiated by driving the normally conducting tube into cutoff, or by driving the tube that is normally cut off into conduction.

#### Failure Analysis.

**No Output.** The input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the grid of V1 can be due to an open coupling capacitor, Cl, or to failure of the external input-trigger source.

Failure of the positive voltage supply, +Ebb, will disrupt the operation of the circuit, as will an open cathode circuit. With tubes (or a single twin-triode tube) installed in the circuit, the filament and plate voltages should be measured, as well as the bias voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether plate-load resistor R3 or R4 or cathode bias resistor R5 is open. If coupling capacitor C2 opens, there will be no feedback signal to effect the multivibrator switching action. An open output coupling capacitor, C3 or C4, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective tube; however, it can also be caused by a decrease in the applied voltage or an increase in the resistance of the associated plate-load

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resistor, R3 or R4. A leaky or shorted output coupling capacitor, C3 or C4, will form a voltage divider with the input resistor of the following stage. If the input resistor of this following stage is returned to ground or to a negative voltage supply, the voltage at the plate of both V1 and V2 will be reduced, and the operation of this following stage will be upset by the change in voltage applied to its grid. Also, the additional current through plate-load resistor R3 or R4 may cause the resistor to bum out.

Incorrect Frequency or Gate Width. The common-cathode-resistor-coupled monostable multivibrator has no components governing the frequency of its outputgate signal; this frequency is governed by the input trigger applied to the circuit. Therefore, any change in the output-gate frequency is a result of improper operation of the trigger-generating circuits. A change in the output-gate width, however, will result if there is a change in the value of either resistor IV?, capacitor C2, or the applied voltage. A change in the resistance or capacitance of the R2-C2 timing control circuit will have the greatest effect on the gate width; changes in the applied voltage will affect the gate width to a lesser degree.

# BASIC ONE-SHOT TRANSISTOR MU LTIVIBRATOR

#### Application.

The basic one-shot transistor multivibrator is used to provide a delay function for compatible logic circuits, or is used as gate in computers, electronic control or communication equipment.

# Characteristics.

Usually uses **fixed** bias.

Requires an on-trigger, but will automatically turn itself off.

Operates at the same repetition frequency as that of the trigger.

Has one stable state (monostable).

Isa saturating type of multivibrator.

# Circuit Analysis.

**General.** The basic one-shot multivibrator is a triggered circuit, which requires a trigger pulse to initiate action. Once the trigger pulse initiates the action, the circuit automatically completes one full cycle of operation. Either the stable state of cutoff or

saturation is used. Normally, one transistor is operated saturated while the other is at cutoff. When the circuit is triggered by an external pulse, the operating point is moved from the initial stable region to the other stable (operating) region. The time constant of the circuit elements determines how long the circuit will remain in the stable (operating) region. At the end of the time constant, the operating point then moves back to the original stable region.

**Circuit Operation.** The schematic of a typical basic monostable (one-shot) multivibrator is shown in the accompanying illustration.



**Basic PNP One-Shot Multivibrator** 

Fixed forward bias is applied to the base of Q2 by resistor R2, while the voltage divider consisting of R4, R3, and R5 forma **fixed** bias divider between the base bias supply and the collector supply and ground. Thus Q1 is biased slightly positive, and is cut off by this reverse-bias. Resistor R4 also is the collector resistor for Q2, and R1 serves a similar function for Q1. Resistor R3 **serves** as the collector-to-base feedback resistor for Q2. Both emitters are grounded and a cross-connected, grounded-emitter circuit is used. The input is applied through coupling capacitor Ccc, while the output is taken directly from the collector of Q2.

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If desired, the output load could also be capacitively coupled.

In the quiescent condition, transistor Q2 conducts heavily while transistor QI is cut off. This **action** occurs initially because of the large negative forward bias placed on the base of Q2 by resistor R2, which is connected back to the negative supply. Thus an application of power Q2 quickly saturates, and developes a positive-swinging output across R4, which is fed back to the base of Q1 through resistor R3, holding the transistor at cut off. During the on-period of Q2, feedback capacitor Cl is charged positively, through R1 and the low base-emitter saturation resistance of Q2. The low saturation resistance of Q2 base-emitter junction acts as a switch, connecting R1 and Cl in series with the negative supply source and ground.

When the negative trigger is applied to Q1 base through coupling capacitor Ccc (time t in the following waveform illustration), transistor Q1 is driven into conduction by this forward bias. The flow of Q1 collector current through RI reduces the effective collector voltage and produces a positive-swinging voltage across R4, which is applied through feedback capacitor Cl as a positive reverse bias to cut off Q2. As the collector current of Q2 reduces, the voltage across collector resistor R4 rises toward that of the negative collector supply, and an increasing forwardbias is fed back to the base of Q1 through feedback resistor R3. Thus Q2 is cut off and Q1 is turned on. Operation is now reversed and the output from Q2 is a negative voltage. Since Cl is positively charged, when disconnected from ground by Q2 being driven into cut off, the capacitor holds the base of Q2 highly positive (reverse-biased) while it discharges. The discharge path is through the low collector-to-emitter saturation resistance of QI, and ground on one side, and through R2 to the negative supply on the other side. The discharge is shown by the typical RC discharge curve on the trailing edge of the Vb<sub>2</sub> waveform (time  $t_1$  to  $t_2$ ) in the waveform illustration. Q2 remains nonconducting until the base voltage drops to zero and the base of Q2 goes slightly negative at time t2. Q2 immediately starts to conduct, and the flow of collector current through R4 produces a positive-swinging voltage, which is applied through feedback resistor R3 to drive Q1 in a reverse-biased direction and stop conduction through Q1. This action occurs quickly, and a positive square wave now appears at the output of Q2. The quiescent state of

operation continues until the next trigger (time  $t_2$ ), whereupon the switching action described above is again repeated.



Monostable Multivibrator Waveforms

# Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of

shunting resistance employed on the low voltage ranges. Be careful to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** Lack of supply voltage, an open collector resistor, R4, or a defective transistor can cause a no-output indication. Measure the supply and collector voltages with a high resistance voltmeter, if the supply voltage is normal but the collector voltage is low or zero, either R4 is open or Q2 is shorted. Checking the resistance of R4 with an ohmmeter will determine if Q2 needs replacement.

Continuous Output. If bias resistor R2 increases with age or opens, the base of Q2 will tend to float in a zero-biased condition. The collector of Q2 will rise to the supplY value, and a continuous output with no switching action will occur. The same indication will also occur if R3 is open, since Q1 will be biased beyond cut off and the trigger will not be large enough to initiate action. At the very best, an attempt to switch may be noticed, with the circuit reverting back to the cut off condition when the trigger ceases. Such action is best observed with an oscilloscope. Should R5 open, a negative (forwardbias) will be placed on Ql, and both Q1 and Q2 will conduct with a continuous positive output from Q2. On the other hand if Q1 is stopped from conducting by a short across R5, Q2 will continue to operate alone, also producing a continuous positive output. Because of the few resistors in the circuit a quick check with an ohmmeter will determine if they are satisfactory. Should Cl be open circuited, no feedback can be applied from the collector of Q1 to the base of Q2 and switching will not occur, again Q2 will rest in a conducting position with a positive output near zero. If Cl becomes short circuited, R1 and R2 will be paralleled and a higher forward bias will be applied. Q2 base, holding it in conduction and preventing operation. Use an in-circuit capacitance checker to check the capacity of Cl. If the resistors are satisfactory, together with Cl, then Q1 must be defective if a continuous output still occurs.

Low Output. Low collector voltage, improper bias, or defective transistors can cause a low output voltage. A change in collector resistor R4 will also affect the output amplitude. Use an oscilloscope to check the output waveform and determine where the reduced amplitude exists. Then check for the proper bias and collector voltages in that portion of the circuit. If normal voltages are present and the collector resistor is within tolerance, but a low output amplitude still exists, it can only be because of reduced collector current.

**Incorrect Frequency. Since the multivibrator has** no parts which govern the frequency of operation, it is governed by the applied input trigger. Hence any change in frequency must be the result of improper operation of the turn-on trigger generating circuits.

Incorrect Pulse Width. While the frequency is governed by the input trigger, the length of time the circuit operates before flipping back to the initial stable condition is determined by the circuit timeconstant governed by the charge and discharge of Cl through R2, and also R1. Thus if the value of Cl changes or that of R1 or R2 changes, or if the saturation resistance of transistor Q2 changes appreciably, a different pulse width may be expected. Observation of the output pulse on an oscilloscope will show any change in width. Measure the value of Cl with an in-circuit capacitance checker, and check the resistance of R1 and R2. If these parts appear satisfactory replace Q2 with a known good transistor. Any delays in switching are the result of minority carrier injection into the base at saturation, which requires a finite discharge time until the circuit can be triggered. Should a noticeable delay in switching occur after the circuit has been operating properly, check all parts values.

# PHANTASTRON MU LTIVIBRATOR

#### Application.

**The** phantastron multivibrator is used to generate a rectangular-wave output having extreme linearity and accuracy, for use as gating or timing signals.

# Characteristics.

Operation is similar to that of a monostable multivibrator.

Pulse width or delay varies linearly with the applied control voltage.

Requires an electron tube of the pentode or pentagrid type.

Circuit operation turn-on is by application of negative trigger to the plate, or positive trigger to the suppressor, of a pentode or the additional control grid of a pentagrid tube; turn-off is automatic by internally generated waveform. Output can be taken from the cathode, screen, or plate, and may be either positive or negative, as selected.

Provides either a low-impedance or highimpedance output, as determined by output connections.

# Circuit Analysis.

General. The phantastron circuit is considered to be a relaxation oscillator similar to the multivibrator in operation; the screen-coupled and cathode-coupled phantastron circuits are analogous to the plate-togrid< oupled and cathode-coupled monostable multivibrators, respectively. A difference in the operation of the circuits is that the monostable multivibrator derives its timing from an exponential waveform developed by an R-C network, whereas the phantastron uses a basic Miller-type sweep generator to produce a linear timing waveform. The phantastron is usually turned on by the application of a gating or trigger pulse, and is turned off automatically by an internally generated waveform. Both a positive and a negative rectangular-wave output with well-defined leading edges may be obtained from the phantastron, depending on the output connections.

For a thorough analysis of Miller circuit operation, and the operation of the screen-coupled, and fastrecovery pentode phantastron circuits, refer to the discussion of time delay circuits in the Special Circuits Section of this Handbook.

**Circuit Operation. The** following schematic illustrates a pentagrid tube (type 6SA7 or equivalent) in a cathode-coupled phantastron multivibrator configuration. Although the schematic illustrates a pentagrid tube, a sharp-cutoff pentode, such as the 6AS6 or its electrically equivalent premium-type miniature 5725 or subminiature 5636, could be used as well, provided that the necessary circuit modifications are incorporated as illustrated and described in the Special Circuits Section of this Handbook.



Pentagrid Phantastron Multivibrator

The functions of the electrodes of the pentagrid tube used in this circuit are as follows: Grid 1, which is the control grid, controls the total tube (cathode) current. Grids 2 and 4, connected internally, act as the screen grid. The cathode, the control grid (grid 1), and the screen grid (grids 2 and 4) correspond to the normally conducting tube of the cathode-coupled monostable multivibrator. (For analysis of Triode Common-Cathode-Resistor-Coupled Monostable Multivibrator operation, refer to the applicable discussion given earlier in this Section of the Handbook.) Grid 3, which is additional control grid, controls the division between screen and plate current; a negative voltage on this grid reduces plate current and increases screen current; a positive voltage has the opposite effect. Also, grid 3 has the effect of changing the cathode current, since some of the

electrons returned toward the cathode by its action pass through the screen grid and reduce the space charge near the cathode, thereby causing the increase of screen current to be less than the corresponding decrease in plate current. Grid 5, connected internally to the cathode, is suppressor grid. The cathode, the additional control grid (grid 3), and the plate correspond to the normally cutoff tube of the cathodecoupled monostable multivibrator.

The circuit components of the pentagrid-tube phantastron multivibrator serve the following functions: Resistors RI and R2 forma voltage divider from the positive voltage supply (+Ebb) to ground, setting the bias level of grid 3 and thereby initially holding plate current cut off. Resistor R3 is the plate-load resistor. The cathode-bias resistor, R4, also serves as the cathode-load resistor. Resistors R6 and R7 form a voltage divider from the positive voltage supply (+Ebb) to ground, setting the operating voltage level of the screen grid. Resistor R5 returns the control grid to the positive voltage supply, setting the bias level that initially permits the screen grid to conduct heavily. Operation of the circuit occurs at the rate determined by the discharge of feedback capacitor C2 through resistor R5; in some circuits this grid-return resistor, which usually has a value exceeding 1 megohm, is made variable to set the maximum delay or pulse width of the output gate. Capacitor C2 also provides feedback from plate to grid to allow rapid response to any changes in the plate voltage. Capacitor Cl couples the input trigger to grid 3; this trigger initiates (or turns on) the phantastron action. Capacitors C3 and C4 are the output coupling capacitors for the screen grid and cathode, respectively; a positive gate is obtained from the screen grid, and a negative gate from the cathode. If desired, a linear sawtooth waveform can be obtained from the plate of the phantastron circuit.

The following simplified schematic diagram shows the charge and discharge paths for capacitor C2. The charge path (part A of the illustration) is from ground through cathode resistor R4, the low cathode-to%rid conduction resistance of VI, to the right side of the capacitor, and then from the left side of the capacitor through plate-load resistor R3 and the positive voltage supply back to ground. This path causes capacitor C2 to charge at an exponential rate during the time that plate current is cut off and the tube is drawing heavy screen current and only slight control grid current. The discharge path (part B of the illustration) for capacitor C2 is from its right side through grid-bias resistor R5 and the positive voltage supply (+Ebb) to ground, and then from ground through cathode resistor R4 and the low cathode-to-plate conduction resistance of V1 to the left side of the capacitor. This path causes capacitor C2 to discharge at a linear rate during the time that screen current is low (near cutoff) and the tube is drawing heavy plate current. The linear discharge of capacitor C2 results from the Miller effect of tube VI, producing a much longer discharge circuit than could be obtained from R5-C2 alone. That is, although the discharge rate of capacitor C2 is determined by the time constant of R5-C2, the discharge capacitance is not the value of C2 alone, but is effectively the value of C2 times the quantity unity plus the gain of V1 (1 + A), which is the Miller effect.





The operation of the phantastron muhivibrator can be more easily understood by referring to the preceding circuit illustrations and the accompanying waveform illustration during the following discussion. When voltage is first applied, the plate section of the tube is in cutoff and there is heavy screen grid current. The conduction of screen current

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is a result of the operating voltage on this electrode, as determined by voltage divider resistor R6 and R7. The voltage is sufficiently positive to attract electrons emitted by the cathode as a result of the positive bias on the control grid (positive voltage return to B+ through resistor R5); this permits the flow of cathode current at this time. In addition to permitting heavy screen current, the positive control grid draws current and charges capacitor C2 through the path described previously. The total screen and control grid current through cathode-bias resistor R4 produces a voltage drop across this resistor. Comparison of the ek and eg<sub>3</sub> waveforms reveals that the positive potential at the top of resistor R4 is now greater than the positive potential at grid 3, which is obtained from the action of voltage divider resistors RI and R2. A bias voltage is therefore established between grid 3 and the cathode; this bias is sufficient to cut off plate current, while having no effect on screen or control grid current. Because there is no plate current, the plate potential is maximum positive (at B+), as depicted by the ep voltage w"aveform during time intervrd a. Notice, also, during time interval a, that the screen voltage  $(eg_{214})$  is at a minimum as a result of heavy screen current, the cathode voltage (ek) is positive, and the control grid voltage (eg.) is positive because the positive-going signal at the plate is fed back through capacitor C2. This, then, is the stable state of the phantastron multivibrator; the circuit remains in this condition (heavy screen current and plate current cut off) until a positive trigger pulse is applied to grid 3 at **t**<sub>1</sub>.





When the positive trigger  $(e_{in})$  is applied through capacitor Cl to grid 3, it overcomes the bias on this grid and permits plate current to flow. This current, in turn, causes an immediate drop in the plate voltage developed across plate-load resistor R3. The

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negative-going signal at the plate is coupled through capacitor C2 to the control grid, where it drives the grid sufficiently negative to reduce the total cathode current. Since the total cathode current is reduced, the screen current is also reduced; thus a positivegoing voltage is produced at the screen grid. Through cathode-follower action, the negative-going signal at the control grid is coupled to the cathode, where it reduces the bias between the cathode and grid 3. With a decrease in this bias voltage there is an increase in plate current, resulting in a further drop in plate voltage. The action just described is cumulative and instantaneous, so that when the positive trigger is applied to grid 3 at  $t_1$ , there is an immediate increase in plate current and a sharp fall in plate voltage, a decrease in screen current and a sharp increase in screen voltage, a decrease in total cathode current and sharp decrease in cathode voltage, and the control grid is driven negative. All of the voltage relationships are depicted at t on the waveform illustration.

The fact that the plate current increases while the cathode current decreases is possible because the screen current is now decreasing. Therefore, the rise in plate current results from the fact that the plate draws current which had previously gone to the screen grid. That is, the bias between the cathode and grid 3 is decreasing, which is a regenerative action, causing the plate current to increase. Simultaneously, the bias between the cathode and control grid is increasing, which is a degenerative action, causing the total tube current (and screen grid current) to decrease. The screen grid current is only reduced-not cut off completely; if it were cut off completely, the plate current would also be cut off and circuit would not function. Hence, there must be a point were the regenerative and degenerative effects are equal and the current stabilizes for an instant. This is the instant (at  $\mathbf{t_1}$ , when the sharp drop in plate voltage ceases) at which capacitor C2 begins its linear discharge action.

As capacitor C2 discharges during time interval b, it loses electrons from its right side, in effect making this side of the capacitor (and the control grid as well) more positive to reduce the bias between the control grid and the cathode. The reduction in control grid bias permits a heavier flow of plate current through the tube, which gradually raises the voltage drop across cathode-bias resistor R4 (ek waveform) and lowers the plate voltage (ep waveform), as illustrated during time intervals b. The rate of change in tube current is governed by the discharge rate of capacitor C2 through resistor R5. Thus, in discharging, the control grid side of capacitor C2 gradually becomes more positive, causing an increase in plate current that produces a constant decrease in plate voltage. The positive voltage increment on the control grid is always slightly greater than the negative-going plate signal it produces; therefore, the the grid potential gradually rises and the plate potential gradually drops, as depicted by the respective grid (eg<sub>1</sub>) and plate (ep) waveforms during time interval b.

An important characteristic of this circuit is the extreme linearity of the rate of change in the plate voltage and grid voltage during time interval b. The positive-going grid increases tube conduction, thereby decreasing the internal resistance of the tube. A decreasing resistance in series with a capacitor results in a linear voltage discharge of the capacitor, instead of the exponential discharge obtained when a **fixed** value of resistance is in series with a capacitor. The phantastron plate voltage during time interval  $\boldsymbol{b}$  is, therefore, a linear downward-sloping voltage, and the grid voltage is a linear upward-sloping voltage.

The action described during time interval b continues until the plate voltage becomes so low (only a few volts) that the tube can no longer amplify the changes in plate voltage. At this instant, t,, capacitor C2 stops discharging and the control grid is rapidly driven positive, causing the tube current to increase at a very fast rate. The rapid rise of current through cathode-bias resistor R4 produces a high positive potential on the cathode, which, in relation to the positive potential at grid 3, is a bias sufficient to cut off plate current. Since the total tube current is increasing at this instant, the additional current must flow in the screen grid circuit. The action occuring is regenerative; as the plate voltage goes positive because of plate-current cutoff, the control grid goes positive and causes an increase in tube current, which produces a higher voltage drop across resistor R4 to increase the bias on grid 3 and further cut off plate current. Thus, the phantastron multivibrator has returned to its original stable state of plate current curoff and maximum screen grid current, as illustrated during time interval c, until the next trigger pulses at t again causes a cycle of phantastron action. Before the phantastron is ready for the next cycle of operation, however, capacitor C2 must

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charge through the relatively long exponential R-C time constant circuit of R3-C2. Because of the relatively slow recharging of C2, a long period must pass after completion of the phantastron gate before the application of the next trigger pulse. The long charge time of C2 is depicted on the plate voltage (ep) waveform during time interval c.

As mentioned previously, when the phantastron is triggered (turned on) there is a sudden drop in the screen current. This produces on the screen grid a positive-going voltage with a steep leading edge  $(e_{g214} waveform)$ . As the tube current gradually increases, producing the linear drop in plate voltage, the screen current increases in the same manner, but by a much smaller amount. The screen waveform will therefore decrease linearly by a small amount until the point of plate-current cutoff (described previously) is reached. At the instant of plate-current cutoff, the screen current increases sharply, causing a sharp drop in screen voltage, as depicted by the trailing edge of the eg<sub>214</sub> voltage waveform; this is the positive-gate output waveform coupled through capacitor C3 to the screen output terminals. The resultant negative-gate output, ek, taken across cathode resistor R4, is coupled through capacitor C4 to the cathode output terminals. This negative-gate waveform also has steep leading and trailing edges, with the flat portion falling off in amplitude at a linear rate.

From the circuit action just described, it is evident that changing the value of the applied voltage will determine the point, and the time, at which the plate voltage "bottoms", with respect to the time of application of the input trigger. Changing the value of either feedback capacitor C2 or grid resistor R5 will also affect the pulse width by controlling the rate of discharge of capacitor C2. For example, increasing the value of either resistor R5 or capacitor C2 will increase their R-C time constant, thereby causing capacitor C2 to discharge more slowly and increase the width of the delay gate. A decrease in the value of either resistor R5 or capacitor C2 will have the oppostie effect on the width of the delay gate. In some phantastron circuits the grid resistor, R5 in this case, is made variable so as to control the maximum width of the delay gate.

Variations o f the phantastron multivibrator include separate diodes for input trigger application and clamping the plate voltage at a predetermined level, and a cathode follower in the charging circuit of

feedback capacitor C2. The diode in the input trigger circuit acts as a trigger injector and also as a disconnecting diode to effectively isolate the trigger circuit after the phantastron action has started. The "platevoltage catching", or clamping, diode establishes the maximum level of plate voltage, and since the turnoff level is fried, effectively controls the time during which the phantastron produces the linear delay gate. The cathode follower is added to reduce the time required for recharging the feedback capacitor, C2 in this case, between gates; the plate circuit of the pentagrid tube merely raises the grid voltage of the cathode follower, and conduction through this tube charges the capacitor at a much faster rate than through the normal plate-load-resistor charge path. The latter typee of circuit is knowrt as a "fastrecovery phantastron". All the variations in phantastron circuitry mentioned in this paragraph are described in more detail in the Special Circuits Section of this Handbook.

#### Failure Analysis.

No Ouput. The input trigger should be checked with an oscilloscope to determine whether it is being applied to the circuitry and whether it is of the proper polarity and amplitude. Lack of an input trigger at the additional control grid (grid 3) can be due to an open input coupling capacitor, Cl, or to failure of the external input-trigger source. It is also possible for excessive bias to make the circuit inoperative because the input trigger amplitude is not sufficient to overcome the bias and initiate the phantastron action. Such a condition is indicated when an input trigger can be seen with an oscilloscope on grid 3 of the pentagrid tube and voltage appears on all tube elements, but either the control grid or cathode voltage is higher than normal. This is most likely to occur when a negative voltage source is used with a common bleeder network to obtain the bias (as in a screen-coupled circuit). Since this cathode-coupled pentagrid circuit develops its own bias, an excessive current drain or short-circuit condition would be needed to increase the bias to the nonoperating point.

Failure of the positive voltage supply, +Ebb, will disrupt the operation of the circuit, as will an open cathode circuit. With a tube installed in the circuit, the filament, plate, screen, and grid 3 voltages should be measured, as well as the bias voltage developed across the cathode resistance, to determine whether

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the applied voltages are within tolerance and whether an associated electrode resistor is open. If feedback capacitor C2 is open, there will be no feedback signal to promote the phantastron action. An open output coupling capacitor, C3 or C4, will prevent the output-gate signal from reaching the following stage.

Reduced Output. A reduction in output is generally caused by a defective tube; however, a low screen gate output can also be caused by a decrease in applied voltage or a change in resistance value in the screen circuit. Low cathode gate output indicates low cathode current, which is the sum of **all** tube element currents, and thus may be caused by any one of numerous conditions (decreased tube conductance, reduce plate or screen voltage, etc). Usually, a voltage check will locate the defective circuit and component. A leaky or shorted output coupling capacitor, C3 or C4, will form a voltage divider with the input resistor of the next stage. If the input resistor of this next stage is returned to ground or to a negative supply, the voltage at the screen grid or cathode will be reduced, and the operation of the stage will upset by the change in voltage applied to its grid.

**Distorted or Unstable Output. Distortion is in**dicated by a nonlinear waveform or an inaccurate time delay. Linearity and accuracy of the output gate

waveform development is the basic property of this circuit, with the controlling elements being the applied d-c control voltage and the R-C time constant in the feedback circuit. Control voltage trouble may occur when the circuit uses a separate external control voltage from a separate power supply, since power supply fluctuations can easily change the operating level and, therefore, the gate duration. A change of time constant due to changes in circuit values or to feedback capacitor failure or leakage will change the rate of operation and hence the gate length; this should be most noticeable for the longer gate lengths. False triggering due to pickup of noise or stray pulses in the control cabling (on remote units) may affect both the turn-on and turn-off of the gate. This instability, or jitter, can also be caused by power supply fluctuations. An oscilloscope waveform check at each electrode is usually the best method of checking for the cause of the jitter, which can then be traced to its source.

**Incorrect Frequency. The phantastron** multivibrator has no components governing the frequency of its output gate signal; this frequency is governed by the input trigger applied to the circuit. Therefore, any change in the output gate frequency is a result of improper operation of the trigger generating circuits.

# SECTION 8 SWEEP GENERATORS

# PART 8-1. SAWTOOTH

# SAWTOOTH WAVE, GAS-TUBE SWEEP GENERATOR CIRCUITS

# General.

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A sawtooth *wave* is defined as a periodic wave which varies in amplitude between two values to provide a waveform pattern resembling the teeth of a saw.

The sawtooth waveform has many applications in television, radar, and special test equipment. It is commonly used as the time base for cathoderay tubes which employ electrostatic deflection of the electron beam. For this type of deflection, the horizontal deflection circuits require a linear time base, that is, a type of voltage waveform which is directly proportional to time. The following illustration shows a sawtooth voltage waveform.



Typical Sawtooth Waveform

The useful portion of the sawtooth waveform is called the sweep time, and the remaining portion is called the retrace, or *fly-back*, time. The sweep volt-

age developed by the sweep-generator circuit is used to move (deflect) the spot across the fluorescent screen of the cathode-ray tube at a uniform rate. During the retrace, or fly-back, portion of the waveform, the spot is returned very rapidly to the initial starting point of the sweep, ready for another sweep trace to be generated. The waveshape of the retrace portion, during the period of time between the end of one sweep and the beginning of the next, is usually not very important insofar as the cathode-ray tube display is concerned. This is because the rate at which the spot returns across the fluorescent screen is usually too rapid to be visible or because a blanking pulse is applied to the cathode-ray tube to supress the spot during the retrace period. The sweep portion of the sawtooth waveform, however, must be very nearly a linear (straight-line) function of time.

The simplest forms of sawtooth sweep generator make use of the principle of charging and discharging a capacitor to obtain the desired output waveform. By using only the most linear portion of the exponential charging **curve** of a capacitor, the gas-tube sweep generator can produce a reasonably linear sawtooth waveform; however, perfect linearity of the sweep is difficult to obtain with this type of sweep generator.

# TRIODE SAWTOOTH-WAVE SWEEP GENERATOR CIRCUITS

#### General.

Triode sweep generators use externally controlled electron-tube sweep circuits which produce symmetrical sawtooth waveforms for the duration of the trigger gate. As shown in the accompanying illustration, the output voltage rises at a linear (constant) rate during the negative input gate, and then drops back to zero between input gates.

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**Triode Sweep Generator Waveforms** 

The duration of the linear portion of the output waveform is known as the sweep time, and is determined by the duration of the input gate. The time from the beginning of one sawtooth wave (sweep) to the beginning of the next sawtooth wave is known as the sweep-repetitwn period, and is determined by the repetition period of the input gate. The term *linearity* is used to describe the straightness of the sweep portion of the sawtooth waveform. The more closely the sweep approaches a straight (but sloping) line, the **greater the linearity**.

In triode sawtooth-wave sweep generator circuits, the electron tube is used as a switch to control the charge and discharge of a capacitor which produces the desired sawtooth output waveform. During the negative input gate, the triode acts as an open switch and allows the capacitor to charge, producing the linear sweep. At the end of the input gate, the triode acts as a closed switch, causing the capacitor to discharge very quickly, and preventing it from **recharg**ing until the next input gate is applied to initiate the next sweep cycle.

Two triode sawtooth-wave sweep generator circuits are in general use: The basic Triode Sawtooth Sweep Generator and the Bootstrap Sweep Generator. The major difference between the two circuits is in the linearity of the sawtooth output waveform. While the output of the basic circuit is sufficiently linear for most applications, the bootstrap circuit provides an extremely linear output for applications where the waveform distortion in the basic circuit cannot be tolerated. Each of these circuits is discussed in detail in the following paragraphs of this section of the Handbook.

# SEMICONDUCTOR SAWTOOTH-WAVE CIRCUITS

#### General.

Although electron tube sweep generator circuits are divided into two classes, the vacuum (hard) tube sweep-generator and the gaseous (soft) tube sweepgenerator, they are not so divided for semiconductors. Actually, the semiconductor sweepgenerator circuits are analogous to the gaseous (soft) tube circuits, utilizing special transistors which are comparable to the thyratron type of electron tube.

Two general types of transistors are used, that is, the unijunction or double-based diode with three terminals and the four-layer diode having only two terminals. These transistors may be used as switches or as relaxation oscillators, and can produce other than sawtoothed waveforms if desired. The discussion in this section, however, will be limited to the production of sawtoothed waveforms by use of the relaxation oscillator form of circuit. The advantages and utility of these semiconductor circuits lie in their extreme simplicity and their use of relatively few components; plus the fact that one unijunction is considered the equivalent of two normal transistors. In most cases only a capacitor and a transistor are required to produce a sawtooth sweep. Where adjustable frequencies of periodic recurrence are desired, a resistor may be added, with the RC combination governing the period of oscillation. The basic principle of operation is that of charge and discharge of a capacitor, controlled by the semiconductor operating as a negative resistance oscillator.

Operation is normally restricted to frequencies from a lower frequency of approximately one or two cycles per minute to an upper frequency which lies between 500 KHz and 1 MHz for presently available transistors. In some experimental units the upper frequency has exceeded 1 MHz but not 3 MHz. Although the upper frequency limit of the transistor is not as high as that of the electron tube, the range is **suffi**cient for normal applications of sawtooth waves. The recovery time is shorted for semiconductors than the deionization time of tubes (on the order of 30 microseconds as compared with 100 microseconds or

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more), which offers some advantage over the electron tube.

#### NEON GAS-TUBE SWEEP GENERATOR

# Application.

**The** sawtooth-wave sweep-generator circuit using a neon gas tube is one form of relaxation oscillator. This type of circuit is occasional used where a simple "free-running" sweep generator will provide a satisfactory sawtooth waveform for use in certain noncritical test-equipment circuits and in cathode-ray tube circuits employing electrostatic deflection.

## Characteristics.

Free-running, relaxation-oscillator type.

Output is sawtooth waveform.

Output sweep frequency is determined by **R-C** circuit, type of neon gas tube used, and voltage applied to circuit. Sweep frequencies up to 10 KHz can be produced.

Neon gas tube is used as switch to control charge and discharge of capacitor.

# **Circuit** Analysis.

**General.** In the discussion of time constants given in the introduction to the **Amplifier** Section of this Handbook, the typical charging curve for an R-C circuit was illustrated. If a capacitor is charged through a resistance from a constant-voltage source, an exponential voltage curve is obtained across the terminals of the capacitor. Eventually the charge on the capacitor rises to a value equal to the applied voltage. The initial portion of the **R-C** charging curve is reasonably straight, with very little curvature, and if only a small part of the initial portion of the charging curve is utilized, the degree of linearity obtained is considered to be satisfactory for many sweep applications.

In order to develop a sawtooth voltage, it is necessary to charge the capacitor and then quickly discharge it to complete the charge-discharge cycle; the cycle is then repeated over and over to produce the desired sawtooth output waveform. A means must be provided to quickly discharge the capacitor once it has received a partial charge. At extremely low frequencies a mechanical switch can be used to short the capacitor terminals and discharge the capacitor; however, such a switching system becomes impractical at the higher frequencies.

The neon gas tube (or neon bulb) is a practical and simple device which can act as an electronic switch to discharge the capacitor. A neon gas tube has a negative resistance characteristic and, because of this characteristic, as soon as the tube is ionized, heavy current will flow through it. If the tube is connected directly across a source of voltage which is sufficiently high to ionize the gas, the current rises rapidly to a value which can damage the tube. However, in a typical sweep-generator circuit, the resistance in the circuit limits the current and prevents it from damaging the gas tube; furthermore, the tube conducts primarily to discharge the capacitor.

The value of the terminal voltage necessary to cause ionization of the gas tube is termed the striking, or *firing*, voltage. When the tube ionizes, its internal resistance becomes very low and will allow a heavy current flow as long as the voltage applied to the tube is sufficient to maintain ionization. However, when the voltage drops to a low value, conduction ceases. The value of voltage at which conduction ceases and the tube deionizes is termed the extinguishing, or recovery, voltage. Approximate values of striking and extinguishing voltages for several common types of neon gas tubes are 65 and 20 volts, dc, respectively.

**Circuit Operation.** In the following illustration, a simple neon gas-tube sweep-generator circuit is shown. Resistor R1 is a series current-limiting resistor; resistor R2 is a variable resistor which permits the frequency of oscillation to be changed. Capacitor Cl is a charging capacitor and V1 is a neon gas tube.



Neon Gas-Tube Sweep-Generator Circuit

Initially, when voltage is applied to the circuit, capacitor Cl begins to charge through resistors R1 and R2, in series. The R-C time constant establishes the frequency of oscillation for a given value of applied voltage and depends upon the value of the capacitor and the combined resistance of the two resistors, RI and R2. The tube is not ionized during this period of time and represents a high impedance in parallel with the charging capacitor. The voltage across capacitor Cl builds up gradually following the R-C charge curve, shown on the accompanying illustration of the output-voltage waveform, until the terminal voltage of the capacitor reaches the striking voltage of the neon gas tube, V1. When the striking voltage is reached, the tube ionizes and conducts to form a low-impedance path to discharge the capacitor. Capacitor Cl discharges through the tube, and the terminal voltage drops rapidly. As soon as the voltage drops to a value equal to the extinguishing voltage of the gas tube, the tube deionizes and current stops flowing. The tube again represents a bigh impedance in parallel with the charging capacitor, Cl, and the voltage again starts to rise across the capacitor. As shown on the waveform illustration, capacitor Cl charges again until the striking voltage of the gas tube is reached. The tube then ionizes and discharges the capacitor; this operation repeats over and over as long as voltage (Ebb) is applied to the circuit.



**Output Voltage Waveform** 

The linear sweep portion of the sawtooth waveform is produced when capacitor Cl is charged, and the retrace or flyback portion of the waveform is produced when the capacitor is discharged by conduction of the tube. The sweep time depends upon the values of resistance and capacitance in the circuit, upon the, applied voltage, and upon the characteristics (striking and extinguishing voltages) of the neon gas tube. The characteristics of the tube are **fixed** and depend upon the particular type of tube used. Therefore the sweep time and frequency are controlled primarily by any of the first three factors previously mentioned: the resistance, the capacitance, or the applied voltage.

In order to obtain reasonable linearity of the sweep portion of the sawtooth wave, the applied voltage is maintained at a high constant potential so that operation of the neon gas tube and charging capacitor takes place on the lower, straight portion of the charging curve, as shown on the accompanying waveform illustration. Variations in operating frequency are usually accomplished by changing either the circuit resistance or capacitance, or both. In a practical sweep generator, the value of the capacitance (Cl) is fixed, and the resistance (R2) is adjusted to change the R-C time constant of the circuit. The range of operating frequency is sometimes extended beyond that obtainable with a variable resistance alone by incorporating a switch either to select one of several fixed capacitors or to select and parallel a number of fixed capacitors.

The time required for the retrace, or flyback, portion of the sawtooth waveform to occur is determined by the impedance of the neon gas tube when ionized, the difference between the striking and extinguishing voltages of the tube, and the value of the capacitor in the circuit. Normally, however, the impedance of the tube is so low that the retrace, or flyback, time does not become appreciable until the sweep frequency exceeds approximately 10,000 Hz.

# Failure Analysis.

**No Output.** A neon gas tube radiates a characteristic orange-red glow when ionized. An indication of gas-tube operation can therefore be obtained by visual inspection to determine the presence of the characteristic glow from the ionized gas within the tube.

If the gas tube is ionized continuously and no sweep output is obtained, it is likely that capacitor Cl is open or that resistors R1 and R2 have decreased in value. In this case the tube attempts to act as a voltage-regulator tube and it conducts continuously; the voltage developed across the gas tube remains a constant value. Capacitor Cl can be checked by using NAVSHIPS 0967-0004120

a suitable capacitance analyzer to determine whether or not the capacitor is defective. An ohmmeter measurement of resistors RI and R2 can be made to determine whether a decrease in resistance has occured. If the conduction current through the neon gas tube is excessive for any great length of time, the tube may be damaged and its characteristic will be impaired as a result.

Although the gas tube may appear to be glowing in the proper manner, this is not a positive indication that the tube is operating correctly; therefore, the tube itself may be suspected as a source of trouble.

If the gas tube fails to ionize, the voltage across capacitor Cl will rise to the full applied voltage, and no sawtooth output voltage will be developed. If the tube is not ionized, however, this does not necessarily mean that the tube is defective, since the same indication (lack of glow) may occur if either resistor (R1 or R2) is open, if there is no applied dc voltage (**E**<sub>bb</sub>), or if the **charging** capacitor (Cl) is shorted. The value of each resistor, RI and R2, can be checked by ohmmeter measurements to determine whether any increase in resistance or an open has occurred. Measurements can also be made across the capacitor terminals to determine whether capacitor Cl is shorted, thus causing the voltage to be either zero or an extremely low value.

**Incorrect Frequency.** It is reasonable to assume that any change in the values of resistance (R1, R2) or capacitance (C1) will affect the R-C time constant of the circuit and, thus, the frequency of operation. When an adjustment is provided, as for example resistor R2 in this circuit, a change in operating frequency can be compensated for by adjustment of the series resistor, R2. " If the R-C time constant is increased, the frequency of operation will decrease; conversely, if the time constant is decreased, the frequency of operation will increase. A change in the value of R1 or R2 can be determined by ohmmeter measurements; the value of capacitor C1 can be measured with a suitable capacitance analyzer.

Assuming that the values of R and C remain constant, a change in the applied voltage  $(E_{bb})$  will affect the operation of the circuit; thus, an increase in applied voltage will increase the frequency of operation, while a decrease in voltage will decrease the frequency.

The characteristics of the neon gas tube may be affected as the tube ages; therefore, the striking and extinguishing voltages of the tube may change causing the circuit to shift its operating range on the R-C charge curve. This condition may cause not only a change in operating frequency, but also changes in sweep amplitude and linearity.

# THYRATRON SWEEP GENERATOR

#### Application.

The thyratron sweep generator is used to produce a linear sawtooth sweep voltage waveform for radar equipments, television sets, electronic displays, and special test equipments employing an electrostatic type of cathode-ray tube.

#### Characteristics.

Employs a thyratron gas tube in a relaxation oscillator circuit.

The thyratron is used as a switch to control the charge and discharge of a capacitor.

Output is a sawtooth voltage waveform.

Output amplitude is determined by the characteristics of the thyratron.

Output sweep frequency is determined primarily by the time constant of the R-C circuit.

Sweep frequencies up to 75 kHz can be produced.

#### Circuit Analysis.

**General.** When a series R-C circuit is connected across a constant-voltage source, the capacitor charges and the voltage measured across its terminals increases at an exponential rate until the voltage becomes equal to the source voltage. Only the initial portion of the capacitor charging curve is sufficiently linear to be used in the generation of a sawtooth wave. To generate the sawtooth wave, it is necessary to restrict the capacitor charge to a small portion of the total source voltage, and then cause it to discharge very quickly. The charging cycle is then repeated. In addition to hard tubes, a thyratron may also be used as a switch to control the charge and discharge of the capacitor, and thus produce the desired sawtooth-wave output.

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In a gas-filled tube the ionization potential (firing voltage) determines the plate voltage at which the tube begins to conduct, and the deionization potential (extinguishing voltage) determines the voltage below which the tube ceases to conduct. When the plate voltage of a gas tube exceeds the ionization potential, the gas in the tube ionizes and the tube conducts very heavily. It continues to conduct heavily until the plate voltage is lowered below the deionization potential, when the gas in the tube deionizes and the tube ceases to conduct. The thyratron is a special type of gas-filled triode in which a third element, a control grid, is used to control the ionization of the tube. The control grid, however, has no effect on the deionization potential of the thyratron; it can ordy initiate conduction. Once triggered, the thyratron continues to conduct until the plate voltage drops below the deionization potential of the tube.

**Circuit Oparation.** The accompanying circuit schematic illustrates a typical thyratron sweep generator.



**Thyratron Sweep Generator** 

Capacitor Cl and resistor R4 make up the R-C charging circuit, which is used as an integrator to produce the sawtooth output wave. Thyratron VI is connected in parallel with capacitor Cl, and functions as a switch to control the charge and discharge

of the capacitor. Resistors RI and R3 forma voltage divider from the negative bias supply to ground, which supplies fixed grid bias voltage to the thyratron through grid-current limiting resistor R2. Since resistor R3 is variable, the brid bias, and thus the trigger potential of the thyratron, can be varied.

When voltage is **first** applied to the thyratron sweep-generator circuit, capacitor Cl begins to charge through resistor R4. As the capacitor charges, the voltage across it, and across thyratron VI, increases from zero toward the full value of the plate-supply voltage. If the capacitor were allowed to reach full charge, the voltage across it would increase exponentially to the full value of the plate-supply voltage, as shwon by the broken line on the accompanying output-voltage waveform illustration.





However, when the voltage across capacitor Cl (and across thyratron VI) exceeds the ionization potential of the thyratron (point A on the waveform illustration), the tube instantly ionizes and begins to conduct very heavily. Since the conducting thyratron has very low (almost zero) impedance, it shunts capacitor Cl and causes the capacitor to discharge very quickly through the tube. Thus, the capacitor charges to the ionization potential of the thyratron, which is determined by the thyratron grid voltage, and then discharges. As the capacitor discharges, the voltage across it drops toward zero. When the voltage across the capacitor drops below the deionization potential of thyratron V1 (point B on the waveform illustration), the tube deionizes and ceases to conduct. Since the non-conducting (cut off) thyratron

has a very high (almost infinite) impedance, it no longer effectively shorts capacitor Cl, and the capacitor again beings to charge toward the full plate-supply voltage value. The capacitor charges until the voltage across it exceeds the ionization potential of the thyratron, at which time the tube conducts and discharges the capacitor. This charge-discharge cycle continues to repeat as long as voltage is applied to the circuit-capacitor Cl charges while thyratron VI is cut off, and discharges when the thyratron conducts. Thus, thyratron VI acts as a switch and causes capacitor Cl to alternately charge and discharge, producing a sawtooth output wave.

The sweep frequency of the thyratron sweep generator is determined by the time it takes for capacitor Cl to charge to the ionization potential of thyratron VI. The charge time of the capacitor is determined by the time constant of the R-C circuit made up of resistor R4 and capacitor Cl, and can be changed by adjusting variable resistor R4. Increasing the value of resistor R4 increases the time constant of the R-C circuit, which increases the charge time of capacitor Cl, and thus decreases the sweep frequency. Decreasing the value of resistor R4 has the opposite effect, and increases the sweep frequency.

The amplitude of the sawtooth output wave is determined by the difference between the ionization (firing) potential and the deionization (extinguishing) potential of the thyratron. The ionization potential is controlled by varying the grid bias. Consequently, resistor R3. is used to adjust the thyratron grid bias for the desired output amplitude. Increasing the value of resistor R3 increases the negative voltage on the grid of the thyratron and raises the ionization potential. The consequent larger difference between the ionization and deionization potentials thus increases the amplitude of the sawtooth-wave output. Decreasing the value of resistor R3 has the opposite effect, and decreases the output amplitude. Adjusting resistor R3 also affects the output sweep frequency slightly, but this frequency can be corrected by readjusting resistor R4.

# Failure Analysis.

**No Output.** A no-output condition maybe caused by lack of plate-supply voltage, an open plate resistor (R4), a faulty sweep capacitor (Cl), or a defective thyratron (V1). Since the thyratron emits a characteristic glow when conducting, observation of the tube

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will show whether or not it is conducting. If the thyratron is glowing (conducting), lack of platesupply voltage and an open plate resistor (R4) can be eliminated as possible troubles, since the tube must have plate voltage applied to it through resistor R4 in order to conduct. If the thyratron is not glowing, first measure the plate-supply voltage with a highresistance voltmeter to eliminate the possibility of a faulty power supply, and then check resistor R4 for continuity with an ohmmeter. If it is determined that neither the power supply nor resistor R4 is at fault (either because they have been checked or because they have been eliminated as possible troubles), further checks must be made to locate the trouble. Use an in-circuit capacitor checker to check capacitor Cl for a shorted, open, or leaky condition. If capacitor Cl is not defective, thyratron V1 is probably at fault.

**Incorrect Output Frequency. Any** fault which changes the charge time of capacitor Cl will cause the output frequency to be incorrect. Therefore, check for changes in the value of capacitor Cl and in the setting of resistor R4, and for incorrect plate-supply voltage. It is good practice to first measure the plate-supply voltage with a high-resistance voltmeter to eliminate the possibility of a defective power supply. If the supply voltage is correct, use an ohmmeter to check resistor R4 for the correct resistance value, and a capacitance analyzer to check capacitor Cl for the correct capacitance value.

**Incorrect Output Amplitude.** Since the amplitude of the sawtooth output wave is determined by the difference between the ionization and deionization potentials of thyratron V1, improper grid bias or a defective thyratron may cause the output amplitude to be incorrect. Measure the voltage on the grid of thyratron VI with a high-resistance voltmeter. If the grid voltage is correct, the thyratron is probably defective and should be replaced. If the grid voltage is either high or low, the bias circuit is probably defective. Use an ohmmeter to check resistors RI, R2, and R3 for the proper resistance values.

# UNIJUNCTION (DOUBLE-BASE DIODE) SAWTOOTH GENERATOR

#### Application.

The unijunction transistor is used as a switch or as an oscillator to produce pulses, amplify pulses, and NAVSHIPS 0967-00041120

produce a sawtooth or triangular waveform for sweep generators. It is used mostly in computers, memory circuits, and electronic clocks, but it may be used wherever the solid state equivalent of the thyratron tube is needed.

#### Characteristics

**Is** the equivalent of two normal junction transistors in power handling ability (one unijunction transistor effectively replaces two standard transistors).

Uses the stable N-type open-circuit negativeresistance characteristics inherent in its construction to provide astable, bistable, or monostable operation.

Any of its three terminals maybe used as an input trigger connection or output load connection.

Provides two different output levels for one input signal, and may be similarly or oppositely polarized.

Is temperature-sensitive, with an almost constant linear response (base resistance changes) from -40 to approximately +150 degrees C.

Is photosensitive, and may be made to respond to changes in illumination.

# **Circuit Analysis.**

**Generel. By** virtue of its construction, the unijunction transistor is basically a negative-resistance device, as indicated by the emitter voltage-current characteristic in the following illustration. By setting the load line so that it touches only one point on the curve (operation in cutoff or saturation-regions only), the unit may be made a one-shot device. By operating only over the negative-resistance portion, on-off operation (oscillation) can be obtained and by operation in all three regions, flip-flop operation may be obtained. These characteristics are inherent in the transistor, and may be obtained if the proper bias and connections are made. In this circuit discussion we shall be concerned only with operation in the *negative-resistance region* with the transistor operating as a relaxation-type oscillator, to produce a sawtooth (sweep) waveform.



As constructed, there are three points from which an output may be taken or to which an input may be applied; these are as follows: from emitter to ground or base 1, from base 1 to emitter or ground, and from base 2 to ground, as shown in the accompanying figure. When any of these points are used as an input, the other two points will supply an output. **As** conventionally used, a negative sync trigger is supplied to B2, with a synchronized sawtooth output between emitter and ground, and with a positive pulse available at B1. When synchronization is not employed, the unit will operate as a free-running oscillator at a frequency set by the circuit RC constants, either external, or internal and external.

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Charge Path

**Circuit Operation.** A simple sawtooth generator circuit using a unijunction transistor is shown in the following figure. Note that only the unijunction

Input and Output Points



#### **Basic sawtooth Generator**

transistor, a capacitor, and a power supply are necessary to produce the sawtooth waveform. With the power supply connected, electron flow is from base 1 to base 2, thus placing an initial reverse bias on the PN junction. With the capacitor connected between emitter and ground, a small amount of reverse current flows through the PN junction because of a flow of hole current from the emitter to base 2. The capacitor charges slowly through the path shown in the following figure.

The rate of charge depends on the time constant, which is equal to the product of the capacitance of C and the internal resistance of the reverse-biased junction. As C charges, the positive dc voltage across it rises. When this voltage is greater than the voltage gradient opposite the P-type material, the PN junction becomes forward-biased and the capacitor discharges very rapidly. (This corresponds to the ionization point or voltage of the gaseous thyratron tube.) This action is caused by a heavy electron flow from base 1 to the emitter and a heavy hole flow through the P material of the junction, which causes an electron flow out of the emitter as shown in the following figure. Thus, the capacitor is effectively shortcircuited through the PN junction. The time of discharge is determined by the capacitance of C times the forward resistance of the PN junction. Since the forward resistance is very low (on the order of 5 ohms), it is essentially equivalent to a short circuit. After capacitor C discharges, the voltage across C is too small to maintain the forward bias (this corresponds to the deionization point or voltage of the gaseous thyratron tube); the reverse bias again resumes control, charging the capacitor through reverse-leakage current, as previously indicated, and the cycle is repeated. This slow charging and rapid discharging of capacitor C produces the sawtooth output waveform.



**Discharge** Path

The recurrence rate of the basic circuit just discussed is fixed by the inherent base leakage resistance of the transistor plus the value of capacitance used. To ensure stable operation at the desired sweep rate, and to provide protection against them-ad runaway, an emitter resistor and a base 2 resistor are usually used, as shown in the following schematic. The operation of this circuit is identical to that of the basic sweep generator previously discussed except for the change introduced by the addition of R1 and R2. During the time of heavy conduction (deionization period), the portion of the interbase region between the emitter and base 1 is a very low resistance, whereas the portion between the emitter and base 2 is of high resistivity. Therefore, practically all the power supplied by the interbase power supply is dissipated across the narrow region near base 2. In the absence of R2, a relatively heavy electron current flows through the base 2 region and causes heating of this small semiconductor area. As a result, this thermal effect causes an increased electron flow through the base 2 to emitter portion of the bar. As the heat is built up by current flow, more and more electron current flows through the bar because no external resistance is provided to limit the flow. Thus a" local hot spot is produced. Since this thermal action is accumulative, thermal runaway can occur and destroy the transistor. The use of R2 in the position shown provides sufficient current limiting to prevent the formation of the hot spot and any possibility of thermal runaway. While the circuit is sensitive otherwise to thermal variations, any thermally produced current flow can never be as great as that produced at the location of the hot spot when no limiting resistance is

employed. No other form of protection is needed to prevent thermal failures.



Stabilized Sawtooth Genarator

By adjusting the value of RI, the emitter voltage can be controlled and the operating point (where the emitter changes from reverse bias to forward bias) fixed for the desired operating voltage. By proper design, if the resistance of RI is less than that of the internal reverse leakage resistance of the base bar, the charging of sweep capacitor C is determined mainly by the value of R1. Thus, variances produced by production tolerances in unijunction transistors can be minimized, and the sweep time controlled independently of the transistor. If required, **R1** can be made variable to provide an adjustable sweep. Regardless of the arrangement used, however, the value of R1 together with that of C determine the frequency of the sweep oscillations.

In this improved circuit, then, operation occurs through the charging of capacitor C through R1. When the voltage across C reaches the breakdown voltage, the initially reverse-biased junction breaks down temporarily, becomes forward-biased, and discharges the capacitor through the low base 1 emitter resistance. (This action is similar to that of the gaseous thyratron tube at the point where the voltage reaches the ionization level.) When the capacitor discharges to the point where the voltage across the emitter junction can no longer sustain a forward bias, the transistor stops conducting, and the original reverse-bias condition again exists. (This action is

similar to that of the gaseous thyratron tube, which stops conduction automatically when the voltage across the tube reaches the deionization point or level and is insufficient to sustain ionization of the gas.)

**Detailed Analysis.** Before proceeding with the following discussion, be certain to read the explanation of the construction and operation of the unijunction transistor given in the Special Circuits Section of this Handbook.

A simplified equivalent circuit for the unijunction transistor may be developed as shown in the accompanying figure.



#### Simplified Equivalent Circuit

Diode CR 1 can be considered to be a conventional junction diode, with  $R_{B2}$  representing the resistance of base 2, and  $R_{B1}$  the resistance of base 1;  $R_{B1}$  is shown as variable since it does vary as a function of the emitter base 1 current (the greater the current, the lower the resistance, and vice versa).

Assuming that the capacitor is not connected to the emitter and that both  $R_{B1}$  and  $R_{B2}$  are of a high value, it is clear that the resistors form a voltage divider across the base supply,  $V_{bb}$ . Thus, a positive potential exists at the cathode of the diode, and the diode is reverse-biased. The current flow through base 1 and base 2 will be that permitted by the conductivity of the base bar (the resistance of  $R_{B1}$  plus  $R_{B2}$ ), and the emitter current will be zero (cutoff). When the capacitor is connected between emitter and ground, it charges exponentially through the reverse leakage current of the diode. The charge path is from ground through the capacitor, diode  $CR_1$ , and  $R_{B2}$ . At this time the value of  $R_{B1}$  is high. As the capaci-

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tor charges, the emitter voltage increases and the reverse bias across the junction diode is reduced. Examine the emitter characteristic curve which follows.



**Static Emitter Characteristics** 

With the emitter biased off, the current due to reverse leakage (I<sub>n</sub>) can be considered negative as shown in the figure. As the capacitor voltage builds up it reaches the peak value of emitter voltage at zero emitter current. At this peak point the reverse bias is no longer sufficient to prevent conduction, and emitter (positive) current flows. As soon as emitter current flows capacitor Cl starts to discharge, and the forward resistance of the junction is decreased; this action becomes regenerative, multiplying the discharge current in a somewhat exponential fashion. Once started, this action cannot be reversed or stopped until the lower voltage level (deionization point) is reached. As this current increases, the diode forward resistance decreases and the emitter voltage decreases. The region of decreased emitter voltage with increased emitter current is due to negative resistance, which is the phenomenon upon which the operation of this unit is based. The negative resistance is caused by the injection of holes into the base bar with forward bias change causing increased conductivity between the emitter and base 1 portion of the bar, with base 2 current remaining essentially constant. The sequence of action is such that each enhances the other. That is, as the forward resistance is decreased, so is the amount of reverse bias decreased, and the emitter current increases similarly. This cumulative action continues until the valley point is reached and the base enters the saturation region. At this point any increase in emitter current merely causes an increased drop in the emitter base 2 portion of the bar. If operation is allowed to enter this saturation region, the unit will merely rest in a stable conducting condition with a fairly low base 1 resistance.

The turn-off action of the unijunction transistor is initiated by the dropping emitter potential as capacitor C discharges through base 1. When the valley point on the curve is reached, the emitter voltage (which is produced by the remaining charge in the capacitor) is insufficient to continue conduction. More emitter voltage would be needed to produce more current, or the emitter voltage would have to remain constant at the valley point to keep the same value of current. Since the capacitor continues to discharge below this point, the initial condition of reverse-biased diode then exists. This action is also regenerative, since a reduction of conductivity of the bar (an increase in resistivity) reduced the amount of current it will carry, and the forward resistance is effectively increased. The increased forward resistance further reduces the conductivity of the bar; thus, the path between emitter and base 1 is quickly reduced to zero current or cut-off, whereupon the reverse bias resumes control, holding until the capacitor is again charged to the forward breakdown voltage. In this respect the unijunction diode operates differently from the normal PN junction. The typical response of a normal diode is shown at the bottom of the static emitter characteristic for comparison. In this case, once current flow is initiated, current flow continues in a relatively steady manner as long as the voltage is applied. The ability of the unijunction transistor to revert from a reverse-biased condition to a forward-biased condition and back again under control of the voltage levels applied to its elements is inherent in its construction. While the previous simplified diode representation was used to help explain its operation, it should be understood that a conventional diode connected schematically with two resistors, as illustrated previously, will not operated as a unijunction transistor.

# Failure Analysis.

**No Output. An** open-circuited capacitor will cause the emitter circuit to be open and produce a nooutput condition. The few components involved may be quickly checked by a resistance or continuity test with a high-resistance volt-ohmmeter. If the components appear to be normal, the trouble can only be in the power source or in the transistor itself. Substitution of a known good transistor would be necessary to determine whether it is defective, since there is no other simple check possible. A short-circuited capacitor would also prevent the circuit from operating, but this is not necessarily true of any of the other components, as the circuit usually will operated with the capacitor alone. Where the components and transistor appear to be normal, a poorly soldered joint or broken wiring might be suspected.

Low Output. Poorly soldered joints or defective resistors can cause low output, as can a defective power supply or transistor. Resistance and voltage checks will determine whether the components are defective. Use of an oscilloscope to examine the waveforms on the emitter, base 1, and base 2 elements should help isolate the defective portion of the circuit. With a sawtooth output, there should be a negative pulse on base 2, with a similarly shaped but smaller-amplitude current pulse in the base 1 circuit. (Place a 100-ohm resistor in series with base 1 and observe the voltage waveform produced by the base current.) Capacitor leakage may prevent the circuit from operating properly, or may reduce the amplitude of the output waveform. Leakage may be suspected if the recurrence rate is different from the original rate. (A change in emitter resistor RI can also produce a similar condition.)

**Distorted Output.** The shape of the sawtooth sweep will depend upon the capacitor to a great extent. If only a small portion of the capacitor charge is used, it will be linear, otherwise, the waveform will curve at the top because of the exponential discharge of the capacitor. The values of the components and voltages applied will also determine the linearity of the output waveform. Operation at too high a frequency for the transistor used will produce a rounding off of the waveform and, if excessive, produce a sine wave. Check the waveform with an oscilloscope. The recovery time is determined by the base 1 current pulse width and the sweep capacitor value. If the recovery time is excessive, a triangular wave may result.
# FOUR-LAYER DIODE SAWTOOTH GENERATOR

# Application,

**The** four-layer diode is used to generate a sawtooth (sweep) voltage waveform for applications where the output waveshape is not critical, and where an extremely simple circuit is desired.

# Characteristics

Acts as a switch to control the charge and discharge of a series **R-C** circuit.

Output is a sawtooth voltage waveform.

Output frequency is determined by the values of resistance and capacitance in the R-C circuit.

Output amplitude is determined by the characteristics of the four-layer diode.

# Cirouit Analysis.

**General.** The four-layer diode is a two-terminal semiconductor device consisting of four alternate layers of P-type and N-type silicon. The accompanying pictorial diagram shows the construction and biasing of the diode.



#### Four-Layer Diode

For convenience in discussing the four-layer diode, its three PN junctions are labeled  $J_1$ ,  $J_2$ , and  $J_3$ . To bias the diode correctly, the positive battery terminal is connected to the P-type diode terminal, and the negative battery terminal is connected to the N-type diode terminal. With the bias voltage applied in this manner (layer P<sub>1</sub>positive with respect to layer N<sub>2</sub>), a voltage gradient is set up along the diode as shown by the polarities placed above the junctions on the fourlayer diode illustration. The voltage gradient forwardbiases junctions  $J_1$ , and  $J_3$ , and reverse-biases internaljunction  $J_2$ . Since a forward biased junction exhibits very low resistance and a reverse-biased junction ex-

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hibits very high resistance, junction  $J_2$  (the reversebiased junction) primarily determines the current flow through the diode. Therefore, the action of junction  $J_2$  determines, to a great extent, the operation of the four-layer diode.

Over the **first** portion (region I) of the accompanying dynamic transfer characteristic curve, which covers from zero level to breakdown voltage  $V_{BR}$ , maximum current flow through the diode is limited to the value of the minority carrier current flowing through reverse-biased junction J<sub>2</sub>.



**Dynamic Transfer Characteristic Curve** 

Therefore, over region I of the characteristic curve (also known as the off region), diode current flow remains at a relatively constant but low value while the applied input voltage increases. When the voltage applied to the diode exceeds voltage  $V_{BR}$ , an action similar to the avalanche breakdown in a Zener diode occurs in junction  $J_2$ . That is, the applied voltage temporarily is relatively constant while the current increases (region H on the characteristic curve). Although the breakdown action is not completely understood at the present state of the art, once breakdown occurs and current increases, the characteristic curve passes through another region, known as the negative resistance region (region III), where the voltage across the diode rapidly decreases as the current through it increases. (This corresponds to the action in a gas-filled electron tube which breaks down at the ionization point and passes a heavy current at a low voltage.) At point A on the curve, the end of the negative resistance region is reached, and the voltage across the diode remains relatively constant throughout the on region (region IV). (This corresponds to the action in a gas-filled electron tube which, one broken dew, operates at a level slightly above the deionization point until the applied voltage drops below this point.)

Although the four-layer diode has many applications, it is most widely used as a switch with two stable states. To use the diode as such a switch, it is operated in regions I and IV of the characteristic curve. The diode remains in the high resistance or off state (region I) until the bias voltage exceeds the diode breakdown voltage,  $V_{BR}$ . The diode then switches to the low resistance or *on* state (region IV) and remains in this state until the bias voltage drops below the diode turnoff voltage level. It then switches back to the off state. The four-layer diode is operated in this manner to control the charge and discharge of an R-C circuit to produce a sawtooth-wave sweep voltage output.

Circuit Operation. The accompanying circuit schematic illustrates a sawtooth-wave generator using a four-layer diode and only two other components.



Four-Layer Diode Sweep Generator

The power supply  $(E_{hb})$  is comected directly across the series R-C circuit made up of capacitor Cl and resistor R1. The four-layer diode, CR1, is connected in parallel with capacitor Cl, and controls the charge and discharge of the capacitor, The sawtooth waveform is taken from across the parallel combination of capacitor Cl and diode CR1.

When voltage is initially applied to the circuit, diode CRI is in the high resistance off state, (because of **the** reverse bias applied to internal junction,  $J_{2}$ , and capacitor Cl begins to charge through resistor R1 toward the supply voltage value. If the capacitor were allowed to charge fully, the voltage across it would increase to the supply voltage value at an exponential rate, as shown by the dashed curve in the accompanying output voltage waveform illustration.





However, when capacitor Cl charges to the breakdown voltage of diode CR1 (voltage  $V_{BR}$  on the waveform illustration), the diode breaks down (effec- tively forward biasing internal junction  $J_2$  and switches to the low resistance on state. Since diode CR1 is connected in parallel with capacitor Cl, the diode effectively shunts capacitor Cl and causes it to discharge very quickly. As capacitor Cl discharges through the conducting diode, the voltage across the capacitor decreases until it drops below the turnoff voltage of the diode (voltage  $V_{TO}$ ). At this time, the internal junction is again reverse-biased and the diode switches back to the off state, and the capacitor again begins to charge through resistor RI. Thus, capacitor Cl alternately charges relatively slowly through resistor RI and discharges quickly through diode CRI.

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Since capacitor Cl charges only during the initial portion of the capacitor charging curve (about 10% of the total time available), the resulting output voltage across the capacitor is a fairly linear sawtooth waveform.

The amplitude of the sawtooth output waveform is determined by the characteristics of the four-layer diode. Since the sawtooth amplitude is equal to the difference between the breakdown voltage  $(V_{BR})$  and the turnoff voltage  $(V_{TO})$ , and since these voltages are constant for any particular diode, the output amplitude is fixed. The only way that the output amplitude may be changed is by using a four-layer diode with different breakdown and turnoff voltage characteristics.

The frequency of the sawtooth output waveform is determined by the charge time of capacitor Cl, and therefore by the time constant of the R-C circuit made up of the capacitor and resistor RI. Resistor R1 is usually made variable so that the output sweep frequency may be varied. Decreasing the value of resistor RI decreases the time constant of the R-C circuit, which decreases the time required for capacitor Cl to charge to the breakdown voltage of diode CR1. The resulting waveform (shown by the dotted curve on the waveform illustration) is a sawtooth wave of shorter time duration than the original sawtooth wave, and therefore one of higher frequency. Increasing the value of resistor RI has the opposite effect, and decreases the output sweep frequency.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since the diode may be forward-biased and break down, causing a false low-resistance reading.

No **Output.** A defect in any circuit component, or a lack of supply voltage may cause a no-output condition. Because of the simplicity of the circuit, the trouble can easily be located by making several quick voltage and resistance checks. First, use a vacuumtube voltmeter to measure the supply voltage. If the correct voltage is measured, use an ohmmeter to check resistor R1 for an open or short circuited condition. Next, use an in-circuit capacitor checker to check capacitor C1 for defects. If these checks fail to locate a defective component, diode CR1 is probably at fault.

**Distorted Output.** A distorted sawtooth output waveform may be caused by low supply voltage, by changes in value of the components in the R-C circuit (Cl, Rl), or by a defective diode (CR1). First, use a vacuum-tube voltmeter to measure the supply voltage to determine that the power supply is not at fault. Next, use an ohmmeter to check the value of resistor R1, and use a capacitance analyzer to check the value of capacitor Cl. If no defective component is found, diode CR1 is probably at fault.

# BASIC TRIODE SAWTOOTH SWEEP GENERATOR (ELECTRON TUBE)

# Application.

The basic triode sawtooth sweep generator produces symmetrical, synchronized sawtooth waveforms for sweep voltage use in radar equipments, display indicators, synchroscopes and other types of special-purpose test equipment which use an electrostatic deflection cathode-ray tube.

# Characteristics.

Employs a high-vacuum triode.

Requires a negative operating gate.

Output is a symmetrical sawtooth voltage waveform with equal intervals between sweeps.

Sweep time is determined by the duration or the negative operating gate.

Sweep-repetition period is the same as the repetition period of the operating gate.

# Circuit Analysis.

**General.** Recall from the elementary discussion of time constants in Section 2, paragraph 2.5.1, of this Handbook that when a series R-C circuit is connected across a constant voltage source, the capacitor charges at an exponential rate until the voltage measured across its terminals equals the source-voltage value. Since the initial portion of the capacitor charging curve is nearly linear. This portion of the curve may be used in the generation of a sawtooth wave. In the basic triode sawtooth sweep generator, the electron tube is used as a switch to control the charge and discharge of a capacitor over the initially linear portion of the charging curve, and to produce a sawtooth output wave with good linearity.

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**Circuit Operation. The** accompanying circuit schematic illustrates the basic triode sawtooth sweep generator.



Basic Triode Savvtooth Sweep Generator

Capacitor C2 and resistor R2 form the R-C circuit which produces the sawtooth output waveform. Triode V1 is connected in parallel with capacitor C2, and acts as a switch to control the charge and discharge of the capacitor. Capacitor Cl and resistor RI form a conventional R-C input coupling circuit, which applies the input gate to the grid of triode V1. The sawtooth output is developed across the parallel combination of triode VI and capacitor C2.

In the quiescent state, with no negative input gate applied, there is practically no bias on the grid of triode V1. Consequently, the tube conducts very heavily and the plate voltage drops to a very low value. Since capacitor C2 is connected in parallel with triode V1, the capacitor charges to the low value of plate voltage existing across the tube, and remains charged to this voltage until an input gate is applied.

When a negative input gate is applied to the basic triode sawtooth sweep generator, it drives the grid of triode V1 below plate current cutoff and the tube ceases to conduct. When the triode cuts off, the plate voltage tends to rise instantaneously to the full value of plate-supply voltage, Ebb. However, capacitor C2 is connected in parallel with the triode and thus prevents the plate voltage from rising instantaneously. Instead, the plate voltage rises exponentially toward the plate-supply value at a rate determined by the time constant of the R-C circuit consisting of capaci-







If triode V1 remained cut off indefinitely the voltage across capacitor C2 (and on the plate of Vl) would rise exponentially to the plate-supply value, as shown by the broken line in the illustration. However, at time  $t_1$  the negative input gate ends and the grid bias on triode VI returns to zero. Therefore, triode V1 again conducts heavily and the plate voltage tends to fall instantaneously to a very low value (the initial quiescent value). Since capacitor C2 is connected in parallel. with triode VI, the plate voltage cannot change instantaneously, but rather falls at a rate determined by the discharge time of the capacitor. Since the conducting triode has a very low impedance, it effectively shunts (shorts) capacitor C2, and the capacitor discharges very quickly through the low impedance offered by the tube. As the capacitor discharges, the plate voltage measured between the plate of triode V1 and ground decreases exponentially to the original quiescent value, and remains there until the next negative input gate is applied. Thus, the basic triode sawtooth sweep generator produces one sawtooth wave each time a negative input gate is applied, and remains in the quiescent (off) state between input gates.

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It can be seen from the preceding discussion that the output waveform characteristics of the basic triode sawtooth sweep generator are determined in part by the duration of the negative input gate. If the duration of the input gate is increased, capacitor C2 charges for a longer **period** of time, and this charges to a higher potential. Since a larger portion of the capacitor charging curve is used when the duration of the input gate is increased, the linearity of the sawtooth output wave is decreased. Thus, increasing the input **gate** duration (for example, by decreasing the input frequency) affects the sawtooth wave in three ways: the sweep time (duration) increases, the sweep amplitude increases, and the sweep linearity decreases.

Changing the charge time of capacitor C2 also affects the characteristics of the sawtooth output wave. Since capacitor C2 charges through resistor R2, the charge time of the capacitor is changed by varying the resistance of R2. Adjusting resistor R2 for a higher resistance value increases the charge time of capacitor C2; thus, for a given input gate duration, a smaller portion of the capacitor charging curve is used, and the capacitor charges to a lower potential. Consequently, the sweep amplitude decreases and the sweep linearity increases, since only the relatively small straight-line portion of the sweep is used.

Both the duration of the input gate and the setting of resistor R2 affect the sweep amplitude and linearity; therefore, resistor R2 is used to compensate for changes in sweep characteristics caused by changes in the input gate duration. Thus, resistor R2 can be adjusted to cause the circuit to produce a sawtooth output waveform of constant amplitude and linearity, even though the input gate duration changes.

## Failure Analysis.

**No Output** A no-output condition maybe caused by either lack of an input gate, lack of plate supply voltage, or a defective tube or circuit component. It is good practice to first check the input gate with an oscilloscope, and the plate-supply voltage with a high-resistance voltmeter, to determine that the trouble is definitely in the sweep generator circuit. If the correct input gate is observed and the proper plate-supply voltage is measured, use the oscilloscope to observe the waveform on the grid of triode VI. If no grid waveform is observed, either capacitor Cl is open or grid resistor **R1** is shorted. Use an in-circuit capacitor checker to check the capacitor, and an ohmmeter to check the resistor. The correct waveform on the grid of triode V1 indicates that the trouble is in the plate circuit (C2, R2, Vl) of the sweep generator. Check capacitor C2 for a short circuit with an in-circuit capacitor checker, and resistor R2 for the proper resistance value with an ohmmeter. If no defective component is found, triode V1 is probably at fault.

Distorted Output. Any defect in the circuit which causes capacitor C2 to charge for a greater than normal portion of the capacitor charging curve will cause a distorted sawtooth output wave. Possible causes of distortion are: A distorted input gate, incorrect plate-supply voltage, changes in the values of capacitor C2 and resistor R2 (including wrong adjustment of resistor R2), and low emission in triode V1. First, observe the input gate with an oscilloscope to be certain that no distortion is present, and then measure the plate-supply voltage with a high-resistance voltmeter to be certain that the supply voltage is correct. If the input gate and the plate-supply voltage are normal, further checks must be made to isolate the trouble. Use a capacitance analyzer to check capacitor C2 for the proper value. Use an ohmmeter to check resistor R2 for the correct value and setting. If these checks fail to locate a faulty component, triode V1 is probably at fault.

# BOOTSTRAP SWEEP GENERATOR (ELECTRON TUBE)

# Application.

The bootstrap sweep generator is used to produce an extremely linear sawtooth waveform for use in navigation equipment, radar test sets, and in other types of electronic equipment where an extremely linear sweep voltage is required.

#### Characteristics

Employs one triode as a switch tube, and another as a constant-current generator.

Uses positive feedback to produce the linear saw-tooth sweep.

Requires a negative input gate.

Output is a symmetrical sawtooth voltage waveform with equal intervals between sweeps.

Sweep time is determined by the duration of the input gate.

Sweep-repetition period is determined by the repetition period of the input gate.

# **Circuit Analysis.**

**General.** Most sawtooth sweep generator circuits use the charging action of a capacitor to produce a sawtooth waveform. By using only the initial portion of the exponential capacitor charging curve, a fairly linear sawtooth output waveform is produced. However, some nonlinearity (curvature) is present in the output waveform because even the initial portion of the capacitor charging curve is not perfectly linear. The bootstrap sweep generator uses a feedback loop to straighten out the **curvature** in the initial portion of the capacitor charging curve, and thus, to produce an extremely linear sawtooth waveform.

Before discussing the operation of the bootstrap sweep generator, it is necessary to review the charging action of an R-C circuit. The charge time of the capacitor in the R-C circuit is determined by the time constant of the circuit. At the first instant that a series R-C circuit is comected across a constant voltage source, the entire supply voltage appears across the resistor. As the capacitor charges, the voltage drop across it increases, and at the end of one time constant interval, 63 percent of applied voltage appears across the capacitor, and the remaining voltage (377.) appears across the resistor. During the next time constant, the capacitor further charges to 63 percent of the voltage remaining across the resistor, that is, to 86 percent of the total applied voltage. During each successive time constant, the capacitor charges to 63 percent of the voltage remaining across the resistor. Thus, as shown by the dashed line in the following illustration, the voltage across the capacitor rises exponentially toward the supply voltage as the capacitor charges.



Generation of a Linear Sweep

Although the capacitor theoretically never fully charges, after five time constants it is charged to over 99 percent of the supply voltage and is considered to be fully charged.

The voltage across the capacitor of a series R-C circuit increases at an exponential rate because the capacitor charges to 63 percent of the voltage across the resistor each time constant. Since the voltage across the resistor decreases as the capacitor charges, the capacitor charges a smaller amount each time constant, resulting in an exponential increase in the voltage across the capacitor charged, so that the voltage across the resistor remained constant, the capacitor would charge the same amount each time constant. This is, the voltage across the capacitor stant capacitor would in-crease at a linear (constant) rate. The bootstrap sweep

generator uses a feedback circuit to cause the effective supply voltage for the R-C circuit to increase as the capacitor charges. Thus, the circuit produces an extremely linear sweep, as shown in the sweep generation illustration.

**Circuit Operation.** The following circuit schematic illustrates one type of bootstrap sweep generator.



**Bootstrap Sweep Generator** 

The portion of the circuit made up of coupling capacitor Cl, grid resistor R1, switch tube V1, charging capacitor C3, and plate resistor R3 is a conventional basic triode sawtooth sweep generator. Triode V2 is a cathode follower which provides feedback to charging capacitor C3 **through** dc blocking capacitor C2. The input gate is applied through capacitor Cl to the grid of triode V1, and the output sawtooth waveform is taken from the cathode of triode V2 across cathode resistor R4.

In the quiescent state, no negative input gate is applied to the bootstrap sweep generator, and therefore, no bias is applied to triode V1. Consequently, the tube conducts very heavily, and the plate voltage is very low. Since capacitor C3 is in parallel with triode V1, it charges to the low value of plate voltage existing across the tube. The voltage across capacitor C3 also appears on the grid of triode V2 (because of the direct coupling from the plate of V1 to the grid of V2), and causes V2 to conduct. The plate current of triode V2 flows through cathode resistor R4 and causes a small, but constant, voltage drop across the resistor. So long as no input gate is applied the circuit remains in this quiescent state, and the output voltage across resistor R4 remains at the low quiescent value.

When a negative input gate is applied to the bootstrap sweep generator, it is applied through coupling capacitor Cl to the grid of triode V1. When the input gate is of sufficient amplitude to drive the grid of triode VI below plate-current cutoff, plate current ceases to flow, and the plate voltage tries to rise instantaneously to the plate-supply valve. However, capacitor C3 is connected in parallel with triode VI, and prevents the plate voltage from changing instantaneously. Instead, the plate voltage rises relatively slowly as the capacitor charges. Normally, capacitor C3 would charge exponentially at a rate determined by the values of resistance and capacitance in the circuit, as shown by the dashed line on the following theoretical waveform illustration.



**Theoretical Input end Output Voltage Waveforms** 

In the bootstrap circuit, however, the voltage across capacitor C3 is also applied to the grid of triode V2, which is connected as a cathode follower with almost unity gain. The changing voltage on the cathode of triode V2 (which is nearly equal to the voltage on the grid) is fed back through dc blocking capacitor C2 to the junction of plate resistors R2 and R3. This feedback loop operates in the following manner. As capacitor C3 charges positive with respect to ground, the voltage impressed on the grid of triode V2 also rises and becomes more positive. The increasing plate current flow through cathode resistor

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R4 causes the cathode voltage on triode V2 to increase, also in a positive direction. This increasing positive voltage is fed back through capacitor C2 to the junction of resistors R2 and R3, aiding the voltage across resistor R3, and effectively increasing the voltage applied to the R-C circuit. Thus, as capacitor C3 charges, the applied voltage is effectively increased so that the voltage appearing across resistor R3 remains constant, instead of dropping as the charge increases. Since the capacitor always charges to 63 percent of the voltage across the resistor in each time constant, and the resistor voltage remains constant, the capacitor charges the same amount each time constant, or in other words, at a linear rate.

When the negative input gate ends, the grid bias on triode VI returns to zero and the tube again begins to conduct heavily. The low impedance of the conducting tube effectively shunts (shorts) capacitor C3, and the capacitor discharges very quickly through the tube. As capacitor C3 discharges, the voltage on the grid of triode V2 decreases, causing the voltage on the cathode to decrease accordingly. The cathode voltage drops to the quiescent value, and the circuit remains in the quiescent state until the beginning of the next input gate.

Thus, the output voltage of the bootstrap sweep generator rises at a linear rate during the input gate, and returns quickly to the quiescent value at the end of the input gate. It remains at the quiescent level until the next gate is applied.

# Failure Analysis.

No Output. A defect in nearly any component in the bootstrap sweep generator may cause a no-output condition. Therefore, it is good practice to use an oscilloscope to locate the defective portion of the circuit. First, use the oscilloscope to observe the input gate to make certain that the proper input is applied. If the correct input gate is observed, use the oscilloscope to observe the signal on the grid of triode VI. No negative gate at this point indicates either an open in capacitor Cl or a short in resistor R1. Use an ohmmeter to check these components. If the normal waveform is observed on the grid of triode V1, observe the waveform on the plate of the tube. No signal on the plate of triode V1 indicates a defect in capacitor C3, resistor R2 or R3, or in the tube itself. If checking capacitor C3 with an in-circuit capacitor checker, and resistors R2 and R3 with an ohmmeter,

does not reveal a defective component, triode V1 is probably at fault. If the sawtooth waveform is observed on the plate of triode VI, the trouble is either a defective cathode resistor, R4, or a faulty cathodefollower tube, V2. Check resistor R4 with ohmmeter for the correct resistance value. If no defect is found, triode V2 is probably at fault.

Low Output. A sawtooth output of incorrect amplitude may be caused by low plate-supply voltage, or by a circuit defect which affects the charge time of capacitor C3. First, use a high-resistance voltmeter to measure the plate-supply voltage to be certain that the power supply is not at fault. If the correct platesupply voltage is observed, use a capacitance analyzer to check capacitor C3 for the proper value and an ohmmeter to check resistor R2 and R3 for the proper values. If no defective component is found, triode V1 is probably at fault.

Poor Linearity. If the linearity of the sawtooth output is poor, probably either capacitor C2 or resistor R4 is at fault. Use an in-circuit capacitor checker to check the capacitor for a shorted or open-circuited condition, and an ohmmeter to check the resistor for the correct value. If neither of these components is defective, triode V2 is probably at fault.

# **TRIODE** TRAPEZOIDAL-WAVE SWEEP **GENERATOR (ELECTRON TUBE)**

# Application.

The triode trapezoidal-wave sweep generator produces a trapezoidal waveform for use as the sweep voltage in television sets, radar equipment, test and other electronic equipment using electromagnetic cathode-ray tube displays.

#### Characteristics

Employs a triode as a switch to control the charge and discharge of a series R42 circuit to produce the output.

Requires a negative input gate.

Output is a series of trapezoidal waves.

Sweep duration and sweep-repetition period are determined by the characteristics of the input gate.

# **Circuit Analysis.**

General. The deflection coils of an electromagnetic cathode-ray tube require a sawtooth wave of current

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to produce a linear sweep across the face of the tube. Because of the inductance and resistance characteristics of the deflection coils, a trapezoidal voltage waveform must be applied across the coils to produce the desired linear sawtooth wave of current through them. The triode trapezoidal-wave sweep generator discussed below produces such a voltage waveform. Since the trapezoidal wave is essentially a sawtooth wave superimposed on a rectangular wave, the triode trapezoidal-wave sweep generator is similar to the triode sawtooth-wave sweep generators discussed previously in this section of the Handbook.

**Circuit Operation. The** accompanying circuit schematic illustrates one type of triode trapezoidal-wave sweep generator. In the quiescent state (with no input gate applied to the circuit), contact bias is applied to the grid of triode VI; consequently, the tube conducts very heavily. Since triode V1 conducts nearly at platecurrent saturation, the voltage drop across plate resistor R2 is very large and the effective plate voltage is wry low. Capacitor C2 charges through resistor R3 to the low value of voltage existing across the tube, and the circuit remains in this quiescent state so long as no input **gate** is applied. The quiescent output is the small constant voltage across capacitor C2.

A negative input gate, such as that shown in the following illustration of theoretical waveforms, must be applied to the circuit to produce a trapezoidal output waveform.



Triode Trapezoidal-Wava Sweep Ganaretor

Capacitor Cl and resistor R1 forma conventional R-C input coupling network used to couple the input gate to the grid of triode VI. Triode V1 acts as a switch to control the charge and discharge of capacitor C2. The charge time of the capacitor is determined by the time constant of the R-C circuit made up of resistors R2 and R3 connected in series with capacitor C2. The trapezoidal output waveform is taken from the plate of triode V1 (across the series combination of capacitor C2 and resistor R3).



#### **Theoretical Waveforms**

The negative gate is applied through coupling capacitor Cl to the grid of triode V1, and is of sufficient amplitude to drive the tube below platecurrent cutoff. Consequently, plate current ceases to flow, and the plate voltage attempts to rise instantaneously to the plate-supply value. However, since the series combination of capacitor C2 and resistor R3 is connected across the tube, the plate voltage

rises in accordance with the charging action of the R-C circuit made up of resistors R2 and R3 and capacitor C2. When triode VI first cuts off (time t. on the waveform illustration), only the small quiescent charge is present on capacitor C2, and the remain de r of the s u pply voltage appears instantaneously across the series combination of resistors R2 and R3. Thus, at time to, the voltage across resistor  $R3(e_R 3)$  rises instantaneously from nearly zero to a high positive value determined by the total resistance in series with capacitor C2 and the power supply. The voltage drop across resistor R3 produced by the initial flow of charging current to capacitor C2 determines the amplitude of the voltage step shown as e<sub>R 3</sub> at time t. in the waveform illustration. At the same time, capacitor C2 charges from the quiescent value to the effective plate voltage value, and the voltage across it  $(e_{\alpha})$  increases toward the plate-supply value. Though the capacitor charges at an exponential rate, only the initial (relatively straight) portion of the capacitor charging curve is used; therefore, the capacitor charge (from time  $t_0$  to time  $t_1$ ) is nearly linear. The output from the circuit is taken across the series combination of resistor R3 and capacitor C2, and is the sum of the voltages across these components. The output voltage, therefore, rises instantaneously from the quiescent value to a more positive value at the beginning of the input gate (time to), and then increases at a nearly linear rate until the end of the input gate (time t 1).

When the negative input gate ends (time  $t_i$ ), the grid bias on triode V1 returns to zero, and the tube again conducts heavily. The low impedance of the conducting tube effectively shunts (shorts) the series combination of resistor R3 and capacitor C2, and the capacitor discharges very quickly through the resistor and the conducting tube. As capacitor C2 discharges, the voltage across it decreases from maximum to the quiescent value. The voltage remains at this value until the beginning of the next input gate.

# Failure Analysis.

No Output. An incorrect input gate, a defective input coupling network (Cl, RI), an open plate resistor (R2), a defective tube (V1) or a lack of platesupply voltage may cause a no-output condition. First, use an oscilloscope to observe the input gate waveform to be certain that the correct input sigml is applied. If the normal input gate is present, observe the waveform on the grid of triode V1. No input gate at this point indicates either an open coupling capacitor (Cl) or a shorted grid resistor (Rl). Use an ohmmeter to check these components for defects. If the correct input gate is observed on the grid of triode V1, use a high-resistance voltmeter to measure the voltage on the plate of the tube. If no plate voltage is present, the trouble may be either a lack of platesupply voltage or an open plate resistor (R2). Measure the plate-supply voltage with the high-resistance voltmeter, and check resistor R2 with an ohmmeter. If the correct voltage is measured on the plate of triode V1, the tube is probably at fault.

**Distortad Output. An** output waveform with poor linearity or low amplitude may be caused either by a defective tube or by a change in value of resistor R2, R3, or capacitor C2. Use an ohmmeter to check the values of resistors R2 and R3, and a capacitance analyzer to check the value of capacitor C2. If no defective component is found, triode V1 is probably at fault.

**Incorrect Output Waveshapa.** An output waveform of sawtooth shape (with no initial step) will result if resistor R3 is shorted, while an initial step of incorrect amplitude indicates a change in value of resistor R3.

An output waveform of square-wave shape maybe caused either by an open or short-circuited condition in capacitor C2 or by an open in resistor R3. Use an ohmmeter to check resistor R3, and an in-circuit capacitor tester to check capacitor C2.

# SECTION 9 CRT CIRCUITS

# PART 9-1. ELECTROSTATIC

# ELECTROSTATIC CATHODE-RAY TUBE CIRCUITS

# General.

The circuits used for the electrostatic type of cathode-ray tube are functionally similar to those used for the electromagnetic type of tube, but they differ in the manner of accomplishing their function. Only the electrostatic type will be discussed in this paragraph. Basically, the cathode-ray tube provides a fast moving, easily and quickly deflected electron beam for use in waveform viewing and analysis, and for special display purposes. Generally speaking, the display types of CRT are mostly magnetically controlled, while the types universally used in test oscilloscopes and synchroscopes, for waveform checking, are electrostatically controlled. Therefore, the discussion in this paragraph will be restricted to oscilloscopes. Later paragraphs in this section will describe deflection-modulated display circuits such as used in type A and J scans, and intensity-modulated circuits such as the B and C types, which can employ an electrostatic CRT. All cathode-ray tubes have basic control circuits which are necessary if the tube is to be used at all. These circuits control intensity (brilliance), focus, and beam positioning (centering, both horizontal and vertical). Other circuits with which the CRT is concerned are horizontal and vertical amplifiers, sweep circuits, and synchronizing circuits. All of the latter circuits are standard circuits, with special attention paid to the design for bandwidth, response, and linearity. In some special cases there are peculiar circuits which are mainly combinations of standard circuits used for packaging the components into a convenient size, and for economy. For example, while a console unit may have high and low voltage supplies, they are usually separate and use separate transformers, whereas the conventional oscilloscope uses one transformer to supply both high and low voltage, bias, and filament power.

# BASIC ELECTROSTATIC OSCILLOSCOPE CIRCUITS

# Application.

The basic circuits described below are used to adapt an electrostatic CRT for use as an oscilloscope which can be utilized for waveform analysis.

# Characteristics.

Vertical input (Y-axis) High input impedance (approximately 2 megohms shunted by 40 picofarads) Step attenuator Good frequency response (10 Hz to 1 MHz) Horizontal input (X axis) High input impedance (approximately 2 megohms shunted by 40 picofarads) Step attenuator Internal sweep or external signal Sweep Selectable sync (polarity and input) Sweep frequency 2 Hz to 100 kHz Retrace blanking

Intensity input (Z axis)

# Circuit analysis.

**General. The** following circuits were chosen as basic examples of the circuits generally used in oscilloscopes. Each was selected to bring out the basic principles and requirements necessary for circuits used in waveform analysis, even though a similar circuit may be found elsewhere in this manual. The discussion is limited to the essentials needed for use with cathode-ray tubes.

**Beam-Positioning Circuits.** A simple oscilloscope using basic beam-positioning circuits is shown in the following illustration. For a complete schematic of an elementary oscilloscope, see Basic Electronics, NAVPERS IO087A. Note that the voltages are taken from a common voltage divider between B+ and B–. The divider is grounded at a convenient point, usually at the positive voltage required for the accelerating anode (No. 2), and both ends are above' ground. Thus,

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# **CRT CIRCUITS**

with the positive low voltage and negative high voltage at above-ground potential, the case and chassis can be grounded for protection of the operator. It also permits the anode and one of each pair of deflection plates to be grounded, to form a simple unbalanced deflection or positioning circuit. This connection also keeps the deflection plates and accelerating anode at the same potential, and avoids defocusing effects from differences in potential between them.



# Simplified Oscilloscope, Showing Controls

It is evident from the schematic that resistors R4, RS, R6, R7, and **R8** form a voltage divider from B minus to ground, and at the junction of R4 and R5 some positive voltage exists. Since the cathode of the CRT is connected at a less negative point on the divider than the grid, the grid is negative with respect to the cathode, and is adjustable by means of potentiometer R8. As in the conventional circuits, variation of this grid bias permits the tube to conduct more or less heavily, as desired. Anode No. 1 is connected to a much lower point on the divider; thus it is effectively much more positive than the cathode and grid, and attracts the electrons from the cathode. By varying the dc potential on this focusing anode, the electron beam from the cathode is directed so that it converges at a point on the face of the CRT. Anode No. 2 of the CRT is grounded; thus, since it is at a more positive voltage than the focusing anode, it attracts the electron beam and accelerates it. The accelerating

anode is a concentric ring similar to the focusing anode and the focused beam passes through the center, losing only stray unfocused electrons. The No. 2 anode current, therefore, is minute, and does not detract from the beam. As the beam passes from the accelerating anode to the face of the tube, it passes between two sets of deflecting plates. The plates of the set nearest the No. 2 anode are positioned horizontally above and below the tube centerline, and deflect the beam vertically. (The vertical deflection plates are physically located nearest the No. 2 anode, for maximum control of the electron beam.) The \_ plates of the second set are nearest the face of the tube; they are positioned vertically to the left and right of the centerline of the tube, and deflect the beam horizontally.

Positioning controls R2 and R3 are parallelconnected, and are connected between B+ and ground through R1 and R4. Since one of each pair of deflecting plates is connected to ground, a dc positioning voltage exists between the plates and ground. Thus, by adjusting the positive voltage on R2 and R3, the electron beam is attracted (deflected) toward them and can be centered on the tube face. A simplified version of the positioning circuits is shown in the following figure; since one of each set of deflecting



#### **Unbalanced Positioning Circuit**

plates is connected to ground, the circuit is unbalanced. Controls RI and R2 are represented simply as variable potentiometers between B+ and ground. A simplified positioning circuit of the balanced type is shown in the accompanying illustration, and is discussed below.

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**Balanced Positioning Circuit** 

In the balanced circuit, each deflecting plate (D1 through D4) is controlled by a separate potentiometer (R2, R3, R6, and R7), and the plates are isolated and balanced equally by being connected to the positioning controls through equal resistors RI, R4, RS, and R8. Each plate is also connected to the deflection amplifiers, through a coupling capacitor, in a pushpull arrangement. Thus the CRT is balanced for dc, for ac, and for any stray capacitance to ground. Since the isolating resistors (RI, R4, R5, and R8) are always of a very large value, the deflecting plates may be connected into any circuit without danger to the operator (it takes a current of only a few microampere to drop the positioning voltage to zero).

**Power Supply.** A typical power supply for an elementary oscilloscope is shown in the illustration. Two fullwave rectifier tubes are used with a single transformer to supply a positive low voltage for circuits other than the CRT and a negative high voltage for the CRT. The low-voltage supply is a conventional full-wave rectifier circuit with the center tap grounded, and  $B_+$  is taken from the cathode and applied to a single pi-type C-L falter (Cl, Ll, and C2). The negative high-voltage supply uses the other **full**wave rectifier tube **(V2)**, with the plates parallel-connected as a half-wave rectifier, and the low-voltage center tap used as a common ground. Because of the small amount of current taken by the CRT, the simple R-C **filter** offered by the bleeder and C3 is

sufficient for hum elimination. The low-voltage output is on the order of 400 volts, and the high-voltage output is about 1000 volts. The filament windings for the CRT, as well as the other tubes, are also included on the same transformer, providing a compact and economical power supply.



**Typical Power Supply** 

Sweep Circuit. To provide a time base for the waveform, the CRT beam must be deflected horizontally across the face of the tube from left to right, then caused to return quickly from right to left, ready to resume another cycle of operation. A sweep voltage obtained by the charge and discharge of a capacitor is employed for this purpose. During the charging period the sweep is developed and the beam moves from left to right; during the discharging period the capacitor reverses polarity of deflection and the beam moves back to the start (retrace time). Some oscilloscopes provide blanking for the retrace period so that the return sweep camot be seen. A typical thyratron type sweep generator for general oscilloscope use is shown in the following illustration. Other types of relaxation oscillators, such as a neon tube, a vacuum tube R-C oscillator with discharge tube, or a multivibrator, could be used, provided that a reasonably linear sawtooth sweep waveform is produced.

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**Typical Sewtooth Generator (Thyratron)** 

Thyratron tube VI operates as a relaxation-type oscillator at frequencies from 5 to 100,000 Hz. The frequency of operation is selected roughly by S1, which connects various values of capacitance between the cathode and plate of the tube. The frequency of operation is adjusted finely by variable resistor R6, which, together with R5 and the capacitor selected by S1, provide a specific frequency fixed by the time constant of the R-C circuit. R5 primarily determines the amplitude over the range adjustable by R6 for a specific supply voltage. Normally, the circuit starts in an inoperative condition with the cathode fixedbiased by voltage divider R3 and R4, and capacitors C2, C3, or C4 (as selected by S1) charge slowly at a rate determined by the setting of R6. When the voltage between the cathode and plate reaches the ionization voltage (value depends upon type of gas used), the tube fires. Heavy current flows from the cathode to the plate and effectively produces a short-circuited condition across the capacitor selected by S1. Thus, the capacitor quickly discharges until the deionization voltage is reached and the tube stops conducting, resting in a biased-off condition, and the cycle of operation resumes again. During the charging period, blanking capacitor C6 is also charging slowly and reduces the CRT bias, allowing operation. When V1 conducts, C6 discharges through a grid-cathode resistor in the CRT circuit, and the common bleeder,

biasing the CRT off and blanking off the retrace interval.

Capacitor Cl is a coupling capacitor which applies the sync signal between R1 and ground; the amount of synchronizing signal fed to the grid of VI is adjusted by the position of RI. Resistor R2 is a protective resistor which limits grid current flow to a safe value; it also acts as a decoupling resistor. Capacitor C5 bypasses cathode resistor R4 to prevent degenerative feedback during sweep operation, and effectively shunts R4 so that it is not a part of the R-C time constant circuit.

Synchronizing Methods. To keep the waveform stationary on the face of the CRT tube, the sweep frequency must be an exact multiple or submultiple of the waveform under observation. To avoid the need for constant resetting of the sweep frequency control because of drift, power-supply voltage changes, etc, a sweep-locking or synchronizing circuit is provided. In the basic unit, a three-position switch is generally provided to permit selection of either an external signal, a 60-Hz signal, or the internal sweep (or input signal) taken from the verticrd deflection amplifier plate. Since some circuits do not have an output of the proper polarity for synchronization, an adjustable synchronizing circuit is sometimes included to permit selection of sync signal and choice of sync polarity. The following illustration shows a typical sync-input circuit of this type. Switch S1 selects one of three inputs: an external synchronizing signal, a 60-Hz signal (usually taken from a filament winding), or the output from the vertical amplifier (this is the signal under observation, but it is called interrrul sync); it then applies the input through coupling capacitor Cl to the grid of V1. Tube V1 is a paraphase amplifier, with the grid returned to ground through R1. The tube is cathode-biased and unbypassed; the plate and cathode resistor, R2 and R3, are of the same value, so that for the same current identical signals are developed in the plate and cathode circuits (except that the polarity of one is opposite the polarity of the other). For a positive input signal, a negative plate-output signal is developed, and the cathode-output signal is positive. For a negative input signal, a positive plate-output signal is developed, and the cathode is negative. Both plate and cathode outputs are coupled through capacitors C2 and C3 to a common load resistor, grounded at its center tap and also variable. At the ground position both signals are

equal and opposite, and of zero amplitude; therefore, no output is obtained. As R4 is rotated in either direction, the signal amplitude is increased. Since the synchronizing signal to the sweep generator must be of positive polarity, for a negative input to VI a positive signal is available on the plate side, and for a positive input to V1 a positive signal is available on the cathode side. Thus a signal similar to the input signal but of positive **polarity** is obtained and coupled through C4 to the thyratron sweep generator discussed above. When this paraphase input is supplied, the sweep generator **has** a **fixed** grid resistor instead of the **variable** one shown in the illustration of the thyratron sweep generator.



**Typical Sync Input Circuit** 

When the sweep generator is adjusted to a slightly lower frequency than that desired, a positive-going sync signal applied to the grid of the thyratron will cause ionization to occur earlier in the operating cycle. Since this has the effect of changing the ionization potential, the frequency of operation is increased and the sweep generator locks-in and operates at the same frequency as the sync signal. Thus the CRT waveform remains stationary, rather than drifting across the screen, because it is synchronized so that the sweep occurs at the same place at the same time each sweep.

**Deflection Amplifiers.** To produce satisfactory deflection with small signals, it is necessary to employ both vertical and horizontal deflection ampli13ers. These stages may be single-ended or push-pull (unbalanced or balanced); they are conventional video

amplifiers designed for the desired frequency response and linearity. A simple equipment usually provides only one stage of **amplification** and an output stage, whereas a laboratory-type equipment provides two or three stages of amplification with output stages.

The horizontal amplifier in a good scope is identical to the vertical amplifier, permitting the same signal to be applied to the X axis and the Y axis. In the majority of oscilloscopes, however, only the horizontal sweep is amplified; thus less gain is needed since the sweep output voltage is large. Because the sweep is usually a submultiple in frequency of the observed signal, less frequency response is needed. Thus the horizontal deflection amplifier need not be described, since the vertical amplifier has more stringent requirements.

Since the vertical amplifier must be able to amplify very weak signals with sharp rising waveforms, it must have good frequency response and large amplification. To cover the range of signal amplitudes encountered, the vertical input is usually provided with an attenuator. Simple potentiometer-type attenuators are shown in the accompanying figure. The simple circuit shown in part A of the illustration uses the potentiometer as the output load resistor of an R-C coupling network. Thus, since the grid-toground impedance  $(Z_g)$  of the input tube is in shunt



**Potentiometer Attenuators** 

across it, as the potentiometer arm is moved upward the impedance presented to the circuit under test is decreased (less loading and less attenuation). The simple step-attenuator circuit shown in part B of the illustration is a better type of input circuit, allowing coarse selection of the attenuation ratio with switch Sl, and fine adjustment with potentiometer R3. It is evident that even for the smallest input step resistance, the full range of R3 is available for control. With the available settings of S1, the input impedance will never decrease to a value less than the series section of R2 (that portion above the upper tap) plus the parallel combination of the remainder of R2, R3, and the grid-to-ground impedance of the input tube. The most desirable input is in the range of megohms, with little or no shunting capacitance to ground. To achieve this result sometimes a cathode follower input stage is combined with a step attenuator to isolate the oscilloscope input from the stage being tested. The usual input capacitance is on the order of 30 picofarads, which can be appreciable (1000 ohms at 5 MHz). Therefore, frequency-compensated attenuators are used in the better type of oscilloscopes to minimize the effect of input capacitance (as shown in the figure), by presenting identical impedanceresponse curves to the circuit under test for the various attenuator settings.



Frequency-Compensated Step Attenuator

Frequency-compensated attenuators further provide the same voltage division ratio (resistive to reactive) of the input signal, so that the drop-off in signal level at the higher frequencies can be compensated for in the following video amplifiers. Attenuator compensation is usually effective over the entire useful frequency range of the oscilloscope. The attenuator potentiometer is frequency-sensitive because of the distributed and stray capacitance from the moving **arm** of the potentiometer, the wiring and circuit elements, and the electron tube input capacitance to ground. While the resistance of the potentiometer must be as high as possible to maintain maximum input impedance, the greater the resistance, the greater the effect of the stray capacitance. Since there is only one setting of the attenuator arm where the resistance division and the capacitance division are of the same ratio, shunt capacitors Cl and C2 are added to the attenuator, as shown in the illustration, to provide frequency compensation. When the attenuator (S1) is set to position 2, the input to the amplifier is reduced to one-tenth of the total signal across the voltage divider. R2 is then one-tenth of R1 plus R2. The ratio of the capacitive reactance is then chosen to be of the same order. That is, the reactance of C2 and the stray capacitive reactance of C3 is made to be one-tenth of the total reactance of Cl in series. with the parallel combination of C2 and C3. Normally, because of the difficulty in measuring the stray capacitance indicated by C3, Cl is made variable and is adjusted during operation to produce the best compensation effects, using a square-wave input (this is made initially and once calibrated requires only an occasional check).

Since most attenuators and amplifiers have reduced high-frequency response because of the shunting effect of stray capacitance, a parallel R-C circuit in series with the input lead is usually inserted to boost the relative response of the attenuator at high frequencies. Another device is an input probe located at the end of a special connecting cable which applies the input to the vertical amplifier. The probe houses a frequency-compensated voltage divider, and is constructed to reduce to a minimum the amount of shunt capacitance existing at its input terminals. This is usually called a "DC probe", or simply "input probe", as distinguished from an "r-f probe", which contains a diode rectifier to remove the modulation.

A typical three-stage vertical amplifier is shown schematically in the accompanying illustration; it

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# Vertical Deflection Amplifier

drives a conventional push-pull paraphase deflection output amplifier (see the Amplifier Section of this Handbook for a discussion of deflection output amplifier stages). The vertical input signal is applied through blocking and coupling capacitor Cl to a cathode follower attenuator stage incorporating triode V1. The attenuator is a two-step, frequencycompensated type. For signals under 25 volts, S1 connects the input directly to the grid of V1. For signals over 25 volts, C2 is adjusted so that the time constant of the circuit consisting of C2 and RI is the same as the time constant of the circuit consisting of C3 and the parallel combination of R2 and R3, including the stray grid-to-ground capacitance of VI. Thus the attenuation in this position of S1 is practically constant for all frequencies. The constants are so proportioned that the input impedance is approximately 2 megohms for either position of the attenuator, with an effective shunt input capacitance of about 40 picofarads. Although V1 has its cathode connected to the

-280-volt supply, the plate current flow through R4 and R5 is sufficient to bias the cathode positive with respect to ground. The output of cathode follower V1 is taken from the cathode through C5, which is a large capacitor (on the order of 8 microfarads), and applied to the input gain potentiometer, R6. Capacitor C4 is a conventional filter capacitor to bypass the negative supply. Y-gain (vertical) control R6 controls the amplitude of the input signal to the two-stage, high-gain compensated video amplifier consisting of V2 and V3. Both high-frequency and low-frequency compensation are employed in each stage. The cathode of V2 is bypassed by a small capacitor, which makes it degenerative for low frequencies, thus reducing the response and flattening out the low-frequency response. Low-pass R-C falters R8, C7 and R9, C1O offer a high impedance to the low frequencies and a shunt path to the high frequencies in the plate circuits of the amplifiers. Thus the effective load impedance at low frequencies is increased, which

compensates for the normal drop off at about 30 Hz, and extends the response down to 2 Hz. The highfrequency response is increased by peaking coils L1 and L2, which compensate for the shunting effect of tube and wiring capacitance, providing a reactance which increases with frequency. The use of the peaking coils extends the response up to about 1 MHz. To help improve the high-frequency response, plate load resistors R7 and RIO are made low in value to reduce the shunting effect of stray capacitance. To improve the low-frequency response, the time constants of R-C coupling networks C8, R11 and C9, R15 are long (on the order of 1 second). Amplifier V3 is fixedbiased by connecting the cathode to the junction of R13 and R14, which are connected in series between the plate supply and ground. Cathode resistor R14 is also unbypassed so that the circuit is completely degenerative for high and low frequencies, further improving the over-all frequency response. The use of the fixed cathode bias sets the operating point of V3 and helps stabilize the stage. An output from the cathode of V3 is taken for application to the sync circuit for internal synchronization. The output of V3 is fed to cathode follower output stage V4, which is biased positive with respect to ground by plate current flow, even though the cathode is returned to the minus supply. Variable potentiometer R16 serves as an output and positioning control for the following paraphase amplifier. The paraphase **amplifier** is similar to those described in the Amplifier Section of this Handbook; therefore, it is not further discussed here.

# Failure Analysis.

Beam-Positioning Circuits. Usually, a control circuit failure is indicated by loss of a specific control function, and can be quickly verified by a resktance or voltage check. It must be understood that all controls affect the electron beam in some manner, and that the controls are interacting. For example, increasing the intensity of the beam will also thicken the beam and require a readjustment of the focus control for the thinnest line at that intensity. Likewise, a change in accelerating anode potential will cause a change in spot diameter and the maximum intensity available. Where high humidity and excessive moisture prevail, control failures from insulation breakdown, are usually more prevalent because

of the high potential involved, which causes a short circuit to ground.

Power Supply Circuits. Because of the high negative potentials used for operation of the CRT electron gun, the oscilloscope power supply is particularly susceptible to flash-over, particularly in damp and humid locations. A voltage check is usually sufficient to reveal the location of the trouble.

Sweep Circuit. Failure of the sweep circuit is evident by a lack of horizontal deflection, assuming that the beam positioning and adjusting circuits operate. A nonlinear sweep produced by changes in value or failure of components will show itself as a crowding together (or an expansion) of the waveform at the ends (or in the middle), particularly when a known linear waveform is observed. Distortion which results from the application of an excessive amplitude of sync pulse to the synchronizing circuit should not be confused with sweep nonlinearity. Most sweep troubles can be corrected by replacement of defective electron tubes, although there may be an occasional component failure. Where thyratron or other gas tubes are used, it may be necessary to try two or three tubes before obtaining one that will operate properly. Even with vacuum-tube sweep circuits, tube selection may be necessary.

Synchronizing Circuits. When the sync pulse amplitude is insufficient, or is of the wrong frequency or polarity, synchronization will not be obtained. With internal synchronization, lack of signal to the synchronizing circuit can occur from poor switching contacts or by failure of any component in the sync circuit. Wrong polarity can occur with external sync, but not with internal sync. Incorrect sync amplitude is compensated for by adjusting the input control. In the case of the controllable sync amplifier, only a shorted or open component or a bad tube can cause difficulty. A resistance check should quickly reveal the trouble. False synchronization is possible with unstable operation due to improper setting of the sync and fine tuning controls. Over synchronization results from too large a synchronizing pulse, and causes distortion of the waveform under view. Reduction of the sync input will return the circuit to normal. The effects of poor voltage regulation may also result in apparent instability, but this is the fault of primary transients rather than sync circuit action. This type of instability is usually recognized easily as it is usually

# **ELECTRONIC CIRCUITS**

coupled with constant fluctuations of the CRT presentation up or down and to the right or left, or by a constant jittering of the pattern.

Deflection Amplifiers. Lack of output can be caused by failure of components or an electron tube, and can quickly be isolated by using another oscilloscope to check the signal from grid to plate through the amplifier for the point of signal disappearance. In most oscilloscope amplifiers, it is possible to have the circuit operating, but producing false indications because of failure of the compensating circuits. Use of a square-wave input will quickly determine whether the circuit is rounding off the peaks because of the lack of highs, or drooping at the top because of bad lowfrequency response. Comparison of the same waveform on another scope which is in good condition is the best method of determining performance.

# SYNC HROSCOPE

# Application.

A synchroscope is a waveform measuring device very similar to an oscilloscope, only it is used primarily for observing pulse waveforms of short duration.

# Characteristics.

Vertical Input.

Variable input impedance - may be matched

with the output impedance of the signal source.

Vertical input delayed before being applied to vertical plates.

Sync Input.

Variable input impedance

Sweep only generated when a sync signal is present.

Sync signal may be internally or externally originated.

Cathode Ray Tube

Electrostatic - uses medium persistence phosphor.

# Circuit Analysis.

**General. The** following circuits were chosen as basic examples of circuits commonly used in synchroscopes. Each circuit was selected to bring out the basic principles and requirements necessary for circuits used in non-repetitive waveform analysis, even though similar circuits may be used in other sections of the manual. The circuit discussion is limited to essentials needed for cathode tube displays.

**Beam-Positioning Circuits.** A basic beampositioning system used in a synchroscope, using a balanced deflection network, is shown in the following illustration.



Simplified Synchroscope CRT Control Circuits

The voltages for **the** CRT electrodes are taken from a common voltage divider between the negative voltage supply and ground. The voltage divider is grounded at the positive voltage required for the accelerating anode, while the cathode is operated at a high negative potential with respect to ground, the low voltage is operated above ground. Thus, with the positive low voltage and negative high voltage at above ground potential, the case and chassis can be grounded for the protection of the operator.

It is evident from the schematic that resistors R1O, R11, R12, R13, and R14 form a voltage divider from the junction of the negative supply to ground, and at the junction of R1O and R11 some positive voltage exists. The control grid is supplied with a positive unblinking pulse, produced by the start-stop sweep generator, which enables the CRT to conduct. As in conventional circuits variation of the voltage on the grid permits the CRT to conduct more or **less** heavily. Anode no. 1 is connected to a much lower point on the divider; thus it is effectively much more positive than the grid and cathode, and attracts the electrons from the cathode. By varying the dc potential on this focusing anode, the electron beam from the cathode is directed so that it converges at a point on the face of the CRT. Anode no. 2 of the CRT is grounded; thus, since it is at a more positive voltage than the focusing anode, it attracts the electron beam and accelerates it. The accelerating anode is a concentric ring similar to the focusing anode, and the focused beam passes through the center, losing only stray unfocused electrons. The second anode current, therefore, is minute and does not detract from the beam. As the beam passes from the accelerating anode to

# **ELECTRONIC CI RCUITS**

the face of the tube, it passes between two sets of deflection plates. The plates of the set nearest the second anode are positioned horizontally above and below the tube centerline, and deflect the beam vertically. The plates of the second set are nearest the face of the tube, and deflect the beam horizontally.

Each deflecting plate (Dl through D4) is controlled by a separate potentiometer (R3, R4, R7, R8), and the plates are isolated and balanced equally being connected to the positioning controls through equal resistors R2, R5, R6, and R9. Each plate is also connected to the deflection amplifiers, through a coupling capacitor, in a push-pulf arrangement. Thus the CRT is balanced for dc, for ac, and for any stray capacitance to ground. Since the isolating resistors (R2, R5, R6 and R9) are always of a very large value, the deflecting plates may be connected into any circuit without danger to the operator (it takes a current of only a few microampere to drop the positioning voltage to zero).

Power Supply. Refer to the discussion of a typical power supply circuit in the previous discussion of Basic Oscilloscope Circuits in this section of the Handbook.

Horizontal (Sweep) Channel. There are two types of sync signal input available at the input of the horizontal channel. A positive pulse derived from the signal input may be taken from the coupling amplifier, or some external sync may be applied from an external source.

With the sync switch in the int. sync position, a positive pulse (taken from the coupling amplifier) is applied to the sync pulse **amplifier**, where it is inverted, amplified, and formed into a sharp spike. The circuit used to develop this spike is shown in the following illustration. The positive pulse is applied through capacitor Cl to triode V1, where it is inverted and amplified at the plate. The variable potentiometer RI determines the amount of amplification of the signal. The sync pulse is coupled through capacitor C2 and resistor R3, which develops a differentiated form of the negative rectangular pulse. The output is taken from across R3 in the form of a negative spike occurring at the pulse input frequency.



Sync Pulse Amplifier

The typical sweep generator is a start-stop multivibrator, shown in the following illustration. This circuit is a cathode coupled type of start-stop multivibrator, with the grid of VI at a high positive potential and the grid of V2 at a high negative bias value, so that V1 is normally conducting heavily and V2 is normally cutoff. With the application of the negative input pulse, V1 is cut off and V2 is brought to maximum conduction for a period of time determined by the time constant of the circuit. This time constant is dependent on the values of R2, Cl and R4, C2. The resulting output, taken from the plate of VI, is a positive rectangular pulse obtained during the time that V1 is not conducting. Besides using the rectangular output for unblinking the CRT during the period that the input signal is to be viewed, the rectangular output pulse is applied to an RC circuit (R5 and C3) where it is integrated. A sawtooth output is then obtained from C3, which has the same duration as the unblinking pulse. This sawtooth is applied to drive the output sweep amplifier shown in the following illustration. The output sweep amplifier is a paraphase push-pull type of amplifier which produces a

sawtooth waveform from each output, equal in amplitude but of opposite polarity. The single input (driving) sawtooth is applied through Cl to the grid of VI where it is amplified and inverted. The output of V1 is applied to the grid of V3 and across voltage divider R5 and R6, connected from output to ground. The voltage dropped across R5 is applied to the grid of V2. Since the input of V2 is 180" out of phase with the input of VI, the outputs of VI and V2 are likewise 180° out of phase. The outputs of V1 and V2 are applied to V3 and V4, respectively, where these outputs are amplified and supplied to opposite horizontaldeflection plates in the CRT to produce a balanced deflection of the electron beam (detailed description of the operation of paraphase amplifiers can be found in the Amplifier Section of this Handbook).



Paraphase Push-Pull Amplifier



Start Stop Sweep Generator

**Vertical Channel. The** signal input is applied to the vertical charnel through an input impedance selector circuit, which is used to match the output impedance of the signal source to the input impedance of the coupling **amplifier.** A typical, simplified, input impedance selector circuit is shown in the accompanying illustration.

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Input Impedance Selector Circuit

This circuit uses a typical tetrode input amplifier, with the input signal being coupled to the control grid of V1 across an input voltage divider consisting of variable resistor R1 and fixed resistor R2. The variable resistor provides both a means of attenuating the input signal, and a method of supplying a variable input impedance for the synchroscope; while fixed resistor R2 determines the minimum input impedance to VI. Together this resistive input arrangement facilitates matching the input impedance of VI, to the impedance of the signal source. Resistors R3, R4, and R5 are different values of cathode bias resistors. These different values are selected by a switch to provide a large range of attenuation for the input signal by changing the input bias. Capacitors Cl, C2, and C3 are conventional cathode bypass capacitors associated with these cathode resistors. Besides providing a variable input impedance, and a large attenuation range, the input selector circuit provides high amplification with undesired inversion of the input signal at the plate of VI. Therefore, another amplifier stage (V2) is provided to supply an additional 180° phase shift, so that the output of stage V2 is in phase with vertical input signal. The output of the input impedance selector circuit is applied to a coupling amplifier.

The coupling amplifier, shown in the accompanying illustration, has two functions.

One function is to supply a pulse to the synchronizing pulse amplifier when internal sync is used. This sync pulse, which is the inverted and amplified input to the coupling amplifier, is obtained at the plate of Vl, and is coupled through an Int-Ext. sync switch to the sync (pulse) amplifier. The pulse then serves as a trigger for the start-stop sweep generator.

The second function of the coupling amplifier is to act as a cathode follower, providing an impedance match for the low-impedance input of the delay network. This input is the uninvested signal pulse obtained at the cathode of **V1** without amplification. A potentiometer is used for R2 instead of a fixed cathode resistor. The potentiometer setting determines the amplitude of the pulse obtained at the cathode of V1. This potentiometer functions as a vertical image size control.

The pulse obtained at the cathode of the coupling **amplifier** is applied to a delay network, which prevents the pulse from causing a vertical deflection of the electron beam until shortly after the sweep has started. (A typical delay time is  $1/2 \mu$  sec.). An accompanying illustration shows a delay network which

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**Delay Network** 

may be used. It is composed of series inductors and shunt capacitances terminating in a resistor having an ohmmic value equal to the total impedance value of the foregoing inductors and capacitors. The delay effect is due to the fact that each capacitor retards the voltage from appearing across it, and each inductor retards the current from flowing through it. The terminating resistor minimizes reflections of standing waves. (Standing waves upset the normal function of the delay line and introduce error).

The delayed signrd is coupled through a signal attenuator, which is a tapped voltage divider, to the vertical amplifier. A typical attenuator is shown in the following illustration.



Signal Attenuator

This attenuator is frequency compensated to reduce the distributed and stray capacitance of this circuit and the following circuit. Frequencycompensated attenuators further provide the voltage division ratio (resistive and reactive) of the input signal, so that the loss in signal level at the higher frequencies can be compensated for in the following amplifiers. Attenuator compensation is usually effective over the entire useful frequency range of the scope. When a potentiometer type of attenuator is used, the attenuator potentiometer is frequencysensitive because of the distributed and stray acitance from the moving arm of the potentiometer, the wiring and circuit elements, and the electron tube input capacitance to ground. While the resistance of the potentiometer must be as high as possible to maintain maximum input impedance, the greater the resistance, the greater the effect of the stray capacitance. Since there is only one setting of the attenuator arm where the resistance division and the capacitance division are the same ratio, shunt capacitors Cl and C2 are added to the attenuator, as shown in the illustration to provide frequency compensation. When the attenuator (S1) is in position 2, the input to the amplifier is reduced to one-tenth of the total sigml across the voltage divider. R2 is then one-tenth of RI plus R2. The ratio of the capacitive reactance is then chosen to be of the same order. That is, the reactance of C2 and the stray capacitive reactance of C3 is made to be one-tenth of the total reactance of Cl in series with the parallel combination of C2 and C3. Normally, because of the difficulty in measuring the stray capacitance indicated by C3, Cl is made variable and is adjusted during operation to produce the best compensation effects, using a square-wave input (this is made initially and once calibrated requires only an occasional check).

Since most attenuators and amplifiers have reduced high-frequency response because of the shunting effect of stray capacitance, a parallel R-C circuit in series with the input lead is usually inserted to boost the relative response of the attenuator at high frequencies.

A typical three-stage vertical amplifier is shown in the following illustration; it drives a push-pull paraphase deflection output amplifier, similar to the one used as the horizontal sweep amplifier.



#### vertical Amplifier

Although VI has its cathode connected to a negative high voltage supply, the plate current flow through R1 and R2 is sufficient to bias the cathode positive with respect to ground. The output of cathode follower V1 is taken from the cathode through C2, which is a large value capacitor, and applied to an input gain potentiometer R3. Capacitor C3 is a conventional filter capacitor used to bypass the negative supply. Vertical gain control R3 controls the amplitude of the input signal to the two-stage, high-gain compensated video amplifier consisting of V2 and V3. Both high- and low-frequency compensation are employed in each stage. The cathode of V2 is bypassed by a small capacitor, which makes it degenerative for low frequencies, thus reducing the response and flattening out the low-frequency response. Lowpass R-C falters R5, C5, and R6, C6 offer a high impedance to the low frequencies and a shunt path to the high frequencies in the plate circuits of the amplifier. Thus the effective load impedance at low frequencies is increased, which compensates for the normal drop off, and extends the low frequency response. The high-frequency response is increased by

shunting effect of tube and wiring capacitance, providing a reactance which increases with frequency. To help improve the high-frequency response, plate load resistors R4 and R7 are made low in value to reduce the shunting effect of stray capacitance. To improve the low-frequency response, the time constants of R-C coupling networks C7, R8 and C8, R12 are long. Amplifier V3 is fixed-biased by connecting the cathode to the junction of R1O and R11, which are connected as a voltage divider in series between the plate supply and ground. Cathode resistor R11 is also unbypassed so that the circuit is completely degenerative for high and low frequencies, further improving the over-all frequency response. The use of a fixed cathode bias sets the operating point of V3 and helps stabilize the stage. The output of V3 is fed to cathode follower output stage V4, which is biased positive with respect to ground by plate current flow, even though the cathode is returned to the minus supply. Variable potentiometer R13 serves as an output and positioning control for the following paraphase amplifier.

peaking coils L1 and L2, which compensate for the

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# Failure Analysis.

Beam-Positioning Circuits. Usually, a control circuit failure is indicated by loss of a specific control function, and can be quickly verified by a resistance or voltage check. It must be understood that all controls affect the electron beam in some manner, and that the controls are interacting. For example, increasing the intensity of the beam will also thicken the beam and require a readjustment of the focus control for the thinnest line at that intensity. Likewise, a change in accelerating anode potential will cause a change in spot diameter and the maximum intensity available. Where high humidity and excessive moisture prevail, control failures from insulation breakdown are usually more prevalent because of the high potential involved, which causes a short circuit to ground.

**Power Supply Circuits. Because** of the high negative potential used for operation of the CRT electron gun, the synchroscope power supply is particularly susceptible to flash over, particularly in damp humid locations. A voltage check is usually sufficient to reveal the location of the trouble.

Horizontal (Sweep) Channel. A failure in the horizontal channel can be due to a failure of any of the individual circuits comprising the channel as well as two circuits within the vertical channel. If the input impedance selector and the coupling amplifier, the two circuits within the vertical channel, are the cause of the sweep faihrre; the vertical deflection will also be defective as well as the sweep. If this is the case, voltage and waveform checks, made by a voltmeter and an oscilloscope will reveal the location of the faulty component within the two circuits. If, however, there is no trouble with the vertical deflection and faulty sweep exists, the trouble exists within the three horizontal channel circuits. Beginning with the sweep amplifier, the inputs should be checked with a voltmeter and an oscilloscope. If the proper input exists the trouble is within this circuit. If an improper input exists check the input of the start-stop sweep generator with an oscilloscope. If the input is proper the trouble must exist in the start-stop sweep generator. Voltage and waveform checks with a voltmeter and an oscilloscope will reveal the location of the faulty component. If the input to this circuit is **proper**, check the input to the sync (pulse) amplifier. If the coupling amplifier is working properly and the sync selector switch is functioning properly, the trouble should be within the sync (pulse) amplifier. Voltage and waveform checks with a voltmeter and oscilloscope will reveal the faulty component.

Vertical Channel. A failure in the vertical channel is characterized by improper amplitude of the presentation of the pulse on the synchroscope screen. There are six circuits which could result in the vertical charnel failure. Two of these, the input impedance selector, and the coupling amplifier, produce sweep failure. The trouble shooting of these circuits has already been mentioned. The other four circuits of the vertical channel, the push-pull paraphase amplifier, the vertical amplifier, the signal attenuator, and the delay network, affect only the vertical display of the scope. If the failure exists in the delay network, the vertieal deflection will not occur at the proper time interval with respect to the sweep. If this effect is apparent on the display, check the delay network with an oscilloscope to determine where the improper waveforms or voltages exist. If the failure exists in the push-pull paraphase amplifier the vertical position of the display on the CRT screen is improper. If this is apparent on the display check the voltages and waveforms of the push-pull paraphase amplifier with an oscilloscope to determine where the faulty component is located. If these circuits of the vertical channel have been checked and found to be operating properly, and trouble still exists in the vertical display, the trouble must exist in the signal attenuator or the vertical amplifier. To determine where the trouble exists check the appropriate voltages and waveforms with an oscilloscope.

# CRT DISPLAY CIRCUITS

# Hew Shew HII Scans

The CRT display supplies a visual indication of – any signals which are applied to the CRT. One of the most important uses to which cathode-ray-tube displays and their associated circuitry are applied is the location of objects or targets in space. This is the prime **purpose** of **radar**. Generally speaking, there are two types of radar systems; the pulsed radar system, and the continuous wave radar system. Since continuous wave radar systems are very rarely used, the discussion in this section is limited to displays associated with pulsed radar systems.

The display units used in pulsed radar are either deflection modulated or intensity modulated. These terms describe the method by which the echo signal

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affects the trace on CRT. In deflection modulated displays, the input signal, after being detected and amplified, is applied to the deflection system of the CRT, and shows up as a pulse or pip on a circular or single horizontal sweep line. Typical radar displays of this type are the A-scope and the J-scope. In intensity-modulated systems, the echo is fed to an intensifying circuit, which changes the bias on the control grid of the CRT. The control grid is normally biased at cut-off. When the signal is received, it causes the bias on the control grid of the CRT to become less negative, thereby increasing the density of the electron beam and the intensity of the trace. Typical radar displays of this type are the B-scope and the C-scope.

# Application.

The A, B, C, and J-scope type CRT presentations are relatively simple radar displays used for the purpose of locating the position (range and bearing) of a target with respect to the position of the radar.

# Characteristics.

A-Scope and J-Scope presentations use deflection modulated displays.

A-Scope and J-Scope presentations use single line displays.

A-Scope and J-Scope presentations show only one component of location (usually direction).

B-Scope and C-Scope presentations use intensity modulated displays.

**B-Scope** and C-Scope presentations form rectangular field displays.

B-Scope and C-Scope displays show two components of location (usually direction and range)

A-scope, J-scope, C-scope and D-scope displays are usually designed to use electrostatic deflection systems.

# Circuit Analysis.

**Generel.** The A-, B-, C-, and J-Scope displays constitute the most commonly encountered types of radar displays employing electrostatic type cathode ray tubes. They respond to the reception of echoes of signal pulses striking specific targets, and present these echoes as pips or illuminated targets on the trace of the display, indicating location of targets through the time relationship of the echo signals compared with the sweep signals. The typical A-scan is shown in the following illustration. It consists of a single horizontal line with a transmitted pulse identication, representing the beginning of the sweep, and echo pulse indications, representing targets. The transmitted pulse indication has an amplitude greater than any of the other echo pulse indications.



The A-Scope is primarily used in conjunction with other radar indicators, since the A-Scope can only locate the range of a target. The A-Scope is particularly used in artillery fue control because of the accuracy of its range determination. The A-Scope is also used as a test instrument to observe video input signals during the testing and alinement of radar receivers.

A typical J-Scan is shown in the following illustration. It consists of a single circular trace line, which remains at a relatively constant distance from the center of the CRT face. A main pulse indication on the circular trace indicates the beginning of the sweep, and the echo pulses are located somewhere along the circumference of this **circle**. The distance between the echo pulse and the main-pulse along the circumference of the circle, indicates the range of the

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target. A calibrated range ring is used to measure the distance along the circular trace.

The J-Scope is used in radar for extremely accurate range determination of a particular target. In the laboratory, the J-Scope is applied to the measurement of very short time intervals.





J-Scope Display

A typical B-Scan is shown in the following

illustration. It consists of a rectangularly scanned

field made up of parallel vertical trace lines, with the

center line of the field representing zero azimuth (dead ahead) position. The radar location is at zero

azimuth position on the horizontal base line. Any

targets which appear to the right or left of this center

line are actually located to the right or left of the ship

or radar center line, at the vertical distance shown.

The B-Scope is used in radar systems for continuous scan of an assigned area, chiefly for ground (or sea) targets in a limited sector.

A typical C-Scan is shown in the following illustration. It consists of a rectangularly scanned field made up of a number of parallel horizontal lines; the center vertical line which bisects the horizontal length of the field represents zero azimuth position, while the center horizontal line which bisects the

vertical length of the field represents zero elevation position. All vertical positions above the zero elevation position represent a positive elevation, and all vertical positions below the zero elevation represent a negative elevation.





The C-Scope is used in radar systems for continuous scan of an assigned area, chiefly for aircraft interception and beam landing.

**Circuit Oparation.** The A-and J-Scopes are similar in that the signal is obtained from the radar receiver and applied through vertical amplifiers to the vertical deflection elements of the CRT. The manner in which each type of scan accomplishes the sweep, however, is different.

A typical A-Scope arrangement is shown in the following block diagram.





In the A-Scope arrangement a trigger signal is fed to the trigger amplifier stage, simultaneously, the received echo signal is applied from the radar receiver through the vertical (video) amplifier to the CRT. The trigger for starting the sweep may come from either the timer within the indicator or from the transmitter. The trigger amplifier both amplifies and sharpens the trigger pulse, which is then applied to the triggered sweep generator where a sawtooth voltage is produced and applied to the horizontal deflection plates. The resultant sweep produces a straight horizontal trace line on the CRT. With the application of the received echo signal, a vertical deflection in the form of a pip appears located somewhere along the horizontal trace. The distance between the radar antenna and the target is indicated by the linear position of the pip on the trace. Some of the pulse voltage of the transmitter is impressed directly upon the

receiver, and produces a large pulse on the extreme left of the CRT trace. All distances are measured relative to this pulse. To facilitate the measurement of the distance of the echo pip from the zero reference point (transmitter pulse), calibrated markers generated by the marker generator stage are also applied to the CRT. Thus by counting the number of markers between the transmitted signal and the received echo, target distance is quickly determined.

A typical J-Scope is shown in the following block diagram. A crystal oscillator and a phaseshifting network furnishes two sine-wave voltages, 90° out of phase, to both sets of CRT deflection plates to produce a circular trace. The trigger and sweep circuits blank out the tube, intensifying the electron beam only during the active sweep time. The J-Scope display is the same as the A-Scope display, except that the J-Scope uses a circular sweep rather than a linear sweep. Time and range measurements on the J-Scope are more accurate than those of the A-Scope since the J-Scope scan is longer. The target echoes are indicated as radial pips or pulses pointing away from the center of the CRT. To produce these pips another CRT electrode is introduced. This electrode is a thin metallic rod inserted through the face of the tube, almost reaching the deflection plates. The echo signals then are applied to this center electrode from the vertical amplifier.



#### J-Scopa Circuit

The B-Scope and the C-Scope, like the A- and J-Scopes are mostly similar in their mode of operation. The B-Scope and the C-Scope both use intensity modulated displays, that is the echo signals appear as bright patches against a dark background. Intensity modulation is produced by applying the amplified echo signals to either the control grid or the cathode of the CRT. In both the B-Scope and the C-Scope, the sweep scans a rectangular area on the screen of the CRT. Also, in both the B-Scope and C-Scope, the horizontal axis always represents azimuth. On the other hand, the vertical axis on the B-Scope represents range while the vertical axis on the C-Scope represents elevation. The block diagram of a typical B-Scope and a typical C-Scope arrangement is shown in the following block diagram. The only difference in the circuitry between them is the omission of the vertical sweep generator in the C-Scope. The vertical deflection circuits of the B-Scope are driven by a linear timebase signal from a sweep generator. This sweep is initiated by a sync signal from the central timing circuits of the radar. The vertical deflection circuits of the C-Scope are driven by a sweep voltage from a variable potentiometer connected the radar antenna.



#### B-Scope and C-Scope Circuits

The horizontal-deflection circuits of the B-Scope and C-Scope are the same type of circuits as those used for the vertical-deflection system of the C-Scope. The horizontal motion of the antenm is translated into a regularly varying (sweep) voltage which produces the horizontal sweep for the cathode-ray tubes.

The electrostatically deflected CRT common to the A-, B-, C-, and J-Scopes is shown in the following illustration with its accompanying control circuitry. The rod shaped dotted lines, extending from the face of CRT almost to the deflection plates represents the electrode used only in the J-Scope to which negative video (echo) signals are coupled. This electrode causes

the electron beam to be deflected radially outward in accordance with the incoming signals.





It is evident from the schematic that resistors R9, R1O, RI 1, R12, R13, R14, R15, R16, R17 form a voltage divider network. The cathode of the CRT is connected at a less negative point on the divider than the grid, the grid is negative with respect to the cathode, and is adjustable by means of potentiometer R13. R13 then, as in conventional circuits, permits the tube to conduct more or less heavily. This is the intensity control. Anode no. 1 is connected to a much lower point on the divider through potentiometer R15; thus it is effectively less negative than the cathode and grid, and attracts electrons from the cathode. This is the focus control. By varying the d-c potential on this control, the electron beam from the cathode is directed so that it converges at a point on the face of the CRT. Anode no. 2 is at a positive

potential and as anode no. 1 attracts electrons from the cathode. It provides the function of acting as an auxiliary focus control and an accelerating anode. As the beam passes from the accelerating anode to the face of the tube, it passes between two sets of deflecting plates. The horizontally positioned plates deflect the beam vertically and the vertically positioned plates deflect the beam horizontally.

A balanced deflection system is used for this cathode-ray tube. Each deflecting plate (Dl, D2, D3, and D4) is controlled by separate dual potentiometers (R2, R3, R6 and R7, respectively), and the plates are isolated and balanced equally by being connected to the positioning controls through equal resistors Rl, R4, R5, and R8. A-C balance is provided by capacitors Cl, C2, C3, and C4. Since the isolating resistors

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Rl, R4, R5 and R8 are always a very large value, the deflecting plates may be connected into any circuit without danger to the operator.

# Failure Analysis.

**Cathode-Ray Tube.** Usually, a control circuit failure in the CRT is indicated by loss of a specific control function, and can be quickly verified by a resistance or voltage check. It must be understood that all controls affect the electron beam in the same manner, and that the controls are interacting. For example, increasing the intensity of the beam will also thicken the beam, and require readjustment of the focus control for the thimest line at that intensity. Likewise, a change in the accelerating anode potential will cause a change in spot diameter and the maximum intensity available. Where high humidity and excess moisture prevail, control failures from insulation breakdown are usually more prevelent because of the high potential involved, which causes a short circuit to ground.

If it is found that all of the voltages on the CRT electrodes are proper the CRT must be the defective component. If, however, the voltages on the CRT electrodes are not proper, and the associated control circuitry is checked and found to be proper and the power supply is functioning properly, the fault must exist in some stage preceding the electrode with the improper voltage on it. It is also possible to determine the area of the fault by the CRT indications.

In the A-Scope, if the improper voltage or waveform exists on the horizontal deflection plates and the CRT indication shows that there is an improper or no horizontal sweep, check the input of the triggered sweep generator with an oscilloscope. If it is correct the fault lies in this circuit. If the voltage is incorrect, check the input of the trigger amplifier with an oscilloscope. If the trigger amplifier input is correct the faulty component is in this stage. If the input is incorrect and an external trigger is used the fault is in this external source. If, however, the input of the trigger amplifier is incorrect and the trigger is obtained from the internal trigger generator, check the input to the internal trigger generator with an oscilloscope. If the voltage or waveform applied to the internal trigger generator is improper the fault should be in the timer. If the CRT display indicates that only the range markers are missing the trouble must be in the marker generator.

If the improper voltage or waveform is present on the vertical deflection plates the trouble must be in the vertical amplifier or circuitry prior to the A-Scope indicator. Check the input of the vertical amplifier with an oscilloscope. If it is correct the fault is within this circuit.

In the J-Scope, if circular trace is improper and improper voltages or waveforms exist on the vertical and horizontal deflection plates, check the input of the phase shifting network with an oscilloscope. If the input is proper the fault is in this circuit. If, however, the input is improper the fault is the crystal oscillator. If the intensity of the display is improper and the voltage existing on the control grid is improper, check the input of the sweep circuits. If the input is proper the fault is in these circuits. If the input is improper the fault must be in the trigger circuits. If the improper signal exists on the center electrode of the CRT and if the video signal on the display is incorrect, check the input of the video amplifier with an oscilloscope. If the input is proper the fault is within the video amplifier. If the input is improper the fault must be in the radar receiver.

In the B- or C-Scope, if the voltages or waveforms on the horizontal plates are improper, or if the horizontal trace is improper check the input to the horizontal positioning circuits with an oscilloscope. If the input is correct the failure is in the horizontal positioning circuits. If the input is improper, the failure is in the antenna azimuth sweep voltage. If the voltages or waveforms on the vertical plates of the B-Scope are improper, or if the vertical trace is improper check the input of the vertical sweep generator with an oscilloscope. If the input is proper the -failure is in the vertical sweep generator. If the input is incorrect the failure is in the trigger source. If the voltages or waveforms on the vertical plates of the C-Scope are improper, or if the vertical trace is improper, the antenna voltage must be incorrect. If the target echo signals are not present on the control grid of the CRT, check the input to the video amplifier stage or stages with an oscilloscope. If the input is proper the fault is within these stages. If the input is improper the failure is in the radar receiver.

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# PART 9-2. ELECTROMAGNETIC

# ELECTROMAGNETIC CATHODE-RAY TUBE CIRCUITS

#### General.

A cathode-ray tube is an electron tube in which the electrons trajecting from the cathode toward an anode are focused into a concentrated beam which eventually strikes the luminescent screen. This beam is varied in position and intensity which produces a visible pattern on the screen. An electromagnetic cathode ray tube utilizes magnetic fields to provide a means of focusing and deflecting the electron beam.

Electromagnetic cathode-ray tube circuits are preferred where the cathode ray tube (commonly) referred to as CRT) is to have a large screen diameter. The electromagnetic CRT has several advantages over the electrostatic tube. Some of these advantages are that: a well focused electron beam of higher current density can be produced; greater accelerating voltages can be used to obtain brighter screen patterns without as great a reduction in the deflection sensitivity of the tube; the structure of the electron gun is simpler and more **rugged**; and the over-all length of the envelope is shorter.

A pictorial representation of the electromagnetic CRT is shown in the accompanying illustration.



Electromagnetic Cathode Ray Tube

The electromagnetic CRT uses a triode type gun. It consists of an indirectly heated cylindrical cathode closed off at one end by a small plate, which is coated with barium and strontium oxides. The oxides emit a large number of electrons. A twisted heater element is

contained within the cylindrical cathode to bring the cathode to the operating temperature. The control grid is also a cylinder, which surrounds the cathode cylinder. It contains a baffle with a tiny aperature of smaller diameter than the emitting surface of the cathode, which is located very close to the aperature. Beyond the control grid is a hollow cylinder which contains several baffles and which has its circumference around the same axis as the control grid. This cylinder is the accelerating anode which is connected to a conductive coating within the tube. This coating acts as an extension of the accelerating anode and as an electrostatic shield. There is no second anode for focusing as there is in the electrostatic CRT. Instead, an external focusing coil encircles the neck of the tube and magnetically focuses the electron beam. The complete focusing system is composed of two lenses, one is produced by the electrostatic field between the control grid and the following electrode. This electrostatic field causes the electron beam to converge at a point some distance before the magnetic field of the focusing coil which acts as the second lens. After the electrons travel beyond the convergent point they again begin spreading until they enter the magnetic field of the focusing coil, where the reaction causes the electrons to later converge at the phosphorescent screen, if the position of and the current through the coil are correct. The position of this external focusing coil is not only capable of being varied along the neck of the tube, but the physical construction of the coil also permits one side of it to come in closer proximity to the tube than the other. This characteristic of the focusing coil provides a means of centering the electron beam as well as focusing it.

The method of accomplishing horizontal and vertical deflection also relies on an external electromagnetic force. This electromagnetic force is provided by a set of coils, which encircles the neck of the CRT and is located after the focus coil. Usually four deflection coils are used. Two of these are wired in series and are mounted in such a way as to produce a magnetic field whose lines of force run vertically through the neck of the tube. This vertical magnetic field causes horizontal deflection of the electron stream. The other pair of coils is wired in series and mounted in such a way as to produce a magnetic field whose lines of force run horizontally through the neck of the tube. This horizontal magnetic field causes a vertical deflection of the electron stream. A current is used to activate the coils and produce the

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magnetic fields at right angles to the electron movement. The amount of deflection that may be obtained is dependant upon: accelerating anode voltage, distance between the screen and the deflection coils, length of the magnetic field, and the strength of the magnetic field. These deflection coils are contained in a mounting and called the deflection yoke. The position of the deflection yoke, hke the position of the focus coil, can be shifted along the neck of the tube to vary the amount of deflection. The deflection yoke can also be rotated about the neck of the tube. This property permits the visual pattern or raster to be centered squarely on the screen.

Another element used on an electromagnetic CRT is called the ion trap. It removes a problem that is specifically peculiar to the electromagnetic CRT. Negative ions exist in the CRT as a result of the bombardment of the residual gas or tube electrodes by the emitted electrons. This condition is of no consequence in an electrostatic CRT since electrostatic focusing networks can focus the ions along with the electrons. In the electromagnetic CRT, however, the greater mass of the ion prevents proper focusing and deflection of these ions. The result is a constant bombardment of the screen at one particular spot, causing the gradual deterioration of the phosphorescent material at this point and a dark spot on the screen. There are several types of ion traps that may be used. One type consists of a modified electron gun arrangement and a permanent bar magnetic unit which is slipped around the neck of the tube close to the electron gun. Although it is not shown in the illustration, the gun is made to produce a bent electrostatic field that carries both ions and electrons toward the accelerating anode. The ion-trap magnet affects only the electrons in this combined beam in such a way that they change their direction of motion and return toward the main axis of the tube. In this reamer only the electrons strike the screen, while the ions strike the anode and are removed.

The types of scan and circuits used with the electromagnetic CRT are described in following paragraphs in this section.

# PLAN POSITION INDICATOR (PPI)

# Application.

The plan position indicator (or PPI) type of radar display is used when it is desired to track objects on a 360° **polar** map giving range and azimuth. This map can **easily** be correlated with standard maps, since, not only the target but also physical features of the area are made apparent.

## Characteristics.

Uses electromagnetic CRT.

May use rotating or stationary deflection yoke.

PPI CRT uses high persistence phosphor.

PPI utilizes intensity modulation.

Antenna and sweep trace are synchronized.

Center of sweep represents radar location.

Sweep starts at the center and moves radially outward.

Angle of **target** from heading represents bearing of target.

Distance of target from center of sweep represents range of target.

# Circuit Analysis.

**General. The** plan position indicator is a type of radar display which utilizes an electromagnetic CRT. A high persistence phosphorescent material is used on the face of the CRT, which permits the glow produced by the electron bombardment to remain for a relatively long period of time. Signals reflected from targets are taken from the radar receiver and applied to the control grid of the CRT, via limiting and amplifying circuits, during the sweep time of the beam. Intensity modulation of the electron beam occurs in accordance with the amplitude of the received echoes, which produce corresponding bright portions on the screen.

The distance that the brightened portion of the trace is from the origin of the sweep, is the range of the target. The angle that is made by the brightened portion of the trace with respect to the zero degree radius of the sweep constitutes the bearing (or azimuth) of the target. This type of display also

permits an operator to locate a target with respect to the position of physical features of an area, which are shown on the display in the form of a polar map.

The rotating sweep which characterizes the polar map display is produced by a magnetic deflection field rotating in synchronization with the radar antenna. This may be accomplished by a mechanical azimuth sweep (rotating deflection yoke) or electrical azimuth sweep (stationary deflection yoke).

A pictorial representation of a typical PPI display is shown in the following illustration.



**Typical PPI Display** 

**Circuit Oparation.** The circuits used in the discussion of circuit operation are typical circuits used, in PPI displays, but do not represent every circuit that could be used in PPI displays. A block diagram of a simple PPI display is shown in the following illustration with corresponding waveforms. An analysis will be made of the operation of each representative circuit corresponding to the block diagram.



Simple PP1-Scan Block Diagram

The timer **trigger** is a negative pulse obtained from the timing circuits, and used to acutate the start-stop multivibrator. The multivibrator produces negative gate signals which are applied to the sweep generator and the marker generator, and a positive gate signal which is applied as an unblinking gate to the control grid of the CRT. A typical start-stop multivibrator is shown in the following illustration. Resistors R1 and R2 are grid bias resistors for triodes VI and V2, respectively. Resistors R3 and R4 are the plate resistors for V1 and V2, respectively. Capacitor Cl couples the grid of VI to the plate of V2. Capacitor C2 couples the grid of V2 to the plate of VI.


Start-Stop Multivibrator

Normally, triode V1 is conducting due to the positive bias applied on the grid of VI. At the same time, triode V2 is normally cut off due to the fixed negative bias applied to the grid of V2. A negative pulse applied to the grid of VI reduces the conduction of Vl, causing the plate voltage to increase. The positive plate voltage swing of V1 drives the grid of V2 into conduction, thereby decreasing the plate voltage of V2. This decrease (Negative swing) in the plate voltage of V2 is fed back to the grid of V1 and drives V1 into cutoff. The circuit now rests in the opposite condition with V2 conducting heavily and VI cut off. During this period the flat portion of the output pulse is generated. Since capacitor C 1 is connected to the positive supply through R1, it eventurdly develops a positive charge which is sufficient to bring the grid of V1 above cutoff. Once again VI conducts and the negative plate swing is coupled to the grid of V2 through C2, driving V2 towards cutoff and producing the trailing edge of the square wave as its plate voltage rises. Eventually, V1 is brought to the state of maximum conduction and V2 is brought to cutoff, where the circuit stabilizes due to the positive biasing voltage on the grid of V1 and the high negative bias voltage on the grid of V2. Another negative pulse must be applied to the grid of VI in order to change the conduction states of V2 and V2.

From the description of the circuit operation of the start-stop multivibrator it can be seen that with the application of one negative timer pulse to the input, one negative rectangular pulse is obtained at the plate of V2. This negative rectangular puke is used to operate the sweep generator and a marker generator. At the same time, a positive rectangular pulse is taken from the plate of V1 and is applied to the control grid of the cathode ray tube for unblinking use.

The typical sweep generator, which receives the negative rectangular pulse from the start-stop multivibrator, produces a trapezoidal sweep. The following schematic is that of a typical sweep generator circuit. The negative rectangular pulse is applied to the grid of triode VI, which acts as a high speed switch. Resistor RI is the plate resistor of V1. R1 is also part of an r-c network, which determines the amplitude of the leading edge and the slope of the trapezoidal waveform, when V1 is cutoff. Resistor R2 is also part of the r-c network when V1 is cutoff. Its vrdue also affects the amplitude of the leading edge of the trapezoidrd waveform. Capacitor Cl is the capacitive part of the r-c network. Its value affects the slope of the trapezoidrd waveform.



Sweep Generator

When no rectangular pulse is applied to the input, triode VI is conducting and effectively shunting R2 and Cl. As the negative rectangular input pulse is applied to the grid of V1, conduction of V1 ceases

and the plate voltage rises towards the supply value generating the leading edge of the trapezoidal sweep waveform. The cutting off of V1 acts like opening a switch, and causes capacitor Cl and resistor R2 to be brought into circuit action. An equivalent circuit with corresponding waveforms is shown in the following illustration for ease of understanding.



#### Equivalent Trapezoidal Sweep Generator Circuit

Capacitor Cl charges up to towards the value of the plate supply voltage through resistors RI and R2 at a rate dependent on the product of Cl times the sum of RI and R2. The output is taken across capacitor Cl and resistor R2. Thus, as capacitor Cl charges, the voltage drop across R1 appears at the output. The output voltage increases toward the plate voltage supply at the charging rate of capacitor Cl until the end of the negative rectangular input pulse occurs. At this time, the positive trailing edge drives V1 into conduction, removing capacitor C1 and resistor R2 from the circuit action by effectively closing the triode switch shown in the illustration of the equivalent circuit of the sweep generator. The circuit remains in this state until the next negative rectangular pulse is applied to the input. The resultant output waveform is a trapezoidal pulse for every negative rectangular pulse applied to the input.

The trapezoidal pulse is applied to a sweep **ampli**fier where it is amplified before being applied to the sweep coil circuit. A typical sweep amplifier is shown in the following illustration. Capacitor Cl is a coupling capacitor and the grid of V1 is returned to ground through grid resistor RI. Cathode bias is provided by resistor R2 and R2 is bypassed by capacitor C2 to prevent any degenerative effect. Vacuum tube V1 is a beam power tube, used because of its high power sensitivity. Power **amplification** is required to provide sufficient current to the deflection coils. The coils may require from 50 to 100 milliamperes of current for maximum deflection. Inductance L1 and resistance R3 comprise the deflection coil and act as the plate load for the sweep amplifier. The output waveform, at the plate of V], is trapezoidal. As this waveform is applied to the deflection coil, it becomes resolved to a sawtooth waveform across the resistance of the coil, and a square waveform across the inductance. The square wave across the inductance produces a sawtooth sweep current due to current lagging voltage in an inductance. (For detailed information on amplifier circuits refer to the **Amplifier** Section of this Handbook.)



Sweep Amplifier

The PPI sweep starts at the center of the CRT, and moves radially outward to the periphery of the CRT. The sweep trace position is made to indicate target bearing (or azimuth) by rotating it in synchronization with antenna rotation. This can be accomplished by any of several methods in two general categories. The **first** category uses a mechanical azimuth sweep, which provides a means of physically rotating the deflection yoke in synchronization with the antenna. This may be accomplished by using synchronous

motors connected to the same power supply which drives the antenna and the deflection yoke; or it may be accomplished by using electromechanical repeaters to provide proper synchronization. The following figure illustrates how deflection is produced at the cathode ray tube.





The accompanying figure shows the deflection coil

currents for electrical azimuth sweep.

Mechanical Azimuth Sweep

The second method is to use an electrical azimuth sweep which uses a stationary deflection yoke. The amplitudes of the sawtooth sweep currents are varied sinusoidally, from zero to maximum, corresponding to the rotation of the antenna. Furthermore, there is a 90° phase difference between the amplitude variations of the horizontal end vertical sawtooth waveforms. The sinusoidal variation is such that at maximum amplitude of the vertical sawtooth signal, the sweep will extend from the center of the CRT to the top of the CRT, or the maximum vertical position, which usually represents north. The amplitude of the horizontal deflection sawtooth waveform is zero, at this time. Thus, the sweep does not extend in the horizontal direction at all. If the sweep were to represent East, or 90° east of the direction of travel, the horizontal deflection sawtooth amplitude would be maximum and the vertical deflection sawtooth amplitude would be minimum, or zero. Once the sweep travels beyond East, or 90° east of the direction of travel, the amplitude of the vertical sawtooth becomes negative; and, once the sweep travels beyond South, or 180° from the direction of travel, the horizontal sawtooth amplitude becomes negative also.

## Deflection Coil Currents for Electrical Azimuth Sweep

In order to obtain two sinusoidally varying sawtooth waveforms, having a 90° phase difference, a rotary transformer is used. This transformer resembles a small electric motor and has two secondary windings, which are mounted at right angles to each other in the stator housing. The primary is mounted on the rotor, which is driven by the rotating antenna. A trapezoidal-wave generator is connected to the primary winding by means of slip rings. As the rotor is turned, the voltage obtained from either secondary varies. Maximum voltage is obtained from one secondary when zero voltage is obtained from the other. The transformer is so constructed that the amplitude of the output voltage varies sinusoidally with the rotor angle. The amplitudes of the trapezoidal output voltages, then, vary sinusoidally, and are 90° apart in phase. The trapezoidal output voltages are applied to separate power amplifiers. The required sawtooth sweep currents are obtained at the output of the power amplifiers. Sweep clampers are usually used to keep the reference level constant, and cause every sweep to start at the same point on the CRT.

It was mentioned previously that the start-stop multivibrator has an output applied to the control grid of the CRT and to the marker generator, as well as to the sweep generator. A positive gate produced

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by the multivibrator is applied to the CRT control grid. This positive pulse increases the electron flow between the cathode and the face of the CRT, and permits the intensity of the trace to increase during the period that the timing pulse is applied. This is in reality an tmblanking gate which permits the CRT to be operated at the desired time.

The negative rectangular pulse applied to the marker generator from the start-stop multivibrator is used to trigger the production of range marks on the screen of the CRT. These range marks provide a means of determining representative distances of targets from the origin. A typical range marker generator is shown in the following illustration. It is comprised of four triodes, the first of which (VI) acts as a switch for triodes V2 and V3, which can only conduct when V1 is cutoff. Triodes V2 and V3 form a complete path for the series resonant circuit L1 C3, or L2 C4, which determines the frequency of the range mark pulses. Transformer T1 differentiates the output waveform of V3 before being applied to V4, which serves as a cathode follower output stage. Capacitor Cl is an input coupling capacitor, and resistor RI establishes contact bias for V1. Resistor

R2 is a plate voltage dropping resistor to provide V1 with a lower potential than the plate voltage value of V2. Resistor R4 is a common plate load resistor for triodes V1 and V2. Resistor R3 places the cathode of VI at a less positive potential than the cathode of V2. Resistor R5 holds the grid of V2 at approximately zero bias. Resistor R6 serves as a return to ground for the grid of V2, and capacitor C2 places the grid of V2 at an a-c ground potential. Resistor R7 places the cathode of V2 at some less positive potential than the cathode of V3. Resistor R8 is part of a cathode bias voltage divider on the cathode of V3. The divider consists of R3, R7 and R8 which places different fixed bias on the cathodes of VI, V2, and V3 respectively. The primary of T1 serves as a plate load for triode V3. Capacitor C5 couples the differentiated waveform to the grid of the cathode follower, V4. Resistors RI 1 and R9 place the grid of V4 at some highly negative potential. Resistor R1O provides a d-c return to ground for triode V4 and together withR11 forms a bias voltage divider between the negative supply and ground. Resistor R12 is the cathode resistor of V4 and serves to match the output of the cathode follower.



Range Marker Generator

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Prior to the application of the sweep starting pulse from the start-stop multivibrator, the triode VI is conducting, which keeps the plate voltage at a low value. This low voltage prevents the plate voltage of V2 from being higher than the grid voltage of V2. This low plate voltage of VI also causes the potential at the grid of V3 to be less positive than the cathode and of sufficient negative value to cutoff the tube. With V3 cutoff no output signal is developed.

When the negative sweep start pulse is applied to capacitor Cl, triode V1 is cutoff, which causes the plate voltage of VI to increase, and the voltage on the plate of V2 to increase, and at the same time causes the grid voltage of V3 to increase. With the increased grid voltage, V3 conducts completing the circuit containing triode V3, the series resonant circuit of L1 C3 or L2 C4, triode V2, and the primary of T1. A pulse type waveform is produced by this circuit with a frequency dependent on the vrdue of the resonant circuit. The waveform is applied to transformer T-1, where it is differentiated by the inductance in conjunction with the resistance of the primary before being coupled to the secondary of T1. From the secondary of T1, the differentiated pulses are applied to the grid of cathode follower (V4) through capacitor C5, which blocks out any d-c component. The output is obtained from cathode resistor R12. This output is not only decreased in amplitude and in phase with the applied pulses, but it is also limited to positive pulses by the high negative bias on the grid of V1. These positive pulses are than applied to the control grid of the CRT to increase the intensity of the trace at the point where the range marker rings are to occur.

The video signal is applied to a biased video limiter, where the signal is made to vary above a specific level, so that the signal will not become so negative as to cause blooming on the screen. A schematic of the video limiter is shown in the following illustration. The limiter consists of only three components; resistor R1, and used to drop the applied voltage when diode V1, the second component, is conducting, and voltage source  $E_{cc}$ , the third component, used to establish the limiting level.



#### Video Limiter

With no signal applied there will be no signal output. When a positive signal is applied, it will appear at the output unaffected by the limiting diode and the voltage source  $E_{cc}$ , since the nonconducting diode acts as an open circuit. Even as the signal begins going negative, the signal will remain unaffected; since the negative voltage on the plate of VI is greater than the applied negative signal, thereby maintaining V1 in the nonconducting state. When the signal becomes as negative as  $E_{cc}$ . Even when the input becomes more negative, the output still remains at the value of the source voltage  $E_{cc}$ . The output voltage will vary as the input signal only when the input signal becomes more positive than  $E_{cr}$ .

The output voltage of the video limiter is applied to a video **amplifier**, or several video amplifiers, where the voltage is increased in gain before being applied to the cathode of the CRT. A typical video amplifier is shown in the following illustration. Resistor **R1** is the grid leek resistor, and resistor **R2** is the cathode bias resistor, which, along with **RI**, establishes the

total grid bias. R2 is made variable to regulate the gain of the amplifier. Capacitor C2 is the cathode bypass capacitor, which bypasses the a-c signal to ground and prevents degeneration. R4 is the screen grid dropping resistor, and capacitor C1 is the screen grid bypass capacitor. The load consists of resistor R5, and resistor R6; however, at high frequencies the signal bypasses R6 through capacitor C4. Capacitor C5 is the coupling capacitor to the following stage.



#### Video Amplifier

Up to this point, the components which were discussed could form a common amplifier. The remaining components add to the previously discussed components to form the video amplit3er. Inductance L1 is a series peaking coil, which functions as a series falter for passing required frequencies. It also isolates circuits preceding it from circuits following it. Resistor R3 aids L1 by extending the effects of L1 and broadening the Q characteristics. Inductance L2 is a shunt peaking coil, which forms a parallel resonant circuit with the distributed capacitance (C3) and provides a high impedance for the signal. Capacitance C6 is the inter-electrode and distributed capacities of the following stage. Vacuum tube **V1** is a pentode.

The negative signal coming from the video limiter is applied directly to the grid of the tube Vl, decreasing the conduction of V1 and varying it in accordance with the signal variation, and at the same time establishing a bias level through resistors R1 and R2. The variation in conduction rate of V1 produces an oppositely varying plate output voltage, which is developed across resistors R5 and R6. The higher frequencies of the signal, which would normally be lost or distorted by distributed capacitance (C3) and the interelectrode capacity, are passed undistorted by means of the series peaking (L1) and shunt peaking coils (L2) inserted in the amplifier. These coils form resonant circuits with the effective capacities, permitting the higher frequency signals to be passed easily **to** the output and preventing these frequencies from being shunted to ground. (For a more detailed discussion of video amplifiers, refer to section 6 of this handbook.) One or several video amplifiers may be used to provide the desired amplitude of output signal.

## Failure Analysis.

#### Start-Stop Multivibrator.

**No Output.** Since the start-stop multivibrator is responsible for producing synchronized sweep, range markers, and intensified trace during the time that information is to be presented, a defect in this circuit will affect each of these areas. If no output occurs it will be difficult to localize the trouble, since no spot will appear on the CRT. This effect can also be caused by the sweep generator or sweep amplifier having no output.

The no-output condition, in the start-stop multivibrator, may be due to lack of signal or lack of plate supply voltage. Check the signal with an oscilloscope at the input of the multivibrator. Check the plate supply voltage with a voltmeter. If the no-output condition exists and there is plate supply voltage, the condition may be due to a combination of faulty components. If resistors R3 and R4 were both open, or if triodes VI and V2 were both defective, the nooutput condition would occur. Measure the resistors on a ohmmeter. If the condition still exists, triodes V1 and V2 are probably defective.

Low or Distorted Output. If a low or distorted output occurs in the start-stop multivibrator, it becomes more apparent that the trouble is in this stage, rather than the sweep generator or the sweep amplifier, since each one of the three applications of the multivibrator will show the effect of the trouble.

The low or distorted output maybe due to any of the following component failures: Shorted or open plate load resistor R3, shorted or open plate load resistor R4, shorted or open bias resistor RI, shorted or open bias resistor R2, shorted or open capacitors Cl or C2, improper plate supply voltage, defective triode V1, defective triode V2, or improper input signal. To determine which of these component failures is responsible for the condition, make the following checks: measure the input signal with an oscilloscope; measure the plate supply voltage with a voltmeter, and adjust the supply for the proper voltage; measure the resistors with an ohmmeter to be certain that they are of the proper ohmic value and within tolerance; and measure the capacitors with an in-circuit capacitor checker. If these components have been checked and the condition still exists, triodes VI and V2 are probably at fault.

## Trapezoidal Sweep Genarator.

**No Output.** If no output is obtained at the output terminals of the sweep generator, no sweep is produced and the cathode ray tube will indicate only a single spot at the origin of the sweep.

A no-output condition may be due to any of the following circuit failures: no plate supply voltage, open resistor R1, open capacitor Cl, or open resistor R2. To determine which of these is responsible for the no-output condition, first check the input signal with an oscilloscope. Check the plate supply voltage with a voltmeter, and adjust the supply voltage to the proper voltage value. Check resistors R1 and R2 with an ohmmeter, and check capacitor Cl with an incircuit capacitor checker.

Low or Distorted Output. If a low or distorted output is obtained at the output terminals of the sweep generator, and the proper input signal is applied, the fault may be due to any of the same component failures that occur in the no-output condition, plus the possibility of a defective triode, V1. The same checks apply in the low or distorted output condition as in the no-out condition. If these checks do not locate the trouble, triode VI is probably defective.

### Sweep Amplifiar.

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**No Output.** If no output is obtained at the output terminals of the sweep amplifier, no deflection will be produced and the trace will be in the form of a single dot at the origin of the sweep.

A no-output condition may be due to any of the following circuit failures: open capacitor Cl, no plate supply voltage, no input signal, or a defective triode, V1.

To determine which of these failures is responsible for the no-out condition, use the following checks: measure the input signal with an oscilloscope; measure the plate supply voltage with a voltmeter, and adjust the source if it is the cause of the condition; measure capacitor Cl with an in-circuit capacitor checker. If these checks do not locate the trouble, triode V1 is probably defective.

Low or Distorted Output. A low or distorted output may be due to any of the following circuit failures: shorted capacitor C1, shorted or open resistor RI, shorted or open resistor R2, a shorted or open capacitor C2, low plate supply voltage, or a defective triode, V1.

To determine which of the circuit elements is responsible for this condition, make the following checks: measure capacitors Cl and C2 with an incircuit capacitor checker; measure **the values of** resistors R1 and R2 on an ohmmeter; measure the plate supply voltage source with a voltmeter, and adjust the source to the proper plate supply voltage. If these checks do not lead to the defective part, triode VI is probably defective.

#### Range Marker Ganarator.

**No Output. A no-output** condition in the range marker generator will result in no range markers being produced on the face of the CRT. This condition may be due to any of the following circuit failures; no plate supply voltage, defective triode V2, defective triode V3, open or shorted transformer T1, open inductors L1 or L2, open capacitors C2 or C4, open capacitor C5, open or shorted resistor R12, or defective triode V4.

To determine which of these components is at fault, make the following checks: measure for possible defective resistors with an ohmmeter; check the applicable capacitors with an in-circuit capacitor checker; check the ohmic values of inductors Ll, L2, and the primary and secondary windings of transformer T1. Check the plate supply voltage with a voltmeter, and adjust the plate supply voltage if it is not the proper voltage. If the no-output condition still exists after all other checks have been made, triodes V2, V3, and V4, and probably defective.

Low or Distorted Output. Low or distorted output may result in improperly situated range marks on the screen of the CRT. This condition may be due to any of the following circuit failures, providing the proper input signal is applied: improper plate supply voltage, shorted capacitor Cl, shorted capacitor C2, shorted capacitors C3 or C4, shorted capacitor C5, shorted inductors L1 or L2, shorted or open transformer T1, shorted or open resistors R1, R2, R3, R4, R5, R6, R7, R8, R9, RIO, or R11; or defective triodes V1, V2, V3, or V4.

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To determine which of the components is responsible for the condition, make the following checks: check the applicable capacitors with an in-circuit capacitor checker; check applicable resistors with an ohmmeter; check inductors and transformer windings with an ohmmeter; Check the plate supply voltage with a voltmeter, and adjust the supply if the voltage is not the correct value. If the low or distorted output still exists after checking and correcting any of the possible foregoing failures, the tubes are probably at fault.

## Video Limiter.

Since the video limiter is composed of three components the failure analysis may be simplified.

No Output. In order to have a no-output condition, an open resistor RI, an open bias supply voltage  $E_{CC}$ , or a defective diode V1 would have to exist. This no-output condition would result in no indication of the target as well as no indication of the area being scanned.

To determine which of the three components is responsible for the no-output condition, measure the bias supply voltage with a voltmeter and adjust it if it is not the correct value; measure resistor R1 and check V].

Low or Distorted Output. A low or distorted output would result if any one of the same three components is defective. Use the same checks to determine which of the components is responsible for the low or distorted output condition.

#### Video Amplifier.

**No** Output. A no-output condition in the video amplifier would result in no visual representation of the target or scanned area. This condition maybe due to absence of signal, absence of plate supply voltage, open resistor R6, open resistor R5, open inductor L2, shorted capacitor C4, open capacitor C5, or a defective pentode V1.

To determine which of these components is defective make the following checks: measure the input signal with an oscilloscope; check the plate supply voltage source with a voltmeter and adjust the source to the proper value, if it is not the proper voltage, check resistors R5 and **R6** with an ohmmeter; check inductor L2 with an ohmmeter, and check capacitors C5 and C4 with an in-circuit capacitor checker. If the no-output condition still exists after these checks and corrections have been made, pentode V1 is probably at fault. Low or Distorted Output. A low or distorted output may be caused by any one of the actual circuit components being defective, or an improper input signal.

To determine which component is at fault, use the following procedures: check the input signal with an oscilloscope, check the plate voltage supply with a voltmeter and adjust the supply voltage to the correct value, if it is not at the correct value. Check all resistors with an ohmmeter and check the ohmic values of inductors L1 and L2 with an ohmmeter. Check capacitors with an in-circuit capacitor checker.

If all of these checks do not locate the defective component, pentode V1 is probably at fault.

## OTHER TYPES OF ELECTROMAGNETIC SCANS

### Application.

Of the remaining types of electromagnetic scans three general types are probably encountered more often than any others. These scans are the spiral, the RHI, and TV scans. The spiral scan is usually used for range measurements where it provides a much longer time base than is available for circular or linear scans. The RHI scan is used where it is desired to determine the range and target height as a special radar presentation, and the television (TV) scan is used to reproduce scenes or images.

#### Characteristics.

A long persistence type of CRT is used with the RHI and spiral scans, while a medium persistence CRT is used with the TV scan to prevent blurring of the moving images.

In the RHI scan the horizontal base line always indicates range, while the height is indicated vertically.

The spiral scan may start at the center of the CRT and rotate spirally outward, or start at the periphery of the tube and rotate spirally inward to the center, depending upon design.

The TV scan uses a two field, odd-line interlaced scan operating at 30 frames vertically per second, and 525 lines horizontally, (a sweep frequency at 15750 Hz).

Scanning begins at top left of the CRT and travels \_ to the right and down.

Each frame consists of 525 individual horizontal scanning lines which move from top to bottom.

## **Circuit Analysis.**

**General. The** spiral scan, the RHI scan, and the TV scan are all produced by means of an electromagnetic deflection system; however, each may be produced by an electrostatic deflection system for special applications. The spiral and the RHI scans are similar in circuitry and in operation to previously mentioned CRT scans. The TV scan is unique in comparison to these scans, since, this type of scan produces a detailed reproduction of a specific scene or image.

An RHI scan is similar to an off-center PPI scan, but has an elevation or height indication in place of what would normally be the azimuth or bearing indication, as shown in the following illustration.



**Range Height Indicator Scan** 

The actual representation of the trace on the CRT originates at the lower left side of the screen and extends horizontally to the right, and vertically at the same time, resulting in an angular type display. The horizontal distance represents the range and the vertical distance represents the height. The origin of the trace represents the radar location. There are equidistant vertical lines along the angle of the display, which are range markers. A movable horizontal

line appearing across the pattern is used to determine the height of the target. Targets appear as intensified portions of the trance on the CRT.

The spiral scan is used when linear and circular traces do not have a sufficiently long time bases to record certain data with the required accuracy. The spiral scan is evolved from the circular scan, as used in PPI and is shown in the accompanying illustration.





#### Spiral Scan

The range of the scan can be varied by changing the number of turns in the spiral. The sweep rotates at a constant rate of speed, so that equal divisions along the spiral indicate equal range increments. The spirrd scan may start at the center of the trace, as it does in PPI, but it rotates spirally from the center of the CRT and only reaches the periphery of the tube by the end of the sweep. It is possible, too, that the spiral scan may start at the center of the CRT, only reaching the center of the CRT by the end of the trace. The origin of the sweep represents the position of the radar location. Targets are represented by intensified portions of the trace.

The TV, or uniform linear scan, is based on a beam that moves much as the human eye does in scanning a written page. It moves from the top left to the right and rapidly returns to the left, only slightly further down from the top than the previous line. It moves this way until reaches the bottom of

the sweep on the right side. This, however, only constitutes half of a complete frame. To complete the second half frame the sweep is rapidly returned to the top center of the CRT. The first line in the second half frame descends less than the first line in the first half frame, since the second half frame starts at the top center and has less horizontal distance to cover, and less time for the line to descend than the first half frame. In this way, the second half frame **fills** in scanning lines between the lines that were scanned during the first half frame.

The TV scanning sequence when looking at the picture tube is shown in the following figure. The scanning spot starts in the upper left hand corner and travels at a uniform rate from left to right along lines that lie at a distance below each other as shown by the solid lines in the figure. When the end of a line such as ab is reached the scanning spot quickly returns to the left (that is from b to c) to start new line cd. During this return interval the spot is blanked out and so is not shown in the figure. As the scanning spot moves back and forth across the tube, the spot also moves downward at a constant rate. Hence the lines in the figure are slightly sloped, and each line begins at a level that is a little below the end of the previous line. When the bottom of the picture is reached (point e in the figure), the spot quickly returns to point f at the top of the picture, while maintaining the back and forth horizontal line motion uninterrupted. Since the time required to travel from e to f corresponds to the passage of a number of lines, the spot traverses a path similar to that shown in the retrace figure as it goes from e to f. This return pattern is not seen by the eye, however, as the spot is blanked out during the return.







**TV Scan** 

The standard television picture takes 1/60 second to go from the top to the bottom of the picture and return to the top. During this time, which is called one *field* 262.5 lines are transmitted. Because each field contains a half line, the next field lies between the lines of the first field as indicated by the dotted lines in the figure; thus successive fields are interlaced. The complete picture, called a frame, therefore, consists of 525 lines and is transmitted in 1/30 second. The original pattern showing the trace lines is what is observed on a television receiver in the absence of a picture, and is termed the raster. Interlacing makes it possible to avoid flicker while using the lowest repetition frequency for the picture that will satisfactorily portray motion. Thus, while a picture repetition rate of 30 times per second is adequate to give the illusion of continuous motion under nearly **all** circumstances, large bright areas repeated 30 times per second will have a noticeable flicker. By interlacing, a flicker rate of 60 hertz is achieved which is too high to be perceptible; at the same time the picture is repeated only 30 times a second.

**RHI Circuit Oparation.** The block diagram of a typical RHI scanning system is shown in the following illustration. Since the operation of each basic circuit is described in detail in other sections of this Handbook, description of circuit operation is limited to the effect of each individual stage on the total scan system.



**RHI Bleak Diagram** 

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The first circuit to be considered is the gate circuit stage. It produces positive and negative gates occurring at the trigger input frequency which switches the range sweep circuit, the height sweep circuit, the height line generator, and the intensifier and intensity compensation and, in addition, a specird count-down gate which is used to gate the range marker circuit stage. The range sweep generator is one of two stages required to produce two linearly increasing, mutually perpendicular, magnetic deflection fields. One magnetic field, causing horizontal movement of the beam, is produced by current in the range sweep deflection coil as a result of the voltage produced by the range sweep generator. The rate of increase of the range magnetic field is proportional to the cosine of the elevation angle of the antenna. The range sweep generator transforms a dc reference voltage into the linearly increasing magnetic field in the CRT. The rate of increase of the magnetic field determines the speed at which the beam moves horizontally across the screen and is proportional to the dc reference voltage.

The height sweep generator stage also produces a linearly increasing magnetic deflection field. This magnetic field supplies the verticrd component of the CRT beam deflection. The rate of increase of the magnetic field is dependent on the dc reference voltage, which in turn is proportional to the sine of the angle of the antenna elevation. The rate at which the vertical magnetic field increases determines the speed at which the beam moves vertically on the screen.

The negative gate from the gate circuit stage is applied to operate the intensifier and intensity compensation circuit stage. This stage has two functions. One function is to allow signals to appear on the CRT only during the sweeping periods. During the intervals between sweeps the CRT is blanked off. The other function is to keep the intensity of the CRT signals constant with the changes in range, pulse repetion rate, and the elevation angle. Intensity compensation is produced by automatic variation of the dc voltage on the cathode of the CRT.

The range marker generator circuit produces equally spaced range markers. The range markers are

applied to a video amplifier where they are **amplified**, and then applied to the grid of the CRT. The nodding of the antenna causes the markers to appear as bright lines on the sweep.

The video amplifier stage **amplifies** the video target signals received from the radar receiver. It also amplifies the range markers, the height line pulses, and the range line input signals, and mixes them with the video signal. The amplified signals are applied to the CRT control grid.

The sector gating circuit, which has its output connected to the video amplifier stage, allows only those targets present in a selected azimuth sector to appear on the CRT face. It also determines the angular width of the sector to be viewed.

The servo amplifier stage supplies voltage to a motor which drives a sector gating synchro rotor. The position of the synchro rotor determines the bearing of the azimuth sector viewed on the RHI scope. The position of the sector gating synchro rotor always corresponds with the setting of the manual sector control.

The resulting RHI sweep appears on the CRT as a wedge. The vertex of the wedge, corresponding to the origin of the trace, appears at the left lower portion of the screen. The horizontal distance of the trace corresponds to the range, and the vertical distance of the trace corresponds to the height or elevation of the trace. The range indicating marks are vertical lines, of intensified trace with angular compensation, equidistant along a horizontal plane. The height line is a horizontal line of intensified trace. The video information coming from the radar receiver, which represents targets within the selected sector, produces intensified portions of the trace at the range and height positions on the display corresponding to the actual location of the target from the radar location.

**Spiral Sean Circuit Oparation.** A typical block diagram of the spiral scan producing system is shown in the following illustration. Since the operation of each basic circuit is described in detail in other sections of this Handbook, circuit operation will be limited to the effect of each stage on the total system.

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Spiral Searl Systam Block Diagram

The primary controlling state is the start-stop multivibrator. It converts an external negative timing pulse into a number of square wave pulse to the sweep generator stage, results in a trapezoidal sweep pulse output with the same duration as the square wave pulse applied to the input of this circuit, and occurring at the same frequency and time as the input pulse. This trapezoidal sweep output is applied to the sweep amplifier stage.

The application of the negative square wave pulse, from the start-stop multivibrator stage, to the trapezoidal generator stage also results in a trapezoidal output. This trapezoidal output, unlike that of the sweep generator stage, is not of the same duration as the input pulse, but occurs for a longer period of time. This period of time normally is an even multiple of the input pulse. The ratio of the trapezoidal pulse to the negative square input pulse determines the number of turns in **the** spiral sweep on the CRT. The trapezoidal output pulse, like the output of **the sweep** generator stage, is also applied **to** the sweep amplifier **stage**. The negative square wave pulse output from **the** start-stop multivibrator stage is also applied to the markers generator stage, where short duration marker pulses are produced for application to the CRT **con**-trol grid. These pulses produce intensified points on the sweep trace **which** correspond to specific range indications.

The positive square **wave** pulse produced by the start-stop multivibrator **stage** is applied to the control **grid of the** CRT. This pulse provides unblinking of the sweep on the CRT during the period that it is applied.

The trapezoidal sweep pulses produced by **the sweep** generator stage and the varying amplitude trapezoidal pulse from **the** trapezoidal generator **stage are** combined in **the sweep amplifier** stage and amplified. The addition of the increasing trapezoidal pulse to **the sweep** pulses produces a continually increasing sawtooth sweep of current through the deflection coils while the yoke rotates.

The resulting sweep on the CRT is similar to that of the PPI sweep, with **the** exception that each pulse

produced by the sweep generator stage does not produce a scanning line which extends from the center of the sweep to the periphery of the CRT. Instead, each sweep line extends a distance from the center of the CRT which corresponds to the amount of sawtooth current occurring in the deflection coil, at that time. Since the current in the deflection yoke continually increases in a sawtooth manner, the distance that the sweep trace extends from the center of the sweep increases in a linear manner, while rotating about the sweep origin, until it reaches the periphery of the CRT, forming a spiral sweep.

The video input is applied to a video limiter stage where any portions of the signal extending beyond the limiting voltage level are clipped off. The limited signal is applied to a video amplifier stage. The video **amplifier** stage amplifies the limited video signal. This **amplified** and limited video signal is then applied to cathode of the CRT, where it causes the intensity of the electron beam to vary accordingly. The resultant scan on the CRT appears as a spiral, with the sweep originating at the center of the CRT and gradually reaching the periphery of the CRT by the end of the spiral, which may contain a number of turns. Equidistant intensified points on the spiral sweep correspond to range indication marks. Any other intensified points or sections of the spiral, or extra-intensified range marks correspond to target indications.

**Television Scan Circuit Operation.** The typical block diagram of a television scanning system is shown in the following illustration, the seaming system comprises approximately one third of the complete television receiver. The synch (pulse) separate stage, which contains a limiter, an integrator and a differentiator is not actually part of the scanning system of the receiver, but is included in the block diagram to give a more complete description of the development of vertical and horizontal sweep pulses.





Actually the integrator and differentiator stage consists of only a resistor and capacitor combination. The clipper circuit eliminates all portions of the composite video signal below the synch pulse level. The differentiator network segregates the horizontal pulse information from the combined horizontal and vertical pulse waveform, and applies the integrated waveform to the vertical sweep stage. The differentiator waveform is used by the afc circuit to maintain the horizontal oscillator output in phase with the synchronizing pulses.

The frequency stabilized horizontal **synchronizing** pulses are applied to a free-running **multivibrator** to develop a sawtooth output waveform. This **multivi**brator, the horizontal oscillator, operates at a frequency which is slightly lower than the synchronizing

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pulse frequency. The synchronizing pulses, then, trigger the multivibrator into action at the synchronizing pulse frequency.

A portion of the output of the horizontal oscillator is fed back to the afc circuit to stablize the horizontal frequency, and the stabilized output is applied to a sweep amplifier, where it is amplified and coupled to the horizontal deflection coil through a transformer. A sawtooth current is developed in the horizontal deflection coil which electromagnetically sweeps the CRT electron beam horizontally. The horizontal output transformer is also used to furnish the high voltage for the CRT anode, and a damping circuit is connected across the deflection coil and output transformer secondary to prevent continuous shock oscillations from occuring in the horizontal deflection coil during the retrace time of the sweep. The damper circuit is also used to furnish an additional dc boost voltage for the horizontal oscillator as shown in the block diagram.

The integrated portion of the synchronized pulse waveform, when applied to the vertical oscillator, triggers the vertical oscillator stage and a free-ruining multivibrator when the value of the integrated waveform reaches a certain amplitude. The integrated vertical waveform reaches this triggering level at a **specific**, regular rate, which is much slower than the differentiated pulse rate. The output of the vertical oscillator, is also a sawtooth type waveform occurring at the triggering level rate of the integrated waveform.

The output of the vertical oscillator is applied to the sweep amplifier stage of the vertical sweep network. Here the vertical sweep waveform is amplified and coupled to the vertical deflection coils, causing a sawtooth current to be developed, which electromagnetically deflects the electron beam of the CRT in a vertical direction.

The resultant scan on the CRT is one in which the horizontal sweep occurs at a frequency of 15,750 Hz which is approximately 5000 times that of the vertical frequency. A total of 262.5 horizontal lines is swept by the time the horizontal scan has completed one top to bottom (vertical) sweep on the CRT. This vertical sweep occurs 60 times a second, however, this only constitutes half of a complete picture frame. During the next vertical sweep an additional 262.5 horizontal lines are scanned from top to bottom of the CRT at the same rate of 60 times a second. These lines interlace between those which were scanned during the **first** half frame. A total of 525 horizontal

scanning lines **are used** to provide greater detail in the picture. The reason for scanning only 262.5 horizontal lines for ordy one vertical sweep rather than scanning the full 525 lines for one vertical sweep, is that if the 525 lines were scanned at one time the complete picture would only be repeated 30 times a second and cause the display to flicker.

The TV scan moves much as human eves do in scanning a written page. The scan starts at the top left hand side of the CRT screen and proceeds horizontally to the right with a very slight downward movement at the same time. The scan is rapidly returned to the left side. After completing the first horizontal scanning line the CRT is blanked out so that it is incapable of producing a visible line during this retrace period. Upon being returned to the left side of the CRT, the next scan line is displaced slightly further down than the starting point of the first scanning line and the CRT is unblanked for the next line. Two hundred sixty two and one half lines are scanned in this manner, until the scan reaches the bottom center of the CRT. Upon reaching this point, the scan again is blanked out during the vertical retrace and is rapidly brought back to the top center of the CRT. The same scanning procedure as described for the first half-frame occurs for the second half-frame, only this time the scanning lines are interlaced between those scanned during the first half-frame. The result is that a complete picture appears on the CRT screen 30 times a second, with half of this picture changing 60 times a second to eliminate flicker.

#### Failure Analysis.

**RHI Scan.** In order for a no-output condition to exist, which is characterized by no indication of any kind on the CRT, a faulty power supply or a failure in each of the circuits comprising the system would have to occur. It is highly unlikely that every circuit in the system would fail, so the no-output condition would normally be limited to power supply failure. Check the power supply with a voltmeter to determine if the supply or a fuse is at fault.

There are several types of low or distorted outputs associated with the RI-H system. **By looking at the** trace on the RI-U indicator it is usually possible to determine the probable location of the failing circuit.

If there is no indication on the CRT, it is not necessarily true that a no-output condition exists. It only means that either improper potentials are being . -

applied to the CRT electrodes, the unblinking circuit is defective, or that the CRT, itself, is defective. First determine if the proper voltages and unblinking waveforms exist on the electrodes of the CRT, the deflection coils, and the centering control with a high resistance voltmeter, and an oscilloscope. If the proper voltages and waveforms are present, the fault is in the CRT. If the proper voltages and waveforms do not exist, proceed from the electrode showing voltage or waveform back towards the preceding stage to locate the defective component.

If, for example, the improper signal exists on the cathode of the CRT, the trouble may be in the intensifier and intensity compensation circuit stage, or in the gate circuit stage, or the sweep circuit stage. If the input of the intensifier or intensity compensation circuit stage is correct but the output is not, the trouble should be located within this circuit.

If improper input voltage to the intensifier and intensity compensation circuit stage exists the trouble preceeds this stage. If the gate circuit stage input is faulty, the intensity of the trace is not synchronized with the range sweep. If it is the gate circuit stage itself that is faulty there will be no range or height sweep. If the trigger **smplifier** and the gate multivibrator of this stage are functioning properly there should at least be height and range sweep. The trouble may then be in the countdown multivibrator of this stage.

If the range sweep generator stage is defective not only is the intensity of the sweep affected, but the range indication is also incorrect. If this condition is indicated by the trace on the CRT, check the input of the range sweep generator stage with oscilloscope to determine if the antenna cosine reference input is incorrect and if this is correct, check the parts within the stage.

If the correct potentird appears on the CRT cathode, but not on the control grid, the video amplifier stage or the preceding stages may be at fault. Check the several inputs of the video amplifier with an oscilloscope. If all the inputs are found to be correct, but the output is faulty the trouble must be in the video amplifier stage. If the video amplifier stage circuits are not faulty the preceding stages must be the cause of the trouble. The presentation on the CRT usually indicates which preceding stage is the cause of the specific fault in the CRT trace. If it is the video signal, itself, that is improper the trouble exists somewhere in the radar receiver, rather than in the

RHI. If the trouble is in the sector gating stage the CRT presentation will indicate improper sector angle or improper selection of azimuth. If this indication is apparent check for the proper antenna bearing synchro input with an oscilloscope. If the sector positioning input signal is not apparent at the sector gating stage input the preceding synchro or the servo amplifier stage may be at fault. If the synchro is functioning correctly check the servo amplifier.

If the CRT presentation indicates that there is no height line available, the failure is either in the height line generator stage, the range sweep generator stage, the gate circuit stage, or the antenna sine reference input. If any of these stages, other than the height line generator stage, are faulty, other CRT presentation failures will also be indicated. If, however, it is the height line generator stage, only the height line will be missing from the CRT presentation.

If the CRT presentation indicates that there are no range marks, the trouble must exist in the range mark generator since any faulty stages preceding the range marker generator stage would affect the presentation in some other way.

If there is no indication of height (or vertical direction) on the presentation of the CRT, the faihrre is in either the **antenna** sine reference input or the height sweep generator stage. If the antenna sine reference input is proper and present, the trouble must be in the height sweep generator stage.

Spiral Scan. Failure of the CRT high voltage supply or loss of the unblinking pulse would cause the indicator to be blank and produce a no-output condition. Check the CRT anode voltage with a voltmeter, and check the start-stop multivibrator for a positive unblinking pulse using an oscilloscope. Usually observation of the indicator will indicate the stage or stages which might be faulty. For example, if there are no range marks visible on the spiral trace and the display otherwise appears normal, the marker generator is most likely at fault. Check the output of the marker stage with an oscilloscope and, if no markers appear when an input pulse is applied, the marker generator is defective. Likewise, if range markers appear on the trace but no targets appear, there is probably no video signal applied to the cathode of the CRT. Check the cathode voltage on the CRT with a voltmeter and use an oscilloscope to check the video limiter input and the video amplifier output. If no video appears at the output with video applied to the input, either the amplifier or limiter

stages are at fault. Check the video limiter output to determine if it is at fault. If there is either no video input, or improper video input at the limiter it is obvious that the trouble is not in the scanning system but somewhere in the radar receiving system.

If there is no sweep apparent on the CRT but a bright spot exists at the center of the CRT, check for proper grid and cathode voltage with a voltmeter. If normal, either the sweep amplifier, sweep generator, or trapezoidal generator may be at fault. Check the output of the sweep amplifier with an oscilloscope and both inputs. If the inputs are normal but the output is improper the amplifier is at fault. If either input is faulty. Also check the input to the presumed faulty stage to make certain the proper input gate is applied. If normal sweep outputs are obtained, either the CRT is defective or the deflection yoke is open or shorted. Check the reistance of the yoke coils with an ohmmeter.

TV Scan. Failure of the CRT high voltage supply, the dc boost supply or a defective picture tube will usually produce a complete no-output condition with a blank CRT. Use a high resistance voltmeter and high voltage probe to check the high voltage, being careful to observe full safety precautions to avoid the possibility of dangerous shock. If the dc boost voltage is normal check the electrode voltages of the CRT. Failure of the dc boost supply can be caused by a shorted filter capacitor, a defective damper tube or circuit. Check the falter capacitor for a short with an ohmmeter and for proper value with an in-circuit capacitance checker. If the boost voltage is low, the darnper tube is bad. Usually failure of the damper circuit involving sweep components, such as a shorted output transformer or defective deflection yoke will also cause loss of sweep, and no raster will appear on the CRT screen. Check the coils for the proper resistance with an ohmmeter. Usually defects in the sweep will be found in the section at fault. If the horizontal sweep is faulty check the horizontal sweep stages from input to output with an oscilloscope. the point at which the waveform disappears or is distorted will usually indicate the circuit at fault. Likewise, for a faulty vertical sweep check the vertical sweep stages for input and output waveforms in a similar manner.

For example, if there is no vertical deflection, or a vertically rolling picture, or some other apparent trouble in the vertical scanning on the CRT, and the electrode and coil potentials have been checked, the trouble must exist in the vertical sweep stage or the integrator or clipper sections of the synch (pulse) separator. First check the input waveform of the vertical sweep amplifier with an oscilloscope. If the proper waveform is present but improper output exists, the trouble must be in this stage. If an improper input waveform is present check the input of the vertical oscillator with an oscilloscope. If the input waveform is proper, but the output waveform is improper, the trouble is within the vertical oscillator stage. If the input to the vertical oscillator is improper the trouble exists in the integrator or clipper sections of the synch (pulse) separator stage or in prior receiver stages. Also be certain to check that the vertical synch pulses appear in the input signal to the receiver.

If the picture on the CRT is horizontally rolling or if there are some other apparent horizontal scanning troubles, and the electrode and coil potentials have been checked and found correct, the trouble must exist in the horizontal sweep stage, the afc stage, or the differentiator or clipper sections of the synch (pulse) separator stage. First check the input of the horizontal sweep amplifier with an oscilloscope. If the input waveform is proper, but the output is improper, the trouble exists within the horizontal sweep amplifier. If the input of the sweep amplifier is improper check the input waveform of the horizontal oscillator. If the oscillator input is proper, the trouble is in the horizontal oscillator. If the oscillator input is improper check the inputs of the afc stage. If these inputs are correct, but the output pulse is incorrect, the trouble exists in this stage. If the input from the synch (pulse) separator stage is proper, but the input feeding back from the horizontal oscillator is improper, the trouble is in the feedback circuitry from the horizontal oscillator to the afc stage. If the feedback input is proper, but the input from the synch (pulse) separator stage is incorrect the trouble must exist in the differentiator or clipper of the synch (pulse) separator, or in preceding receiver stage, or in the horizontal synch pulse contained in the input signal to the receiver.

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# PART 9-3. ANCILLARY CIRCUITS

# **BLANKING CIRCUITS**

## Application.

Blanking is used in TV, radar, synchroscopes, and oscilloscopes to reduce the beam intensity and render invisible the retrace portion of the electron beam which produces the visible trace on the CRT.

#### Characteristics.

Blanking is dependent on the sweep signal.

Blanking reduces the intensity of the electron beam of the CRT.

Blanking is accomplished by application of negative voltage to the control grid.

Blanking circuit is a resistor-capacitor combination.

## Circuit Analysis.

**General.** Blanking circuits are used in CRT displays to prevent any indication of the retrace line from appearing with the display. This is accomplished by applying the sweep signal to an RC differentiating circuit, which develops a rectangular type waveform during the sweep discharge period. The rectangular (blanking) waveform is applied to either the control grid or the cathode of the CRT, depending on the polarity of the waveform. The rectangular waveform is usually connected in series with the CRT bias so that it increases the CRT bias and causes the electron beam to be cut off during the retrace time of the sweep, but has no effect on the beam during the active portion of the trace time of the sweep.

**Circuit Operation.** A typical RC blanking circuit is shown in the following illustration.



**Blanking Circuit** 

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Capacitor Cl and resistor R1 form a differentiating circuit. Capacitor C2 is a large a-c bypass capacitor which effectively places the lower end of RI at ground potentird. The sawtooth sweep voltage is applied to Cl and the charging current is relatively constant with the linear increase of the sweep voltage. Thus, the current flowing through R1 remains at a relatively constant and low value for the duration of the sweep trace. The voltage drop across Rl, likewise, remains at a small but constant value for the linear rise of the sawtooth sweep. This small positive voltage drop is small enough, however, so that it has little affect on the grid bias which it opposes. The intensity of the electron beam is, then, relatively unaffected.

When the sawtooth sweep voltage quickly retraces, however, the discharge current change is great and rapid. As Cl discharges the high discharge current through R1 produces a large voltage drop across R1 which is opposite in polarity to the drop produced across RI during the sweep. This retrace voltage series aids the normal negative grid bias applied to the control grid of the CRT. Hence, the bias voltage applied to the control grid of the CRT is now a large enough negative value to cut off the electron beam of the CRT, causing the CRT trace to disappear. The electron beam remains cut off during the entire retrace period, and for a short portion of the beg'inning of the trace period. Greater linearity of the sweep voltage and shorter retrace time of the sweep voltage causes the cutoff of the electron beam to extend less into the trace period.

A similar circuit may be used with a negative sawtooth **applied** to the input capacitor provided that the voltage across the resistor is applied to the cathode of the CRT. In this case a positive increase in bias is produced across R1, effectively driving the grid more negative and producing the same biasing-off of the beam.

## Failure Analysis.

**No Output.** If capacitor Cl were open none of the sweep voltage would be applied to the differentiating circuit and thus no voltage would be produced across R1. In this case, only the normal gird bias would be applied to the control grid of the CRT and blanking would not occur. To determine if Cl is defective, check it with an in-circuit capacitor checker. If resistor RI were open, not only would no voltage drop across it, but no grid bias would be applied to

the CRT and the screen would be brightly illuminated. To determine if RI is open, check the resistance with an ohmmeter. If capacitor C2 were open there would be no ground return, which would also cause no output to result. In order to determine if capacitor C2 is open check it with an in-circuit capacitor checker. If, after checking these components, the no output condition still exists the sawtooth sweep voltage must be faulty, or the grid bias supply voltage must be faulty. By checking the sweep voltage input with an oscilloscope and the grid voltage with a voltmeter, the faulty voltage will be located.

Low or Distorted Output If capacitor Cl becomes shorted the full sawtooth sweep voltage will be placed across Rl, resulting in a sawtooth grid waveform with the grid bias voltage opposing it, and the resultant voltage appearing at the control grid of the CRT. To determine if capacitor Cl is shorted measure the voltage between each plate of Cl and ground. If they are equal the capacitor is shorted. If resistor R1 is shorted no voltage can be developed across it. The voltage applied to the grid of the CRT will then be distorted. To determine if R1 is shorted, check R1 with an ohmmeter. If capacitor C2 were shorted the lower half of R1 would beat dc ground, and the grid bias supply would be shorted to ground. A certain amount of self grid bias would be generated by the flow of grid current through R1 and any grid signrd would probably be distorted if it was large enough to overcome the bias and illuminate the CRT. To determine if C2 is shorted check the voltage between each plate of C2 and ground. If the voltages are equal the capacitor is shorted. If the low or distorted output condition still exists the sawtooth sweep voltage or the grid bias voltage must be faulty. Check the sawtooth sweep voltage with an oscilloscope, arrd the grid bias voltage with a voltmeter to determine which voltage is at fault.

## DC RESTORER

## Application.

**The** dc restorer is used in CRT display systems to re-establish the dc level of the composite-video signal,

which is lost when the video signal is applied to the CRT control grid through a coupling capacitor from the preceding video **amplifier**.

## Characteristics

Maintains a constant bias level on the CRT control grid.

Receives input from video amplifier load.

Basic components are a diode, a capacitor and resistor.

Output signal waveform varies between the reference level and some positive value, which is determined by the peak-to-peak amplitude of the input waveform.

## Circuit Analysis.

**Generel. The** dc restorer consists of a diode connected in parallel with the resistor of a conventional RC coupling network. The diode is connected so that whenever the waveform swings in a negative direction the diode conducts and produces a short RC time constant; whenever the waveform swings in a positive direction the diode does not conduct, and this results in a long RC time constant. Thus, two different time constants are produced–a short time constant during the negative half cycle of the input waveform, and a long time constant during the positive hrdf cycle. It is this difference in time constants that produces a clamped output voltage at the required dc value, which is applied to the control grid of the CRT.

This voltage restores the dc components which was blocked by the capacitor coupling the video amplifier signal to the control grid of the CRT.

**Circuit Operation.** A typical dc restorer circuit is shown in the accompanying illustration within the dotted lines. The circuitry outside of the dotted lines is included in the illustration to clarify the explanation and function of the dc restorer.

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**DC** Restorer

V1 represents the plate circuit of the video amplifier. L1 and RI are the series peaking components of the amplifier. L2 is the shunt peaking coil and R3 is the plate load of the video amplifier. Cl couples the plate of V1 to the grid of V2, the cathode ray tube. Resistors R4, R6, and the dc restorer resistor **R5** form a grid leak biasing network for the CRT. Resistor R2 and capacitor C2 couple the video signal to the cathode of dc restorer diode V3.

As the negative video output pulse appears at the plate of Vl, it is capacitively coupled to the CRT grid. Since the coupling capacitor blocks dc, only the ac waveform appears on the grid. Without any dc restoration arrangement the pulse would establish an average voltage on the CRT grid which would change slightly with each different pulse. As a result, the maximum and minimum levels of the pulse would produce different intensities than they normally would with a freed bias level. By inserting a dc restoration circuit which in effect automatically controls the bias on the CRT to compensate for the loss of the dc component through the coupling circuit, a more faithful waveform reproduction is obtained.

When a negative output is applied through Cl to the CRT grid, a portion of this output is applied to the cathode of dc restorer diode V3 through R2 and C2, causing the diode to conduct. Current flow through R2, meanwhile, charges capacitor C2 in such a direction that the end of R5 closest to the CRT control grid becomes positive and reduces the total CRT bias. When the video pulse goes positive (becomes less negative) diode V3 ceases conducting. Meanwhile, C2 discharges during the positive portions of the pulse but only very slightly, due to the long time constant to ground offered C2 by R5 and R6. When the video pulse again goes negative, diode V3 conducts and restores the charge on C2 back to its former value. Thus if the average brightness is high, the negative swing from maximum positive to maximum negative value is greater, and diode V3 conducts longer causing a greater peak current flow and a greater positive charge appears across C2. Hence the CRT bias decreases further producing the greater brilliance. Conversely, when the negative swing applied to V3 is smaller, conduction of V3 occurs for a smaller period and less voltage is developed across C2. Consequently, the CRT negative bias increases by the reduction of charge voltage developed across C2 and a less brilliant signal appears. Parts values are normally chosen so the CRT bias is normal with V3 operating.

#### Failure Analysis.

No Output. Normally, failure of the dc restorer circuit will cause the CRT presentation to appear darker than normal. A quick check on operation is to remove diode V3 and note if the presentation changes. If there is no change, either the diode is defective or a faulty component exists. Check resistor R5 for proper value with an ohmmeter. With R5 shorted the dc restorer will not operate. If R5 is open no bias voltage will appear on the CRT grid when checked with a voltmeter. Also check R2 with an ohmmeter for proper value. If capacitor C2 is open the restorer will not operate, check C2 for value with an in-circuit capacitance checker. If C2 is shorted a positive bias will be placed on the grid of the CRT, and in all probability the CRT will be constantly illuminated. Do not neglect to check the values of R4 and R6 with an ohmmeter since they are a portion of a voltage divider across which the dc restorer

operates. If either is open no output will occur, but a change in value will not necessarily cause no output.

Impropar Output A defective V3 can cause a dark or distorted presentation. A shorted C2 can cause constantly illuminated display, check C2 with an in-circuit capacitance checker. It is important to remember that distortion or improper waveforms can occur in circuits prior to the dc restorer.

Therefore, when in doubt check both sides of Cl to ground with an oscilloscope. If the trouble exists on the input side of Cl the cause is not the dc restorer. If the trouble appears on both sides of Cl it is still necessary to eliminate components other than the dc restorer. In most instances a simple resistance and capacitance analysis will quickly reveal if any portion of the dc restorer is defective.

## DAMPER AND FLYBACK CIRCUITS

#### Application.

The flyback circuit uses the horizontal output transformer to supply sweep voltage to the horizontal deflection coils, while the flyback (retrace) portion of the horizontal sweep is used to develop the extremely high voltage necessary for the CRT anode. The damper circuit is necessary to eliminate any undesired oscillations occurring in the output circuit due to resonance in the horizontal deflection circuit, and to supply an additional dc low voltage boost.

## Characteristics.

Receives its power from the horizontal output sweep circuit.

Uses a special flyback transformer and two diodes to furnish both a high voltage and a low voltage from the same source.

Flyback transformer secondary supplies both horizontal sweep voltage to the deflection coils and high voltage rectifier **filament** voltage.

Flyback transformer primary operates as an autotransformer to furnish extremely high voltage developed at the sweep frequency of the high voltage **rectifier**.

Damper diode prevents undesirable oscillation and provides dc low voltage boost.

## Circuit Analysis.

**General. The** flyback transformer couples the horizontal sweep voltage output to the horizontal deflection coils. It also develops a high voltage for the

second anode of the CRT. This high voltage is produced when the sharp trailing edge of the sawtooth sweep voltage (the flyback or retrace portion of the sweep) causes the current in the deflection coils to collapse and induce a sharp reverse pulse in the primary of the transformer. Here it is stepped up by auto-transformer action and applied to the plate of the high voltage rectifier, where it is rectified, faltered, and applied to the second anode of the CRT.

The damper circuit is essentially a diode rectifier connected between the top side of the secondary and the bottom of the primary of the flyback transformer. This diode prevents the collapsing current in the deflection yoke during the steep trailing edge of the sawtooth sweep from causing continuous oscillation in the deflection coils. In rectifying these oscillations it also provides an additional dc voltage, for boosting the out-put of the low-voltage dc power supply.

**Circuit Operation.** There are many circuit arrangements which can produce flyback and damper operation. Therefore, circuit operation is devoted to an explanation of one of the most commonly used flyback and damper circuit combinations. This circuit arrangement is shown in the following illustration.



Flyback and Damper Circuits

In this circuit arrangement the plate of the horizontrd sweep output amplifier is tapped across part of the primary of flyback transformer **T1** (which

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operates as a high voltage autotransformer). The secondary (output winding) of transformer TI is connected across horizontal deflection coils L3 and L4 and associated capacitors C3 and C6 which are used to balance out the distributed capacity of the circuit. Inductance L1 is a width control for the CRT display. It is a small coil with a tunable core, and is shunted around a portion of secondary winding of T1. Adjusting the value of the width coil changes the total inductance of the secondary. The larger the total inductance vrdue, the greater is the width. Diode V3 is the damper tube. Inductance L2 and capacitors Cl and C2 comprise a simple pi-falter network for the darnper low voltage boost supply. The top of the primary of T1 is connected to the plate of high voltage rectifier V2, while the small power needed to heat the filament is supplied by a small single turn tertiary winding on T1, and is connected in series with protective surge and load resistor RI. Resistor R2 together with capacitors C4 and C5 form a resistance type of pi-falter network to eliminate any sweep frequency ripple appearing on the high voltage applied to the second anode of the CRT.

A positive-going sawtooth current applied to the primary of the flyback and darnper transformer develops a positive going voltage in the secondary to T1. This **produces** a rising deflection current through horizontal sweep coils L3 and LA. Diode V3 conducts during this period because of the positive potential present on the plate of damper tube V3. During the rising sweep V3 acts as a light resistive load and dissipates" a very small amount of the total power present. The resistive load of V3 and the resistive load of the deflection coils require a slight linear increase in the amplitude of the induced square wave to produce the required sawtooth current for the deflection coils. This is provided initially by a small amount of stored voltage in the coils.

The retrace of the sawtooth sweep causes the secondary voltage of T1 to drop to zero. This, in turn, causes the current in the deflection coils to collapse, and shock excites into oscillation the resonant circuit formed by the deflection coils and distributed capacity (the oscillation frequency is in the vicinity of 75 KHz). The first alternation of the flyback oscillation is a sharp negative pulse of high potential and V3 does not conduct during this negative transient. This negative spike, however, also appears across the secondary of T1 and it is inductively coupled into the primary of T1. Here it is

stepped up to a very high positive voltage by the large number of turns of the complete primary of T1. This voltage causes high voltage rectifier tube V2 to conduct and rectify the positive kickback pulses. The pulsating dc voltage from the high voltage rectifier is varying at a high ripple frequency and is easily faltered by the RC arrangement of capacitors C4, and C5, and series resistor R2, and is applied to the second anode of the CRT.

When a positive transient appears on the plate of V3, damper tube V3 conducts heavily. The oscillating transient is heavily damped by the load placed across the deflection coils by the damper tube. Before the transient oscillations are completed eliminated, however, the sawtooth sweep begins again. The combination of the heavily damped oscillations and the increasing sawtooth input produces a slight linear increase in the deflection coil current at the start of the sweep.

During the time that V3 is conducting, dc voltage is applied to the falter network consisting of capacitors Cl and C2 and inductance L2. This voltage is connected in series with the voltage from the lowvoltage power supply and provides a small dc voltage boost.

#### Failure Analysis.

**Note:** Although this type of circuit is designed to supply ordy a small output current from the high voltage supply to prevent lethal shock, be careful to observe standard high voltage safety precautions. It is important to discharge *both* the CRT anode and the high voltage filter capacitors before making voltage or resistance checks on the high voltage portions of this circuit.

No **Output.** Assuming that the input of this circuit, which is the output from the horizontal sweep output amplifier, is correct, a no-output condition could occur if the primary of T1 were shorted or open. In either case no voltage would be coupled to the secondary of T1, and no voltage would appear on the plate of the high voltage rectifier V2. Thus there would be no sweep voltage produced by the deflection coils, or high voltage on the second anode of the CRT. To determine whether or not T1 is defective, measure the dc resistance of the primary of T1 were open or shorted, no voltage could be coupled to the deflection coils, and no large negative kickback pulse would be developed for the production of the high

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voltage for the second anode of the CRT. To determine if the secondary of T1 is shorted or open check the dc resistance value of the secondary with an ohmmeter.

if horizontal deflection coils L3 and L4 were shorted or open no sweep would be produced and, likewise, no negative pulse would be developed for the production of the high voltage and the CRT would not be illuminated. To determine if L3 and L4 are open or shorted measure their dc resistance value with an ohmmeter.

If capacitor C6 were open no sweep voltage would be produced and no high voltage would be produced. Check the value of capacitor C6 with an in-circuit capacitor checker to determine if it is open.

Low or **Distorted Output**. If the input of this circuit is correct a low or distorted output could exist if T1 were partially shorted. Check the dc resistance values of the primary and the two secondaries with an ohmmeter.

If either L3 or L4 is shorted, or partially shorted, the sweep voltage will be distorted and a distorted pattern will appear on the CRT. While an improper kickback voltage value may be coupled to the plate of the high voltage rectifier the distortion may not create sufficient difference in value to show on a voltage check. Measure the dc resistance of L3 and L4 with an ohmmeter.

If capacitor C3 were shorted the same effect as a shorted inductance L3 would occur. To determine if C3 is shorted check C3 with an in-circuit capacitor checker.

If inductance **L1** were shorted or open, the voltage coupled from the primary to the secondary of T1 would be lower than normal resulting in a smaller

sweep and a lower high voltage value. To determine if inductance **L1** is shorted or open check the dc resistance value with an ohmmeter.

If diode V3 is shorted, the sweep voltage will be greatly decreased and show a smaller pattern on the CRT. The high voltage at the cathode of V2 will also be lower than normal, and the best voltage will also be low.

If falter components Cl, L2, or C2 were defective the boost voltage would be lower than normal. To determine if any of these components are defective, check capacitors Cl and C2 with an in-circuit capacitor check, and check the dc resistance of L2 with an ohmmeter.

If diode V2 were shorted or open no high voltage would appear on the CRT and the presentation would not appear. Check the voltage from the fdament of V2 to ground. If resistor R1 were open, V2 would not conduct and no high voltage would be available at the second anode of the CRT. Observe whether or not the fdament appears to be illuminated, if not check RI, for value with an ohmmeter.

If capacitor C4 were shorted, the high voltage would be grounded and none would be available at the second anode of the CRT. Measure the voltage from C4 to ground, if it is low or zero check C4 for proper value with an in-circuit capacitor checker. If resistor R2 is open no high voltage would be available at the second anode of the CRT. Measure the voltage of C4 and C5 to ground with a voltmeter. If the voltage on C4 is normal but voltage appears across C5, check the resistance value of R2 with an ohmmeter. If capacitor C5 were shorted the high voltage would be shorted to ground. Check C5 with an incircuit capacitor checker.

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# SECTION 10 DETECTORS

## PART 10-1. AM

## AM DETECTORS

## General.

Detector circuits are used to remove the modulation (transmitted intelligence) from a received r-f signal and transfer it back into its original form, so that it may be used for listening, viewing, communication, or other purposes. The process of detection is also called *demodulation*, which should not be confused with the special methods used for reducing the percentage of modulation.

There are many methods of detection and many circuit variations. Amplitude-modulation detectors will be discussed here. Other types of detectors are discussed later in this section. While the diode forms the basic detector, triodes (or other multielement devices can also be used to obtain additionl amplification, or can be connected to operate as diodes. When triodes (or other types of electron tubes) are used, the detector circuits are divided into two general classes - grid detectors and plate detectors. Square-law-detectors, small-signal detectors, largesignal detectors, or power detectors may be either grid or plate types. When detection occurs in the grid circuit, it is called grid *detection*; when it occurs in the plate circuit, it is called @rte detection. Grid detectors are usually small-signal detectors, and nearly always have a "square law" response, with the output varying as the square of the input voltage. This type of detection is characterized by extreme distortion (as high as 25 percent) at high percentages of modulation, in contrast to practically linear operation for diodes or plate detectors. Strictly speaking, from a technical standpoint every detector, whether considered linear or not, produces a certain amount of distortion; however, some circuits produce less than others.

Generally speaking, small-signal detectors are linear over a very small range of input voltages, and, as the input increases, so does the distortion. On the other hand, plate detectors are also linear when operating over small ranges at small amplitudes; but even though considered linear, the tube grid-plate transfer characteristic is never a perfectly straight

line, so that for large-signal inputs some distortion is produced. Large-signal detectors are called power detectors. They are designed to handle large input signal swings with as little distortion as permissible, and to produce large output voltages capable of driving power amplifier tubes directly. The actual power involved is relatively small though being on the order of milliwatts; consequently, with the present day multipurpose tubes and techniques, the power detector is used mostly for special purpose applications. In fact, with the present day trend to superheterodyne receivers, which feed the large output of the i-f stages into the detector, most of the high-grain detector circuits are no longer used (or needed) and are supplanted by the simple diode detector. In the less complex types of receivers, however, the highgain detectors are still favored.

The grid-leak type detectors depend on the flow of grid current for their operation, and are used where sensitivity is more important than lack of distortion. The grid-bias detector (also known as the *linear plate* detector, the infinite-impedance detector, etc) is used where a large output with low distortion is needed. The heterodyne detector is used for the reception of unmodulated (CW) signals and for single-sideband applications. The regenerative detector (which may be grid or plate) is used where high sensitivity provided by regenerative feedback is desired, usually in two or three-tube receivers. The super-regenerative detector, which utilizes maximum regenerative feedback without producing oscillations, is used where the lack of gain in the stages preceding the detector makes its use desirable. The autodyne detector is essentially a regenerative detector with sufficient feedback to produce oscillation so that it can be used for unmodulated CW reception, as well as AM reception.

The semiconductor diode detector for AM is used in one of two types of circuits: the *voltage-output* circuit and the *current-output* circuit. (In other texts these circuits may be called "series diode detector and shunt diode detector". ) Although semiconductors operate basically by virtue of a changing *current*, when current is passed though a resistor a *voltage drop* is produced across the resistor. Therefore both types of circuits are applicable to either

tubes or semiconductors, and the functioning is similar regardless of whether tubes or semiconductors are used. The voltage output circuit is usually preferred for electron-tube applications.

Because of the lack of gain in the diode detector, transistors are also used for detection. The transistor detector provides amplification of the detected signal. With the proper circuit comections and bias it can be made the semiconductor equivalent of the grid, plate, or infinite-impedance electron-tube detector. By suitable arrangement of biasing potentials and proper selection of the transistor, either square-law or linear detection can be achieved.

While the semiconductor diode detector is **used** universally in electron-tube equipment, the transistor triode detector is generally used only in all-transistor equipments. When used, the transistor detector is limited to the common-base and **common-emitter** configurations because of the less-than-unity gain provided by the common-collector circuit.

## **DIODE DETECTORS (ELECTRON TUBE)**

## Application.

Diode detectors are used to remove the modulation from the received r-f carrier and convert it into the original intelligence transmitted. These types of detectors are usually used in superheterodyne receivers, or in receivers supplying a large input signal to the detector. They are also used in test equipment where linear detection is required (particularly in vacuum-tube voltmeter applications) and as field strength indicators for transmitters.

### Characteristics.

Operates linearly over a large range of input voltages.

Has a relatively constant input impedance which is independent of the input voltage.

Does not amplify the input signal.

Distortion produced for normal operation is on the order of 1 to 2 percent.

## Circuit Analysis.

**General.** The ideal detector produces no distortion in the process of detection, and reproduces the modulation signal exactly as it was before modulation

of the carrier. There are three forms of distortion possible in the detection process, namely, amplitude, frequency, and phase distortion. When extra frequencies are developed in the demodulation process that did not exist in the original modulation, the result is a form of amplitude distortion. When the detector is more responsive to some frequencies than to others, frequency distortion results. When the phase relationships between the modulation frequencies are changed, phase distortion is produced. The diode operation, while considered linear, is not perfectly so; that is, instead of a straight line relationship between the input and output, the tube transfer characteristic is curved, especially at the low end. Thus, for small signals (on the order of millivolts), a nonlinear or distorted output is obtained. Actually, for small signals the diode operates as a square-law detector; that is, the output varies as the square of the input voltage. Thus like the grid detector, which also operates on a curved transfer characteristic, the greater the percentage of modulation, the greater the distortion (a maximum of 25% distortion). To minimize this form of amplitude distortion, which is inherent in the diode construction and cannot be eliminated, the diode detector is usually operated with large input voltages. In other words, it is used only after numerous stages of r-f or i-f amplification, so that the signal to be demodulated is on the order of volts. It is evident that while a steady signal can be made to produce no distortion, a signal which varies in amplitude from zero to some maximum value will produce a slight amount of distortion whale operating near its zero value, even with many stages of amplification. Hence the nominal rating of 1 to 2 percent distortion for diode detection. Finally, excessive capacitive reactance shunting the detector load will cause a dropping of output at the high audio frequencies (above 10 kHz), producing a phase shift of the high frequencies as compared with the low and medium frequencies, and thereby causing distortion. Thus it is clear that, while the diode is considered the best of the large-signal detectors, it does produce some distortion.

Since the diode is a **two-element** electron tube, it operates essentially as a simple half-wave rectifier, similar to the power rectifier used to supply plate voltages, except that it operates at radio frequencies

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rather than at powerline frequencies. Like the power rectifier, the diode detector must also have a filter (rf) to minimize ripple voltage at the carrier frequency. Similarly, it produces a dc output voltage, plus the audio-frequency modulation component. Since the detector supplies a voltage to the audio amplifier stages following it, full-wave rectifier circuits are occasionally used to supply greater output with less faltering. For most applications, however, the simple half-wave rectifier connection is used because it requires fewer components, is cheaper to produce, and has sufficient output for present-day audio stages.

Although the diode consumes little power in the detection process, it does place a load on the input stage; it is usually considered to act as if it were a resistor of half the load-resistance value, shunted across the input circuit. Normal efficiency ratings are better than 80 percent, with 90 percent being the rule rather than the exception. This is true because the loss in the diode is small, since the diode plate resistance is usually much less than the detector load resistance.

**Circuit Operation.** Two forms of the basic diode circuit are shown in the following illustration, with circuit A being the most prevalent in use. Both diode circuits are identical in operation, but circuit B offers an alternative output connection (accross capacitor C) if desired, and, since the capacitor is in series with the input and the diode, it prevents the low dc resistance of the input transformer secondary from shunting the diode local at the signal frequency.





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For simplicity, the following illustration shows an untuned input transformer; actually, in most modern receivers, both the primary and secondary circuits are tuned. Where high-Q circuits with extreme selectivity are employed, some of the high-frequency sidebands are removed by the narrow pass band; as a result there is a lack of high-frequency response in the detector output. This effect, however, is not inherent in the detector–it is due to poor design of the tuned circuits.

Basic operation consists of the charge and discharge of the R-C circuit, which uses the voltage developed across R to charge C to nearly the peak voltage of the input signal. When the plate is positive with respect to the cathode, the diode conducts and charges capacitor C. Since there is a small voltage drop in the diode between cathode and plate when conduction occurs, it is apparent that the maximum developed detector voltage can never be exactly equal to the peak applied voltage, but will depend upon the ratio of load resistor R to the resistance of the diode. Therefore, the detector efficiency can never reach 100 percent, though it does average around 90 percent. However, if C is too large, its low reactance in parallel with R will shunt the signal, and a lower output will result. Detector charge action and discharge action are shown in the accompanying figure for the tone-modulated input waveform of A; B, C, and D illustrate the charge and discharge of the capacitor. On each positive half-cycle of the radiofrequency signal, capacitor C charges to a maximum value as determined by the percentage of modulation. On each negative half-cycle, capacitor C discharges at a rate fixed by its circuit time constant. As shown in waveform B, the time constant is too slow, and C cannot discharge fast enough to follow the modulation on the negative swing before the next positive r-f half-cycle begins; consequently, the negative portion of the modulation signal is effectively chopped off, and a distorted output results. The time scale is exaggerated to convey the idea more clearly. In contrast to the time constant just considered, the time constant of example C is too fast, and the average output drops to a low value. Example D shows the effect of a proper time constant. It is evident from the examples that either too fast or too slow a discharge rate (time constant) will distort the received-signal waveform.



**Detector Charga and Discharge Action** 

From part E of the figure, it is evident that the modulation consists of pukes at the carrier frequency and that the amplitude is proportional to the modulation percentage. Also, it can be seen that at zero modulation a carrier frequency voltage exists which is proportional to the carrier amplitude. Thus across load resistor R is developed a dc voltage for automatic volume control use, which will be discussed more fully in a following paragraph. It can also be seen that a carrier-frequency ripple will exist; that is eliminated by use of a low-pass falter (in addition to the bypassing action of C, whose reactance is small at the carrier frequency).

From part E of the figure, it is also evident why the diode detector can be considered as a half-wave rectifier. For linear operation and assuming perfect rectification, the diode would conduct only on the positive excursions of the modulation signal, remaining inoperative on the negative signal excursions. In this case, the positive excursions are the signal above the f. line, and the negative excursions are the signal below the line. Thus, only the positive portion of the modulation signal is rectified, and the output consists of pulses of current at the modulation frequency. These pulses of current are used to charge and discharge capacitor C and thereby produce the audio output voltage of part D, as explained previously.

A typical diode detector circuit with an r-f filter is illustrated in the following figure. The input transformer (T3) has both primary and secondary tuned for maximum selectivity.



**Typical Diode Detector** 

The r-f filter consists of Cl and **R1** acting as a low-pass filter arrangement assisted by C2. Capacitor

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C2 performs a dual function: in conjunction with R2 it can be considered to form a low-pass r-f filter, and it can also be considered as a straight bypass across load resistor R2. In either instance, however, it helps eliminate any r-f remaining in the i-f carrier, and also develops an audio output voltage in accordance with the average value of the diode load current passing through load resistor R2.

Design Considerations. When the plate of the diode is more positive than the cathode, current flows, producing a voltage drop across load resistor R2 which follows the modulation signal. Current flow on the positive signal swing is limited only at saturation, which normally does not occur even with very strong signals at 100 percent modulation. As the modulation signal swings in the negative direction, the current flow diminishes until the negative peak is reached, where it again reverses and increases (assuming a sine-wave signal). On strong signals with high percentages of modulation (over 75%), however, peak clipping may occur. The clipping effect is produced by the inability of the diode to conduct when the plate becomes negative with respect to the cathode. Even with the unmodulated carrier signal, noise effects produce conduction in the diode and provide a small residual average dc voltage which makes the cathode positive with respect to the plate, Thus, on the negative peaks of the modulation signal, with large signal swings and percentages of modulation between 80 to 100 percent, the output voltage is driven to zero, the extreme portions of the negative peaks are clipped off, and the output voltage no longer follows the modulation signal, With improper design, this distortion can be as great as 10 to 12 percent; the practical diode detector, however, is not operated at levels which produce such excessive distortion, and a normal value of 1 to 2 percent is maintained.

The diode detector is also subject to a reduction of output at the higher audio frequencies (above 10 kc) because of the capacitive shunting effect of C2 on load resistor R. Note also that when the reactance values of any of the detector bypass capacitors become low for the frequency of the modulation signal being detected, R1 and R2 are effectively connected in parallel, reducing the load resistance and output voltage. The same effect holds true for the resistance-coupled load of the amplifier stage following the detector. When the reactance of the coupling capacitor becomes a low-resistance path for

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the audio signal, then the grid input resistance of the audio stage is effectively in parallel with both RI and R2, and the reduction in output voltage is particularly noticeable at high gain settings of the volume control. This a-c shunting of the diode load is taken into consideration in the design, so that normally no effect on operation is noticed unless parts values have changed.

# Failure Analysis.

**No Output.** A no-output condition is usually limited to an open or short-circuited component or a defective diode. With an open input transformer, stray capacitive coupling may feed enough signal through to produce an output. With an open diode load resistor or a short-circuited bypass capacitor, however, no output will be obtained. Usually, a resistance analysis will quickly locate the defective component.

Low Output. Lack of sufficient input signal will cause a low output, and could be due to poorly soldered (high-resistance) joints or to a defective input transformer. Low tube emission may also cause a weak output, although it usually shows up as a fading signal on a strong local station. An open load bypass capacitor will reduce the output, as only the average current flow through" the load resistor will now prerduce an output. A lack of r-for i-f amplification preceding the detector can also cause low output; therefore, it is necessary to isolate the detector by checking with a TVTM for adequate input and output. Since no amplification is produced in the diode detector, but the detection efficiency is high, an output indication lower than 10 percent of the input indication would be indicative of possible detector trouble.

**Distortad Output Since** diode detection is linear, a distorted output signal usually indicates component changes. Amplitude distortion is a definite indication of nonlinearity in the detector, provided that the input signal to the detector is linear. Lack of high audio frequency response would be directly traceable to excessive selectivity, caused by regeneration in the preceding i-f stages or to excessive capacitive shunting of the detector, particularly in video applications. Distortion at high volume levels with a strong, heavily modulated local signal would indicate normal peak-clipping effects. Poorly soldered (high-resistance) joints can be suspected when component values and tube emission are normd. Fringe howl or a tendency

toward oscillation would indicate a lack of r-f filterring. Because of the simplicity of the circuit, an oscilloscope waveform check should quickly locate the trouble.

# VOLTAGE OUTPUT DIODE DETECTOR (SEMICONDUCTOR)

# Application.

The semiconductor diode detector with a voltage output is usually used as the second detector in superheterodyne receivers, or as a linear detector where large input signals are supplied. It is also used in test equipment where linear response is desired, as in VTVM'S and field strength indicators.

#### Characteristics.

Operates linearly over a large range of voltage.

Does not amplify the input signal.

Has an average efficiency of approximately 90 percent.

Normal large-signal distortion is on the order of 1 to 2 percent.

Is not restricted to any particular frequency range, but is operable on the entire electronic spectrum.

## Circuit Analysis.

General. The principal difference between a tube diode and a semiconductor diode is the reverseleakage current of the semiconductor, plus a difference in current and voltage ratings. As far as the diode detector is concerned, the reverse-leakage current is usually negligible. Although it does produce a slightly increased loading effect on the input circuit, this increased loading is of interest only when the diode is operated as a small-signal detector. In this instance operation is not linear, but observes a square-law response (output varies as the square of the input voltage). It is this weak-signal square-law response which creates the inherent distortion in the diode detector. As normally operated, the diode voltage-output detector is employed after a number of stages of amplification. Thus, the input signal to the detector is relatively large in amplitude, the response is relatively linear, and the basic fidelity of the diode detector is achieved.

**Circuit Operation.** A simplified schematic of the voltage-output diode detector is shown in the following figure.



Voltage-Output Diode Detector

From this figure it can be seen that diode CR is in series with the input voltage; it acts as a simple rectifier, with RI as the load and Cl as the filter. The diode conducts only during the positive half-cycle of the input signal. During the negative half-cycle it remains inoperative, since it is then reverse-biased. When the diode conducts, current flows through R1 and produces a voltage drop across the resistor. The voltage developed across RI is equal to the peak value minus the drop across the diode (which is very small and much less than in an electron tube diode). Since capacitor Cl is connected in parallel with R1 it changes to the same voltage. Since the diode response is considered linear, the larger the input voltage the greater the current through R1 and the larger the charge on Cl. As the positive half-cycle ceases, the diode ceases conducting and capacitor Cl discharges through RI for the duration of the negative halfcycle. The capacitor discharge is controlled by the time constant of RI and Cl, and is not quite completed before the positive half-cycle again begins. The diode again conducts, and capacitor Cl is again charged for the duration of the positive half-cycle. Since these alternations are at radio-frequency rates and the RC time constant is on the order of seconds, the voltage to which Cl is charged never has time enough to reach the full peak value of the input voltage, and the voltage to which Cl is discharged never has time enough to reach zero value. The voltage is, however, proportional to the envelope of the modulation, rising as the input signal amplitude increases, and falling as the input signal amplitude decreases, as shown in the following illustration. Thus, the voltage across Cl is a nearly linear replica of the original modulation.



**Detector Waveforms** 

When the time constant of R1 and Cl is too short (capacitor, resistor, or both are too small), the capacitor voltage cannot follow the envelope (it reaches full charge before the signal reaches its peak), part of the signal is lost, and the detected modulation is distorted. When the time constant is too long, the capacitor tends to smooth out variations in the modulation (it cannot respond to very fast voltage variations–only slow variations), and distortion occurs. With the proper time constant, the capacitor is never fully charged or fully discharged, but rather follows the peak excursions of the envelope in accordance with the audio modulation.

## Failure Analysis.

**No Output.** A no-output condition can occur from failure of the diode to conduct, from an open or shorted load resistor, or from a defective capacitor. A resistance and continuity check will determine whether the resistor is satisfactory, whether the diode front-to-back resistance is normal, and whether the capacitor is short-circuited. With the resistor and diode checked out, it is a simple matter to connect a capacitor in parallel with the suspected capacitor to determine whether it is open (an output will appear if the capacitor is open). If an oscilloscope is available,

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it may be used to observe the waveform across the load resistor.

Low Output. Low output can occur from a change in the time constant of the circuit, or from a lack of sufficient input to the detector to produce the desired output amplitude. Poorly soldered connections, a leaky capacitor, or a defective diode can cause this condition. Under normal operation, the amplitude of the signal across the detector should be from 80 to 90 percent of the input amplitude. Less than this value indicates lack of efficiency due to increased resistance in the diode or leakage in the capacitor.

**Distorted Output.** This can result from a change in capacitor value. Either too large or too small a capacitor will cause distortion. A change in a resistor or capacitor value, producing too short or too long a time constant, will also cause distortion. The parts should be within 10 to 15 percent of their rated values. If the values are normal, the trouble must be in the diode. A high-resistance condition caused by a poorly soldered joint is always a possibility.

# CURRENT OUTPUT, DIODE DETECTOR (SEMICONDUCTOR)

#### Application.

The current output diode detector is used to detect the audio modulation in semiconductor receivers, where the voltage output is small and does not vary sufficiently to produce full output from the audio amplifier states.

## Characteristics

Is usually self-biased.

Linear current swings produce linear output voltage swings.

Impedance at the output is low, and usually direct coupling is employed.

Is inherently a small signal detector.

## Circuit Analysis.

**Generel.** The current form of diode detector operates similarly to the voltage form of diode detector. Except that the output variations are in the form of current pulses rather than voltage pulses. However,, by passing this current through a shunt resistor, a voltage output is developed across the resistor. The voltage output is, however, much reduced so that a

current amplifier is required to build up the signal to a respectable output level. Thus, while the voltage detector will supply an output which can drive the following audio stage, the current detector usually utilizes direct coupling and an additional transistor stage to control another transistor stage in the output. Because of the direct coupling, response is somewhat better. On the other hand, the higher frequency signals are slightly attenuated by the coil reactance of the series inductor, which operates similar to the power supply low pass filter. This has the effect of eliminating any high frequency ripple and distortion in the output, so that practically the response is identical to the voltage diode but of lesser magnitude. Actually the current detector operates as a square law detector and is usually used in circuits other than the superheterodyne (which uses the voltage form of detector). Therefore, the shunt diode (current) detector is used mainly in regenerative receivers of the pocket variety and is usually combined with reflex audio circuits to provide a loud but distorted output.

**Circuit Operation.** The circuit of a typical current diode detector is shown in the following illustration.



Current Diode (Shunt) Detector

As shown, the diode is connected in shunt with the input circuit, and L1 is connected in series, with load resistor RI also connected in shunt to ground. The LR combination of L1 and **R1** have a combined time constant which is satisfactory for detection.

When the input signal is applied across CR1 the output is shunted to ground for the negative half cycle of the r-f input signal because CR1 conducts

and no output occurs. During the positive half-cycle the signal is applied to L1 and current flows through RI to ground and produces an output current which follows the r-f envelope. This action occurs because of the integrating effect of the LR circuit. During the current flow through Ll and RI to ground a field is built up around L1 with tends to keep current flowing in the same direction when conduction ceases, and during the time that the detector diode is shunting the signal to ground, the field discharges through RI. Thus an integrating action occurs similar to that which would be produced if R1 were shunted by a capacitor, and the output current follows the peak waveform closely. Because of the reactance offered to high frequencies by L1, there is always a loss of voltage which makes the output smaller than the applied signal. Since a conducting path to ground is offered on the positive half-cycle of input signal, the rectification efficiency is lower than for a series connected diode (voltage detector) hence this circuit is not often used. In addition the low shunting effect during conduction and the low overall impedance to ground during the nonconducting period provide a heavy load on the source, and creates distortion when sufficient driving power is not available. Thus, the shunt detector is usually less preferred than the higher impedance, voltage-output form.

## Failure Analysis,

**No Output.** If the diode is shorted, or if either L1 or R1 are open there will be no output. Because of the few components involved a resistance check with an ohmmeter will usually locate the defective part.

Low Output. A defective diode CR1, high resistance soldered joints, or large changes in L1 or R1 can reduce the output. Check the values of L1 and R1 with an ohmmeter.

**Distorted Output.** If the output is continuously distorted, check the diode. If the distortion still persists, use an oscilloscope to observe the input and output signals, since the distortion is probably located in an earlier r-f stage or a later audio stage.

# DIODE DETECTOR WITH AVC (ELECTRON TUBE)

Application.

The diode detector with AVC is universally used in broadcast, TV, communications receivers, and other

high-gain superheterodyne circuits to provide automatic gain or volume control with detection, in a signal tube or envelope.

## Characteristics.

Operates linearly over a large range of voltage.

Input impedance is relatively constant and independent of the input voltage.

Does not amplify the input signal.

Maximum distortion is of the order of 1-to-2 percent.

AVC output voltage varies directly with the amplitude of the input carrier.

## Circuit Analysis.

**General.** The diode detector with AVC is identical to the diode detector without AVC, except for the circuit arrangements provided for AVC take-off. Discussion of the operation of the detector in stripping-off the modulation from the carrier is covered completely in the discussion of the Electron Tube Diode Detector earlier in this section of the Handbook. The reader should refer to the previous discussion for proper background before preceding with this discussion.

**Circuit Operation.** The schematic of a typical diode detector arranged for AVC take-off is shown in the following illustration.



**Diode Detector With AVC** 

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The plate of VI is connected to IF input transformer T1 and the cathode is grounded. Resistor R1 with capacitors Cl and C2 form low-pass RF filters, while C3 and R2 are audio and decoupling falters. The audio voltage is developed across volume control R3, and applied through coupling capacitor  $C_e$  to the following audio amplifier stages.

When unmodulated, the input consists of a single frequency. When modulated, the input consists of a basic carrier frequency plus an upper and lower sideband containing the modulation. Thus the diode detector output always contains a dc component which is directly proportional to the carrier amplitude or strength. This is the voltage which is used for AVC. For large signal detection the diode detector is considered to be a simple half-wave rectifier, which conducts as long as VI plate is positive with respect to the cathode. When VI conducts, election flow is from the grounded cathode to the plate, through the secondary coil of IF transformer T1, R1, and R3 to ground. Thus current flow through R1 produces a negative voltage at point A (which is not used), and the AVC voltage is developed across volume control R3 at point B. This negative voltage drop is applied through R2, back to the grids of the r-f and i-f stages. Because the feedback of the AVC bias is to the grids of the preceding stages it is clear that there must be no extraneous modulation or RF on this lead. Otherwise, both the audio and RF components could again be amplified and redetected causing distortion and unwanted feedback. Therefore, R1 and C1 and C2 are connected as a conventional low-pass falter in series with the current flowing through R3. The output waveform at point A consists of the dc and r-f component as shown in the following waveform illustration for an unmodulated carrier for ease of discussion. The instantaneous r-f carrier component  $(e_{car})$  is bypassed to ground partially by Cl. During the positive portion of each carrier cycle C2 is charged through R1, and during the negative portion of the carrier signal the capacitor tends to discharge.



**Detector Voltage Relationships** 

The result is the heavy curve labelled  $E_0$ . The average value of pulsating voltage  $E_{DC}$  is the actual AVC voltage. Since these pulsations occur at radio frequency rates, the effective voltage variation between charge and discharge of the capacitor is so small as to be negligible. Recall from the above discussion that the modulation component of the signal is also present. However, when modulated signals are detected, these audio ripples are smoothed out by another low-pass falter consisting of R2 and C3. In this instance, the value of the filter time constant are such that output voltage E. appears as a straight line (pure de). The time constant of R2 and C3 is made sufficiently large so that it takes more than a single audio cycle to charge or discharge. Although this increase of time constant prevents on instantaneous change of AVC voltage for an instantaneous change in carrier level it is usually satisfactory for most types of fading encountered. Particularly, since decoupling RC networks similar to R2 and C3 are also inserted at each tube grid associated with the AVC and increase the effective values of R2 and C3. The fast time constant response necessary for single sideband or CW use is obtained by making the value of C3 much lower than is normally used in AM circuits. Since the grids of the controlled stages do not draw grid current, there is no flow of current through R2,

other than that required to charge the other decoupling capacitors on the AVC line. Hence there is no large voltage drop, and the RC filter can be used without encountering any losses because of excessive current drain. The detected audio or ac component appears across volume control R3 and is applied through coupling capacitor  $C_e$  to the audio amplifier stage.

## Failure Analysis.

No Output. Lack of an input signal due to failure of the associated receiver circuits, a detuned or defective IF transformer, T1, a defective diode, V1, or open or short circuited parts will cause a no-output condition. Measure the voltage to ground at points A and B with a high resistance voltmeter. A negative voltage at these points indicates normal functioning. Lack of voltage at these points indicates either lack of an input signal or a defective component. Use a VTVM or an oscilloscope to determine if an input is present, With an r-f signal on the primary, but not on the secondary, T1 is defective. If the secondary voltage is much lower than the primary the secondary tuning needs adjustment. When adjusting, if it still provides a low output and does not respond to the adjustment, T1 is defective. If either R, R2 or R3 is open, the series circuit will be interrupted and no AVC voltage will appear at points A or B. If R1 or R3 is shorted, no AVC voltage will be developed; however, if R2 is shorted the circuit will still operate. With normal AVC voltage but no audio output, either volume control R3 is tuned down, R3 is defective, or coupling capacitor C may be open. A resistance check will determine if these parts are open or shorted. If Cl or C2 are shorted, no AVC voltage or detected output will be obtained. Use an ohmmeter to measure the resistance to ground, or an incircuit capacitance checker Cl and C2. If the parts are satisfactory, diode V1 must be at fault.

Low Output. A weak input signal, or low emission in the detector diode are the prime cause of low output, as well as mistuning of T1. The effects of humidity can also cause circuit leakage which reduce the output. Although a slight change in parts values with age may cause a reduction of output, it most probably would go unnoticed, since turning up the volume slightly would restore the output to normal. If it becomes necessary to turn the volume control excessitively for a known signal, first check the preceding circuits to be certain that they are operating properly and are not at far.dt, before trouble-shooting the detector.

**Distorted Output.** If the values of Cl and C2 changed sufficiently to produce the wrong time constant, either too fast or too slow, distortion would occur. Likewise, if the emission of V1 is so low as not to supply the full peak current demand, distortion caused by clipping will also occur. Check the values of Cl and C2 with an in-circuit capacitance checker. A change in the values of R2 and C3 will change the attack time of the AVC loop but will not normally cause distortion. However, if C3 should short-circuit, the AVC voltage would be grounded out and the stages preceding the detector would operate at maximum sensitivity, and probably cause overloading with consequent distortion.

# DIODE DETECTOR WITH NOISE LIMITER (ELECTRON TUBE)

## Application.

The diode detector with noise limiter is usually used in radiotelephone reception to prevent noise pulses from interfering with, or garbling, voice transmissions.

## Characteristics

Operates linearly over a large range of voltage.

Input impedance is relatively constant and independent of the input voltage.

Does not amplify the input signal.

Noise peaks are clipped without excessively increasing the distortion.

#### Circuit Analysis.

**General. The** diode detector with noise limiter is identical in operation with the Diode Detector described earlier in this section of the Handbook, except for the noise limiting circuitry. The reader should refer to the previous discussion for proper background before proceeding with this discussion.

Both shunt and series types of noise limiters are used. The series type continually conducts but stops conducting when a noise pulse arrives, and thus leaves a gap in the signal in place of the noise pulse. The shunt type noise limiter conducts only when the noise pulse exceeds a predetermined bias level, shorting the input to ground, and also leaves a void in the signal. Since these noise pulses and consequent

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signal holes are of short duration, the integrating effect of the ear on the sound minimizes this effect. In most practical noise limiters, the limiter becomes effective at around the 85 percent modulation level, so that subsequent peak flattening causes some distortion and a slight loss of audio volume. The voice, however, is understandable through heavy noise interference, which would otherwise completely mask or garble the intelligence being transmitted.

**Circuit Operation. The** schematic of a typical diode detector with noise limiters is shown in the following illustration.



**Diode Detector With Noise Limiters** 

Diode VI is the detector diode which rectifies the input signal from I-F transformer T1. Resistors R1 and R2 form a voltage divider load for diode detector VI, bypassed for RF by Cl. The detector voltage appearing across R1 is applied to the anode of series noise limiter V3. Resistors R5 and R6 form a bias voltage divider from a separate negative supply to ground, to supply a fixed negative cutoff bias to the anode of shunt diode limiter V2. Resistor R6 is bypassed by capacitor C4 so that any instantaneous voltage change appearing at the anode of V2 is bypassed to ground. Resistors R3 and R4 together with capacitors C2 and C3 form a low-pass falter and load circuit for series diode V2. Capacitor  $C_c$  is the detector output coupling capacitor.

When an unmodulated input signal is applied to the primary of IF transformer T1, the secondary voltage appears across diode V1 and V1 conducts for the duration of each positive r-f pulse, causing a flow of current from the cathode to plate, through T1 secondary, R1 and R2, back to the cathode and ground. A negative de voltage thus exists at point A on the schematic and varies in amplitude directly with the r-f carrier amplitude. This is the AVC voltage discussed in the previous circuit for the Diode Detector (with AVC), in this section of the Handbook. When the input signal is modulated, the negative voltage at point A also varies slowly at audio frequencies in accordance with the modulation. At point B the detected voltage is identical with that at point A except that it is smaller than at point A because of the drop across resistor RI. The RC lowpass filter combination of R3 and C2 charges capacitor C2 relatively slowly so that audio frequency signals are effectively smoothed out. Low pass falter R4, C3 operates similarly except that the time constant is faster to ensure that no r-f component appears at point C to cause feedback. Thus both falters place the cathode of series diode V3 on a common negative bus, and the drop across RI (between points A and B) appears as a forward bias on the anode of V3 (point A is more negative than point B). Thus diode V3 normally conducts, and the detected pulsating voltage at point B appears undistorted at point C, and is applied through coupling capacitor C<sub>c</sub> as the audio output of the detector. Because RI and R2 form a voltage divider, the detected voltage to ground which appears across R2 is considerably smaller than the developed AVC voltage. When a negative noise burst appears at point B, the anode of series limiter V3 is instantly driven highly negative, while the cathode voltage changes very slowly because of the slow filter time constants provided by R3, C2, and R4, C3. Thus for most of the noise burst, conduction of diode V3 is stopped and no output appears (a hole occurs in he output). Thus the noise spike is chopped off the detector waveform, and because it occurs for such a short time, the instantaneous loss or signal goes unnoticed. When the noise burst occurs for a long period of time or is a repetitive occurrence, the loss of signl may be noticed. For random short noise pulses this type of limiter is fairly effective.

Note also that when the negative noise bursts occur, the negative voltage at point A is increased,
## **ELECTRONIC CIRCUITS**

and if it is fed back as an AVC voltage change the overall sensitivity of the receiver will simultaneously decrease, just when a strong signal is needed to overcome the adverse signal to noise ratio. Therefore, shunt limiting diode V2 is connected from point A to ground. Normally, the negative plate voltage, which appears on V2 from voltage divided R5 and R6 connected across the separate negative bias supply, holds V2 in a nonconducting condition. When a negative noise burst appears and is of sufficient amplitude to drive the cathode of V2 more negative than the fixed biased anode, V2 conducts and the voltage at point A is temporarily shunted to ground via V2 and resistor R6. Capacitor C4 bypasses R6 and allows the instantaneous noise burst to be discharged to ground. Meanwhile, the relatively slowly moving dc component produced by AVC action remains relatively unaffected. Consequently, the AVC voltage does not instantaneously increase (or decrease) and is effectively prevented from desensitizing the receiver during the noise burst. Thus conduction of diode V2 effectively removes the noise spike from the signal. Although the entire noise spike is not eliminated, the large peak amplitude above the fixed-bias level is removed so that the effect of the noise is considerably reduced by the shunt diode. In addition, the shunting effect of diode V2 on the detected audio temporarily reduces the signal supplied to the audio stage via series diode V3, and produces a noise silencing effect. The use of both a shunt and series diode although not absolutely necessary provides better overall noise limiting performance.

# **Failure Analysis**

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**No Output.** Any open circuited or short circuited condition as well as defective diodes can result in a loss of output. Lack of a negative voltage to ground at point A indicates a possible defective IF transformer T1, diode VI, or that RI or R2 are open, or Cl is shorted. Use an oscilloscope with an r-f probe to determine if an input exists on the primary of T1. A large signal on the primary, but none at all or a very minute one on the secondary indicates that T1 is defective. With an input across the diode, check the resistance of RI and R2 with an ohmmeter, and check Cl for a short. If an output can be observed at point C with the oscilloscope, but not on the other side of Cc, check coupling capacitor  $C_c$  with an

in-circuit capacitance checker. If these parts are satisfactory diode V1 or V2 is at fault (an output at point C indicates that V1 is not at fault). Failure or defects of the remaining parts and diodes will not normally produce a no-output condition, but instead will produce a low output or ineffective noise elimination.

Low Output. A partial shunting of the detector output through diode V2 can occur if V2 is shorted, if the negative bias supply voltage fails, if R5 or R6 change in value, or if capacitor C2, C3, or C4 is either shorted or leaky. The capacitors may be checked for shorts with either an ohmmeter or an in-circuit capacitance checker, and the resistors can be checked with an ohmmeter. If diode V3 is defective, the output will probably be very low and distorted, depending upon the stray capacitance in the circuit.

**Distorted Output.** Since in normal operation the noise limited effectively eliminates a noise signal, it is evident that the output waveform will always be different than the input waveform to a certain extent. Thus a slightly distorted output will practically always be obtained. The degree of the distortion depends upon the design of the circuit. Theoretically, the limiter should operate only on noise pulses which are larger in amplitude than the signal; however, most practical circuits start operating at about the 85 percent modulation level. Hence some peak clipping of the signal usually occurs and causes distortion on the modulation peaks. In normal operation, a slight amount of distortion will be noticed and the strength of the output signal will drop noticeably when the noise limiters are activated. Follow the signal through the circuit with an oscilloscope and notice where the distortion occurs, Further resistance checks of the associated parts with an ohmmeter will usually locate the defective part.

## **GRID-LEA K DETECTOR**

#### Application.

The grid-leak detector is used in simple two-orthree tube receivers, such as the regenerative type. Since this type of detector is particularly susceptible to overload and distortion at high levels of modulation, it is never used in modern high-gain superheterodyne receivers.

#### Characteristics.

Is self-biased by a grid-leak.

Provides good sensitivity with increased signal gain.

Operates as a square-law detector for small signals and as a linear detector for large signals.

Is subject to overload and blocking effects on strong signals.

Although it produces a relatively larger output voltage than other comparable AM detectors, it is subject to more distortion.

## Circuit Analysis.

General. The grid-leak detector, basically, uses a triode electron tube, and is considered to operate similarly to a diode detector with the added advantage of triode amplifkation. Although pentodes have been used to provide additioml gain, the triode with a **low** plate voltage is usually preferred because of a reduction in tube noise and distortion. In operation, the grid and cathode of the triode operate similarly to the anode and cathode of the conventional diode detector (discussed previously in this section of the Handbook). The dc bias produced by carrier rectification and the detected modulation appear across an RC network known as the grid-leak, and the modulation appears in amplified from in the plate of the triode. Since the detection occurs in the grid circuit it is known as grid detection. Because the developed grid bias is automatically controlled by the carrier amplitude, the grid-leak detector operates over a wide range of input voltage. On weak signals it operates near zero bias and uses the curved lower portion of the grid-current, grid-voltage characteristic to provide an output which varies as the square of the input signal, and is known as non-linear (square-law) operation. For large signals and large self-bias it operates over the linear portion of the characteristic curve. When overloaded by extremely strong signals, the bias reaches cutoff and conduction occurs for only part of the cycle, and the peaks are clipped, creating excessive distortion. The detailed operation of this detector under different conditions is discussed in the following paragraphs.

**Circuit Operation. The** schematic of a typical gridleak detector is shown in the following illustration.



**Basic (Series) Grid-Leak Detector** 

The r-f input is applied through r-f transformer T1, and the grid-leak network consisting of RI and Cl are connected in series with the grid of V1 and the output of T] secondary, while the cathode is grounded. In the plate circuit, resistor R2 is the plate load, and is isolated from the plate r-f component by radio frequency choke RFC. The plate is also bypassed to ground by capacitor C2, which is small enough to act as a shunt for the r-f carrier voltage appearing in the plate circuit but not the modulation. Thus only the amplified modulation appears across load resistor R2 and is applied to the output through coupling and plate voltage blocking capacitor Cc.

In the absence of an input signal, V1 is contactbiased by grid-leak resistor RI, and operates near zero bias. In this condition, only a small potential is built up across RI by grid current flow, biasing and grid slightly negative. Thus V1 is in a position to respond to both positive and negative signal variations for small signal detection. The following waveform illustration demonstrates how the curvature of the grid current versus grid voltage characteristic of V1

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distorts the basic signal and produces amplification with distortion.



**Small Signal Detection Characteristics** 

As shown in the illustration, when the input signal increases in amplitude grid current increases, flowing in the direction of the arrow on the schematic. Thus grid capacitor Cl is charged negatively during the positive grid swing. On the negative grid swing, grid current flow is reduced and the capacitor discharges slightly through the grid-to-cathode resistance which is lower than the high resistance grid-leak. Because of the curvature of the grid characteristic curve, the positive excursions are larger than the negative excursions. Therefore, a slowly increasing average grid current is developed as the signal modulation rises, and the average grid current falls when the signal modulation decreases, in synchronism with the modulation envelope. This develops a negative voltage across RI, which varies at the audio rate of the modulation around the negative bias level produced

by the constant amplitude carrier pulses. Since the grid of V1 controls the operation and plate current of the triode, the change of grid voltage produced by the detected signal causes an identical but amplified plate current fluctuation. As this plate current varies in accordance with the modulation, a similar but amplified voltage is developed across plate load resistor R2. This is the audio output voltage which is coupled through C to the following audio amplifier stage. Because the r-f carrier voltage appears between the grid and the cathode of V1 it also appears in the plate circuit. Therefore, there is an r-f plate component of voltage which must be eliminated so that it can not cause spurious beats with the modulated signal, or unwanted oscillation by feedback within the tube. This is the function of RFC and C2. The r-f choke offers a high inductive impedance at the carrier frequency, while capacitor C2 offers a low impedance shunt path to ground. Hence, the r-f component is bypassed around the load resistor and power supply, and has no effect on circuit operation. Only the relatively slowly moving audio frequency current component flows through load resistor R2, to produce a corresponding audio frequency output voltage.

For large signals, the average carrier amplitude also rises, so that the grid is biased considerably negative, and only the positive excursions of r-f voltage on the input signal are effective in causing grid current flow. In this condition the detector operation is similar to a half-wave rectifier, and operates as a linear detector. The positive signal excursions produce a negative voltage across the grid leak by charging capacitor Cl. During the negative signal excursions the charge on Cl keeps VI inoperative so that the tube operates for a half cycle or less. Because maximum modulation peaks produce maximum negative grid voltage, the plate current of V1 is reduced during modulation. The reduction of plate current occurs at an audio rate and produces a corresponding audio output. As the current through detector output load resistor R2 reduces, the voltage across it and the output rises, as shown in the waveforms illustrated in the following figure of large signal detection characteristics.

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Large Signal Datection Characteristics

The linear grid detector is also known as a gridleak *power* detector. In the small-signal or square-law grid-leak detector the output voltage although amplified is usually greatly distorted, therefore, large output voltages create greater overall distortion. In the power detector, the grid-leak values are reduced to prevent excessive distortion, and the input signal and the detector plate voltage are increased to provide a greater output. Thus the larger input signal produces operation over a larger output voltage swing, producing a greater output voltage with less overall distortion.

In operation, the major difference between the two types of detectors is obtained by making the large-signal, power-detector grid potential swing sufficiently negative that the flow of grid current is stopped for the major portion of the negative half cycle. During the positive half cycle of carrier voltage, grid current flow charges the grid capacitor negatively. During the next negative half cycle, some of this accumulated charge leaks off through the grid-Ieak resistor (which is connected across Cl), and is replenished during the next positive swing. Thus grid current can only flow for a small portion of the positive cycle. In the small-signal grid detector, however, grid current flows continuously, since the grid is never driven sufficiently negative to reduce grid current flow to zero. Under these conditions, the charge on the grid capacitor leaks off through the internal grid-to-cathode resistance, which is much lower than the high value of grid leak resistance used. --In the large signal power detector the grid-to-cathode resistance is practically infinite during most of the cycle (because grid current is cut off'). Operation of both detectors is essentially the same as shown in the waveform illustration for the small signal detector, except that the grid amplitude of the large signal detector is greater, and the grid current cut-off point corresponds to the value of bias developed by the carrier signal. Whereas in the small signal detector the grid bias is always less than grid-current cutoff.

As in all electron tube amplifiers, the platecurrent, grid-voltage characteristic curve is linear up to the point where saturation begins. So that both the lower and upper regions of operation are curved. If the large signal power detector is driven sufficiently, the bend on the upper portion of the curve will also cause plate rectification to occur. Thus second and third harmonic distortion components will be produced and the overall detector distortion will increase. It is also necessary that the charge and discharge of the grid-leak follow the signal amplitude during large signal detection, otherwise, blocking and distortion will occur. With proper choice of grid-leak constants (which is inherent in good design) and an adequate plate voltage which does not exceed tube ratings, the distortion can be kept to low values almost equivalent to that of the diode detector. If the input signal is reduced to a very small value, the large signal power detector merely operates as a smallsignal, square-law detector with a low output and the advantages of power detection are lost.

The schematic of a typical shunt grid-leak detector is shown in the following illustration. Components are symbolized identical to. and operate exactly as explained for the series grid-leak detector discussed above. This circuit is generally used for the power type detector because slight advantages are claimed for avoiding blocking effects. The shunt grid resistor

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provides more loading on the tuned r-f input circuit, however, and produces a reduction in selectivity.



Shunt Grid-Leak Detector

## Failure Analysis.

No Output. An open or shorted grid of plate circuit, a defective tube, or an open coupling capacitor, Cc, can cause loss of output. Measure the plate supply and plate voltage with a high resistance voltmeter. Normal plate voltage indicates that load resistor R2 and the RFC are probably satisfactory and that C2 is not shorted. Apply a modulated signal from a signal generator to the input terminals of r-f transformer T]. Use a VTVM, electronic voltmeter or an oscilloscope (it must offer high impedance so as not to load or disturb the circuit operation) connect between grid and ground, to determine if the input signal produces a slight negative bias and if a signal is present. If no signal is present, T1 is defective. If the detected signal can be observed in the grid circuit but not in the plate circuit, VI is defective. If the signal is present in both grid and plate circuits but no output exists, check coupling capacitor C<sub>c</sub> for an open circuit. (Use an in-circuit capacitance checker).

Low Output. Low plate voltage, a defective tube or too weak an input will each cause a reduced output. The weak input signal may occur because r-f transformer T1 is not tuned to resonance. If T1 will not tune to resonance, either the signal frequency is out of range or T1 is defective. When in doubt, apply a modulated input from a local signal generator and note that the signal peaks in intensity as the resonance point of T1 is reached. If this occurs but the desired signal is still weak, additioml r-f amplification or a better antenna are required. If the signal generator cannot produce a strong output, the detector is probably at fault. Check the plate voltage of VI: if the plate voltage is normal, either V] is defective or output coupling capacitor C is leaky or paretically open. If the plate voltage is not normal but is lower than usual, R2 may have changed value, the rfc may have developed a high resistance, or C2 may be leaky or shorted. Use an ohmmeter to check the resistance of R2 and the RFC, and check the resistance of C2 to ground. Replace any part which has a resistance higher or lower than that specified in the technical manual for the equipment. If the detector seems to be operable but the receiver output is low, it is possible that the audio stages following the detector are at fault, and not the detector circuits. To check the audio stages, use an audio signal generator and apply it to the output stage plate, then to the grid and note if the signal increases. Follow this procedure back to the detector to locate the defective audio stage.

**Distorted Output.** Excessive distortion can be produced by a change in the constants of the grid-leak network, by too high a plate voltage, or as a result of low emission from VI. If replacing the tube with a known good one does not eliminate the distortion, check the plate voltage with a high resistance voltmeter. If the plate voltage is normal, check the value of R1 and Cl with an ohmmeter and capacitance checker. If the grid-leak components are within tolerance value and distortion still occurs, it is possible that the input signal is too strong and overloading is causing the distortion. It is also possible that T1 is only tuned near resonance and the sidebands are being clipped. Tune T1 properly, and reduce the input signal, if possible.

# PLATE DETECTOR

### Application.

The plate detector is used in small receivers as a power detector. It is usually used in tuned r-f receivers to supply a large audio output. While it can be used in the modern superheterodyne, it camot be used to supply a simple AVC voltage. Thus, it is usually more economical and simpler to use a diode

detector. The plate detector is, however, extensively used as the detector circuit in vacum tube voltmeters and similar test equipment.

#### Characteristics.

May use either self- or **fixed-bias** (self-bias is most prevalent).

Provides good sensitivity and increased signal gain. Operates as a linear detector for large signals.

Is normally operated with large input signals as a power detector.

Distortion is considered to be slightly less than that of the grid-leak detector, and not better than the diode detector.

# Circuit Analysii.

General. The plate detector usually operates class B, that is, it is biased to plate current cutoff, and for this condition it operates as a large signal linear detector. When used for small signals, or as the detector of a vacuum-tube voltmeter it operates on the lower curvature of a class A biased tube characteristic, and is a square law detector. In the plate detector there is no rectification of the signal in the grid circuit. The r-f input signal causes the ac grid voltage to vary the tube plate current, producing both amplification and detection. Detection occurs in the linear plate detector because only one side of the signal (the positive portion) causes the tube to conduct, while the negative portion remains below cutoff and has no effect. Thus the plate output varies in accordance with the r-f envelope of the modulated carrier as shown in the following waveform for linear detection. The square Iaw detector operates





over both the positive and negative variations of the input signal. Because of the curvature of the tube  $e_g/i_p$  characteristic for small input signals, an amplified but distorted plate output results. The large positive grid swing produces a greater plate current than the smaller negative swing. Thus the average output is greater during modulation than without modulation, as shown in the following waveform illustration.

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Square Law Operation

Since the output varies as the square of the input signal, at 100 percent modulation the maximum distortion can be as high as 25 percent. Operating as a linear detector the distortion is considerably less, as long as the signal is strong enough to keep it from operating in the lower curved portion of the tube characteristic, and not so large as to include operation over the upper curved portion. However, since the  $\mathbf{e_g/i_p}$  characteristic curve of a tride is never perfectly straight but has a slightly howed appearance, there is greater basic distortion than in the half-wave diode detector.

**Circuit Oparation.** The schematic of a typical plate detector is shown in the following illustration.

Transformer T1 is the r-f input transformer, with the transformer secondary tuned by Cl. Cathode bias is obtained from R1 and C2. The plate load R2, is bypassed for R-f by C3. The output is capacitively coupled through Cc.

With no signal applied, the average bias produced by cathode current flow through RI holds the grid to plate current cut off. Although spoken of as cutoff bias, the tube is actually biased to projected cutoff, as shown in the following illustration. (See the introduction to the Amplifier Section of this Handbook for a detailed explamiton of cathode bias.) Therefore, negative input signal excursions occur over the curved portion and produce some slight distortion. For full linear operation a separate and higher fixed bias is always applied and the complete negative

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excursion of the input signal is eliminated with a consequent reduction of overall distortion.



**Detector Operation Characteristic** 

When an input signal is applied, the positive portion of the signal increases the grid voltage, and the plate current of VI follows, likewise. Thus the plate waveform of **V1** consists of pulses of current at the input frequency, whose peak values trace out a curve which varies exactly as the modulated r-f. Thus the audio frequency component of plate current developes a similar plate voltage output waveform across the plate load resistor R2 of opposite polarity or phase. Thus at the peak of current, the plate and output voltage is a minimum, while at the minimum value of plate current the output voltage is maximum. Capacitor C3 bypasses any r-f which might appear on the plate of V1 after rectification, to avoid feedback through the plate to grid capacity causing oscillation or unwanted beats. In some instances, C3 may be bypassed to ground instead of to the cathode, this is usually done in receivers operating at the higher radio frequencies.

Normally, no grid current is drawn and the plate detector offers an extremely high input impedance

with practically no input loading. Since the input circuit is not loaded down, a slight improvement in selectivity is usually observed over that of the gridleak detector. If, however, the input is large enough to draw grid current (signal exceeds the bias), additional plate distortion is obtained by curvature of the upper portion of the tube characteristic, and the lowered grid input impedance also reduces the selectivity, so that the overall performance is lower than for the grid-leak detector.

#### **Failure Analysis**

No Output. An open input or output circuit, or a defective tube, as well as lack of plate voltage, will cause a **no-output** condition. Check the plate supply and plate voltage with a high resistance voltmeter. No output with a normal supply voltage, but with no plate voltage indicates that plate load resistor R2 may be open, or that bypass capacitor C3 is shorted. Check the resistance of R2 with the plate voltage off, and check C3 with an in-circuit capacitance checker. If plate voltage is normal but no output is obtained, use an oscilloscope and r-f probe to observe that an input signal exists on the grid of V1. If it does and no output exists, either cathode resistor R1 is open or V1 is defective. Check the bias voltage across R1 with a voltmeter. Since bias bypass capacitor C2 may be shorted, it is usually simpler to measure the resistance of R1. If the resistance across R1 is zero, the C2 is shorted. If RI is infinite it is open. Also, do not neglect the possibility of a shorted secondary winding or tuning capacitor Cl.

Low Output. A low plate voltage, a defective tube, or a small input signal will produce a low output. Check the supply voltage with a voltmeter. If normal, check the plate voltage of Vl; lower than normal voltage on the plate indicates that R2 has increased in value, or that an abnormal plate current exists. Check the voltage between cathode and ground, if it is normal or slightly low check R2 for the proper resistance value (with plate voltage off). If T1 is defective, or if Cl is not tuned to resonance a low output can also occur. If T1 primary is open, a weak output signal may still be obtained if there is sufficient capactive coupling between primary and secondary, or to VI grid. In this case, while Cl will tune through resonance there will not be the normal large build up of output signal as the resonant point is passed. If T1 is defective, a resistance analysis can be made with an ohmmeter to verify if the windings are open, but there is also the possibility of a short circuit or leakage across one of these windings. To determine if T1 is at fault, temporarily disconnect it from VI grid and connect the input signal through an isolating capacitor direct to VI grid. A large increase in signal indicates that T1 must be defective. The output of a modulated signal generator tuned to the input frequency can be used to supply an input directly to the grid of VI, if a known strong local signal is not available. If the output signal obtained in this case still is weak, but increases considerably when the generator output is applied to the plate circuit, tube VI is at fault. Where all signals fade in and out and the output is low, VI is usually at fault because of low emission.

Distortion. Since there is normally some distortion from the linear detector, particularly on strong signals at high percentages of modulation, there may be some doubt as to whether or not the distortion is normal or excessive. When distortion is suspected, check the plate voltage and cathode bias with a voltmeter. Abnormal voltages indicate that the detector is probably at fault. If, however, it is found that tuning Cl eliminates the distortion, or that it only exists on extremely strong signals, the detector is most likely performing normally. When the distortion continuously occurs with either weak or strong signals the detector is definitely at fault. Note, however, that when strong fading exists it is possible that selective fading is phasing out some of the sideband frequencies and causing the distortion. Such distortion will not appear on signals having a steady amplitude.

# COMMON-EMITTER DETECTOR

#### Application.

The common-emitter transistor detector is usually used in semiconductor superheterodyne receivers to supply a detected and amplified output.

#### Characteristics.

Uses self-bias.

Offers a high input impedance.

1s equivalent to the diode detector in quality, with more gain available.

May be operated as either a small-signal, or a large-signal detector, depending upon bias voltage.

# Circuit Analysis.

**General.** This detector is equivalent to the grid and plate detector used in electron tubes. The baseemitter ,junction acts as a diode rectifier for largesignal linear detection when biased sufficiently, or as a square-law, small-signal detector when operating with low bias. When used in a receiver with only a few transistors it operates as a small signal detector, when used in superheterodynes it is used as a large signal detector. The operation is similar to that of the electron tube counterparts (grid and plate detectors) described earlier in this section.

Diode detection occurs in the base-emitter junction and amplification occurs using the emittercollector junction. The combination can be considered the same as that of a diode and a transistor used separately.

**Circuit Operation.** The schematic of a typical transistor common-emitter detector is shown in the following illustration.



**Common-Emitter Detector** 

Tuned input transformer, T1, has a primary and secondary winding. The primary winding, L1 is tuned by capacitor Cl to the operating frequency (in superheterodyne receivers it is tuned to the IF), while secondary L2 remains untuned and inductively coupled. Resistors RI and R2 are fixed-bias voltage dividers connected from the supply to the base and ground. Resistor RI is bypassed by C2 for radio frequency and this RC combination also acts as the load resistor and bypass capacitor as used in a diode detector. The audio is detected in the base-emitter circuit and is applied as a dc bias varying at audio frequencies to control collector current. The output is developed across collector load resistor R4, which is bypassed for r-f but not for audio frequencies. The emitter is connected to ground through a conventional swamping resistance (R3) for temperature stabilization, and is bypassed by C3 for both RF and audio.

In the absence of an input signal, transistor Q1 rests in a Class A-biased condition, drawing a moderate but steady collector current, and no output is obtained. When an input signal appears on the base of QI it is rectified by the base-emitter junction (operating as a diode) and appears as a dc bias voltage with a varying audio frequency component across RI. This a-f component is developed across RI as in the conventional diode detector previously discussed earlier in this section. Variations in base current flow caused by the input signal develop a voltage across R1 which follows the modulation envelope of the signal, any degenerative bias which tends to develop across emitter resistor R3 is eliminated by bypass capacitor C3. The output is developed by collector current flow from the supply through R4 which varies under control of the bias voltage across R1. Any radio frequency ripple in the output is bypassed across the collector load resistor by capacitor C4. The audio frequency variations, however, are not bypassed, and as the base is forward-biased by the negative half-cycle of input, it increases collector current flow, and a positive output voltage is developed across load R4. Likewise, when the base current is made to decrease on positive portion of the input signal (which reverse-biases the junction) collector current flow is reduced, and the collector output voltage rises towards the supply (becomes more negative). Thus since the output rises and falls in accordance with the modulation envelope, an amplified output of similar waveform is obtained and passed through coupling capacitor Ccc to drive the base of the following audio stage.

When a small fixed-bias is applied Ql, operation is on the lower (curved) portion of the base-emitter transfer curve and square law detection is obtained, with an increase of distortion. When biased higher (on the straight portion of the curve) the transistor operates as a linear diode detector with the additional amplification supplied by the collector circuit. The type of operation is determined during design by selecting the proper values of RI and R2 to provide the desired bias for square law detection, and by choosing the proper value of emitter resistor R3 and bypass capacitor C3 for linear detection. The output in both instances is equivalent to that from a separate diode, amplified by a separate transistor operating at the same bias voltages. Usually when operating as a high-level (large signal) detector it is capable of driving an audio output stage directly. In this respect, it is the transistor equivalent of the electron tube power-detector.

# Failure Analysis.

No Output. Loss of an input signal, lack of bias, a defective transistor, loss of supply voltage, an open load resistor, or an open output capacitor can produce a no-output condition. Check the bias, supply, and collector voltages with a high resistance ohmmeter. If normal base bias is obtained, L2 and bias, divider Rl, and R2 are satisfactory, and C2 is not shorted. Likewise, with normal collector voltage R4 is okay and C4 is not shorted. An emitter voltage slightly larger than the bias applied and still no signal indicates that R3 and C3 are operating satisfactorily and that either L1 is open or Cl is shorted. Check the input circuit for continuity and shorts with an ohmmeter. The possibility exists that coupling capacitor Ccc may be open. In this instance, use of an oscilloscope would immediately show an output on the transistor side of Ccc, but nothing on the output side. When an oscilloscope is available, follow the signal through the circuit and note where it disappears or changes in shape or amplitude to locate the trouble.

**Low Output.** Improper bias, low collector voltage, or a defective transistor are the most likely causes of low output. Check for proper bias and collector voltage, and also check the supply to be certain that a blown fuse or the supply itself is not the cause. With normal voltages, the transistor must be defective.

Distortion. Normally the output is distorted to a certain extent, however, the modulation should be intelligible. When it is so distorted that it is garbled, check the output circuit to make certain the trouble is not in the following audio stage. When the distortion appears in the output stage but not in the detector, the trouble is in the output stage. Improper bias is usually the foremost cause of excessive distortion, and should be checked first with a *voltmeter*.

# **ELECTRONIC CIRCUITS**

DETECTORS

If the bias voltages are normal, use an oscilloscope and follow the signal through the circuit until the pattern changes and shows the part at fault. It is important to remember to use an r-f probe when checking with the oscilloscope, since distortion in the r-f portion of the circuit will not show unless it is first detected by an r-f probe.

# COMMON-BASE DETECTOR

#### Application.

The common-base detector is usually used in small portable semiconductor receivers to provide detection with some amplification, and where extreme fidelity is not required.

## Characteristic%

Employs grid-leak bias.

Is equivalent in output to a diode and a separate amplifier stage.

Produces more distortion than the commonemitter detector, or a diode detector.

Operates as a small signal detector which can easily be overloaded.

## Circuit Analysis.

**General. The** common-base detector is the transistor equivalent of the electron tube grid-leak detector. Detection occurs in the base+ mitter junction and amplification occurs through use of the collector junction. The output is the equivalent of a diode detector followed by a stage of audio amplification, but with more inherent distortion. Where less distortion and better quality are required a separate diode and transistor audio stage are used.

**Circuit Operation.** The schematic of a typical common-base detector is shown in the following illustration.





Transformer T1 is an r-f transformer when used in simple two or three stage receivers, or an i-f transformer when used in superheterodynes. It is tuned to either the i-f frequency or the operating frequency, as applicable. In the drawing TI is single tuned in the secondary, but may also be tuned in the primary. Resistor R1 and capacitor Cl form a grid-leak bias network which sets the operating point of the emitter junction. The audio output is taken from the collector circuit through audio output transformer T2, however, RC coupling may be used to help improve fidelity if a smaller output is satisfactory. The primary of T2 forms the detector output load and is bypassed for r-f ripple by capacitor C2.

The input signal is applied to either the tuned or untuned primary and inductively coupled to the L2 secondary. When tuning capacitor C is tuned to the proper frequency, the input signal is coupled through Cl to the emitter. In the absence of a signal, contact bias exists as determined by resistor RI. The small

flow of reverse current develops small bias voltage across R1 which is near zero and only the small normal reverse current flows. When the positive portion of the input signal occurs, current flows through the emitter-base junction driving the emitter positive (forward bias) and capacitor Cl is charged negatively, establishing the operating point. On the negative excursion of the input signal capacitor Cl is discharged through RI creating a negative, reverse-bias which reduces conduction in the emitter junction. The bias developed follows the wave envelope of the modulated signal and produces a dc emitter bias which varies at audio frequencies. Variation of the emitter bias causes the collector current to flow in accordance with the audio frequency variations of the modulation, and the output voltage is developed by collector current flow through the primary of audio transformer T2. Capacitor C2 effectively acts as a low pass filter, and filters out any r-f or i-f component (ripple) existing in the collector circuit. Thus only the audio variations induce a voltage in the primary of T2, and the field around the secondary of T2 varies in accordance with collector current changes, inducing an output voltage in the secondary. Strong signals may develop to much bias on the emitter, cut off collector current flow, and cause blocking. Since the bias ordinarily is small, the transistor operates on the lower portion of the emitter-base transfer characteristic curve and is a square law detector. Thus, at 100% modulation, distortion up to a maximum of 25 percent can exist. Such high values of distortion render this type of detector unsuitable for music or high fidelity broadcast use, except in cheap receivers in which the distortion can be tolerated for the sake of simplicity, economy, and portability.

## Failure Analysis.

**General.** When making voltage checks use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of conventional voltohmmeters. Be careful, also, to observe proper polarity when checking for continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output. Lack of collector voltage**, an open input or output circuit caused by a defective transformer (T] or T2), or a defective transistor can cause

a no-output condition. Measure the collector voltage with a VTVM. Normal collector voltage on Q1 indicates that T2 and the output circuit are satisfactory. If no collector voltage exists, either T2 is open or C2 is shorted. Use a volt-ohmmeter and a capacitance checker to check these two parts. When collector voltage exists but there is no output, check TI primary and secondary for continuity with an ohmmeter and tuning capacitor C for a short circuit. There is also the possibility of Cl being open. Use an ohmmeter and capacitor for proper value. If T1 is satisfactory the transistor must be at fault.

Low Output. Lack of collector voltage or an open output circuit, as well as a defective transistor can cause a reduced output. Measure the collector voltage, if it is normal, either output transformer T2 is open or shorted, or Q1 is defective. Check the transformer for continuity or short circuit with an ohmmeter, and check C2 with a capacitance checker.

**Distorted Output. The** output will normally be distorted, but should be intelligible. If the distortion is so bad that the modulation is garbled, check the input and output waveform with an oscilloscope. If the waveform is undistorted in the base circuit but appears distorted in the collector circuit, check the values of Cl and R1. Since these parts set the bias point, a change in the value of either one can cause clipping or peck distortion effects. If these parts values are proper and within the tolerance indicated in the instruction book on the equipment, the transistor is most likely at fault.

# INFINITE IMPEDANCE DETECTOR (ELECTRON TUBE)

### Application.

The infinite impedance detector is used in tuned radio frequency receivers where less distortion than that supplied by the conventional plate detector is required, and no gain through the detector stage can be tolerated. Its light loading effects improve sensitivity and selectivity.

# Characteristics.

Uses self-bias, but can be fixed-biased, if desired. Provides good sensitivity, with reduced distortion. Operates as a linear detector for large signals.

Is normally operated as a modified power detector.

The cathode output connection prevents any large increase of gain.

Presents a very high or infinite impedance to the input signal.

## **Circuit Analysis.**

General. The infinite impedance detector is also known in other texts as a *reflex* detector because of the large value of degenerative feedback provided in this arrangement. However, this nomenclature is misleading since it also applies to reflex circuits where detection and amplification through positive feedback occur in the same stage, and these circuits are not infinite impedance detectors. The basic infinite impedance detector used a bypassed plate load to achieve more than unity gain. In effect, it combined the advantages of plate detection with the equivalent of diode detection which offered no load to the source. The circuit is always easily recognized because of the cathode output comection, large cathode resistance, and relatively small r-f bypass (about 250 picofarads), plus the fact that when the plate resistor is used the plate bypass is sufficiently large enough for both RF and audio bypassing (about 0.1 microfarad). Because of the infinite impedance offered this circuit does not load the input. Consequently, greater sensitivity and selectivity is obtained than with conventional plate detectors. On the other hand, it is not as sensitive as the grid-leak detector, but the output is practically distortionless and much lower than is normally obtained by either the plate or grid types of detectors previously discussed. If not better, it is at least as good as the conventional diode detector. The two major disadvantages which restrict its use, is that it cannot supply a simple source of AVC, and the negative feedback through cathode degeneration produces less than unity gain.

**Circuit Operation.** The schematic of a typical infinite impedance detector is shown in the accompanying illustration.





Transformer T1 is the r-f input transformer, and is tuned by C1 (in superheterodyne **receivers** T1 represents the i-f input transformer). Cathode bias is supplied by R1 which is only bypassed for RF by C2 so that it is degenerative at audio frequencies. The output is taken from across R1 **through** coupling capacitor Cc. Resistor R2 and capacitor C3 form a plate filter and voltage dropping network, which reduces the plate voltage and bypasses to ground any rf or audio currents in the plate circuit. In some circuits R2 is not used, while in other circuits both R2 and C3 are eliminated. In either event, there is no change in circuit operation.

By using a large value of resistance for R1, the average plate current flow through this resistor develops a high bias. Thus, in the absence of an input signal only a small plate current flows because of the cathode bias is almost at plate current cutoff value. Since current flow through the tube is from cathode to plate, any increase in cathode current develops a positive voltage at the cathode with **respect** to ground and increases the instantaneous bias. However, RI is bypassed by C2, which is chosen to offer a low impedance to ground for radio frequencies, but not for audio frequencies. Consequently, the r-f signal does not pass through the load (cathode resistor RI)

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but the audio frequency variations of the modulation on the detected signal do. Thus a degenerative voltage is developed on the cathode, which makes the output signal amplitude always less than the input signal which produces it. This is a form of negative feedback which places the output signal in series with the gridcathode circuit. Since the output signal appears in opposite polarity to the input it helps cancel a portion of the input signal, eliminates distortion, and improves linearity. (See the Amplifier Section of this Handbook covering Feedback Amplifiers for a complete discussion of inverse or degenerative feedback.) Because of the degenerative feedback inherent in a cathode output connection, the output signal amplitude can never exceed the input signal, and the gain is always less than unity.

Another result of the feedback action is to prevent the flow of grid current. The increase of bias with increase of signal ensures that the input signal never exceeds the bias, hence grid current will never flow. Thus the infinite impedance detector always presents a very high (infinite) impedance between grid and cathode, and produces no load on the input circuit. Consequently, there is no shunt load across the secondary of T1 and Cl, and the selectivity of the tuned input circuit depends only on the Q of the tank circuit. Thus better selectivity is obtained. When the input signal reduces in amplitude, the decreased grid voltage produces a reduction of plate and cathode current, accordingly. Since cathode resistor R1 is not bypassed for audio frequencies, the instantaneous audio current variations through RI develop an output voltage which varies with a modulation envelope of the received signal. The process is practically identical to that of the diode detector discussed previously in this section of the Handbook, since only the positive portion of the input is effective as shown in the following illustration, (the negative portion is biased off).



**Detection Characteristics** 

With a large input signal the circuit always operates over the straight (linear) portion of the plate current-grid voltage characteristic. Since plate load resistor R2 is bypassed by C3, any instantaneous r-f or audio current variations are bypassed to ground, and the plate voltage remains constant regardless of cathode current fluctuations.

## Failure Analysis.

**No Output. An** *open* or shorted input or output circuit, lack of plate voltage, or a defective tube can create a no-output condition. Check the supply voltage with a high resistance voltmeter to determine that

the fault is not in the power supply, and then check the plate voltage. No plate voltage indicates possibility of R2 being open or C3 being shorted. Check R3 for proper resistance with an ohmmeter, and C3 for a low resistance to ground. Check the cathode bias voltage developed across RI. If no bias exists, either VI is defective, RI is open, or C2 is shorted. Check RI and C2 with an ohmmeter. If normal plate and cathode voltages exist use a VTVM to check the grid input voltage. If no grid signal voltage is found, make certain that Cl is set to, the proper frequency for the desired input signal, and if still no input exists, check T1 for continuity with an ohmmeter. If an input signal exists on the grid of V1, check coupling capacitor C<sub>c</sub> to make certain it is not open (use an in-circuit capacitance checker).

Low Output. A weak input signal can cause a low output. A low emission tube usually causes erratic fading on all signals and a low output. Low plate voltage will also cause a reduced output. Check the plate and cathode bias voltages. If the plate voltage is low with a normal supply voltage, check R2 for an increased resistance value and C3 for a partially shorted or leaky condition. If the cathode bias is low, RI may have changed value, C2 may be leaking and shunting R1 with a low value of resistance, or V1 plate current may be weak because of low emission. Check R1 with an ohmmeter and C2 for leakage. A weak input signal can also be caused by defective r-f transformer, TI, or by a defective or mistuned tank tuning capacitor, Cl. If there is any change in signal as Cl is tuned, the tuning capacitor is probably satisfactory and the primary of TI is probably open. Check T1 for continuity with an ohmmeter. If the transformer continuity is complete and weak signals still occur on a known local signal, there is still the remaining possibility that T1 is shorted.

**Distortion.** Since the infinite impedance detector is noted for its fidelity and lack of distortion, it is evident that noticeable distortion indicates improper performance. Check the bias with a voltmeter. Low bias will place the operating point on the bend of the  $E_g/I_p$  curve, and square law detection with its high distortion products will result instead of linear detection. Distortion accompanied with a low output can also be caused by a defective tube.

#### **REGENERATIVE DETECTOR (ELECTRON TUBE)**

#### Application.

**The** regenerative detector is used in simple one or two tube receivers, particularly in the high frequency regions where normal r-f amplifiers do not provide much gain. It is mostly used for CW and voice reception.

#### Characteristics.

Uses a grid-leak detector with regenerative feedback from plate to grid.

Has better sensitivity than any non-regenerative detector.

Has better selectivity than any non-regenerative detector.

Has poor fidelity with relatively high distortion for music and, therefore, is mostly used for voice and CW (code) reception.

#### Circuit Analysis.

**General.** The regerative detector utilizes the high sensitivity of a grid-leak detector, together with the increased amplification afforded by regenerative feedback to provide a unique detector with extreme sensitivity and high gain. Since grid-leak detection is used, the distortion level is high, and because regeneration increases the selectivity of the tuned input circuit, a narrow band-width is obtained. Thus, the high frequency components of a modulated signal are effectively eliminated by circuit selectivity of the order of a 2-to-3 kHz. Hence, this circuit is restricted in use mainly to communications applications involving only voice and code reception.

There are a number of circuit variations, most of which involve the method of controlling the regenerative feedback. Because feedback varies with the frequency range covered, fixed forms of feedback are suitable only over a very narrow range of operation. With smooth control of feedback, it is possible to increase the regeneration until the feedback reaches the critical point where any further regeneration will cause continuous oscillation of the circuit. Voice reception is amplified the greatest just below this point. For code reception, the amount of regeneration is increased until the circuit just oscillates, and

the desired signal is tuned in by adjusting the tuning capacitor slightly off resonance until an audible note is produced. This type of reception is known as *autodyne* reception, which uses a single tube to perform detection and oscillation simultaneously; as contrasted with *heterodyne* reception, which uses a *separate* oscillator to produce a heterodyne signal.

**Circuit Operation. The** schematic of a typical regenerative detector is shown in the following illustration.



#### **Regenerative Detector Circuit**

The r-f input signal is applied to Ll, the primary winding of the r-f input transformer, of which L2 is the secondary, tuned by capacitor Cl. Feedback winding L3 is inductively coupled to L2, and consists of a few turns wound in the same direction as those of the secondary coil and located at the ground end of the secondary coil (L3 is called the "tickler" coil). Variable capacitor C3 is connected in series between ground and tickler coil winding to control the amount of regenerative feedback. The radio frequency choke, RFC, and capacitor C4, form a lowpass filter which bypasses any r-f component in the plate circuit to ground. Capacitor C2 and resistor RI form a conventional parallel grid-leak arrangement. The audio output is applied to the primary of transformer T1, used to provide a step-up in output voltage between primary and secondary. Although any other method of audio coupling may be used, the transformer is usually used because of the large output it produces in comparison with other types of coupling.

Initially, the circuit rests in its quiescent condition with no signal applied, and draws heavy plate current because only contact bias is supplied by R1 (see the introduction to the Amplifier Section of this Handbook for a complete explanation of contact bias). We shall also assume that feedback capacitor C3 is set to the middle of its range and offers a low capacitive reactance to ground. Tickler coil 1.3 is freed-coupled to L2, and wound so that both grid and plate ends of the winding are of additive polarity.

When an input signal is applied to L1 it is inductively coupled into the resonant tank consisting of L2 and Cl. The low reactance of the grid-leak capacitor, in turn, allows the tank signal to appear at the grid of V1, across R1. On the positive half cycle grid current flow is increased, and capacitor C2 is charged negatively as shown by the polarities and current flow arrow on the schematic. Thus as the signal rises in a positive direction the negative grid bias on V1 increases. This negative grid bias increment decreases plate current flow because of control grid action within the tube. In the quiescent condition, plate current flows through the tickler coil winding in such a direction as to produce a polarity similar to that of L2 across L3. Thus the plate end of the tickler is negative when the grid is positive. Since, in the absence of an input signal there is a steady unchanging flow of plate current, the field built up around L3 remains steady and constant so that no feedback voltage is induced into L2. When the input signal is applied, however, the reduction of plate current with the increase of grid-leak bias produces a change in the lines of magnetic flux cutting the two coils, and a feedback voltage is induced in L2 by the current change in L3. The reduction of plate current causes the field around L3 to collapse and induce a voltage of opposite polarity to that normally produced in the increasing current direction. Hence a positive voltage is fed back to further activate the grid of VI. Since the input signal and the feedback voltage are of the same polarity they add, and produce a still greater negative grid bias. The increased bias, in turn,

causes a further reduction of plate current, and a larger feedback voltage. This cycle of signal build-up by regenerative feedback continues until the input signal amplitude changes. As the amplitude changes, the feedback action follows. That is, as the signal increases the feedback increases, and as the signal decreases the feedback, likewise, decreases. With feedback, the combined signal value is always greater than without feedback. Thus, weak signals are greatly enhanced and the sensitivity of this type of detector is greater than for non-regenerative types.

On the negative half-cycle of input signal, the flow of grid current is reduced, and a small amount of the charge on capacitor C2 leaks off to ground through grid-leak RI. Therefore, the grid bias on V1 is reduced and an increased plate current flows. The increased current flow is in the direction of original (quiescent) current flow and produces a feedback voltage of negative polarity, which adds to the negative signal voltage on the grid. This regenerative build up in the opposite direction during the negative half-cycle of operation is limited to a value less than zero bias, since the tube is operating on the lower bend of the characteristic transfer curve. Hence the positive and negative swings developed across the primary of audio output transformer T1 are unequal and distortion is produced.

The following waveform illustration shows the relationships between the grid and plate voltages and currents. The dotted lines in the waveforms indicate the build up of signal by regenerative action during the positive half-cycle. When the input voltage increases, the secondary voltages increases and is further enhanced by feedback, while the detected signal produces a grid bias which increases and is further enhanced by the feedback. The plate current, in turn, is progressively reduced, while the plate voltage increases. The changes of plate current occurring at audio frequencies in the primary of T1 induces a similar output voltage in the secondary.





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When the capacitance of feedback capacitor C3 is increased, the reactance to ground is reduced and a greater r-f current flows through tickler coil L3, and produces a larger feedback voltage. As long as the feedback is kept below the point of oscillation, maximum amplification is obtained. Once the feedback becomes great enough to drive the grid to cut-off and beyond, the tube conducts only during the peak of the signal and for less than a half cycle (class C operation). During the cutoff period the tank circuit supplies the missing portion of the signal and continuous amplitude sine-wave oscillations occur.

Although the r-f component in the plate circuit is effectively bypassed to ground by regeneration capacitor C3, radio frequency choke RFC, is placed in series with the **plate** lead to offer a high r-f resistance (impedance) and prevent the possibility of r-f feedback through the load consisting of audio output transformer T] and the power supply. To ensure that no RF remains to cause a fringe howl and deteriorate detector performance, capacitor C4 is also used to bypass the primary of T1. Thus, any remaining RF which might exist at the load end of the RFC is bypassed to ground by C4, so that only the slow current variations caused by modulation and occurring at audio frequencies appear in the transformer primary, and induce an output voltage in the secondary.

When voltage is fed back from the plate to the grid circuit, the result is to effectively reduce the losses in the grid circuit. Since the Q of an inductance is the ratio of the reactance to the resistance in the circuit. It is evident that when the r-f resistance in the circuit is decreased and the same reactance exists, a higher Q results. Thus, with a higher Q tank circuit resulting from feedback, a greater selectivity exists. This improved selectivity makes for sharper tuning, and will cut off the higher modulation frequencies in wideband transmission such as is used for music at broadcast frequencies. At high frequencies, however, the side bands are a much smaller percentage of the signal so that not as much sideband clipping occurs and usable voice reception is possible without excessive distortion. Since code transmissions occupy a very narrow frequency spectrum of one thousand cycles or less the increased selectivity of the tuned circuit during feedback is not sufficient to affect code reception. One of the major disadvantages of this circuit for Military use is that, when oscillating it reradiates and produces a low powered CW output; which, besides interfering with nearby receivers tuned to the same frequency, offers a convenient means for the enemy to locate the source with direction finders. This radiation can be eliminated by use of an r-f stage between the detector and antenna, which acts as a buffer stage when properly neutralized.

## Failure Analysis.

No Output. Lack of an input signal, loss of plate voltage, an open or shorted input or output circuit, or a defective tube can result in a loss of output. First measure the supply voltage with a high resistance voltmeter to make certain that the supply or a blown supply fuse is not at fault. Then measure the plate voltage to ground. If the plate voitage is normal, plate circuit components C3, C4, RFC and the primary of T1 are not at fault. If removing and replacing the tube produces a click in the output device it indicates that the secondary of T1 is not open or shorted, and that the trouble is most probably located in the grid circuit. Turn regeneration control C3 past the point where oscillation usually begins and touch the grid of V1 with your finger. A click in the output indicates the circuit is oscillating and that the tube and feedback portion of the circuit are operating. If there still is no output, the input coil is probably open or shorted. Use an ohmmeter to check the input coil for continuity. If the coil is not open, the possibility of a grid to ground short or an open grid capacitor, C2, still exists. Therefore, it is usually easier to connect the antenna or the output of a signal generator direct to the grid of V1. If the input or tuning portion of the circuit is at fault and C2 is not open, a weak signal will usually be heard. Also rotate tuning capacitor Cl, and listen for a noise indicating shorted tuning capacitor plates.

If no plate voltage is obtained, either T1 or the RFC is open, or capacitors C3 or C4 are shorted, or tube VI is defective. An infinite resistance when measuring across T1, RFC, or L3, indicates an open circuit.

**Low Output.** Low plate voltage, a defective tube, or partially shorted or open parts can cause a reduced output. If the plate voltage is low, check T1 primary, the RFC, and coil L3 for high resistance soldered joints and partially open windings, as indicated by a high resistance reading on an ohmmeter. Also check C3 and C4 for leakage to ground with an in-circuit capacitance checker. If the plate voltage is normal but the output is low, check the secondary of T1 for

continuity with an ohmmeter (if sufficient stray capacitance coupling between primary and secondary windings exists weak signals may be heard even though the **secondary** is open). Rotate tuning capacitor Cl to determine if it is tuning. If it tunes the signal, check input coil L1 for high resistance or an open, since a small, stray capacitive coupling from primary L1 to secondary L2 will produce an output signal even if L1 is open, especially at the higher radio frequencies. Where a strong local signal exists, touching the input winding (or VI grid) with the finger will increase the signal if the antenna is defective or too small (this type of indicator may not be too effective below decks or in a well-shielded compartment).

Distorted Output. Since grid-leak detection is used there will normally be noticeable distortion, particularly on strong, heavily modulated signals. A continuous tone beat-note heard with the modulation indicates the detector is oscillating and that a readjustment of the regeneration control is necessary to prevent self-oscillation. A high-pitched audio squeal which occurs when the audio gain is increased is known as fringe howl, and occurs only if the RFC and capacitor C4 are not operating properly to bypass the excess r-f plate component to ground. This could occur if the RFC were shorted or C4 were open. First substitute a good RFC, then if the squeal persists shunt C4 with a capacitor of similar value. If V1 is low in emission, there will usually be distorted signals coupled with continuous fading and a weak output. Should the values of the grid-leak resistor or capacitor change noticeably, both blocking and excessive distortion may occur.

# SUPER-REGENERATIVE DETECTOR (ELECTRON TUBE)

#### Application.

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The super-regenerative detector is used in cheap, one or two tube receivers for the VHF and UHF regions where RF amplification does not provide much gain, and good selectivity is not required. It is particularly popular in portable-mobile transceivers and walkie-talkies, where small size and low power consumption is important.

### Characteristics

May be separately quenched or self-quenched.

Uses a low quenching frequency to obtain high \*in.

Selectivity is much less than for any other form of detector.

Has an inherent noise reducing and limiting action. Responds almost equally as well to strong signals as to weak signals.

Provides high sensitivity and gain in a single tube.

### Circuit Analysis.

General. The super-regenerative detector uses a low frequency (from 15 kHz to 100 kHz) as a quench oscillator, generated either internally or separately, to control the regeneration applied to a grid-leak detector, and thus supply an extremely high gain from a single tube. The use of a quenching frequency effectively broadens the selectivity of the tuned input circuit to the point where it acts almost as if it were not tuned. Hence, a major disadvantage is that any strong signal within a few hundred kilocycles of the desired frequency will override it and blank out the desired signal. It also responds somewhat logarithmically to input signal strength so that an amplitude limiting and AVC action is obtained. Thus, extremely weak signals below the threshold level are not detected, and both weak and strong signals above the threshold appear at the output with nearly the same intensity. In addition, high amplitude noise interference, such as produced by spark ignition systems is minimized without the necessity of adding a limiter stage. Signals with low levels of modulation (less than 50 to 60 percent) produce only a weak or garbled output, whereas signals with high percentages of modulation produce a loud output, accompanied by high distortion. In most instances, the interruptions of the quenching oscillator produce an audio output in the form of a high-pitched hiss caused by noise, which appears between stations, and disappears as the signal is tuned in (on extremely weak signals the hiss will mask out the signal). Since the super-regenerator is oscillating, except during the quench period, it is usually necessary to use an r-f amplifier as a buffer to prevent reradiation and interference with other reception. This is also a major disadvantage when used in

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Military equipment, since interception by enemy direction finders is still possible even with an r-f stage if it is not perfectly neutralized.

**Circuit Operation. The schematic** of a typical super-regenerative detector is shown in the following illustration.



Typical Self-Quenched Supar-Reganerative Detector

Transformer T1 is an r-f input transformer, with primary L1 (antenna winding) untuned, and secondary L2 tuned by Cl. The tuned secondary tank is connected between the grid and plate of triode VI as a conventional ultraudion oscillator. Grid-leak bias and low frequency quenching is provided by RI and C2. The audio output is taken through r-f isolating choke RFC and applied to the primary of audio output transformer T2. The plate voltage is varied to control regeneration by potentiometer R2, and the primary of T2 is bypassed by C3 to prevent r-f feedback.

In the absence of an input signal, the grid-leak produces contact bias, and a steady plate current flows. When an unmodulated carrier signal **1s** applied to the input, the grid is driven positive on the positive peaks, and **grid** current flows from cathode to grid and back to ground via grid-leak R1, charging grid capacitor C2 negatively. This negative grid bias, in turn, causes a slight reduction in plate current, and a consequent rise in plate voltage. When the carrier is modulated by an audio signal, the grid bias varies at

an audio rate in accordance with the modulation. When the grid bias increases, the plate current decreases. So far, this is conventional grid rectification and detection. In the regenerative detector this change of plate current induces a field around tank coil L2 which produces an in-phase voltage in the grid portion of the tank coil. Hence, as the plate current decreases a positive voltage is fed back to the grid, and causes still smaller plate current to flow. In the conventional regenerator, this feedback is limited to an amplitude which is just below the point where continuous oscillations are produced. Consequently, even though this type of regenerative feedback results in a gain, it is not as large a gain as could be obtained if the circuit were prevented from oscillating until a larger feedback amplitude was obtained. Such action is accomplished in the super-regenerator by developing a low frequency oscillation in the grid circuit known as the quench voltage. In the self-quenched circuit described above, the quench voltage is obtained by using a large grid-leak resistance and capacitance to provide a long time-constant. Because of the large time-constant very little voltage can leak off capacitor C2 during the negative portions of each r-f input cycle, so a cumulative build-up in negative bias voltage develops as the input signal is applied, until the bias is sufficiently large to drive the grid to plate current cut off and beyond. When C2 is charged to this cut-off voltage, grid and plate current flow ceases while capacitor C2 discharges through the long time-constant grid-leak. During this discharge period the detector circuit is inoperative.



Thus, the action consists of an ON period followed by an OFF period. During the ON period the audio output is developed, while during the OFF period no output is developed, although this action results in a signal consisting of chopped up pieces of the original modulation, the modulation frequencies are very low

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in comparison to the operating frequencies (cycles compared with megacycles), so that only a small portion of the modulation is lost during any one OFF cycle, as shown in the exaggerated waveform in the preceding illustration. It is evident that the overall waveform shape is retained, but a ripple component at the quench frequency is introduced. This ripple of quench voltage is filtered out by capacitor C3 which bypasses it to ground. Thus, only the audio frequencies pass through the primary of output transformer T2, and induce an output voltage in the secondary. Since the output waveform is chopped up and is not exactly the same as the input waveform, distortion is produced (this is in addition to any normal distortion caused by grid-leak detection). Thus, it is evident that the output of the superregenerator must always contain more distortion than in the ordinary regenerative detector. However, this inherent distortion is somewhat nullified by the large gain possible through super-regeneration. The gain is of the order of one hundred times or more than that of the ordinary regenerative detector.

When a separate quench oscillator is used, it is connected in series with either the grid or plate circuit, and the grid-leak values are changed to provide additional gain, since the tube does not have to develop its own quench voltage. However, for the sake of economy and simplicity the single tube selfquenching circuit is usually used. Since the superregenerator is unique in its action, operating at very high frequencies, at low frequencies and at audio frequencies practically simultaneously, it is necessary to examine the operating sequence more closely to completely understand operation. First consider the quench voltage, regardless of whether or not it is externally supplied, or is generated internally, it primarily serves to gate the grid circuit. During the positive half cycle it permits operation, and during the negative half cycle it reduces operation to almost zero. At the same time, this quench voltage control permits the circuit to oscillate at a very high frequency (the tuned tank frequency) during the conducting half cycles and prevents these oscillations during the non-conduction half-cycle. In the selfquencher, the off period allows time for the grid-leak network to discharge, so that a' train of r-f pulses may be generated during each on-period. Grid-leak bias is developed by rectifying the positive half cycles of this train of r-f pulses each time they cause a flow of grid current. Thus, the grid-capacitor is charged negatively

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at an r-f rate, and since the discharge time constant is longer than the charge time constant (the conduction of grid current presents a low resistance charge path), the charge cannot leak off the grid between r-f pukes and, therefore, builds up and eventually reaches cutoff bias. This **cut-off** bias point in the self-quencher determines the start of the off-period, and the tube is held inoperative during this period until grid capacitor C2 discharges through the large grid-leak resistance.

It is important to note that during the on-period r-f oscillations occur at the tank frequency, regardless of whether or not an input signal is applied. This action occurs because of the large feedback from plate to grid. Thus, in the absence of an input signal, the tank circuit is started oscillating by random current flow in the tube due to noise, which through feedback quickly builds up to a high amplitude and develops a dc bias across the grid-leak. This grid bias, in turn, reduces the amplitude of the r-f oscillation slightly and maintains it at this value for the remainder of the on-period. When an input signal is applied, the amplitude of the r-f oscillation does not change, but instead, the oscillation starts sooner (it has the signal to help it), and the duration of oscillation for the on-period lasts for a slightly longer time than without an input signal, as shown in the following illustration.



**Typical Grid Waveforms** 

Since a negative grid bias is produced by the rectification of this r-f oscillation, the plate current is decreased slightly when a signal appears. Because the high-frequency oscillations exist even when no input signal is applied, the output response is limited to the average change of plate current which can occur from the start of the on-period to the beginning of

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quiescent oscillation. The result is that if the incoming signal is strong enough to mask out the hiss noise, there is little difference between weak and strong signals, since the detector output current varies logarithmically as shown in the following graph. As a result, large amplitude noise variations caused by ignition interference, static, and similar impulse sources are also reduced in intensity. What would be a loud crash in the conventional detector appears as a rather small noise in the super-regenerator, and can be more easily tolerated without distraction from the desired signals. In a similar manner, small variations in amplitude caused by low percentages of modulation produce weak and unreadable signals, while the large variations in 100 percent modulated signals are sufficient to produce an appreciable output.



**Detector Response Characteristics** 

The amount of feedback and plate voltage is controlled by potentiometer R2. For larger feedback and greater amplification the plate voltage is increased, while for less amplification and feedback it is reduced. For each setting of the control the r-f oscillations will reach a maximum value **limited** by the saturation voltage for this operating condition, and fixed by the developed grid-leak bias.

# Failure Analysis.

**No Output. A** defective tube, loss of plate voltage, or open or shorted input or output circuits will cause a loss of output. Use a high resistance voltmeter to measure the supply and plate voltages and eliminate

the possibility of an inoperative power supply or blown fuse. Since the plate voltage will depend on the position of plate potentiometer R2, it is good practice to vary R2 over its range to determine whether or not an output can be obtained. If R2 is open at some point between the slider and ground, the plate voltage wiJI be higher than normrd, if open on the slider side there will be no voltage (provided T2 primary and the RFC and upper half of coil L2 have continuity). No voltage for any setting of R2 indicates that T2 primary, the RFC, or coil L2 is open. Check for continuity with an ohmmeter or measure voltage to ground. If there appears to be sufficient plate voltage present, check the values of the grid-leak resistor and capacitor using a voltohmmeter and an in-circuit capacitance checker. Check L2 for possibility of a defective tuning condenser Cl which will usually create a noise when rotated, if shorted. If still no output exists it is possible that T2 secondary is open or shorted. Place a pair of headphones across the primary winding or couple a speaker to the primary by a coupling capacitor. Any output indicates the secondary of T2 is at fault. Note also, that if C3 is shorted, plate voltage will appear about normal but no output 'will occur because of the shorted load winding. However, this condition usually is determined at the time that continuity checks are made of L2, T2, and R2. It is important to note that lack of an input signal will not result in a no-output condition, since the circuit will still operate, and produce a hiss.

Low Output. A low or reduced output can be caused by a weak input signal, a partially shorted input circuit, an improperly modulated signal, a defective tube, low plate voltage or a defective output transformer, T2. Signals below the threshold level for detection and those signals with low percentages of modulation (say 50% or less) will not be detected, this is normal operation. If, however, the signal is weak because of an open or a partially shorted input transformer, it can be found by checking the coils with an ohmmeter. Likewise, with a low plate voltage indicated on the voltmeter, both feedback and output will be low. If the trouble is not in the plate supply, most likely bypass capacitor C3 is at fault and leaky, check it with an in-circuit capacitance checker. Check the values of the grid-leak and grid capacitor, using an ohmmeter and capacitance checker. Continued Iow output indicates L1 is either open or partially shorted,

## **ELECTRONIC CI RCUITS**

**Distorted Output, The output** will normally be somewhat distorted, particularly on voice peaks, however, the signal should be intelligible. If distortion is such that the voice is badly garbled, improper biasing is usually the cause. Check the grid-leak resistor with an ohmmeter and the grid capacitance with an incircuit capacitance checker. To eliminate the following audio stages from suspicion, place a pair of headphones across the primary of T1. If the distortion disappears, the distortion is caused by the audio amplifier stages after the detector.

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## PRODUCT DETECTOR (ELECTRON TUBE)

#### Application.

**The** product detector is universally used as a detector for heterodyning and demodulating single-sideband transmissions in modern communications type receivers.

### Characteristics.

**Is** usually self-biased.

Operates as a combined heterodyne mixer and detector.

Has excellent selectivity.

Offers a slight improvement in gain.

Is more linear than the diode detector.

### Circuit Analysis.

General. The product detector can be considered a form of heterodyne mixer with an audio output instead of the usual r-f output. The purpose of this detector is to mix locally generated low frequency carrier oscillations with the incoming r-f sideband signals to generate beat notes in the audio frequency range. For single-sideband the beat varies in both pitch and amplitude, producing the detected audio. The product detector may also be used for code reception using the beat frequency oscillator (BFO) to produce a single-tone audio beat. The use of mixing to develop the beat signal reduces the tendency to grid-block, when strong signals from a local oscillator are applied to the grid simultaneously with a weak input signal. Ordinary double-sideband AM signals can also be detected with the product detector, provided the BFO is tuned to zero-beat. When used with a strong BFO input and a weak signal input exulted carrier reception is simulated. With a strong (exalted) local carrier inserted, phase cancellation of the sideband frequencies during fading is minimized, as the local BFO substitutes for and fills in the carrier. Although during extreme fading this represents an improvement in ordinary AM reception it has the disadvantage that it is usually necessary to continually adjust the local BFO find tuning control to keep the local oscillator at zero beat. Otherwise, the steady CW beat note produced by the two carriers (input signal and BFO) beating together garbles the signal.

**Circuit Operation.** While there are a number of product detector circuits, one of the most prevalent in use is the typical pentagrid converter illustrated in the following schematic.



**Pantagrid Product Detector** 

A single pentagrid tube is connected as a heterodyne converter, with the triode portion connected as a simple series-fed Hartley oscillator and operating as the beat frequency oscillator (BFO) to supply a carrier signal. The r-f input with its carrier missing is

injected in mixer grid no. 2, which is shielded by the screen construction around it, and the audio output is taken from the plate of the pentode section. Tuned tank L and C is connected in a Hartley circuit with VI, and the lower end of the tank is bypassed to ground by C4, while C2 is the grid capacitor with R2 acting as a shunt grid-leak to supply the bias for the oscillator. The screen receives its supply voltage from dropping resistor R3 from the plate supply. Capacitor C5 bypasses the screen to ground and effectively connects it to the lower end of the tank thereby forming the triode oscillator portion of the circuit. The BFO signal is electron-coupled to the pentode section by electron flow from cathode to screen and plate. The input signal is capacitively coupled through Cl to the mixer grid, and RI is the dc return resistor supplying grid bias for the mixer grid. This resistor is made adjustable to set operation at the proper point for complete mixing and reduction of intermodulation distortion from input signals. The BFO signal is thus mixed with the r-f input signal and is heterodyned to produce audio beat signals, which vary in accordance with the modulation of the r-f input signal. Since the plate of V1 is bypassed to ground for rf by C3, only the audio frequency current variations appear in the plate circuit. These audio current variations develop an output voltage in passing through load resistor R4, and thus develop the audio output which is coupled through C<sub>s</sub> to the following audio amplifier stage.

With no signal applied, V1 rests in its quiescent state with the triode section oscillating at the i-f (carrier) frequency, and with no input signal there is no output developed. Operation of the BFO is by feedback through tank coil L between the grid and screen @ate) to supply a continuous feedback from screen to grid and produce continuous oscillations at the frequency determined by the tuning of tank capacitor, C. Since C4 has a low r-f reactance to ground, and C5 which grounds the screen also has a low reactance to r-f, the screen is effectively connected to the lower end of the tank. During the oscillation period, grid-leak network C2 and R2 alternately charge and discharge. During the conduction period on positive half-cycles the grid capacitor is negatively charged, and develops a Class C bias on the grid of V1 through grid current flow from the cathode through R2 to ground. On the negative half of the oscillation, grid capacitor C2 discharges to ground through grid-leak R2, so that the bias is reduced to a value which will permit conduction on the next positive r-f excursion.

Meanwhile r-f is supplied to the circuit by the tank during the non-conducting period thus producing continuous oscillation at the tank frequency. (See the Oscillator Section of this Handbook for a complete discussion of Hartley oscillator operation.)

When an input signal is applied to the mixer grid of V1 through coupling capacitor Cl the input signal appears on the mixer grid. During the positive halfcycle of the input signal plate current flow is increased, and during the negative half-cycle it is decreased. As the electron flow from cathode to plate occurs, the electrons pass through the screen, and the BFO oscillations are heterodyned with the input signal to produce an audio beat note in the plate circuit. A portion of these electrons also flows through the mixer grid and return resistor R1 to provide bias for the mixer grid. Since the pentode section of V1 is connected as an amplifier, this bias fixes the operating point of the number 2 (mixer) grid at the position for maximum undistorted operation (usually in the Class A region). However, when undesired signals close to the tank frequency are strong, the strong signals tend to over-ride the weaker signal and cause response to both signals regardless of the tuning of tank capacitor C. Therefore, if RI is adjusted to produce clear undistorted reception on the strongest signal, weak signrds will not be pulled in frequency and the strong signal will not cause saturation and produce intermodulation distortion. The change in plate current caused by the input signal alternately increasing and decreasing plate current flow through load resistor R4 develops an output voltage across R4. Since C3 bypasses any r-f signal component and any BFO signal component to ground, only the audio beat note will be effective in producing output voltage across the load. Thus, the modulation amplitude variations of the r-f sideband signal, in effect, modulate the oscillating electron stream and produce the output. If the BFO stopped oscillating there would be no output, since there would be no beat note developed between the low frequency i-f signal and the high frequency r-f signal to produce audio variations in the electron stream between cathode and plate.

Although R1 is shown as variable in the schematic, some circuits use a freed value of resistance which, together with screen resistor R3, is selected to provide optimum operation. In other circuit variations a separate BFO is employed and pentagrid tube VI is connected as a simple mixer with both control grids biased to operate as amplifiers, so that only a simple mixing function is accomplished. The combined circuit discussed above represents a saving in tubes and economy of circuit components, hence its more prevalent use. Regardless of circuitry, the two signals are always heterodyned to produce a beat output which is in the audio range and thereby demodulates the sideband signal.

### Failure Analysis,

No Output. Loss of plate or screen voltage, lack of oscillation in the triode section of V1, an open or shorted input or output circuit, as well as a defective tube can produce a loss of output. Check the plate and screen voltages with a high resistance voltmeter, to make certain that a faulty supply or blown fuse is not at fault. If plate voltage is lacking, either R4 is open or C3 is shorted. Likewise, if no screen voltage is present, either R3 is open or C5 is shorted. Measure the resistors with an ohmmeter and check the resistance to ground across the capacitors, or use an incircuit capacitance checker to check for shorts, leakage, and proper value. Determine if' the BFO is oscillating, and if there is an input signal. Use an oscilloscope and r-f probe connected between the no. 1 grid and ground to check that oscillation occurs. An alternative procedure is to use a high-resistance voltmeter, and place a 1-rnegolun resistor in series with the probe, and measure the voltage across grid-leak R2. If oscillating, usually a 10-volt or better indication is obtained and, in addition, when grid-leak is shorted with your fingers the oscillation will cease as indicated by a drop in voltage to about 1 volt or less. If oscillations do not occur check coil L for continuity, and tuning capacitor C for a short or leakage (use an in circuit capacitance checker). Check grid-leak R2 for proper resistance value and C2 for leakage and proper value. If still no oscillation, check C4 for an open circuit (if shorted it would still oscillate). With the BFO operating it is still possible that RI is shorted and is bypassing the input to ground through C4, or for Cl or C to be open, check each capacitor with a capacity meter. Usually it is only when the BFO is not oscillating that a true no-output condition occurs, and the set sounds dead. There will probably be some hum or occasional noise noticed, except of course if output coupling capacitor C<sub>c</sub> is open.

Low Output. Low plate or screen voltage, a defective tube or a change in some parts values can pro-

duce a weak output. Measure the plate, screen, and supply voltages with a high resistance voltmeter. Low voltage indicates that C5 or C3 is leaky or that VI is shorted and drawing larger than normal current. Check the capacitors with a capacity checker. With normal plate and screen voltages check the voltages on both grids with an oscilloscope and r-f probe. On some detectors it is still possible to get a weak output even though the **BFO** is not operating. Also check the adjustment of RI since the signal may be biased off too far and provide a weak output. Normally both the oscillator and incoming signal should be about the same level, but in no case should the BFO voltage be greater than the r-f sideband voltage. Check also the setting of the receiver RF GAIN control since it may be set too low.

Distorted Output. If the input signal is too strong, the detector can be overloaded and cause distortion, make certain the receiver R-F GAIN or AVC system is holding the input signal to the proper level. ALSO check the adjustment of RI, since if it is set up for weak signal reception the detector wilf overload and distort on strong signals. When it is adjusted so that the strongest signal is clear, the weaker signals will still be readable. It is also necessary that the receiver be tuned to the proper sideband in single-sideband reception otherwise, the modulation may be present but inverted and be garbled and unintelligible. In this case on a receiver equipped with upper and lower sideband switching, placing the switch to the opposite sideband position will eliminate the distortion. Since it is necessary to keep the inserted carrier within 10 to 12 cycles of the proper frequency, slight frequency instability in the receiver local oscillator may constantly keep the station frequency drifting. This will show up as distortion which disappears as the BFO tuning is slightly , readjusted. In the last case the trouble exists in previous receiver stages, not the detector. It is, however, advisable to check the BFO for drift first using a stable primary standard, if available.

# COHERENT (SYNCHRONOUS) DETECTOR (ELECTRON TUBE)

#### Application.

The coherent (synchronous) detector is used in electronic equipments where a phase change between

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two frequencies is used to provide an output signal. It is extensively used in color television and for other special applications.

#### Characteristics

May use diodes, triode, or pentode tubes. May use balanced or unbalanced arrangements. Requires a reference oscillator signal.

## **Circuit Anelysis.**

General. The synchronous detector is phasesensitive with respect to a reference oscillator signal which is applied simultaneously with the desired modulated signal. When both signals are in-phase, a negative output is obtained, when the signals are outof-phase, a positive output is produced. In a TV color receiver the I and Q components of the chrominance signal are always in quadrature (90 degrees out-ofphase), therefore, a synchronous detector may be used to separate the color components, since at a phase difference of 90 degrees the output is always zero, as shown in the following illustration. As can be seen from the illustration, the maximum output occurs at zero, 180, and 360 degrees phase difference between the input signal and the reference signal, while no out-put is obtained at 90 or 270 degrees. Since a reference signal is always necessary to produce an output, the synchronous detector can also be considered as a special form of product detector.



Synchronous Detector Response Curve

**Circuit Operation.** A typical pentode demodulator is shown in the following illustration and is one form of coherent (synchronous) detector commonly used in color TV receivers.



Synchronous Detector

Potentiometer R1 is the input control and R2 is a grid current limiting resistor. Cathode bias is supplied by resistors R3 and R7, with R7 adjustable and bypassed by capacitor C2. Fixed cathode resistor R3 is unbypassed to provide a slight amount of degeneration and improve linearity. (See paragraph 2.2.1 in Section 2 of this Handbook for a complete discussion of cathode bias.) Screen voltage for VI is supplied by R8, which drops the supply voltage to the proper value. Capacitor C3 is the screen bypass capacitor which places the screen at ground potential as far as any signal voltages are concerned. Resistors R4, R5 and R9 are the plate load resistance, with capacitor C4 serving as the ground bypass for resistor R9. In addition, resistors R4 and R5 act as terminating resistors for the lowpass filler network (CIA, CIB and Ll). Series resistance R6 and inductance L2 provide, in effect, a high impedance output, which is capacitively coupled to the next stage by capacitor C5. Both the low pass plate filter and the series reactance in the output are used to ensure that a minimum harmonic output of the reference oscillator is obtained. Normally, with ordinary RC coupling, a strong second harmonic output of the reference oscillator would be produced in the output.

The chrominance subcarrier input signal is normally applied to grid one of pentode tube V1; the reference oscillator signal, which is a CW sine wave of

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the same frequency as the chrominance subcarrier, is applied to the suppressor grid (grid three). Since the suppressor grid is located between the plate and screen grid, it acts as a gate. During the half cycle that the reference signal is positive, and increased flow of electrons is attracted to the plate; during the negative half cycle, plate current flow is effectively cut off. With no input signal applied to grid one and the reference signal to grid three, the positive and negative plate voltage excursions are equal and average out to zero, so there is no plate output and the coupling capacitor charges to the average plate voltage value, establishing the zero axis.

When an in-phase signal is simultaneously applied to grid one, while the reference signal is applied to grid three, both voltages add and produce a larger plate current flow. Thus, a higher plate voltage drop occurs in the plate load and a negative output voltage is developed. When the input signal is out-of-phase with the reference signal a lower than normal plate current is produced. With a lower than normal plate current, the average plate voltage increases and effectively produces a positive output.

When the input signal is either 90 or 270 degrees out-of-phase with the reference signal their voltage maximums occur at opposite times. Hence, when one signal is at a maximum, the other is at a minimum or zero. Thus, the effect is as if only one signal were applied (the reference voltage with no input signal), and the average output is zero. Between the angles of zero degrees and 90 degrees, and between 90 degrees 180 degrees the output varies in accordance with the cosine of the phase angle difference. A similar situation exists between 180 and 270 degrees, and 270 and 360 degrees, except that the output polarity is reversed. A typical series of waveforms showing the conditions explained above is shown in the following illustration. For ease of illustration each of the basic waveforms is considered to be of the same amplitude though in practive they may vary from cycle to cycle. The first part of the waveform shows the reference voltage alone applied to grid three with no input to grid one, producing zero output. The second part shows the addition of grid one and grid three waveforms when inphase, producing a negative output. The third part shows the subtraction of the grid one signal from the grid three signal during outof-phase conditions, with a consequent positive

output voltage. In part four both waveforms are 90 degrees out-of-phase and zero output is obtained.



**Operating Waveforms** 

When used for I and Q signal demodulation separate synchronous detectors are required for each signal component; by inserting the proper phase delay in the reference oscillator for one of the components, both signals may be obtained with similar coherent detector circuits. In the discussion of operation, constant amplitude signals were assumed for ease of discussion; in normal operation, the output is also dependent to a slight extent on the amplitudes of the reference and chrominance signals. Usually the reference signal amplitude remains relatively constant, while that of the chroma signal will vary with brightness and hue, and the output will vary accordingly.

#### Failure Analysis.

**No Output.** Loss of line or supply voltage, a defective tube, a constant 90 degree phase shift, or no input signal can produce a **no-output** condition. Measure the line and supply voltage to make certain that a blown fuse or defective power supply is not at fault. Check the phase of the input signal **against** that of the reference oscillator. If a constant 90 degree phase difference exists either the imput signals are at fault or the reference oscillator is incorrectly tuned. If no chrominance signal is visible on the grid of V1, either RI or R2 may be open, or the grid may be shorted to ground. check the resistance of RI and R2, and between grid and ground.

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Measure the cathode bias, screen, and plate voltage of VI. If the bias is almost at cut off, the output will be so low as to be practically no output at all. Check the plate and screen circuits for a short to ground, particularly capacitors C3 and C4. If the capacitors are not shorted, V1 may be defective. If no screen voltage appears on grid two, either R8 is open or C3 is shorted. Check the values of R8 and C3. If no plate voltage appears at the plate there will be no output and the screen of VI will glow red. Check R4, R5, and R9 for proper value or an open circuit, and C4 for a short. If there is no bias voltage present, but both screen and plate voltage exist check R3, and R7 for an open. If the input, bias, and plate circuits are satisfactory, it is still possible for R6 or L2 to be open since they are in series with the output.

If no reference signal is present either no output will be present, or it will be the same as the imput signal and very weak. No voltage indicates that no reference signal is present. If an oscilloscope is used, it should show on RF pattern if the reference signal is present. Do not neglect the possibility that output coupling capacitor C5 may be open.

Low Output. Low plate or screen voltage, high bias, or a defective tube can cause a low output. If the supply voltage is low the trouble is in the power supply or line. Low screen voltage can be caused by an increase in the value of R8, a leaky capacitor, C3, or a defective tube. If the plate voltage is low check the resistance of R9 and capacitor C4 for leakage, and check the resistance of R4 and R5, and L1. Also check R6 and L2 for the proper resistance, since they are in series with the output signal. A change in value of coupling capacitor C5 may also reduce the output. If all voltages and parts check out normal and the output is low there is still a possibility that R1 is set for too low an imput. Potentiometer RI should be adjusted for sufficient drive to produce normal output without distortion. It is also possible that R7 can be set for insufficient bypassing by C2, and excessive cathode degeneration may be causing the reduction of output. If an adjustment of R1 or R7, or both, will return the output to normal the circuit most likely is in normal operating condition.

**High Output.** An abnormally high supply, plate, or screen voltage, or misadjustment of input control R1 can produce a larger than normal output. First, check the adjustment of R1 to determine whether or not the output may be restored to normal by a simple readjustment of the control. Then measure the supply

voltage to determine that the input voltage is not excessive. If the supply voltage is normal, but either the plate or screen voltage is higher than normal, either resistors R8 or R9 have changed value or the through these resistors is less than normal. If these resistors are normal, either low tube emission or a change in value of bias resistors R3 or R7 can be causing the low current.

#### PART 10-2. FM

#### FM (OR PM) DETECTORS

#### General.

The process of detection (demodulation) removes the modulation (transmitted intelligence) from a received r-f signal and transforms it back to its original form so that it may be used for communications or other purposes. While the Am detectors explained previously in this section 'of the Handbook are used to demodulate an amplitude-modulated (AM) r-f signal, the FM detectors explained in the following paragraphs are used to demodulate a frequency-modulated (FM) r-f signal. Because of the similarity between a frequency-modulated (FM) signal and a phase-modulated (PM) signal, FM detectors may also be used (with minor circuit changes or adjustments) to demodulate a phasemodulated signal.

Although the circuits used in FM transmission and reception are more complex than those used in AM, FM has a number of advantages which far outweigh this disadvantage. An important advantage of FM over AM is the reduction of distortion due to natural and man-made noise. Most noise occurs in the form of amplitude variations in the r-f signal, and in AM. the intelligence is also carried by the amplitude variations. The AM receiver can not distinguish between the amplitude variations caused by the intelligence and those caused by noise, and consequently reproduces both the noise and the intelligence. In FM however, the intelligence is carried by frequency variations in the r-f signal and the FM receiver is designed so that it does not respond to amplitude variations. Consequently, the noise is not reproduced in the FM receiver output. Another important advantage of FM over AM is the possibility of wide-band transmission. Because of the higher carrier frequencies normally used in frequency

modulation, it is possible to use a much wider band of modulating frequencies. This allows FM to be used for such applications as high fidelity transmission (such as in the FM broadcast band) and for multichannel communications (such as in commercial communications). Moreover, FM transmitters can also be designed to produce a narrow-band output signal (comparable to AM band-width) when it is desired to operate many FM transmitters within a small portion of the frequency spectrum.

The FM signal contains the transmitted intelligence in the form of instantaneous frequency variations to a constant amplitude r-f signal. Therefore, to demodulate the received FM signal without distortion, the FM detector must convert these frequency variations into voltage variations which are identical to the variations in the original modulating voltage. Any variations in the amplitude of the received FM signal are the result of unwanted noise or fading, and will result in distortion of the output signal if passed through the FM detector. Therefore, the FM detector must respond to input frequency variations, but not to input amplitude variations.

Three types of Electron Tube FM detectors are presently in common use: discriminators, ratio detectors, and gated-beam detectors. Discriminator circuits exhibit excellent response to frequency variations, but also respond to amplitude variations, and therefore, must be preceded by limiters to ensure that the discriminator input is of constant amplitude. Ratio and gated-beam detector circuits exhibit slightly poorer response to frequency variations than discriminator circuits, but when properly adjusted, do not respond to amplitude variations. Therefore, ratio or gated-beam detectors are used when economy and simplicity are desired, or precise control of frequency (AFC) is needed.

Semiconductor FM detectors also can be divided into roughly three groups of circuits, namely, discriminators, ratio detectors, or slope detectors. These detectors are very similar in circuitry to that of their electron tube counterparts in that crystal diodes are merely substituted for the vacum-tube diodes. Although these diodes do not have the practically infinite back resistance of the electron tube, otherwise, their performance is similar. And, they do have the advantage of not requiring filament power. For precise frequency response or frequency control discriminator circuits are usually employed. Whereas, the reduced response of the ratio detector is reserved for receivers where economy and simplicity are desired.

# FOSTER-SEELEY DISCRIMINATOR (ELECTRON TUBE)

# Application.

The Foster-Seeley discriminator is used as the detector in high quality FM receivers to demodulate the received r-f signal, and in automatic frequency con t rol (AFC) circuits to transform frequency changes into d-c control voltage changes.

#### Characteristics.

Converts instantaneous frequency variations into instantaneous dc voltage variations.

Employs a double-tuned transformer and two diodes.

Has very low inherent distortion.

Must be preceded by a limiter since the output is affected by input amplitude variations.

## Circuit Analysis.

General. The Foster-Seeley discriminator (also known as the phase-shift discriminator) uses a double-tuned transformer connected in such a way that the instantaneous frequency variations of the input FM signal are converted into instantaneous amplitude variations. The amplitude variations are then rectified and filtered in a manner similar to that employed in AM detectors to provide a dc output voltage which varies in amplitude and polarity as the input signal varies in frequency. The output voltage is zero when the input frequency is equal to the *center* frequency (unmodulated carrier frequency). When the input frequency- rises above the center frequency, the output voltage increases in one direction (for example, become more positive), and when the input frequency drops below the center frequency, the output voltage increases in the other direction (for example, becomes more negative). The specific polarity of output voltage obtained for an increase or a decrease in input frequency is determined by the design of the circuit and may vary in different circuits.

The output of the Foster-Seeley discriminator is dependent not only on the input frequency but also, to a certain extent, on the input amplitude. Since variations in the amplitude of the FM signal are due

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to unwanted noise or fading, they must be prevented from reaching the discriminator. Therefore, the discriminator is normally preceded by a limiter stage. The limiter produces an output of constant amplitude regardless of variations in the input amplitude, and thus, effectively removes the noise from the received FM signal. (Refer to the Special Circuits Section of this Handbook for a complete explanation of limiter circuits).

**Circuit Operation. The** accompanying circuit schematic illustrates a typical Foster-Seeley discriminator.



Foster-Seeley Discriminator

The input tank circuit, made up of capacitor Cl and the primary winding of transformer T1, is tuned to the center frequency  $(f_R)$  of the received r-f signal. Capacitor C3 and the secondary winding of transformer T1 also form a tank circuit tuned to the center frequency. Capacitor C2 couples the input signal to the center tap on the balanced secondary winding of transformer T1, which is returned to ground through radio-frequency choke RFC to form a dc return path for the diodes. Diodes V1 and V2 rectify the signal from the secondary tank circiut and develop opposing voltage drops across load resistors R1 and R2, respectively to the applied input frequency. The secondary of  ${\rm T}_{\mbox{\scriptsize l}}$  is a Capacitors c4 and series tuned c ircu it. C5 are r-f filter capacitors which remove any remaining r-f signal from the output . The output is taken from across the series combinat ion of the two load resistors ( from the cathode of V1 to the cathode of V2)

The operation of the Foster-Seeley discriminator

can be best explained with vector diagrams whic' show the various phase relationships between the voltages and currents in the circuit. The accompanying vector diagram illustrates the circuit phase relationships when the input frequency (f) is equal to the center frequency.



Vector Diagram at Resonance

The input voltage applied to the primary tank circuit i<sub>5</sub> shown as vector e<sub>p</sub> on the diagram. Since coupling capacitor C2 has negligible reactance at the input frequency, and r-f choke RFC is effectively connected in parallel with the primary tank circuit, voltage e, also appears across the choke. When voltage e, is applied to the primary winding of transformer T1, a voltage is induced into the secondar winding which causes current to flow around the secondary tank circuit. When the input frequency is equal to the center frequency, the tank is at resonance and acts resistive. Therefore, tank current is in phase with primary voltage e, as shown in the vector diagram. The current flowing in the tank causes voltage drops to be produced across each half of the balanced secondary winding of transformer T1, which are of equal magnitude and opposite polarity with respect to the center tap of the winding. Since the winding is predominately inductive, the voltage drop across it is 90° out of phase with the current through it. Because of the grounded center top arrangement the voltages to ground at each end of the secondary vindingare180° out of phase, and are shown as  $e_1$  'and  $e_2$  on the vector diagram.

The voltage appfied to the plate of V1 consists of the vector sum of voltages  $e_p$  and e, shown as  $e_3$  on the diagram. Likewise, the voltage applied to the plate of V2 consists of the vector sum of voltages  $e_p$ and  $e_2$ , shown as  $e_4$  on the diagram. Since at resonance there is no phase shift, voltages  $e_3$  and  $e_4$ are equal as shown by the same length vectors. Equal plate voltages on diodes VI and V2 produce equal plate currents, and with identical load resistors produce equal and opposite voltages ( $\epsilon_3$  and  $\epsilon_4$ ) rcross R1 and R2, respectively. Thus capacitors C4

and c5 are charged to equal voltages, and, since these voltages are of opposite polarity, the output voltage at resomnce is zero. Since the opposite ends of the secondary winding are out of phase, only one diode conducts at a time, and conduction occurs as a series of dc pulses occuring at the center radio frequency. Although the output of the diode is a direct current it contains a ripple component at the center frequency. This r-f component is filtered out by capacitors C4 and C5 since they offer a low reactance path to ground (action is similar to a power supply filter capacitor except for the frequency).

When an input frequency higher than the center frequency is applied to the discriminator circuit a phase shift occurs, and the current and voltage phase relationships change as shown in the following vector diagram.



Vector Diagram For Higher Input Frequency

When a series tuned circuit operates at a higher frequency than resonance, the inductive reactance of the coil increases, while the capacitive reactance of the tuning capacitor decreases. Therefore, above resonance the tank is predominately inductive and acts like an inductor. Hence, secondary current lags the primary tank voltage e. Although secondary voltages e<sub>1</sub> and e<sub>2</sub> are still 180 degrees out of phase, they are also 90 degrees out of phase with the current which produces them (is). Thus the change to a lagging secondary current rotates the vector in a clockwise direction. Referring to the vector diagram it is seen that  $e_1$  is brought nearer in phase with  $e_p$ , while  $e_2$ is shifted further out of phase with e<sub>p</sub>. Thus the vector sum of  $e_p$  and  $e_1$  is larger than that of  $e_p$  and e<sub>2</sub>. Therefore, above the center frequency, diode V1 conducts heavier than diode V2. Consequently, voltage  $e_3$  developed across RI is greater than  $e_4$ developed across R2, and the voltage on capacitor C4 is likewise greater than on C5. The combined output voltage is therefore, a positive voltage.

When an input frequency lower than the center frequency is applied to the discriminator circuit a phase shift also occurs, and the current and voltage phase relationships change as shown in the following vector diagram.



Vector Diagram for Lower Input Frequency

When a tuned circuit operates at a lower frequency than resonance, the capacitive reactance of the tuning capacitor increases, while the inductive reactance of the coil decreases. Therefore, below resonance the tank is predominately capacitive and acts like a

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capacitor, Hence, secondary current is *leads* the primary tank voltage e<sub>n</sub>. Although secondary voltages e<sub>1</sub> and e<sub>2</sub> are still 180 degrees out of phase, they are also 90 degrees out of phase with the current which produces them. Thus the change to a leading secondary current rotates the vector in a counterclockwise direction. From the vector diagram it is seen that e, is now brought nearer in phase with  $e_p$ , while  $e_1$  is shifted further out of phase with e<sub>p</sub>. Thus the vector sum of  $e_p$  and  $e_2$  is larger than that of  $e_p$  and  $e_1$ . Therefore, below the center frequency, diode V2 conducts heavier than diode V1. Consequently, voltage drop  $e_4$  across R2 is greater than  $e_3$  across RI, and the voltage on capacitor C5 is, likewise, greater than on C4; thus the combined output voltage is a negative voltage.

When the input voltage is varied from a lower frequency through the resonance point of the discriminator and is then raised higher in frequency, the typical discriminator response curve shown in the following illustration is obtained. The usable portion of the typical "S" shaped response curve is from point A to point B in the illustration. Between these points, the curve is linear and the instantaneous output voltage is directly proportional to the instantaneous frequency deviation.



### **Discriminator Response Curve**

When weak A-M signals which are too small in amplitude to reach the limiting level pass through the limiter stage, the amplitude variations cause primary voltage  $e_p$  to fluctuate with the modulation and induce a similar secondary voltage in T1. Since the diodes are connected as half-wave retifiers, these small A-M signals are detected as in a diode and appear in the output. This unwanted AM interference

is cancelled out in the ratio detector (to be discussed later in this section of the Handbook) and is the main disadvantage of the Foster-Seeley circuit in comparison with other FM detectors.

## Failure Analysis.

**No Output.** A defect in the primary winding of . transformer T1, in the RFC, or in capacitors C 1, C2 or C3 may cause a no-output condition. Use an ohmmeter to check the primary winding of trans-former T1 and the RFC for continuity; also check both for leakage or shorts to ground. If these checks fail to locate the trouble, use an in-circuit capacitance checker to check capacitors C 1, C2 and C3. Note that  $\checkmark$  the failure of either diode will cause distortion rather than a no-output condition; if both diodes fail, however, there will be no output.

Low or Distorted Output. A defect in nearly any component in the discriminator circuit may cause the output to be either low to distorted. Therefore, it is good practice to use an r-f sweep generator and an oscilloscope to isolate the trouble. First, use the oscilloscope to observe the input to the discriminator to be certain that the preceding (limiter) stage is not at fault. If the input signal does not change in amplitude as the input frequency varies, the trouble is most likely in the discriminator circuit. To determine if the discriminator is at fault, ground the grid of the preceding limiter stage, connect the r-f sweep generator to the discriminator input, and connect the oscilloscope to the discriminator output. With the sweep generator set to produce an output which varies above and below the center frequency, the pattern observed on the oscilloscope should be similar to the discriminator response curve illustrated previously. Defects in the circuit will cause either the entire curve, or a portion of it to be distorted to flattened.

If the entire response curve is distorted, the trouble may be caused by either improper alignment or by a defect in transformer T1. First check to be certain that both the primary and secondary tank circuits are properly tuned to the center frequency. If the discriminator is properly aligned, the trouble is most probably caused by a defect in transformer T1.

If only the upper portion of the response curve is distorted, the trouble may be caused by a defect in diode V1, capacitor C4, Resistor RI, or transformer T1. Use a capacitor checker to check capacitor C4 for

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value and leakage, and use an ohmmeter to check **resistor** RI for a change of value. If these checks fail to locate the trouble, transformer T1 is probably defective.

Conversely, if only the lower portion of the response curve is distorted, the trouble may be caused by a defect in diode V2, capacitor C5, resistor R2, or transformer T1. Check capacitor C5 for value and leakage, and use an ohmmeter to check resistor R2 for a change of value. If these checks fail to locate the trouble, transformer T1 is problebly defective.

# FOSTER-SEELEY DISCRIMINATOR (SEMICONDUCTOR)

#### Application.

**Same** application as electron tube version.

## Characteristics.

Same characteristics as electron tube version.

## Circuit Analysis.

General. The Foster-Seeley discriminator (also known as the phase-shift discriminator) uses a double-tuned r-f transformer to convert the instantaneous frequency variations of the received f-m signal into instantaneous amplitude variations. The amplitude variations are then rectified and filtered to provide a dc output voltage which varies in amplitude and polarity as the input signal varies in frequency. The output voltage is zero when the input frequency is equal to the *center frequency* (unmodulated carrier frequency). When the input frequency rises above the center frequency the output increases in one direction (for example, becomes more positive), and when the input frequency drops below the center frejuency, the output increases in the other direction '(for example, becomes more negative).

Since the output of the Foster-Seeley discriminator is dependent ont only on the input frequency, but also to a certain extent upon the input amplitude, it is necessary to use one or two limiter stages before detection. When properly limited, and the input frequency is varied from a lower frequency through the resonance point of the discriminator, and is then raised higher in frequency, the typical discriminator response curve shown in the following illustration is obtained.



**Discriminator Response Curve** 

The usable portion of the typical "S" shaped response curve is from point A to point B in the illustration. Between these points, the curve is linear and the instantaneous output voltage is directly proportional to the instantaneous frequency deviation.

**Circuit Operation**, The following circuit schematic illustrates a typical Foster-Seeley semiconductor discriminator.



Foster-Seeley Discriminator Circuit (including limiter stage)

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The collector portion of the preceding i-f (limiter) amplifier Q1 is shown on the schematic with conventional emitter resistor  $R_E$  and bypass capacitor  $C_E$ . The collector circuit tank consisting of Cl and L1 is the primary tank of i-f input transformer T1, while L2 and C2 form the secondary tank circuit; both tanks are tuned to the center frequency. Choke L3 forms the dc return for diode rectifiers CR I and CR2. While CR1 and CR2 are shown bypassed by equalizing resistors RI and R2, they are not always used (they are usually used when the diode back resistances are different). Resistors R3 and R4 are the load resistors bypassed by C3 and C4, respectively, for r-f, capacitor C5 is the output coupling capacitor.

The center tap on coil L2 is capacitively coupled through coupling capacitor CCC to the primary. And the full voltage exists across choke L3. At resonance (the center frequency) equal voltages  $e_1$  and  $e_2$  are produced across both halves of L2, thus equal vokages are applied to the anodes of CR1 and CR2. Assuming these voltages are positive, conduction occurs and current flow through diode load resistors R3 and R4 produce equal and opposing voltages across filter capacitors C3 and C4. Since the output is taken from C5 to ground, the equal and oppositely polarized signals cancel and produce no output at the center frequency. However, as the frequency is raised above the center frequency, the phase relationships in the halves of the tank circuit cause a voltage change so that  $e_1$  becomes larger than  $e_2$ . Since it is larger than the voltage across R4, the voltage of R3 predominates, creating a positive output voltage.

Conversely, when the input signal frequency drops below the center frequency and is lower, voltage e<sub>2</sub> is larger than e<sub>1</sub> and the voltage across R4 predominates, creating a negative output. As long as the input frequency variations remain within the limits of peak separation marked A and B on the discriminator curve, a linear frequency versus amplitude relationship is maintained. That is the higher the frequency the larger the positive output voltage becomes, and the lower the frequency the larger the negative output becomes. (If desired, the discriminator transformer can be wound and connected to produce opposite polarities from that described above.) In any event, the output voltage is always developed across both R3 and R4, and it is always the algebraic sum of these. Capacitors C3 and C4 are used to store the instantaneous voltages and develop an average output which varies at audio frequencies. This output, in

turn, is coupled to the audio amplifying stages by coupling capacitor C5 (any coupling method may be, used). Thus, while the input consists of a constantly varying f-m signal of steady amplitude, the output is an audio frequency which varies linearly both in frequency and amplitude in accordance with the frequency swing of the input signal.

#### Failure Analysis.

**No Output.** A defect in the primary or secondary windings of T1, in the RFC, or in tank tuning capacitors C 1, C2, or C3, as well as defective diodes can cause a no-output condition. It is also possible for coupling capacitors CCC or C5 to be open, or for bypass capacitors Cc, as well as C3 or C4 to be shorted and bypass the signal to ground. Use an ohmmeter to check the primary and secondary of T1 and the RFC for continuity, and for shorts to ground. If these checks fail to locate the trouble, use an in-circuit capacitance checker to measure the values of cl, cc, ccc, C3, and C4. Note also, that both diodes must fail to cause no-output, since if only one fails there still will be an output. When possible, use an oscilloscope to observe the waveform at the input and follow the signal through the circuit noting where the signal disappears to locate the source of the trouble.

Low or Distorted Output. A defect in nearly any component in the discriminator circuit may cause the output to be low or distorted. Use a R-F Sweep Generator and an oscilloscope to isolate the trouble. Connect the sweep generator to the input and check the output with the scope on Q1 and at the anode of diode CR1 or CR2. Lack of signal at Q] indicates defective transistor or part in the transistor stage of O1. A signal on O1 but not at the diode anodes indicates CCC is either open or shorted to ground. If the input signal does not change in amplitude as the input frequency varies, the trouble is most likely in the discriminator circuit. To determine if the discriminator is at fault, ground the base of limiter stage Q1 and connect the r-f sweep input to the discriminator input, with the oscilloscope connected to the discriminator output. Adjust the sweep generator to produce an output which varies both below and above the discriminator center frequency and observe if the pattern on the oscilloscope is that of the typical "S" curve shown in the first illustration of this discussion. Defects in the circuit will cause either the entire curve or a portion of it to be distorted, or flattened.

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If the entire response curve is distorted the trouble may be caused by either improper alignment or by a defect in transformer T1. First check to be certain that both the primary and secondary tank circuits are tuned to the proper center frequency. If the discriminator is aligned properly, the trouble is most likely in the transformer.

If only the upper portion of the response curve is distorted, the trouble may be caused by a defect in diode CR1, capacitor C3, resistor R3 or transformer T1. Use an in-circuit capacitance checker to check capacitor C3 for value and leakage, and use an ohmmeter to check resistor R3 for a change of value.

Conversely, if only the bottom portion of the discriminator response curve is distorted, the trouble may be caused by diode CR2, capacitor C4, resistor R4, or transformer T1. If the trouble persists use an in-circuit capacitance checker to check C4 for value and leakage, and use an ohmmeter to check resistor R4 for a change of value. If these checks fail to restore the output to normal, transformer T1 is most likely defective.

### **RATIO DETECTOR (ELECTRON TUBE)**

#### Application.

The ratio detector is used in FM receivers to demodulate the received r-f signal, and in automatic volume control (AVC) circuits to transform frequency changes into dc control voltage changes.

#### Characteristics.

Converts instantaneous frequency variations into instantaneous dc voltage variations.

Employs a double tuned transformer and two diodes.

Has very low inherent distortion.

Output not affected by input amplitude variations.

#### Circuit Analysis.

**General.** The ratio detector uses a double tuned transformer, connected so that the instantaneous frequency variations of the FM input signal are converted into instantaneous amplitude variations. These amplitude variations are rectified to provide a dc output voltage which varies in amplitude and polarity as the input signal varies in frequency. The output is zero when the input frequency is equal to

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*the center frequency* (unmodulated carrier frequency). When the input frequency rises above the center frequency, the output voltage increases irr one direction (for example, becomes more positive).

When the input frequency drops below the center frequency, the output voltage increases in the other direction (for example becomes more negative). The specific polarity of the output voltages obtained for an increase or decrease in input frequency is determined by the design of the circuit and may vary in different circuits.

**Circuit Operation.** The accompanying schematic diagram illustrates a typical ratio detector.



#### Ratio Detector

The input tank circuit, made up of capacitor Cl and the primary winding of transformer T 1, is tuned to the center frequency (fr) of the received r-f signal. Capacitor C2 and secondary winding L2 of transformer T1 form a tank circuit also tuned to the center frequency. Tertiary winding L3 provides additional inductive coupling which reduces the loading effect of the secondary circuit of the detector on the primary circuit of the detector. Diodes V 1 and V2 rectify the signal from the secondary tank circuit. Capacitor C5, in conjunction with resistors RI and R2, determines the operating level of the detector, while capacitors C3 and C4 determine the amplitude and polarity of the output. Capacitors C6 and C7, together with R6, form a filtering network at the output. Resistor R5 modifies the peak diode currents. Resistors R3 and R4 (shown in dotted lines on the schematic) were used in the original design of the circuit to compensate for the changing reactance of the diodes for different amplitude input signals. In practical circuits, however, they are combined with RI and R2, and achieve the same result. The output of the detector is taken from the common connection between C3 and C4 to the common connection between RI and R2 which is also ground. Resistor  $\mathbf{R}_{\mathbf{I}}$  represents the load.

Operation can be best explained with vector diagrams which show the various phase relationships between the voltages and currents in the circuits. The following vector diagram illustrates the circuit phase relationships when the input frequency (f) is equal to the center frequency (fr).



Vector Diagram at Resonance

The input voltage applied to the primary tank circuit is shown as vector  $\mathbf{e}_{\mathbf{p}}$  on the diagram. Since L3 is effectively connected in parallel with the primary tank circuit, voltage  $\mathbf{e}_{\mathbf{p}}$  appears across it. When voltage  $\mathbf{e}_{\mathbf{p}}$  is applied to the primary winding of transformer T1, a voltage is induced in the secondary winding which causes current to flow around the

secondary tank circuit. When the input frequency is at the center frequency, the tank is at resonance and  $\checkmark$ acts resistive. Therefore, tank current is in phase with the primary voltage  $e_p$ , as shown in the vector diagram. The current flowing in the tank causes voltage drops to be produced across each half of the balanced secondary winding of transformer T1, which are of equal magnitude and opposite polarity with respect to the center top of the winding. Since the winding is predominately inductive, the voltage drop . across it is 90° out of phase with the current through it. Because of the center tap arrangement, the voltages to ground at each end of the secondary are 180° out of phase, and are shown as  $e_1$  and  $e_2$  on the vector diagram.

The voltage applied to the cathode of VI consists of the vector sum of voltages  $e_p$  and  $e_1$  shown as  $e_3$ on the diagram. Likewise, the voltage applied to plate of V2 consists of the vector sum of voltages  $e_p$  and  $e_2$ shown as  $e_4$  on the diagram. Since at resonance there is no phase shift, voltages  $e_3$  and  $e_4$  are equal as shown by the same length vectors.

Consider now the manner in which the tubes operate with the discriminator voltages discussed above. When a positive input signal is applied to L1, a voltage of opposite polarity is induced into secondary L2. As shown in the following simplified schematic, the cathode of V1 is negative with respect to its plate, while the plate of V2 is positive with respect to its cathode. Since both voltages are of equal magnitude at resonance, both tubes conduct equally. Hence, current flow through VI is in one direction, while current flow through V2 is in the opposite direction. This direction of current flow causes a negative polarity at point A and a positive polarity at point B, and through R<sub>1</sub> applies a positive charge to C3. In a similar manner current flow through V2 produces a negative polarity at point B \_ and a positive polarity at C. Hence, Capacitor C4 is charged negatively. Since the polarities are additive, capacitor C5 across the output charges to the series value of twice this voltage. In the example shown it is assumed that equal but opposite voltages of 5 volts exist across C3 and C4. Therefore, the total charge across C5 is 10 volts. Since the voltages across C3 and C4 are equal in amplitude and of opposite polarity the output across load R<sub>1</sub> is the algebraic sum or zero.

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Vector Diagram for Higher Input Frequency

**Current Flow and Polarities at Resonance** 

When the input signal reverses polarity, the secondary voltage across L2 also reverses polarity. The cathode of VI is now positive with respect to its plate, and the plate of V2 is negative with respect to its cathode. Under these conditions neither tube conducts, and there is no output. Meanwhile, C5 retains most of its charge because of the large time constant supplied by R1 and R2, and discharges very slightly.

When an input frequency higher than the center frequency is applied to the detector circuit, a phase shift occurs and the current and voltage phase relationships change as shown in the following vector diagram.

When a tuned circuit operates at a higher frequency than resonance, the inductive reactance of the cbil increases, while the capacitive reactance of the tuning capacitor decreases. Therefore, above resonance, the tank is predominately inductive and acts like an inductor. Hence the secondary current is lags the primary voltage e<sub>p</sub>. Although secondary voltage e, and e, are still 180 degrees out of phase, they are also 90 degrees out of phase with the current which produces them (i<sub>s</sub>). Thus the change to a lagging secondary current rotates the vector in a clockwise direction. Referring to the vector diagram it can be seen that  $e_1$  is brought nearer in phase with  $e_p$ , while  $e_2$  is shifted further out of phase with  $e_p$ . Thus the vector sum of  $e_p$  and  $e_1$  is larger than that of  $e_p$  and  $e_2$ . Thesefore, above the center frequency,  $e_3$ , which is applied to the cathode of V 1 becomes greater than  $e_4$ , the voltage applied to the plate of V2.

Let us now examine the manner in which the tubes operate with the discriminator voltages developed above resonance as discussed above. When a

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positive input signal is applied to L1, the same polarity as in the previous example discussed above exists, namely, V1 cathode is negative and V2 plate is positive and both tubes conduct. However,  $e_3$  is not greater than  $e_4$ . Therefore, diode V1 conducts more than diode V2, and C3 charges to a higher voltage than at resonance, as shown in the following simplified illustration.



Current Flow and Polarities Above Resonance

Thus we assume in the figure an 8 volt charge on C3 and only a two volt charge on C4. Since C3 is positive with respect to C4, the output is a 6 volt positive signal. Meanwhile, capacitor C5 still remains charged to the sum of these voltages, or 10 volts, as originally stated. When the input signal reverses polarity, the polarity of the secondary also reverses, biasing both diodes in the opposite direction and preventing conduction. During the nonconducting period, C5 discharges very little because of its long time constant.

When an input frequency lower than the center frequency is applied to the detector circuit, a phase shift also occurs, and the current and voltage phase relationships change as shown in the following vector diagram.



Vector Diagram for Lower Input Frequency

When a series tuned circuit operates at a lower frequency than resonance, the capacitive reactance of the tuning capacitor increases, while the inductive reactance of the coil decreases. Therefore, below resonance, the tank is predominately capacitive and acts like a capacitor. Hence, secondary current is leads the primary voltage  $e_p$ . Although secondary voltages  $e_1$ and e<sub>2</sub> are still 180 degrees out of phase, they are also 90 degrees out of phase with the current which produces them. Thus the change to a leading secondary current rotates the vector in a counterclockwise direction. From the vector diagram it can be seen that  $e_2$  is now brought nearer in phase with  $e_{p}$ , while  $e_{1}$  in shifted further out of phase with  $e_{p}$ . Thus the vector sum of  $e_n$  and  $e_2$  is larger than that of  $e_1$ . Therefore, below center frequency,  $\sim$  $e_4$ , which is applied to the plate of V2, becomes greater than  $e_3$ , the voltage applied to V1.

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# **ELECTRONIC CIRCUITS**

The following simplified schematic shows the polarities and voltages developed for the lower than resonance condition. Once again VI and V2 are conducting, but this time V2 is conducting more than V1, and hence, capacitor C4 is charged to the larger voltage 8 volts while C3 is only charged to 2 volts. The output voltage across the load in this case is a negative 6 volts because C4 is negatively charged with respect to C3. Again the charge across capacitor C5 consists of the sum of the voltages across C3 and C4, 01 10 volts as originally developed.



**Current Flow and Polarities Below Resonance** 

When the input signal reverses its polarity, the **signal** across the secondary also reverses its polarity. The cathode of V1 is now positive with respect to its plate, and the plate of V2 is negative with respect to its cathode. Under these conditions, neither tube conducts, but the time constant of C3 and C4 maintains the current through the load in a negative direction until the next cycle of input.

When the input signal is varied from a lower than center frequency, through center frequency, and is raised to a frequency higher than the center frequency, the typicrd "S" shaped discriminator response curve shown in the following illustration is obtained. The usable portion of the typical "S" shaped response curve is from point A to point B in the **illustration**. Between these points, the curve is linear and the instantaneous output voltage is directly proportional to the instantaneous frequency deviation.



Ratio Detector Response Curve

The output of the ratio detector adjusts itself automatically to the average r-f amplitude of the input signal. Through the action of resistors R1 and R2, together with capacitor C5, audio output variations which would occur due to r-f amplitude variations in the input (such as noise) are eliminated. As previously mentioned, C5 charges to the sum of  $e_3$ and  $e_4$ . The average sum of  $e_3$  and  $e_4$  depends upon the average r-f amplitude of  $\mathbf{e_p}$ . Any amplitude variations at the input of the detector tends to change the voltages across R1 and R2, but because of the long time constant of C5, across the resistors, these voltages are held constant. Before the capacitor can charge or discharge to the higher or lower amplitude variation the impulse disappears, and the difference in charge on C5 is so slight that it is not discernible in the output. Because the voltage across C5 remains relatively stable and changes only with the amplitude of the center frequency, and since it is negative with respect to ground it is usually used for automatic volume control (AVC) applications.

Capacitors C6 and C7 together with resistor R6 form a low pass filter which attenuates the high audio frequencies and passes the lower frequencies. This is known as a de-emphasis network, which compensates for the pre-emphasis with which the high frequencies are transmitted and returns the audio frequency

**balance** to normal. When pre-emphasis is not employed these parts are not needed.

# Failure Analysis.

**No Output.** A defective discriminator transformer, Tl, shorted tuning capacitor Cl or C2, an open output resistor R6, and open coupling capacitor C8, or shorted filter capacitors (C6 or C7) will produce a no output condition. Check the continuity of the windings of T1 with an ohmmeter. Check capacitors Cl, C2, C6 and C7 for shorts, and capacitor C8 for an open with an ohmmeter, and measure the resistance of R6. If above checks fail to restore the output, check all capacitors with an in-circuit capacitor checker. Note that one defective diode will produce a partial loss of output, and that both diodes must fail to cause a complete loss of output.

Low or Distorted **Output.** A defect in nearly any component in the detector circuit may cause the output to be either low or distorted. Therefore, it is good practice to use an r-f sweep generator and an oscilloscope to isolate the trouble. Ground the grid of the last I-F tube, connect the r-f sweep generator to the detector input, and connect the oscilloscope to the detector output. With the sweep generator set to produce an output which varies above and below the center frequency, the pattern observed on the oscilloscope should be similar to the discriminator response curve illustrated previously. Defects in the circuit will cause either the entire curve, or a portion of it to be distorted or flattened.

If the entire **response** curve is distorted, the trouble may be caused by either improper alignment or by a defect in the transformer T1. First check to be certain that both primary and secondary tank circuits are properly tuned to the center frequency. If the detector is properly aligned, check capacitors Cl and C2 with an in-circuit capacitor checker. Check RI and R2 with an ohmmeter for their proper values, and capacitor C5 for value and leakage with an in-circuit capacitor checker. If the trouble is still not located, the trouble is most likely caused by a defect in transformer T1.

If only the upper portion of the response curve is distorted, the trouble may be caused by a defect in diode V1, capacitor C3, or transformer T1. If the diode VI checks good, use an in-circuit capacitor checker to check C3 for value and leakage. If these checks fail to locate the trouble, transformer T1 is probably defective.

Conversely, if only the lower portion of the response curve is distorted, the trouble may be caused by a defect in diode V2, capacitor C4, or transformer T1. Use an in-circuit capacitor checker to check C4 for value and **leadage**. If these checks fail to locate the trouble, transformer T1 is probably defective.

# **RATIO DETECTOR (SEMICONDUCTOR)**

#### Application.

Same application as electron tube version.

# Characteristics.

Same characteristics as electron tube version.

# Circuit Analysis.

General. The semiconductor ratio detector, like the electron tube ratio detector previously discussed the this Handbook, uses a double tuned transformer (discriminator) connected so that the instantaneous frequency variations of the FM input signal are converted into instantaneous amplitude variations. These amplitude variations are rectified by the diodes to provide a dc output voltage which varies in amplitude and polarity as the input signal varies in frequency. The output is zero when the input is equal to the center frequency (unmodulated carrier" frequency). When the input frequency rises above the center frequency, the output "voltage increases in one direction (for example, becomes more negative). The specific polarity of the output voltages obtained for an increase or decrease in input frequency is determined by the design of the circuits and may vary from circuit to circuit.

**Circuit Operation.** The accompanying schematic diagram illustrates a typical semiconductor ratio detector.



**Ratio Detector** 

The input tank circuit comprised of Cl and primary winding L1 or T1 is tuned to the center frequency of the received f-m signal. Secondary winding L2 and capacitor C2 also form a tank circuit tuned to the center frequency. Tertiary winding L3 provides additional inductive coupling which reduces the loading effect of the secondary on the primary circuit of the detector. Solid state diodes CR1 and CR2 rectify the signal from the secondary tank. Capacitor C5, in conjunction with resistors R1 and R2 determines the operating level of the detector, while capacitors C3 and C4 determine the amplitude and polarity of the output. Resistor R3 modifies the peak diode current and furnishes a dc return path to ground. The output of the detector is taken from the common connection between C3 and C4 to ground, which is also the common connection of R1 and R2. Resistor  $\mathbf{R}_{\mathbf{L}}$  is the load resistor. A low-pass filter is formed by R5 together with C6 and C7 to provide high frequency reemphasis. Capacitor C8 is the output coupling capacitor.

When input voltage  $\mathbf{e_p}$  is applied to the primary, it also appears across L3 since it is effectively connected

in parallel with the primary tank circuit by inductive coupling. When voltage  $e_p$  is applied to the primary winding of transformer T1, a voltage is also inducted in the secondary winding and causes current to flow around the secondary tank circuit. When the input frequency is at the center frequency, the tank is at resonance, is resistive, and acts like a resistor. Therefore, tank current is in phase with primary voltage e<sub>n</sub>. The current flowing in the tank circuit causes equal voltage drops to be produced across each half of the balanced secondary winding of Tl, which are of equal magnitude and of opposite polarity with respect to the center tap of the winding. Since the winding is predominately inductive, the voltage drop across it is 90 degrees out of phase with the current through it. At the same time, because of the center tap arrangement, the voltages to ground at each end of the secondary are 180 degrees out of phase and are shown as e, and e, on the schematic.

The voltage applied to the cathode of CR1 consists of the vector sum of  $\mathbf{e}_1$  and  $\mathbf{e}_p$ . Likewise, the voltage applied to the anode of CR2 consists of the vector sum of voltages e, and e... Since at resomnce there is no phase shift, both voltages are equal. Consider now the manner in which the diodes operate with the discriminator voltage discussed above. When a positive input signal is applied to Ll, a voltage of opposite polarity is induced into secondary L2. As shown in the accompanying simplified schematic, the cathode of CR1 is negative with respect to its anode and is forward biased, while the anode of CR2 is positive with respect to its cathode and is likewise, forward biased. Since both voltages are of equal magnitude at resonance, both diodes conduct equally. Hence current flow through CR1 is in one direction, while the current through CR2 is in the opposite direction. This direction of current flow causes a negative polarity at point A and a positive polarity at point B. Through  $\mathbf{R}_{\mathbf{I}}$  a positive charge is applied to C3. In a similar manner current flow through CR2 produces a negative polarity at point B and a positive polarity at C. Hence Capacitor C4 is charged negatively. Since the polarities are additive, capacitor C5 across the output charges to the series value of twice this voltage.



Simplified Schematic

In the example shown, it is assumed that equal but opposite voltages of 5 volts exist across C3 and C4. Therefore, the total charge across C5 is 10 volts. Since the voltage across C3 and C4 are equal in amplitude (5 volts) and of opposite polarity, the output across load resistor  $R_L$  is the algebraic sum or zero.

When the input signal reverses polarity, the secondary voltage across L2 also reverses polarity. The cathode of CR1 is *now* positive with respect to its anode, and the anode of CR2 is negative with respect to its cathode. Under these reverse-bias conditions neither diode conducts, and there is also no output. Meanwhile C5 retains most of its charge because of the long time constant offered by RI and R2 and discharges very slightly.

When a tuned circuit operates at a higher frequency than resonance, the inductive reactance of the coil increases, while the capacitive reactance of the tuning capacitor decreases. Therefore, above resonance the tank is predominately inductive and acts like an inductor. Hence the secondary current (i, ) lags the primary voltage e<sub>n</sub>. Therefore, when an input frequency higher than the center frequency is applied to the detector circuit, a phase shift occurs. Although secondary voltages e, and e, are still 180 degrees out of phase, they are also 90 degrees out of phase with the current  $(i_{c})$  which produces them. Thus the change to a lagging secondary current rotates the vector in a clockwise direction and e is brought nearer in phase with primary voltage  $e_p$ , while  $e_2$  is shifted further out of phase with e<sub>p</sub>. Thus the vector

sum of  $\mathbf{e_p}$  and  $\mathbf{e_i}$  is now larger than that of  $\mathbf{e_p}$  and  $\mathbf{e_2}$ . Therefore, above the center frequency the voltage applied to the cathode of CR1 becomes greater than the voltage applied to the anode of CR2.

Consider not the manner in which the diodes operate with the discriminator voltages developed above resonance, as discussed above. When a positive input **is** applied to **L1** the same polarity as in the previous example discussed above exists, namely CRI cathode is negative and CR2 anode is positive, and both diodes conduct. However,  $\mathbf{e_1}$  is now greater than  $\mathbf{e_2}$ . Therefore, diode CR1 conducts more than diode CR2, and C3 charges to a higher voltage than at resonance, as shown in the following simplified illustration.



**Current Flow and Polarities above Resonanea** 

Thus, we assume in the figure an 8-volt charge on C3 and only a 2-volt charge on C4. Since C3 is positive with respect to C4, the output is a 6-volt positive signal. Meanwhile, capacitor C5 still remains charged to the sum of these voltages or 10 volts, as originally stated. When the input signal reverses polarity, the polarity of the secondary also reverses, biasing both diodes in the opposite direction, and preventing conduction. During the nonconducting period, C5 discharges very little because of the long time constant.

When a tuned circuit operates at a lower frequency than resonance, the capacitive reactance of the tuning capacitor increases, while the inductive reactance of the tank coil decreases. Therefore, below resonance, the tank is predominately capacitive and acts like a capacitor. When an input frequency lower than the center frequency is applied to the detector circuit, a phase shift also occurs and secondary current  $i_s$  *leads* the primary voltage  $e_p$ . Although secondary voltages  $e_1$  and  $e_2$  are still 180 degrees out of phase they are also 90 degrees out of phase with the current which produces them. Thus the change to a leading secondary current rotates the vector in a counterclockwise direction, and  $e_2$  is now brought nearer in phase with  $e_p$  while  $e_1$  is shifted further out of phase with  $e_p$ . Thus the vector sum of  $e_p$  and  $e_2$  is now larger than that of  $e_p$  and  $e_1$ . Therefore, below the center frequency the voltage applied to the anode of CR2 becomes greater than the voltage applied to the cathode of CRI as shown in the following simplified schematic.



**Current Flow and Polarities Below Resonance** 

Once again CR1 and CR2 are conducting, but this time CR2 is conducting more than CR1, hence, capacitor C4 is charged to the larger voltage of 8 volts, while C3 is only charged to 2 volts. The output voltage across the load in this case is a negative 6 volts because C4 is charged negatively with respect to C3. Again the charge across capacitor C5 consists of the sum of the voltages across C3 and C4, or 10 volts as originally developed.

When the input signal reverses its polarity, the signal across the secondary also reverses its polarity. The cathode of CR1 is now positive with respect to its anode and the anode of CR2 is negative with respect to its cathode. Under these conditions, neither diode conducts, but the time constant of C5 together with RI and R1 maintains the current through the load in a negative direction until the next cycle of input, and C5 discharges but **slightly**.

The output of the ratio detector adjusts itself automatically to the average amplitude of the input signal. Through the action of resistors RI and R2 together with capacitor C5, audio output variations which would occur due to r-f amplitude variations in the input (such as noise) are eliminated. Since C5 charges to the sum of the voltages developed across R1 and R2, any amplitude variations at the input of the detector tends to change the voltages across R1 and R2, but because of the long time constant of C5 across these resistors, these voltages are held to a minimum. Before C5 can charge or discharge to the higher or lower amplitude variation the impulse disappears, and the difference in charge across C5 is so slight that it is not discernible in the output. Because the voltage across C5 remains relatively stable and changes only with the amplitude of the center frequency, and since it is negative with respect to ground, it is usually used for automatic volume control (AVC) applications.

Capacitors C6 and C7 together with resistor R5 form a **low** pass filter which attenuates the high audio frequencies and passes the lower frequencies. This is known as a de-emphasis network, which compensates for the preemphasis with which the high frequencies are transmitted, and returns the audio frequency balance to normal. When pre-emphasis is not employed these parts are not needed.

### Failure Analysis.

**No Output.** A defective discriminator transformer, T1, shorted tuning capacitor Cl and C2, an open output resistor R5, an open coupling capacitor C8, or shorted filter capacitors (C6 or C7) will produce a no-output condition. Check the continuity of the windings of T1 with an ohmmeter. Check capacitors Cl, C2, C6 and C7 for shorts and capacitor C8 for an open with an ohmmeter, and measure the resistance of R5. If any of these checks fail to restore the output check all capacitors for value with an incircuit capacitance checker. Note that while one defective diode will produce a partial loss of output, both diodes must fail to cause a complete loss of output,

Low or Distorted Output. A defect in nearly any component of the detector will cause the output to be either low or distorted. Therefore, it is good practive to use an r-f sweep generator and an oscilloscope to locate the trouble. Ground the grid of the

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last I-F stage and connect the r-f sweep generator to the detector input. With the sweep generator set to produce an output which varies above and below the center frequency, the pattern observed on the oscilloscope should be similar the discriminator response curve illustrated previously. Defects in the response curve will cause either the entire curve or a portion of it to be distored or flattened.

If the entire curve is distorted, the trouble maybe caused by improper alignment or by a defect in transformer T1. First check to be certain that both primary and secondary circuits are tuned properly to the center frequency. If the detector is properly aligned, check capacitors C 1 and C2 with an in-circuit capacitance checker. Check R1 and R2 for their proper value with an ohmmeter, and capacitor C5 for value and leakage with an in-circuit capacitance checker. If the trouble is still not located, it is most likely caused by a defect in transformer T1.

If only the upper portion of the response curve is distorted, the trouble may be caused by a defect in diode CR1, capacitor C3, or transformer T1.

Conversely, if only the lower portion of the response curve is distorted, the trouble may be caused by a defect in diode CR2, capacitor C4, or transformer T1.

# TRAVIS DISCRIMINATOR (ELECTRON TUBE)

### Application.

**The** Travis discriminator is used as a detector in FM receivers and for automatic frequency control (AFC) circuits.

#### Characteristics.

Converts instantaneous frequency variations into instantaneous dc voltage variations.

Employs a triple-tuned transformer.

Has low inherent distortion.

Circuit is difficult to align.

Must be preceded by a limiter since the output is affected by input amplitude variations.

# Circuit Analysis.

General. The Travis discriminator uses two secondary tank circuits, with each tank turned so slightly different resonant frequencies to convert the FM input signal frequency variations into amplitude variations. The r-f amplitude variations are then rectified and filtered to produce a dc output voltage which varies in accordance with the variations of the input frequency. When the input frequency is equal to the center frequency (unmodulated carrier frequency), the discriminator output voltage is zero. As the input frequency rises above the center frequency, the output voltage increases in one direction, for example, increases in the positive direction, and as the input frequency drops below the center frequency, the output voltage increases in the other direction (for example, increases in the negative direction). Thus, the instantaneous discriminator output voltage is dependent on the instantaneous input frequency deviation (shift) from the center frequency. The specific polarity of output voltage obtained for an increase or a decrease in input frequency is determined by the design of the circuit and may vary in different circuits.

The Travis discriminator output is dependent not only on variations in the input frequency, but also to a certain extent, on variations in the input amplitude. Since variations in the amplitude of the FM signal are caused by unwanted noise or fading, they must be prevented from reaching the discriminator or the circuit will reproduce the unwanted noise as well as the desired intelligence. To prevent this, the discriminator is usually preceded by a limiter such as those explained in the Special Circuits Section of this Handbook. The limiter produces an r-f output signal of constant amplitude regardless of input amplitude variations, and thus effectively eliminates any AM noise from the FM signal.

Circuit Operation. The accompanying schematic diagram illustrates a simple Travis discriminator.



Travis Discriminator

Capacitor Cl and the primary winding (L<sub>2</sub>) of transformer T1 form a resonant tank circuit which is tuned to the center frequency. The upper half of the secondary winding  $(L_{s1})$  of transformer T1 and capacitor C2 form a resonant tank circuit which is tuned above the center frequency by an amount slightly greater than the maximum input frequency deviation. The lower half of the secondary winding  $(L_{s2})$  of transformer T1 and capacitor C3 form a resonant tank circuit which is tuned below the center frequency by the same amount that the upper tank circuit is tuned above the center frequency. The r-f signals from the two tank circuits are rectified by diodes VI and V2, and a dc voltage is developed across load resistors R1 and R2. Capacitors C4 and C5 are filter capacitors which remove the r-f ripple component from the detected signals developed across resistors R1 and R2, and holds these voltages relatively constant. The total output voltage is taken across the sen"es combination of resistors R1 and R2 (that is, from the cathode of diode V1 to ground).

When an input signal with a frequency equal to the center frequency is applied to the primary tank circuit ( $L_p$  and Cl), a voltage is induced into the secondary winding of transformer T1 which develops r-f voltages of equal amplitudes in secondary tank circuits  $L_{s1}$  and C2, and  $L_{s2}$  and C2, as shown in the accompanying illustration of the tank circuit response.





Since the two secondary tank circuits are tuned to resonant frequencies  $(f_1 \text{ and } f_2)$  equidistant from the center frequency, both tank circuits are tuned offresonance by equal amounts and equal r-f voltages are produced. On the positive half of the input cycle the anode of V1 is positive and current flows through resistor R1, developing a dc output voltage with polarity as marked on the schematic. Simultaneously, the anode of diode V2 is also positive and the d-c output voltage produced across R2 by current flow is equal and opposite that of RI. Therefore, the total output voltage taken across the two resistors in series (from cathode of V1 to ground) is zero. The condition is shown at the center frequency  $(f_{p})$  on the accompanying discriminator response curve illustration.



**Discriminator Response Curva** 

Voltage  $E_1$  is developed across load resistor R1 (with respect to ground), and voitage  $E_2$  is developed across load resistor R2. As shown in the illustration, voltage  $E_1$  is equal in magnitude and opposite in polarity to voltage  $E_2$  at the center frequency. Thus, at the center frequency, the output voltage ( $E_{out}$ ) is zero.

When an input frequency higher than the center frequency is applied to the primary tank circuit of the discriminator, a voltage is induced into the secondary winding of transformer T1 which is nearer to the resonant frequency of the upper tank, and therefore, a larger voltage is applied to V1 anode. Consequently, VI conducts heavvier and the iarger current flow through RI produces a larger dc output voltage, El, charging C4 to a higher value. In a similar manner, the voltage developed across the lower tank circuit as shown by response curve B is further away from the lower-tank resonant frequency and the positive anode voltage on V2 is lower than that of V1. Hence, the small current flow through resistor R2 develops a smaller output voltage, E2, and C5 is charged to a lower value. The net output voltage,  $E_{out}$  across the two resistors is positive when the input frequency is higher than the center frequency, since El is always positive and greater than E2. When a still higher frequency is applied the primary tank, the same action occurs except that El becomes much larger and E2 becomes much smaller. Likewise, when the input frequency is lower and nearer the lower

tank frequency the opposite condition prevails. That is El becomes smaller, while E2 becomes larger. Consequently, the net output voltage,  $E_{out}$ , across the two resistors is negative when the input frequency is lower than the center frequency, since E2 is always negative and larger than El,

Thus, the output voltage of the Travis discriminator varies in magnitude and polarity as the input frequency varies above the below the center frequency. As mentioned previously, the discriminator output is dependent not only on the input frequency, but also to a certain extent on the input amplitude. If the input signal amplitude drops below the limiting level of the preceding limiter stage, the signal and any variations in the signal amplitude will appear at the discriminator. Since the discriminator diodes are essentially half-wave rectifiers, they will detect the amplitude variations in much the same manner as an AM detector, producing noise in the discriminator output. Thus, for proper operation, the input signal to the limiter must always remain above the limiting level of the stage. Another disadvantage of the Travis discriminator is that it is difficult to align because each of the three tank circuits must be tuned to a slightly different resonant frequency. Because it is sensitive to amplitude variations, and because it is difficult to align, the Travis discriminator is not often used in modern FM circuits.

### Failure Analysis.

**No Output. Loss** of input signal, the failure of capacitor Cl, transformer T1, or both diodes can cause a no-output condition. (Note that if only one diode fails, the output will be distorted rather than completely absent.) If the diodes are not at fault, either transformer T1 is defective or capacitor Cl is shorted.

Low or Distorted Output. The failure of nearly any component in the Travis discriminator may cause the output to be low or distorted. Therefore, it is good practice to use an r-f sweep generator and an oscilloscope to locate the specific portion of the circuit that is faulty. First, use the oscilloscope to observe the input to the discriminator to be certain that the trouble is not due to distorted input signrd. If the correct discriminator input signal is present, ground the grid of the limiter stage preceding the discriminator, connect the r-f sweep generator to the discriminator output. With the sweep generator adjusted to produce an output signal which varies above and below the center frequency, a characteristic "S" shaped discriminator response curve will be obtained if the circuit is operating properly and aligned correctly. Defects in the circuit or alignment, however, will cause a portion of the response curve to be distorted.

If only the upper (positive) portion of the response curve is distorted, the trouble may be caused by a defect in diode VI, resistor RI, capacitors C2 or C4, transformer T1 or misalignment of tank  $C_2$ ,  $L_s$ . Check resistor R1 for proper value with an ohmmeter, and check capacitor C4 for proper value, leakage, or a short with an in-circuit capacitance tester. If these checks fail to locate the defective component, the transformer assembly (consisting of T1 and Cl, C2, and C3) is either misaligned or defective. Check the alignment.

When only the lower (negative) portion of the response curve is distorted, it may be caused by a defect in diode V2, resistor R2, capacitors C3 or C5, transformer Tl, or misalignment of tank C3,  $L_{s2}$ . Check resistor R2 for proper value with an ohmmeter, and check capacitor C5 for proper value with an ohmmeter, and check capacitor C5 for proper value, leakage, or a short, with an in-circuit capacitance tester. If these checks fail to locate the defective component, the transformer assembly (Tl, Cl, C2, and C3) is either misaligned or defective. Check the alignment.

Distortion or flattening of the entire response curve is usually caused by improper alignment of the discriminator, although it may also be caused by low diode emission.

### GATED-BEAM DETECTOR

### Application.

**The** gated-beam detector is used in FM receivers to demodulate the received r-f signal.

### Characteristics.

Converts instantaneous frequency variations into instantaneous dc voltage variations.

Employs three tuned tank circuits and a special beam-power tube.

Has low inherent distortion.

Output is independent of input amplitude variations. Provides both limiting and discriminator action in a single tube.

#### Circuit Analysis.

**General.** The gated-beam detector uses a gatedbeam tube to limit, detect, and amplify the received f-m r-f signal. The output is a dc voltage which varies in amplitude and polarity as the input varies in frequency. This output voltage is zero when the input frequency is equal to the center frequency (unmodulated carrier frequency). When the input frequency rises above the center frequency, the output voltage increases in a positive direction, and when the input frequency drops below the center frequency, the output increases in a negative direction.

**Circuit Operation.** Before attempting to explain the circuit operation of the gated beam detector, a brief review of the tube used in the circuit is essential. The following illustration shows a cross-sectional diagram of a typical gated-beam tube.



Gated-Beam Tube Cross-Section

There are two major differences between the gated-beam tube and an ordinary pentode. First, the flow of electrons from the cathode to the plate is maintained in a concentrated beam formed by the elements of the tube, and secondly, cathode current

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flows at all times, even during the period of time during which no plate current flows.

The shield around the cathode, known as focusing **plate** No. I, is internally connected to the cathode, and as the electrons leave the cathode they pass through a narrow opening in the shield, which is at cathode potential and repels electrons. Thus a narrow stream of electrons is formed.

As the electron stream enters the accelerating chamber, which is at a high positive potential, it tends to spread, due to the attraction of the positive field. Ordinarily, the stream would continue to spread, but as it approaches the No. 1 control grid, it is prevented from spreading further by the repelling action of a second focusing plate, also connected to the cathode. Once the electrons pass through the first control grid. they are attracted towards the accelerator grid, which is at the same potential as the accelerator plate, and again the electron stream tends to spread. However, before the spreading becomes excessive, the stream enters the field of focusing plate No. 3 which is also at cathode potential, and further spreading is checked. The focusing plate is provided with a narrow opening, which concentrates the beam into a narrow stream again as it passes through this orifice. The electron stream then passes through a second control grid (referred to as the quadrature grid) and is attracted to the potential positive plate.

If a signal is applied to the first control grid, and it is sufficiently negative to prevent the electron stream from passing through it, the electrons approaching this grid rapidly build up a dense space charge in front of the grid. Because electrons repel each other, the accumulated space charge aids the control grid in quickly cutting off plate current flow, and accounts for the sharp cut-off tube characteristic. (This control grid is also referred to as the limiter grid for this reason.) The electrons cannot return to the cathode because of the narrow opening in the focusing plate, and they are attracted to the wall of the accelerator chamber instead, thus maintaining cathode current flow, as shown in the following illustration.





In a similar manner, when a signal of sufficient strength and of proper polarity to repel the electron stream is applied to the quadrature grid (No. 2 control grid), with the limiter grid above cut-off, plate current will not flow. Cathode current flow continues, however, because the electron stream is attracted to the accelerator wall instead, as illustrated in the following figure.



Second Control (Quadrature) Grid at Cut-off

To summarize tube operation, both the limiter grid and the quadrature grid must be sufficiently positive at the same time to permit passage of the electron stream to the plate.

The following circuit schematic illustrates the gated beam tube connected as a typical gated-beam detector.



#### Typical Gated-Baam Detaetor

The input tank circuit, consisting of LI, the primary of i-f transformer T1, and capacitor Cl, is tuned to the center frequency of the incoming f-m signal. L2, the secondary of the transformer TI, and capacitor C2, also. comprise another tank circuit, which is also tuned to the center frequency. The first

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grid of the tube and the cathode, perform the function of a limiter stage, with resistor RI and capacitor C4 in the cathode circuit to provide a method of adjusting the limiter bias. The accelerator grid is connected to voltage-dropping resistor R3 which establishes the proper voltage on the accelerator grid, andC5 bypasses it to ground. Capacitor C3, together with L3, form another tank circuit also tuned to the center frequency, and is connected to the second control grid. Resistor R2, (usually of a small value) is placed in the plate lead to increase output linearity. Resistor R4 is the plate load, and together with capacitor C6 forms an integrating network which produces the sine-wave output. The output is taken from across C6, and applied to the audio stages through coupling capacitor Cc.

The limiting capabilities of the gated beam detector are much better than that of a conventional pentode, because of the sharp control characteristic, as shown in the following graph.



- LIMITER GRID VOLTAGE IN VOLTS -----

Limiter Grid Tube Control Curve

Cathode resistor R1 is adjusted to bias the limiter at the center of the steepest part of the controlcharacteristic curve. With no signal applied to the limiter grid, the tube conducts. When the electron stream arrives at the quadrature grid, some electrons are absorbed by this grid, and the resulting current flow charges C3 of the quadrature tank circuit. When C3 is charged sufficiently negative, the grid current stops and this negative charge momentarily maintains the quadrature grid at cut-off, Tank inductor L3, however, tries to keep the current moving in the same direction, but when its field collapses it causes a reverse flow of current which discharges C3. When C3 discharges sufficiently, the grid again becomes positive and begins drawing grid current, and the cycle repeats. Since the tank is tuned to the center frequency of the received signal, it oscillates at the tuned frequency. The voltage across C3 lags the current which produces it, and the result is a series of pulses appearing on the quadrature grid at the center frequency, but lagging the limiter grid voltage by 90 degrees. Because the quadrature grid has the same control characteristics as the limiter grid, these pulses place the tube alternately at cut-off and at saturation on alternate half cycles of oscillation.

When a signrd appears on the limiter grid at the center frequency and increases slightly in a positive direction, the tube is effectively driven into saturation. That is, as the electron stream passes through the limiter and accelerator grids, and arrives at the quadrature grid, the quadrature grid is out-of-phase and is at cut-off, and the electron stream is attracted to the accelerator wall. However, some 90 degrees later, the quadrature grid shifts in a positive direction because of the favorable oscillation of the quadrature tank, and this time the electron stream is permitted to pass through the quadrature grid to the plate. Before the quadrature grid phase changes, the signal applied to the limiter grid drives the tube quickly into cut-off, and plate current again ceases. The resulting signal appearing on the plate, therefore, is a square shaped pulse, which starts with the delayed opening of the quadrature grid, and ends with the closing of the limiter grid, as shown in the following "At Center Frequency" illustration.



**Relationship of Pulses At Center Frequency** 

If the signal on the limiter **grid** shifts to a frequency higher than the center frequency, the pulse appears on the limiter grid at an earlier time than at the center frequency, and therefore, also arrives at the quadrature grid at an earlier time. Since the pulses on the quadrature grid are still occurring at the center frequency (because of tank circuit oscillation), and the limiter pulse arrives earlier, the resulting pulse relationships are as shown in the "Above Center Frequency" waveform illustration.



Relationship of Pulses above Center Frequency

Since plate current starts with the delayed opening of the quadrature grid, and ends with the closing of the limiter grid, the plate pulse is now narrower than it was at the center frequency.

Conversely, if the signal on the limiter grid shifts to a frequency below the center frequency, the pulse arrives on the limiter grid at a later time, and thus arrives at the quadrature grid at a later time. It is therefore nearer in phase with the pulses on the quadrature grid, since these quadrature pulses are still occurring at the center frequency, and the resulting pulse relationships are as shown in the "Below Center Frequency" waveform illustration.

Under the three circumstances discussed above, the peak amplitude of the plate current remains the same (it is effectively at saturation and limited), while the variations in the frequency of the input pulses are represented at the plate only by the length of time for which plate current flows. A higher input frequency produces a shorter duration of plate current, and a lower input frequency produces a longer duration of plate current.

These plate pulses, however, are occurring at an r-f rate, and therefore will not be reproduced by the following audio stages. However, since the width of the plate pulses constantly vary in accordance with the f-m modulation, the plate pulses also vary at an audio rate. Therefore, the average plate current varies at audio frequencies, and a useable audio output is obtained by an integrating network consisting of C6 and R4. Since the charge on C6 varies at the same rate as the average plate current, taking the output from capacitor C6, provides an audio output, and at the same time, it changes the squared pulse into a useable sine-wave to minimize distortion.



**Relationship of Pulses Below Center Frequency** 

The advantage of the Gated Beam Detector lies in its extreme simplicity. It employs only one tube, yet provides a very effective limiter with a linear detector. It requires relatively few components, and is very easily adjusted. Operation, however, is limited to the frequencies below 30 MHz. Since at the higher frequencies, the shunting effect of the interelectrode capacitance between the limiter and quadrature grids is sufficient to produce an out-of-phase voltage across the quadrature grid, which subtracts from the quadrature voltage and reduces the output. This effect is minimized in some circuits by the addition of a screen grid, to the tube or by careful shielding, but neither method completely eliminates the out-ofphase effect, and for this reason, the gated-beam circuit is usually used ordy in low frequency applications.

#### Failure Analysis.

**No output.** A defect in nearly any component in the circuit could cause a no-output condition to exist. Check the plate supply voltage at the tube socket, if

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plate voltage is not present, check resistors R2 and R4 and capacitor C6. If plate and grid voltages are normal, the tube is probably defective.

Check for a signal on the limiter grid with an oscilloscope. If no signal is present, check for a signal on the primary of the transformer. If still no signal appears, the trouble is somewhere in the preceding stages, and the detector is probably not faulty. If there is a signal on the primary of the transformer, check the tuning capacitors with an in-circuit capacitor checker. If they are found to be good, the trouble is probably a defective transformer. Check cathode resistor R1 for proper value and adjustment, and capacitor C4 also, using an in-circuit capacitor checker. With the oscilloscope, check for a signal on the quadrature grid. If a signal is present, make sure it is at the center frequency. If no signal is present, check C3 with an in-circuit capacitor checker, and L3 with an ohmmeter. Check R3 for proper value, and C5 for a short to ground.

Low or Distorted Output. It is unlikely that a low output condition will exist, but if it does, R2, R4, or C6 is most likely at fault. Check R2 and R4 for proper value, and C6 with an in-circuit capacitor checker.

If the output is distorted, make the checks just mentioned above for a low output condition, and if the distortion still occurs, make certain that the three tanks are aligned properly, and contain no defective components. Also check R1 for proper value and adjustment, using a voltohmmeter and also check capacitor C4 with an incircuit capacitor checker.

# PART 10-3. VIDEO

## **VIDEO DETECTORS**

## General.

A video detector is very similar to the standard AM detector, with the exception of the requirement for handling a broader range of frequencies. Since it is located between the IF and the video amplifier stages, it must be able to handle the same wide range of frequencies as the IF and video amplifier stages without distortion. The IF frequencies used in radar applications vary from about 30 Hz to 8 MHz, and in television, from about 20 MHz to 4.5 Hz. This requirement necessitates the use of high-frequency compensating circuits in the detector output, which consist of both series and hunt peaking circuits. When using electron tube diodes, a diode with low plate-tocathode capacitance should be selected. When using semiconductor diodes, it is necessary to keep the input impedance level on the high side to maintain the rectification efficiency of the diode at a high level. A transistor, however, can serve efficiently as a video detector into a relatively low value of impedance. The high base impedance provides the necessary high impedance input, while the output at medium or moderately low impedance matches the following video amplifier stage.

# **BASIC VIDEO OETECTOR (ELECTRON TUBE)**

#### Application.

The video detector is used to change the received amplitude modulated video signal into a dc voltage.

# Characteristics.

Employs a basic AM diode detector.

Has a wider bandwidth than the conventional AM detector.

Employs compensating networks for frequency compensation and to improve linearity.

#### **Circuit Analysis.**

**General.** The operation of the basic video detector is identical to the operation of the AM diode detector previously discussed in this section of the Handbook. The only difference lies in the addition of compensating circuits for the added frequency response requirements. Discussion of the operation of the detector in stripping off the modulation from the carrier is covered completely in the previous discussion of the diode detector. The reader should refer to the discussion of the Diode Detector in this section of the Handbook for proper background before proceeding with the discussion of the video detector.

**Circuit Operation.** The schematic diagram of a typical video detector employing series and shunt peaking is shown in the following illustration.



Basic Video Detector (Electron Tube)

The anode of diode VI is connected to the untuned secondary of IF transformer, T1, with the primary tuned by capacitor C. Inductance L1, in series with resistor RI, together with capacitor C1, forms a shunt peaking circuit, referred to as impedance network Z1. Inductance L2, together with R2, forms a series peaking circuit, referred to as impedance network Z2. Capacitor C2 is the output coupling capacitor. Resistor R1 broadens the bandwidth of Z1, and R2 broadens the bandwidth of Z2.

Peaking circuits Z1 and Z2 are utilized to improve the output linearity, and provide a wide band-pass characteristic. The circuit operates in the following manner. A frequency increase causes the capacitive reactance of the stray capacitance to decrease, and since this stray capacitance (represented by Cl) shunts the output, the output voltage tends to decrease at high video frequencies. Z1 is a paralleltuned circuit resonated to the high frequency at which the output first tends to decrease, by the stray and distributed wiring and circuit capacitance represented by Cl. Since the impedance of the parallel tuned (shunt peaked) circuit is maximum at resonance, the output remains linear beyond the high frequency drop-off point (without compensation). The bandwidth of this tuned (shunt peaked) circuit is widened because the Q of the circuit is decreased by the presence of series resistor RI. As the output frequency is increased still further, it passes beyond the resonant peak of Z1, and as the impedance of Z1 now decreases, the output again tends to decrease.

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**Z2**, however, forms another broadly-tuned circuit, and is series-resonated at a point above the resonant frequency of Z1. These circuits are so tuned that some overlap of the tuned circuit response curves occurs, as shown in the following illustration.



Combined Response Curve of Z1 and Z2

Since the impedance of a series tuned circuit is minimum at resonance, and because Z2 is in series with the load, the output once again is extended. Actually L2 is series peaked using the stray capacitance to ground, and is also broadened by shunt resistor R2.

The resultant overall response curve for the video detector is shown as follows.



**Overall Response Curve for Video Detector** 

#### Failure Analysis.

**No Output.** A defect in transformer T1, a defective tube, or an open C2 will cause a no-output condition. Check the continuity of the windings of T1 with an ohmmeter. Check C2 for an open with an ohmmeter. If a no-output condition still exists, check the value of the capacitor with an in-circuit capacitor checker.

Low or Distorted Output. A defective diode is about the only component in the circuit that would cause a low output condition to exist. While a low output is also possible because the values of L1 or L2 may change and change the response curve, this possibility is rather remote. Do not neglect the possibility of either RI or R2 changing value sufficiently to affect the response,

If the output is distorted only at the lower frequencies, the defect is probably in one of the components of Z1. Check the value of L1. Check L1 for continuity and RI for proper value with an ohmmeter.

If the output is distorted only at the higher frequencies, series peaking circuit Z2 is probably defective. Check C2 with an in-circuit capacitor checker. Check L2 for continuity and R2 for proper vahre.

# BASIC VIDEO OETECTOR (SEMI CONDUCTOR)

## Application.

**The** basic video detector is used in semiconductor receivers of the superheterodyne type to provide a high gain video output.

#### Characteristics.

Uses either fixed or self-bias.

Is equivalent of a diode and one stage of transistor amplification.

Uses video peaking circuits to provide good high frequency responses.

# **Circuit Analysis.**

**General.** The operation of the basic video detector is identical to the operation of the AM diode detector previously discussed in Part A of this Handbook. The only difference lies in the use of the base-emitter junction of the transistor as a diode in place of a separate diode. Compensating circuits are added in the collector circuit to ensure better high frequency response. The reader should refer to the discussion of the Diode Detector, in Part A of this section of the Handbook, for proper background before preceding with the discussion of the semiconductor basic video detector.

**Circuit Operation. The** schematic of a typical transistor video detector using shunt peaking is shown in the following illustration.



Basic Video Detector (Semi Conductor)

The base of transistor Q1 is connected to the untuned secondary of i-f transformer T1, with the primary tuned by capacitor C. Resistors R2 and R3 from a base bias voltage divider from the negative supply to ground, with the voltage drop across R3 supplying the base bias to Q1 through the secondary winding L2 of TI. R3 is bypassed by C2 to prevent a degenerative voltage from being developed across R3 with the instantaneous bias swings, thus allowing voltage divider R2 and R3 to provide a steady forward bias to the base of Q1. Resistor RI is a conventional emitter swamping resistor used to stabilize the transistor against thermal changes and, Iikewise, is bypassed by Cl to prevent degeneration in the emitter circuit and negative feedback effects. Inductor L3 is a shunt peaking inductance with R4 supplying resistance to widen the response. L3 also acts as the detector output load resistor across which

the output voltage is developed and applied through coupling capacitor Ccc to the following stage, or direct to the CRT if sufficient drive exists.

When an input signal is applied to T1, the i-f frequency is selected by tuned circuit Ll and C, and this i-f together with any modulation component is inductively coupled through secondary L2 which is left untuned for a broad response, and the signal is applied to the base of Q1. The emitter-base junction of QI acts as a rectifier and instaneously changes the bias in accordance with the low frequency variations of the modulation envelope. Any remaining i-f is bypassed through capacitors Cl and C2 to ground and has no effect on circuit operation. As the audio envelope of the received signal changes the bias on Ql, the collector current is varied likewise, and the collector current fluctuates in accordance with the modulation. The audio frequency variations are bypassed across emitter resistor R1 by capacitor Cl so that only the long time temperature variations can produce a voltage change across RI. However, the flow of collector current through L3 and R4 produces a change of collector voltage on the collector side of the choke. A positive modulation swing causes a decrease of forward conduction and raises the instantaneous collector voltage. Likewise, a negative audio excursion causes an increased forward bias and conduction, and the collector voltage of Q1 reduces. Since only a small change in base current causes a large change in collector current, amplification of the detected signal is obtained in the collector circuit of O1 and appears as a larger output voltage across L3 and R4. By resonating L3 with the stray capacitance in the circuit, the normal drop off in amplitude of higher frequencies is compensated for and the high frequency range is extended. Resistor R4 keeps L3 loaded down so that the overall frequency response of the detector is broadened. As the output voltage is developed across L3 it also is applied through Ccc to the output. Where the output voltage is sufficient the CRT may be driven directly. Where the voltage is not sufficient, an additional voltage amplification driving amplifier stage is added to increase the overall drive, as required.

## Failure Analysis.

No Output. An open input transformer, an open base circuit, emitter circuit, or collector circuit, as

well as a defective transistor or open coupling capacitor can cause a no-output condition. Check the collector, base, and emitter bias with a high resistance voltmeter. Voltage at the collector indicates that L3 and R4 are not open, while emitter voltage indicates that RI is not open or shorted. Likewise, base bias indicates that voltage divider R2 and R3 is operating, and that secondary L2 or T1 has continuity. With these voltages obtained and no output, either winding LI of **T1** is open or shorted, or Ccc is open. Check C and CCC with an in-circuit capacitance checker, and also check the continuity of T1 primary LI with an ohmmeter. If base bias is zero R3 is shorted, also check C2 for capacity with an in-circuit capacitance checker. If the emitter voltage is also zero R1 is shorted cy Cl, however, the transistor will still function and produce an output which will vary with temperature. If there is no collector voltage, check the supply voltage to make certain it is not at fault, check the value of R4 with an ohmmeter and check L3 for continuity.

Low Output. High base bias, low collector voltage, or a defective transistor can cause a no-output condition. If bias voltage divider resistor R3 changes to a higher value of resistance, or if R2 becomes lower in value, the net effect is to make the total base bias higher, check these resistors with an ohmmeter. If R4 becomes higher in resistance, the collector voltage will also drop and reduce the output. Check R4 with an ohmmeter. If a high bias is measured across emitter reisitor RI, capacitor Cl is open, check Cl for value with an in-circuit capacitance checker. Do not neglect the possibility that the input tank controlled by capacitor C may be detuned from the desired i-f input frequency. If not shorted, tuning C will peak the response. If the response does not peak as C is tuned around the input frequency, check capacitor C for a short or open on a capacitance meter.

## PART 10-4. BALANCED

## **BALANCED DETECTORS**

# General.

Balanced detectors usually employ two tubes or transistors in a balanced circuit arrangement with two

inputs applied and with a single output. One input, usually the carrier or reference oscillator, is so balanced that no output is produces unless the second input is applied. The balanced detector circuit is practically identical to a balanced modulator, and both operate similarly, except that the inputs and outputs are reversed. There are as many balanced detector circuit arrangements as there are balanced modulator circuits. Usually each circuit has some advantage over another and each type is selected for its particular use and because of the availability and cost of the components. The simpler and more commonly used circuits such as the lattice type, ring type, balanced-bridge type, and basic diode type all employ diodes, whereas the more complicated types provide larger outputs, improved sensitivity, and lower noise, using triodes and pentagrid tubes. Each of these circuits will be explained in more detail later in this section of the Handbook. While the diode type of circuits may appear at first glance to act as conventional rectifiers, they act as non-linear impedance across which the inserted carrier is combined with the input signal to produce the proper audio beat output, and rectification noise is eliminated.

The balanced detector may be used to convert an r-f input to an i-f output, an i-f input to an audio output, or an audio input to an audio output. While the majority of circuits are used for single-sideband detection, the ring and lattice types are usually not used in receivers, but are particularly popular in multiplex telephone circuits where their bilateral characteristic makes them particularly desirable for this type of work. The basic balanced diode detector is frequently used in color TV receivers to obtain the hue and saturation components of the color signal.

# BASIC DIODE BALANCED DETECTOR (ELECTRON TUBE)

#### Application.

The basic diode type of balanced detector is frequently used in 'single-sideband and color television receivers.

#### Characteristics.

Has balanced inputs and outputs.

Requires a local (reference) oscillator input at a fixed frequency.

Oscillator signal is applied in-phase and input signal is applied in push-pull.

May use either electron tube or semiconductor diodes.

## Circuit Analysis.

General. The basic balanced diode detector is similar in appearance and operation to an FM or phase detector except that the input and output is always a balanced arrangement. The reference oscillator signal which usually simulates the carrier signal is applied inphase to both diodes (same polarity is supplied to each pair of anodes) and is balanced out in the output circuit. Thus, with no input signal there is no output. The input signal is applied in push-pull to the diodes and the in-phase component of the input signal adds to the reference oscillator signal and unbalances the detector at the difference frequency. In a similar manner, the out-of-phase components reduce the amplitude of the signal at the other diode. When the difference frequency is an audio frequency an audio output is produced.

**Circuit Oparation.** A typical balanced diode type of detector is shown in the following schematic. Transformer T1 is the push-pull input transformer. Oscillator transformer T2 is connected in-phase (same polarity) with both diodes VI and V2, and T3 is the output transformer. Capacitors C1 and C2 are r-f bypass capacitors connected across the primary of output transformer T3.



**Balanced Diode Detector** 

The reference oscillator (carrier) is applied to the center tap of T1 so that the anodes of both diodes are both of the same polarity (in-phase) as far as the oscillator signal is concerned. Thus, if no input signal is applied, the oscillator signal causes equal conduction in both diodes during the positive portion of its operating cycle.. Equrd currents are passed through the primary of output transformer T3 in opposite directions from the center tap to the cathode of the diodes. Hence, the induced voltages are of opposite polarity and cancel out so that no output voltage is induced into the secondary winding. As long as no input signal is applied, the oscillator signal will always automatically cancel in the secondary of T3.

When the sideband signal input is applied to Tl, one end of the secondary winding will be positive while the other end is negative, considering one halfcycle of operation. Thus, VI will normally conduct while V2 remains non-conducting. On the opposite half-cycle of operation, the anode of V1 will be negative while the anode of V2 is positive. Hence on this half-cycle V2 will conduct while V1 remains non-conducting. Since the reference oscillator signal is connected in-phase, on one half-cycle of input signal both the oscillator and input signal will add to increase conduction through V1, while the input signal opposes the oscillator signal through the other half of the winding so that the anode of V2 is at zero or at a slight negative potential (considering both to be of equal amplitude). Since the input signal and the carrier oscillator differ in frequency by the audio modulation frequency, they will beat against each other and produce the difference frequency in the output transformer. The sum frequency created by the beating of the two signals is a high radio frequency which is bypassed across the primary of T3 by either Cl or C2, so that only the difference frequency can pass through the primary and induce an audio output in the secondary of T3.

During the negative half cycle of oscillate signal, the in-phase comection of T2 will place a negative potential on the anodes of VI and V2 so that neither V1 nor V2 can conduct. Thus, in the absence of an input signal, again there is no output. When an input signal is applied, the in-phase component will place a negative potential on the anode of V1, while the outof-phase component will reduce the negative oscillator potential on the anode of V2 to zero; still no conduction will occur. Thus, during the negative portion of the oscillator signal, no output will occur.

The alternate pulses of current flowing through the primary of T3, when a diode is conducting, will induce a secondary voltage in T3 of the same frequency; any i-f or r-f component will be shunted around the primary winding through Cl or C2 so that only the detected audio appears in the output. Output transformer T3 may be replaced by resistors shunted by Cl and C2 and connected in series in some circuit variations. Operation is the same, with the capacitors being charged by the voltage drop across the resistors and, since they are connected in series, the output is the difference between the two voltages. When connected to an audio coupling capacitor this dc output varying at audio frequency rates will produce an audio output also. Whether the diodes operate alternately or simultaneously depends upon the phase and value of the signal applied to the anodes. With in-phase signals of the same polarity and amplitude both diodes operate, and equal and opposite output voltages cancel out in the secondary of T3 to produce no output (assuming perfect balance). With out-of-phase signals (push-pull input), one anode will be positive and conduct while the other is negative, and remain back-biased and non-conducting. Whether the diodes conduct on alternate half-cycles depends upon whether the input signal is stronger than the reference oscillator. The output may be push-pull or single-ended as desired, without affecting operating.

## Failure Analysis,

No Output. Loss of reference oscillator signal, no input signal, a defective output transformer, or defective diodes can produce a loss of output. Check for the presence of an output from T2. If an output exists, check T1 similarly for a signal input. If there is no output from T2, check the primary and secondary windings for continuity. If continuity exists in the windings of T2, the oscillator circuit is probably defective. If an output exists at T2 but there is no signal input, check the primary and secondary windings of T1 for continuity. If continuity exists, the r-f or i-f input circuits are probably at fault. If an input exists at T1 and a reference oscillator signal exists at T2, but there is still no output, both diodes VI and V2 may be defective. In addition, check Cl and C2 for value and for a shorted capacitor, and check T3 primary and secondary for continuity. If continuity exists in T3 and neither Cl nor C2 is shorted, there is still a possibility that T3 primary or secondary may

be shorted. Measure the resistance of the windings of T3; a resistance of a few ohms or less indicates a probable short-circuited winding between the primary and secondary. The possibility of a short in T] or T2 also exists, but since these transformers usually have a very low resistance, it is usually difficult to determine if they are defective by resistance readings alone. Because of the few parts in this circuit, a quick resistance check of all parts will usually reveal the defective item except for the transformers which a voltage check will determine more clearly. If the shunting resistance of T3 on capacitors C1 and C2 is low, it may not be possible to make a capacitance check without first disconnecting one terminal of the capacitors from the circuit.

Low Output. A low output may be caused by defective diodes, partially shorted transformer windings on T1, T2, or T3, or leaky capacitors Cl and C2. The output of the reference oscillator should also be checked for normal amplitude. If the amplitude is normal, diodes VI and V2 are probably defective. Check the values of Cl and C2 and check them also for excessive leakage. If the low output persists, check transformers Tl, T2, and T3 for partial shorts (shorted turns), shorts, and leakage to ground. To do this, it will be necessary to make separate dc resistance checks of the windings, and to check the winding inductance on an inductance bridge. Also check leakage to ground and transformation ratio (turns ratio). Since precise measurements are necessary and require laboratory-type equipment, it is doubtful that all these tests can be performed aboard ship. Do not neglect the possibility that an excessively low input and oscillator signal can cause a low output. Usually the oscillator output is kept at about ten times the input signal to create a strong beat signal and reduce the actual ratification of the input signal to such a small value that ratification distortion effects are eliminated.

**Distortion.** Since faithful reproduction in a balanced detector depends upon the operation of the reference (carrier) oscillator at the exact frequency of the suppressed carrier, and that distortion components are not introduced by overdrive at the transmitter, it is often erroneously assumed that the detector is at fault, whereas adjustment of the transmitter or receiver is actually required. When distortion is encountered carefully tune the receiver to the

proper sideband as shown by the strongest S-meter reading, and adjust the reference oscillator *fine* tuning for the clearest signal. At the same time, adjust the r-f gain control for the clearest signal and the audio gain for proper volume. Place the upper-lower sideband switch in the position which provides the most intelligible **signal**. If distortion exists at the clearest tuning point, check by tuning in other sideband signals. If they are undistorted, the transmitter is being driven too hard. If all signals are distorted, the tubes are probably defective. Check each part separately until the distortion is located.

# **BASIC TRANSISTOR BALANCED DETECTOR**

# Application.

The basic transistor type of balanced detector is frequently used .in single-sideband and color TV receivers.

#### Characteristics\_

Has balanced inputs and outputs.

Requires a local (reference) oscillator input together with an r-f sideband input.

Oscillator signal is applied in-phase, and the input signal is applied in push-pull.

Uses fixed bias but may also use self bias.

## Circuit Analysis.

General. The basic transistor detector is similar in appearance and operation to an FM or phase detector, except that the input and output is always a balanced arrangement and transistors are used instead of diodes. The reference oscillator signal which usually simulates the carrier signal is applied in-phase to both transistors and is balanced out in the push-pull output circuit. Hence, with no input signal there is no output. The sideband input signal is applied in pushpull to the transistors, and the in-phase component of the input signal adds to the reference oscillator signal and unbalances the detector at the difference frequency. In a similar manner, the out-of-phase components reduce the amplitude of the signal at the other transistor. When the difference frequency is an audio output frequency, an audio output is produces.

**Circuit Operation.** A typical balanced transistor type of detector is shown in the following schematic.



**Transistor Balanced Detector** 

Transformer T1 is the push-pull r-f input transformer. Oscillator transformer T2 is connected in parallel with the bases of both transistors Q1 and Q2, isolated for dc through coupling capacitors C 1 and C6. The secondary winding of T2 is tuned to resonance by C5. Resistors RI and R2 form the base voltage bias divider for Q1, while R5 and R6 are the base bias dividers for Q2. Hence a forward bias is applied to the transistors. Resistors R3 and R4 are emitter swamping resistors bypassed by C3 and C4 to provide temperature compensation for the transistors, and prevent possibility of thermal runaway. (See the introduction to the Amplifier Section of this Handbook for a complete discussion of common-emitter bias and stabilization.)

The reference oscillator (carrier) is applied to the center tap of T1 so that the bases of both transistors are fed in-phase (of the same polarity) as far as the oscillator signal is concerned. Thus if no input signal

is applied, the oscillator signal causes equal conduction in both transistors during the positive portion of the operating cycle. Since equal collector currents flow in opposite directions through the primary of output transformer T3, no voltage is induced in the secondary and there is no output developed across the secondary of T3. As Iond as no r-f input signal is applied, the oscillator signal will always cancel out automatically in the secondary of T3. Capacitors C2 and C7 also bypass to ground any r-f components in the collector circuit so that no oscillator output can be produced if no input signal is applied. Likewise, with only an r-f input applied but no reference oscillator signal the collector is bypassed to ground so that no output can be produced by the sideband r-f input alone.

When the sideband input signal is applied to T1, one end of the secondary winding will be positive while the other end is negative, considering one half cycle of operation. Thus, Q1 will normally conduct heavily while Q2 remains lightly conducting. On the opposite half cycle of operation, the base of Q1 will conduct lightly while Q2 conducts heavily. Since the reference oscillator signal is connected in-phase, on one half cycle of input signal both the oscillator and sideband input signal will add to increase conduction through Q1, while the input signal opposes the oscillator signal through the other half of the winding, so that the base of Q2 is at zero bias or at a slight positive potential (considering both of equal amplitude). Since the input signal and the difference frequency can pass through the primary winding of T3 and induce an audio output in the secondary of T3.

During the positive half cycle of oscillator input signal, the in-phase connection of T2 will place a positive potential on the base of Q1 and Q2 so that neither Q1 nor Q2 will conduct. Thus, in the absence of an input signal, again there is no output. When an input signal is applied, the in-phase components will place a positive reverse bias potential on the base of Q1, while the out-of-phase component will reduce the reverse bias but Q2 will not conduct, since the oscillator amplitude is greater than the sideband signal. Thus during the positive half cycle of the oscillator signal no output will occur.

The alternate pulses of current flowing through the primary of T3, when the transistor is conducting, will induce a secondary voltage in T3 of the same

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frequency, and any i-f or r-f component in the collector circuit will be shunted to ground, so that only the detected audio appears in the output. Output transformer T3 may be replaced by resistors shunted by C2 and C7 and connected in series in some circuit variations. Operation is the same in this instance, with the capacitors being charged by the voltage drop across the resistors, and, since they are connected in series, the output is the difference between the two voltages. When connected to an audio coupling capacitor this dc output varying at audio frequency rates will produce an audio output also. Whether or not the transistors operate alternately or simultaneously depends on the phase and value of the signal applied to the bases. With in-phase signals of of same polarity and amplitude, both transistors operate, and equal and opposite output voltages cancel out in the secondary of T3 to produce no output (considering perfect balance). With out-ofphase signals (push-pull input) one base will be negative and conduct while the other is positive and remains backbiased and non-conducting. Whether or not the transistors conduct on alternate half cycles also depends upon whether or not the input signal is stronger than the reference oscillator. The output may be push-pull or single-ended as desired, without affecting operation.

## Failure Analysis.

No Output. Loss of reference oscillator signal, no input signal, a defective output transformer, or defective transistors can produce a loss of output. Check for the presence of an output from T2. If an output exists check T1, similarly, for a signal input. If there is no output from T2 check the primary and secondary windings for continuity. If continuity exists in the windings of T2, the oscillator circuit is probably defective. If no output exists at T2 and there is no signal input, check the primary and secondary windings of T] for continuity. If continuity exists, the r-f or i-f input circuits are probably at fault. If an input exists at T1 and a reference oscillator signal exists at T2, but there still is no output, both transistors are probably defective. Also check C2 and C7 for value and for a short. Check T3 primary and secondary for continuity. If continuity exists in T3 and neither C2 nor C7 is shorted there is still a possibility that T3 primary or secondary may be shorted.

Measure the resistance of the windings of T3; a resistance of a few' ohms or less indicates a probable short-circuited winding. The possibility of a short in T1 or T2 also exists. Because of the few parts in this circuit a quick resistance check of all parts will usually reveal the defective item: If the shunting resistance of T3 on capacitors C7 and C2 is low, it may not be possible to make a capacitance check without first disconnecting one terminal of the capacitors from the circuit.

Low Output. A low output may be caused by defective transistors, partially shorted windings on T1, T2, or T3, or by leaky capacitors C2 and C7. The output of the reference oscillator should also be checked for normal amplitude. If normal, transistors Q1 and Q2 may be at fault. Check the values of C2 and C7 with a capacitance checker, and also check them for excessive leakage. If the low output persists, check transformers T1, and T2, and T3 for partial shorts (shorted turns), shorts and leakage to ground. To do this, it will be necessary to make separate dc resistance checks of the windings with an ohmmeter; check the winding inductance on an inductance bridge; and also check leakage to ground and transformation ratio (turns ratio). Since precise measurements are necessary and require laboratory type of equipment, it is doubtful that all these tests may be performed aboard ship. Do not neglect the possibility that excessively low sideband input and r-f oscillator signals can cause a low output. Usually the oscillator output is kept at about ten times the input signal to create a strong beat signal, and reduce the actual rectification of the input signal to such a small value that rectification distortion effects are eliminated.

**Distortion.** Since faithful reproduction in a balance detector depends upon the reference oscillator operating at the exact frequency of the suppressed carrier, and also that distortion components are not introduced by overdrive at the transmitter, it is often erroneously assumed that the detector is at fault when adjustment of the transmitter or receiver are what is actually required. When distortion is encountered, carefully tune the receiver to the proper sideband as shown by the strongest "S" meter reading and adjust the reference oscillator fine tuning control (C4) for clearest signal, at the same time adjust the r-f gain control for clearest signal, and the audio gain for proper volume. Place thee upper-lower sideband

switch in the position which provides the most intelligible signal, If distortion exists at the clearest tuning point, check by tuning in other sideband signals. If they are undistorted, the transmitter is being driven too hard. If all signals are distorted, the transistors may be defective. Check each part separately until the distortion is located.

# LATTICE TYPE DIODE BALANCED DETECTOR (SEMICONDUCTOR)

#### Application.

The lattice-type diode detector is used for single sideband reception, and for double sideband suppressed carrier detection, particularly in carrier telephone multiplex circuits.

#### Characteristics.

May use either electron tubes or crystal diodes.

Has push-pull input and balanced output.

Requires reference oscillator input, and signal input.

Uses only transformers and diodes.

# **Circuit Analysis.**

General. The lattice-type detector is sometimes called a shunt-quad demodulator. The output of a reference oscillator, which simulates the carrier signal, is applied in series with the center taps of the input and output transformers to provide a signal of the same polarity to each pair of diodes. When no sideband input is applied, this in-phase signal causes two of the diodes to conduct simultaneously and produce a circulating current traveling in opposite directions through one-half of the input and output transformer primaries. The magnetic flux induced in each half of the same winding in each transformer opposes the other, and the voltage induced in their secondaries cancel, so that no output is produced from either transformer because of the carrier signal. Thus, with no input signal applied, there is no output from the circuit. When an input signal is applied, it alternately adds to and subtracts from the oscillator signal, thus unbalancing the circuit. Each diode conducts alternately on opposite half cycles, producing an audio output in the secondary of the output transformer.

**Circuit Operation.** The schematic of a typical lattice-type balanced diode detector is shown in the accompanying illustration.



Lattice-Type Diode Balanced Detector

Transformer Tl is the i-for subcarrier input transformer, while T2 is the reference (carrier) oscillator transformer which is connected in-phase between T1 and T3. T3 is the audio output transformer. Diodes V1 and V3 form one group of rectifiers and diodes V2 and V4 form the other set of rectifiers. The rectifiers conduct simultaneously for in-phase signrds and alternately for push-pull signals.

Consider first the condition where no input signal is applied except the reference oscillator signal. Assuming an instantaneous polarity such that the center tap of T3 is positive and that of T1 is negative, the plates of V2 and V4 have a positive voltage applied and both diodes are forward-biased and conduct. Electron flow is from the negative termind of T2 through the upper half of T1 to the cathode and plate

of V2, back through the top half of the primary winding of T3 to the positive terminai of T2. Similarly, current flows through the bottom half of the winding of T1 from the negative terminal of T2 to the cathode and plate of V4, and back through the bottom half of the primary of T3 (in the opposite direction) to the positive terminal of T2. With equal voltages applied to the plates of the diodes equal currents flow. Therefore, the flux generated by the flow of current through the top half of T] is opposite to the flux created by current flow through the bottom half of Tl, and no output is induced in the primary. In a similar manner, the opposing plate current flow through the upper and lower halves of T3 produces opposite and canceling magnetic fields around the primary of T3 so there is no output from the secondary. Thus, the effect of an output from the reference oscillator is cancelled in both the input and output transformers because the circuit is completely balanced. Hence, with no input signal there will be no output, even though the reference oscillator voltage is applied. During the first half cycle of operation, the plates of diodes V1 and V3 are back-biased and do not conduct. On the opposite half-cycle, the polarity of the reference oscillator is such that the plates of diodes V2 and V4 are back-biased and do not conduct, while diodes V1 and V3 are forward-biased and conduct. With still no input and the r-f oscillator input of the opposite polarity, current flow is in the opposite direction through the bottom half of T3 and the top half of T2 for diode Vl, and through the upper half of T3 and the lower half of T1 for diode V3. Although current flows in the opposite direction to that for V2 and V4, the current flow through the upper and lower halves of both transformers is still in opposition. Hence, once again opposing fluxes are created in the transformer primary which cancel at the output so that no signal output is produced at the primary of T1 or the secondary of T3. Thus, regardless of oscillator polarity, there is never any output when only the in-phase signal from the reference oscillator is applied.

Since the reference oscillator amplitude is stronger than that of the incoming signal, the polarity of the reference oscillator determines which set of diodes conduct. At the instant diodes V2 and V4 are conducting, the push-pull input signrd connection will supply an in-phase signal to V2 and an out-of-phase signal to V4. Thus, conduction through diode V2 will be increased while the current through V4 is decreased. The reduced current through one half of the primary winding of output transformer T3 and the increased current through the other half of the winding add to produce a single polarity output in the secondary.

On the opposite half cycle of the reference oscillator signal, the plates of V1 and V3 will be driven positive and conduct while V2 and V4 are backbiased. Since the reference oscillator is almost the same frequency (except for the audio difference signal) as the input sideband signal, the polarity of T1 will also reverse and an in-phase signal will be sup plied to V3 and an out-of-phase signal to V1. Thus, conduction through diode V1 will be decreased while that through V3 will be increased. The reduced current through one half of the primary winding of output transformer T3 and the increased current through the other half of the winding add to produce a single polarity output in the secondary. This time, the polarity is opposite to that produced by V2 and V4 so that the negative half of the audio cycle is produced.

When the sideband input signal is mixed with the reference oscillator in the diode, sum and difference beat frequencies are produced. The high inductive reactance and leakage capacitance between turns of audio output transformer T3 effectively bypass the sum (high frequency) signal so that it does not appear in the output. Meanwhile, the audio frequency (difference) signal produces a voltage drop across the primary of T3 and induces a voltage into the secondary. This is the desired audio output voltage.

When this type of detector is used in multiplex telephony, the sideband input beating against the audio subcarrier also produces sum and difference frequencies. However, the sum frequency is still a high audio frequency (15 to 20 kHz or higher) and does not appear in the output because its amplitude is very low and it is inaudible. Thus, only the desired low frequency audio (difference) signals are produced.

#### Failure Analysis.

**No Output.If** there is no reference oscillator signal, or if transformers T1, T2, or T3 are defective, or the diodes are defective, no output will be produced. Likewise, if there is an oscillator signal but no input signal, no output will be obtained, Check for input and output signals. If an oscillator signal appears on the primary of T2 but not on the secondary, T2 is open or shorted. Similarly, if there is an input on the primary of T1 but not on the secondary, T1 is open or shorted. If there is an input signal and a reference signal present but there is no output signal, either the diodes, or transformer T3 is defective. Note that it is necessary for all diodes to be defective to prevent an output, since each pair of diodes controls only one hrdf of the cycle. Usually a quick resistance analysis will locate the open or shorted component except for the transformers, in which case a voltage check should be made.

Low Output. With a normal input signrd and a normal oscillator signal, a low output can only be caused by low diode emission or by partially shorted transformers. Check the transformers and diodes. In this instance it is possible for only two of the diodes to be defective.

**Distorted Output.** Defective diodes, a low oscillator output, shorted transformer turns, or excessive leakage to ground or the core can produce distortion. It is also important that the oscillator frequency be correctly tuned. If an adjustment of the oscillator tuning does not improve the condition, the diodes or transformers are defective. There also remains the possibility that the transmitter is being overdriven and causing distortion. Try receiving other signals and if the distortion clears up the transmitter is being overdriven and causing distortion.

# RING-TYPE DIODE DETECTOR (ELECTRON TUBE)

## Application.

The ring-type diode detector is used for doubleside-band suppressed carrier and single-sideband detection, particularly in multiplex telephone carrier equipment.

# Characteristics.

May use either tube or crystal diodes.

Has a push-pull input and a balanced output.

Requires both a reference oscillator input, and a signal input.

Uses only transformers and diodes.

## **Circuit Analysis.**

**General.** The ring-type detector is basically a lattice-type detector which resembles a bridge circuit.

# ORIGINAL

A simulated carrier signal from a reference oscillator is applied between the center taps of the input and output transformers to provide an in-phase signal to each pair of diodes. With equal conduction between opposite diodes and equal but, opposite-direction, currents flowing in the two halves of the same transformer, the fields cancel, and no output is obtained as long as only the simulated carrier signal is applied, When an input signal is applied simultaneously with the simulated carrier, it alternately adds to, and subtracts from, the oscillator signal. Thus, each diode conducts alternately on opposite half-cycles, and an audio output is produced.

**Circuit Operation.** The schematic of a typical ringtype detector is shown in the accompanying illustration.



**Ring-Type Detector** 

Transformer TI is the r-f of subcarrier input transformer, and T2 is the reference (carrier) oscillator transformer which is connected in-phase between T1 and T3. Transformer T3 is the audio output transformer. Diodes VI and V3 form one pair of rectifiers, and diodes V2 and V4 form the other pair. The diodes conduct simultaneously for in-phase signals and alternately for push-pull signals.

Consider first the condition where no input signal is applied except the reference oscillator signal. Also, assume that the instantaneous polarity is such that the center tap of T3 is positive, while that of T1 is negative. Therefore, the plates of V2 and V4 have a positive voltage applied, and the diodes conduct. Electron flow is from the negative terminal of T2 through the lower half of T1 and cathode to plate of diode V4, and back through the lower half of T3 primary winding to the positive terminal of T2. Similarly, current flows through the top half of the secondary winding of T1 and cathode to plate of V2. and back through the top half of the primary winding of T3 to the positive terminal of T2. With equal plate voltages applied to the diodes, equal currents flow through the transformers. Since the current flows in opposite directions through each half of the transformer winding, equal and opposite fields are generated around the windings. Because the opposing fields cancel each other, no oscillator signal is produced in the primary winding of T1 or in the secondary winding of T3. Thus, the possibility of an output resulting from the application of the reference oscillator is eliminated because the circuit is completely balanced. Hence, with no input signal, there will be no output, even though the reference oscillator voltage is applied. During the first half-cycle of operation, the plates of diodes V1 and V3 have a negative potential applied and do not conduct. On the opposite half-cycle, the polarity of the reference oscillator changes so that the plates of diodes V2 and V4 are supplied with a negative voltage and do not conduct, while the plates of diodes V1 and V3 are supplied with a positive voltage and do conduct. This time, current flow through the circuit is in the opposite direction through the top half of T3 and cathode to plate of V3, back through the lower half of T1 to the positive terminal of T2. For diode V1, current flow is through the top half of T1 and the lower half of T3. Although current flows in the opposite direction to that for V2 and V4, the current flowing through the upper and lower halves of each transformer is still in opposition. Hence, once again opposing fields are created around the windings and cancel, so that no signal output is produced in the primary of T1 or the secondary of T3. Thus, regardless of the oscillator polarity there is never any

output when only in-phase signals from the reference oscillator are applied.

Since the reference oscillator amplitude is stronger than that of the incoming sideband signals, the polarity of the reference oscillator on the diodes controls conduction. At the instant that diodes V2 and V4 are conducting, assume that the push-pull input signal supplies an in-phase signal to V4 and an out-ofphase signal to V2. Thus, conduction through diode V4 is increased, while the current through V2 is decreased. The increased current through one-half of the primary winding of output transformer T3, and the reduced current through the other half of the winding produce aiding fields around the transformer, and induce an **output** voltage in the secondary winding.

During the opposite half-cycle of reference oscillator signal, the plates of V1 and V3 are driven positive and conduct, while those of V2 and V4 are supplied with a negative plate voltage and do not conduct. Since the reference oscillator frequency is almost the same as the sideband signal (except for the audio difference signal), the polarity of T 1 input also reverses. An in-phase signal is now applied to V1, and an out-of-phase signal to V3. The reduced current through one half of the primary winding of output transformer T3, and the increased current through the other half of the winding produce aiding fields around the transformer, which induce an output voltage in the secondary. This time, the output polarity is opposite to that produced by V2 and V4 because of the change in the direction of current flow, and the negative half of the audio cycle is produced.

When the sideband input signal is mixed with the reference oscillator in the diode, sum and difference (beat) frequencies are produced. The high inductive — reactance and leakage capacitance between turns of audio output transformer T3 effectively bypasses the high frequency (sum) signal so that it does not appear in the output. Meanwhile, the audio frequency (difference) signal produces a voltage drop across the primary of T3 and induces a voltage into the secondary. This is the desired detected audio voltage.

When this type of detector is used in multiplex telephony, the sideband input beating against the audio subcarrier also produces sum and difference frequencies. However, the sum frequency is still a

very high audio frequency (15 to 20 kHz or higher) and does not appear in the output because its amplitude is low and it is inaudible. Thus, only the desired low frequency audio (difference) signals are produced.

### Failure Analysis.

No Output. If there is no reference oscillator signal, or if transformers T1, T2, or T3 are defective, or the diodes (V1, V2, V3 and V4) are defective, no output will be produced. Likewise, if there is an oscillator signal but no input signal, no output will be obtained. Check for the presence of input and output signals. If an oscillator signal appears on the primary of T2 but not on the secondary, T2 is either open or shorted. Check the transformer resistance and continuity. Similarly, if there is an input on the primary of T1 but not on the secondary, check the primary and secondary resistance and continuity of T1. If there is an input signal and a reference signal present, but there is no output signal, the diodes are probably defective. Also check output transformer T3 for continuity and resistance. Note that is is necessary for all diodes to be defective to prevent an output, since each pair of diodes only controls one half of the cycle. Usually a quick resistance analysis will locate" the open or short-circuited component.

Low Output. With a normal input signal and normal oscillator signal, a low output can only be caused by low diode emission, or partially shorted or leaky transformers. Check the transformers for the proper winding resistance, and check all diodes. It is rdso advisable to check the input and reference oscillator signals on an oscilloscope for peak amplitude. Usually, the oscillator is about ten times the strenght of the input signal. If the input signal is too small in amplitude and cannot be increased by adjustment of the receiver r-f gain control, the receiver circuits are probably at fault. If the reference oscillator output is low, check the oscillator for possible trouble such as low plate voltage, high bias, or defective parts.

**Distortad Output.** Defective diodes, a low oscillator output, too strong a sideband input signal, shorted transformer turns, or excessive leakage to ground or to the core can produce distortion. It is also important that the oscillator frequency be correct. If an adjustment of the oscillator tuning does not improve the signal, try reducing the setting of the r-f gain control. If the distortion persists, the diodes, or the transformers are probably at fault. The possibility also remains that the transmitter is being overdrive. Try receiving other signals; if the distortion clears up, the transmitter is at fault.

# BALANCED BRIDGE DETECTOR (ELECTRON TUBE)

### Application.

The balanced bridge detector is used for doublesideband suppressed carrier and single sideband detection particularly in multiplex telephone carrier equipment.

## Characteristics.

May use either electron tube or crystal diodes.

Has a balanced input and a balanced output.

Requires both a reference oscillator input and a signal input to produce an output.

Uses only transformers and diodes.

#### Circuit Analysis.

General. A simulated carrier signal from a reference oscillator is applied between the midpoints of the balanced bridge rectifier. One one half cycle of r-f carrier operation the bridge diodes are back-biased, and the brdanced bridge is effectively opened so that there is no path for the r-f carrier through the output transformer. During the next half cycle of carrier signal the bridge diodes are forward-biased, and effectively shunt the carrier signal around the output transformer. Thus, in the absence of a molulated input signal, no output can occur. When an input signal is applied together with the simulated carrier, it alternately adds to and subtracts from the oscillator signal, and the bridge is unbalanced. Consequently, each diode conducts alternately on opposite half cycles and current flows through the output transformer first in one direction and then in the opposite direction, and an audio output is produced.

**Circuit Oparation.** The schematic of a typical balanced bridge type detector is shown in the accompanying illustration.

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**Baianced-Bridge Detector** 

As shown in the schematic, T1 is the i-f input transformer (the line input transformer for telephone carrier equipment). T3 is the audio output transformer and T2 is the simulated r-f carrier (oscillator) transformer. Four identical tube diodes are used, with VI and V4 conducting simultaneously as one set of rectifiers, and V2 and V3 as the other set of rectifiers.

Let us first consider operation of the r-f carrier oscillator with no input signal applied to T1. Considering the half cycle of operation where a positive potential is applied to point A of the bridge and a negative potential to point C of the bridge it is evident that all four diodes are back-biased and will not conduct. Therefore, the bridge is effectively open and there is no output. During the next half of the oscillator cycle, point A is made negative and point C positive. Therefore all diodes are forward biased and conduct, effectively shunting both T1 and T3, and again there is no output. For these two conditions the bridge is balanced, and with no sideband input signal present on T1 there can be no output from T3.

When a signal appears on the secondary of T1, the bridge is unbalanced and two of the diodes are forward-biased while the other two diodes remain reverse biased and do not conduct. Assume that the i-f input signal produces a positive voltage on the top

of T1 secondary and a negative voltage at the bottom. Diode V1 thus has a positive voltage applied to the anode from the input signal, and when the simulated oscillator signal is negative at point A, the cathode of V1 is also negative and V1 conducts. At the same time a negative input signal is applied to the cathode of V4, while a positive oscillator voltage is applied to the anode, and V4, likewise, conducts. During this half cycle of operation V3 has a negative voltage applied to the cathode from the oscillator at point A, but the plate has a larger negative voltage applied from the input signal. Hence, V3 does not conduct. In a similar manner, V2 has a positive oscillator voltage applied to the anode and a larger positive signal voltage applied to the cathode. Hence, V2 also does not conduct.

When the input signal changes polarity, diodes V2 and V3 are forward-biased and conduct. However, diodes V1 and V4 are now back-biased and cease to conduct, assuming that the carrier (oscillator) polarity has not changed. When the bridge is unbalanced and either set of diodes conduct, a path for the flow of current exists through the conducting diodes and the secondary of T1, in series with the oscillator secondary winding of T2. Depending upon which set of diodes conduct, the flow is first in one direction and then in the opposite direction during the next half cycle. The current flow through these paths is controlled by the amplitude of the signals applied and the respective reactance offered by the transformer windings. At the same time, the changing sideband input frequencies and the constant carrier (oscillator) signal are mixed, and sum and difference beat frequencies are produced. At any one instant, the difference frequency is the audio frequency, while the sum frequency is a higher radio frequency. Since transformer T3 is an audio transformer, it offers a high reactance (impedance) to the flow of radio frequency currents, and because of its appreciable capacity between turns offers a low (shunting) leakage reactance. Therefore, the r-f signals are effectively bypassed around T3 so there is no output for these frequencies. On the other hand, the audio beat signal current flows through the primary of T3 and induces an audio output voltage in the secondary.

The following waveform illustration shows pictorially how the bridge detector develops the audio output. The r-f carrier (oscillator) input is shown as a Т

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constant amplitude signal consisting of alternate positive and negative half cycles. It is assumed that the sideband input signal consists of an r-f signal one Hz more than the carrier frequency. Thus if we assume the oscillator operating at one million Hz, the sideband input signal occurs at a frequency of one million and one Hz and is the upper sideband (assuming signal sideband operation). When these two frequencies flow through the diodes they are mixed, and beat together producing a two million and one Hz sum frequency and a one Hz audio difference frequency.



**Detector Waveforms** 

The one Hz audio frequency produces one positive and one negative half Hz; during this interval one million positive oscillator half Hz and one million negative oscillator half Hz occur and are shown in the illustration as seven half Hz for convenience and ease of drawing. Thus we see that V1 and V4 conduct during the positive input excursion of the single audio cycle while V2 and V3 conduct during its negative excursion. During each audio conduction period the amplitude first increases and then decreases to produce the audio sine wave originally introduced in the modulation process.

Idealized waveforms were used in the illustration and discussion of circuit operation. In actual operation the complex waveforms of speech (or music) are reproduced with a minimum of distortion. In the bridge detector the sideband signal is the larger and controlling signal, whereas in the bridge modulator the audio is the controlling signal and the oscillator signal is kept larger in amplitude to minimize distortion.

#### Failure Analysis.

**No Output. A no-output** condition can result from lack of sideband input or loss of carrier (oscillator) input, as well as from defective diodes or transformers. An open transformer primary or seconary winding on Tl, T2, or T3 can prevent an output, Check the primary and secondary windings for continuity with an ohmmeter. There is also the possibility of a shorted winding which can be located by checking the primary and secondary windings with an oscilloscope. While a defective diode may cause loss of one half of the signal, it is necessary for all four diodes to be defective to prevent any output.

Low Output. Low oscillator or input signals, or low emission in the diodes can produce a reduced output. Check the oscillator and input signal amplitude on an oscilloscope (use an r-f probe for high frequency signals). There is also the possibility that a partially shorted winding can reduce the signal. Use an oscilloscope and check that the waveform and amplitude in the secondary of each transformer is equal to or greater than the primary signal.

High or Distorted Output. A higher than normal output is rather unlikely and would be a direct result of greater than normal input and oscillator signal amplitudes. Check the preceding circuits for improper inputs and plate voltages. Distortion will usually occur because of higher or lower than normal inputs or outputs (carrier and sideband signals). Normally the oscillator and sideband signals are of different amplitudes to produce a good beat signal. When the signal amplitudes become equal, or have less than a 3 to 1 ratio, over-modulation distortion occurs. There is also the possibility of spurious beat signals causing unwanted signals or noise. Usually observation with an oscilloscope will indicate if any unwanted signals are present. If present, it will be necessary to determine the source, which is usually external (strong local signals) and either trap out the unwanted signal or minimize the pickup with either a low pass or a high pass band filter.

# TRIO DE, PUSH-PULL OUTPUT BALANCED DETECTOR (ELECTRON TUBE)

#### Application.

The triode push-pull output type of balanced detector is commonly employed in single sideband

receivers used in fixed-station transoceanic telephony rather than in modern communications receivers, which generally use the product type detector.

### Characteristics.

Uses a triode tube for increased gain and better brdancing.

Has a balanced input and a balanced output.

Requires a reference oscillator input and a sideband input to produce an audio output.

Can use either fixed or self bias.

# **Circuit Analysis.**

General. The simulated carrier (r-f oscillator) signal is applied to the triode grids in parallel, and in the absence of a sideband input cancels out in the output transformer. Thus with no sideband input and only an oscillator input there is no output. When a sideband signal is applied to the grids it alternately adds in series with the simulated carrier (oscillator) signal on the in-phase half cycles, and causes the plate current of one tube to increase while that of the other tube decreases. The carrier and input signals beat together. The difference frequency appears in the primary of the output transformer producing an audio output, while the sum frequency is bypassed to ground. When the polarity of the input signal changes during the next half cycle, the polarity of the oulput changes and the other half cycle of the audio output is produced. The amplitude of the oscillator input is made adjustable to obtain a minimum of distortion.

Circuit **Operation.** The schematic of a typical triode push-pull output type of balanced detector is shown in the accompanying illustration.



#### **Triocle Push-Pull Output Balanced Detector**

The i-f input transformer, T1, is center tapped to provide a push-pull sideband input to the grids of V] and V2. The center tap is returned to the variable arm of potentiometer R1, which is connected across the secondary of oscillator transformer T2. Variable capacitor Cl is used to tune the secondary of T2 to resonance. Potentiometer R1 provides the proper amplitude of the oscillator signal applied to VI and V2. To provide a good beat frequency ratio, the oscillator amplitude is **usually** adjusted for about ten times the input amplitude from the i-f stage. Fixed

bias is applied from a separate negative supply through decoupling resistor R2, by-passed by C2 to ground. The rotor of Cl is placed at r-f ground potential by C2. The cathodes of VI and V2 are grounded. The plates of VI and V2 are connected in push-pull through audio output transformer T3, with the plate supply connected to the center tap on the transformer. Capacitors C3 and C4 are r-f bypass capacitors which allow only the audio signal to flow through T3 primary.

When the carrier (oscillator) output alone is applied to VI and V2 grids, it is effectively applied in parallel by connecting the secondary of T2 between both grids and ground. Thus when VI grid is driven positive a current flows from the cathode of V1 to the plate and through T3 to the center tap and power supply. Simultaneously, the grid of V2 is also driven positive, and an equal flow of current occurs from the cathode of V2 to T3 center tap and the supply in the direction opposite that of V1. Both currents of equal magnitude flowing in opposite directions through the primary of T3 cause opposing fields which cancel, so that no output is produced from the secondary winding of T3. Hence, no output is produced when the oscillator signal alone is applied to VI and V2. When the sideband input is applied to **T1** primary it induces equal and opposite voltages in the center-tapped secondary so that the grid of VI is driven positive, while the grid of V2 is driven negative. These two secondary voltages add algebraically to the oscillator signal from T2. If at any instant the oscillator signal is operating on the positive half cycle, the voltage at the grid of V1 is the sum of the oscillator and sideband signal and causes the plate current of V1 to increase. At the same time the grid of V2 is driven negative and subtracts from the oscillator signal. Since the oscillator signal is adjusted for about ten times the amplitude of the input signal, the plate current of V2 is reduced. The magnetic field caused by the decrease of V2 conduction, is the same field polarity as that caused by the increase of V1 conduction. Thus, the two fields add to induce an output voltage in the secondary of T3.

The induced secondary voltage is an audio frequency since the oscillator and sideband signals beat together in the plate circuit, and **produce** sum and difference frequencies. The sum frequencies are bypassed to ground by C3 and C4 since they are at a higher radio frequency than the oscillator. While the difference frequency is at a low (audio) frequency and is offered a low reactance path through the primary of T3. Thus, only the audio component of the input signal is passed through T3 to produce the detected or demodulated audio output of the stage.

On the opposite half of the input signal cycle the opposite condition occurs. That is, VI is driven negative, while V2 is driven positive, and the negative half of the audio output cycle is developed in the primary of T3, and induced into the secondary as the audio output, When R1 is adjusted for the proper amplitude, the oscillator push-push input is balanced properly to produce a strong audio beat in the plate circuit, providing a minimum of noise and a relatively undistorted audio output signal.

## Failure Analysis.

No Output. I\_Qss of sideband input signal or loss of the oscillator (simulated carrier) signal when the opposite signal is present (or loss of both signals) will prevent any output. A defective tube or loss of plate voltage, open or shorted transformers T1, T2, or T3, too high a bias, or defective bypass capacitors C2, C3, or C4 can also prevent an output. With the plate voltage off, check the transformer primary and secondary windings with an ohmmeter, and check the resistance from grid to ground, and plate to ground, of each tube. If C3 or C4 is shorted, the plate to ground resistance will be zero and no plate voltage will be measured on either tube. If C2 is defective the bias voltage supply will be grounded and the entire bias supply voltage dropped across R2. Both tubes will draw a steady, heavy, plate current, there will be no output and the plate will most probably glow red. If RI is open or T2 is defective there will be no output. In the case of R1 open, no grid voltage will be measured from grid to ground with a voltmeter. In the case of a defective T2, no beat signrd will be present to provide an output and no r-f (oscillator) voltage will be present at the grid. If T1 is open no bias will be measured from grid to ground of V1 or V2, and either there will be no output, a weak output, or a badly distorted output. If tuning capacitor Cl is shorted there will be no oscillator output and no audio output from T3. If the secondary of T3 is open there will be no output, and continuity cannot be measured with an ohmmeter. There is also a possibility that the plate supply may be open because of a blown fuse in the power supply. Check for supply

voltage to ground at the center tap of T3, if not present the trouble is in the power supply. If R2 is shorted and an extremely high bias exists at the grids of V1 and V2 they can be held at cutoff and there will be no output. Also, do not neglect to check the bias supply for the proper voltage since it may be at fault.

Reduced or Low Output. Improper plate or bias voltage, or a defective tube can cause a reduction of output. Measure the bias and plate voltages to ground with a voltmeter. If the voltages are lower than normal, check the values of RI and R2 with an ohmmeter (with bias voltage disconnected). Check capacitor C2 for leakage using an in-circuit capacitance checker. If the plate voltage is low check the resistance of the primary winding of T3 (with plate voltage off), and check C3 and C4 for leakage to ground with a capacitance checker. There is also the possibility that R1 may be misadjusted, and the output can be brought back to normal by resetting RI. Also check the input and output with an oscilloscope. The signals in the secondary of T1 should be greater in amplitude than in the primary. Likewise the output voltage should be greater than the primary audio voltage. If the signal at the primary of T1 is lower than normal with the receiver gain control at maximum, the receiver is at fault. Check the preceding stages of the receiver.

Distorted Output. If the simulated carrier (oscillator) is not set at the correct frequency there will be distortion. If the frequency is sufficiently low it is possible that the lower sideband is being received rather than the upper. This can be recognized by the inverted speech. As the simulated carrier is reduced in frequency by tuning Cl the speech should develop more low frequencies; if the frequencies increase instead, the lower sideband is being received and the carrier frequency should be increased until the distortion disappears. If the ratio between the input and the oscillator signal amplitudes is less than 10:1. readjust RI for the proper amplitude until the distortion disappears. If the bias on V1 and V2 is improper the output may be larger than normal but greatly distorted. Check the bias with a voltmeter and check the bias supply for normal output voltage. Also check R2 for proper tolerance value.

# TRIODE, PARALLEL OUTPUT **BALANCED** DETECTOR (ELECTRON TUBE)

#### Application.

The triode parallel output type of balanced detector is commonly employed in single sideband receivers used in fixed station transoceanic telephony, where the full output of a push-pull type detector is not required.

# Characteristics.

Uses triode tubes for increased gain and improved balancing.

Has a balanced input and a push-push (parallel) output.

Requires a reference oscillator input, together with a sideband input, to produce an output.

Uses either fixed or self bias.

### Circuit Analysis.

General. The simulated carrier (r-f oscillator) signal is applied to the triode grids in push-pull and cancels out in the plate circuit. Thus, with an oscillator input, but no sideband input there is no output, since any r-f not cancelled is bypassed to ground. When a sideband signal is applied to the grids it alternately adds to and subtracts from the simulated carrier signal. The plate current of one tube increases while the plate current of the other tube decreases. Thus the net change of current flow through the output transformer primary is zero for the r-f signals. Since opposing fields are produced in each half of the transformer primary, and the plate circuit is bypassed to ground for r-f, no output can occur. Simultaneously, the signals beat together and produce an audio frequency plate current flow which is not bypassed to ground. The audio voltage changes in the primary of the output transformer produce an audio output in the secondary. When the polarity changes from cycle to cycle, so does the audio signal and both the positive and negative half cycles are produced. The amplitude of the oscillator input is made adjustable to reduce distortion.

**Circuit Operation.** The schematic of a typical triode parallel output type of balanced detector is shown in the following illustration.



**Triode Balanced Detector with Parallel Plates** 

Oscillator transformer T1 has a center-tapped push-pull secondary. Fixed bias is applied to the grids of V1 and V2 through i-f input transformer T2 tuned by variable capacitor Cl. R-f decoupling is provided by feeding the bias voltage through decoupling resistor R2, and C2 bypasses any r-f to ground, effectively placing the rotor of Cl at r-f ground potential. Potentiometer R1 acts as an adjustable voltage divider across the input tank to permit adjusting for the proper amplitude ratio between the oscillator and sideband signals. The plates of VI and V2 are parallel connected and bypassed to ground for r-f by C3. Transformer T3 is an audio output transformer from whose secondary the audio output signal is taken.

Assuming that the r-f oscillator alone is operating with no sideboard input signal, the grids of VI and V2 are driven in opposite directions by the push-pull connected secondary of T1. Thus, if VI is driven in a positive direction, V2 is driven in a negative direction. Since the amplitude of the oscillator signal is the same at both grids, with the plates connected in pardlel an increase of plate current on one tube is balanced out by an equal decrease of plate current on the other tube. Hence, the net change of current flowing through the primary of output transformer T3 is effectively zero. In addition any r-f component appearing in the plate circuit is offered a low impedance path to ground by bypass capacitor C3 and no output is developed by T3.

When a sideband input signal appears on the secondary of T1 it is applied in parallel to both tube grids and alternately adds to and subtracts from the oscillator signal. Thus, during one half cycle VI is conducting heavily and V2 is conducting lightly. On the next half cycle of oscillator, or signal input, the opposite polarity prevails at the grids and V2 conducts more than V1. Since the signal component is applied equally to both grids the increase in plate current flow through one tube is counteracted by the decrease of plate current in the other tube. Once again, the net change for any current flowing through output transformer T3 is effectively zero and no output is produced. To ensure that no r-f output exists, bypass capacitor C3 is used to shunt the plate circuit to ground for r-f signals. Thus, neither the sideband input signal or the simulated carrier (oscillator) signal can appear in the output of T3. However, when both signals are applied to the tube grids, they beat together and produce sum and difference frequencies. Since the sum frequency is a bigh radio frequency it is bypassed to ground C3 and has no effect on the output. On the other hand, the difference signal is the low frequency audio signal which was orignally changed to a sideband signal in the transmitter modulator. Since the capacity of C3 is very small it offers a high impedance to the audio component, while the path through the primary of audio output transformer T3 offers a low impedance. As a result, the audio frequency changes in plate current pass through the primary of T3 and induce an audio output voltage in the secondary.

Potentiometer R1 is used to adjust the relative amplitude of the sideband input signal so that with a given oscillator input amplitude, the sideband signal may be adjusted to be one tenth of this value (a 10:1 ratio produces optimum beat frequency performance). Also, capacitor Cl is used to tune the secondary of T2 for maximum input signal response. In some circuit variations Cl is placed across the oscillator transformer primary together with R1, and adjusts the oscillator amplitude instead of the input signal amplitude. Use of these adjustments permits a better balance to be obtained and reduces the effects of noise and spurious beats when properly adjusted.

# **Failure Analysis**

No Output. Lack of an input signal, or no oscillator input, will prevent an output. Defective tubes, loss of plate voltage, improper bias voltage, or a shorted capacitor (C2 or C3) can also cause loss of output. First measure the bias and plate supply voltages. If either the bias or plate supply is at fault, the power supply fuse is blown or the trouble is in some portion of the power supply. With normal supply voltages check the grid voltage on tubes V1 and V2, and the plate voltage. With normal bias voltage at the supply terminal lack of bias on the grid of the tubes may be caused by RI, R2, or T2 secondary being open. Check the voltage at the junction of R2 and C2 to ground. If no voltage is present either R2 is open or C2 is shorted. Check the resistance of R2, and check C2 for a short. Zero resistance to ground across C2 indicates the capacitor is shorted. If bias voltage is present at R2 but not at the center tap of T1 secondary, potentiometer RI is open. Check the resistance of RI with the power off. If there is bias voltage at the center tap of T1 secondary, but not at either V1 or V2 grid, the secondary winding between the center tap and the tube grid indicating no voltage is open. Check the secondary winding for continuity. With normal plate supply voltage, but no voltage on the plate of V1 or V2, either the tubes are defective, capacitor C3 is shorted, or the primary of T3 is open or shorted. If T3 primary is open, no voltage can be measured from the top end of T3 primary to ground; if shorted, no voltage will be measured at either end of the winding. Check for continuity, with the power off, to verify that T3 is open, and measure the resistance to ground and across the winding. If the resistance to ground is less than 1-ohm, T3 is shorted to ground. Likewise, if the winding resistance is less than 1-ohm, the winding is shorted and no output will be obtained from the secondary. If the winding is open there will be no continuity and the meter will read infinity. In the case of a low resistance to ground the possibility exists that the ground is due to C3 being shorted. Similarly, a short to ground in V1 or V2 will cause a similar indication, however, the short will disappear when the defective tube is removed.

**Low Output.** If the ratio of amplitude between the oscillator simulating the carrier and the sideband signal input is less than 10:1 the beat signal will most probably be reduced. Low emission in tube V1 or V2, or low plate voltage and improper bias voltage can

also cause reduced output. It should also be kept in mind that a weak input signal which is below the normal threshold value of the receiver will also produce a low output, however, this is normal and can be caused by fading or other poor reception conditions. In the event of trouble it will usually be noted that all signals are weak. When due to external conditions, there will usually be signals of different strengths as the receiver is tuned over the operating spectrum. Where the receiver is equipped with a signal strength meter. comparison of known signals will usually indicate if operation is below normal. Assuming that a low output is suspected, check the plate and grid voltages. If these voltages are normal values as specified in the technical manual for the equipment, either one of the transformers T1, T2, or T3 may be defective, the oscillator stage may be at fault, or preceding receiver stages may not be performing properly. Check the amplitude of the input signal and that of the oscillator signal using a simulated test signal input. If the oscillator and input waveforms and amplitudes appear normal, or within specifications, the fault is probably in the plate circuit of the detector. If not normal, the trouble is in either the preceding stages or the oscillator stage, dependent upon which one is abnormal. If the oscillator signal is below normal either T2, Cl, or RI is at fault if the bias voltage is normal. If the bias voltage is abnormal either R1, R2, or C2 may be at fault. In either case check the resistors for within tolerance values and T2 for continuity. Check capacitor C2 for leakage. A lower than normal plate voltage and output can be caused by leakage in C3. A defective output transformer can be caused by leakage to ground in T3 or by shorted primary or secondary turns. If T3 is not at fault, the possibility exists that either or both tube sockets are defective or that leakage exists at some wiring tie point.

**Distortion.** Usually distortion is caused by overmodulation effects produced by the lack of sufficient oscillator amplitude or an excessively strong input signal. Check the oscillator stage and T2 for normal output. Readjust RI to see if the distortion can be changed or minimized, and in the case of a stronger than normal input signal check the preceding stages of the receiver for lack of AVC control or improper settings of the r-f gain control. Also check plate and bias voltages on V1 and V2. There is also the possibility that peaking of Cl or changing the oscillator
**ELECTRONIC CI RCUITS** 

frequency slightly may restore normal operation. If these changes do not restore operation, each of the parts in the circuit should be checked for proper value and leakage, and the preceding stages of the receiver checked to make certain that the distortion is not being produced elsewhere.

# PENTAGRID BALANCED DETECTDR

# Application.

The pentagrid type of balanced detector is employed in single sideband receivers where improved sensitivity and better balancing is desired than is obtained with diodes or triodes.

# Characteristics.

Uses pentagrid tubes to supply increased gain and improved balancing.

Has a push-pull input and a push-pull output.

Requires both a reference oscillator input and a sideband input to produce an audio output.

Uses self bias and degeneration for improved operation.

### Circuit Analysis.

General. The oscillator signal simulating an r-f carrier is applied through an input transformer with a center tapped secondary so that the input is applied in push-pull. The plates are also connected in pushpull through an audio output transformer. Thus the oscillator signal is cancelled in the plate circuit and does not appear in the output. The sideband input is resistance-capacitance coupled in parallel (push-push) to the tube grids. Because of the push-pull output, any r-f is cancelled in the plate circuit. Adjustable cathode bias permits setting for proper balance and cancellation. When both the oscillator and r-f signals are applied simultaneously, they beat together, and the difference voltage develops an audio output. The sum voltage is bypassed around the output transformer so that ordy an audio output is produced.

**Circuit Operation.** The schematic of a typical pentagrid balanced detector is shown in the accompanying illustration.



#### Pentagrid Balanced Detector

The oscillator input is applied through T1 which has a center tapped secondary, and the oscillator signal is applied to grid 3 or VI and V2 in push-pull. Resistor RI is the grid return resistor, bypassed for r-f by Cl. The sideband r-f input signal is applied through coupling capacitor C2 and grid resistor R2 to the control grids of V1 and V2. This connection applies the input signal in parallel (push-push), while the plates of both tubes are connected in push-pull through center tapped audio output transformer T3. The plate voltage is applied to the center tap of the primary winding of T3, and through voltage dropping and decoupling resistor R4 to the screens of both tubes. The screens are bypassed by C3 to place the screen grids at r-f and audio ground potential. Potentiometer R3 is connected between both cathodes with the variable arm connected to ground. Thus, the circuit may be accurately balanced by adjustment of the potentiometer, and complete cancellation of the r-f plate signal is obtained.

In the absence of an input signal, the simulated carrier input from the oscillator is applied to T1. Because of the center tap connection, which is grounded for r-f by Cl, the opposite ends of the

secondary winding are of opposite polarity. Thus when the grid of VI tends to increase plate current because of a positive input polarity, the grid of V2 is driven negative and reduces plate current flow. Normally, the fields in the primary halves of T2 would aid each other and produce a larger secondary output. However, transformer T2 is an audio transformer and offers an extremely high impedance path for r-f, and the distributed turn-capacitance offers a high leakage reactance which shunts the r-f around the transformer and to ground. Hence, there is no oscillator output from the secondary of T2. On the next half cycle of operation, the oscillator signal changes polarity and so do the grids of V1 and V2. Again, no output is obtained because of the high impedance and shunting capacitance of T2 primary winding. Since there is no effective change of plate current over the complete cycle of operation, the average plate current remains at the static value determined by the bias of grid 3. Grid bias is developed across RI by the flow of grid current, which charges C 1. Although grid current only flows on the positive half cycles, first VI grid conducts and then V2 grid conducts to produce a constant bias across c1.

When an input signal is applied to C2 an output is applied across R2 feeding both tube grids in parallel. Thus, if both grids are driven positive, plate current will increase and flow through the windings of T2 in opposite directions. Hence, equal magnetic fluxes are developed in the primary of T2 and cancel, so that no output appears in the secondary. On the negative half of the input cycle, plate current is reduced and again flows equally in opposite directions through the primary of T2, so that no output is produced. With R3 connected to ground, the cathode current of each tube can be adjusted for complete balance. Since R3 is not bypassed the cathode circuit becomes degenerative, and each signal instantaneously developes an opposing bias, which is applied to the cathode to reduce amplification to a low value. With the screen of V1 and V2 connected to the power supply through R4, a constant dc screen voltage is developed to determine the maximum plate swing available. Bypass capacitor C3 ensures that the screen voltage does not change with the signal and modulation to provide screen degeneration. Since the cathode current of both tubes flows through the screen and is controlled by the bias or signal voltages on number 1 and number 3 grids, it is clear that complete mixing of

both signals occurs. Therefore, when both the oscillator and input signals are simultaneously applied they produce a beat in the plate circuit which develops both sum and difference frequencies. Since the sum frequency is a high r-f or i-f signal it is bypassed across the primary of T2 by the high capacitance per turn (leakage reactance) and no output is produced. The difference voltage beat, however, is a low audio frequency which is offered a low reactance path through the primary winding of T2. Thus, the audio beat signal produces a change in magnetic flux linking the primary and secondary windings of T2, and these moving lines of force cutting the secondary winding develops an output voltage in T2. Since the rate of change of flux is at an audio rate, an audio output signal is produced. Because the circuit is degenerative the full amplification of the electron tubes is not realized. Since the output is taken in push-pull, the ratio of one half of the primary turn winding to the secondary turns usually provides a step up of voltage. It is important to remember that an output can only be obtained when both signals are applied together to create the audio difference (beat) signaL

### Failure Analysis.

No Output A loss of plate voltage, a lack of input (sideband) signal or simulated carrier (oscillator) signal, a defective tube, or open or shorted part can produce a loss of output. If T1 or T2 are defective the grid circuit of V1 and V2 can be open or shorted to ground. This will be indicated by a lack of bias developed across RI as measured with a high resistance voltmeter. If sideband input signal coupling capacitor **C2** is open no signal will appear on the grids of V1 and V2. Check for a signal on the grids of the tube and, if not present, check the input side of C2. If a signal appears on the input side but not on the grid side, check C2 for capacitance. If Cl is shorted to ground no oscillator signal will appear on grid 3. Check Cl resistance to ground or use a capacitance checker. If a signal appears on number 1 grid and an oscillator signal appears on number 1 grid and an oscillator signal on number 3 grid and there is no output, either R4 is open, C3 is shorted, or T2 is defective, or the tubes are at fault. Check for proper screen voltage on V1 and V2. If screen voltage is missing check R4 for a resistance value within tolerance (with plate and screen voltages off). Check C3 for a short, and also check the resistance of cathode

potentiometer R3. If plate supply voltage is present at the center tap of T2 primary winding but does not appear at the plates of VI and V2, the primary of T2 is open or shorted to ground. If plate voltage appears satisfactory but there is still no output, either the tubes are defective or the secondary winding of T2 is open or shorted.

Low Output Improper bias, plate, or screen voltage may cause a low output. A defective tube or partially open transformer T1 or T2 can also produce a low output. Check the bias, screen, and plate voltages. If normal bias is obtained across R3, or from the cathodes of VI and V2 to ground, and R3 can be adjusted for balanced voltages the tubes are probably satisfactory. If low screen voltage is indicated, R4 may have increased in resistance or C3 can be partially shorted. Check R3 for resistance and check C3 for capacitance. It is also possible that a high resistance primary on T3 can produce 10ss of, or low plate voltage. Check the resistance of T2 primary. If the bias, plate, and screen voltages appear within normal tolerance values, tubes VI and V2 may be at fault. Also, the oscillator amplitude may be low or the input (sideband) signal may be too weak. Check the operation of the oscillator and check for normal oscillator amplitude. If the oscillator circuit is satisfactory input transformer T1 may be defective. Check T1 primary and secondary for resistance, continuity, and turns ratio. A normal primary input, but low secondary output, indicates either T2 is defective, or Cl or RI is low. Check Cl for a partial short and RI for normal value. If the oscillator input is normal and the previous checks have been made, a low output may be produced by low input (sideband) signal. This can be caused by lack of proper amplification in the preceding receiver stages, or because coupling capacitor C2 is open, or grid return R2 is open. If R2 is open the circuit will most probably block on strong input signals. Check C2 for capacitance and leakage, and measure the resistance of R2.

Distorted Output. If the ratio of the oscillator signal to the input signal is too small, an improper beat will be developed and the output will be distorted. With an assumed normal oscillator this condition can be quickly checked by adjusting the receiver r-f gain control, and noting if the distortion can be made to disappear. If not, either the bias is at fault or the circuit is not properly balanced. Try readjusting R3 to determine whether or not balance will restore normal operation. If the distortion remains, make a resistance check of the resistors, and a capacitance check of the capacitors in the circuit. There is also the possibility that the oscillator which simulates the carrier is set to the wrong frequency and that the lower side band is being received instead of the upper sideband or vice-versa. This condition is easily determined by noting if the audio is inverted as the oscillator is tuned slightly past its center frequency (the audio note increases in pitch as the oscillator frequency is reduced). There also exists another possibility of distortion which is caused by improper transmitter adjustment. This can be determined by requesting the sender to reduce his audio gain or reduce peak r-f output and noting if the signal improves. Any distortion caused by selective fading will quickly return to normal when the fade is completed. Hence occasional bursts of distortion can be due to selective fading which cannot be controlled by the technician.

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# SECTION 11 MIXING, HETERODYNING, AND AUTOMATIC CONTROL CIRCUITS

# PART 11–1. MIXER CIRCUITS

# AUOIO MIXERS

# General.

Audio-frequency mixing is defined as the combining of two or more audio-frequency (20 to 20,000 Hz) **signals** from separate sources in any desired proportion at the input to an audio-amplifier system. The term *audio mixer* should not be confused with the term *mixer* used to designate the nonlinear circuit that heterodynes the r-f and local-oscillator signals in a superheterodyne receiver. Audio mixers are considered as "combining" circuits and are operated as linear circuits.

Audio mixing circuits are used in public-address, sound-distribution, and similar audio systems to combine two or more input-channel signals for further amplification in the main channel of an audioamplifier system. It is necessary to control the individual input-channel signal levels before mixing occurs. Also, if frequency compensation of the individual input signals is required, the frequency compensation must be accomplished before the signals are applied to the mixer input. It is desirable to have the individual signals to each mixer input as nearly equal to one another as possible so that similar control settings of the mixer circuit will produce similar output signal levels. This is especially true where the mixer circuit (channel) controls are front-panel controls which are easily accessible to the operator and require frequent operation or adjustment.

When a low-amplitude signal is to be mixed with a signal of greater amplitude, an audio-amplifier stage, called a *preamplifier*, is used to increase the amplitude of the smaller signal so that it is approximately equal to the amplitude of the larger signal; then the two input signals will be of approximately the same amplitude (level). before mixing occurs. In some instances, if the smaller of the two signals is at a satisfactory level for application to the mixer circuit, the signal with the larger amplitude is simply attenuated to a level which is equal to that of the smaller signal.

Audio mixer circuits can be classified as either electron- tube type of resistance-network type. Mixers may be further classified as high- or lowimpedance, constant- or nonconstant-impedance, and high- or low-level mixers. The audio mixer circuits briefly described in this section are representative of typical electron-tube audio mixers.

# COMMON PLATE-LOAO AUDIO MIXER

### Application.

The common plate-load audio mixer circuit is used to combine two (or more) input audio signals by amplifying the signals and combining them in a common load impedance. The mixer circuit is generally used in public-address and sound-distribution systems to provide for the control and mixing of several input channels.

### Characteristics.

Operates Class A with cathode bias.

Combines two individual input signals; each input signal is amplified, inverted, and combined in a common plate-load impedance with relatively low distortion.

Additional circuits can be connected in parallel to provide for additional input channels.

### Circuit Analysis.

**General. The** common plate-load audio mixer combines two input signals. The circuit is fundamentally two Class A audio amplifiers in parallel with a common plate-load resistance. The combined output signal is taken from across the plate-load resistance. More than two input signals can be mixed by applying each signal to a separate amplifier tube; each tube in turn, operates into the common plate-load resistance.

**Circuit Operation.** The following circuit schematic illustrates two triode electron tubes in a common plate-load audio mixer circuit. Electron tubes V1 and V2 are identical-type triode tubes; although two separate triodes are shown, a twin-triode is commonly used in this circuit. Potentiometer (variable resistors) RI and R2 are the grid resistors for V1 and V2, respectively. Also, R1 and R2 are used to terminate a preamplifier, crystal pickup, or other highimpedance signal source, and control the level of

signal applied to each grid of the mixer circuit. Resistor R3 is the common cathode-bias resistor for V1 and V2; capacitor C1 is the cathode bypass capacitor. Resistor R4 is the common plate-load resistor for both V1 and V2; capacitor C2 is the output coupling capacitor.



Common Plate-Load Audio Mixer

In this mixer circuit, the two input circuits are isolated from one another, so that the setting of one control (Rl or R2) will have no effect upon the other. The two inputs are relatively high impedance; potentiometers R1 and R2 generally range from 500K to several megohms. in practice, no great attempt is made to achieve an exact match of impedances at the input to the mixer circuit. However, the values of R1 and R2 are usually made sufficiently high to act as a load or terminating impedance for a preamplifier stage, a crystal pickup, or a highimpedance, high-output microphone. If the signal source is a low impedance, an input matching transformer is required to obtain impedance transformation from the low-impedance source to the relatively high-impedance input of the mixer circuit.

The operation of each tube in the common plateload audio mixer is similar to the operation of the R-C coupled triode voltage amplifier, described in the Amplifier Section of this Handbook, for individual input signals. For example, assume a condition where an audio signal is applied to Input No. 1 but no signal is applied to Input No. 2. In this instance, assuming that potentiometer RI is adjusted for a suitable input level to the grid of VI, the output signal developed across the plate-load resistor, R4, is 180 degrees out of phase with the input signal and is a reproduction of the input signal as it would be for any R-C coupled voltage amplifier. When audio signals are applied to both inputs of the mixer circuit, the combined signals appear across the plate-load resistor, R4, and are coupled through capacitor C2 to the grid circuit of the following audio amplifier stage. If the grid circuit of the following stage uses a potentiometer as the grid resistance (R-C coupling), then this potentiometer functions as a master gain control for the amplifier, since it controls the amplitude of the mixed audio signals applied to the grid of the following stage.

The mixer circuit illustrated is very satisfactory for two input channels. It uses two tubes sharing a common plate-load resistor. When more thao two inputs are desired, as for example three or four inputs, various circuit combinations incorporating three or four tubes may be used; however, there is a limitation to the number of tubes which can share a common plate-load resistance without suffering considerable loss of gain and introducing some distortion. Therefore, common plate-load mixers are generally limited to two or possibly three tubes. (Where more input channels are desired, modification of the basic circuit is necessary to provide a degree of plate-load isolation.) Since the plate resistances of the two tubes (V1 and V2) are in parallel, each tube works into a load impedance which is always less than its own plate resistance. Under such conditions of operation, the output voltage obtainable from the circuit is seriously limited.

Since one tube operates into a load consisting of the other tube's plate resistance effectively in parallel with the load impedance (R4), it is obvious that the gain of the two tubes as shown in the schematic will be less than the gain of a single voltage-amplifier tube because the load impedance for either tube is always less than its own plate resistance ( $r_p$ ). Therefore, the gain of each tube will always be less than one-half the gain obtained from a normal voltage amplifier. If the normal voltage amplifier is considered to be a constant-voltage generator, as shown in part A of the following illustration, the a-c component of plate current ( $i_p$ ) is:

$$i_p \frac{-\mu e_s}{r_p + Z_L}$$

and the ac component of output voltage (en) that appears across the load impedance,  $Z_{\rm \tiny L}$ , is:

$$e_o = i_p Z_L$$

By substitution then:

$$e \ . \quad \begin{matrix} -\mu e_s \\ r_p^= + Z_L \end{matrix} \quad Z_L$$





**Simplified Amplifier Circuit** 

It is apparent that the output voltage (e<sub>o</sub>) of a normal voltage amplifier is not  $\mu$  times the applied signal (e<sub>s</sub>), because some voltage is lost in the internal resistance (r<sub>p</sub>) of the tube and is not developed across the load impedance, Z<sub>L</sub>: In part B of the illustration, the plate resistance (r<sub>p</sub>) of a second tube is shown in parallel with the load impedance, as would be the

case for a two-tube mixer circuit. The load impedance for this condition can now be expressed as:

$$\frac{\mathbf{p} 2^{z} \mathbf{L}}{\mathbf{r}_{p} + \mathbf{Z}_{\mathbf{L}}}$$

where:  $Z_{L} = load$  impedance

'p2 <sup>■</sup>plate resistance of second tube

However, since identical tubes (Vl and V2) are used in the mixer circuit, the plate resistance of each tube can be considered to be equal to that of the other; therefore,  $r_{p2}$  is equal to  $r_p$ . The ac component of output voltage (e<sub>o</sub>) for the two-tube mixer can now be expressed as:

$$e \cdot \frac{-\mu e_s Z_L}{r_p^2 + Z_L}$$

Substituting 
$$\frac{r_p Z_L}{r_p + Z_L}$$
 for  $Z_L$ :

$$e_{o} = \mu e_{s} \frac{r_{p}Z_{L}}{r_{p} + Z_{L}}$$

$$\mathbf{P} \quad \frac{\mathbf{r}_{\mathbf{p}} \mathbf{Z}_{\mathbf{L}}}{\mathbf{r}_{\mathbf{p}} + \mathbf{Z}_{\mathbf{L}}}$$

$$=\frac{-\mu e_{s}Z_{L}r_{p}}{Z_{L}r_{p}+r_{p}^{2}+Z_{L}r_{p}}$$

$$\frac{-\mu e_{s} Z_{L} r_{p}}{r_{p}^{2} + 2 Z_{L} r_{p}}$$

$$e_{.} = \frac{-\mu e_{s} Z_{L}}{r_{p} + 2 Z_{L}}$$

From this expression it can be seen that, for two triodes in parallel, the output voltage  $(e_o)$  will always be less than one-half that obtained with a normal voltage amplifier. Similarly, for a three-tube mixer the gain will be less than one-third the gain obtained from a normal voltage amplifier; for a four-tube mixer it will be less than one-fourth.

Improved performance can be obtained by using pentode instead of triode tubes. The accompanying circuit schematic illustrates two pentode electron tubes in a common plate-load audio mixer circuit. Electron tubes VI and V2 are identical-type, sharpcutoff pentodes. The circuit is fundamentally the same as that previously described for triode tubes except for the addition of the screen-dropping resistor, R5, and the screen bypass capacitor, C3. The circuit operation is the same as that described for the triode mixer circuit.



Pentodes Using Common Pkrte-Load

When pentodes are used in the common plate-load mixer circuit, the loss of gain due to the shunting of the load impedance by other tubes is slight and, for all practical purposes, may be neglected. The plate resistance of a pentode as a resistance-coupled amplifier is extremely high compared to that of a triode, so that nearly the full gain of the pentode can be realized in this circuit.

#### Failure Analysis.

No Output. The common plate-load audio mixer circuit is similar in many respects to a resistancecoupled voltage amplifier circuit insofar as failures are concerned. Failure of the plate-voltage supply will disrupt operation of the circuit, as will an open circuit in the cathode. The filament and plate voltages should be measured, as well as the dc voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether the plate load resistor (R4) or cathode resistor (R3) is open. Each input should be checked with an oscilloscope to determine whether signals are applied to the input of the circuit and whether they are of the proper amplitude. An open output coupling capacitor (C2) will prevent signals from reaching the stage following the mixer.

If the mixer circuit uses pentode tubes, the voltage applied to the screen grid should be measured, to determine whether it is within tolerance and whether the screen bypass capacitor (C3) is shorted. A shorted screen bypass capacitor will remove screen voltage from the tubes and may cause the screen-dropping resistor, R5, to burn out. When normal output is obtained from one channel but not from the other, the input to the faulty channel should be checked with an oscilloscope to determine whether the trouble is due to an open input potentiometer (Rl or R2) or failure of the input-signal source.

Low or Distorted Output. The applied plate voltage should be measured to determine whether it is within tolerance. Also the output coupling capacitor, C2, should be checked to determine whether it is leaking; leakage of this capacitor will drop the applied plate voltage and permit voltage-divider action to affect the operation of the following stage. Thus, if \_ the input resistor of the following stage is returned to ground, the voltage at the plates of VI and V2 will be reduced, and the operation of the following stage will be upset by the change in voltage applied to its grid. An open cathode bypass capacitor Cl will cause the mixer circuit to be degenerative, and wiil also result in "cross-biasing" of the tubes so that the stage gain will be severely decreased. A shorted cathode bypass capacitor will result in a loss of bias and distortion of the output signal. Depending upon the configuration of the preceding stage (for example, a preamplifier stage, R-C coupled), it is possible that a dc voltage \_ may be applied to the input potentiometer (RI or

R2) because of a leaky or shorted coupling capacitor. In this case, a dc voltage which is dependent upon the setting of the potentiometer will be applied to the grid, and the tube bias will be affected.

In the pentode audio mixer circuit, a leaky screen bypass capacitor (C3) or an increase in the value of the screen-dropping resistor (R5) will cause reduced gain because of the decreased screen voltage, while an open screen bypass will cause reduced gain because of degeneration within the stage.

# SEPARATE PLATE-LOAD AUDIO MIXER

#### Application.

The separate plate-load audio mixer circuit is used to combine two (or more) input audio signals by amplifying the signals and combining them at the common input of a following stage. The mixer circuit is commonly used in public-address and sound distribution systems to provide for the control and mixing of several input channels.

# Characteristics.

Operates Class A with cathode bias.

Combines two individual input signals; each input signal is amplified, inverted, and fed through an isolation resistance to the common input of a following stage.

Additional circuits can be connected in parallel to provide for additional input channels.

### **Circuit Analysis.**

General. The separate plate-load audio mixer circuit combines two input signals. The circuit is fundamentally two separate Class A audio amplifiers with each output fed through an isolation resistor to a common input impedance of the following stage. More than two input signals can be mixed by applying each additional signal to a separate amplifier which has its own plate-load resistance, and feeding the amplifier output through an isolation resistance to a common input impedance of the following stage.

**Circuit Operation.** The following circuit schematic illustrates two triode electron tubes in a separate plate-load audio mixer circuit. Electron tubes VI and V2 are identical-type triode tubes; two separate triodes are shown, but a twin-triode is commonly used in this circuit. Potentiometers (variable resistors) RI and R2 are the grid resistors for V1 and V2, respectively. Also, R1 and R2 are used to terminate a preamplifier, crystal pickup, or other highimpedance signal source, and control the level of signal applied to each grid of the mixer circuit. Resistor R3 is the common cathode-bias resistor for V1 and V2; capacitor C1 is the cathode bypass capacitor. Resistors R4 and R5 are the plate-load resistors for V2 and V1, respectively, resistors R6 and R7 are the output-isolation resistors. Capacitor C2 is the output coupling capacitor.



Separate Plate-Load Audio Mixer

In this mixer circuit, the two input circuits are isolated from one another, so that the setting of one control (RI or R2) will have no effect upon the other. The two inputs each have a relatively high impedance; potentiometers RI and R2 generally range in value from 500K to several megohms. In practice, no great attempt is made to achieve an exact match of impedances at the input to the mixer circuit. However, the values of R1 and R2 are usually made sufficiently high to act as a load or terminating impedance for a preamplifier stage, a crystal pickup, or a high-impedance, high-output microphone. If the signal source is a low impedance, an input matching transformer is required to obtain impedance transformation from the low-impedance source to the relatively high-impedance input of the mixer circuit.

The operation of each tube in the separate plateload audio mixer is similar to the operation of the R-C coupled triode voltage amplifier, described in

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Section 6. When audio signals are applied to both inputs of the mixer circuit, the individual amplified signals appear across the respective plate-load resistors, R5 and R4. The individual signals are then applied through the series isolation resistors (R6 and R7) to the output coupling capacitor, C2, which couples the combined signals to the grid circuit of the following audio amplifier stage. If the grid circuit of the latter stage uses a potentiometer as the grid resistance, then this potentiometer functions as a master gain control for the amplifier, since it controls the amplifier grid.

The mixer circuit illustrated is very satisfactory for two input channels. When more than two inputs are desired, as for example three or four inputs, an additional tube is connected to the circuit for each additional input desired, and its individual plate load resistance is coupled to the common output circuit by means of an isolation resistor to provide a degree of isolation between amplifier tubes. Thus, some of the inherent disadvantages of the basic common plate-load audio mixer are overcome. The isolation resistors (R6 and R7) are usually two to five times the value of the individual plate-load resistors (R4 and R5). As a result, each tube in the mixer circuit works into a complex load impedance which approaches a normal load for a voltage amplified stage; therefore, distortion due to nonlinearity is considerably reduced. Although the normal stage gain is obtained when the tube works into a normal load, the output signal voltage available at the input of the following stage is considerably reduced because of the loss introduced by the signal-voltage drop across the isolation resistor. However, the net result is that the higher output voltage from the mixer is available at the input of the following stage for a given percentage of distortion, as compared to the output voltage obtainable from other triode mixer circuits, such as the common plate-load audio mixer.

The voltage delivered to the input of the following stage by the mixer is always less than one half that obtainable with a normal voltage amplifier. In the following **illustration**, the complex load impedance into which one tube works is simplified to show the amplified-signal voltage division and the resulting useful signal output available across the load impedance,  $Z_L$ , corresponding to the inPu<sup>'</sup>of the s<sup>ucc</sup> ceeding stage. Since both tubes (V1 and V2) employed in the mixer are identical-type tubes, the plate

resistances  $(r_p)$  can be considered to be equal. Also, the isolating resistors  $(R_s)$  are equal to each other, and the plate-load resistors  $(R_L)$  are equal to each other. The a-c component of output voltage  $(e_o)$  for the mixer using isolation resistors, expressed as a voltage relationship, is as follows:

where: 
$$\mathbf{e}_{1} = \mathbf{e}_{Rs}$$
  
 $\mathbf{e}_{Rs} = \text{voltage developed across } \mathbf{R}_{L}$   
 $\mathbf{e}_{Rs} = \text{voltage developed across isolating}$   
resistor  $\mathbf{R}_{n}$ 



Simplified Mixer Circuit

Since the resistance of  $\mathbf{R}_{s}$  is greater than the pedance,  $\mathbf{Z}_{T}$ , a greater signal voltage appears across  $\mathbf{R}_{s}$  than across  $\mathbf{Z}_{T}$ . Therefore, the output voltage (e<sub>o</sub>) developed across  $\mathbf{Z}_{L}$  must always be less than the voltage developed across the isolating resistor,  $\mathbf{R}_{s}$  and less than one-half the voltage obtainable from a normal voltage amplifier. Depending upon the value of the load impedance,  $\mathbf{Z}_{L}$ , the output voltage (e<sub>o</sub>) may be as low as one-third the voltage obtainable from a normal voltage amplifier.

Pentodes can be used to advantage in this circuit because the plate resistance of a pentode is extremely high compared to that of a triode. The value of the isolation resistor need only be several times the value of the plate-load resistor and, since nearly the full im-

gain capability of the pentode can be realized, the output voltage available at the load impedance will be greater than one-half of the output voltage obtained from a normal amplifier.

### Failure Analysis.

No Output. The separate plate-load audio mixer circuit is similar in many respects to a resistancecoupled voltage amplifier circuit insofar as failures are concerned. Failure of the plate-voltage supply will disrupt operation of the circuit, as will an open circuit in the cathode. With tubes known to be good installed in the circuit, the filament and plate voltages should be measured, as well as the dc voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether the individual plate-load resistors (R4 and R5) or cathode resistor (R3) is open. Each input should be checked with an oscilloscope to determine whether signals are applied to the input of the circuit. An open output coupling capacitor (C2) will prevent signals from reaching the stage following the mixer.

If the mixer circuit uses pentode tubes, the voltage applied to each screen grid should be measured, to determine whether it is within tolerance and whether the screen bypass capacitor is shorted. A shorted screen bypass capacitor will remove screen voltage from the tubes and may cause the screen-dropping resistor to burn out.

When normal output is obtained from one channel but not from the other, the input to the faulty channel should be checked with an oscilloscope to determine whether the trouble is due to an open input potentiometer (RI or R2) or failure of the inputsignal source.

Low or Distorted Output. The applied plate voltage should be measured to determine whether it is within tolerance. Also the output coupling capacitor, C2, should be checked to determine whether it is leaking. A leaky (or shorted) output coupling capacitor will form a voltage divider comprised of both isolating resistors (R6 and R7) effectively in parallel, and this combination is in series with the input resistor of the following stage. Thus, the voltage at the plates of V1 and V2 will be reduced somewhat, and the operation of the following stage will be upset by the positive voltage applied to its grid. An open cathode bypass capacitor C 1 will cause the circuit to be degenerative, and will also result in "cross-biasing" of the tubes so that the stage gain will be decreased. A shorted cathode bypass capacitor will result in a loss of bias and distortion of the output signal. Depending upon the configuration of the preceding stage (for example, a preamplifier stage, R-C coupled), it is possible that a positive d-c voltage may be applied to the input potentiometer (Rl or R2) because of a leaky or shorted coupling capacitor. In this case, a positive d-c voltage, the amount of which is determined by the setting of the potentiometer, will be applied to the grid and affect the bias.

If plate-load resistor R4 (or R5) should open, the plate voltage applied to V2 (or Vl) will be considerably below normal, since the plate voltage will be applied to the tube through both isolating resistors in series with the plate-load resistor, R5 (or R4) of the other tube, VI (or V2). As a result, the signal output from the tube with the plate voltage below normal will be extremely low.

If the mixer circuit uses pentode tubes, a leaky screen bypass capacitor or an increase in the value of the screen-dropping resistor will cause reduced gain because of the decreased screen voltage, while an open screen bypass will cause reduced gain because of degeneration within the stage.

#### **VIDEO MIXERS**

#### General.

Video mixing is defined as the combining of two or more video signals. The video signals to be combined consist of various forms of pulse information and may include any number of the following: radar video, beacon video, range markers, range strobe, azimuth markers, IFF video, blanking gates or pulses, and other special forms of information.

The term *video mixer* should not be confused with the term *mixer* used to designate the circuit that heterodynes the r-f and local-oscillator signals in a superheterodyne receiver. Video mixers are considered as "adding" circuits and perform algebraic addition of pulse information; the pulses can be of either polarity and need not be in coincidence. In certain applications, video mixers are designed to combine signals of a given polarity only. Also, in many radar applications, video mixers are designed to combine time-coincidence pulses in a nonadditive manner; operation in this manner prevents excessive output amplitude and possible overloading in subsequent video amplifier stages, and thus prevents "blooming" of the indicator display.

The majority of electron-tube video mixing circuits presently in use are variations of two basic types: the common-cathode video mixer and the common-plate video mixer. Most video mixer requirements can be met by one or the other of these two circuits. The common-cathode video mixer does not invert the signal but acts in a manner similar to the cathode follower, whereas the common-plate video mixer does invert the signal. The common-cathode video mixer is degenerative, and the amplitude of the combined output of the two input signals in coincidence is less than that of the larger input signal. The common-plate video mixer normally has some gain; as a result, the amplitude of the combined output of the two input signals in coincidence is generally greater than the larger of the two input signals. Therefore, if the amplitude of the combined output signal from the common-plate mixer is excessive for the application, modifications to the basic circuit are necessary to reduce the adding effect. Otherwise, the output is likely to overload subsequent video amplifier stages when coincident signals are applied to the input.

A video mixer is normally required to handle pulse information having pulse widths of 0.5 to 500 microseconds and pulse repetition rates of 200 to 2000 pulses per second. Common-cathode video mixers are capable of handling very fast rise-time pulses because of the cathode-follower action of the circuit. Common-plate video mixers are purposely designed with high frequency compensation, to enable them to handle the rise time of the input video pulses.

# COMMON-CATHODE VIDEO MIXER

### Application.

The common-cathode video mixer circuit is used to combine two (or more) input video or pulse signals. Depending upon the circuit configuration, when input signals are in time-coincidence the output signal can be a limited-amplitude combination of the input signals or a nonadditive output signal which is representative of the larger input signal only.

### Characteristics.

Input signals are of positive polarity; output signal is of positive polarity. Negative input signals can be combined (by the basic mixer circuit) only at very low levels.

Gain of video mixer (as a cathode follower) is approximately 0.75.

Degenerative circuit (cathode follower) provides limited-amplitude additive mixing of time-coincident signal pulses because of common-cathode biasing arrangement. Modification of basic circuit to include fixed bias near cutoff provides nonadditive mixing of time-coincident signal pulses.

When more than two input signals are to be combined, additional common-cathode video-mixer circuits may be connected in parallel with little change in operating characteristics.

Output impedance is relatively low.

### Circuit Analysis.

**General.** The basic common-cathode video mixer combines two positive video signals. The circuit is fundamentally two cathode followers in parallel with a common cathode resistance. The output polarity is positive, and the combined signal is taken from across the cathode resistance. Any number of positive input signals can be mixed by applying each signal to a separate cathode follower; each cathode follower, in turn, operates into the common cathode resistance. Whether or not any addition of signals occurs in the output depending upon the biasing of the cathodefollower stages.

Circuit Operation. The following circuit schematic illustrates two triode electron tubes in a common-cathode video mixer circuit. Electron tubes VI and V2 are identical-type triode tubes, although the accompanying schematic illustrates two separate triodes, a twin-triode is commonly used in this circuit. Capacitor Cl couples one input signal to the grid of V1; capacitor C2 couples the other input signal to the grid of V2. Resistors RI and R2 are the grid resistors for VI and V2, respectively. Resistor R3 is the common cathode-bias resistor for V1 and V2, and it is also the cathode load resistance for the videomixer circuit across which the combined, or mixed, pulse output signal appears. The plate of each tube is tied directly to the supply voltage,  $+E_{bb}$ . The tolerance of component values in this circuit is not critical, and 10-percent-tolerance parts are normally used.



Basic Common-Cathode Video Mixer Circuit

When voltage is first applied to the circuit, the grids (of VI and V2) are at zero bias, and the combined plate current of both tubes passes through common-cathode resistor R3 to quickly establish the no-signal, or quiescent, bias. The electron tubes, V1 and V2, are assumed to be identical-type tubes, or a single-envelope twin-triode with identical characteristics; however, a small unbalance in tube characteristics will not greatly affect the circuit operation.

The operation of each tube in the commoncathode video mixer circuit is similar to the operation of the cathode follower, described in the Amplifier Section of this Handbook, when the input signals are not in time-coincidence. For example, assume a condition where a positive pulse is applied to the input of V1 but no signal is applied to the input of V2. In this instance, as the input signal to V1 increases in a positive direction, the plate current of V1 increases, causing an increased voltage drop across cathode-load resistor R3. As the input signal to VI falls, the plate current decreases to its former value, causing a decrease in the voltage drop across cathode-load resistor R3. Thus, the output-signal voltage developed across the cathode-load resistor is a reproduction of the original input signal applied to the grid of V1. Furthermore, since the input signal produces a change in the cathode bias, this bias voltage is in phase with the input signal and therefore reduces the amplitude of the grid-to-cathode voltage of VI, producing degeneration of the output voltage. (Cathode-follower gain is

always less than one.) Note that as the plate current of V1 increases with signal the voltage developed across cathode-load resistor R3 also increases, and that this instantaneous voltage, in turn, changes the no-signal bias for the grid of V2. Thus, the instantaneous voltage increase developed across R3 by the signal applied to V1 effectively decreases the plate current of V2 and results in a decrease in the plate current of V2 through the common cathode-load resistor, R3. The net result is a decrease in the signal current through the cathode-load resistor because of the cathode-follower action of V1 and the degenerative action of V2. Therefore, the output-signal amplitude for one input signal is always less than the original input-signal amplitude.

The operation of the common-cathode video mixer when two input signals are in time-coincidence produces some adding of signals to give a combined output which is always less than the amplitude of the larger of the two coincident input signals and greater than the output signal that results when only one input signal is present. The limited addition of timecoincident positive input signals results from the use of a common cathode-load resistance which causes "cross-biasing" of the two tubes. The extent of signal adding is primarily a function of the value of the cathode resistor, R3, and the level of the input signals. Where the value of the cathode resistor is such that the gain of each stage is considerably less than unity (relatively small value cathode resistor), the biasing action is not complete and some addition of signals will always occur. When the no-signal bias is large (relative large value cathode resistor), but not sufficient to completely cut off the plate current, the gain of the cathode follower is less for small positive signals than for the larger positive signals. This effect is caused by nonlinearity in the gain characteristic at low input levels. Also, the gain is reduced, resulting in the addition of the input signals. Since some additive effect can be tolerated, initial cutoff of plate current for each tube is not necessary, and grid bias is normally obtained by cathode-resistor action only.

If the output of the common-cathode video mixer is required to operate into a low-impedance coaxial cable which is terminated in a low impedance, the effective value of the cathode-load resistance is also a low value. When this is the case, the gain of the mixer is decreased because of the lower output impedance; therefore, less cross-biasing is produced by coincident signals appearing at the cathode-load resistance.

If the mixer is biased to cutoff, it combines coincident input signals of identical pulse width (duty cycle) in which a manner that only the input with the largest amplitude appears at the output; this manner of operation is called *nonaddictive mixing*, and is described later as a modification to the basic mixer circuit.

The following tabulation compares the performance of a typical common-cathode video mixer circuit for three values of cathode-load resistance, 4700, 470, and 150 ohms. Two input signals of different pulse widths were used to obtain the data given. Each individual input level was adjusted to provide the output voltage given in the table, and then the input signals were applied simultaneously to each respective input to obtain time-coincident signals. The effect in each case was to obtain a combined output which was greater than the output obtained from either signal alone.

Cathode-Load Resistor (ohms)	4700	470	150
Output Volts (for one input)	3.0	3.0	3.0
Output Volts (two inputs in			
coincidence)	3.6	3.9	4.3
Input No. 1 (volts):			
<b>180-μsec</b> pulse at 400 pps	4.1	4.9	8.0
Input No.2 (volts):			
10-µsec pulse at 400 pps	4.0	4.9	6.0



Gain Characteristic of Common-Cathode Mixer

The preceding graph illustrates the gain characteristic and linearity of a single cathode-follower stage in a typical common-cathode video mixer circuit for three values of cathode-load resistance. Note that the largest value of cathode-load resistance offers the largest gain and provides the greatest range of linearity; whereas, the smallest value of cathode-load resistance provides less gain and poor linearity. Furthermore, the *additive factor* for time-coincident input signals will increase for the lower values of cathodeload resistance because the stage gain decreases; as a result, less cross-biasing is produced by the combined output **signals** developed at the common cathode-load resistor.

As previously stated, the output of the commoncathode video mixer for signals in time coincidence is always less than the amplitude of the largest input signal and greater than the output obtained from either input signal alone. An indication of the amount of addition of two signals in time coincidence is given by the *additive factor*. The additive factor (in percent) is expressed as:

Additive factor = 
$$10\frac{E_R - E_H}{E_L}$$

where  $E_R$  = resultant (combined output voltage for inputs in coincidence

 $E_{\rm H}$  = output voltage for highest input level

E<sub>L</sub> <sup>=</sup> output voltage for lowest input level

The effect of the value of cathode-load resistance (R3) upon the combined output pulse amplitude and the additive factor can be seen by comparing the re--suits obtained when using different values of cathode-load resistance. In the first example, a 4700-ohm cathode-load resistor is used; in the second example, a 150-ohm cathode-load resistor is used.

*a.* The value of cathode-load resistor for a video mixer is 4700 ohms. Assume two positive input signals of 4.8 and 4.1 volts amplitude and corresponding output signals of 3.6 and 3.0 volts amplitude. When the input signals are in coincidence, the measured output-signal amplitude is 4.2 volts. Using the formula given above to determine the additive factor:

E <sub>R</sub>	=	4.2
E <sub>H</sub>	=	3.6
E	=	3.0

Given:

Therefore:

Additive factor = 
$$100 \frac{4.2 - 3.6}{3.0} = 100 \frac{0.6}{3.0}$$
  
=20 percent

b. The value of cathode-load resistor fo, the video mixer is changed to 150 ohms. Again, assume two positive input signals of 4.8 and 4.1 volts amplitude and corresponding output signals of 2.0 and 1.8 volts amplitude. When the input signals are in coincidence, the measured output-signal amplitude is 2.8 volts. Using the formula given above to determine the additive factor: Given:  $E_{\mathbf{R}} = 2.8$   $E_{\mathbf{H}} = 2.0$  $E_{\perp} = 1.8$ 

Therefore:

In the

Additive factor = 
$$100 \frac{2.8 - 2.0}{1.8} = 100 \frac{0.8}{1.8}$$
  
=44 percent

load resistor is decreased in value, the gain is also decreased; however, as the gain is decreased the additive factor increases. **Conversely**, as the cathode-load resistor is increased in vahre, the gain approaches unity; however, as the gain is increased, the additive factor decreases.

The following waveforms illustrate the signalcombining characteristics of a typical basic commoncathode video mixer for four different signal-input conditions. In part A of the illustration, a 4-volt positive input pulse is applied to one input only, and the resulting output is a 3-volt signal. In part B, a 4-volt input pulse is applied to each input, and the resulting output is a 3.6-volt signal. This output signal results from the additive mixing effect when the two input signals of equal amplitude and pulse width combine to produce an output pulse which is greater than the 3-volt output signal of part A (resulting from only one input signal) but which is less than either input signal. In part C, two equal-amplitude input signals of unequal puke width are applied to the video mixer circuit. This waveform group illustrates the effect of duty cycle on the mixing action. In this case, the additive mixing effect is readily apparent, since the combined signals produce a stepped output waveform

which is 3.6 volts at maximum amplitude for the duration of the short pulse, and 3.0 volts amplitude for the remainder of the long pulse. For all practical purposes, upon termination of the short pulse, the output can be assumed to be the result of a single input signal. In part D, two equal-amplitude input signals which are not time-coincident combine to produce a series of 3-volt output pulses. This condition is representative of time-delayed or random pulses (neither input signal in coincidence) and, therefore, each signal produces an output voltage <u>similar</u> to that obtained in part A with one input signal.



Modified Common-Cathode Video Mixer, Nonadditive Circuit

In some radar applications, especially where the output pulse information is displayed on a cathoderay tube indicator as video or range marks, it is desirable to provide some form of limiting for timecoincident pulses so that the output voltage will be the result of the largest signal only. The process of combining two signals so that only the larger of the two signais is present in the output is called *non-additive* mixing.



Theoretical Signal-Combining Characteristics of Basic Common-Cathode Video Mixer

Modification to the basic common-cathode video mixer to achieve nonadditive mixing consists of biasing the tubes, VI and V2, approximately to platecurrent cutoff. This is accomplished by returning grid resistors R1 and R2 to a source of negative voltage, as illustrated in the accompanying circuit schematic. Then, if the common cathode-load resistance, R3, is made relatively large so that the voltage gain of each cathode-follower stage approaches unity, a signal applied to one grid in excess of the value of fixed bias will produce in the common cathode circuit sufficient cathode bias to prevent the other tube from conducting. For example, assume that the fixed negative bias has been adjusted to provide a quiescent condition at or near plate-current cutoff for both tubes. If a posi-

tive video pulse of approximately 10 volts is applied to the grid of V1, the resulting signal appearing across cathode-load resistor R3 will produce approximately 8.5 volts output, which is applied as additional (cathode) bias to the grid of V2. Thus, a signal of less than 10 volts amplitude at the input of V2 cannot overcome the total effective instantaneous grid bias, and the signal does not appear in the output developed across cathode-load resistor R3. As can be seen from this example, the largest input signal at any instant of time effectively takes over the circuit and masks input signals of lesser amplitude. This is true provided that the time-coincident signals have the same pulse width (duty cycle); however, if the signals are of different pulse widths and of sufficient amplitude to overcome the fixed bias, the signal with the longest pulse width will, always appear in the output.

#### Failure Analysis.

No Output The common-cathode video mixer circuit is similar in many respects to a cathode-follower circuit insofar as failures are concerned. Failure of the plate voltage supply will disrupt operation of the circuit, as will an open circuit in the cathode. The filament and plate voltages should be measured, as well as the dc voltage developed across the cathode-load resistance, to determine whether the applied voltages are within tolerance and whether the cathode resistor, R3, is open. Each input should be checked with an oscilloscope to determine whether signals are applied to the circuit and whether they are of the proper amplitude. Lack of signals at the grid of VI or V2 can be due to an open coupling capacitor (Cl or C2) or to failure of the external input-signal source. The output circuit should be checked to determine whether the load impedance has decreased or whether the output is shorted. Such a condition would effectively place the cathode at ground potential, resulting in very low or no output; for example, a low value of terminating resistance or a shorted coaxial cable could cause this effect. Also, if the output is taken through an output coupling capacitor, an open in the capacitor would prevent signals from reaching the stage following the mixer.

No **Mixed or Combined Output** Assuming that applied voltages are within tolerance and the tube is

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known to be good, each input signal should be checked with an oscilloscope to determine whether both signals are of correct amplitude and are present at the respective grid of VI and V2. Lack of a signal at the grid of VI or V2 can be due to an open coupling capacitor (Cl or C2) or failure of the external input-signal source. If the circuit uses fixed grid bias to place each tube at or near plate-current cutoff, the applied bias should be measured at each grid to determine whether the bias voltage is excessive, thus preventing signals from combining in the cathode circuit.

Low or Distorted Output. If capacitor Cl or C2 is leaky or shorted, any value of dc voltage present at the input from the previous stage will be applied to the grid of V1 or V2. If the grid is made positive as a result, the tube will conduct additional plate current and cause the cathode voltage to be higher than normal. Thus, positive pulses on the grid will be severly limited in the cathode circuit. Where fixed bias is applied to the grid of V1 and V2, a leaky or shorted coupling capacitor C 1 or C2 will cause voltage-divider action to change the value of bias at the grid. This will cause the tube to shift its operating point on the  $E_g - 1_p$  characteristic curve. Depending upon the previous stage and the input circuit configuration, the bias may be shifted to place the tube in either the cutoff or saturated region.

If the cathode-load resistor (R3) is paralleled with a terminating or impedance-matching resistor, a decrease in the value of either resistance will affect the output voltage. Also, if the output is taken through an output coupling capacitor, a shorted capacitor will affect the output voltage, since the impedance in the cathode circuit will be decreased and a dc path will be provided in parallel with the cathode-load resistance.

# COMMON-PLATE VIDEO MIXER

#### Application.

The common-plate video mixer circuit is used to combine two (or more) input video or pulse signals. The mixer circuit normally has some gain. When two positive input signals are in time-coincidence, the circuit performs algebraic addition to produce a combined output signal which is of greater amplitude than the output produced by either input signal alone.

#### Characteristics.

Produces inverted signal in output; input signals of positive polarity produce output signals of negative polarity. The circuit is capable of combining small negative input signals to produce positive output signals.

Gain of normal video mixer (as designed) is slightly greater than unity for single input signal; gain is always greater than unity for time-coincident input signals.

When more than two input signals are to be combined, additional common-plate video-mixer circuits may be connected in parallel with little change in operating characteristics.

Output impedance is approximately equal to the value of plate-load resistance at low and medium frequencies, but decreases at high frequencies unless compensation is used.

High-frequency compensation, if required, is accomplished by the addition of a series plate-load inductance or a cathode bypass capacitor of relatively small value.

### Circuit Analysis.

**General.** The basic common-plate video mixer combines two positive input signals. The circuit is fundamentally two video amplifiers in parallel with a common plate-load resistance. The output polarity is negative, and the combined signal is taken from the plate circuit.

The common-plate video mixer has good adding characteristics for signals in time-coincidence. For this reason, when the input signals are timecoincident, the circuit may not be satisfactory for certain radar applications unless modifications are made to reduce the adding effect and prevent overloading of subsequent video amplifier stages. In some applications the video mixer circuit is followed by a limiter or cathode follower, or each input is preceded by a limiter. The circuit described here purposely has a very low plate-load resistance and an unbypassed cathode resistance, to keep the gain as low as possible. Also, the use of a low value of plate-load resistance makes frequency compensation unnecessary.

**Circuit Operation. The** accompanying circuit schematic illustrates two triode electron tubes in a common-plate video mixer circuit. Electron tubes V1 and V2 are identical-type triode tubes; although the

accompanying schematic illustrates two separate triodes, a twin-triode is commonly used in this circuit. Capacitor Cl couples one input signal to the grid of V1; capacitor C2 couples the other input signal to the grid of V2. Resistors RI and R2 are the grid resistors for V1 and V2, respectively. Resistor R3 is the common plate-load resistor for VI and V2 and is generally a low-value resistance. Capacitor c3 is the output-coupling capacitor. Resistor R4 is the common cathode-bias resistor. The circuit utilizes a low value of plate-load resistance to achieve an extremely short rise time; no high-frequency compensation @ate-load inductance or cathode bypass) is used. The unbypassed cathode resistor makes the circuit degenerative, and also keeps the stage gain stabilized throughout the life of the tube to compensate for tube aging. The tolerance of component values in this circuit is not critical; 10-percent-tolerance parts are normally used.



Basic Common-Plate Video Mixer Circuit

When voltage is first applied to the circuit, the grids (of V1 and V2) are at zero bias, and the combined plate current of both tubes passes through common-cathode resistor R4 to quickly establish the no-signal, or quiescent, bias. The electron tubes, VI and V2, are assumed to be identical-type tubes, or a single-envelope twin-triode with identical character-

istics; however, a small unbalance in tube characteristics will not greatly affect the circuit operation.

The operation of each tube in the common-plate video mixer circuit is similar to the operation of the triode video amplifier, described in the Amplifier Section of this Handbook, when the input signals are *not* in time-coincidence. For example, assume a condition where a positive pulse is applied to the input of V1 but no signal is applied to the input of V2. In this instance, as the input signal to VI increases in a positive direction, the plate current of V1 increases, causing an increased voltage drop across plate-load resistor R3; therefore, the voltage at the plate of VI falls. As the input signal to V1 falls, the plate current decreases to its former value, causing a decrease in the voltage drop across plate-load resistor R3, and the plate voltage at V1 returns to its former value. Thus, a positive-going pulse applied to the grid has produced a negative-going pulse at the plate, resulting in signal inversion. However, since the cathode resistor, R4, is not bypassed, degeneration is introduced in the circuit, and the signal developed across cathode resistor R4 resulting from the change in VI plate current is in phase with the input signal; therefore, the amplitude of the instantaneous grid-to-cathode signal voltage of VI is reduced. The stage gain is also reduced, and, as a result, the amplitude of the negative signal developed in the plate circuit is effectively limited. The plate-load resistor, R3, is purposely a low value of resistance, and because of degeneration in the cathode circuit (resistor R4 is not bypassed) the gain of the stage is practically reduced to unity for a single input signal.

Note that as the plate current of VI increases with signal, the voltage developed across cathode resistor R4 also increases, and that this instantaneous voltage, in turn, changes the no-signal bias for the grid of V2. Thus, the instantaneous voltage increase, developed across cathode resistor R4 by the signal applied to Vl, appears as additional bias to the grid of V2 and effectively decreases the plate current of V2 through the common plate-load resistor, R3, and the common cathode resistor, R4. The net result is a limiting of the maximum instantaneous signal current through R3 and R4 because of the cathode-follower action of VI and the degenerative action of V2. Thus, the negative output-signal amplitude at the plate for one input signal is only slightly greater than the original inputsignal amplitude.

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The operation of the common-plate video mixer when two positive input signals are in timecoincidence produces addition of the signals, to give a combined negative out-put signal which is always greater than either of the two coincident input signals and greater than the output signal that results when only one input signal is present. The common cathode resistor, R4, is purposely left unbypassed to obtain degeneration and "cross-biasing" of the tubes; therefore, the amplitude addition of time-coincident signals is somewhat limited.

The accompanying graph illustrates the gain characteristic of a common-plate video mixer for one input signal In practice, the circuit is normally sup plied positive input pulses, Since the gain characteristic is nonlinear, a small positive input pulse will produce a negative output pulse which is only slightly greater than the input (gain approximately unity); whereas input pukes from approximately 3 to 9 volts result in a gain greater than unity, and input pulse greater than 9 volts result in a gain less than unity. Note that if small negative pulses are applied to an input, a small positive output pulse. will be obtained.



Gain Characteristic of Common-Plate Mixer

Two additional tubes can be paralleled with the mixer circuit, if desired, to provide four inputs. If the values of the plate and cathode resistors (R3 and R4) are not changed, the gain of each stage will be reduced to half the gain obtained for two tubes; how-

ever, if cathode resistor R4 is reduced accordingly to keep the bias approximately the same as for two tubes, the gain of each of the four tubes will be slightly greater than unit y.

An indication of the amount of addition of two signals in time coincidence is given by the *additive factor*. The additive factor (in percent) is expressed as:

Additive factor = 
$$100 \frac{E_{R} - E_{H}}{E_{H}}$$

where:

Å

ER	=	resultant (combined) output voltage
		for inputs in coincidence
Eu	=	output voltage for highest input level

 $E_{L}$  = output voltage for lowest input level

The signal addition occurring at the plate as a result of combining two time-coincident input sigmls compared to the output obtained for a single input can be seen from the measured results obtained from a typical common-plate video mixer. The mixer in this example used a plate-load resistor (R3) of 680 ohms, a cathode resistor (R4) of 270 ohms, and a supply voltage ( $E_{bb}$ ) of 150 volts. Two equal positive input signals of 3.5 volts amplitude produced equal corresponding negative output signals of 4.0 volts amplitude. When the two input signals were applied to the mixer input circuit in time-coincidence, the measured output-sigml amplitude at the plate was 6.2 volts. Using the formula given above to determine the additive factor:

Given:

$$\begin{aligned} \mathbf{E}_{\mathbf{R}} &= 6.2 \\ \mathbf{E}_{\mathbf{H}} &= \mathbf{E}_{\mathrm{L}} = 4.0 \end{aligned}$$

Therefore: Additive factor =

$$\frac{1006.2 - 4.0}{4.0} = 100\frac{.2.2}{4.0} = 55 \text{ percent}$$

From the example it is seen that the common-plate video mixer combines time-coincident input signals in an additive manner.

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The following waveforms illustrate the signalcombing characteristics of a typical basic commonplace video mixer for two different signal-input conditions. In part A of the illustration, a 3.5-volt positive input pulse is applied to one input only, and the resulting negative output is a 4-volt signal. In part B, a 3.5-volt input pulse is applied to each input; the pulses are of equal amplitude but are of unequal pulse width (duty cycle). The resulting combined output signal is a negative pulse which is 6.2 volts maximum amplitude when the two signals are time-coincident. Note that the longer input pulse produces a 4-volt output signal and that, when the short input pulse is applied to the circuit, the combined output signal is increased to 6.2 volts for the duration of the short pulse.



Thaoretieel Signal-Combining Charaetaristics of Basic Common-Plate Video Mixar

This type of mixer cannot prevent overloading of subsequent video amplifier stages by time-coincident input sigmls; therefore, the mixer is usually followed by a limiter stage to limit the output signal applied to the video amplifier chain. The limiting **level** is determined by the highest output-sigml amplitude resulting from one input signal; any additional output-signal amplitude resulting from two input signals in time-coincidence will result in clipping at the limiter stage.

#### Failure Analysis.

**No Output.** The common-plate video mixer circuit is similar in many respects to a video-amplifier circuit insofar as failures are concerned. Failure of the platevoltage supply will disrupt operation of the circuit, as will an open circuit in the cathode. With a tube known to be good installed in the circuit, the filament and plate voltages should be measured, as well as the dc voltage developed across the cathode resistance, to determine whether the applied voltages are within tolerance and whether the plate-load resistor (R3) or cathode resistor (R4) is open. Each input should be checked with an oscilloscope to determine whether signals are applied to the circuit and whether they are of the proper amplitude. Lack of signals at the grid of VI or V2 can be due to an open coupling capacitor (Cl or C2) or to failure of the external input-signal source. An open output coupling capacitor (C3) will prevent signals from reaching the stage following the mixer; a leaky or shorted output coupling capacitor will form a voltage divider with the input resistor of the following stage. Thus if the input resistor of the following stage is returned to ground or to a negative supply, the voltage at the plates of VI and V2 will be reduced, and the operation of the following stage will be upset by the change in voltage applied to the grid.

No **mixad or Combined Output.** Assuming that the applied voltages are within tolerance and the tube is known to be good, each input sigml should be checked with an oscilloscope to determine whether it is of correct amplitude and is present at the respective grid of VI and V2. Lack of a sigml at the grid of V1 or v2 can be due to an open **coupling capacitor (C1** or C2), an open grid resistor (RI or R2), or failure of the external input-sigml source.

Low or Distortad Output. If one input coupling capacitor (Cl or C2) is leaky or shorted, any value of dc voltage present at the input from the previous stage will be applied to the grid (V1 or V2) by voltage-divider action of the capacitor and grid resistor (R1 or R2). If the grid is made positive, the tube will conduct additional plate current and cause the cathode voltage developed across R4 to be higher than normal. Thus, the bias of one tube is shifted because of a change in voltage at the grid, and the bias of the other tube is changed as a result of a change in cathode voltage. Since the input pulses are positive, it is possible that plate-current saturation

will occur for the fust tube and that the second tube will provide an output pulse of reduced amplitude when tirnecoincident signals are applied to the circuit. The output, therefore, will be low or distorted and will not be representative of a normal mixed or combined output.

# PART 11-2. HETERODYNING CIRCUITS

### MIXERS

### General.

The frequency-moversion function in a superheterodyne receiver is accomplished either by a mixer circuit with a separate local oscillator or by a pentagrid converter circuit (described later in this section).

The term *mixer* used in this section should be confused with the term *audio mixer*, which designates the linear circuit used to combine audio signals. The term *mixer*, as used in this section, designates a nonlinear circuit that heterodynes radio-frequency and local-oscillator signals in a superheterodyne receiver to produce an intermediate-frequency signal.

In receiver design practice, it is desirable to convert the receiver r-f signal to an intermediate frequency before further amplification takes place. The principle of frequency conversion and subsequent amplification at an intermediate frequency results in excellent selectivity and over-all gain characteristics for the receiver. The frequency conversion is obtained by the *heterodyne* process, which is the combining of an incoming radio-frequency signal with a locally generated sigml in a nonlinear device, to produce frequencies equal to the sum and difference of the two combining frequencies. The mixer stage sometimes referred to as the *first detector in* the superheterodyne receiver, performs only the frequency conversion function, and must be supplied a heterodyning r-f voltage generated by a separate localoscillator circuit. The output frequencies of the mixer stage, in addition to the frequencies of the input voltages, are primarily the sum and difference of the

signal-input frequency and an integral multiple of the local-oscillator frequency. The output circuit of the mixer stage is tuned to select only one frequency, which is usually a beat frequency equal to the difference between the signal-input frequency and the local-oscillator frequency. This difference, or beat, frequency is known as the *intermediate frequency*.

At this time a brief discussion of the heterodyne principle is helpful in order to better understand the production of beats in a superheterodyne receiver. The accompanying illustration shows graphically how a beat (intermediate) frequency is produced when two different signal frequencies of unequal amplitude are combined. If the two waveforms, parts A and B, are superimposed, the waveform given in part C results; this waveform shows amplitude fluctuations with respect to the time axis. At each instant, the two signal frequencies (A and B) combine to produce a resultant amplitude which is equal in value to the algebraic sum (A + B) of the individual sigml values. The amplitude variations, represented in part C as the dotted lines forming an envelope for the resultant, are called *beats*, and vary in amplitude at a frequency that is equal to the difference between the frequencies of the two signals being combined. Thus, from a study of the combined waveform given in part C, it can be seen that during the time interval between t. and  $t_1$  the number of beats per second is equal to the *difference* between the two frequencies given in parts A and B.

For simplicity, frequencies of 12 and 8 Hz are given in parts A and B, respectively. The evelope of the resulting waveform in part C is shown as 4 cycles per second. The output signal which results after the combined signals are acted upon by a nonlinear device in the mixer stage is shown in part D as the intermediate (beat) frequency. Although the frequencies (12, 8, and 4 **Hz**) used in the following illustration are extremely low, the heterodyne principle would be the same for other corresponding frequencies, such as 1200, 800, and 400 kHz, or 12, 8, and 4 MHz. Thus part A can be thought of as the received r-f signal, part B as the local-oscillator signal, and part D as the intermediate-frequency (beat-frequency) output of the mixer stage after demodulation.



Heterodyning of Two Signals of Unequal Amplitude

To produce an output which has very little distortion, the amplitude of the locally generated signal must be larger (usually at least ten times larger) than that of the received r-f signal. This principle is shown by the previous illustration representing the heterodyning of two signals of *unequal* amplitude. The following illustration shows the heterodyning of two signals of *equal* amplitude, and the distortion which results. Note that the envelope of the waveform shown in part C drops to zero, and that there is resulting distortion in the demodulated waveform shown in part D.





If one of the two frequencies (A or B) being heterodyned is modulated, the same action as previously described will occur, except that the resultant waveform shown in part D will vary in amplitude according to the modulation component of the original input frequency (A or B).

The accompanying block diagram illustrates the heterodyne principle of a frequency converter consisting of a mixer and local oscillator. Two voltages of different frequency are each fed to the input of the mixer; one voltage is the r-f signal voltage, and the other is the voltage generated by the local oscillator. These two voltages beat, or heterodyne, within the mixer to produce an output having, in addition to the frequencies of the two input voltages, many sum- \_ and-difference frequencies. The output of the mixer

includes a tuned circuit to select the desired beat frequency. The beat frequency is generally chosen to be a frequency which is the difference between the two mixer-input frequencies.



### Block Diagram of Mixer and Looal Oscillator

In the block diagram, a modulated r-f sigml is applied to the mixer stage; an unmodulated r-f signal of constant amplitude from the local-oscillator circuit is aJso applied to the mixer stage. The heterodyning, or mixing, of these two signals produces, in the mixer output, an intermediate-frequency sigml which contains all of the modulation characteristics of the origiml modulated r-f signal. The undesired sum-anddifference frequencies and the two mixer-input frequencies (r-f and oscillator signals) are rejected by the tuned circuit in the output of the mixer; only the desired intermediate (difference or beat) frequency is permitted to pass through the tuned circuit. This intermediate-frequency sigml is then amplified and detected in succeeding stages of the receiver.

The local-oscillator frequency differs from the frequency of the received r-f signal by an amount equal to the intermediate frequency; therefore, the localoscillator frequency can be either *above* or *below* the received r-f sigml and, in either case, produce the desired intermediate frequency. Depending upon the design requirements of the receiver and the frequencies involved, the local oscillator is tuned to a frequency either higher or lower than the r-f signal frequency. When the local-oscillator frequency is *below* the received r-f signal, the following formula applies:

$$fif = f_s - f_{osc}$$

where:

 $f_{ii}$  = intermediate frequency  $f_s$  = received r-f signal frequency  $f_{osc}$  = local-oscillator frequency

When the local-oscillator frequence is *above* the received r-f signal, the following formula applies:

fif 
$$\mathbf{f}_{\mathbf{0}\mathbf{s}\mathbf{c}} \mathbf{f}_{\mathbf{s}}$$

The mixer circuit includes a nonlinear element, consisting of either an electron-tube or semiconductor device; if an electron tube is used, the nonlinear element can be a simple rectifier (diode), a triode, or a multigrid tube. When a triode, tetrode, or pentode electron tube is used as the nonlinear circuit element, the tube is biased at or near cutoff, or otherwise operated on a nonlinear portion of its characteristic curve. Triode and multigrid electron tubes used as the mixer in superheterodyne receivers generally produce some signal amplification (conversion gain), in addition to the desired frequency conversion. A discussion of similar nonlinear elements is given in the Detector (Demodulator) Circuits Section of this Handbook.

Mixer-local oscillator combination circuits can provide reasonable frequency stability in superheterodyne receivers up to approximately 500 MHz. The mixer circuits described in this section are representative of typical electron.tube mixers found in many communication-electronic equipments.

### **DIODE MIXER (ELECTRON TUBE)**

#### Application.

The diode mixer is used in superheterodyne receiver circuits to combine, or "mix", the r-f sigml from a local oscillator with the incoming r-f signal, in order to produce the desired i-f (intermediatefrequency) output signal. The electron-tube diode

mixer is generally used in applications where signalto-noise ratio is an important consideration or where the transit time at very high frequencies becomes critical for other types of electron-tube mixers.

#### Characteristics.

Requires a separate local-oscillator circuit to supply the heterodyning voltage.

Utilizes the principle of rectification by a nonlinear device.

Output circuit is tuned to the difference frequency, or intermediate frequency.

Conversion gain is less than unity.

Signal-to-noise ratio is good.

#### Circuit Analysis.

General. The diode mixer is one of the simplest types of mixer circuits employed as a frequency converter. In this application, voltages of the two input frequencies to be heterodyned are applied in series to the diode, and the mixer-output voltage is obtained from a tuned transformer or impedance-coupling arrangement. The output circuit is tuned to the difference frequency (intermediate frequency) so that it will pass this frequency on to the succeeding intermediate-frequency amplifier stages but will attenuate (reject) all other frequencies.

The electron-tube diode used as a mixer is subject to transit-time effects; therefore, its use as a mixer at very high frequencies is somewhat limited. When transit-time effects are important, the crystal diode is frequently used as a mixer in preference to the electron-tube diode.

**Circuit Operation.** A simple diode mixer circuit is illustrated in the following circuit schematic. Transformer T1 consists of an untuned primary winding and a tuned secondary winding; capacitor Cl and the secondary winding of T1 form a resonant circuit at the frequency of the r-f sigml to be received. Transformer T2 is similar to TI, except that capacitor C2 and the secondary winding T2 form a resonant circuit at the frequency of the local-oscillator signal. The resomnt circuits, shown in the schematic as Tl, Cl and T2, C2, are actual L-C circuits composed of inductors and capacitors at all radio frequencies up to the ultra high frequencies. At the ultra high frequencies and above, the tuned circuits may be in the form of tuned lines or resonant cavities.



**Diode Mixer Circuit** 

Electron tube V1 is a cathode-type diode; the **filament** (heater) circuit is not shown on the schematic.

Transformer T3 is a double-tuned transformer, with the primary and secondary circuits resonant to the output (intermediate) frequency. This **trans**former exhibits a bandpass characteristic and thereby discriminates against frequencies above and below the desired output frequency.

When no r-f signal is applied to the input of transformer Tl, but the local-oscillator signal is applied to the input (primary) of transformer T2, diode V1 acts only as a rectifier. For this input condition, the current pulsations passing through the primary winding of the double-tuned transformer, T3, are those of the local-oscillator frequency; however, the tuning of transformer T3 does not permit the **local-oscillator** frequency to reach the output because of the bandpass characteristic of the transformer.

When the r-f sigml and the local-oscillator signal are simultaneously applied to their respective tuned circuits (T1 and T2), the two signal voltages are ap plied in series to the mixer diode, V1.

Since the two applied signals differ in frequency, the voltages are not always in phase with each other. Periodically these two voltages algebraically add or subtract to produce an amplitude variation at regular intervals; it is this periodic amplitude variation in the form of a beat-frequency voltage which is of greatest importance. The beat frequency is actually the difference frequency produced by the instantaneous L

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signal voltages as they combine to increase amplitude when approaching an in-phase relationship and to decrease amplitude when approaching an out-of-phase relationship.

Because the two sine-wave frequencies are superimposed, the mixer diode rectifies, or detects, both frequencies. As a result, pulsating currents which vary in amplitude at the beat-frequency rate are produced in the primary of transformer T3. Thus, a carrier envelope is formed which varies in accordance with the difference frequency. The pulsating currents forming the carrier envelope flow through the primary winding of transformer T3. Since the primary circuit is tuned, it presents a high impedance to the difference (intermediate) frequency. Consequently, this frequency is passed by transformer T3, and a voltage is induced in the secondary winding which varies is amplitude in accordance with the amplitude of the origiml r-f sigml.

If the received r-f sigml contains amplitudemodulation components, the beat difference will also contain amplitude-modulation components, which vary in accordance with the audio frequencies modulating the original r-f signal. If the received r-f sigml is frequency-modulated, the beat difference will deviate at the same rates as the original r-f sigml. Thus, it is seen that the characteristics of the intermediate-frequency sigml are the same as those of the original received signal, except that the frequency of the received signal has been "converted" to a lower frequency.

The output signal voltage developed across the secondary tuned circuit of transformer T3 is applied to succeeding intermediate-frequency amplifier stages and is subsequently detected, or demodulated.

#### Failure Analysis.

**General.** Since the circuit of the diode mixer is relatively simple, failure of the circuit to operate can be resolved to one of several possibilities. The diode, VI, should be checked to determine whether it is in satisfacary condition and whether the correct filament (heater) voltage is applied to the tube.

The presence of an r-f signal (or a test signal) and the local-oscillator signal must be determined, since no output can be obtained from the mixer circuit unless both sigmls are applied to the mixer input. Resonant circuits T1, **C1** and T2, C2 must be prop erly aligned, each to its specified frequency. The double-tuned output transformer, T3, must also be correctly tuned to the desired intermediate frequency. Since one or more open windings in the tuned circuits (TI, T2, and T3) can cause a lack of output, these windings should be checked with an ohmmeter to determine whether continuity exists.

# DIODE MIXER (SEMICONDUCTOR)

### Application.

The semiconductor diode mixer is used in transistorized superheterodyne receivers in heterodyne frequency converter circuit arrangements to provide the intermediate frequency; and in electron tube high-frequency receivers to provide a low-noise r-f to i-f mixer. Special purpose applications include test equipment, microwave repeaters, and single-sideband transmitters, in which mixers are used for frequency conversion.

#### Characteristics

Requires a separate source of heterodyning voltage (local oscillator).

Uses nonlinear transfer characteristic of a diode to provide mixing action.

Conversion gain is less than one, and efficiency is high.

Signal-to-noise ratio is high (better than that of an electron tube).

Heterodyne-signal (local oscillator) amplitude must be larger than received-signal amplitude for minimum distortion and best efficiency.

#### Circuit Analysis.

**General. The** semiconductor diode mixer is one of the simplest types of mixer circuits employed in frequency conversion. In this application, the two signal voltages to be heterodyned are supplied in series to the diode, and the mixer output voltage is obtained from a tuned-transformer arrangement. The output circuit is tuned to the intermediate frequency, which is usually the difference frequency between the two signals. Thus all other unwanted frequencies are rejected, and the i-f signal (which also contains the modulation components of the input signal) is sup plied to the i-f amplifier for further amplification. The preceding discussion concerns the use of the mixer in receivers where the input signal is converted

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to a lower frequency. In very low frequency receivers, or in a sideband generator where the signal in generated at a low frequency and heterodyned to a higher frequency, the opposite condition exists, and the sum frequency is the output frequency. In each case, the circuit actions are the same, but the frequencies of interest are different.

**Circuit Operation. The** accompanying circuit schematic shows a simple diode type mixer.



In this circuit, T1 is tuned to the high frequency input sigml, and T2 is tuned to the lower-frequency local-oscillator signal. The secondaries of T1 and T2 are connected in series, and the r-f input is superimposed on the local oscillator signal. The combined sigmls are effectively rectified by crystal diode CR, producing a difference frequency current in the primary of output transformer T3, comected in series between the cathode of the crystal and ground. Since T3 is tuned to the desired intermediate frequency, it offers a high impedance at that frequency, and thus serves as the load across which the output voltage is developed. The secondary of T3 is also tuned to the i-f signal, and together with the tuned primary, it provides a highly selective circuit with bandpass characteristics.

When the signal voltages in the secondary of T1 and T2 are in phase, they add and the voltage applied to the crystal is increased. When they are out of phase, the voltages subtract and the crystal input voltage is reduced. Since the two voltages are sinusoidal, the resultant sigml will also be sinusoidal, and vary similarly. Because the new signal is a composite signal, its maximum and minimum amplitudes will occur at different times from those of the other signals. Thus the frequency of the new signal will be different from the original frequencies. Any intelligence existing as modulation (either AM or FM) on these carriers will be transferred to the new signal. Since the local-oscillator signal is unmodulated, the new sigml will contain the modulation of the highfrequency received signal, together with an unwanted hum or noise components present on the localoscillator signal.

Since the crystal conducts only when its anode is positive with respect to the cathode, only the positive alterations are effective. Pulses of current are produced at the rate of the original sigmls plus the com**posite** signal. This current flows through the primary of T3 and induces a voltage in the secondary of T3. Since both the primary and secondary of T3 are tuned, the greatest output voltage will occur at the frequency or over a range of frequencies for which the highest impedance is offered. Frequencies outside this band will be offered a low impedance, and little or no output voltage will be developed. Thus only the selected output frequency is obtained.

The basic principle of mixer operation is the use of the noniinear transfer characteristic of the crystal diode to produce signal voltages in the output which did not exist in the input signaL At the same time, all modulation components present on the original signal must be effectively transferred to the new signals. The desired output frequency is then selected by a tuned circuit and separated from all the other unwanted frequencies. The manner in which this is accomplished is shown in the accompanying illustrations.

First, let us examine the transfer characteristic of a crystal diode and compare it with a linear characteristic, as shown in the accompanying illustrations.

**ELECTRONIC CI RCUITS** 

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Crystal Diode Characteristic

Characteristic



**Mixer Output Wavaforms** 

As the input voltage to the crystal varies the current also varies, but not equally for all increments of input voltage. On the other hand, the ideal linear curve will result in equal current increments for equal voltage increments. If the diode voltage-current characteristic were linear, the input voltage would produce a current which, when passed through a resistor or load impedance, would produce an output voltage identical to the input voltage. Therefore, if two different voltages were applied as inputs, exactly the same voltages would be obtained in the output (except for a slight loss due to the resistance in the crystal). Thus, frequency conversion could not occur if the diode transfer characteristic were linear. On the other hand, when an input voltage is applied to the nonlinear diode, a distorted output is obtained. The distortion consists of signals which differ in frequency from the original sigml. If two different signals are applied to the nonlinear diode, the output circuit contains distortion products for both sigmls. These extraneous signals are the sum and difference frequencies of the original sigmls, plus beats between the origiml signals and the distortion products (which are beat signals themselves), as illustrated in the following figure.

To produce the desired conversion with fidelity, one input (usually the input supplied by the local oscillator) must be larger than the other. This is easily accomplished by using the weak high-frequency input signal as the small signal, and the strong localoscillator signal as the large signal. When the input voltage is large enough to appear at the point of greatest inflection on the diode characteristic curve, the best efficiency is obtained. The following figure illustrates the conversion transfer graphicrdly. In effect, the small input signal of 5 MHz modulates the large local-oscillator signal of 4 MHz and produces a 1-MHz beat signal, which rides on the local-oscillator carrier somewhat like a ripple voltage. The output

circuit contains pulses for each positive cycle of the two input frequencies, plus the beat signal. Selection of the desired output frequency is obtained by using a tuned circuit as the load. The greatest output is developed, of course, at the beat frequency to which the load is tuned, and the other frequencies are effectively rejected.



#### **Development of Beat Signal**

The manner in which the conversion efficiency varies with local-oscillator signal amplitude is shown graphically in the following figure. As can be seen the best efficiency is obtained for the strongest local-oscillator signal that can be handled by the diode. Since the detector output increases very slowly after the maximum inflection point of the characteristic curve is reached, the efficiency changes very little beyond this point. Thus there is a limit beyond which not much change of efficiency occurs if the local-oscillator power is increased. Note, however, that for very small sigmls the efficiency is low. In addition to low conversion efficiency when the input signal is of the same amplitude as the local-oscillator sigml, extreme distortion is produced, because the beat signal varies from zero to a maximum of twice normal (in effect 100% modulation). In **this case** the circuit acts somewhat like a square-law detector. Little use is made of this circuit characteristic. Normally, the local-oscillator signal amplitude is fixed at about ten times the amplitude of the received signal.





It is interesting to observe that the local-oscillator signal is always unmodulated; if both signals were modulated, the linear transfer of modulation would be annulled because of phase cancellation between modulation components. The normal transfer of modulation occurs linearly even through the beat is produced by deliberately distorting the r-f signal. This deviation from the normal rule of avoiding distortion is due to the large separation in frequency between the modulation (usually an audio-frequency signal) and the input and local-oscillator signals (which are always radio-frequency signals). The audio modulation varies at such a relatively slow rate that many r-f cycles can be lost without a noticeable change in fidelity; that is, any change in the amplitude of a single r-f cycle has little effect on the over-all operation.

Since the semiconductor diode will conduct in a reverse direction, it represents a lower-impedance load than the conventional electron tube diode, and it also has a lower forward resistance. Neither parameter, however, has any great effect on the operation of the diode as a mixer.

# Failure Analysis.

L.

No Output. If the local-oscillator signal or the r-f input is missing, no i-f output will be produced. Both signals must be present to obtain frequency conversion. An open circuit in the input transformer (T1) or the local-oscillator transformer (T2)-either primary or secondary-will also render the circuit inoperative. A defective crystal may be checked by making forward- and reverse-resistance checks of the diode. The reverse resistance should be very much larger than the forward resistance. Since the proper functioning of transformer T3 is necessary to select the output signal, an open circuit in this transformer could also result in no output. Moreover, it is possible that mistuning of the input circuits could cause absence of one of the signals and produce a no-output indication. A resistance or continuity check of the transformers should be made to insure that the circuit is complete, and a test signal should be applied to the input to heterodyne with the local-oscillator signal while checks are made for an output signal in T3. It will be necessary to use a VTVM with an r-f probe to determine whether the i-f voltage is present. With a modulated input to the mixer, an oscilloscope with an r-f probe can be used to observe whether the modulation appears in the output.

Low **Output.** A low-output condition can occur if the local-oscillator signal is equal to or less than that of the input signal. Such a condition could be caused by mistuning of T1 or T2. Substituting a test signal in place of the local-oscillator signal will quickly determine whether the oscillator output is low (if the proper value is known, the oscillator voltage can be measured with a VTVM and r-f probe). A similar result could be produced by the local-oscillator being tuned off frequency as a result of improper padding or alinement.

**Other Conditions.** Defective shielding or lack of proper lead dress after repair may permit the local-oscillator signal to leak into the preceding stages of the receiver and reduce the receiver sensitivity by producing a high avc voltage. Or it may allow the local-oscillator signal to feed through the i-f and detector stages and cause birdies and unwanted signals. Such troubles will disappear when the local oscillator is temporarily disabled and a well shielded test-sigml source is substituted in its place.

# MICROWAVE DIODE MIXER (SEMICONDUCTOR)

#### Application.

**The** microwave diode mixer is used in superheterodyne radar receivers to combine, or "mix", the incoming r-f microwave signal with the local oscillator signal to produce the desired intermediate frequency (i-f) output signal. The microwave diode mixer is generally used applications where signal-to-noise ratio is an important consideration or where transit time at very high frequencies becomes critical for other types of semiconductor mixers.

#### Characteristics,

I-f voltage is linearly dependent upon signal amplitude, for sigmls small compared with the local oscillator power.

Transit time effects are minimized.

Overall noise figure is as low as 7 dB at frequencies Up to 25,000 MHz.

Requires a separate local oscillator to supply the heterodyning voltage.

Output circuit is tuned to the i-f frequency.

Conversion gain is less than unity.

# **Circuit Analysis.**

General. The crystal is the most effective element for the superheterodyne receiver at microwave frequencies. The operation of a crystal as a mixer is similar to that of the diode electron tube. Since a crystal is not an **amplifier**, there can be no conversion gain. The conversion loss is taken as the ratio of the available i-f sigml power to the available r-f signal power. It varies with the circuit impedance but is normally about 6 to 10 dB. Crystals are easily damaged, and voltages should not be applied which are greater than about 5 volts in the blocking (anode to cathode) direction or which result in more than about l-vdc in a resistive load. In application, the desired r-f input signal and the local oscillator signal are applied in series to the microwave diode, and the mixer output voltage is obtained from a transformer tuned to the desired i-f signal so that it will pass this frequency and reject all other frequencies.

**Circuit Operation.** A simplified microwave diode mixer circuit is shown in the accompanying illustration.



**Microwave Diode Mixer Equivalent Circuit** 

**Transformer** TI consists of an untuned primary winding and a tuned secondary winding; Capacitor Cl and the secondary winding of T1 form a resomnt circuit at the frequency of the received r-f signal. Transformer T2 is similar to Tl, except that capacitor C2 and the secondary winding of T2 form a resonant circuit at the frequency of the local oscillator. This resonant circuits, shown in the schematic as Tl, Cl and T2, C2, are actual LC circuits composed of inductors and capacitors at radio frequencies.

Semiconductor CR1 is a point contact crystal diode used at microwave frequencies. Transformer T3 is a doubletuned transformer, with the primary and secon&ry circuits resonant to the intermediate frequency. This transformer has a bandpass characteristic which discriminates against frequencies above and below the desired output frequency.

When no r-f signal is applied to the input of transformer Tl, but the local oscillator signal is applied to the input (primary) of transformer T2, semiconductor CR1 acts only as a rectifier. For this input condition, the current pulsations passing through the primary winding of the double-tuned transformer, T3, are those of the local oscillator frequency; however, the tuning of transformer T3 does not permit the local oscillator frequency to reach the output because of the bandpass characteristic of the transformer.

When the r-f and local oscillator signals are applied simultaneously to their respective tuned circuits, the two signal voltages are applied in series to semiconductor mixer diode CR1. Since the two applied signals differ in frequency, the voltages are not always in phase which each other. Periodically these two voltages algebraically add or subtact to produce an amplitude variation at regular intervals; it is this periodic amplitude variation in the form of a beat frequency voltage which is of greatest importance. The beat frequency is actually the difference frequency produced by the instantaneous signal voltages as they combine to increase amplitude when approaching an in-phase relationship and to decrease amplitude when approaching an out-of-phase relationship.

Because the two sine-wave frequencies are superimposed, the mixer CR I rectifies, or detects, both frequencies. As a result, pulsating currents which vary in amplitude at the beat frequency rate are produced in the primary winding of transformer T3. Thus a carrier envelope is formed which varies in accordance with the difference frequency. The pulsating currents forming the carrier envelope flow through the primary winding of transformer T3. Since the primary circuit is tuned, it presents a high impedance to the difference (i-f) frequency. Consequently, this frequency is passed by transformer T3, and the output voltage is induced in the secondary winding which varies in amplitude in accordance with the amplitude of the original r-f signal.

If the received r-f signal contains amplitudemodulation components, the beat difference will deviate at the same rates as the original r-f signal. Thus, the characteristics of the intermediate fre quency signal are the same as that of the original r-f signal, except that the received sigml has been changed to a lower frequency.

The output (i-f signal) voltage developed across the secondary tuned circuit of transformer T3 is applied to the succeeding stages where it is amplified and demodulated.

### Failure Analysis.

**General.** When making voltage checks use a VTVM to avoid the low values of shunting resistance employed on the low range of conventional volt-ohmmeters. Be careful to observe the proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the diode junctions will cause a false low resistance **reading**.

No Output Since the circuit of the microwave diode mixer is relatively simple, failure of the circuit to provide an output can be resolved to one of several possibilities, The resonant circuits Tl, Cl and T2, C2 must be properly aligned to their respective frequencies. The double-tuned output transformer T3, must also be correctly aligned to the desired intermediate frequency. The presence of the desired r-f and local oscillator frequencies must be determined, since no output can be obtained from the mixer circuit unless both signals are applied to the mixer input circuits. One or more open windings in the transform"ers Tl, T2, or T3 can cause a no-output condition, so these windings should be checked with an ohmmeter to determine whether continuity exists. Capacitors Cl, C2, C3, and C4 can be checked with an in-circuit capacitor checker.

**Low Output.** If the tank circuits are not tuned to the proper frequencies, or if one of the capacitors should become leakly, a low output condition could occur. Check to see if the r-f, local oscillator, and i-f tank circuits are tuned properly, and check all capacitors for a leaky condition. output frequency, called the intermediate or i-f frequency, remains the same, regardless of the frequency of the r-f signal received.

By operating over the non-linear portion of the tube's characteristic  $E_g - I_p$  curve, harmonic distortion is produced in the plate circuit, and as a result of this harmonic distortion, new frequencies, which are harmonics of the input, are introduced. By proper selection of the local oscillator frequency, specific output frequencies can be obtained. This mixing of frequencies is called heterodyning, and the result at the plate is the presence of four basic frequencies: Namely, the sum and the difference of the two inputs, and the two original inputs (various other beats are also produced but are not often used particularly because of the small amplitude remaining as compared with the basic outputs). A resonant tank in the plate circuit is tuned to the selected difference frequency, so that it will pass only this frequency on to the succeeding i-f amplifier stages and thus effectively attenuate all of the other beat frequencies.

**Circuit Operation.** The accompanying circuit diagram illustrates a typical triode mixer.

# TRIODE MIXER (ELECTRON TUBE)

#### Application.

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The triode mixer is used in receiver circuits to combine or "mix" the r-f signal from the local oscillator with the incoming r-f signal, to produce the desired intermediate frequency (I-F) output.

#### Characteristics.

Requires a separate local oscillator circuit to supply the heterodyning voltage.

I-F frequency remains the same for any selected input frequency.

Operates on the non-linear portion of the  $E_g - I_p$  curve.

Has an amplification factor, which is referred to as conversion gain.

### Circuit Analysis.

**General. The** purpose of the mixer stage is to convert the incoming r-f frequency, usually into a lower frequency, which contains the same characteristics (modulation) as the original r-f frequency. This lower



**Typical Triode Mixer** 

L2, the secondary of T1, together with Cl, forms a tank circuit tuned to the desired r-f frequency, and

this selected r-f signal is applied directly to the control grid of tube VI. The tube is biased class "C" by the use of C2 and R1, which form a cathode bias circuit, and it is for this reason that the tube operates on the non-linear portion of the  $E_g-I_p$  curve. The signal from the local oscillator is coupled through transformer T3 to the cathode circuit of the tube, and because the tube operates on the non-linear portion of the characteristic curve, the two input signals are mixed. The result at the plate is a signal containing the sum and difference of the two inputs, plus each of the two originally applied signals. The primary, L3, of T2, together with C4, forms a tank circuit tuned to the difference, or i-f frequency, and capacitor C5 bypassed the unwanted r-f frequencies to ground.

With no r-f signal applied, and with the signal from the local oscillator applied to the cathode circuit, tube V1 conducts. The current through the cathode starts charging capacitor C2, but because of its long time constant, the cycle ends before the capacitor can charge to the peak value of the input. The charge is slow to leak off, however, because of the value of R1, and within a few cycles, the cathode circuit stabilizes at a voltage which determines the operating bias of the tube. For additional information on cathode bias, refer to the introduction to the Amplifier Section of this Handbook. Because of the large cathode bias, the tube operates class "C", and thus over the nonlinear portion of the  $E_g$ - $I_p$  curve.

Capacitor CI and the tuning capacitor in the local oscillator are mechanically connected. so that whenever the value of Cl is changed to operate the r-f tank at a particular frequency, the local oscillator tank is also changed automatically by the same amount. This results in the **local** oscillator frequency and the r-f frequency always being separated by the same amount of any frequency which may be selected at the input. The amplitude of the local oscillator voltage is approximately ten times as great as the r-f signal amplitude, for efficient mixing and the frequency is selected either above or below the r-f frequency, depending upon the application of the circuit, by an amount which is equal to the i-f frequency.

Under actual operating conditions, the following action takes place. The input r-f frequency and the local oscillator frequency are simultaneously applied to the grid and cathode circuits, respectively. As previously mentioned, these two inputs are of different frequencies, and consequently, they periodically vary in their phase relationships with each other. For this reason, they add or subtract algebraically at regular intervals, and the result at the plate is a new signal whose amplitude varies at a steady rate. This variation in amplitude is of primary importance, and is known as the "beat-frequency". This "beat-frequency" is in reality, the difference frequency which results from the algebraic addition of the two inputs as they approach an in-phase relationship, and their subtraction as the,y approach an out-of-phase relationship. This beat frequency is equal to the desired i-f frequency.

The resulting plate current pulses, whose amplitudes vary at the beat-frequency rate, arrive at the primary of transformer T2, and a carrier envelope which varies at the beat (i-f) frequency is developed. Since the primary of T2 is tuned to this i-f frequency by the use of C4, it presents a maximum load to the plate of the i-f frequency and the changing field that is developed around the primary winding induces an output in the secondary. All other beat frequencies present in the primary are not developed, because the impedance to these frequencies is of a minimum. For a detailed description of the heterodyning action, refer to the introduction to this section of the Handbook.

If the received r-f signal contains amplitude modulated components, the beat frequency also contains similar amplitude modulated components, which vary in accordance with the audio frequencies modulating the original r-f signal. If the received r-f signal is frequency modulated, the beat difference will deviate in frequency at the same rate as the original r-f signal. Thus, the characteristics of the i-f signal are the same as those of the original received signal, except that the frequency of the received signal is converted to a lower frequency.

A commonly used circuit variation of the triode mixer applies both the local oscillator and r-f signals to the grid of the tube. There is little operational difference, but cathode injection provides better oscillator stability, since the load impedance presented to the oscillator is lower.

The advantage of the triode mixer lies in its relative simplicity and relatively high signal to noise ratio. The conversion gain is about one third of that of the same tube used as an amplifier.

The use of the triode mixer, however, is limited to the VHF spectrum or lower. Above these frequencies, the effect of the interelectrode capacitance of the
tube elements becomes to great, and the low output is not practical.

# Failure Analysis.

**No Output.** A defective tube, an open or shorted Cl, C4, or C5, or a defective T1 or T2 can cause a no-output condition to exist. If no output exists, check the plate of V1 with a voltmeter for the presence of plate voltage. If plate voltage is not present, check L3 for a possible open and C5 for a short, with an ohmmeter. If no output still exists check C2, C4, and C5 with an ohmmeter for shorts or opens, also check T1 and T2 for continuity or possible shorts. Check the secondary of T3 also for a possible open circuit. If the above checks fail to locate the trouble, check all capacitors for value with an in-circuit capacitor checker.

Low or Distorted Output. A defective tube, or low plate supply voltage can cause a low output condition to exist, Check the plate supply voltage with a voltmeter for the proper voltage. Check the output of the local oscillator with an oscilloscope to make sure that it is of proper amplitude.

A distorted output can be caused by a defect in nearly any component in the circuit. Check for the presence of the r-f signal on the grid of V1 with an oscilloscope. If no signal is present, check for a signal on the primary of T1. If the signal is present on the primary, check the transformer windings with an ohmmeter for an open or short, and capacitor Cl for a possible short. If no signal is present on the primary, the trouble lies in the preceding r-f amplifier stages, and the mixer is probably not defective. Check for presence of the local oscillator signal on the cathode. If not present, check for its presence on the primary of transformer T3. If not on the primary, the trouble lies in the oscillator circuit, and the mixer is probably not at fault. If the signal is present on the primary, check the secondary of the transformer for a short or an open, and check RI and C2 for proper value. If both the local oscillator and the input r-f signals are present at the grid and cathode of the tube, the trouble is in the plate circuit. Make certain that the plate tank circuit is tuned to the proper i-f frequency. Check C5 with an in-circuit capacitor checker to determine if it has changed in value. Check the windings of T2 for a partial short, as this can change the resonant frequency of the tank.

# COMMON EMITTER MIXER (SEMICONDUCTOR)

#### Application.

The common emittermixerisused in transistor iz ed superheterod<sub>yne</sub> receivers to combine the incoming r-f signal with the local oscillator signal to produce the desired i-f frequency.

### Characteristics.

Provides conversion gain.

Requires a separate local oscillator to provide the heterodyning signal.

Utilizes the nonlinear transfer characteristics of the transistor to provide heterodyning action.

The transistor is biased in the low current region where nonlinearity is high.

A relatively high signal to noise ratio is obtained.

Operates better at higher frequencies because of reduced transit time effects.

#### Circuit Analysis,

General. The purpose of the mixer stage is to convert the incoming r-f frequency usually into a lower frequency which contains the same characteristics (modulation) as the original r-f frequency. This lower output frequency, called the intermediate frequency, or the i-f frequency, must remain the same for any r-f signal received within the range of the receiver for proper operation. The radio frequency is converted to an intermediate frequency by a process called heterodyning. When the input signal, along with another specific frequency referred to as the "local oscillator signal," is injected into the base (or emitter) of a transistor, four basic frequencies are obtained at the collector (although many other beat frequencies are also generated they are seldom used). These are the original two frequencies and the sum and difference of these inputs. A resonant tank in the collector circuit is tuned to the difference frequency, so that it will accept and pass this frequency on to the 'following stages and effectively attenuate all the other unwanted frequencies present.

There are also applications where an incoming signal is converted to a higher frequency, as in Very Low Frequency receivers and in Single Side Band generators, where the sum frequency instead of the difference frequency is used as the intermediate frequency. Circuit operation is the same for this

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application, the important change is that the output tank is tuned to the desired (sum) frequency.

The efficiency of frequency conversion in the transistor at lower frequencies is strongly dependent on the alpha rating or maximum usable gain capability of the transistor. Over the medium frequency range conversion output depends primarily on base resistance, and in the high frequency range conversion efficiency is limited by the amount of emitter reverse shunting capacitance, the less the capacitance the better is the performance. Conversion gain also influences the noise factor. At low frequencies the transistor is equal to a crystal diode with a transistor amplifier, while at vhf some gain may still be obtained, the noise is usually higher than that produced by the diode and transistor amplifier combination.

Circuit Operation. The accompanying diagram illustrated a typical common-emitter mixer.



Common-Emitter Mixer

As can be seen from a study of the schematic, resistors R1 and R2 form a voltage divider to provide base bias for Q1. Resistor R3, bypassed by capacitor C3, is a conventional emitter swamping resistor used to prevent temperature changes from altering transistor performance.

Winding L1 is the primary of Tl, and, together with capacitor C 1, forms a parallel resonant tank circuit tuned to the selected r-f signal frequency. This signal is inductively coupled to secondary L2 of TI. Transformer T2 injects the local oscillator signal on the base of Q1. Transistor Q1 is the nonlinear device used for heterodyning. The primary, L5, of transformer T3 together with C4 forms a parallel resonant tank circuit tuned to the difference (i-f) frequency, and capacitor C5 also shunts the unwanted frequencies remaining in the collector circuit to ground.

The bias voltage divider formed by RI and R2 together with emitter resistor R3 biases transistor Ql in the low current region of its dynamic transfer curve. Operation in this region provides good heterodyning action since considerable nonlinearity occurs " here.

The received r-f signal is coupled through T1 in series with the local oscillator signal injected through T2, to the base of Q1. Since these two frequencies are different the phase relationship between them is constantly changing. This causes these two signals to constantly add or subtract algebraically so that amplitude variations appear on the collector at regular intervals in the form of a newly developed beat frequency. This beat frequency is the desired product of heterodyning the two signals and is called the intermediate frequency. If the received r-f signal is amplitude modulated the resultant i-f signal will have the same amplitude modulation characteristics (the modulation is transferred linearly from one signal to the other). Likewise, if the received r-f frequency deviates around a center frequency at the same rate as the original r-f signal deviated. See the introduction to this Section for a detailed discussion of frequency conversion. C 1 and the tuning capacitor of the local oscillator are mechanically connected so that whenever Cl is turned to tune the r-f tank to a different frequency, the local oscillator frequency is, likewise, changed a corresponding amount. This results in a constant difference frequency being produced as the receiver is tuned over the entire range. The local oscillator signal amplitude is made approximately ten times that of the incoming r-f signal for efficient mixing. The resonant tank formed by the primary of T3, and consisting of L5 and C4 is tuned to the difference frequency or i-f. This resonant tank presents a high impedance only to the intermediate frequency and a maximum amplitude output signal is developed and inductively coupled to the secondary, (L6), of T3. Capacitor C4 which tunes the output tank circuit also presents a low impedance to the unwanted frequencies in the collector circuit, and they are shunted around L5 and bypassed to ground by C5. Normally this bypassing is sufficient.

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It has been noted, however, that in strong signal areas, and especially in all-wave types of superheterodyne receivers, that sometimes strong beat harmonic frequencies are "generated which are of sufficient amplitude to appear somewhere in the tuning range. Since these signals seem to appear at nonharmonic frequency points on the dial they cause the operator to infer that this station is operating off-frequency. This effect depends upon the choice of the i-f, whether or not it is single or double conversion, and it also depends upon how well the shielding is effective, and varies from model to model. This effect is mentioned here to indicate the importance of selecting only desired frequencies.

### Failure Analysis.

**General.** When making voltage checks, use a vacuum tube voltmeter to avoid low value of multiplier resistance employed on the low voltage ranges of the standard 20,000 ohm-per-volt meter. Be careful to observe proper polarity when checking continuity with an ohmmeter. Since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. A no-output condition is usually indicative of a defective transistor, or an open base, emitter, or collector circuit. In the common-emitter circuit a shorted base or collector would also cause no output. These conditions can easily be found by resistance and continuity checks with an ohmmeter. To prevent false readings, be careful to observe proper polarity when checking resistance or continuity. Check the power supply voltage to make certain that loss of output is not due to a blown fuse or a defective power supply.

It should be noted that an i-f frequency could not be produced by the mixer if the local oscillator signal can not reach the base of Q1. Presence of this signal can be determined by simulating this signal with a signal of proper frequency from a signal generator and injecting it into the base of Q1. An output then would indicate a fault in either the local oscillator, or local oscillator coupling transformer T2. Trouble could then be localized to either the local oscillator or T2 by injecting the simulated local oscillator signal in the primary of T2. If this causes an output it would be safe to assume that the local oscillator is at fault. If signal injection into the base of QI produced an i-f output and injection into the primary of T2 did not, T2 can be assumed to be at fault. It should also be noted that failure to the local oscillator will cause very little noise to be present at the output of the receiver. In contrast, failure of the r-f stages would not greatly affect the noise present at the receiver output, but would prevent or greatly diminish radio reception.

Presence of the r-f input signal can be determined by utilizing the procedure described above and applying it to transformer T1.

If resistance and continuity checks reveal that all components are good but an output cannot be produced even when injecting frequencies from a signal generator it is possible that the output tank, the primary of T3 is badly mistuned or the trouble probably exists in the secondary of T3. Check the resistance of the secondary of T3 with an ohmmeter. If the trouble persists the defect could possibly be in the input circuits to the following stage.

Low Output. Low output could be caused by a change in bias of a defective transistor. Check DC bias levels with a vacuum tube voltmeter. With power removed, indications of improper bias should be followed up with resistance checks to determine the component at fault.

It should be noted that deterioration with age causing lack of gain may result under high temperature conditions. Unlike vacuum tubes, however, transistors have operated for years without noticeable deterioration under proper operating conditions.

Another possible cause of decreased output would be insufficient local oscillator signal reaching the base of Q1. This condition could be checked by tracing the local oscillator signal through transformer T2 to the base of Q1, with an oscilloscope, noting that the amplitude is sufficient on the primary of T2 and that there is not excessive attenuation through T2. Less likely though a still possible cause of low output would be insufficient r-f signal reaching the base of Q1. This condition could be isolated to the proceeding r-f stages or transformer T1 by using the procedure described above for checing the local oscillator signal. Should all the conditions necessary for proper operation be met, i.e., proper operating bias, good transistor and sufficient amplitude input and local oscillation signals, poor performance could be the result of mistuning of output tank T3. With an r-f input into the receiver try tuning T3 for a peak receiver output.

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# AUTODYNE CONVERTER (SEMICONDUCTOR)

### Application.

The autodyne converter is generally used in transistorized radio receivers to convert the incoming r-f signal to an intermediate frequency (i-f), and amplify the i-f, for application to succeeding stages.

#### Characteristics.

Uses a single transistor to provide the functions of these stages.

Acts as a local oscillator.

Acts as an i-f amplifier.

Acts as a self-contained mixer.

Has lower conversion gain than circuit using a separate oscillator.

#### **Circuit Analysis.**

**General.** The autodyne converter is used as a combination local oscillator, mixer, and i-f amplifier in transistorized radio receivers. In operation, random noise in the oscillator section produces a slight variation of collector current. This signal is induced into the secondary winding of a transformer tuned to the oscillator frequency, and is then fed back to the emitter circuit. With the feedback winding of the transformer properly phased, the feedback is positive (regenerative) and of **suficient** amplitude to cause sustained oscillations.

In the mixer section, the transistor is biased in a relatively low current region, thus operating on quite non-linear characteristics. As the desired incoming r-f signal is tuned, it mixes with the local oscillator signal and provides at the output the following four signals; the original r-f signrd, the local oscillator signal, the sum of the two, and the difference of the two. Because the i-f tank circuit is tuned to the difference of the two signals, it is this signal which is selected, amplified, and applied to the following stage.

**Circuit Operation.** The schematic of a typical autodyne converter is shown in the accompanying illustration.



#### **Typical Autodyne Converter Circuit**

Q1 is a PNP type transistor whose base is capacitively coupled to the r-f input by Cl. Fixed base bias is supplied by the voltage divider consisting of RI and R2 bypassed for r-f by C2 (see the introduction to the Amplifier Section of this Handbook for a detailed explanation of biasing). Capacitor C3 couples the local oscillator tank circuit to the emitter of Q1, and also bypasses emitter swamping resistor R3 to prevent degeneration. The swamping resistor stabilized the transistor against theramal current changes (see the introduction to the Amplifier Section of this Handbook for a detailed explanation of emitter swamping action). The secondary winding of T1 together with tuning capacitors C4 and C5 form the oscillator tank circuit, which is inductively coupled to the collector by the primary winding. Thus, feedback is obtained from collector to emitter to sustain oscillation. Another tuned tank circuit resonated at the i-f is formed by the primary of T2 and capacitor C6. Collector voltage is obtained from the supply through dropping resistor R4, bypassed by C7 for undesired r-f and i-f signals. The secondary winding of T2 is inductively coupled to the primary to furnish the i-f output.
In operation, current flows through the transistor as determined by the biasing circuit. Internal noise or thermal variations initially produce a feedback voltage between the collector and the emitter which is in-phase with the input circuit. As the emitter current increases, the collector current also increases, and additonal feedback between the windings of Tl further increases the emitter current until it reaches the saturation region, where the emitter current no longer increases. When the current stops increasing, the induced feedback voltage is reduced until there is no longer any voltage fed back to the emitter circuit. At this time, the field around the tank and tickler coils collapses and induces a reverse voltage into the emitter circuit, which causes a decrease in the emitter current, and hence a decrease in the collector current. The decreasing current then induces a larger reverse voltage in the feedback loop, driving the emitter current in the opposite direction, that is, to zero or cutoff. Although the emitter current is cutoff, a small reverse saturation current (I<sub>ceo</sub>) flows; this current has essentially no effect on the operation of the circuit, but it does represent a loss which lowers the overall efficiency. In this respect, the transistor differs from the electron tube, which has zero current flow at cutoff.

The discharge of the tank capacitor through the primary winding of the transformer causes the voltage applied to the emitter to rise from a reverse-bias value through zero to a forward bias value. Emitter and collector current again flows, and the previous described action repeats itself, resulting in sustained oscillations.

The tuning capacitors in the r-f and local oscillator tank circuits are mechanically connected, so that whenever one is varied, the other is varied by the same amount. This results in the local oscillator frequency and the r-f frequency always being separated by the same amount at any frequency which may be selected at the input. The amplitude of the local oscillator voltage is approximately ten times as great as the amplitude of the r-f signal, for efficient mixing, and the frequency is selected either above or below the r-f frequency, depending upon the application of the circuit, by an amount which is equal to the i-f frequency.

Since the two applied signals differ in frequency, their voltages are not always in phas with each other. Periodically, these two voltages algebraically add or subtract to produce an amplitude variation at regular

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intervals; it is this periodic amplitude variation in the form of a beat frequency voltage which is of importance. The beat frequency is actually the difference frequency produced by the instantaneous signal voltage as they combine to increase amplitude when approaching an in-phase relationship, and to decrease amplitude when approaching an out-of-phase relationship. When the incoming r-f signal contains amplitude modulated information, the resulting beat frequency also contains the same amplitude modulated information, and varies in accordance with the audio frequency modulating the incoming r-f signal. If the received r-f signal contains frequency modulated information, the beat frequency difference deviates at the same rate as the incoming r-f signal frequency. Thus the characteristics of the resulting i-f are the same as those of the original r-f signal, except that the frequency of the received signal is converted to a lower or higher frequency, depending upon the application.

As a result of the heterodyning action taking place within the elements of the transistor, the output signals present at the collector of **Q1** are as follows: the r-f signal, the local oscillator signal, the sum of the two, and the difference of the two. Since the i-f transformer T2 is freed tuned to the difference frequency, it is this frequency which is inducted into the secondary winding and applied to the succeeding stages. All other signals are bypassed to ground through capacitor C7. The output signal present on the secondary winding of T2 contains all of the information that was present sent on the original r-f signal.

# Failure Analysis.

**General.** When making voltage checks use a vaccum tube voltmeter to avoid the low values of shunting resistance employed on the lower ranges of conventional voltmeters. **Be** careful also to observe the proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output. A no-output** condition can occur from one of the following faults; a defective Q 1, an open Cl, R4, or R3, open windings on T1 or T2, or if capacitors C2 or C7 are shorted. Be sure that the supply voltage is correct before performing any checks. If  $V_{cc}$  is not correct, the trouble is probably not in the autodyne but in the power supply. If an r-f signal is present at the input to the circuit, check for the r-f signal at the base of Q1, if the signal is not present, Cl is defective. If the signal is present on the base of Q1, check for the signal on the collector of Q1; if it is not present, Q1 is defective, R3 is open, C3 is shorted, or T1 or T2 has an open winding. Check R3 and T1 and T2 with an ohmmeter. Check C3 with an incircuit capacitor checker. If the signal is still not present on the collector of Q1, Q1 is probably defective.

**Low Output. A low output** condition may arise from the components in the circuit changing value, the oscillator not being tuned properly, shorted turns on the transformers, a change in bias voltages, a defective Q1, or mismatched impedances.

Check for the proper oscillator frequency on the emitter of Q1. If the oscillator frequency is not present, C3 is defective. If the oscillator frequency is incorrect, tune the tank circuit to the proper frequency. Check for the proper bias voltages on Q1. If the bias voltages are incorrect, check the components in the circuit which have an inproper bias.

# PENTODE MIXER

#### Application.

The pentode electron tube is used as a mixer in superheterodyne receivers to combine, or "mix", the r-f signal, in order to produce the desired intermediate frequency (i-f) output signal.

#### Characteristics.

Requires a separate local oscillator circuit to supply the heterodyning voltage.

Output circuit is tuned to resonate at i-f frequency.

Plate resistance and transconductance are fairly high.

Operates on non-linear portion of  $E_g$ - $I_p$  curve.

Output frequency (i-f) remains constant under normal operating conditions.

Has a relatively high conversion gain and signal to noise ratio.

#### Circuit Analysis.

**General.** The pentode mixer is frequently used in f-m equipment for the vhf band. At frequencies where the screen grid is effective, the pentode mixer provides good isolation between the input and output

circuits. This means reduced input loading and elimination of possible instability as compared with a triode mixer. The oscillator and signal voltages are usually applied to the control grid simultaneously. In this way, a noise figure is obtained which exceeds that of a normal pentode amplifier, but which is much lower than in any of the multigrid mixers.

The pentode has an extremely high conversion transconductance and permits high voltage gain in the mixer stage. The equivalent noise voltage produced by the tube is twice that of a triode mixer of the same transconductance. Because of the high obtainable transconductance of pentodes, the overall performance can exceed that of most triodes. Since the triode has a certain amount of stray coupling between grid and plate circuits, it is at a disadvantage in this respect when compared with the pentode. At the signal frequency, the i-f circuit is capacitive, and this, because of Miller effect, results in a reflected low resistance in the grid circuit. The screen in a pentode effectively stops this loading. With a pentode, cathode injection of the oscillator signal is possible, but this mode of injection increases the effective cathode inductance. Since the input load is proportional to the cathode inductance, cathode injection lowers the voltage gain of the input circuit and also the noise performance. The stability of the oscillator, however, is improved at very-high frequencies, where a low-impedance oscillator load is needed. Unless the oscillator and mixer are loosely coupled, interaction and pulling becomes severs. Interaction of the oscillator and the signal is greatest when they are both applied to the same grid. Similarly, oscillator radiation becomes a greater problem; however, the high transconductance of the pentode permits the use of small oscillator voltages, and radiation is not as great a problem as in a triode.

In operation, the use of a pentode as a mixer is similar to the use of a triode as a mixer. However, the use of a single grid for both the carrier and local oscillator signals sometimes gives rise to difficulties resulting from coupling between the carrier input circuit and the local oscillator circuit. Using the pentode as a mixer, one signal may be applied to the suppressor grid and the other signal to the control grid. By applying the input signals to separate grids, it provides some isolation between the local-oscillator and r-f signals. The value of the cathode resistor is chosen so that it will cause the tube to operate on the non-linear portion of the  $E_{g}$ -I<sub>p</sub> curve (the lower bend of

the response curve). The plate current of the tube then contains the two original input frequencies as well as the sum and difference frequencies of the two original signals. The signal from the local oscillator is normally made much stronger than the r-f input signal so that the percentage of modulation is kept low. The low percentage of modulation required for frequency conversion can be produced in several ways. The method most frequently used depends on the transfer characteristic of a tube or other circuit element. The transfer characteristic expresses the relationship between the signal applied to the input of a device and the signal obtained from its output. The transfer characteristic of a vacuum tube is not a straight line, since the relationship of  $\mathbf{E}_{\mathbf{g}}$  to  $\mathbf{J}$  usually is curved at low values of plate current. Therefore, the vacuum tube is a non-linear device. When the voltage on the grid of a vacuum tube becomes more negative and reaches the plate current cut-off value, no current flows in the plate circuit. Consequently, for an entire range of voltages no current flows in the input circuit. Therefore, the vacuum tube is nonlinear, even if its transfer characteristic is perfectly straight.

circuit operation. The schematic of a typical pentode mixer circuit is shown in the accompanying illustration.



**Typical Pentode Mixer Circuit** 

Transformer T1 consists of an untuned primary winding and a tuned secondary winding; capacitor Cl and the secondary winding of T1 form a resonant circuit at the frequency of the r-f signal to be received. Electron tube V1 is a pentode; the filament (heater) circuit is not shown on the schematic.

After being amplified in the step-up transformer T1, the r-f signal is applied to the grid of mixer tube V1 along with the local oscillator signal which is applied through coupling capacitor C3. Blocking capacitor C2 isolates the contact bias resistor R1 from the signal source. Screen bypass capacitor C4 has a low enough reactance to place the screen at ground potential. Dropping resistor R2 determines **the** screen voltage on the screen grid of V1. An r-f bypass to ground is provided by capacitor C5; and the primary winding of transformer T2 in parallel with tuning capacitor C6 provides a resonant tank circuit for tuning the desired i-f output signal.

With no r-f input, the control grid of V1 has only contact bias. That is, some of the electrons in the space charge have enough velocity to reach the grid. This flow of electrons from cathode to grid causes a small grid current to flow. By making the value of R1 a high resistance (approximately 1 megohm) the resulting voltage drop across it provides a negative bias on the tube, which is called contact-potential bias. Capacitor C2 charges to the voltage developed across RI, holding the tube near cutoff.

Varying capacitor Cl tunes the tank circuit to the desired incoming r-f signal. This signal is amplified in step-up transformer T1, and is applied to the control grid of Vl, along with the local oscillator signal, The amplitude of the local oscillator voltage is approximately 10 times the value of the incoming r-f signal voltage. The local oscillator frequency is either above or below the desired i-f frequency (depending on the circuit application), by an amount which is equal to the desired i-f frequency.

Since the two applied signals differ in frequency, their voltages are not always in phase with each other. Periodically these two voltages algebraically add or subtract to produce an amplitude variation at regular intervals; it is this periodic amplitude variation in the form of a beat frequency voltage which is of greatest importance. The beat frequency is actually the difference frequency produced by the instantaneous signal voltages as they combine to increase amplitude when approaching an in-phase relationship, and to decrease when approaching an out-of-phase relationship.

If the incoming r-f signal contains amplitude modulated information, the resulting beat frequency will also contain the same amplitude modulated information. This information varies in accordance with the audio frequency modulating the incoming r-f signal. If the receiver r-f signal contains frequency

modulated information, the beat frequency difference will deviate at the same rate as the incoming r-f signal frequency. Thus the characteristics of the resulting i-f are the same as those of the orignal r-f signal, except that the frequency of the received signal has been converted to a lower or higher fequency depending upon the application.

As a result of the heterodyning action taking place within the elements of the tube, the output signals present at the plate of VI are: the sum of the two input signrds, the difference of the two input signals, and the two input signals themselves. Since the primary winding of transformer T2 is tuned, it will present a high impedance to the desired i-f frequency. This frequency is passed by the tank circuit consisting of the primary winding of T2 and variable capacitor C6, and a voltage is induced in the secondary winding which varies in amplitude in accordance with the amplitude of the orignrd r-f signal. All other signals are bypassed to ground through capacitor C5. The output signal voltage developed across the secondary windings of T2 then contains all of the information present on the desired r-f input signal.

One variation of the pentode mixer circuit is to use cathode injection of the local oscillator signal, but using this mode will increase the effective cathode inductance. Because the input is proportional to the cathode inductance, cathode injection will lower the voltage gain of the input circuit and also the noise performance. Another variation of the pentode mixer circuit uses the suppressor grid for one of the inputs and the control grid for the other. This provides a slight amount of isolation between the two inputs.

# Failure Analysis.

No Output. A defective tube, an open or shorted Cl, C5, or C6, or a defective T1 or T2 can cause a no-output condition. Check the plate of V1 with a high resistance voltmeter. If plate voltage is not present, use an ohmmeter to check the continuity of the primary winding of T2 and to check Cl, C5, and C6 for a shorted or open condition. If the previous checks fail to locate the trouble, the circuit supplying the plate voltage is probably at fault.

Low Output. A low output would normally be caused by a defective or weak VI, or a low filament or plate voltage, or if the i-f and r-f tank circuits are not tuned to the proper frequencies. A weak local oscillator voltage can cause a low output. Check the filament and plate voltages with a VTVM. If they are

not normal, refer to the procedure in the previous paragraph. If they are normal, check the amplitude of the local oscillator signal. If it is low, check C3 with an in-circuit capacitor checker. If the output is still low, the trouble is probably in the local oscillator circuit.

Distorted Output. A distorted output can be caused by a defect in nearly any component in the circuit. With an oscilloscope, check for an r-f signal on the secondary winding to TI. If the r-f signal is not present, check the windings of TI with an ohmmeter for continuity. Should the windings not be defective, the trouble lies in the preceding stages and the mixer is probably not defective. If the signal is present on the secondary winding of T1, check for the presence of the local oscillator signal on the high side of C3. If it is not present, the local oscillator is at fault. If it is present, both the r-f and local oscillator signals should be present on the control grid of VI. If the local oscillator signal is not present, C3 is defective. If the r-f signal is not present, C2 is defective. If both the r-f and local oscillator signals are present on the control grid of V1, Tube VI is probably defective. If the output is still distorted, check the plate and screen voltages with a VTVM, If both voltages are low, check the output of the plate voltage supply. If it is low, the trouble lies in the plate supply. If it is normal, and the screen voltage is low, check R2 with an ohmmeter, and C4 and C5 with an in-circuit capacitor checker and the primary winding of T2 with an ohmmeter. If the output is still not present, check the secondary winding of T2 with an ohmmeter.

#### **BALANCED MIXER (ELECTRON TUBE)**

#### Application.

The balanced mixer is used in receiver circuits to combine or "mix" the r-f signal from the local oscillator with the incoming r-f signal, to produce the desired intermediate frequency (i-f) output.

#### Characteristics.

Uses two triodes connected in push-pull. Fixed, class "C" bias is used.

Requires a separate local oscillator circuit to supply the heterodyning voltage.

Provides amplification, which is referred to as conversion gain.

I-F frequency remains the same for any selected input frequency.

# Circuit Analysis.

**General.** The purpose of the mixer stage is to convert the incoming r-f frequency, usually into a lower frequency, which contains the same characteristics (modulation) as the original r-f frequency. This lower output frequency, called the intermediate, or i-f frequency, remains the same, regardless of the frequency of the r-f signal received.

The local oscillator signal is applied in parallel to the grids of tubes VI and V2 while the r-f signal input is applied in series with the local oscillator input so that the r-f input alternately aids and opposes the local oscillator signal.

By operating both the tubes class "C", and by applying two different frequencies to the input of the tubes, a mixing, or heterodyning action occurs, and the result at the plates is a number of different frequencies, which consist primarily of the sum and the difference of the two inputs, and the two originally applied signals.

Since the tubes are connected for push-pull operation, the outputs aid each other at the output transformer, which is usually tuned to the difference frequency, and for this reason, a higher amplification factor is obtained.

**Circuit Operation.** This accompanying circuit diagram illustrates a typical balanced mixer.



**Typical Balanced Mixer** 

The input r-f signal, applied to the primary of Tl, is selected with tuning capacitor Cl, which is mechan-

ORIGINAL

ically connected to the tuning capacitor in the 10CSI oscillator. The secondary of T1 is split, and the local oscillator signal is applied through transformer T2 to the center tap of the split secondary. Capacitor C2 provides an effective ground for the center tap of the split secondary, and C3 provides a ground return for the secondary of T2 and keeps r-f out of the bias supply. Resistor RI establishes Class C bias on tubes V1 and V2, and capacitor C4 is an r-f bypass to ground. Resistor R2 is a plate voltage for the tubes. Capacitors C5 end C6 in the output circuit are used to tune the primary of the output transformer, T3, to the desired difference frequency.

With no r-f signal applied at transformer T1, and the signrd from the local oscillator applied at transformer T2, the voltages applied to the grids of V1 and V2 are in phase with each other.

By applying a signal at the input transformer Tl, voltages are developed in the secondary windings L2 end L3, which are equal and opposite with respect to each other, because of the grounded center tap arrangement. Thus, when the grid of V1 is positive with respect to its cathode, the grid of V2 is negative with respect to its cathode, and conversely.

Capacitor Cl and the tuning capacitor in the local oscillator are mechanically connected, so that whenever the value of Cl is changed to operate the r-f tank at a particular frequency, the local oscillator tank is also changed automatically by the same amount. This results in the local oscillator frequency and the r-f frequency always being separated by the same amount at any frequency which may be selected at the input. The amplitude of the local oscillator voltage is approximately ten times as great as the r-f signal amplitude, for efficient mixing, and the frequency is selected either above or below the r-f frequency, depending upon the application of the circuit, by en amount which is equal to the i-f frequency.

When both the local oscillator and the r-f inputs are applied simultaneously, the following action results.

Assume that the local oscillator signal end the r-f input signals on the grid of V1 are positive and in phase. A voltage is developed in the plate circuit which is the algebraic sum of the two applied signals. At the same instant, a positive local oscillator signal and a negative r-f input signal is applied to the grid of V2. The result in the plate circuit of V2, therefore, is also a signal which is the algebraic sum of the two inputs. Since the two inputs are 180 degrees out of phase with each other, they subtract, and the signal at the plate of V2 is smaller in amplitude than the signal at the plate of VI. Because the tubes are connected in push-pull, the two out-of-phase r-f signal inputs add in the primary of T3, and the two in-phase local oscillator components subtract. The local oscillator components are of equal amplitude, and of opposite polarity at the plate, so their algebraic difference is O volts. The two r-f signals are in phase, and they add in the plate circuit, the result being a positive going signal.

Let us consider the opposite set of circumstances. As the polarities of the local oscillator and the r-f signals at the grids of the tubes change, the signal in the plate circuit also changes. When the signal from the local oscillator becomes negative on the grids of the tubes, and the r-f signal input is such that it applies a negative signal on the grid of Vl, and a positive signal on the grid of V2, the following results occur. Because both of the signals on the grid of V1 are in phase, they add algebraically, and the result at the plate of V1 is a negative going signal which is the sum of the two input signals. The two signals on the grid of V2, however, are out of phase, and the result at the plate is the algebraic difference. Because the local oscillator component is cancelled out in the plate tank circuits, the resultant output is a negative going signal which is the algebraic sum of the two r-f inputs.

The local oscillator signal is of a different frequency than. the r-f input, so their phase relationship with each other is constantly varying. The closer they are in phase with each other, the greater is the output, and the further out of phase they are, the smaller the output. These variations in the amplitude of the plate current occurs at the desired difference frequency, and it is this difference frequency or i-f to which the plate tank circuits are tuned. Since the tanks present a high impedance to the i-f, a changing field is developed around the primary winding, which induces an output in the secondary winding.

The local oscillator component is eliminated in the plate circuit because they are of opposite polarity, and since they always are equal in amplitude and opposite in polarity, they cancel. All other frequencies in the plate circuit are bypassed to ground through capacitor C4 without being developed. For a detailed description of heterodyning action, refer to the introduction to this section of the Handbook.

If the received r-f signal contains amplitude modulated components, the beat frequency also contains similar amplitude modulated components, which vary in accordance with the audio frequencies modulating the original r-f signal. If the received r-f signal is frequency modulated, the beat difference will deviate in frequency at the same rate as the original r-f signal. Thus, the characteristics of the i-f signaf are the same as those of the original received signal, except that the frequency of the received signal is converted to a lower frequency.

#### Failure Analysis.

**No Output.** The only components which will cause a no output condition to exist is an open R2, a shorted C4, or a defective T3. Check the value of R2 with an ohmmeter, and check C4 for an open or a short with an ohmmeter. Check the windings of T3 for continuity. Note that one defective tube will not cause a no-output condition to exist. Both tubes must be defective.

Low Output and Other Conditions, If the output appears to be low when observed on an oscilloscope, it could be simply a heterodyned signal of insufficient amplitude, or an output which is the result of one or the other of the input signals being coupled through the mixer stage without being mixed, and thus useless. Determine first of all whether or not the mixer is at fault by checking for the r-f input and the local oscillator input on their respective transformer primaries. Remember to disable the r-f amplifier when checking the local oscillator input, and the local oscillator input when checking the r-f input. If either one of them are not present, the mixer stage is probably not faulty, and the output will most likely be restored with the renewal of the missing input signal. If each signal is present on its respective primary, check the continuity from the grid of VI to the grid of V2 with an ohmmeter. If it is an open circuit, the secondary of T1 is probably open. Also check the secondary of T2 for continuity with an ohmmeter. Check C2 for a possible short, as this would place a short across the secondary of T2. Check C3 for an open, and RI for proper value with an ohmmeter. If the above components check good, and the proper signals are applied to their respective primaries, these signals should be present on the grids

of the tubes. If the trouble still exists, one of the transformers is probably defective.

If both signals are present on each grid, and the output is low, the tubes are probably defective. Do not overlook the possibility of the tuned circuits being misaligned. If the low output still exists, check the bias supply and the plate voltage supply to be certain that voltages are normal. Check R1 and R2 with an ohmmeter for proper value. Check C4, C5, and C6 for an open or a short with an ohmmeter, and the primary and secondary of transformer T3 for continuity. If above checks fail to locate the trouble, check all capacitors with an in-circuit capacitor checker, and double check all transformers.

#### PENTAGRID MIXER

#### Application.

The pentagrid mixer is used in modern superheterodyne receivers as a frequency converter. Incoming r-f signals are combined with signals from a local oscillator to produce an intermediate frequency (i-f).

# Characteristics.

Offers good selectivity.

Serves both as a frequency converter and a high gain amplifier.

Signal-to-noise ratio is poor.

Requires a separate local oscillator to supply the heterodyning voltage.

Uses two input control grids to provide electron coupling.

Operates with either cathode-self, fixed, or avc bias voltage.

#### Circuit Analysis.

**General.** The functional operation of the pentagrid mixer is very similar to that of other mixer circuits discussed previously in this handbook. R-f and oscillator voltages are injected into the tube and added algebraically. The fundamental frequencies, along with their sum and difference frequencies, appear across the output circuit. The output circuit is a parallel resonant tank, tuned to the i-f. The desired i-f signal is transformer coupled into the next stage.

The primary difference between the pentagrid mixer circuit and other mixer circuits is the input arrangement. In the diode, triode, and pentode mixer the r-f and oscillator voltages are inserted on the same tube element, allowing for greater interaction between input signals. In the pentagrid mixer, r-f and oscillator signals are inserted on separate control grids, isolated from each other and the plate by screen grids. Consequently, the frequency pulling effects and signal interaction, common to other mixer circuits, is virtually eliminated.

**Circuit Operation.** Before discussing operation of the pentagrid mixer it will be helpful to review the operation of the pentagrid tube.

The pentagrid tube consists of a plate, cathode, filaments and five grids, hence the name pentagrid. Two of the grids are used as control grids (C1 and G3), two are used as screen grids (G2 and G4), and the fifth is used as a suppressor grid. For all practical purposes the gain of the pentagrid tube is comparable to that of the pentode, however the introduction of an extra screen grid increases the partition noise, and consequently, the circuit noise.

The screen grids are operated at a positive voltage and serve as **the** accelerating anodes for electrons leaving the cathode. However, the electrons strike the plate of the tube with such force that they bounce off (secondary emission) and form a space charge around the positive screen grid (G4).

The space charge greatly limits the plate voltage swing, so a negative grid (G5) is placed between screen and plate, and its negative charge diverts electrons back to the plate,

By following the above discussion it can be seen that the pentagrid tube plate current is made independent of plate voltage. In fact, the plate voltage may swing as low as, or lower than, the screen voltage without serious loss of amplifier gain capabilities. In mixer circuits gain (gin) is referred to as "conversion transconductance" and represents the quotient of i-f output current divided by r-f input voltage; or, conversion transconductance = Iif/Erf. In pentagrid tubes conversion transconductance may run as high as 500 micromhos.

In the mixer circuits previously discussed, such as the triode and pentode mixer, the r-f and oscillator signals are injected on the same control grid. Thus the r-f input circuit is "seen" by both inputs and stray coupling induces oscillator detuning, or frequency pulling. In pentagrid mixers, r-f and oscillator signals are simultaneously injected on separate control grids (G1 and G3). As stated previously in this discussion, G2 acts as an electrostatic shield between the input

elements, and is effectively grounded at r-f frequencies by capacitor C3. Thus, the input circuits are shielded from each other, and interaction caused by stray capacitive coupling is virtually eliminated. Hence the instability of operation and frequency pulling effects common to other mixers is not experienced in the pentagrid circuit.

Thus, in the pentagrid mixer the gain is high, and the input grids are also isolated creating a stable circuit free from pulling effects.

A typical pentagrid mixer circuit is illustrated in the accompanying schematic diagram.



**Pentagrid Mixer** 

Fixed bias from an external bias supply is applied to the control grid Cl through decoupling resistors R1 and coil L2 and to G3 grid via R3 and R4. The tube is biased below cutoff with no input from the r-f and local oscillator, so that in the absence of a signal the tube will not conduct. Capacitors C2 and C6 are r-f bypass capacitors which prevent r-f signals from entering the bias supply.

Dc voltage is applied to the plate and screen through plate decoupling resistor R5 and coil L3, and through screen resistor R2. Capacitors C3 and C5 are also r-f bypass capacitors to prevent r-f from entering the power supply.

With no r-f signal applied to G1, and oscillator voltage applied to G3 the tube begins to conduct, with the plate current varying at the oscillator frequency; however, due to the highly selective tuning of the output tank comprised of L3 and C4, the current variations are by-passed through the tank to ground via C5 and no output is realized at L4.

As the receiver is tuned to the desired r-f frequency the r-f signal is impressed across coil L1. Transformer action takes place and the signal is transferred inductively from the primary to secondary winding L2. Coil L2 and capacitor C 1 form a parallel resonant tank between the control grid (Gl) and cathode, tuned to the selected r-f frequency. Capacitor C2 by-passes extraneous frequencies to ground and prevents their entering the bias supply.

As r-f and oscillator signals appear simultaneously on G1 and G3, respectively, plate current increases and the tube operates just above cutoff on the non-linear portion of the Eg-Ip curve (the lower bend in the response curve).

Harmonic distortion, caused by operating the tube nonlinearly, results in mixing action within the tube. The two original frequencies, plus their sum and difference frequencies, appear between the plate and ground across L3, and C4. The parallel resonant tank, formed by L3 and C4, selects the difference frequency and transformer action occurs between the primary or secondary of T2, resulting in the i-f appearing across L4. The unwanted frequencies (the two originals and their sum) are bypassed through C5 to ground. Capacitor C5 is of a circuit value which will bypass the high frequency components in the plate, but not the relatively low frequency i-f. Since the i-f tank offers a high primary load impedance, only the i-f signal is developed across it and is inductively coupled to the secondary or output winding. The output then consists of a signal at the intermediate frequency which contains all the original signal modulation and any hum modulation from the local oscillator, if not adequately plate faltered.

#### Failure Analysis.

**No Output.** Before troubleshooting the mixer stage it is necessary to ascertain that r-f and local oscillator signals of proper amplitude and frequency are present at the inputs to the mixer circuit. The operation of the mixer circuit depends upon the heterodyning of these two signals and if either is absent an i-f output will not appear across L4. An oscilloscope, equipped with a high frequency-high impedance probe, must be used to check the presence of r-f and oscillator signals on L1 and G3 respectively.

After assuring the presence of input signals, check the dc and bias supply output voltage for nominal output and ripple as directed in the equipment handbook.

If power supply voltages are present and of correct amplitude, check each component visually for signs of overheating. Also check connections for good electrical and mechanical contact.

Use a vacuum tube voltmeter to check each tube element on the base of the socket. If plate, filament, or screen voltage is absent the tube will not conduct, resulting in no output. Remove power and check power supply plate decoupling resistors R2 and R5 and coil L3 for correct dc resistance. Also check capacitors C3 and C5 with a in-circuit capacitor checker to determine if they are shorted or leaky. If bias voltage is appreciably off value the tube will either be cutoff (increased bias) or saturated (decreased bias). Check bias resistors R1, R3, and R4 and coil L2 for correct dc resistance. Use an in-circuit capacitor checker to check capacitors C2 and C6 for a shorted or leaky condition.

If all circuit components are within tolerance and the presence of both r-f and oscillator signals is verified, the tube is most likely at fault.

If still no output is obtained, check the tuning of the input and output circuits as directed in the equipment handbook. If either tank will not tune, carefully check the "capacitor and coil associated with the tank. Remove power and use an ohmmeter to check the primary and secondary windings of T1 and T2 for the correct dc resistance. If the resistance has increased the Q of the circuit will be decreased and output of the desired frequency may be impossible to obtain.

Low or Distorted Output. Check the r-f oscillator input circuits for proper amplitude and frequency with an oscilloscope. Be especially watchful for distorted input waveforms caused by noise, hum, defective coupling, etc. If input waveforms are correct and free from distortion, check the waveform at the plate of V1 (use a 30-100 pf, 250 v dc blocking capacitor in series with the probe).

If the waveform appearing on the plate is clipped or small in amplitude, check for correct dc operating voltages on the tube elements. Check bias voltage first, as increased bias will cause abnormal plate voltage due to decrease conduction. If bias voltage is incorrect check resistors R1, R3 and R4 and coil L2 for correct dc resistance. Check r-f by-pass capacitors, C2 and C6, for shorts using an in-circuit capacitor checker. If bias voltage is correct and plate voltage is low check the dc resistance of R5 and L3. Also check C5 for a shorted or leaky condition.

If all voltages are correct and the output of the tube is still weak, the tube is probably defective.

If the output of V1 appears normal and the output of the mixer stage is still weak or distorted, check the tuning of the output tank circuit. If the tuning of capacitor C4 has shifted appreciably the band pass of the tank circuit will be greatly reduced and the i-f frequency will be suppressed.

# PENTAGRID CONVERTER

#### Application.

The pentagrid converter is used in modern superheterodyne receivers to convert radio frequencies (**r**-**f**) to intermediate frequencies (i-f) by heterodyning (mixing) the received r-f signal with a locally generated signal.

# Characteristics,

One tube functions as both oscillator and mixer. Output is stable up to and including the h-f band. Signal-to-noise ratio is poor.

Offers high gain (conversion transconductance).

Oscillator section is electron-coupled and isolated from input signls to minimize "pulling effects".

# Circuit Operation.

**General.** The pentagrid converter is a low cost, high gain, frequency converter with excellent stability, commonly used for frequencies up to and including the h-f band. Perhaps the most frequent application of the pentagrid converter is in the standard acdc house-hold receiver where, due to the high gain characteristics of the pentagrid tube, an r-f amplification stage is not required. By combining the r-f amplifier, local oscillator and mixer into one tube the over-all cost of the receiver is greatly reduced without sacrificing quality; however, in more sophisticated receivers where greater sensitivity and selectivity are desired, the pentagrid converter is usually preceded by at least one stage of amplification.

Basically, the pentagrid converter can be divided into two separate circuits; an electron-coupled oscillator (formed by the cathode, inner control grid, and screen grid) and a conventional pentagrid mixer with separate grid injection.

CIRCUITS

The tube is biased below cutout by a shunt grid leak bias network, and plate current only flows when the oscillator signal is large enough to overcome the heavy negative bias. Thus, conduction takes place for the small amount of time that the oscillator signal is at its peak amplitude. This breaks the plate current into pulses varying at the oscillator frequency. As the receiver is tuned to the desired r-f frequency, the r-f voltage injected on the outer control grid is added algebraically with the oscillator signal so that plate current now follows their combined sum voltage.

Operating the tube just above cutoff on the non-linear portion of the Eg-lp curve causes harmonic distortion. Consequently, in addition to the two original frequencies, their sum and difference frequencies are now present in the plate circuit.

A parallel resonant tank circuit is placed in the plate circuit and is tuned to the desired i-f, which can be either the sum or difference of the two original frequencies. Transformer action transfers the selected i-f to the input of the next stage. The two original frequencies and their sum or difference (depending upon which frequency was selected for the r-f) are by-passed to ground through the relatively low impedance offered by the screen bypass capacitor.

**Circuit Operation.** A typical pentagrid coverter circuit is illustrated in the following schematic diagram. Pentagrid converters are occasiomlly modified to function in special circuits, consequently, circuit arrangements which vary from the accompanying schematic may be incorporated in different receivers; however, the functional operation remains basically the same.



**Pentagrid Converter** 

R-f signals arriving at the antenna are impressed across L1 and coupled across transformer T1 to the secondary tuned tank formed by inductor L2 and capacitor Cl. C2 is a trimmer capacitor used to track the high frequency end of Cl during alignment. The selected r-f frequency is inserted into the converter tube on the outer control grid, G3.

Oscillator signals are developed in the grid tuned tank formed by inductor L3 and capacitor C4. C5 is a

trimmer capacitor used for tracking the high frequency end of the main tuning capacitor C4, and C6 is a padder capacitor used to track the low end of C4. The oscillator signals are coupled to inner control grid G1 through coupling capacitor C3 which, working id conduction with RI, develops the shunt grid leak bias voltage for the tube.

Conduction takes place when the positive peaks of oscillator signal overcome the class C bias, causing plate current to flow in pulses at oscillator frequency. The pulsed electron stream is further modulated by the r-f signal and both frequencies, plus their sum and difference frequencies appear in the plate circuit. The parallel resonant tuned tank formed by inductor L4 and capacitor C8 acts as a plate load, and is tuned to the desired i-f frequency. Capacitor C7 prevents r-f from entering the power supply.

The output is taken across the parallel tuned tank formed by inductor L5 and capacitor C9 which further selects the desired i-f frequency.

The schematic diagram shown incorporates an electron-coupled Hartley oscillator as the frequency generating section. For illustrative purposes the oscillator portion of the pentagrid converter has been re-drawn in the following schematic diagram. Notice that the screen grids (G2 and G4) form a composite oscillator anode. A detailed operational description of the oscillator section is included in the following paragraphs.



**Oscillator Section** 

In frequency converter circuits it is desirable to have as nearly a stable oscillator injection signal as possible with little variation in frequency or amplitude. In the pentagrid converter this need was intensified by combining two separate functions into one tube envelope. It is known that variation in the plate load of conventional oscillator circuits causes considerable variation of oscillator frequency. Hence, the need for an oscillator whose output circuit is completely isolated from the tuned grid circuit.

In the electron coupled Hartley oscillator, the internally connected screen grids are supplied with a dc potential and act as a composite anode for the oscillator section of the pentagrid converter. Electrons are attracted from the cathode and flow towards the screen grids (anode); however, because of the relatively large spacing between the wires of the screen grid, most of the electrons pass on through to the plate element of the pentagrid tube. Consequently, only a small amount of screen current flows and the screen voltage remains comparatively constant. It can be seen then that electrons leaving the cathode "see" a relatively constant load because of the stable anode potential on the screen grid, but the actual output circuit of the oscillator is in the pentagrid tube plate. The screen grids are held at r-f ground potential by r-f by-pass capacitor C7 whose impedance is very low at r-f. Thus the only coupling which exists between the input and output circuit is the electron stream, hence the name "electroncoupled" oscillator.

To sustain oscillations in the grid circuit it is necessary to "feedback" an in-phase portion of the output signal. In the electron coupled Hartley the tapped inductor acts as an autotransformer to accomplish this purpose. For illustrative purposes the grid and cathode circuit has been redrawn in the accompanying schematic diagram.



**Simplified Oscillator Circuit** 

The inductor L3 is divided into two sections which will be designated L3k (cathode winding) and L3g, (grid winding). It can be seen that the total inductance former by L3, in parallel with the total capacitance of C4, C5 and C6, forms the frequency determining tank circuit. The solid lines represent the initial flow of current (charge path) and the broken lines represent the reverse of current (discharge path).

At the instant power is applied to the tube, zero bias exists on the control grid and the tube readily conducts. For the following discussion it will be helpful to remember that cathode current "follows" plate current. Increased cathode current develops a voltage potential across inductor L3 and capacitors C4, C5 and C6, represented by CT, begin to charge (O to 1 on the sine wave). At point 1, the capacitors have charged to approximately the applied voltage and begin to discharge back through inductor L3, (point 1 to 2) setting up a magnetic field, (point 3). The magnetic field begins to collaspe, (point 3 to 4) recharge capacitor CT (point 5) and the cycle repeats itself; however, notice that the voltage at point 5 is less then that at point 1. This is due to inherent circuit losses (coil resistance, etc.) and eventually, after a few more cycles, the oscillations will dampen out entirely. Thus, it can be seen that an in-phase signal of sufficient amplitude to cancel out circuit losses is necessary to sustain oscillations.

For simplification, bias voltages are disregarded in this discussion and will be discussed later in the text.

The positive going grid (O to point 1) causes an increase in plate (and cathode) current, resulting in an increased voltage across inductor L3k,  $180^{\circ}$  out of phase with the grid signal. The mutual inductive action of the autotransformer L3g and L3k produces another  $180^{\circ}$  phase shift, so that regenerative (in-phase) feedback is accomplished. The feedback voltage will be relatively small due to the turns ratio of the transformer but it is of sufficient amplitude to reinsert and compensate for any circuit losses. Thus, the flywheel effect of the tuned tank circuit, aided by the mutually induced voltage from L3k, impresses a linear sine wave on capacitor C3, which is part of the shunt grid leak bias circuit.

As has been previously mentioned, it is required that a mixer operate over the nonlinear portion of the Eg-Ip curve, thus the tube must be biased below cutoff. The grid leak bias circuit comprised of resistor RI and capacitor C3 performs this function and will be discussed in detail in the following paragraphs.

The oscillator input signal arriving from the grid tank circuit is impressed on the tank side of capacitor C3. On the positive swing of the oscillator input signal the grid is driven positive, causing current to flow from cathode to grid through the internal gridcathode resistance, Rgk (The value of Rgk is considerably lower than that of the parallel resistance R1 so the major portion of the current will flow through Rgk) and C3 charges rapidly, placing a negative voltage on the control grid. As the oscillator signal swings negative, grid current ceases to flow and capacitor C3 begins to slowly discharge through resistor R1. The value of R1 is considerably larger than Rgk, so discharge time is longer than charge time. Before C3 can become fully discharged the oscillator signal begins to swing positive and grid current flows again, charging C3 to a higher potential and placing more bias voltage on the control grid. Eventually, after a few more cycles of oscillator signal, the charge on C3 becomes stabilized and grid voltage remains at a constant level.

If the time constant of the R-C bias network is too long, capacitor C3 will eventually become fully charged, placing the tube in absolute cutoff and no current will flow, consequently, oscillations will cease. Hence, the value of grid leak resistor R1 is critical. It must be large enough to develop a sufficient negative voltage for cutting the tube off and small enough to allow a partial discharge of C3 before the next oscillator cycle begins. Thus, by using the correct value of grid leak resistance the circuit may be designed to cut off for 9070 of the time only 10% (the positive peak) of the signal causing tube conduction.

The positive peaks of the oscillator signal brings the tube out of cutoff and modulates the electron stream in pulses. R-f signals arriving at the antenna are impressed across inductor LI, the primary winding of T1. The signals are transformer coupled to the secondary winding, inductor L2. Capacitor Cl and L2 make up a parallel resonant tank tuned to the selected r-f frequency. Notice that Cl in the r-f section and C4 in the oscillator section are mechanically ganged, and varying one will cause the other to vary by an equal amount, hence the oscillator and r-f stage are always, theoretically, separated by the intermediate frequency. However, on the extreme ends of the tuning range the variable capacitors become somewhat non-linear and if proper tracking is to be acquired it is necessary to insert trimmer and

padder capacitors to "fine tune" the local oscillator and r-f sections. Capacitors C2 and C5 are "trimmer" capacitors used to track the low frequency end of Cl and C4 respectively and C6 is a "padder" capacitor used to track the high frequency end of capacitor C4.

The frequency selected by Cl and L2 is applied to the outer control grid, G3. The r-f signal grid is electrostatically shielded from the oscillator grid by screen grid G2 which is at ground potential. Consequently, very little electron coupling exists between the r-f and oscillator circuits and frequency pulling effects are virtually eliminated,

The electron stream, varying at oscillator frequency, is further modulated by the r-f signal and plate current begins flowing at a rate, as determined by the algebraic sum of the two signals. Harmonic distortion, caused by operating the tube non-linearly, produces various frequencies (the origiml rf and oscillator signals and their sum and different frequencies) in the plate circuit. The fixed tuned output tank comprised of L4 and C8 is tuned to the desired i-f, which is usually the difference frequency, and inductively couples the selected i-f to the secondary winding tuned circuit comprised of L5 and C9.

The unwanted original frequencies and their sum frequency are shunted to ground through r-f by-pass capacitor C7.

# Failura Analysis.

**No Output.** Before troubleshooting the converter stage check each component visually for signs of overheating. Also, check all component connections for good electrical and mechanical contact. Check the mechanical coupling between the ganged capacitors C4 and Cl. If the coupler has loosened the oscillator and r-f signals will not be separated by the desired i-f frequency and no output will be obtained from the converter circuit.

The output tuned tank comprised of L4 and C8 is tuned to the desired i-f which is a mixture of the locally generated oscillator signal and the received r-f signal. Thus, if both input signals are not present on their respective control grids the tube will not operate properly, resulting in no output. Before further troubleshooting is accomplished the presence of both input signals must be ascertained. It is important to remember that oscillator signals are dependent upon tube conduction.

To check the r-f signal, connect an oscilloscope (equipped with a high impedance-high frequency

probe) between the outer control grid and ground. If receivers where the converter is not preceded by an r-f amplifier the r-f signal may not be of sufficient amplitude to produce an indication on the oscilloscope. If this is the case a signal generator, adjusted to the selected r-f and loosely coupled to the antenm loop, should produce an indication on the oscilloscope. If no signal is obtained after performing the preceding checks, use an ohmmeter to check inductors L1 and L2 for the correct dc resistance. Also, check capacitors Cl and C2 for a shorted condition using an in-circuit capacitor checker. In receivers where an externa. antenna is used the antenna transmission line must be checked for a short or open.

Since grid leak bias voltage depends upon the applied oscillator input signal, both the bias voltage and oscillator signal may be checked simultaneously by connecting a vacuum tube voltmeter between the inner control grid and ground. If no voltage is present on the control grid, remove power and check the dc resistance of inductor L3 using an ohmmeter. Also check capacitors C4, C5 and C6 for a shorted condition. If the components forming the oscillator tank appear normal, use an in-circuit capacitor checker to check capacitor C3 for a shorted or leaky condition. If C3 is defective the bias on VI will decrease and the tube will be saturated. Also check resistor RI using an ohmmeter. If R1 has increased in value the bias on V1 will increase, cutting the tube off.

If both signals are present on the control grids, check the plate and screen elements for the correct dc potential. If plate or screen voltage is abnormal check inductor L4 for nominal dc resistance using an ohmmeter. Also check capacitor C7 using an incircuit capacitor checker.

If all the circuit components are found to be within tolerance check inductors L4 and L5 for the exact d-c resistance as specified in the equipment handbook. Also, use an **in-circuit** capacitor checker to check C8 and C9 for a shorted condition.

If it is verified that the circuit components are within tolerance and the correct voltages are applied to the tube elements and a no-output condition still exists, tune the primary and secondary of the output transformer T2 as directed in the equipment handbook.

Low or Distorted Output. A low or distorted output in converter stages could be caused by

numerous defective components within the circuit; however, the two most likely causes would be either distorted input signals or improper bias voltage.

First, check the r-f oscillator signals for correct amplitude and frequency using an oscilloscope equipped with a high impedance-high frequency probe. Be especially watchful for distorted waveforms caused by noise, hum, clipping, etc.

If the quality of the received r-f signal from the antenna (or r-f amplifier) is questionable, disconnect the antenna and inject the signal from an r-f signal generator and recheck the signal applied to the control grid. If the sigml is distorted, check the tuning of the grid tank. Also, carefully inspect the grid tank ground connections for good electrical contact. A loose or intermittent ground comection would introduce hum and distort the signal.

If the oscillator signal shows signs of distortion, check the d-c resistance of tapped inductor L3 and resistor RI. Use an **in-circuit** capacitor checker to check capacitor C3 for a shorted or leaky condition.

If the input waveforms present on the control grids appear to be normal, check the output waveform in the plate circuit. (Use a d-c blocking capacitor in series with the oscilloscope probe). If the output waveform is clipped or small in amplitude, check the cathode and inner control grid for proper operating voltages. A noticeable 60 Hz hum in the output waveform could be caused by a cathode to heater short or high grid leakage.

If the waveform at the plate appears normal, but the output of the converter remains distorted, tune the output transformer T2 as specified in the equipment handbook.

#### PART 11-3. AGC CIRCUITS

# AGC (AVC) CIRCUITS

#### General.

AGC (automatic gain control), frequently referred to as *AVC* (automatic volume control), is a control circuit that automatically changes the over-all gain of a receiving system in a manner which is inversely related to the strength of the received carrier signal. The terms AGC and *AVC* have been used interchangeably, and some confusion has resulted from this practice. The exact use of one or the other term is determined principally by the type of circuit(s) being controlled or by the type of useful output obtained from the controlled system.

Originally, the circuit was used extensively in radio and communications equipments where the useful output obtained was an audible signal heard in headphones or from a loud speaker; the circuit was therefore called *automah"c volume control*. However, basically the same circuit has also been employed to provide automatic control of amplification, or gain, in other electronic equipments. Since these similarly controlled equipments produce a useful output that does not necessarily result in an audible output signal, the term volume does not apply; in this case the term gain is technically correct. For example, if the basic circuit is used to control the amplification (gain) of the r-f and i-f amplifier stages in a communications or broadcast receiver, it is frequently still referred to as an A VC circuit; on the other hand, if it is used to control the amplification (gain) of the i-f amplifier stages in a radar receiver, or the r-f and i-f stages in a television receiver, it is called an AGC circuit. In either example the electronic function is the same-to control an output signal in accordance with the strength of the input carrier signal.

In the paragraphs to follow and throughout this section, the distinction between AGC and AVC will not be made. The term AGC (automatic gain control) will be used to designate the circuit that controls useful output, regardless of whether it is in the form of a visual (video) display or similar indication, or an audible signal.

The basic AGC circuit is intended to maintain the output of a receiving system nearly constant within relatively narrow limits, and must do so as the input carrier signal level varies over a considerable range. AGC action is normally accomplished by developing a dc control voltage which is proportional to amplitude of the received carrier signal, and then applying this voltage in the form of bias to regulate the gain of one or more remote cutoff amplifier stages within the receiving system.

#### Types of AGC Circuits (Electron Tube).

**AGC** circuits vary somewhat because of the overall gain characteristics required of the receiving system. However, most electron tube AGC circuit configurations fall into one of three general classifications: simple AGC, delayed AGC, and amplified and delayed AGC. These three classifications of AGC circuits are described briefly in the paragraphs which follow.

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**Simple AGC. A** simple AGC circuit and a diodedetector circuit (described in the Detector Section of this Handbook) are very similar in many respects. For this reason, the AGC circuit and the signal detector circuit of a receiving system are frequently combined within a single stage. The accompanying block diagram illustrates a simple AGC system; this AGC system makes use of a negative dc control voltage obtained directly from the signal detector output, since the rectified voltage produced by the detector is proportional to the amplitude of the received carrier.



Simple AGC System

The resulting d-c voltage obtained from the detector circuit is filtered by an R-C circuit to remove any amplitude modulation components present in the detector output, and is then applied as bias to the control grid of each stage to be controlled in the receiving system. The time constant of the R-C filter is long enough to remove the lowest modulation frequencies from the dc voltage, but short enough that a change in dc bias level will respond to moderately rapid changes in received signal strength due to signal fluctuations, fading, etc. The simple AGC circuit is employed in many typical AM superheterodyne receivers which use a diode-type detector; it is also employed in some FM receivers which use a ratiotype detector.

**Delayed** AGC. The term delayed AGC is used to denote a voltage delay, and should not be confused with a time delay. The simple AGC system just described is effective on all received signals, from the weakest to the strongest. It has the disadvantage of developing an AGC voltage even for very weak received signals and, as a result, the sensitivity of the receiver to weak signals is reduced considerably. Therefore, in order to increase sensitivity and enable the receiver to respond to weak signals, it is desirable to provide a means of delaying the application of AGC voltage until the received signal reaches a predetermined value, sometimes called the *threshold* 

level of AGC. The accompanying block diagram illustrates a typical delayed AGC system.



Simple Delayed AGC System

The delayed AGC system makes use of a fixed delay voltage applied to a separate AGC detector. The delayed AGC detector must be a separate diode, independent of the signal detector (demodulator) diode, because the fixed delay voltage prevents the AGC detector diode from rectifying an r-f signal until the signal level exceeds the value of the delay voltage. Thus, if separate diodes were not used, the delay voltage would prevent the detector (demodulator) diode from rectifying weak signals which are below the threshold level established by the value of the delay voltage. Once the signal level rises and exceeds the value of the delay voltage, the AGC detector begins to rectify and produce a dc output voltage which is applied as bias to the controlled stages. The requirement for filtering of the dc output voltage to remove amplitude modulation components and the R-C time-constant considerations are essentially the same as the simple AGC system. The delayed AGC circuit is employed in many AM boradcast, communications, and dual-diversity super-heterodyne receivers, as well as in similar microwave and radar receiving systems.

Amplified and Delayed AGC. There are many variations in amplified and delayed AGC systems. However, these various AGC systems can be classified according to two categories: systems which amplify a signal *before* rectification, to obtain the AGC voltage, and systems which amplify the AGC voltage *after* signal rectification. In either case, a form of delay Voltage is incorporated so that the maximum sensitivity

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of the receiver can be realized for weak-signal reception. When amplified and delayed AGC is used to control a receiving system, the over-aU output versus signal input characteristics can be made to approach an almost ideal condition.

The accompanying illustration shows block diagrams for two basic types of amplified and delayed AGC systems.





Part A of the illustration shows a system in which the signal is amplified by an AGC i-f amplifier *before* rectification by the AGC diode. Part B shows a system in which the signal voltage is amplified by a dc amplifier *after* rectification by the AGC diode. The dc amplifier stage is followed by a delay diode which supplies AGC voltage to the controlled stages only when its cathode is negative with respect to its plate, and the diode conducts; when the delay diode is not conducting, the AGC output voltage is zero and the receiver gain is at maximum for **all** signals below the threshold of AGC operation.

Note that both AGC systems illustrated incorporate a form of delay voltage. In the amplified and delayed AGC system illustrated in part A, the delay voltage is applied to the AGC detector, which follows a separate amplifier; the separate amplifier receives its signal from the last i-f amplifier of the receiving system. Another variation of this AGC system employs an independent AGC amplifier channel consisting of several stages and having a greater over-all amplification (gain) than does the signal i-f amplifier channel. In the AGC system illustrated in part B, the delay voltage is shown applied to the d-c amplifier stage. One possible variation of this circuit applies a delay voltage to the AGC detector as in the circuit for the delayed AGC system shown in Part A. In practice, however, almost all AGC circuits using a dc amplifier to control the AGC voltage employ a delay diode in the output to prevent the dc output voltage from ever becoming positive with respect to ground.

# Types of AGC Circuits (Semiconductor)

AGC circuitry in the semiconductor field falls into two general classes. One class uses the variation of dc bias on one or more elements of a transistor amplifier stage to control its **gain**. The other class employs a diode or another transistor to shunt the input signal to ground (or around the controlled stage) and thereby reduce the over-all gain. The output of the second detector in a superheterodyne receiver provides, in addition to the desired signal, a dc component which is proportional to the carrier strength of the received signal. This dc component offers a convenient method of controlling the bias on a preceding r-f or i-f amplifier and thus controlling the stage gain.

Variation of transistor bias to control the gain may be accomplished either by changing the emitter current ( $I_E$ ) while the collector voltage is held substantially constant, or by changing the collector voltage (VC) by means of the collector current. These two methods are sometimes called *reverse AGC and firward AGC*, respectively. The following illustrations show a comparison of the two methods. In the figures, curves are shown for both the commonemitter and common-base circuit configurations. Upon examination of the figures, it is evident that the two configurations perform similarly, with the



**Emitter Current Control** 



Collector Voltage Control Comparison of Bias Control Methods

common-emitter circuit providing a somewhat greater control range. The emitter current control circuit is more generally used than the collector voltage control circuit, mainly because of the very low collector voltage provided. At low collector voltages the collector capacitance is increased (an inherent disadvantage in the transistor); consequently, the alpha cutoff frequency is reduced, making the transistor a poor r-for i-f **amplifier**. The illustrations also indicate an important difference between the semiconductor AGC circuit and the electron tube AGC circuit; namely, the transistor AGC unit operates at very much lower power and voltage levels. For example, over the first

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decade (between .01 and 0.1 ma), the CE emittercontrol circuit provides a range of from approximately O to 18 dB gain variation with a current variation of only 100 microampere. In the collectorvoltage control circuit a similar range is covered with a variation of only 0.28 volt. Over the second decade, this performance is halved with the curve reaching its zenith and then declining.

When the bias of the transistor is changed by AGC control, the input and output impedances also change and produce a shift in the bandwidth and center frequency to which the circuit is tuned. For example, when the emitter current of a CE stage is reduced to decrease the gain, it causes an increase in input impedance and capacitance. As a result, the bandwidth of a parallel resonant circuit used with it is decreased (because of the increased Q), and its center frequency is shifted higher. This is a basic disadvantage of this type of circuit and presents a design problem. In addition, at the very low currents and voltages given in the examples the stage cannot handle much power, particularly since the reduction is usually in a downward direction. The usual practice is to apply AGC control to a single stage (either the 1st r-f or i-f), rather than a number of stages as is common in electron tube practice. In those cases where substantial power is required to drive and control the emitter current of the transistor gaincontrolled stage, a dc amplifier may be provided. Usually, however, amplification is obtained by applying the control voltage to the base of the transistor amplifier and allowing it to act as its own dc amplifier. Delayed AGC action can also be provided by adjusting the bias to be effective only above or below the desired operating level.

**Typical AGC Characteristics. One** of the purposes of the AGC system is to hold the i-f (or r-f) signal input to the detector (demodulator) relatively constant over a considerable range of received signal strength at the input terminals to the receiving system. It was previously stated that a simple AGC system accomplishes control of receiver gain by varying a negative dc bias voltage applied to the control grids of remote cutoff tuhes in the r-f and i-f stages of the receiver. Thus, as the received signal increases, the signal at the detector also increases, resulting in a greater negative dc voltage available for control purposes. The control (bias) voltage is applied to the early stages of the receiver to reduce the overall gain. The reduction in receiver gain lowers the input to the detector and, within limits, tends to keep the detector output from rising too rapidly as the input signal increases. However, it is virtually impossible to hold the input to the detector (demodulator) constant, because the AGC voltage is dependent upon the strength of the received signal, which is amplified by the controlled stages of the receiver and rectified by the detector. Thus, an increase in the strength of the received signal means that the rectified output of the detector also increases, and this voltage (or a corresponding voltage) is, in turn, fed back as a control voltage. Therefore, it is reasonable to assume that there must always be some increase in the receiveroutput voltage. The rate of increase, however, is determined by the individual circuit design, and desirable characteristics can be attained which approach the ideal characteristic.

The following illustration graphically compares the receiver-output characteristics of typical AGC systems with the characteristic of a receiver using a conventional diode detector without AGC. The plot of receiver output versus input signrd strength for a receiver without AGC (curve A) shows that the output rises rapidly for an increase in signal strength; however, the receiver output soon becomes distorted because of overloading which occurs with large input signals. The plot of receiver output for a receiver with simple AGC (curve B) shows that even small input signals are acted upon by the AGC voltage, and, as a result, the output obtained from weak signals is reduced. The plot of receiver output when delayed AGC is used (curve C) shows that the output for small input signals closely follows the output obtained when no AGC is used and that, when the input signal reaches some predetermined strength, the output is prevented from rising too rapidly as the input signal is further increased. The plot of receiver output when amplified and delayed AGC is used (curve D) approaches an ideal condition wherein the receiver is sensitive to weak signals and the output is held relatively constant once the input signal exceeds some predetermined strength.



**Reeeiver Output Versus input Signal Strength** 

Methods of Feeding AGC-Controlled Stages. Two methods are used to feed AGC voltage to the input of a controlled amplifier. These two methods are commonly called series feed and parallel (or shunt) feed. In either method, the AGC voltage is actually in "series" between the control grid and the cathode of the controlled tube. The terms *series feed* and *parallel* feed are used for convenience to identify the circuit arrangement which enables the AGC voltage to be applied to the control grid. AGC systems utilize one method or the other in feeding the control voltage to an individual tube. Sometimes, because of resonant circuit design or interstage coupling arrangements, one method is used to feed one stage of the receiver and the other method is used to feed another stage. For example, in a typical VHF superheterodyne receiver, the single r-f amplifier is a parallel-fed stage while the i-f amplifier channel incorporates several series-fed stages.

The series-feed arrangement is illustrated in part A of the accompanying simplified schematic diagram. Impedance Z is normally a tuned circuit, transformer, or other coupling impedance. Resistor R and capacitor C form a decoupling network; in addition, capacitor C must also be considered as a d-c blocking

and r-f bypass capacitor for the grid-circuit impedance, Z. The d-c path for the application of control voltage to the grid of the tube is through impedance Z; in other words, the impedance is in "series" with the control voltage.

The parallel-feed arrangement is illustrated in part B of the accompanying simplified schematic diagram. In this circuit, resistor R is effectively in parallel with impedance Z, and provides a "parallel" (or "shunt") dc path for the application of control voltage to the grid of the tube. The value of the resistor is usually made high so as not to "swamp" or "load" the impedance; however, the actual value of resistor R together with the other resistors in the series circuit between the control grid and cathode must not exceed the rated maximum grid-circuit resistance recommended for use with the particular type of tube. Capacitor C is a d-c blocking capacitor, and is used to prevent impedance Z from acting as a voltage divider in conduction with resistor R.



Methods of Feeding AGC-Controlled Stages

AGC Time-Constant Considerations. In a previous paragraph it was mentioned that a dc control voltage obtained from a detector must be filtered to remove any modulation or alternating component of the rectified pulsating voltage; otherwise, if not removed, the modulation or alternating component would be applied to the controlled stages, along with the dc voltage. If any modulation component is fed back to the inputs of the controlled stages, a degenerative effect occurs and, as a result, the percentage of modulation on the carrier signal being amplified by the

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controlled stages will be reduced accordingly. Also, this effect may introduce considerable amplitude distortion in the output (demodulated) signal.

An R-C circuit is normally used to filter the dc control voltage. The design of a suitable R-C falter, of necessity, may be a compromise; the time constant must be sufficiently long to effectively filter out the lowest modulation-frequency component from the control voltage, and the time constant must be short enough to permit a change in dc control voltage when rapid fluctuations in signal level occur. (Time constants are discussed earlier in this section under Wave-shaping Circuits). Thus, the R-C networks of the AGC circuit influence the ability of the control voltage to follow rapid changes in the strength of the received signal.

A simple AGC system is illustrated in the following simplified schematic diagram. The r-f amplifier, mixer, and first i-f amplifier stages are series-fed and controlled by AGC voltage taken from the detector (demodulator) diode. (The second i-f amplifier stage is **self-biased** and is not controlled by AGC voltage.) RI is the detector load resistor and capacitor Cl is the r-f bypass capacitor for R1. Resistor R2 and capacitor C2 form an R-C network to filter the AGC voltage obtained from the detector. Resistor R3 and capacitor C3 form a decoupling network for the mixer stage; similarly, resistor R4 and capacitor C4 form a decoupling network for the r-f amplifier stage.

The time constant of an AGC system will depend largely upon the design of the receiving system and the type of transmissions to be received. Typical values of time constants used in communications work range from 0.1 second to 0.5 second. The time constant of an R-C circuit is given as:

TC = RC where:

TC = time in seconds

R = resistance in megohoms

C = capacitance in microforads

However, the typical AGC circuit is usually a complex network, and, because of the action of the detector diode in the circuit, the charge time constant and the discharge time constant of the circuit are not the same. The charge time constant for the AGC system shown in the illustration when the detector diode is conducting and rectified dc output is **devel**oped across load resistor R1 can be expressed as follows:

Charge TC = R2 (C2 + C3 + C4) + R3C3 + R4C4

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Simple AGC System

The discharge time constant for the system when the detector diode is not conducting (or is conducting less) can be expressed as follows:

Discharge TC = (R4 + R2 + R1)C4 + (R3 + R2 + R1)C3R1)C3 + (R2 + R1)C2 + RIC1

Note that the discharge path for the network is not the same as the charge path. Furthermore, because detector-load r-f bypass capacitor **C1** is usually a small value, the term R1 Cl in the discharge timeconstant expression can be neglected because its effect on the over-all constant is small.

Occasionally, the detector load resistor, Rl, is used as a manual volume control for the receiver; the variable contact of the volume control is coupled by means of a capacitor to an audio amplifier stage. When this is the case, the audio coupling capacitor, together with the grid resistor for the succeeding amplifier stage, may have an effect upon the AGC time constant, especially when the volume control is adjusted for maximum volume. Although the effect upon AGC action by the audio coupling capacitor and the grid circuit of the amplifier stage is a design consideration, the effect is usually neglected when making time-constant calculations.

The following example illustrates the difference between the charge and discharge time constants in a typical AGC system. The resistors and capacitors in the simplified schematic given earlier are assigned typical circuit values as follows:

R1 = 1 meg 
$$c1 = 0.0001 \mu f$$

$$R2 = 1 \text{ meg} \qquad C2 = 0.05\mu \text{ f}$$
  

$$R3 = 0.1 \text{ meg} (100\text{ K}) \text{ C3} = 0.05\mu \text{ f}$$
  

$$R4 = 0.1 \text{ meg} (100\text{ K}) \text{ C4} = 0.01\mu \text{ f}$$
  
To calculate the charge time constant in seconds:  
Charge TC = R2(C2 + C3 + C4) + R3C3 + R4C4  
= 1(0.05+ 0.05+ 0.01)+ (0.1 x 0.05)  
+ (0.1 x 0.01)  
= 0.11 + 0.005 + 0.001  
= 0.116 second

To calculate the discharge time constant in seconds:

Discharge TC = 
$$(R4 + R2 + R1)C4 + (R3 + R2 + R1)C3 + (R2 + R1)C2 + RIC1$$
  
=  $(2.1)0.01 + (2.1)0.05 + (2)0.05 + (1)0.0001$   
=  $0.021 + 0.105 + 0.1 + 0.0001$   
=  $0.2261$  second

Thus, from the calculations made above, the charge time constant is found to be 0.116 second and the discharge time constant 0.2261 second. From this example it can be seen that if the discharge time constant is too long and the received signal fades rapidly, the output of the receiver will be reduced until the **R-C** networks have discharged sufficiently to permit the receiver gain to increase and compensate for the drop in input signal level. This inability of AGC voltage to respond and follow rapid changes in input signal level is called *time delay* (or *time kg*) in the AGC response. The greater the values of R and C, the longer the AGC time constant and the time delay of the AGC system; the smaller the value of R and C,

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the shorter the time constant and the time delay. However, if the charge time constant is too short, modulation components which are present on the dc control voltage may cause degenerative effects, (These effects were mentioned earlier in this discussion.) Thus, reducing the values of R and C below some practical minimum for a particular AGC system results in a reduction of filter efficiency; therefore, it is usually necessary to reach some compromise between filter efficiency and time delay in the design of an AGC system.

# SIMPLE AGC CIRCUIT (ELECTRON TUBE)

# Application.

The basic AGC circuit is used in many communications and broadcast receivers and in certain radar and television receivers, to obtain a dc control voltage which is supplied as an automatic bias for the r-f and i-f stages of the receiver.

#### Characteristics.

D-C control voltage is obtained directly from a detector (demodulator) diode or from an additional diode used as a half-wave rectifier,

Uses an R-C network as an **output** filter.

Dc output voltage varies in proportion to r-f input voltage. This circuit has a disadvantage in that weak input signals produce a small output voltage which, in turn, tends to lower over-all receiver sensitivity to weak signals.

#### Circuit Analysis.

General. The diode detector circuit, described in the Detector Section of this Handbook, and the diode detector with AGC circuit, described in this section, are very similar. Because of this similarity and because it is a simple matter to add a few components and make use of the detector output as a source of control voltage, the functions of the detector and AGC circuit are frequently combined in a single stage. The rectified voltage produced by the detector (demodulator) diode across its load resistance is proportional to the amplitude of the received carrier; therefore, the resulting rectified dc output voltage can be used to control the over-all gain of the receiving system. An R-C network is used to filter the pulsating dc output of the detector and rdso to remove any modulation component which might be present

**Circuit Operation.** A combined detector and AGC circuit is illustrated in the accompanying circuit schematic.



**Combined Detector (Demodulator) and AGC Circuit** 

A comparison of this circuit with the typical diode detector given in the Detector Section of this Handbook will show that the circuits are basically the same except for the addition of resistor R3 and capacitor C3.) Transformer T1 consists of tuned primary and secondary windings which are resonant at the frequency of the i-f amplifier; T1 is the output transformer of the i-f amplifier channel in a conventional receiving system.

Electron tube V1 is an indirectly heated cathodetype diode, and may be included within the envelope of a multi-purpose tube; the filament (heater) circuit is not shown on the schematic.

Capacitor Cl, resistor R1, and capacitor C2 form a low-pass R-C filter network. Potentiometer (variable resistor) R2 is the diode load resistor, and also the manual volume control for the receiver. The setting of potentiometer R2 determines the amplitude of audio output signal which is coupled by capacitor C4 to succeeding amplifier stages. Resistor R3 and capacitor C3 form an R-C network to filter the dc voltage applied to the controlled stages as automatic bias.

The operation of a typical detector (demodulator) circuit is given in the circuit analysis portion of Diode Detectors, in the Detector Section of this Handbook, and may be reviewed at this time if desired. Thus, for the purpose of this discussion, it is sufficient to say that a dc voltage which varies in amplitude according to the modulation frequency is developed across

diode load resistor R2 whenever a modulated signal is applied to the input of the detector circuit. The polarity of the rectified voltage is given on the simplified schematic diagram.

The R-C network consisting of resistor R3 and capacitor C3 is connected to the junction of resistors RI and R2. The negative voltage at this point is a dc voltage with an alternating component which is the result of amplitude modulation present on the r-f signal. The purpose of resistor R3 and capacitor C3 is to remove the modulation components so that a steady dc voltage is available as a bias voltage for the controlled stages of the receiver.

Assume for the moment that a weak signal is being received. In this case the voltage developed across diode load-resistor R2 will be a small voltage, and the resulting AGC output voltage will also be small; therefore, the value of grid bias voltage applied to the controlled stages will be small, and the gain of controlled stages will be reduced only a slight amount.

Next, assume that a moderate signal is being received. In this case the voltage developed across diode load resistor R2 will increase in value, and, as a result, the value of grid bias voltage applied to the controlled stages will also increase; thus, the gain of the controlled stages will be further reduced.

Now, assume that a strong signal is being received. In this "case the voltage developed across diode load resistor R2 will increase considerably, and, as a result, the bias voltage applied to the controlled stages will also increase; thus, the gain of the controlled stages will be still further reduced.

From the three signal input conditions just described, it can be seen that as the strength of the input signal to the receiver increases, the detector output and the value of the control voltage increase as a result, and, to offset the increase in input signal strength, the over-all gain of the receiver is reduced. Conversely, as the strength of the input signal to the receiver decreases, the detector output and the value of the control voltage decreases as a result, and, to offset the decrease in input signal strength, the over**all** gain of the receiver is increased.

The effect of an automatic bias control voltage is to "level out" the response of the receiving system. Thus, the change in receiver output for a given change in input signrd is always less with an AGC circuit than it is without an AGC circuit.

A simple AGC circuit which is independent of the detector (demodulator) diode is illustrated in the

accompanying schematic; this circuit is a variation of the basic diode detector circuit discussed previously in the Detector Section of this Handbook. The diode, V1, is not used to demodulate the signal; instead, it is used only as a half-wave rectifier to obtain an AGC voltage which is proportional to the input signal. The diode may be a separate electron tube, or may be included within the envelope of a multipurpose tube. Capacitor Cl is an r-f coupling capacitor, and is normally connected to a relatively high-impedance signal source, such as the plate of the detector (demodulator) diode or the plate of the last i-f amplifier tube. The dc output voltage is developed across diode load resistor R1 as a result of signal rectification by diode VI. Resistor R2 and capacitor C2 form an R-C network to filter the dc voltage applied to the controlled stages.



Simple AGC Diode Circuit

The main disadvantage of the two AGC circuits just described is that *all* received signals-including weak signals–will develop AGC voltage. Thus, even a very weak signal will produce a small amount of AGC voltage, causing a reduction in the over-all receiver gain at a time when maximum gain is desired.

# Failure Analysis.

**General.** Before suspecting trouble in the AGC circuit, it must first be established that the detector (demodulator) circuit and the r-f and i-f amplifier circuits are functioning normally. Checks must be made to determine whether there are any shorted, leaky, or open components in the **R-C** networks of the controlled stages (either series- or parallel-fed). Defective components in these networks will affect the AGC voltage distribution, the AGC circuit time constant,

and perhaps the resonance and selectivity of the tuned coupling circuits.

No AGC Voltage. The AGC voltage no-output condition is generally caused by a failure in the detector (demodulator) circuit, and is usually accomplished by a lack of detector output. Since the AGC circuit is often a part of the detector circuit, the correct operation of the detector should be determined (as given in the Detector Section) before investigating the AGC circuit for a possible failure. An exception to this procedure is the case where a diode which is independent of the detector (demodulator) diode is used to obtain AGC voltage. The procedure for failure analysis of the independent AGC diode circuit is essentially the same as the procedure given for the detector (demodulator) diode circuit,

In either the simple AGC circuit or th independent AGC diode circuit, if the output capacitor of the R-C filter network is shorted, the AGC output voltage will be developed across the filter resistor, and, therefore, no AGC voltage will be applied to the controlled stages.

Because AGC circuits are nearly always lowvoItage, high-impedance circuits, it will be necessary to use a suitable vacuum-tube voltmeter when making AGC voltage measurements.

Low AGC Voltage. Low AGC voltage will result in greater than normal over-all receiver gain, and will often cause distortion when a strong signal is received. With a known r-f or i-f signal (either modulated or unmodulated) applied to the input of the receiver or to the input of the detector circuit, a dc voltage measurement should be made across the diode lead resistor to determine the value of negative AGC voltage present. (AGC voltages should always be measured with a suitable vacuum-tube voltmeter.) A second voltage measurement should then be made at the output terminals of the AGC circuit (across the output capacitor of the R-C filter network) to determine whether the voltage at the output is the same value as the voltage measured at the input to the R-C filter network. If the output voltage measured is less than the input voltage, it is likely that a voltagedivider action is taking place, causing a current to flow in the circuit, with a consequent voltage drop across the filter resistor. In this case, the output capacitor of the R-C filter network may be leaky, or the capacitors, tuned circuits, or other impedances in the controlled stages may have leakage paths to ground (chassis). Measurements may be made

throughout the voltage distribution system to determine the points at which voltage-divider action is occurring, in order to further isolate the faulty component. As an alternative, the circuit connection at the output of the R-C filter network, sometimes referred to as the AGC bus, should be disconnected to isolate the controlled stages; the components of the networks associated with these stages should then be checked by means of resistance measurements to locate the faulty component(s) in the voltage distribution system.

# EMITTER-CURRENT CONTROL AGC

## Application.

Emitter-current control of AGC is universally used in transistorized receivers to keep the output voltage relatively constant regardless of input signal variations.

#### Characteristics.

To control a PNP transistor, AGC circuit requires a positive voltage which increases as receiver input signal increases; to control an NPN transistor, it requires a negative voltage which increases as input signal increases.

For CE configuration, provides 18 dB control for first decade of emitter current variation, decreasing to half this value for successive decades (for CB configuration, the range is approximately 5 dB less).

Uses base bias voltage variation to provide dc amplification of control signal.

When transistor amplifier is directly controlled by control source (detector), the source must be capable of supplying full emitter current of transistor amplifier.

Resistive component of input impedance increases as CE emitter current decreases.

Input and output capacitance decreases as signal strength increases, and this decrease shifts center tuning frequency upward.

#### Circuit Analysis.

**General.** The emitter-current controlled AGC circuit operates normally with maximum gain at zero input signal. As the input (detected) signal increases in strength, the emitter current of the controlled amplifier is reduced. Hence, the gain of the transistor is also reduced. Therefore, with a large input signal the emitter-current controlled amplifier operates at a very

low level. As a general rule, currents above **500** microampere have little control over the gain; that is, the gain variation for currents over 500 microampere is so slight that the circuit provides too small a range of control to be useful. However, as the emitter current is reduced below 500 microampere, the over-all gain is greatly affected. The most effective control action is obtained over a current range of 10 to 100 microampere (as illustrated by the emitter current control curve shown above).

Since the emitter current operates over a very small current range for large input signals, distortion is produced by detector nonlinearity. Over the middle range of operation the detector is linear and little distorion is produced. At very low levels of input signal, distortion again occurs because of detector nonlinearity in the small-signal region.

**Circuit Operation. The** accompanying figure shows a typical emitter-current controlled amplifier.



**Emitter-current Controlled Amplifier** 

Capacitor Cl is a dc blocking and ac coupling capacitor which prevents the low dc resistance of the input transformer from shorting the base and bias network to ground. Resistors RI and R2 provide fixed voltage-divider bias for the base circuit. Since the base is negative with respect to the emitter, forward bias is applied. The AGC control signal is also applied to the base, and consists of a positive voltage which increases as the signal at the detector increases. When the control voltage increases, the total forward (negative) bias on the base is reduced, and the emitter current is reduced accordingly. Emitter swamping is provided by R3 (by-passed by C2) to provide temperature stabilization of the amplifier (refer to the discussion of Bias Stabilization in the introduction to Amplifiers in this Handbook for a discussion of emitter swamping and voltage-divider biasing). The collector is tapped down on inductor L of the series-tuned resonant output circuit, consisting of L and C, to provide proper matching. The output circuit is tuned to provide maximum gain and selectivity at the intermediate frequency. Capacitor C3 is a dc blocking and ac coupling capacitor for the next stage (a transformer may be used in place of L, C, and C3 if desired).

Consider now the dynamic operation of the circuit. Normally **Q1** is resting, with the base biased for class A operation by voltage divider R1 and R2. Emitter and collector current values are normal class A values for quiescent conditions. When an i-f signal is applied between base and ground through Cl, normal CE amplifier action occurs (assuming, of course, that no AGC voltage is applied from the control circuit). This, then, is the condition for no AGC where the amplifier operates at full gain with a very weak input signal. It is further assumed that the AGC control circuit is inoperative because of delayed AGC since the circuit is normally almost instantaneous in action. For this condition the emitter dc current is at its maximum value. As amplification occurs, the instantaneous emitter current varies (decreases for the positive portion of the signal and increases for the negative portion). Since both positive and negative variations of signal are equal (assuming a sine wave), there is no average change in emitter current. The instantaneous i-f variations, however, are amplifed and appear in the collector circuit (refer to the discussion of Tuned Interstage Amplifiers in the Amplifier Section of this Handbook for a complete discussion of normal amplifier action). As far as the amplifier is concerned, R3 is effective only for temperature variations, because it is by-passed by C3 for i-f signals. When the amplified signal appears in the detector, a dc voltage is developed, in addition to the demodulated signal. This dc voltage is proportional to the carrier strength and is taken at a point in the detector which provides an increasingly positive dc voltage for an input signal which is increasing (for PNP transistors). Assume that the input signal level rises to a point where the detector positive AGC control voltage exceeds the delay voltage and provides a positive dc voltage to the base of the transistor. Since the base

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#### ELECTRONIC CIRCUITS

of the transistor is negatively biased, the positive control voltage adds algebraically to reduce the total forward bias. Consequently, hole flow through the transistor is reduced, and the emitter current is reduced accordingly. (Both base and collector currents are reduced.) Therefore, the transistor forward current gain and the effective amplification of the transistor are reduced. Under these conditions, the transistor still amplifies the i-f signal, but not as much as before the forward bias was reduced. Thus, as the input signal increases, the output of the transistor is decreased. When the input signal becomes weaker, the detector control voltage is decreased, the forward bias, in turn, is increased, and the amplifier produces a greater output signaL In this manner, the output of the amplifier is controlled by the input voltage, which automatically controls the gain of the transistor amplifier.

The over-all power gain is contingent upon matched input (and output) conditions. When the base current is reduced by AGC action, the effect is the same as though the input resistance of the transistor were increased  $(R_{in} = V_{in}/I_{in})$ . The output impedance also changes, but not as much as the input impedance. Thus a mismatched input and output condition results. Such a condition enhances the control action and provides more effective AGC control. Where insufficient range of control is provided by a single stage, more than one stage of control is used. However, this is the exception rather than the rule, since cutoff bias may be reached on extremely strong signals, or AM modulated signals may be compressed to the point where actual suppression of modulation occurs (FM signals are not affected by this amplitude suppression action).

Another design problem is introduced by the change of input and output capacitance with signal In the CE circuit, both capacitances strength. decrease with strong signals. As a result, the center frequency of the tuned output circuit is shifted upward. (In the CB circuit this effect is exactly opposite, and a downward shift is produced.) As the design of transistors improves, it is probable that types similar in action to the remote cutoff electron tube will be developed and used in AGC circuits. At present, however, the action is the same as that of a sharp cutoff tube, so that control amplifiers must be restricted to handling fractional powers to avoid blocking and distortion, and some circuit detuning must be expected.

#### Failure Analysis.

**No Output.** Usually a no-output indication is produced only by an open- or short-circuited condition in the controlled stage. Observation of the signal using an r-f probe and oscilloscope will indicate where the signal disappears. Once this is determined, a resistance or voltage analysis of that portion of the circuit should reveal the defective component.

Low Output. If excessive bias is produced, cutoff current may be reached, or the signal may be reduced so much that little range of control is offered. In such cases the increase in amplitude caused by AM modulation can cause suppression of modulation. Such a condition can be observed on an oscilloscope. If oscillations occur in the controlled stage, a preceding stage or a following stage, an excessively strong input signal to the detector will result, and the control stage may be biased off. Removal of the input signal would cause the gain to increase, as evidenced by an increased noise output with no signal present. If an output signal is still observed, the signal is being produced internally through feedback, and it will probably be necessary to temporarily disconnect each stage preceding the detector and control amplifier from its collector supply to locate the defective stage. An alternative method for an experienced technician is to quickly short-circuit the input or output of a stage to determine whether the oscillation ceases. Do NOT short-circuit the input to output to ground, or the transistor rating may be exceeded or the heavy current produced may cause the delicate i-f transformer winding to open.

Distortion. The changing of the input and output impedances and capacitances by changes in signal strength will cause a shift in the tuned frequency and the overall circuit Q. Therefore, it is to be expected that some distortion will occur, particularly on quickly varying strong signals. If the distortion is continuous, an improperly operating circuit or a defective transistor may be the cause. Use an oscilloscope, and simulate a varying input signal by means of a signrd generator connected to the input circuit. Observation of the waveform at various points in the circuit should indicate the defective portion, whereupon a resistance analysis will isolate the defective component in this portion of the circuit. If the waveforms preceding and following the controlled amplifier are identical except for amplitude, the distortion is probably occuring in later stages and is not caused by the control circuit.

# AUXILIARY DIODE CONTROL CIRCUIT (SEMICONDUCTOR)

# Application.

Auxiliary diode control AGC circuits are used in conjunction with the regular limited range AGC circuit, normally employed in solid-state receivers, to provide additional AGC action when extremely strong signals are encountered.

#### Characteristics.

Provides considerable AGC action for strong signals.

Has little or no effect on weak or medium strength signals.

Utilizes a diode to shunt strong signals around one of the i-f amplifier stages, thereby decreasing system gain.

Auxiliary diode operation is indirectly controlled by the regular AGC circuit.

# Circuit Analysis.

General. Automatic gain control circuits in the semiconductor field can be placed into two general classes. One class, referred to in this Handbook as standard AGC, uses a variation of bias on one or more of the transistor elements to control the gain of the receiver, while the other class employs a diode to shunt the input signal around the controlled stage to lower the gain of the receiver. The auxiliary diode AGC circuit operates on the latter principle, however, it is usually used in addition to a standard AGC system to obtain improved control, and to prevent the receiver from being overloaded when very strong signals are received, since the range of control of most standard AGC circuits is somewhat limited, especially at high input signal levels. In a receiver using both auxiliary and standard AGC, the auxiliary AGC circuit is controlled by the standard AGC circuit. When weak and medium strength signals are received the auxiliary AGC circuit is not operated, and the receiver output is held fairly constant through the action of the standard AGC circuit (which frequently uses emitter cm-rent control, although collector voltage control can be used, if desired). As the input signal increases beyond a predetermined point, the AGC control voltage increases to a level sufficient to forward bias the auxiliary diode AGC circuit, and the auxiliary diode conducts.

The conducting diode provides a low impedance shunt around the standard AGC controlled stage, creating a great deal of **additional** AGC action. It is important to keep in mind that the auxiliary diode AGC circuit does not operate independently, rather it operates in conjunction with a standard AGC circuit, and its operation is controlled by the standard AGC circuit. A knowledge of standard AGC circuits, (emitter current control or collector voltage control) is helpful in the understanding of the auxiliary diode control circuit. For the interested reader, detailed information concerning these circuits is located in this section of this Handbook.

**Circuit Operation. The** following schematic diagram illustrates a typical emitter current controlled amplifier with auxiliary diode AGC.





Transformer T1 provides inductive coupling between the controlled amplifier and the preceding stage. Resistor RI, which is in the collector circuit of the preceding stage develops bias for the anode of auxiliary diode CR1. Resistor R2 together with resistor R3 form a base bias voltage divider between ground and the negative supply to forward bias the emitter base function of transistor Q1. Resistor R4, which is bypassed by capacitor C1 is a conventional emitter stabilization resistor which compensates for ambient temperature variation. Capacitor C2, together with the primary of transformer T2 forms a tuned output load for amplifier Ql, and the signal developed across the primary of T2 is inductively coupled to the secondary of T2 to the following NAVSHIPS 0967-000-0120

stage. Resistor R5 also develops cathode bias for auxiliary diode CR], and capacitor C3 shunts to ground any signal voltage that may be developed across R5. Resistor R5 should not be confused with the resistor used in the collector voltage control AGC circuit since the value of R5 is insufficient to achieve collector voltage control.

When there is no signal input to the receiver, there is no voltage developed. Auxiliary diode CRI is normally back biased by the voltage drop across R5 caused by the quiescent collector current of Q], and by the higher negative voltage, applied to RI and the collector of the preceding converter stage. Component values are such that the voltage across R1 exceeds the voltage drop across R5 thereby back biasing (or reverse biasing) auxiliary diode CR1, since the cathode of CR1 is less negative than the anode. When an input signal is applied to the receiver, AGC voltage is produced by the receiver detector and is coupled to the controlled stage, or stages. This AGC voltage, which is in the form of a dc voltage, is directly proportional to the average carrier power received by the receiver. However, delayed AGC is usually used and the AGC voltage must exceed a fixed "delay voltage" also called the "threshold voltage" before AGC voltage is applied to the controlled stage. In this manner the receiver gain is maintained at a maximum, since there is no AGC action when weak signals which are below a predetermined level are received. Assume that a signal is received which is of sufficient amplitude to overcome the AGC delay voltage. The positive AGC voltage (positive AGC voltage is used with PNP transistors, negative voltage is used with NPN transistors) developed in the receiver detector is applied to the junction of bias voltage divider R2, R3 and decreases the forward bias applied to the emitter base junction of Q1. The conduction of Q1 decreases, resulting in a decrease in gain of the stage. Decreased conduction of Q1 also results in a decreased voltage drop across R5 which in effect decreases the original back bias applied to diode CR1. As the strength of the input signal increases the level of the AGC voltage increases, resulting in a further decrease in conduction of Q1 and a further decrease in the voltage drop across R5. When the voltage drop across R5 no longer exceeds the voltage drop across R1 (that is the anode of CR1 becomes more positive than the cathode) auxiliary AGC diode CR1 is no longer back biased. CRI then conducts, and provides a low impedance (shunt) path

around IF amplifier stage Q1. Much of the IF signal generated in the converter stage is then shunted around Q1 through CR1 and C3 to ground, providing additional AGC action (signal reduction). Component values are usually chosen so that the auxiliary diode is back biased for all but very strong signals.

# Failure Analysis.

**Generel.** When making voltage checks use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low voltage ranges of the standard 20,000 ohm-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. No output from the auxiliary diode AGC controlled amplifer could be caused by defective power supply voltage, defective transistor or diode, or by a defective circuit component. Check the power supply voltage with a VTVM. If the transistor is not defective, a defective circuit component is more likely the cause of no output. An open emitter, base, or collector circuit, or a shorted base or collector circuit, would render Q1 inoperative and no output would result. With the power removed, check the base and collector circuits for a possible short to ground with an ohmmeter, and check R2, R3, R4, and R5 for an open. Also check the secondary of T1 and the primary of T2 for an open, and check C2 and C3 do for a possible short. A defective auxiliary diode or a change in value of circuit components is more likely to cause a low output condition, rather than a no output condition to exist.

Low Output. If oscillations occur in the controlled stage, or in a stage following the controlled stage, there could be excessive input to the detector and the resultant excessive AGC voltage produced by the detector could greatly reduce the gain of the controlled stage causing a low output condition to exist. Oscillation of this type usually result in excessive receiver noise, in addition to low output. If an output signal is present with no input applied to the receiver, oscillations are probably being produced internally through feedback and it will probably be necessary to temporarily disconnect each stage, preceding the detector, from its collector supply to locate the oscillating stage. Improper power supply voltage, a defective transistor or **auxiliary** diode, or a defective circuit

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component which alters the bias on either the transistor or auxiliary diode could also cause a low output condition to exist. Check the power supply voltage and adjust if necessary. Check the front to back ratio of the diode. If proper operation is not restored a defective circuit component is probably the cause of of low output. A change in the value of either RI or R5 could alter the bias applied to auxiliary diode CR1, possibly causing CR1 to conduct continuously, and greatly reduce the gain of the contolled stage for all input signal levels. A change in value of either R2, R3, or R4, would alter the emitter base bias of Q1 and could also reduce the gain of the stage for all input signal levels. If Cl opens, the resulting degeneration across R4 could rdso lower the gain of the stage. If C2 or C3 become leaky low output could also result. All resistors should be checked for proper value with an ohmmeter and all capacitors with an in-circuit capacitor checker if the trouble cannot otherwise be located.

**Distorted Output.** Some distortion may occur in AGC controlled stages, since the input and output impedances vary as the gain of the stage is varied by the AGC circuit. The condition may be **especially** noticeable on quickly varying strong signrds. However, if distortion is continuous an improperly operating circuit or a defective transistor usually is the cause. A resistive analysis, with the power removed, should reveal the component at fault.

# COLLECTOR VOLTAGE CONTROL CIRCUIT (SEMICONDUCTOR)

# Application.

Collector voltage control AGC is one method of AGC control used in transistorized receivers to keep the output level relatively constant regardless of input signal strength variations.

# Characteristics.

Automatic gain control is achieved by varying the collector voltage applied to an i-f amplifier stage.

When PNP transistors are used, the AGC voltage must be negative. For NPN transistors a postive AGC voltage is required.

# Circuit Analysis.

**Generel. The** power gain of a common emitter amplifier may be varied by varying the dc collector

voltage of the amplifier. This principle is the basis of collector voltage automatic gain control. By applying AGC voltage to the base of the controlled amplifier the dc emitter current is varied which in turn varies the dc collector current. Variation of dc collector voltage (which varies the amplifier power gain) is accomplished by passing the dc collector current through a series resistor in the collector circuit. An increase in dc collector current results in an increased voltage drop across this collector resistor, which lowers the collector voltage and the gain of the amplifier decreases. In the collector voltage control AGC system as in other AGC systems, over all receiver gain is maximum for weak signals and is decreased by AGC action when stronger signals are received, so that the receiver output remains fairly constant.

It is interesting to note the similarities and differences between emitter-current control and collectorvoltage control. Circuitwise they are quite similar, the major difference betweem them is the addition of a large resistor in the collector circuit of the collector voltage control AGC circuit. In both circuits the AGC voltage is applied to the base of the transistor, however, each circuit uses a different polarity AGC voltage. The AGC voltage in the collector voltage controlled circuit is polarized so that it increases the forward bias at the emitter base junction, when a stronger signal is received (as the carrier increases), thereby increasing conduction of the transistor. Thus, an increased voltage drop occurs across the collector resistor as the forward bias increases the collector current, resulting in a decrease of voltage at the collector. This decresase of collector voltage, in turn, lowers the power gain of the amplifier.

In contrast, the AGC voltage applied to the emitter current control AGC circuit, is of such a polarity as to decrease the forward bias at the emitter base junction, when a stronger signal (carrier) is received. As the forward bias is reduced, the conduction of the transistor decreases. Since there is no large series resistor in the collector circuit of the current controlled AGC circuit, the only resistance offered to the flow of collector current is the normally low dc resistance of the output transformer; therefore, the collector voltage remains practically constant despite the change of collector current. The gain of the amplifier, however, decreases since the emitter current decreases. Hence it is seen that the current controlled AGC circuit operates near the region of emitter current cutoff, while the voltage controlled AGC circuit operates near the limits of collector current saturation. As a result, transistorized AGC circuits also usually used a strong signal, shunting device such as an auxiliary diode to secure effective AGC action over large ranges.

**Circuit Operation.** The following schematic diagram illustrates a typical collector voltage automatic gain controlled amplifier.



**Collector Voltage Controlled Amplifier** 

Resistor R1 together with resistor R2 forms a base bias voltage divider between ground and the negative supply, to furnish fixed forward bias to the emitter base junction of Q1. The negative AGC control voltage from the detector is applied to the base of Q1 through decoupling resistor R3 and both R2 and R3 are bypassed by Cl. Resistor R4, which is bypassed by capacitor C2 is a conventional emitter stabilization resistor, sometimes called a "emitter swamping" resistor, intended to prevent transistor operational characteristics from varying with changes in temperature. Collector voltage control is achieved by the addition of resistor R5 to the collector circuit of Q1. Capacitor C3 together with the primary of output transformer T1 forma tuned output load for amplifier Q1. Capacitor C4 in conjunction with collector voltage control resistor R5 also forms an i-f decoupling network to prevent if energy from feeding back into the power supply.

With no signal input the conduction of Q1 is determined by the fixed forward bias applied to the base of Q1 by base bias voltage divider R1, R2. There is no detector output and hence no AGC voltage is developed. The gain of the controlled stage is at a maximum since the voltage drop across collector voltage resistor R5 is at a minimum and the voltage applied to the collector of Q1 is, therefore, maximum. W'hen a signal of sufficient strength to produce a detector AGC output large enough to overcome the AGC delay voltage is received an AGC control voltage is applied to the base of controlled amplifier Q1. The polarity of this voltage is such as to increase the forward bias applied to the base of the transistor. In this case controlled amplifier Q1 is a PNP transistor and the AGC control voltage is, of course, negative. Conduction of Q1 is increased and the resultant collector voltage drop across R5 increases, reducing the actual voltage applied to the collector of Ql, and thereby reducing the gain of the amplifier. The receiver output remains relatively constant since a further increase in input signal strength tends to incresase the AGC control voltage. This results in a further incresase in conduction of Q1 and an increased voltage drop across R5. As a consequence, the collector voltage of Q1 decreases and the gain of the controlled amplifier is, again, lowered.

Collector voltage control is not frequently used because of the low vahre of collector voltage applied to the transistor. At low collector voltages the collector capacitance is increased and consequently the alpha cutoff frequency is reduced, making the transistor a poor r-for i-f amplifier.

# Failure Analysis.

**General.** When making voltage checks, use a vacuum tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of a standard 20,000 ohms per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No **Output. No output** from the collector voltage controlled amplifier could be caused by defective power supply voltage, a defective transistor, or by a defective circuit component. Check the power supply voltage. An open emitter, base, or collector circuit, or

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a shorted base or collector circuit would render Ol inoperative, and no output would result. With the power removed, check the base and collector circuits with an ohmmeter for a possible short to ground. If the collector circuit appears to be shorted to ground capacitor C4 may be shorted or the primary of TI may be shorted to its case. Check the emitter and collector circuits for a possible open, paying particular attention to R4 in the emitter circuit, and R5 and the primary of T1 in the collector circuit. Check resistors RI and R2 for proper vrdue, since an open or short of either part would alter the bias applied to Q1 and drive QI either heavily into saturation or into cutoff. This condition would probably produce little or no output from the controlled stage. If capacitor C3 becomes shorted, the output signal would be shunted around transformer T1 and there would not be any output coupled to the following stage. Improper AGC control voltage caused by a defect in the AGC deterctor circuit, could also cause a nooutput condition to exist. The existence of this condition may be determined by measuring the voltage present at the base of Q1 with no signal applied to the receiver.

Low Output. A low output condition could be caused by defective power supply voltage, a defective transistor, defective circuit components, or by self oscillation. Since self oscillation would result in an excessive detector input, it would also result in the generation of excessive AGC control voltage, and therefore could cause a low output. Oscillations of this type usually also result in excessive receiver noise in addition to the low output. If an output signal is present with no signal input to the receiver, self oscillations are probably being produced internally through feedback. If self oscillations are not the cause of low output, check the power supply voltage with a high resistance voltmeter. If proper operation is still not restored, a defective circuit component is most likely the cause of low output. A change in the value of RI, R2 or R4 would alter the bias applied to the base emitter junction of Q1 and low output could result. If emitter bypass capacitor C2 opened the resulting degeneration would lower the gain of Q1 and a low output would also result. Low output would also result if R5 increased in value since the collector voltage applied to OI would be correspondingly reduced. A defect in output transformer T1 would also reduce the output by either detuning the output tank which consists of C3 and the primary of

Tl, or by reducing the amount of signal coupled to the following stage.

**Distorted Output. Since the** input and output impedances of the amplifier vary as the gain of the amplifier is varied by AGC, some distortion is to be expected especially when strong signrds are received. However, if distortion is severe and continuous a defective transistor, power supply, or circuit component probably exists. The power supply and the transistor should be checked, and if distortion persits, voltage checks of the transistor elements should be made with a VTVM to localize the trouble. Resistance measurements with the power removed, may then be made to locate the faulty component.

# AGC-CONTROLLED AUDIO AMPLIFIER (ELECTORN TUBE)

The AGC-controlled audio amplifier is used to silence (squelch) the receiver until a signal of usable level is received, and to reduce the noise output as the receiver is tuned from one signal to another. It is particularly useful in mobile and controlled net operation.

#### Characteristics.

It is turned off by a positive AGC delay voltage.

It is turned on by a negative AGC voltage.

It may be rendered inoperative by a separate switch.

Operating threshold is determined by a manual bias control.

It is operated by a negative AGC voltage of from O to 35 volts.

May be packaged as a self-contained accessory, or supplied as an integral part of the receiver.

# Circuit Analysis.

**General.** To ensure that the squelch is opened by the weakest readable signal, it is **necessary** that a high sensitivity level be maintained. To achieve this high sensitivity without excessive background noise from various sources, the squelch circuit bias is determined by a threshold control. Thus the operator may adjust the operating threshold to suit local operating conditions. To permit operation of the reciever without squelch action, the squelch circuit is normally completed through a switch. When this switch is open the squelch circuit is inoperative. Although not necessary for circuit operation, both the threshold control and the squelch off-on switch are usually provided for convenience in operation.

**Circuit Operation.** A typical audio squelch operated by receiver ACC voltage is shown schematically in the following illustration.



AGC Controlled Audio Amplifier Circuit

A twin-triode electron tube is used, with halfsection VIA connected as a dc control amplifier, and half-section VIB operating as the bias controlled first audio stage. The grid of VI A is direct-coupled to the AGC control circuit, and is supplied with a portion of the control voltage by voltage divider Rl, and R2. Resistor R1 is also connected in series with VIA tube grid and acts as an isolation and current limiting resistor. Normally, the cathode circuit of the sequelch tube is completed through off-on switch S1. The plate of VIA is direct-connected to the grid of VIB through grid resistor R3, and the audio input to VIB is capacitively coupled through Cl. Resistor R4 is the plate resistor of VIA, which is connected to the bias voltage divider between the plate supply and ground formed by R9, R6, R7, and R8. The cathode of VIB

is connected to this voltage divider at the junction of R9 and R6, while plate dropping resistor R4 is connected at the junction of R6 and R7. In this manner the cathode of VIB is always more positive than the plate of VIA, a typical direct-coupled biasing arrangement. Resistor R8 is variable and acts as the threshold control. Tube V1 B is resistance-coupled to the second audio stage, R5 is the plate load resistor, and C2 is the coupling capacitor. Cathode bypassing for VIA *is* accomplished by C3.

With no signrd applied, the receiver ACC delay voltage of approximately +1 .S volts is applied to input voltage divider RI and R2. Since the grid of VIA is connected across R2 only that voltage appearing across R2 is effective in driving the grid; approximately one-fifth is dropped and lost across R1. Because R1 is connected in series between the ACC bus and the grid of VIA, any loading of the AGC bus by grid current flow is prevented by the high resistance of R1. Cathode bias for VIA is developed across threshold control R8, which is bypassed for audio frequencies by C3. Thus the average cathode bias remains unaffected by the signal or by instantaneous changes in the plate current of VIA. Switch S1 is normally close to complete the cathode circuit; when it is open the squelch circuit is made inoperative.

As the positive input (AGC delay) voltage causes VIA to conduct, a negative voltage drop is produced by plate current flow through R4. Current flow is from the cathode of VIA to the plate, through R4, and through the voltage divider to the supply. Thus the end of R4 which is direct connected through R3 to the grid of VIB is always driven negative when plate current increases in VIA. This negative bias on the grid of VIB biases the audio stage to cutoff, silencing the receiver. The point at which cutoff occurs is determined primarily by the setting of threshold control R8. When R8 is adjusted so that heavy plate current flows in VIA, a large bias is produced and only a very small positive signal is necessary to drive the squelch sufficiently to produce cutoff control bias.

When the incoming signal produces a negative AGC voltage in the receiver it causes plate current flow through VIA to be reduced. The reduced plate current produces a smaller voltage drop across R4, thus reducing the bias applied to VIB grid, and permitting the audio stage to operate. The audio

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output reaches maximum when squelch tube VIA is cut off. In a typical circuit, a AGC voltage of -0.3volt will ungate the audio stage and the output will increase until the ACC voltage reaches 0.8 volt. At this time, the squelch tube is completely cut off, normal bias is applied to the audio stage, and full audio output is obtained. The following chart shows a typical squelch sensitivity curve.



**Squelch Sensitivity Curve** 

Once the squelch tube is completely cut off, normal fixed bias for operation of the audio stage is supplied by the voltage divider connected to the cathode. By employing R6 and R7 as unbypassed cathode resistors, some cathode degeneration is provided to improve the linearity of the first audio amplifier. Any audio signal appearing on V1 B grid will not affect squelch operation, because squelch tube VIA is cut off when full output is obtained. During the time the squelch is biasing off VIB and partially reducing the audio output, any audio voltage coupled through R3 to the squelch plate is attenuated by the large resistance value of R3 and has no effect on circuit operation. Although there is a slight delay from application of the signal to the receiver until the circuit is completely ungated, it is only a few microseconds (which appears to be instantaneous) and has no effect on the intelligibility of the audio signal.

# Failure Analysis,

**Squelch Inoperative.** Lack of proper input signal, an open plate or cathode circuit, or a defective tube will prevent squelch tube VIA from operating. If the

receiver does not supply a positive delay voltage, or if R1 is open, or R2 is shorted, the circuit also will not operate. Measure the voltage from the grid of VIA to ground with a voltmeter, also the voltage on the AGC bus. Voltage at the bus, but not at the grid indicates either R1 is open, or R2 is shorted. Use an ohmmeter to check these resistors. If S1 is defective, the cathode circuit will be open and the squelch will not operate. Make a continuty check of the switch. If plate resistor R4 is either open or shorted, no bias will be developed to control the audio stage and the squelch will not operate. Measure the plate voltage on VIA. No plate voltage indicates R4 is open. With plate voltage on the plate of VIA and the squelch inoperative either the tube is defective, R4 is shorted, R3 is open, or threshold control R8 is set too high. Replace VIA with a known good tube and adjust the threshold control. If the squelch still will not operate, remove plate power and check the resistance of R4, and R3. If R3 is shorted, the squelch will operate but the audio will be reduced when the squelch is inoperative. On the other hand, if R3 is open there will probably be a reduced audio output and the squelch will not operate.

Squelch Operates, Audio Output Low. When the squelch operates, but the audio output is low, the receiver may be applying a weak audio signal, or the audio stage is improperly biased. Check the bias voltage divider with a volt meter to locate the defective resistor. Apply an audio signal form an audio signal generator to the grid of VI B. A larger output indicates the amplifier is operating and that the receiver is not supplying sufficient input.

#### PART 11-4. AFC CIRCUITS

# AFC CIRCUITS,

#### General.

Automatic Frequency Control circuits have a wide range of applications in radio, television, and radar. Their purpose is to automatically compensate for any drift in local oscillator frequency, as well as to automatically lock onto the selected frequency once the receiver is tuned to the approximate frequency. Thus, it is the function of afc to compensate for the warmup time of the receiver, during which the receiver is very susceptible to drift, as well as to compensate for any error in the mechanical tuning of the receiver.

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Our discussion here will be primarily concerned with afc systems which change the frequency of the local oscillator to compensate for any frequency drift which may occur in the r-f stage of the receiver, and also counteracts any tendency towards a frequency drift in the local oscillator.

The introduction of afc to a receiver necessitates the employment of one or more additional circuits, consisting essentially of a discriminator and a control device. The function of the discriminator is to change the direction and amount of the frequency error into a corresponding correction or control voltage variation. Many discriminators or detectors employed in f-m receivers are capable in themselves of providing an afc voltage, so it may not be necessary in these cases to add a discriminator to the receiver. This type of afc system is shown in part A of the following illustration. If the receiver detector is not capable of producing an afc error voltage, the addition of an afc discriminator becomes necessary, as shown in part B of the illustration. This error voltage, regardless of how it is obtained, is now applied to the control device, whose function it is to receive the error voltage from the discriminator and change it into a frequency correction for the local oscillator.



Block Diagrams of Typical AFC Systems

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If the output of the i-f amplifier is at the **proper** frequency, it is coupled directly through the discriminator and no error voltage is coupled back to the control device. Thus, the local oscillator frequency remains the same. If the i-f frequency is too high, the error voltage, for example, increases, and provides the necessary adjustment to the local oscillator. Conversely, if the i-f frequency is too low the error voltage, for example, decreases, and provides the **necessary** adjustment to the local oscillator.

A more refined method of afc contains its own separate mixer. This type of afc is used primarily in radar and thus the receiver employs two **converters**: one converter is used to mix the echo signal, and the other is used for the afc. A block diagram illustrating such a system is shown.



Block Diagram of Double Mixer AFC

Since the transmitted pulse is used as the frequency sample for the afc mixer in this application, it is not necessary that a TR tube preceed the afc mixer. A freed attenuator can be used instead, as a protection for the afc circuit. The remainder of the afc operation is the same as that of any other afc system, that is, the mixer discriminator produces an error voltage for application to the control device, and the control device changes the local oscillator frequency as necessary. It should be noted that the local oscillator now supplies *two* mixer circuits instead of the usual one, but  $\textcircled{\bullet}$  this power requirement is easily attained by the use of a special oscillator tube.

Examples of circuits which maybe used as control devices are discussed in this chapter. The particular control circuit chosen is contingent upon the receiver in which the circuit is to be used. The phantastron control circuit, for example, is most commonly used in radar receiver applications because of its sweep voltage characteristics, while for the same reason, it is not used in the standard f-m radio receiver. A control device commonly found in the f-m radio receiver is the reactance tube control device, or the thyratron control device.

# PHANTASTRON AFC CIRCUIT

# Application.

The phantastron afc circuit is used in radar and other electronic equipment to control the local oscillator and maintain the i-f within the receiver passband to minimize the effect of local oscillator or transmitter dirft.

# Characteristics.

Uses a hard tube phantastron oscillator as a search sweep.

Search sweep operates at a rate of about one cycle per second.

Automatically controls the local oscillator repeller voltage to maintain the proper i-f difference frequency.

Output may be taken from the cathode, screen, or plate, and be either positive or negative.

Combines a stable multivibrator action with dc amplifier action in one tube.

#### Circuit Analysis.

**General. The** phantastron afc system provides a means of automatically controlling the frequency of a klystron local oscillator. The output of the receiver discriminator is coupled through a pulse amplifier stage to a diode search stopper stage. The phantastron search tube, in the absence of control signals from the search stopper diode, applies a one cycle per second sawtooth wave to the klystron repeller. When the sweeping klystron reaches a frequency which produces the proper output from the discriminator, the search stopper diode applies a blocking bias to the grid of the phanstastron search tube and converts it into a dc amplifier. Corrections for small frequency changes are then accomplished by the search stopper diode and the dc amplifier.

**Circuit Operation.** The accompanying schematic illustrates a typical phantastron-diode afc sweep circuit.



#### **Phantestron AFC Circuit**

Only the search sweep tube and the search stopper diode are shown in the schematic, since the discriminator and pulse amplifier used to furniab the afc control pulse are common basic circuits discussed in other sections of the Handbook. Capacitor Cl is the input coupling capacitor with RI operating as the input coupling resistor and cathode bias resistor for diode VI; it also offers a dc return path to ground for the diode. Resistor R2 is the diode load resistor across which the rectified afc control pulses develop a dc bias to charge filter capacitor C2. Resistor R3 couples the search stopper diode direct to the grid of phantastron sweep amplifier tube V2, and incidentally acts as a series filter resistor to eliminate any ripple frequency appearing across C2. Resistor R4 is the phantastron plate load resistor; and R5 is the screen resistor for V2. Capacitor C3 is the plateto-grid feedback capacitor. Capacitor C4 couples the suppressor of V2 to the screen and also acts as a screen bypass to around via resistor R6. Resistor R6 serves the dual function of acting as a charging and discharging resistor for C4, and as a ground return resistor for the suppressor of tube V2. The voltage divider network consisting of R7, R8, and R9 is connected between the plate of phantastron sweep tube V2 and the -300 volt repeller supply to the

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# **ELECTRONIC CI RCUITS**

klystron local oscillator. Resistor R8 is a potentiometer to permit manual adjustment of the local oscillator voltage for approximately the proper frequency.

In normal operation, the application of plate voltage to phantastron tube V2 causes the plate to draw current, which decreases the plate voltage abruptly because of the high resistance of R4. This drop is applied through capacitor C3 to the control grid. The control grid voltage will not decrease far enough to cut off the plate current, since the source of voltage is in the plate circuit. The plate voltage  $e_n$ now begins to decrease gradually while the control grid voltage  $\mathbf{e}_{\mathbf{g}}$  of V2 now rises slowly as C3 discharges, causing plate voltage  $e_p$  to continue to drop and produce a negative-going output sweep voltage as shown in the accompanying waveform illustration.

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Since the plate current of a pentode remains nearly constant over a specific range of plate voltage, the discharge of C3 is fairly linear. When the plate voltage drops sufficiently to reach the bend or knee in the tube  $\mathbf{E}_{\mathbf{p}} \cdot \mathbf{I}_{\mathbf{p}}$  characteristic curve the plate current no longer remains constant and decreases toweard zero. Since the cathode current of the phantastron is essentially constant, the screen grid draws the current not being drawn by the plate, and the screen voltage drops. This drop in screen voltage is applied to the suppressor grid through C4 and develops a suppressor voltage across R6 which causes an additional drop in plate current. The process is regenerative and soon cuts off the plate current. The plate current remains cut off until C4 discharges sufficiently to allow the plate to start drawing current again. During plate current cutoff C3 charges. This circuit action is repeated at a rate of about one cycle per second, developing a negative sawtooth sweep at the plate of the phantastron. As the negative sweep voltage is applied to the voltage divider consisting of R7, R8, and R9 the klystron repeller voltage becomes more negative, and the klystron frequency increases.

Normally, the discriminator stage is connected to produce negative output pulses for an intermediate frequency greater than 30 MHz. Since these pulses are inverted by the pulse amplifier stage and produce a positive pulse input to the cathode of search stopper diode V1 through Cl the diode will not conduct, and the klystron frequency is permitted to rise until the intermediate frequency becomes less than 30 megacycles, at which time the discriminator produces positive output pulses. At this point the locking action begins to take place. The positive discriminator pulses are amplified and inverted by the pulse amplifier stage. The input to the cathode of the search stopper now is a series of negative pulses which cause the diode to conduct. After a few pulses capacitor C2 is charged sufficiently by the voltage drop across R2 to hold the phantastron grid bias constant. The gradual decrease of V2 plate voltage now ceases and stops the negative sweep of repeller voltage, and the repeller voltage is held constant at this point. A small displacement of the intermediate frequency form 30 MHz will exist in order to maintain a charge on C2, and keep the phantastron plate at the desired potential.

If the klystron local oscillator frequency or the magnetron transmitter frequency now change to

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produce an i-f greater than 30 MHz, positive pulses are applied to the search stopper diode to prevent it from conducting and the negative going plate voltage sweep continues until it brings the intermediate frequency back to 30 MHz. If the drift is in the opposite direction and causes the intermediate frequency to further decrease in frequency the search stopper diode conducts heavier and develops a larger bias on the grid of V2. Tube V2 now acts like an amplifier and the plate current decreases as the negative grid bias increases, developing a positive voltage swing in the output across the plate voltage divider. Thus the klystron frequency is lowered to bring the intermediate frequency back to the normal 30 MHz difference value.

#### Failure Analysis.

**No Output. Loss** of plate or screen voltage due to failure of the power supply, or if resistor R4, R7, R8, R9 and R5 are defective, or a defective tube V2 can make the circuit inoperative and produce a no-output condition. Measure the positive and negative supply voltages with a voltmeter to make certain that the supply or a blown fuse is not the fault. Check the resistance of R4, R5, R7, R8, and R9 with an ohmmeter for continuity and proper value. If the resistors are satisfactory and the voltages are normal, V2 may be at fault. Usually failure of any other components will produce an improper sweep or a constant output rather than none at all.

Low **Output. Low** supply voltage, a defective tube V2, or a change in value of resistors R4, R5, R6, R7, R8 and R9 can produce a low output. Check the supply voltage with a voltmeter, and the resistor for vahre with an ohmmeter.

**Improper Sweep.** Normally, with no input to search stopper tube VI, a constant negative output sweep voltage should occur about once each second, indicating that V2 is operating normally. A faster or slower sweep indicates that V2 is not operating correctly. A faster sweep will indicate reduced time constants such as a shorted resistor or lower valued capacitor, while a slower sweep indicates an increased time constant such as a larger vahre of resistance or capacitance. Check the values of R2, R3, and R6 with an ohmmeter, and check C3 and C4 with an in-circuit capacitance checker. If circuit voltages are normal and the capacitance and resistance are satisfactory, V2 is most likely at fault. It is usually necessary that the afc circuit be adjusted so that the local oscillator

frequency cannot pass through the wrong sideband, or improper locking will result.

Constant Sweep. A constant sweep with no lock-in occurring indicates either a faihrre of the search stopper circuit, diode V1, or failure of the preceding pulse amplifier or discriminator stages. Check for a pulse input from cathode to ground of V1 with an oscilloscope. If pulses exist on the input side of C1 but not across R1, capacitor C1 is open. If pulses exist across R2, either C2 is shorted, or VI is defective. If the voltage at the anode of VI is low, check the values of R1 and R2 with an ohmmeter and the capacity of C2 with a capacitance checker.

# THYRATRON AFC CIRCUIT

#### Application.

The thyratron afc circuit is used in radar or other electronic equipment to maintain the i-f frequency within the receiver pass band, and minimize the effect of local oscillator drift.

Utilizes two thyratrons, functioning as relaxation oscillators.

Changes an error voltage input into a sweep voltage output.

Sweeps continuously with no input.

Sweep speed changes for a change in error voltage.

#### Circuit Analysis.

**General.** The thyratron afc system provides a means of controlling the frequency of a klystron local oscillator. The output of the receiver discriminator is coupled through a pulse amplifier stage, and is applied to the input of the first relaxation oscillator (hence-forth referred to as the search stopper). A frequency hunting afc system is necessary because of the relatively large oscillator frequency drifts encountered in high frequency radar. Two thyratrons provide a coarse and a fine tuning system, in which the sweep generator brings the i-f frequency within range of the search stopper. The search stopper, in turn, acts as the fine tune control, tuning the klystron **locl** oscillator so as to produce precisely the correct i-f frequency for lock-in.

System design is such that it sweeps a large band of frequencies, and locks onto the desired frequency when it reaches the discriminator cross-over point. An error voltage from the discriminator cross-over point.

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An error voltage from the discriminator controls the speed of the search stopper (the first thyratron), and in the absence of an error voltage, such as when the transmitter is not operating, the sweep generator (second thyratron) hunts continuously. When the transmitter is operating, and when the i-f frequency is within the receiver bandwidth, the error voltage is supplied by the discriminator, the value of which determines the output of the search stopper.

Circuit **Oparation.** A schematic diagram of a thyratron afc circuit is illustrated in the accompanying schematic.



## **Thyratron AFC Circuit**

Thyratron VI is the search stopper, functioning as a relaxation oscillator. Capacitor. Cl is the input coupling capacitor, and R3 is the grid resistor. Capacitor C2, connected between the plate and cathode of V1, determines the repetition rate of the search stopper. R1 and R2 form a resistive series charge path for capacitor C3, which determines the repetition rate of sweep generator V2. R4 is the grid resistor for V2, and R5 and R6 form an output voltage divider, to supply a portion of the output to the repeller of the klystron. Bias supply Ecc<sub>2</sub>, applied to the grid of each tube, determines the firing point of the thyratron. Variable resistor R7 permits setting the repeller voltage to the proper value so that the sweep generator output causes the klystron local oscillator to hunt by an equal amount above and below the cross over frequency.

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If the transmitter is operating, and the local oscillator and the transmitter differ by approximately the intermediate frequency, the search stopper receives a series of pulses from the discriminator (one pulse for each pulse of transmitted energy). The time constant of capacitor C2 in the plate circuit of the search stopper is such that it charges sufficiently to allow VI to fire once for every three or four discriminator pulses at the input. When the thyratron ionizes, the plate potential drops to a voltage which is very close to the cathode potential. This is due to the low conduction resistance of the tube. The capacitor begins to rapidly discharge, and as soon as it discharges sufficiently, the tube deionizes. Immediately upon deionization, the capacitor begins recharging, and the cycle repeats. The search stopper continues to ionize and deionize at the same rate, as long as the pulses from the discriminator remain at the same amplitude. These sawtooths generated by the search stopper are smoothed out to a pulsating dc voltage, by the RC network in the plate circuit, and are applied to the repeller of the klystron. Under these conditions, the klystron repeller is kept at its proper operating voltage, and the i-f frequency is correct. If there is a change in the intermediate frequency because of local oscillator drift, the amplitude of the pulses arriving at the input to the search stopper changes. For an increase in the i-f frequency, the pulses for example, decrease their amplitude. Since the amplitude of the pulses on the grid are now less positive, C2 in the plate circuit must charge to a higher voltage to ionize the tube. Thus it takes a longer period of time for the tube to reach the ionization potential, and the repetition rate is slowed down. A slower repetition rate produces a lower average plate current, so that the average plate voltage is increased in a positive direction. This voltage change appears at the repeller of the klystron, and the klystron local oscillator changes its frequency accordingly, automatically correcting the i-f frequency.

For a decrease in the i-f frequency, the opposite condition prevails. The pulses arriving from the discriminator arrive at a greater amplitude, causing V1 to ionize more frequently, and produce a higher average plate current. The higher plate current causes the average plate voltage to decrease, and this decrease (a change in the negative direction) is applied to the repeller of the klystron. The more negative repeller voltage changes the klystron local oscillator frequency accordingly, and the change in the i-f frequency produced by oscillator drift is corrected.

During the time that VI controls the repeller voltage, sweep generator V2 remains cut-off, because its plate voltage is not positive enough to allow it to ionize. The search stopper's ability to vary the repeller voltage, however, is limited. If the i-f should drift too far off frequency, the search stopper no longer receives pulses of sufficient amplitude from the discriminator to ionize V1, and the plate voltage increases towards the value of supply voltage Ebb. It is under this condition that the sweep generator tube is activated. As the plate voltage begins rising, C3 in the plate circuit of V2 begins charging, and the output voltage to the repeller begins increasing positively. The ionization point of the tube is established by grid bias Ecc<sub>2</sub>, and as soon as C3 charges sufficiently to bring the plate voltage to the proper level, the tube ionizes, rapidly discharging C3, and dropping the plate voltage (and thus the repeller voltage) to almost cathode potential. When the capacitor discharges sufficiently, the tube deionizes, and C3 again begins charging, repeating the cycle. The sweep output which is generated by this action is applied to the repeller. As the sweep voltage rises (during the time that V2 is deionized), the repeller voltage also rises and the local oscillator frequency changes accordingly.

When the sweep voltage at the repeller reaches the proper voltage to produce the correct i-f frequency, search stopper tube VI once again receives operating pulses from the discriminator, and prevents V2 from ionizing, stopping the long sweep and locking-in the local oscillator. Once again search stopper tube V2 "fine tunes" the local oscillator, until the next large oscillator frequency shift occurs, whereupon the long sweep cycle repeats.

## Failure Analysis.

**No Output.** A defective V1 and V2, an open resistor RI, R2, R5, R6, or R77, a shorted C2 or C3, or the loss of supply voltage can cause a no-output condition to exist. Check RI, R2, R5, R6, and R7 with an ohmmeter for proper value. Check capacitors C2 and C3 for value, or possible shorts or opens with an in-circuit capacitor checker. Measure the plate supply voltage, and the bias supply voltage with a voltmeter for proper value, and correct if necessary.

**Continuous Hunting.** The loss of input from the discriminator, an open Cl or C2, or an open R3 can

cause the failure of the afc system to lock on to the current frequency. With an oscilloscope, check for the presence of the pulses from the discriminator at the input. If not present, a defect is present in some preceding circuit, and the afc system is probably not defective. If a signal is present, thyratron V1 maybe at fault. Check R3 with an ohmmeter for proper value, and check capacitors C 1 and C2 with an in-circuit capacitor checker for proper value.

No Hunting. A defective thyratron V2, an open C3, or an open R4 are the only components which can cause the system not to hunt when the frequency drifts beyond the control of the search stopper. Check resistor R4 with an ohmmeter for proper value, and capacitor C3 for proper value with an in-circuit capacitor checker.

# REACTANCE TUBE AFC CIRCUIT

# Application.

The reactance tube afc circuit is used in radio receivers when it is desired to maintain the local oscillator frequency or the output of the mixer stage of the receiver at a specific frequency, which is always in the i-f pass band.

# Characteristics.

Converts an input voltage change to a reactance variation at the output.

Controls the frequency of the receiver local oscillator.

Utilizes a triode, with cathode (self,) bias.

#### Circuit Analysis.

**General.** In the basic reactance tube AFC system, a reactance tube is used to change the resonant frequency of the receiver local oscillator by an amount and direction which corresponds to the amount and direction of the frequency shift of the incoming signal. If the i-f frequency of the input changes, it causes the discriminator to produce a dc voltage at its output having an amplitude and polarity which is proportional to this change. It is this dc voltage which is applied to the grid of the reactance tube. The reactance tube circuit is connected across the tank circuit of the local oscillator, and its characteristics are such that a change in reactance across the oscillator tank circuit. Thus, the resonant

frequency of the local oscillator tank circuit changes, compensating for the frequency drift in the i-f stage.

**Circuit Operation. A schematic** diagram of a basic reactance tube AFC control circuit is illustrated.

 $C^{4}$   $E_{bb}$   $C^{3}$   $C^{3}$   $C^{3}$   $C^{3}$   $C^{4}$   $C^{1}$   $C^{1}$   $C^{1}$   $C^{2}$   $C^{$ 

**Basic Reactance Tube AFC Control Circuit** 

Triode VI is the reactance tube, using cathode bias, supplied by resistor R2 and capacitor C2. LI is an r-f choke which keeps the r-f out of the plate voltage supply. L2, together with C3, is the oscillator tank circuit, connected across the C1-R1 combination. Cl and R1 make up the variable capacitive reactance circuit, and capacitor C4 prevents the d-c from being applied to the oscillator tank circuit. The error voltage from the discriminator is applied between the grid of VI and ground, as shown on the illustration

With no error voltage applied to the grid of VI, the only voltage present across the C1-R1 network is the voltage across the oscillator tank circuit, L2 and C3. The values of Cl and R1 are chosen so that the reactance of Cl is large in comparison to the resistance of R1, permitting the capacitive reactance to be the current controlling component, and causing the voltage across it to lag the current through it by approximately 90 degrees. Since the same current which flows through Cl also flows through R1, and since this current leads the applied voltage by 90°, it produces a voltage drop across the resistor which leads the applied voltage by 90 degrees. The reactance tube is effectively in shunt with the oscillator tank (C3 and L2) and the phase shift network (Cl and R1). Capacitor C4 allows the ac component of

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current to pass through it, and at the same time, prevents the dc plate voltage from being applied to the phase-shift circuit and the tank.

The relationship of the currents and the voltages in the circuit can be best explained through the use of a vector diagram, as shown in the following illustration.



Relationship of Currents and Voltages with no Modulation Input

Voltage  $\mathbf{e}_{\mathbf{p}}$  is the alternating component of the plate to ground voltage which appears simultaneously across the reactance tube, the phase-shift network and the oscillator tank circuit. The ac grid-input voltage is applied across R1. This voltage drop across RI is in phase with the plate current  $\mathbf{i}_{\mathbf{p}}$  and the grid current,  $\mathbf{i}_{g}$ , a relationship characteristic of amplifier tubes.

Since both  $i_p$  and  $i_g$  are in phase with  $e_g$ , and since  $e_g$  leads  $e_p$  by approximately 90 degrees,  $i_p$  and  $i_g$  also lead  $e_p$  by 90 degrees. both of these currents are supplied by the oscillator tank circuit, and since they lead the tank voltage, they act like the current in a capacitor. Thus the injection of these currents into the tank circuit accomplishes the same effect as placing a capacitor across the oscillator tank circuit. The frequency of the tank in this case is, therefore, decreased. With no error voltage applied at the input, this frequency is the operating frequency of the local oscillator.

If the i-f frequency drifts, the output of the mixer changes, and the discriminator produces an error voltage at its output which is proportional to the drift in i-f. This error voltage is produced as result of the input frequency to the discriminator being different than the frequency to which it is tuned. The amplitude and polarity of the error voltage is determined by the amount and direction of the frequency drift, respectively.

Consider now the application of this error voltage to the grid of the reactance tube. It is important to keep in mind that we are not speaking of actual capacitive reactance or capacitance changes. Our concern here is an *effective* capacitance produced by the leading current in the R1-C1 combination. If the voltage applied to the grid of VI increases in a positive direction, the plate current of V1 also increases, and since this current is an effective capacitance shunt across the oscillator tank circuit, the frequency of the oscillator is decreased. Conversely, when the grid signal shifts in a negative direction, V1 plate current decreases, and since this current is an effective reduction in capacitance across (shunting) the oscillator tank circuit, the frequency of the oscillator is increased.

To summarize, a positive error voltage causes an increase of frequency, while a negative signal causes a decrease in frequency. Likewise, a large amplitude error voltage causes a greater frequency change than a smaller amplitude error signal.

If resistor R1 and capacitor Cl were reversed, and their values were changed so that the resistance of R1 becomes large in comparison to the reactance of Cl, circuit operation will be reversed. The result of the change is that an inductive (lagging) current is injected into the local oscillator tank circuit instead of a capacitive (leading) current, as in the previous example. A positive error voltage will now produce a decrease in local oscillator frequency, and a negative error voltage will produce an increase in local oscillator frequency.

# Failure Analysis.

**No Output.** An open or shorted L1, an open R2 or C4, the absence of the plate supply voltage, the absence of the input error voltage, or a defective VI may cause a no-output condition to exist. Check L1 for an open, and R2 for proper value with an ohmmeter. Check capacitor C4 for value with an in-circuit capacitance checker. Check for the presence

of the plate supply voltage and the presence of the input error voltage with a voltmeter. If plate voltage is not present, either choke L1 is open or the power supply is defective. If an error voltage is not present the trouble is in the discriminator or i-f stages. If the output is still not restored with normai plate and input voltages, the tube is probably at fault.

**Improperly Controlled Output.** A defect in nearly any component in the circuit can produce a condition in which the afc circuit does not control the local oscillator. Check **L1** for continuity, and capacitors Cl, C2, and C4 with an ohmmeter for opens or shorts, and resistors R1 and R2 for value. Check for the proper value of plate supply voltage, and the correct error voltage. If the condition still exists, check all capacitors with an in-circuit capacitor checker for their proper value. Also, do not neglect the possibility that the discriminator may be detuned from the proper frequency, causing the frequency to shift in the wrong direction.

# DC AMPLIFIER AFC SYSTEM (ELECTRON TUBE)

# Application.

The dc amplifier afc system is used in cw, radar, or radio applications where a slowly varying dc error voltage is used directly to produce automatic frequency control action.

#### Characteristics.

**DC** coupling is used between the discriminator and control stage.

No afc sweep is used (it is a non-hunting system). The error voltage is generated by a discriminator. Can be used on either CW or pulsed systems.

# Circuit Analysis.

**General.** The dc amplifier system forms a simple tracking system for a reflex klystron. It uses a discriminator to convert any deviation from the i-f amplifier center frequency into bias variations which are applied to the grid of a dc amplifier. Since the plate of the dc amplifier is connected to the repeller of the klystron local oscillator, any variation of the grid bias varies the plate voltage of the. dc amplifier and thus the repeller voltage of the klystron. This, in turn, varies the frequency of the local oscillator in such a direction as to return the local oscillator to the

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proper frequency with respect to the transmitter frequency. The system requires manual adjustment of the klystron resonator and of the repeller voltage, to bring the difference-frequency signal within the bandpass of the afc discriminator, before the system can produce any tracking action. Although this system will compensate automatically for slight frequency variations of the transmitter, or of the local oscillator, it will not correct the klystron frequency if ever the difference signal falls outside the bandpass of the afc discriminator. Such a situation commonly occurs whenever the receiver is turned on after having been inoperative for a number of hours, and necessitates a manual readjustment of the repeller voltage. More complicated afc systems use a simple search sweep to obviate the necessity for initial adjustment.

**Circuit Operation.** A schematic diagram of a typical dc amplifier afc circuit is shown in the accompanying illustration.



**DC Amplifier AFC Circuit** 

A Weiss discriminator is used to supply the dc afc error voltage. Capacitors Cl and C2 couple the discriminator to the last i-f stage. Inductor L1 is slug tuned to the i-f or crossover frequency. Resistors RI and R2 are diode return resistors which effectively center-tap the tuned input circuit, thus half the input voltage is impressed across each diode. L2 is an r-f choke which forms part of the dc return to the load resistors. V1 and V2 are the discriminator diodes, with R3 and R4 acting as load resistors. Capacitors

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C3 and C4 filter the i-f ripple from the output and furnish a practically pure d-c output from the discriminator. The grid of dc amplifier V3 is connected to the cathode of V1 and through diode load resistors R3 and R4 to a negative bias supply. This forms the quiescent or resting bias above and below which the discriminator output varies V3 grid. Resistor R5 is the plate resistor for dc amplifier and also forms a portion of a voltage divider comected between the positive and negative power supplies, consisting of R5, R6, R7, and R8. Resistors R5, and R7 and R8 limit the range over which R6 operates, and R6 is variable and used to manually adjust the klystron repeller voltage for the desired center frequency. Normally, with the local oscillator tuned so that the i-f is at the center frequency, say 30 megacycles, L] offers a maximum impedance and equal voltages are supplied to the plates of diodes V1 and V2. Thus equal load currents flow through R3 and R4 in opposite directions and develop equal and opposing voltages. Hence there is no change in bias on V3 and the klystron reflector voltage is not affected, so there is no change in frequency. Coupling capacitors Cl and C2 are unequal in value and are designed to control the peak separation of the tuned input circuit. When the transmitter frequency increases, the i-f increases and a more positive output voltage is applied to V1, and a lower output to V2. Consequently, VI conducts more heavily than V2 and a large positive output voltage is developed at the cathode. This positive increase in bias causes the plate current of dc amplifier V3 to increase, lowers the plate voltage, and consequently increases the negative repeller voltage. As a result, the local oscillator frequency increases and returns the i-f difference frequency back to its orignal value.

Conversely, when the transmitter frequency decreases, and a negative output voltage is applied to V1 while a more positive output is applied to V2. Diode V2 now conducts more heavily than V1 and a large negative voltage is developed across R4. The negative output developed across R4 is larger than the positive output across R3, so that the grid of V3 is driven in a negative direction. The increased positive output across R5 produces an effectively less negative repeller voltage and the klystron is shifted in the correct frequency direction to compensate. These changes are slowly varying dc voltages for cw operation. For pulse operation, design is such that the filter capacitors are quickly charged by the **low** resistance

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path through the diodes, while the discharge is slow through the high resistance shunting load resistors. Thus an effective pulse stretching action is produced which provides well filtered dc for pusle control.

# Failure Analysis.

No Output. Lack of klystron voltage or improper repeller voltage can cause a no-output condition. Check both the positive and negative supply voltages with a high resistance voltmeter to determine that a fuse or the supply is not at fault. Do not neglect the fact that potentiometer R7 may be misadjusted and cause the klystron to operate on a frequency out of range of the discriminator. Lack of reflector voltage on the klystron may be caused by a defective R7 or R8. Check the resistors for proper value with an ohmmeter. Resistors R5 and R6 will affect the klystron voltage also, and may be checked with an ohmmeter. If resistors R5, R6, R7, and R8 appear satisfactory and the power supplies are normal, tube V3 may be drawing abnormal current and preventing circuit action. Normally, failure of the discriminator or input circuit will show as an inability to provide

proper local oscillator action rather than no output at all. If resistor R3 or R4 opened, or if the grid of V3 were shorted, lack of grid bias on the dc amplifier might cause the local oscillator to operate outside the range of the discriminator. Check the voltage from V3 grid to ground and the values of R3 and R4 with an ohmmeter.

Improper AFC Action. Usually improper afc action can be isolated to a malfunction in the discriminator. Diode VI and its associated circuit controls i-f shifts in a higher frequency direction, that is when the output of V1 is positive. When lower i-f shifts occur they are controlled by V2 and its associated circuit. If either C 1 or C2 were shorted a continuous positive plate voltage would be applied V1 or V2 and cause the repeller frequency to increase greatly. If the capacitors were open, afc control would only occur in one direction, depending upon which capacitor is open. Use an in-circuit checker to check for the proper capacitance value. Use an ohmmeter to check L1 and L2 for continuity, and also RI, R2, R3 and R4 for proper value. Check C3 and C4 for proper value with a capacitor checker.

# SECTION 12 MODULATORS

# PART 12-1. AM

#### AMPLITUDE MODULATION (ELECTRON TUBE)

## General.

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Modulation is the process by which a signal (or signals) containing intelligence (modulating signal) is impressed on some other signal (usually a radio frequency, called the carrier). There are three basic methods for accomplishing modulation:

**Amplitude Modulation.** In this method the modulating signal and carrier signal are combined in such a manner as to cause the amplitude of the resultant waveform to vary in step with the changes in the modulating signal.

**Frequency Modulation.** In this method the output frequency is varied in accordance with the modulating signal.

**Phase Modulation.** In this method the phase of the output signal is varied in accordance with the modulating signal. Only amplitude modulation will be discussed in this paragraph.

Usually, in amplitude modulation, the modulation varies at an audio rate because the intelligence to be transmitted consists of voice, music, or other audio frequencies; the signal which is modulated is a radiofrequency signal of a constant amplitude and frequency, known as the r-f carrier. As will be seen later, once the modulation is achieved, the r-f carrier is no longer necessary and need not be transmitted, or may be transmitted at a reduced amplitude, for certain special applications.

Modulation is normally achieved by varying the voltage applied to one of the elements of an electron tube, and the modulator circuits are classified accordingly. For example, varying the grid bias of a tube to obtain modulation is known as grid modulation, while varying the cathode voltage to obtain modulation (a similar process) is called cathode modulation. Modulators are further subdivided into two general classes - high level and low level. The high-level modulator usually employs plate circuit modulation; it usually modulates the final (output) stage of a transmitter, and it usually requires an audio power

amplifier (modulator) capable of supplying 50 percent additional power over the normal maximum unmodulated output of the final transmitter amplifier stage for 100 percent modulation. The low-level modulator usually modulates a stage perceding the final stage of the transmitter. The exact audio power required depends upon the stage modulated. When low-level modulation is employed then the stages following the modulated stage must be operated as linear power amplifiers.

Strictly speaking, high-level modulation is defined as modulation produced at a point in the system where the power level approximates that at the output of the system. Low-level modulation is defined as modulation produced at a point in a system where the level is low as compared with the power level at the output of the system. This does not mean that high-level modulation must always be applied to the plate of the output tube or that lowlevel modulation is always applied to the grid of an intermediate stage. In some Navy equipment, modulation applied to the grid circuit of the power amplifier is referred to as *low-level modulation*. A combination of plate and screen modulation is referred to as *highlevel modulation*.

High-level modulation seems to predominate in the low- and moderate-power fields, since it gives somewhat better efficiency and less distortion for the same powers. However, in the extremely high-power field or where broad-band stages are necessary (as in television), low-level modulation seems to be preferred. Theoretically, with the same amount of sideband power, both modulation methods are equal.

The original concept of the modulated signal was that of a basic carrier frequency with an envelope which varied with the modulation impressed upon it, as shown in the following illustration. This concept is still valid, but is misleading in as much as it appears that for the signal to be reproduced, the carrier is required. Further analysis and investigation have proved that when modulation is accomplished, three signal frequencies are generated. One frequency is higher in frequency than the carrier by the frequency of the modulating signal; the second is the middle

frquency, or carrier; the third frequency is that of the lower sideband, which is lower than the carrier by the frequency of the modulated signal. The sidebands are produced by mixing the audio modulating frequency against the carrier to produce the sum and difference frequencies, At the time modulation is accomplished, and at the time of detection or demodulation, the carrier is required, but it can be either partially or entirely suppressed from the output as long as a similar signal (with same phase and polarity) is reinserted at the receiver; It must also be understood that each sideband is independent, and contains exactly the same moduating frequencies as the other sideband, being displaced in frequency above and below the carrier by this amount. Thus the carrier and one (either) sideband can be eliminated, which is done in single-sideband operation.



#### Modulation Envelope

Since the sideband frequencies are transmitted along with the carrier frequency, it is evident that the total bandwidth occupied is twice that of the modulating frequency. Therefore, the modulated signal requires more space than the unmodulated signal. Since frequencies up to 3000Hz must be reproduced for good, intelligible speech, it can be seen that a 6-kHz bandwidth is necessary for radiotelephony using AM double sideband. For single-sideband operation on a basis, with only one sideband transmitted, only 3kHz is required. To broadcast music and speech with reasonably good quality, a 10-kHz bandwidth is required when using AM double sideband.

As stated before for plate modulation, a 50% increase in power above the normal carrier power is required to achieve 100% modulation. The following figure illustrates these conditions. Thus each sideband contains one-half of the total audio power supplied (that is, 25 percent of the carrier power). For the composite signal, however, the carrier contains 66-2/3% of the total energy, with 33-1/3% of the total energy represented in the two sidebands. That is, approximately one-sixth of the total power is contained in each sideband (50 + 200 + 50), or a total of 300 divided on a 2-to-1 basis). To achieve this result, the modulator must drive the modulated amplifier plate voltage down to zero and then twice the normal plate voltage, as illustrated previously. Since the peak power varies as the square of the plate voltage, a peak power of four times normal is produced at 100% modulation. For plate modulation a Class C biased r-f amplifier is used because its output varies linearly with plate voltage. To produce lowlevel modulation a Class B linear amplifier is employed, in which the output varies as the square of the excitation voltage. The Class B amplifier is adjusted for maximum output and then reduced to one-quarter maximum output and driven to four times this power on peaks. Or, as is generally done with most of the efficiency types of modulation, the plate current on the output stage is adjusted (by changing the output load) for one-half maximum plate current (the output varies as the square of the plate current) and the peak power output is four times normal. In any event, plate modulation is characterized by a steady d-c plate current indication, and low-level and efficiency types by a varying d-c plate current indication. In each case the results are similar as far as amplitude variations are concerned;

however, the distortion and linearity vary from type to type.



Modulation Amplitude and Power Relationships

The amount of modulation is expressed in percentage based upon the amplitude of the carrier. When the amplitude of the modulated signal reaches twice the carrier amplitude on positive peaks and reduces to zero on negative peaks, as illustrated above, the modulation is 100% At any in-between values the modulation is less than 100Yo. Since the power in the sidebands varies as the square of the amplitude, it also varies as the square of the modulation percentage. Therefore, for a 50% modulated signal the sideband power is only one-quarter of that available at 100% modulation. It is evident, then, that the percentage of modulation must always be kept as near 100Yo modulation as possible. When the modulation exceeds 100%, the negative peaks cross the zero level and the signal is effectively chopped off, creating carrier shift, distortion, and severe adjacent-channel interference with other stations. For a sine-wave signal the amplitude variations above and below the average are even. There are other waveforms, however, which are not equally spaced or symmetrical, such as speech. Certain speech sounds contain large positive peak components and if the system is properly polarized, the negative component is of smaller amplitude. In this special case it is possible to modulate more than 100% on positive peaks without causing carrier shift. Therefore, the criterion for 100% modulation is generally considered as being the amplitude at which the negative peaks are just driven to zero, regardless of the positive peak amplitude. On the same basis, since speech is complex and not a sine wave, it can easily be seen that setting the modulation level with a tone signal for 100% will result in a loss of modulation, as only occasional peaks will reach this value. Thus the general practice of advancing the gain control so that occasional positive peaks exceed that value required for 100% modulation produces more effective speech communication with a slight amount of distortion and external interference. In the design of modern transmitters and speech equipment for voice communication, peak clippers are used to permit a greater average level of modulation without exceeding the 100% limit. For broadcast and highfidelity transmissions, however, the modulation must be set so that the peaks never exceed 100%.

Because the intelligence which is impressed as modulation on the carrier is of prime importance, the modulator (and output stage) must be linear; that is, it must produce a minimum of distortion. Distortion

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**can** be caused by incorrect amplitude, extraneous (spurious) frequencies injected during the modulation process, phase shift at some frequencies exceeding that at others, and other conditions. These items will be discussed as the circuits are analyzed.

Since modulation involves an increase of power in the modulated stage, it is important that the electron tubes used to supply the output signal have sufficient reserve **emission** to permit 100% modulation on peaks; otherwise, the signal will be clipped. Also, the tubes must be operated at reduced ratings so they will handle the excess power dissipated during modulation without exceeding the voltage and current ratings for the elements. With good design the tubes will operate without showing any sign of plate heating, and under average conditions they may show just a trace of color on modulation peaks.

# AMPLITUDE MODULATION (SEMICONDUCTOR)

# General.

Although the same general conditions must be fulfilled to achieve amplitude modulation with semiconductors, the semiconductor usually operates at a much lower power level that the electron tube; also since it is a low-impedance device, it operates on the principle of current gain or variation. Thus, instead of speaking of varying the voltage from zero to twice normal to achieve 100-percent modulation, the general practice is to speak of varying the *transistor gain* to achieve modulation. (This is similar to control grid modulation.)

Since the gain of a transitor is dependent upon the voltages applied to its electrodes, it is evident that changing the dc bias or the ac signal to any one of its three terminals will produce a corresponding change in gain. Therefore, it is possible to produce AM modulation of a transistor by any of three basic methods, namely, base injection, emitter injection, or collector injection. Each of these basic circuits are discussed later in this section.

At present, semiconductor modulators operate over a relatively low power range as compared with that of electron-tube modulators. In the majority of applications they are operated over a range of milliwatts, with the range of from 1 to 100 watts representing special and high-power applications. As highpowered r-f and audio transistors are developed, this power *range* will be extended so that it will be more comparable to that of the electron tube. Although it operates at low power levels, the performance of the transistor modulator is approximately equal to that of the vacuum-tube modulator as far as fidelity and efficiency are concerned. Their small size, ruggedness, and economy of power consumption make them particularly useful as low-power modulators for small portable and mobile equipments.

# CHOKE (HEISING) MODULATOR (ELECTRON TUBE)

## Application.

The choke (Heising or constant current) modulator circuit is used to produce 100% high-level plate modulation of the transmitter output stage. In the early days of radio it was the most popular modulator circuit because of its simplicity and economy of parts, plus good performance.

# Characteristics.

Uses a single choke in an impedance-coupled arrangement to match the modulator to the output stage.

Operates at a higher voltage level than the transmitter output stage.

Can be adjusted to obtain 100% modulation or more.

It is the most economical modulator from a cost standpoint.

It is not as efficient as the transformer-coupled circuit.

## Circuit Analysis.

General. There are three versions of this type of circuit two of which will not be discussed further than to indicate their form and the reasons for omitting the discussion. One version uses a tapped choke, which is usually connected as an autotransformer. Basically, then, the tapped-choke type is equivalent to the transformer-coupled type except for the transformer's isolation of the primary and secondary windings and the effects incidental thereto. Also, it is practically as expensive to build the tappedchoke circuit as the transformer-coupled circuit, so little is gained by its use. In the second version the transmitter plate voltage dropping resistor is not used, so that 10070 modulation cannot be obtained; therefore, it is considered a less desirable circuit. The remaining circuit to be described is the basic Heising circuit, which is also known as a "constant current"

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modulator. This latter name is derived from the use of a common choke in the power supply lead, which tends to keep a constant current flowing; thus when the transmitter current reduces because of modulation, the modulator current increases a like amount, and vice versa. A simpler and more easily understood analogy is to consider that the modulator output voltage is equal to the plate voltage applied to the transmitter, and that on positive peaks they add, making the instantaneous total plate voltage equal to 2Eb; on negative peaks they subtract and drive the voltage to zero. Thus the instantaneous voltage varies from zero to two times maximum, and the current does likewise. For this type of circuit the modulator is simply a Class A power amplifier capable of supplying 33-1 /3% of the total transmitter output power (50% of rated carrier power, neglecting losses). Since a Class A amplifier is normally linear, the instantaneous signal varies equally for positive and negative signals (assuming equal drive, equal signals, and no distortion); thus the average plate current remains steady (for 100% or less modulation) and does not vary as indicated by a plate meter. The instantaneous signals, however, are constantly varying in accordance with the modulation impressed.

The Heising circuit has not been very popular up to now because of its lack of plate efficiency, and because advances in the art have developed other more efficient modulator circuits requiring much less audio power. However, the Heising circuit once again is gaining in popularity because of its simplicity, and does serve as a basic circuit for studying and understanding basic modulator principles, thus leading to an understanding of other types of modulator circuits.

**Circuit Operation.** A typical choke modulator circuit is shown schematically in the following figure. For simplicity and ease of discussion, only the pertinent circuit parts are shown, as the basic modulator may be applied to any transmitter amplifier or oscillator stage. Functionally, V1 is a Class A audio power amplifier, which is impedance-coupled through choke L1 to r-f power amplifier V2 operating Class C. See the Amplifier Section of this Handbook for a discussion of a-f and r-f power amplifier circuits.



Typical Choke (Heising) Modulator Circuit

From an inspection of the illustration, it is evident that V2 is a conventional r-f amplifier, with the output tank circuit shunt-fed. The RFC keeps the rf out of the modulator and the dc power supply, which in this circuit is connected through choke V1 and dropping resistor R1. Resistor RI is adjusted to keep the applied d-c plate voltage of V2 at a value less than that at the plate of modulator tube V1. Capacitor Cl is selected to offer minimum reactance at the lowest usable frequency so as to pass the lower audio frequencies around R1 without attenuation. Since the higher frequencies are offered much less attenuation, Cl effectively bypasses R1 completely for the audio frequencies (assuming that the modulation is audio). The grid drive of V2 is considered to be more than that necessary to drive the tube to saturation, with a dc bias voltage of twice the amount needed for cutoff operation. Therefore, V2 is operating as a Class C amplifier and is assumed to be linear. That is, the plate current and r-f tank current of V2 vary linearly with a change in plate voltage. Thus, as the instantaneous plate voltage of V2 is varied, the instantaneous

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plate current and r-f tank current vary likewise. In this mode of operation, V2 appears as if it were a pure resistance connected between R1 and ground, and the value of this resistance is:

$$R_p = \frac{E_{\bar{p}}}{I_p}$$

The output of V2 is designed to produce the proper plate current at full load for the plate voltage set by Rl, to produce the desired plate load resistance for modulator V1.

Tube V1 is operated as a Class A audio amplifier, with cathode bias supplied by  $R_k$  bypassed by  $C_k$ . In this case the method of supplying bias is immaterial; it can be any of the methods applicable to a power amplifier. The modulator input to the grid of V1 is shown transformer-coupled, but can be by any method that will supply sufficient drive. Since the tube is operating Class A, no grid current is drawn, and only sufficient voltage need be supplied to operate the tube over the linear portion of the tube grid-plate transfer characteristic. When the input (modulation) signal goes positive, the plate current of V1 increases and produces a voltage drop across choke L1 in a negative direction; for a negative input the plate current of V1 decreases, reducing the drop across L1, so that effectively the voltage at the plate of V1 increases (goes positive). Since tube V1 normally operates at a quiescent value of current and voltage (Class A biased), the result of an input signal is to instantaneously increase or decrease the plate voltage and current in accordance with the grid modulation. When the plate voltage of V1 goes positive, the polarity is such that it adds to the source voltage  $E_{bb}$  obtained from the power supply; when it goes negative, the source voltage is reduced. It can be seen then, that at the peak of the negative modulator swing, the maximum positive instantaneous plate voltage applied to V2 is the sum of the dc power supply voltage, set by R1 and the audio component on the plate of V1 coupled through Cl. If properly adjusted, the audio voltage developed by V1 will just equal the dc voltage supplied V2, and the instantaneous plate voltage supplied to V2 will be zero, while on the positive modulator swing it will be twice that of the normal applied d-c plate voltage. Without resistor RI in the circuit, the plate voltage of V1 would have to be driven to zero to reduce the instantaneous plate voltage of V2 to zero. When reduced to zero no plate current would flow in V1, the tube

would no longer operate Class A, and distortion would be produced. Likewise, on the positive swing, the d-c voltage drop through L1 would be subtracted from the V2 plate voltage, and the instantaneous plate voltage would never reach the two-times-normal value. With R1 correctly adjusted, the d-c plate voltage of V2 is always less than that of V1, and the positive and negative swings of V1 are sufficient to drive the plate voltage of V2 from zero to two times normal, thus producing 100% modulation. It is evident that, since the output of V2 is varying linearly in accordance with the plate voltage swings produced by the modulating signal, V2 is amplitudemodulated. When the plate voltage of V2 is increased, the plate current is increased also. To increase the plate voltage of V2 instantaneously, it is necessary for the plate current of V1 to be reduced during that instant. Choke L1 supplies the energy for this power change through its collapsing field as the plate current of V1 reduces. Thus the power supply current drain remains substantially constant, even though the instantaneous variations of current and voltage in this circuit are from zero to twice the normal value; hence the derivation of the term constant current modulation, as applied to the average dc drain.

The modulated tube (r-f amplifier) must be operated at below maximum ratings of tube current and voltage during modulation because of the possibility that the instantaneous variations of voltage and current will exceed the safe ratings during sustained peaks of modulation when the peak power is four times maximum. Conversely, the modulator tube (which supplies half the power taken by the r-f amplifier) is at best only 30% efficient as compared with 70 to 8070 for the r-f amplifier, and is subject to the same range of instantaneous voltages and currents (or peak power). Therefore, this type of modulator usually uses a tube of equivalent or greater power rating than the r-f amplifier being modulated. Like the Class A amplifier, the modulator just discussed produces the least amount of distortion; however, because of its low efficiency, it has become practically obsolete in favor of other more efficient types.

Vacuum Tube Considerations. While the preceding circuit discussion was based upon triodes, this modulator may be used with other types of electron tubes if the proper electrode voltages and currents are applied. For screen-grid tubes of the tetrode, beam, or pentode type, it is important that the modulation be applied to the screen grid as well as to the plate.

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This is usually accomplished by using a series voltagedropping resistor from the plate to screen, for screen voltage supply, so that both electrodes have the same modulation impressed upon them. Thus, as the screen controls the plate current, it permits full swing on positive peaks and reduced swing on negative peaks, effectively aiding the modulation process. The reduced swing on the negative peaks prevents the plate voltage from falling below that of the screen and creating a virtual cathode. Since the series screen resistor does not permit plate current cutoff, bias is chosen on the basis of projected cutoff for a fixed screen voltage under quiescent conditions. In addition, the power from the modulator must be sufficient to supply the screen modulation power, or about 10Yo additional. In circuits using a fixed screen voltage supply, 100% modulation is achieved by inserting a series choke of about 5 henries between the screen and the screen supply. The electrical inertia of the choke produces on effect similar to the constant current action. When the plate current is greatest and tends to increase beyond the limits fixed by the screen voltage, the plate robs the screen of electrons and decreases the screen current. Whereupon, the reduction of current through the choke produces an induced voltage because of the collapsing lines of force in the choke field. This voltage is in the direction which continues current flow (that is, an increase in screen voltage), and the effect is similar to that caused by the modulation superimposed on the series screen comection. Likewise, on the negative peaks of the modulating signal, the screen current tends to increase, because less plate current is drawn and the screen tends to become the plate. The increased screen-current flow through the screen choke produces an opposing voltage, which tends to decrease the screen voltage and the total current Wrmissible, and reduces plate swing. Thus the raising and lowering of screen voltage with modulation is simulated by the choke, permitting practically 1007o modulation. Without the choke the modulation is limited to about 90 to 95%.

#### Failure Analysis.

**No Output.** Lack of output should first be isolated to either the transmitter r-f amplifier or the modulator circuit. Even though the modulator is operative, an open RFC or tank circuit, a shorted or gassy electron tube, or a lack of grid excitation in the amplifier will produce a no-carrier indication.

Checking the r-f amplifier plate meter will indicate whether the circuit is complete and whether a resonant dip can be obtained; also, a check on the grid drive meter will determine whether excitation exists. Lack of grid drive indicates trouble in the transmitter, while lack of plate current places the trouble in either the transmitter or the modulator. Where the modulator plate meter indicates but the transmitter does not, the probability is an open dropping resistor, open RFC, or poor transmitter tube; the trouble can be isolated with a high-voltage voltmeter (turn off the high voltage and use a shorting bar before connecting the meter). If both the modulator and transmitter meters are not indicating, either the power supply is defective or modulator choke L1 is open. With both meters indicating but with no modulation, either a shorted modulation choke, a bad modulator tube, or lack of modulator drive may be suspected. High plate current usually indicates short-circuited components or lack of bias, while low plate current indicates excessive bias, highresistance joints, or poor tube emission. Voltage checks on the grid and plate elements will indicate continuity as well as terminal voltages. No output generally indicates lack of voltage, lack of continuity, or short-circuit conditions. A resistance check to ground will be helpful, but is normally unnecessary. With the voltages and currents usually involved in high-power transmitters and modulator, breakdowns are usually obvious from external symptoms such as arcing, charring, and burning; on low-power equipment additional test equipment may have to be used. But remember, DANGEROUS voltages are involved; take all safety precautions before connecting or disconnecting any test equipment.

Low Output. It must first be determined whether the low output is lack of audio power or reduction in percentage of modulation. While low modulation is normally due to lack of sufficient audio power, this can occur from a reduced setting of the audio driver gain control, or from trouble in the speech amplifier stages which drive the modulator. An oscilloscope is very useful in determining the cause of malfunctioning since the waveform may be directly observed. For simple, quick tests of modulation percentage, the trapezoidal pattern is useful. The waveform check, however, can show both percentage of modulation and distortion, and is more useful. Too high a grid bias will cause a reduction of output (with the same

drive). A short-circuited coupling capacitor will eliminate the dropping resistor for the r-f amplifier, so that the percentage modulation will be reduced, and even with increased drive the 10070 level will not be reached. But, since the capacitor is shunted by the dropping resistor, such trouble is rather infrequent. On the other hand, since the dropping resistor is constantly carrying the current of the r-f amplifier, it will most likely change in value with age. If it increases in value sufficiently, over-modulation will occur, even though the stage can be loaded by antenna coupling adjustments to the operating value of current. While the modulator load will be correct, the reduced voltage will permit less swing; thus the same audio output will overdrive and cause carrier shift, as indicated by a varying plate meter with modulation. Note that normally with modulation, if the power supply regulation is insufficient in either the transmitter or the primary a-c supply line, there will be some movement of the plate current meter. Overmodulation will be indicated by more than normal movement. Where the power supply regulation is satisfactory, the normal meter indication will be rock-steady, and any meter movement will indicate overmodulation or a distorted condition.

A modulation choke that has partially shorted turns may not be easy to locate from external appearance, but will probably show up as low power output, as well as insufficient and usually distorted modulation. Ordinarily, this condition can be located only by substitution of a new choke after the other parts have been eliminated by systematic analysis.

Lack of fdament emission in the r-f amplifier or modulator tube will cause peak clipping and inability to obtain 100% undistorted modulation.

**Distorted Output.** Distortion is usually obvious when monitoring audio modulation. It may occur from a number of causes. For example, overmodulation will cause carrier shift, severe interference with other stations, and distortion. Changing of the modulator load impedance, by adjusting the r-f amplifier output loading for different currents than normal, will change the modulator load line; depending upon the magnitude of the change, this condition may be easily detected, or a special check may be required to determine the amount of distortion. Any change of grid bias will shift the operating point and require a change of drive. With low bias the input will be clipped and distorted, and with high bias a larger input signal will be required; thus speech amplifier distortion will most likely be increased. Should the bias reach the Class B point, actual plate current cutoff will cause distortion, while with Class AB operation there is the possibility that grid current being drawn on peaks may cause some distortion. Thus the region of operation between Class A and Class B becomes somewhat of a problem. With proper drive and with symmetrical modulation, little or no distortion will occur; on the other hand, with improper drive and with large unsymmetrical or sustained peaks of modulation, excessive distortion can result.

Lack of sufficient plate voltage will cause a reduction of plate swing, and thus cause distortion by plate clipping. Shorted modulator turns can cause an insufficient inductive effect to produce the amount of modulation required, and thereby result in distortion. A change in the value of the coupling capacitor will result in different attenuation for different frequencies, so that attenuation of these frequencies (usually the low frequencies) will cause another form of distortion,

Lack of sufficient fdament emission in the r-f amplifier (and modulator) tubes will cause peak clipping, produce distortion, and make it impossible to obtain 100% modulation.

# PLATE MODULATOR

#### Application.

**The** transformer-coupled plate modulator circuit is used to produce high-level modulation of the transmitter r-f output stage. It is used for both low- and high-power applications, particularly where it is desired to use a triode as a high-level modulator.

# Characteristics.

Uses a transformer to match the modulator stage to the transmitter output stage.

Supplies an audio (modulator) output equivalent to one-half the dc input power of the r-f output stage.

Operated class A for a minimum of distortion with low efficiency and low output, or class B for highest efficiency with some distortion. When operated between the two classes (Class AB or AB ), intermediate values of efficiency and distortion are produced.

# **ELECTRONIC CIRCUITS**

Uses triode type electron tubes only (see Transformer-Coupled Plate and screen Modulator circuit for tetrodes).

#### Circuit Analysis.

**General.** Before reading this discussion, read the introduction to this section covering Amplitude Modulation for background. A better understanding of the various voltage and current relationships in class C amplifiers will also be obtained by reviewing RF Power Amplifier Circuits (Class B or C) for both single-ended and push-pull applications, in the Amplifier Section of this Handbook.

The *high-level plate modulator* uses the audio output of a conventional *a-f power amplifier* (the modulator) to produce a modulated r-f output signal in the *plate* circuit of the transmitter r-f amplifier connected to the antenna. A typical high-level system is shown in the accompanying block diagram. The *transformer-coupled plate and screen* modulator which is used with screen-grid tetrodes and pentodes employed as the final RF power amplifier is a variation of this type of modulator circuit; it is discussed separately later in this section of the handbook.



High-Level Modulation System

High-level modulation is defined as modulation produced at a point in the system where the power level approximates that at the output of the system. Therefore, plate modulation always involves considerable power output from the modulator. For 100-percent modulation, the plate modulator must produce an output equivalent to 50 percent of the dc input power to the final r-f power amplifier. For an

r-f power amplifier having an efficiency of 80 percent and an r-f carrier output power of 100 watts, the total dc input power would be 125 watts. The power required from the modulator would be one half of this, or 62.5 watts, and the resulting output to the antenna would be 100 watts of carrier power and 50 watts of audio (sideband) power. For high-power operation the circuit must incorporate design considerations to prevent corona loss, arcing and flashover, and damage or destruction of parts. On the other hand, for low-power applications as in mobile operations, the audio power is relatively small (for example, 50 percent of 5 watts is only 2.5 watts) and may be handled by receiving type audio amplifier output stages. Regardless of power output, however, the basic principles of operation are the same.

Modulation involves frequencies other than audio, such as video (television) or pulses (control systems, or telemetry); however, since modulators are conventionally associated with audio frequencies, other types of signals which may affect modulator circuit operation are discussed only as required to bring out the manner in which they differ from audio use. The accompanying chart illustrates some typical ranges of frequencies involved for various forms of modulating signals.



**Frequency Ranges Required** 

The maximum power from a particular transmitter with a given type of electron tube operating at its maximum ratings can be obtained when operating the transmitter in the Al **(CW)** mode of emission. When

using the A3 (AM) mode of emission, the power output for plate modulation is about 20 percent less than for CW operation. The reason for this is that during plate modulation, at the peak of the modulation cycle (at 100% modulation), the plate voltage is doubled and the input power is increased by a factor of four. In order that the maximum tube ratings will not be exceeded, the tube must be operated below its normal operating point as a class C amplifier. Other factors that affect the power output from a platemodulated stage are the loading of the antenna (the amount of antenna coupling) and the value of the load impedance that the r-f amplifier presents to the modulator. The power output of the modulator and the amount of distortion it develops are directly dependent upon the loaded value of plate current and voltage applied to the r-f stage.

The plate efficiency of the high-level, modulated r-f stage is constant at about 70 percent, and does not change with modulation. Therefore, the r-f output (carrier) produced by a given type of electron tube with no modulation is at a maximum value in the plate-modulated high-level transmitter (although not as large as can be produced for CW operation). Lowlevel modulation, using the same type of electron tube, produces a carrier output of half this value. The reason for this is that during low-level modulation the tube efficiency varies with the percentage of modulation. At no modulation the efficiency is approximately 33 percent, and represents the condition of greatest tube loading (maximum plate dissipation because of low efficiency). At the peak of modulation the highest efficiency (about 66 percent) is obtained. Although the plate voltage and current are doubted to produce a four-time power increase at the peak of modulation .(which is necessary for all AM modulators), the low-level modulator must obtain this increase from the transmitter power supply. In the high-level modulator, the additional power required for modulation is obtained from the modulator.

Since in high-level plate modulation the modulation occurs in the final stage of the transmitter, the r-f driver stages can be operated more efficiently (they need not be linear as in the low-level transmitter); therefore, they can be operated without considering distortion to produce maximum r-f output. Hence, the r-f section of the high-level platemodulated transmitter is most efficient for r-f production, and its power supply need only be large enough to supply the power required to produce the r-f carrier. When fully modulated, the audio output (modulator) stage of the high-level modulator supplies an additional 50 percent of the power required to produce the carrier. The additional power supplied by the modulator represents the output power in the sidebands, which is equal to 50 percent of the carrier (25 percent in each sideband). Therefore, the total average power output of the high-level plate-modulated stage at full modulation is 1.5 times the unmodulated (carrier) power.

Since the low-level modulator must be operated at a carrier level which is one-quarter of the maximum power obtainable from the same type of electron tube in high-level operation, it is adjusted to operate at one-half the maximum plate current. Thus it is clear why, for a given type of electron tube, the highlevel modulated stage produces a greater power output. To do this, the audio (modulator) stage must also produce considerable power (to supply the 50 percent additional (sideband) power necessary for 100 percent modulation). For high-power transmitters such a powerful modulator is costly and involves special component design to operate at the high voltages and currents required.

The various power relationships and differences between high- and low-level modulation methods will become clearer and will be more fully explained as the various modulator circuits involving these methods are discussed. It should be borne in mind, however, that regardless of whether operation is at a *high level* or at a low *level*, the *equivalent ratings are the same*. For example, a 1000-watt 100-percent modulated transmitter produces the same output whether or not the modulation is accomplished by high-level or low-level methods.

Circuit **Oparation.** A simplified diagram of the basic transformer-coupled plate modulator is shown in the accompanying figure. The a-f modulator stage is represented as a block since it may be any one of a number of audio amplifier combinations as long as the proper audio power output is obtained. Likewise, the r-f output stage is also represented as a block since it may consist of any arrangement of tube(s) to produce the desired carrier output to the antenna. The r-f output stage is always biased so that it operates as a class C amplifier. Since class C operation requires a bias of two times the cutoff value, a separate bias supply is used to provide fixed bias. Since the r-f excitation to

# **ELECTRONIC CIRCUITS**

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the r-f- stage is relatively constant, grid leak bias (produced by grid drive) is also used, with the total bias being the combination of the fixed and grid-leak (grid-drive) bias. In case of failure of the grid drive, the fixed bias provides a protective bias to prevent the final bias provides a protective bias to prevent the final-stage tube ratings from being exceeded.



**Basic Transformer-Coupled Modulator** 

With no modulation applied, the carrier r-f output is developed by the application of the normal dc plate voltage to the plate of the class C stage, with sufficient r-f grid drive and antenna loading to produce the desired r-f carrier. When modulation is applied, the audio output of the modulator is applied through the secondary of T1 in series with the dc plate voltage, and adds to or subtracts from this voltage to produce an instantaneous plate voltage which increases the r-f output to 1.5 times the rated carrier power at 100 percent modulation. To do this, the plate voltage of the r-f stage is varied from two times the normal plate voltage at the positive audio peak down to zero on the negative peak, both varying in accordance with the modulating frequency.

**Class A Modulator. The** schematic diagram of a simple triode modulator which operates to modulate a triode r-f output stage is shown in the accompanying figure.



#### **Triode Plate Modulator**

This single-tube triode modulator can be operated class A, Al, or A2, depending upon the fidelity desired and the amount of distortion that can be permitted. Class A operation provides the best fidelity with the least amount of distortion, but uses a large power input to obtain a small power output (highest efficiency), with usable fidelity for the amount of distortion allowed. Class Al operation is intermediate between these two levels.

Although the modulator driver may be r-c coupled, if the modulator is operated class A2, grid current is drawn. Therefore to minimize grid-voltage drop and the development of a reverse bias which will seriously affect the operating point and produce excessive distortion, it is necessary to provide a low-impedance grid circuit. Thus the illustration shows

transformer coupling to the modulator. Through the use of a transformer with taps, the driver stage can be made to operate at the desired load point to produce maximum audio output with minimum distortion by selecting the taps that provide the required turns ratio for matching impedances (output to input). Thus the input and output impedances of the transformer can be selected for sufficient distortiordess voltage drive at all times, including the time during which the modulator grid draws grid current (when the positive drive peak voltage exceeds the modulator grid bias). Modulator bias is produced by cathode resistor RI, which is bypassed to prevent degeneration (see the introduction to the Amplifier Section of this Handbook for a discussion of degeneration effects). Since cathode bias is used, current must flow throughout the cycle to produce the bias; therefore, this circuit is limited to class A operation (a class B modulator will be described later). Since transformer coupling is used, T1 in the input and T2 in the output, the frequency response is somewhat limited (see introduction to amplifier section for explanation of transformer coupling response limitations). Because of a loss of low and high frequencies causing a nonuniform audio response, the modulation signal is similarly affected. In practice, this condition is overcome by opeating the modulator at less than the maximum output over the mid-range of frequencies, and by providing bass and high frequency boost to provide reasonably linear response over the audio frequency range when necessary. Actually, for ordinary speech transmissions the desired frequency response is usually easily obtained with transformers of good design, but for the higher audio frequencies and for video applications special design is required, including both high and low boost compensating circuits.

Since the output of the modulator is developed across transformer T2, the transformer must be provided with the proper load impedance to produce the desired output (both voltage and power) from V2. This is achieved by employing the transmitter output tube (a class C r-f stage) as the load across the secondary of T2. The r-f stage can be used as the audio load because radio-frequency choke RFC presents a high r-f impedance to the r-f signal developed by tube V3 and prevents it from feeding back into, and being shorted out by, the power supply filter capacitor. Thus T2 remains unaffected by the rf and sees only a resistive dc path from the plate to the cathode of V3 and gound. This dc path is the effective resistance placed across the secondary of T2 (the modulator load), and is equal to the dc plate voltage applied to V3 divided by the dc plate current a simple Ohm's law relationship:

## R = E/I

Since the transformer has the inherent property of transforming impedance in accordance with the square of the turns ratio of primary to secondary, with a multi-tapped transformer it is possible to select the proper turns ratio to make the dc plate resistance \_ of V3 properly match V2 for maximum output. (Taps are not necessary if the proper ratio is used, but they do provide a convenient and easy method for load matching.) Final adjustment of the load is achieved, once the proper turns ratio is obtained, by setting the output coupling of V3 for the exact plate current at the rated plate voltage.

Transmitter output amplifier V3 operates as a conventional shunt-fed r-f amplifier, with combination freed and grid-leak bias being supplied by R2, which is bypassed by C4. The plate voltage is applied in series with the secondary of transformer T2, and C2 is the conventional shunt-feed coupling and dc blocking capacitor which connects tank L1, C3 to the plate of V3. In addition to the bias supplied by R2, fixed bias is applied through RFC<sub>1</sub> to the grid of V3 from a separate "C" supply. Thus the final bias applied to V3 is the sum of the fixed and grid-leak bias voltages, with the fixed bias providing protection in case of failure of the grid-drive (r-f excitation). The r-f output of the transmitter driver stage is capacitively coupled to the grid of V3 by Cc. When the grid of V3 is driven above its bias level by the r-f grid drive from the buffer amplifier, plate current flows and develops an r-f voltage across the parallel resonant tank circuit consisting of L1 and C3, which is isolated from the modulator by the RFC. An r-f output is thus produced in the inductively coupled antenna circuit. When the modulator is operated at static values of plate current and voltage, the output is the r-f carrier signal, with no modulation applied.

Assume that a sine-wave input is applied to Vl, the modulator driver stage. On the positive excursion of the input signal (with proper phasing of transformer connections) modulator tube V2 produces a positive output voltage at the secondary of T2. Since T2 is connected in series with the transmitter plate supply, the plate voltage of transmitter output tube V3 is effectively increased and made more positive, so that the output of V3 also increases. Thus a positive modulation signal produces an increase of r-f voltage and output power in the transmitter output stage. At the peak of the sine-wave modulating signal (100% modulation), T2 supplies an instantaneous positive voltage equal to the dc voltage supplied by the transmitter power supply. These two voltages add, so that the plate of V3 operates at twice normal voltage, as shown in the following figure.



Equivalent Plate Voltage at 100-Percent Modulation

The dc applied voltage is E<sub>b</sub>, and the instantaneous ac plate voltage component is  $e_p$ ; when added, they produce the maximum instantaneous voltage, em, which varies throughout the cycle as shown by the heavy line; this is the effective plate voltage,  $e_{\rm b}$ . When  $e_m$  equals  $2E_b$ , the instantaneous plate voltage is twice the normal dc value, thus producing a plate current which is also twice the normal value. As a result, the instantaneous (peak) power output is four times the normal (carrier) value. As the sine-wave modulation signal decreases, it reaches the zero (no modulation) level or starting value, and the r-f amplifier plate voltage consists of the dc supply voltage alone, which produces normal carrier output, completing the positive half cycle of modulation. In a similar manner, as the modulating since wave goes through its negative alternation, it produces a negative voltage in the secondary of transformer T2. At the peak of the negative half-cycle, the voltage at the secondary of T2 exactly equals that of the dc power supply feeding V3, but it is not opposite polarity. Thus both voltages cancel (instantaneously), and the instantaneous voltage applied to the plate of V3 is

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zero. At this time the r-f output is zero. The r-f output rises to the normal carrier value as the negative halfcycle of the modulating sine wave goes positive, and returns to zero at no modulation. Thus, by varying the instantaneous plate voltage, the sinewave modulating signal produces a similar and amplified sine wave of r-f voltage at the plate of V3, which is coupled to the tank and thence to the antenna, where the modulation envelope is radiated. It is an amplified replica of the original sine-wave modulating signal. Thus, it can be seen that during modulation by a sine wave, the instantaneous r-f output power of the transmitter varies as follows: it is increased from its normal carrier value to four times normal, it is reduced to zero, and it is returned to the original carrier level. Therefore, in a plate-modulated amplifier, during modulation the instantaneous power varies from zero to four times normal, and the instantaneous plate voltage and current vary from zero to twice normal to produce 100 percent modulation, as shown in the following illustration.



Modulation Power Relationships

Actually, only the instantaneous values of current and voltage change, and these vary at the rate of the modulating signal. For a sine wave applied over a complete cycle, the positive and negative variations are equal and opposite; since the plate meter cannot follow the audio variations at the carrier frequency (and the average value is unchanged), the dc plate current appears to remain steady at the normal input value without modulation. Therefore, as long as the positive and negative alternations average out to zero, the plate meter remains steady. In practice, however, this is true only if there is perfect regulation of both modulator and r-f amplifier plate supplies. Since the plate current is instantaneously varying in both tubes and since the voltage regulation is usually not perfect, there is a slight amount of meter movement with modulation. On the other hand, when the negative alternation exceeds the normal carrier level, the plate current is cut off for the time that the zero voltage line is exceeded, as shown in the following figure.



Effect of Excessive Negative Drive

Such interruption of the carrier appears as a noticeable jump in the plate meter indication each time the negative peak is exceeded. In actual practice, the r-f amplifier (transmitter) tube is not driven to zero plate voltage, because at zero plate voltage the current would become zero and the carrier would be interrupted in the same manner as when the negative peak is exceeded. To prevent such undesirable action, the modulator is adjusted to swing the r-f amplifier plate voltage between predetermined minimum and maximum values. Such adjustment prevents cutoff of the carrier (provided these values are not exceeded). It

also prevents excessive interference, known as splatter, from being produced by the chopped-up carrier. When the carrier is interrupted, it acts as if it were a highly damped wave instead of a continuous wave. This type of emission is a form of ICW (interrupted continuous wave), and is similar to that produced by spark transmitters and some types of noise generators. Instead of a single frequency, a number of harmonics and spurious frequencies are produced in bursts each time the carrier is interrupted. Thus the radiation is spread over a spectrum of a few hundred kilohertz about the carrier frequency, and causes ... interference to other signals since the receiver cannot tune it out. The actual plate voltage relationships in the transmitter tube plate circuit are shown in the following figure, together with the actual instantaneous plate cathode voltage. Since the transmitter stage is operating class C, current flows for less than a half-cycle, usually somewhere between 120 and 150 degrees. Therefore, the illustration shows operation on only one side of the zero line during the conducting period. The smooth envelope which varies above and below the zero level, as shown by the plate-cathode voltage, is the result of tank 'circuit action. Although pulses are supplied to the tank, since the tank circuit charges and discharges sinusoidally, any output taken from the tank, directly or indirectly, will also be sinusoidal. Thus, the upper and lower portions of the plate voltage  $(E_{h} + em)$  effectively add and subtract from the tank current. The result is the production of the modulation envelope shown, since the tank provides the impedance across which the rf is generated, and sees no zero level. In addition to supplying what might be considered as the missing half of the modulation waveform, the tank is also the frequency-selecting device, permitting only those frequencies within its pass band to be amplified. If the tank is too selective (has a high Q), some of the sideband frequencies may be cut off, in which case distortion is produced because of the missing frequencies. For radiotelephony the Q is usually 10 to 15 to prevent excessive selectivity. For CW (unmodulated) signals it can be much higher. For very wide band transmissions, as in television, it must be much lower. The highest sideband frequencies to be transmitted determine the allowable Q of the tank circuit.

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Plate Voltage and R-F Voltage Relationship

The transmitter output amplifier is always operated class C to produce linear modulation with high efficiency. In class C operation, the power output of an r-f amplifier varies as the square of the plate voltage while the plate current varies directly with the plate voltage. Therefore, a high-level plate modulator can be used to vary the effective plate voltage in accordance with the modulating signal and produce an output which varies exactly as the modulating signal. The r-f amplifier acts as a resistive load on the modulator because the plate tank is tuned to the same frequency as the r-f grid-driving signal. Since the tank appears as a resistive load, the plate voltage and plate current are in phase. Therefore, the current flow is limited only by the effective resistance in the plate circuit, which can be determined by the simple Ohm's law relationship of E/I. Although the r-f amplifier could be operated class B and modulated with the plate modulator, serious distortion would be produced because the r-f class B amplifier output varies as the square of the input voltage and not linearly with plate voltage. For full efficiency and minimum distortion, the class B r-f stage would be better modulated by applying the modulation to its grid circuit. In this case it would be operated as a linear r-f amplifier with low-level modulation.

The modulator can be operated class B (instead of class A) provided that two tubes are employed (one for each half of the audio cycle).

**Class B Modulator.** Since class B audio amplifiers provide a more efficient modulator and are in popular use, a schematic of a typical class B driven plate modulator is shown in the accompanying illustration.





The actual operation of the class C modulated stage is exactly as just described for the class A modulator. The difference between them is in the manner in which the audio modulation is obtained. When the output of preamplifier V1 is applied to Tl, the grids of V2A and V2B are simultaneously driven in opposite directions. These tubes are class B zerobias tubes, which are normally inoperative without grid drive (although with some tube types a small plate current may flow). When tube A is driven positive, the grid of tube B is driven further negative. On the opposite half-cycle, tube B is driven positive and tube A is driven below cutoff. The current pulses produced in the plates of each tube flow through the primary of modulator transformer T2 in opposite directions, and are added together in the secondary to produce the complete and amplified replica of the signal applied to the primary of driver transformer T1. The output of the secondary of T2 is connected in series with the plate voltage of the r-f stage, V3. On the positive alternation, the plate of V3 is driven to twice the normal plate voltage; on the negative alternation, the audio output voltage is of opposite

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polarity and reduces the instantaneous plate voltage of V3 to almost zero. Thus, the circuit operates as previously described. For a more detailed and complete story on the operation of class B audio amplifiers, see the discussion of the Push-Pull (Class A, AB, and B) Audio Amplifier, in the Amplifier Section of this Handbook.

Capacitor Cl, across the secondary of T2, is a simple high-pass filter, which attenuates any high frequencies produced on modulation peaks to prevent splatter. Capacitor Cl is not necessary for operation of the modulator, but it does minimize distortion products produced by overmodulation on voice peaks.

The plate of r-f stage V3 is shown with series plate feed, rather than shunt-feed as is used in the class A modulator previously discussed, to illustrate that there is no essential difference between the two. In either case, the secondary of modulator transformer T2 is connected so that the audio output is in series with the dc plate voltage applied to V3, and the rf is isolated from the power supply and modulator by an rfc. To avoid loss of frequency response, C2 is limited to a size which will not bypass any of the audio modulation. Otherwise, the operation is identical with the operation of the class A modulator just discussed. In practice, the use of a class B modulator results in some problems with power supply regulation and audio distortion products. These effects, however, are all a part of the audio power amplifier design, and do not change the modulation action previously described.

**Detailed Analysis.** In the high-level plate modulator, the modulator consists of an audio power amplifier whose output is applied to a class C r-f amplifier which operates as both a mixer and a frequency and power converter to superimpose the modulation signal on the r-f carrier. A simplified equivalent circuit is shown in the following figure. The audio modulator stage is represented as a sine wave generator coupled by T1 to the plate circuit of the r-f stage, V1. The modulator functions exactly as any class A, AB, or B audio power amplifier capable of producing an audio output equal to one-half the carrier power of the r-f stage, with the desired fidelity. The instantaneous a-c output of the modulator at the secondary of T1 is represented by the



**Plate Modulator Equivalent Circuit** 

instantaneous voltage em. Under conditions of no modulation, e is zero and the power for the carrier is supplied by the transmitter power supply, represented by the voltage Ebb connected in series with e, and the plate of V1. Under modulation conditions, the additional power needed for 100 percent modulation is obtained from the modulator stage, which at 100-percent modulation must supply exactly one-half of the dc input power to V1 at zero modulation. The rfc isolates both modulator and power supply from the class C r-f stage, with  $C_1$ acting as a bypass to ground for any rf which might leak through the rfc. For the circuit to operate properly, the rfc must offer a very high impedance to the rf and little or no opposition to the audio modulation frequency, since it is desired to vary the plate voltage at the audio frequency. Although capacitor C<sub>1</sub>must have a low enough reactance to

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bypass the carrier frequency and a small range of sidebands around this frequency, it must not be low enough to bypass any of the audio output from the modulator. Otherwise, there will be a progressive loss of high frequencies and consequent lack of fidelity with a predominantly bass response. Since the plate current of V1 flows through the secondary of Tl, the effects of core saturation produced by the flow of  $1_{p}$ must be taken into account by the use of a heavier core than would normally be required for an ordinary a-f power output transformer. In addition, the transformer windings must have the proper power handling capacity (proper wire size) so as to handle the maximum current taken by VI. In this respect, the design of the output transformer of the audio modulator represents a slight difference from that of a conventional audio amplifier. Since the modulator output must produce considerable undistorted audio output power, it must be properly matched to the load. This is achieved by providing a transformer (preferably multi-tapped), which through the impedance transformation produced by the difference in turns ratio between primary and secondary provides the desired load impedance for maximum output with minimum distortion. The modulator load is essentially resistive, being the quotient of the dc plate voltage applied to V1 and the loaded dc plate current to which VI is adjusted. In the equivalent schematic, ebb represents the instantaneous applied plate voltage, which is  $E_{bb} + e_m$ . The voltage between plate and cathode is represented by  $e_b = e_{bb} - e_L$ , where e<sub>I</sub> represents the voltage drop across the r-f load offered by the tank circuit impedance. This load is represented by resistor R, which is the effective dc load presented to the modulator, and is equal to the applied dc plate voltage, Ebb, divided by the dc plate current, I<sub>p</sub>, neglecting the small dc resistance in tank coil L. Since the tank circuit is resonant, X<sub>c</sub> equals XL, and the tank appears solely as a resistive load to VI. Because the tank circuit is resonant to a single -frequency (the carrier) which is much higher than the relatively low modulating-signal frequencies, no audio voltage is developed across the tank. The instantaneous plate current is represented by ib, and the plateto-cathode resistance, which is equal to  $E_{\mu}A_{p}$ , in transformed by T1 to the proper value to load the modulator for maximum undistorted output. Although the instantaneous values of plate voltage and current change during modulation, the average values remain unchanged so that tube VI could be replaced

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by a resistor as far as modulator loading is concerned.

Consider now the grid bias applied by  $E_{cc}$ . This represents a freed negative bias, but actually may be a combination of protective cathode bias, fixed bias from a separate supply, and bias developed across a series resistor as a result of grid current flow produced by the r-f driver. The driver signal (r-f grid excitation) is represented by a-c generator voltage e, which on the positive half-cycle is polarized in opposition to the freed bias, as shown in the plate modulator equivalent circuit above. The effective grid voltage is the instantaneous value from grid to cathode, represented by e. The dc value of grid current is represented by I, and the instantaneous value, by i... The grid rfc isolates the bias supply from the driving source and prevents shorting the input to ground, and C2 acts as a conventional r-f bypass shunting the bias supply. An illustration o,f a typical bias circuit is shown in the following figure.



Typical Bias Circuit

When used, the cathode bias produced by cathode resistor  $\mathbf{R}_{\mathbf{K}}$  offers protection from excessive **plate** current when either the drive or freed bias fails. The cathode resistor is conventionally bypassed by  $C_{\kappa}$ . Usually cathode bias is used only when the freed bias supply is not employed, since double protection is unnecessary. For high-voltage transmitter tubes, it is also desirable to keep the cathode at ground potential, so cathode bias is used only in low-power applications. The freed bias is obtained from a separate bias supply and is usually set for about 1.5 times

cutoff, with the remaining bias (that developed by the r-f drive) being developed across grid leak  $\mathbf{R}_{g}$ . Placing  $\mathbf{R}_{g}$  after the rfc helps attenuate any rf which may leak through the rfc, and C2 bypasses any r-f residue to ground. Note that i flows in a direction which adds to the polarity of E,- so that the total effective bias value is **fixed** by the amount of grid drive from the preceding r-f amplifier. Normally, tube V1 operates in a lightly saturated condition, that is, where an increase of grid excitation will not increase the plate current very much, if at all, but an increase of plate voltage will, as explained below.

The following figure illustrates how the output voltage varies with an increase of excitation before and after saturation is obtained. Since fixed bias is used the output is zero for values of excitation lower than the cutoff-bias voltage with a corresponding high plate to cathode voltage. As the cutoffbias voltage is exceeded plate current flows and the drop across the load, EL, becomes greater while the plate-to-cathode voltage is reduced. When the drive reaches the value at point 1 on the curve, the tube is just starting to saturate (light saturation), and it takes much more drive to increase the current sufficiently to develop an appreciably greater output voltage. At this point the effective plate voltage reaches its minimum vahre (approximately), which is the applied value **less** the drop across the load (Ebb  $- E_1 =$  $E_{mm}$ ). At this point the tube is operating most efficiently and produces an output voltage almost as great as the applied voltage. At point 2 heavy saturation is obtained, and it takes almost twice as much drive to obtain a slightly greater output. If the applied Vohage,  $E_{bb}$ , is increased, a greater drive is required to reach saturation, and a greater output voltage results.





It can be seen, then, that when the excitation is adjusted for saturation at the peaks of modulation, during the resting or carrier condition the drive will be much more than is required. Thus it is evident that while the r-f drive voltage is essentirdly constant, it will tend to vary somewhat in accordance with modulation and loading. Under resting conditions, the grid current is about the rated tube value, and produces the remaining bias needed (plus the fixed bias) to attain twice the plate current cutoff value. When an input is applied to the modulator grid, the output at the plate of the modulator adds to the plate voltage, and more plate current flows. At the same time, if the grid excitation is obtained from a source which is barely able to supply the required drive at modulation peaks, the effect of poor regulation is obtained and the grid current tends to decrease (the source cannot supply more excitation). At the peak of the modulation cycle, the r-f grid excitation is made just sufficient to drive the tube to twice normal

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plate current (assuming perfect linearity). The tendency of the grid current to decrease during modulation peaks lowers the effective bias (since it is partially produced by grid drive) and permits a greater plate current to flow, producing the same effect as though the drive were increased at the peak of the cycle, just when the most drive is needed to handle the increased plate voltage. Since the grid current is at a minimum at this time, it represents the lowest drive power during the operating cycle and the grid dissipation is also the lowest. Conversely, as the modulation decreases and reaches the trough of the signal, the effective voltage applied to the plate  $(E_m i_n)$ in the preceding figure) is the lowest, since the modulation and dc plate voltage are canceling each other; and the drop across the load is at its lowest with an output voltage just greater than zero. For best efficiency,  $E_{min}$  is made just equal to  $e_{c}$ ; hence, the grid becomes more effective than the plate (since it is closer to the cathode), and more electrons are attracted to the grid, increasing  $i_c$ . As  $i_c$  increases, the grid dissipation becomes greater since the tube is also overdriven, having much more drive than is needed to swing the small plate current at the minimum plate voltage. The result is excessive heating of the grid.

By using grid-leak resistor  $R_g$  (together with the fixed bias), the effect of poor regulation in the grid circuit is achieved. Thus the excessive grid dissipation caused by the low plate voltage at the trough of modulation (discussed above) is reduced. The waveforms in the following figure illustrate the use of the grid leak in providing poorer grid regulation and improved operation. At the peak of the modulation, the reduction of grid current caused by poor regulation from the source produces less voltage drop in the grid leak, and the bias is reduced as before (but to a larger extent). On the other hand, as the modulation trough is reached, the increase of grid current (because of the increased drive, since the plate voltage is now low) produces greater grid bias, which is the same as reducing the drive, just at the time it is needed least. Thus, the addition of the grid leak helps reduce grid heating, and helps the plate reach its maximum and minimum swings so that full 100percent modulation is achieved. Although the circuit operates satisfactorily without the grid leak, use of the grid leak results in less distortion and cooler tube operation.



Grid-Leak and Fixad Bias Relationships

Note that, while the instantaneous grid current and grid voltage change, their meter indications appear as an average steady dc value since a sinusoidal symmetrical modulating signal is being applied. Therefore, as in the constant-current system, proper operation is indicated by steady grid and plate current indications (assuming perfect power supply regulation and neutralization of the r-f output stage).

Assuming no modulation and a steady input to the plate of the r-f amplifier, with the proper load coupling a steady r-f carrier is produced. As the modulating signal is applied, the power in the plate circuit and in the tank of the r-f stage is increased to a peak value of four times normal (output power varies as the square of the plate voltage). Since the tank circuit cannot absorb all the additional power (the load does not change), the additional power mostly appears as an increase in output (except for the amount replacing the losses in the circuit and a small percentage wasted in extra plate dissipation). Because the modulator furnishes this power increase, it is clear that the r-f power supply furnishes only the carrier power, while the modulator provides the audio or sideband power. Hence, the reason for requiring the large amount of power needed for plate modulation. Although a peak power of four times normal exists, the average output over the entire cycle is only 1.5 times normal at full 100 percent modulation. That is, for a 100-watt radiated carrier modulated 100 percent by a continuous tone, the radiated power would be 150 watts total. For this condition, 25 watts

resides in each of the two sidebands developed by the modulation.

Other Considerations. Because of the requirement that the r-f amplifier tube handle peak powers of four times normal, the tube is operated 20 percent below the ratings for class C operation. Although the efficiency does not change during modulation, the plate dissipation is greater because more power is developed and applied. Therefore, the tube cannot be operated at maximum rating during periods of no modulation. As a result, the normal carrier output is less than the maximum output possible using the same tube unmodulated.

Since the tank circuit must pass both the carrier frequency and the sideband frequencies, the tank circuit Q is important. The half-power bandwidth of the tuned tank must be sufficient to pass the carrier frequency plus the sidebands which extend on each side to a frequency equivalent to plus or minus the highest modulation frequency. For example, if the modulation is 5 kHz and the carrier is 5 MHz, the half-power points must cover a range of 4.995 to 5.005 MHz; otherwise the sidebands will be clipped, causing 10ss of the bigher frequencies.

While too great a drive results in excessive grid dissipation, the r-f grid excitation to the class C stage must be great enough to drive the tube at twice normal plate voltage. Otherwise, on the peaks of modulation lack of sufficient drive will cause peak flattening with distortion. There must also be sufficient reserve electron emission to supply the peak power requirements, or peak flattening will also occur.

For efficient operation, the grid signal should never exceed the minimum plate voltage, or excessive grid current will flow. Excessive grid current will cause grid heating and a loss of efficiency.

# Failure Analysis.

No Output. Lack of output should first be isolated to either the transmitter r-f amplifier or the modulator stage. Even though the modulator is operative, an open rfc or tank circuit, a defective electron tube, or a lack of r-f grid excitation in the transmitter r-f amplifier will produce a no-carrier indication, and thus no output. Checking the r-f amplifier plate meter for current will reveal whether the circuit is complete, and whether a resonant dip can be obtained. A check on the drive meter (dc grid current) indication will also determine whether r-f excitation is present. Lack

of grid drive indicates trouble in the driver stages or transmitter power supply, and lack of plate current indicates trouble in the transmitter or in the modulation transformer. If the plate meter indicates at all, the trouble is probably in the r-f stages; if no indication is observed, the modulation transformer is open, the transmitter power supply is defective, or the plate circuit in the transmitter is open.

A no-output condition is generally indicative of lack of voltage, lack of continuity in the circuit, or a short-circuited condition. A resistance check to ground will be helpful, but is usually unnecessary. -With the voltages and currents commonly involved in high-powered transmitters and modulators, breakdowns are usually obvious from external symptoms, such as arcing, charring, and burning. On low-power equipment, additional test equipment may have to be used. But remember, DANGEROUS VOLTAGES are involved; be certain to take all safety precautions before connecting or disconnecting an test equipment.

A no-plate-current indication is usually indicative of an open circuit, or lack of continuity, which can be determined by a resistance check or a voltage check. Voltage checks on the grid and plate elements will indicate continuity as well as terminal voltages. A low-plate-current indication usually indicates lack of sufficient r-f drive, high-resistance joints (poorly soldered connections), low tube emission, or an excessively high grid bias. A high-plate current indication usually indicates short-circuited components or insulation breakdown, or a lack of sufficient grid bias. In the last two cases, check for proper grid voltage before making any other checks.

Low Output. It must first be determined whether the low output is due to lack of audio power or a reduction in the percentage of modulation. Although low modulation is normally due to lack of sufficient audio power, it can also be caused by a reduced setting of the audio drive gain control or by trouble in the speech amplifier stages which drive the modulator. An oscilloscope is very useful in determining the cause of malfunctioning since it permits direct observation of the waveform. For a simple quick test of the modulation percentage, the trapezoidrd pattern is helpful. The envelope waveform check, however, can show both percentage of modulation and waveform distortion, and is more useful in trouble analysis. Too high a grid bias (with the same drive) will cause a reduction of output. Insufficient r-f drive on

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the peaks of modulation will also cause flattening of the waveform peaks and prevent full 100-percent modulation. A similar effect is also obtained when the r-f amplifier plate voltage is too high for the amount of audio voltage supplied (indicating loss of modulator output), and when the modulator output exceeds the r-f plate voltage. In the latter case the negative peaks are clipped and carrier shift results, with accompanying distortion, reduced output, splattering, and a shifting plate current indication (this immediately pinpoints the trouble as overmodulation). Refer to the Basic Measurements section of NAVSHIPS 0967-000-0130, Test Methods and Practices, for specific modulation tests, oscilloscope connections, and waveforms.

Normally, with modulation, if the power supply regulation is inadequate in either the transmitter or the primary ac supply line, there will be a slight movement, or flicker, of the plate current meter during the process of modulation. Overmodulation will be indicated by a sharp noticeable movement each time the peak exceeds the maximum value, If the power supply regulation is satisfactory, the normal meter indication will be rock-steady, and any meter movement will indicate either overmodulation or the presence of distortion products.

A modulation transformer which has partially shorted turns or which is partially shorted to ground may not be easy to locate from external appearances. If the short is to ground, there may be a noticeable arcing or an audible indication. If the short is between turns, however, it will probably result in an unusually low or distorted output. If the short circuit is severe, the output voltage will be too low to provide 100-percent modulation; a less severe short circuit will probably indicate itself by distortion and a mismatched type of presentation on the oscilloscope. Failure of the modulation transformer that is not visible by external symptoms is difficult to determine, and usually can be remedied only by replacement of the transformer with a good one after all other components have been checked and found satisfactory.

Lack of sufficient electron tube emission to develop the extreme peaks of modulation in the r-f amplifier can cause peak clipping, more than usual distortion, and inability to obtain 100 percent modulation. Such a condition is usually progressive and can be observed by noticing that the output indicator (r-f ammeter) fluctuations become less for modulating signals known to produce large indications. (At 100-percent modulation the output indication on an r-f ammeter will increase approximately 22 percent above the normal indication without modulation.)

Distorted Output. Any distortion in the output is usually obvious when the audio modulation is monitored. R may occur from a number of causes. For example, overmodulation will cause carrier shift, severe interference with other stations because of spurious signals, and audio distortion. Changing the modulator load impedance, by adjusting the r-f amplifier loading (r-f output) for a value of plate current which is different from the normal value, will change the modulator load line; depending upon the magnitude of the change, this condition may be easily detected, or a special check may be necessary to determine the amount of distortion. Any change of modulator grid bias will shift the operating point and require a corresponding change in the r-f drive. With low bias (for a given drive voltage) the input will be clipped and distorted, and with high bias a larger input signal (drive) will be required; thus speech amplifier distortion will most likely be increased. If the audio gain control is advanced too far in the speech amplifier, the modulator can be overdnven, regardless of whether it operates class A, AB, or B. This can cause peak distortion in both the modulator and the r-f amplifier. With proper drive and symmetrical modulation, little or no distortion will occur. On the other hand, with improper drive and with large unsymmetrical or sustained peaks of modulation, excessive distortion can result. Use of a modulation indicator to indicate the percentage of modulation is a help in determining whether distortion is caused by overmodulation. Only, a waveform check can positively determine whether distortion is present. An oscilloscope arranged to check waveforms at key points is most helpful in isolating trouble.

Lack of sufficient plate voltage in either the modulator or the r-f amplifier can cause a reduction in plate-voltage swing with a consequent loss of the peaks in the output. In the modulator, this is evidenced by a rounding off of the peaks and an inability to reach 100-percent modulation with a further increase in the audio drive. In the r-f amplifier, it is shown by peak clipping caused by overdrive from the modulator. In either case, distortion components can be heard in a monitor, as well as seen on the oscilloscope.

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Operating at a higher than rated load can also cause core saturation effects in the modulation transformer and thus produce a flattening off of the peaks. Such a condition will return to normal when the load is readjusted for the proper current. Poor frequency response in the transformer can also cause distortion by loss of low or high frequencies, but this is an inherent design problem and will not occur unless the modulation transformer is defective or is replaced with an inferior part. Poor connections or internal dc leakage will most likely be shown by the presence of noise components in the modulation. Use of a harmonic analyzer will usually indicate the source of the distortion.

Iack of sufficient filament (cathode) emission in the r-f amplifier and modulator tubes can cause distortion due to peak clipping and make it possible to obtain 100-percent modulation.

# COLLECTOR-INJECTION MODULATOR

#### Application.

The collector-injection modulator is used to produce modulation at either low or relatively high levels, and up to a maximum of 100 per cent for semiconductor transmitting equipment.

#### Characteristic.

**Is** operable under either small signal or **large** signal conditions.

Uses fixed bias.

Is capable of full 100 per cent modulation.

# **Circuit Analysis.**

**General.** Collector-injection is the semiconductor counterpart of electron tube plate modulation. While plate modulation is usually always at a high level, collector-injection can be at very low levels. In fact, at the present state of the art, linear modulation for high frequency transistors is limited to a maximum change of one tenth of a volt or less which is a very low level of operation. In addition, the transistor ratings must be such that normal dc collector voltage does not exceed one half of the collector breakdown rating, otherwise the peak swing on large signal operation may cause breakdown. When inputs larger **than** the emitter bias are applied, rectification occurs in the base circuit and causes an increase of bias. However, this slight bias shift does not create as much

distortion when collector-injection is used as it would if either base-or-emitter injection were **used**.

**Circuit Operation.** The accompanying illustration is a schematic of a typical collector-injection modulator circuit.



**Collector-Injection Modulator** 

The r-f drive voltage is applied to the base of Q1, through r-f transformer T1, inductively from primary L1 to secondary L2. The base is held at a fixed forward bias by bias voltage divider R1 and R2. Cl is the r-f bypass for R1, preventing feedback of r-f into the bias supply and possible regeneration. Emitter resistor R3 provides thermal compensation and is bypassed by C2 to prevent degeneration. With the emitter at ground potential, only slowly varying d-c current changes caused by a temperature change will bias off the emitter and counteract the tendency of increased current flow with increasing temperature. The audio modulation is inserted in series with the collector of Q1 through audio transformer T3 by connecting secondary L6 between the collector supply and the output tank. The secondary of T3 is also bypassed for r-f by C3 to prevent r-f squeal in the audio circuits caused by feedback. Output transformer T2 has its primary tuned, with L3 and C4 forming the tank, which is inductively coupled to secondary L4 providing a modulated output.

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The freed negative base bias causes heavy forward conduction in Q1, and base current flows from the supply through R2, L2 secondary, and through Q1 emitter-base junction back to ground through emitter swamping resistor R3. Thus the base is held near cutoff for large signal operation (and is Class A biased for small signal operation). With only the r-f drive signal applied, collector current is decreased during the positive half-cycles and increased during the negative half-cycle. This is conventional r-f amplifier operation and provides the normal r-f carrier.

Assume now, that modulation is applied to the input of L5. The signal is transformer coupled into the secondary. Thus during the positive hrdf-cycles of modulation (assuming an in-phase connection) the collector voltage is opposed decreasing the effective collector voltage. On the negative half-cycle the polarity of the modulation adds to the collector voltage, increasing it. Thus the transistor gain is alternately decreased or increased in accordance with the modulation swing. When the gain is increased a peak of modulation occurs, when decreased a trough in the modulation occurs. If the transistor gain varies linearly, 100 percent modulation is achieved when the collector voltage is doubled on the negative half-cycle. Although secondary L6 of T3 is bypassed by C3, the bypassing is effective for rf only and the af signal remains effective in changing the instantaneous collector voltage. The output tank circuit varies in accordance with the modulation and inductively couples the output to L4 secondary of T2. In smrdlsignal, Class A operation the tank circuit determines the output frequency. In large-signal, Class B or C operation, the tank supplies the missing half cycle which is lost during cutoff, and also determines the output frequency. Thus distortion is kept to a minimum for either small- or large-signal operation.

## **Failure Analysis**

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**General. When** making voltage checks use a vacuum tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of conventional voltmeters. Be careful, also, to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No **Output.** A defective transistor, open base, emitter, or collector circuit, or a loss of bias will prevent operation. An open base circuit can be caused

by lack of continuity in the windings of T1. Check L1 and L2 for continuity with an ohmmeter. Likewise, an open bias circuit may be caused by either R1 or R2 open. If R2 is open the operation is certain to cease, but with only R1 open some bias will be produced through R2 and the transistor, so complete output should not be lost. Check the values of R1 and R2 with an ohmmeter. An open circuited emitter, possibly caused by a defective swamping resistor R3, will also stop operation. Check the value of R3 using an ohmmeter. An open circuited collector will also stop operation; this can be caused by an open tank coil L3, a high resistance soldered joint, or by shorting of tank capacitor C4. An open modulation transformer will also prevent collector voltage from appearing if it is in the secondary of T3, as well as a short on C3. Use an ohmmeter to check the winding for continuity and an ohmmeter to check C3 for a short. If all the circuits thus far are found to have continuity and correct value there are still two possibilities. Transistor Q1 may be defective or output winding L4 of T2 may be open. Check L6 and IA for continuity with an ohmmeter. Improper supply polarity will reverse the bias, stop operation, and most likely ruin the transistor. In most cases a continuity check combined with a voltage analysis, using a high impedance voltmeter, will locate any of the no-output troubles.

Low Output. Improper bias can result in a low output with distortion. Check R1 for proper value with an ohmmeter. Low output can also be caused by low collector voltage. First check the unmodulated value to be certain it is normal, and then check the instantaneous value with modulation using an oscilloscope. The modulation should be able to drive the collector from zero to twice normal voltage, less than this will produce less than 100 per cent modulation. Check the waveform with an oscilloscope. Lack of sufficient r-f drive will also produce a low-output condition, since the af merely functions to modulate the carrier. A defective or mistuned tank circuit can also cause a low-output condition, since the maximum output is developed on the same frequency as that of the input (carrier). With no a-f applied and low drive, the carrier amplitude will show on an oscilloscope as being less than normal or less than one-half the maximum possible amplitude at peak modulation. To determine if the tuning is correct adjust the tank for maximum r-f output (minimum current) if there is no sharp dip in current or

pronounced peak output as the tuning capacitor is rotated, check the tuning capacitor for an open or short.

Distortion or Incorrect Output. Distortion will be caused by improper bias or collector voltage, and by excessive input signals. The r-f signal must not exceed the dc bias; otherwise, rectification of the r-f will occur and change the bias, and, as a result, produce a slight modulation shift on peaks. This will not be as pronounced a distortion as if the injection were of base or emitter type, since only a small fraction of the signal is affected in collector modulation. Too great a modulation signal will cause peak clipping and distortion since the negative peaks will enter saturation and be lost. Use of an oscilloscope will permit this type of waveform distortion to be observed and located. It is also possible that excessive modulation peaks can exceed the maximum inverse voltage, and likewise cause peak clipping effects and possibly damage the transistor.

# CONTROL GRID MODULATOR

#### Application.

The control grid modulator is employed as a low-level modulator in applications where it is desired to use a minimum of audio (modulator) power. It is widely used in portable and mobile equipments to reduce size and power consumption, It is also used in extremely high-power, wide-band equipment such as television transmitters, where plate modulation is more difficult and costly to achieve, and grid modulation is considered standard.

# Characteristics.

Varies effective grid bias of transmitter r-f stage to achieve modulation.

Operates as a basic low-level modulator, with mixing process occurring in grid circuit.

Requires very little audio power (on the order of 1 percent of carrier power).

Is more critical in adjustment than platemodulated class C amplifier.

Produces very little distortion up to 75-percent modulation limit, with greatest distortion occurring between levels of 75 and 100 percent.

Has lowest efficiency for unmodulated (carrier) condition, and highest efficiency at 100-percent modulation.

Has greater bandwidth capabilities than plate modulator when **full** 100-percent distortionless modulation is not required.

Usually uses triodes, rdthough tetrodes and beam power tubes may also be employed to provide greater power gain and to utilize their inherently low-grid-toplate capacitance, thus avoiding necessity of neutralization.

## Circuit Analysis.

**General.** Before starting this circuit analysis, the reader should review the discussion on RF Power Amplifiers, in Section 6 of this Handbook, for background on class C amplifiers.

The grid modulator utilizes the variation of grid bias (at the frequency of the modulating signal) to vary the instantaneous plate current and voltage, and thus achieve modulation. The modulating signal is introduced into the grid circuit in series with the **fixed** bias, so that on each half-cycle the modulating signal alternately aids and opposes the bias. Although the modulation actually takes place in the plate circuit, the modulating signal is applied to the grid circuit, where the power is at a relatively low level (as compared with the plate circuit); thus, the modulator power requirement is low. For this reason, the grid modulator is also classified as a low-level modulator.

Under ideal conditions, only a voltage amplifier would be necessary to produce grid bias modulation. However, in actual practice, the grid w-ill draw current at the positive crest of the signal, and extra power is dissipated in the grid circuit. Therefore, grid modulation does require a modulator capable of supplying a few watts of power (on the order of 2 to 5 watts for moderate power applications). This condition also requires that the r-f driver stage be capable of supplying sufficient drive power to prevent peak flattening on the modulation peaks.

Unlike the plate modulator, the sideband power and the carrier power are both developed from the same power source. Since this power supply must furnish all of the power on the peaks of modulation, it is necessary to operate the electron tube so that it produces a carrier power which is only one-fourth of that available from the same tube operating as an ordinary class C amplifier. (The plate modulator operates at approximately two-thirds of the rated class C amplifier output.)

**Circuit Operation.** The schematic of a typical triode modulator is shown in the accompanying

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illustration. The r-f excitation (drive), which is at the same frequency as the output, is coupled capacitively



#### **Triocle Modulator**

through  $C_c$  to the grid of VI, and a freed negative bias is supplied through **RFC1**. The modulating (audio) signal is coupled in series with the bias through TI. Capacitor Cl, a decoupling and bypass capacitor, prevents any rf that leaks through RFC1 from entering the audio circuits or the bias supply. Capacitor Cl has a value high enough to bypass the rf, but not high enough to bypass any of the modulation and cause a loss of high frequencies. Since the r-f output is at the same frequency as the r-f input, capacitor C<sub>a</sub>, together with a portion of tank coil L, provides a neutralizing arrangement to prevent selfoscillations from being produced as a result of feedback from plate to grid through the grid-plate

interelectrode capacitance. To provide a tank comection for neutralizing the modulator and also to provide a low Q, a split-stator capacitor is used to tune tapped coil L. Since the plate end of coil L is 180 degrees out of phase with the neutralizing end, a signal of the proper phase can be fed back to the grid (through C<sub>2</sub>) to prevent self-oscillations. RFC2 and C2 form a conventional series plate-feed decoupling arrangement (shunt plate feed may also be employed, if desired). The r-f drive voltage, the modulation voltage, and the fixed bias are selected so that, on the positive peaks of the modulation signal, the tube operates as a lightly saturated class C amplifier. As shown in the following waveforms, the freed bias is slightly greater than 1.5 times the cutoff voltage for the tube, and the modulation signal (Em) varies the effective bias about  $E_{cc}$ , with the positive peaks of E<sub>m</sub> approximating cutoff. With the effective bias varying in this manner, the r-f drive voltage  $(E_{r})$  is of such an amplitude that: (1) on the positive swing of  $E_m$ , the r-f signal drives the grid positive, grid current flows, and the plate draws current for approximately 120 to 150 degrees of the r-f cycle; (2) on the negative swing of the modulation cycle, the r-f signal drives the grid just barely above cutoff, and plate current flows for just a few degrees of the r-f cycle; (3) with no modulation present, the plate current and voltage are approximately half their maximum values, and the output carrier produced is one-fourth the power of the same tube operating as an ordinary class C amplifier. The most positive swing of the instantaneous grid voltage is  $E_{max}$ , and is equal to  $-E_{cc}$ +  $E_m + E_{r}$ ,  $E_{min}$  is the minimum instantaneous plate voltage, and must never be less than the instantaneous grid voltage, Emax. That is, the grid must never go more positive than the plate. (This is explained fully in Section 6 under Class C Amplifiers.) Since the plate current consists of pulses of current, it may appear that the plate-to-cathode voltage would be in the shape of pulses extending downward from  $E_b$ . However, the other half of the sine wave is supplied by the flywheel effect of the tuned tank circuit, and the output is as shown in the diagram. The pulses of plate current in effect reinforce the oscillations of the tank circuit, and thereby make up for any losses in the tank.



Grid and Plate Waveforms

To accomplish modulation, the varying grid bias drives the plate current from zero to twice normal, and the plate voltage from approximately half the applied dc potential to the full value. This is the same as driving the plate voltage (and current) to two times normal, as in the plate modulator.

Grid bias modulation uses the linear variation of plate tank current with bias voltage variations to produce the modulated envelope, as shown in the following illustration. The **grid** voltage versus plate current transfer curve is essentially linear over the operating portion, but drops off nonlinearly at the begirming and end. The operating bias is selected so that the resting value  $(E_{cc})$  is at the center of the linear portion of the curve.

With no modulation (time t. to  $t_i$ ), the bias is Ecc, the r-f signal drives the grid above cutoff, with the positive peaks just below O volts. Plate current flows for the portion of the r-f cycle that is above cutoff, with an amplitude approximately half that for the modulation peaks. The plate voltage is one-half the applied voltage, and the power output is onefourth the maximum power available. As the modulation signal swings in the positive direction (time t<sub>1</sub>to  $t_{2}$ ), the grid bias is now  $-E_{cc} + E_{m}$ , the r-f signal now drives the grid positive, and grid current begins to flow. Because of the reduced bias, the plate current increases and the instantaneous plate voltage is reduced. At the most positive peak of the modulation signal (time  $t_2$ ),  $i_p$  is maximum and  $e_p$  is minimum,  $E_{min}$  in the diagram (previously shown). At time  $t_2$ the operation is much the same as for an ordinary class C amplifier (with full r-f drive and fixed grid

bias). At time  $t_3$ , the grid bias is once again  $E_{cc}$ . As the modulation cycle continues in the negative direction, the bias becomes  $-E_{cc}-E_{m}$ , this increased bias reduces the plate current to its minimum value, and the plate voltage increases toward the applied voltage. At time t<sub>4</sub>, the negative peak of the modulation cycle, the r-f drive voltage is just able to bring the tube out of cutoff (assuming slightly less than 100 percent modulation), and plate current flows for just a few degrees of the r-f cycle. At this time in is minimum and  $\mathbf{e}_{\mathbf{p}}$  is almost equal to the applied voltage. The power output varies between 4 times the unmodulated carrier on the positive modulation peaks and zero power on the negative troughs, resulting in an average power of 1.5 times the unmodulated carrier. Thus, 100-percent modulation is attained.



Grid Voltage Versus Plate Current Relationships

The dc plate current during the time of no modulation is one-half of that supplied during the peaks of modulation. However, the power output during this time is only one-fourth of that supplied during the peaks of modulation. Thus, the efficiency during unmodulated times is only half of that for 100 **ELECTRONIC CIRCUITS** 

percent modulation. Typical values of efficiency are 33 percent for no modulation, and 66 percent for 100-percent modulation.

The linearity of the output depends on the linearity of the  $i_p - e_g$  characteristic curve. In the preceding discussion it was assumed that the curve was linear from the maximum value of grid bias ( $-E_{cc}$ -Em). However, the curve is actually nonlinear in the region near cutoff (and near saturation); thus, some distortion occurs on the negative peaks of the modulation cycle. Distortion also occurs on the positive peaks of the modulation cycle. This is true because of nonlinearity of the curve at saturation, and for the following reason. When the grid is driven positive, grid current is drawn, which places a load on the modulator, the r-f source, and the bias supply. This load is not present during the remainder of the modulation cycle. Because of this varying load, good regulation is required for these circuits. Distortionfree operation may be realized by decreasing the modulation voltage. However, this decreases the percentage of modulation, the power output, and the efficiency of the circuit.

To improve the regulation of the modulator circuit, the primary of the modulation transformer is usually shunted with a load resistor equal to the rated dc modulator load, and the audio output stage is usually designed to have a power output of two to three times the output actually required. In addition, some form of inverse feedback is used. in the audio output stage to keep load variations and distortion to a minimum.

Various combinations of bias supplies are used. Good regulation is achieved by providing a bias supply capable of supplying two or three times the required load. Since the dc (average) power to the plate is constant throughout the modulation cycle, a convenient means of obtaining bias is the use of a cathode resistor. The cathode resistor must be bypassed for the modulating frequencies as well as for the r-f frequencies.

Good regulation in the r-f driver stage is usually accomplished by designing the driver stage to be able to supply more power than is actually required.

The total result is that, because of these interacting requirements, the full theoretical advantages of grid bias modulation are not obtained practically, and the basic distortion is always greater than that obtained with plate modulation. Although extra r-f and audio drive power is needed **to minimize** distortion, the small amount of modulator power needed for full modulation makes it economical to use grid modulation where the increased distortion can be tolerated.

# Failure Analysis.

**No Output.** Lack of output should **first** be isolated to failure of the r-f amplifier stage or the modulating signal circuit(s). Even though the modulator is operative, an open rfc or tank circuit, a shorted or defective electron tube, or a lack of grid excitation to the r-f amplifier will produce a **no-carrier** condition. Check the r-f plate current meter for an indication to determine whether the plate circuit has continuity, and check the griddrive meter for an indication to determine whether grid excitation is present. With both indications normal, and with the tank tumble for a minimum dip of plate current, a lack of coupling or continuity in the output circuit of the r-f amplifier is indicated.

Lack of grid drive places the trouble in the exciter stages of the transmitter or the input circuit to the r-f output stage, whereas lack of plate current indicates possible power supply trouble or an open circuit in the r-f stage.

With an r-f carrier existing, the trouble is **definitely** in the audio circuits or modulation transformer. An open transformer secondary would remove the grid bias to the r-f stage and cause excessive plate current; a shorted transformer would allow the r-f stage to operate normally and produce a carrier, but no modulation could occur.

High transmitter plate current usually indicates short-circuited components or lack of bias; low plate current indicates excessive bias, high-resistance joints, low tube emission, or a possible lack of coupling to the load. With open-circuited or **short-circuited** conditions indicated on the equipment meters, a simple resistance analysis made with the power OFF, and with the high-voltage supply grounded for safety, will reveal the defective components.

Low Output. It must first be determined whether the low output is from lack of sufficient audio drive or from an actual reduction in percentage of modulation. Although low modulation is usually due to lack of sufficient audio drive, it can also be caused by a reduced setting of the audio gain control, by trouble in the speech stages, or by lack of sufficient r-f drive. An oscilloscope is very useful in determining the

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cause of malfunctioning, since the waveform may be directly observed. For simple, quick tests of modulation percentage a trapezoidal pattern is helpfuL'A waveform check, however, can show both percentage of modulation and waveform distortion, and is more useful. Too **high** a grid bias will cause a reduction of output and an inability to reach 100-percent modulation with the same drive.

Loading too heavily will increase the r-f carrier output, but it will also result in inability to obtain 100-percent modulation; on the other hand, loading too lightly will produce a reduced carrier, overmodulation on the peaks, and a greater amount of distortion as indicated by a flickering plate meter reading. In the plate modulator, a flickering plate meter reading always indicates distortion and carrier shift, but this is not always true of the grid modulator. Because of the use of a changing efficiency to obtain the modulation, and since the power is obtained from the same source, distortion and lack of full modulation (and even overmodulation) can exist sometimes without greatly disturbing the normal meter indications. Therefore, it is important that the grid modulator be adjusted for. proper results, using an oscilloscope.

A partially shorted modulation transformer will not indicate its condition externally by arcing or burnt. spots since it operates at a very low level; instead, it w-ill probably cause a loss of output combined with distorted modulation. Such a condition can be determined by substitution of a new transformer known to be good after the other parts have been eliminated by a systematic analysis.

Lack of sufficient **filament** emission in the r-f amplifier or modulator tube will produce peak clipping and a lower output because of inability to obtain 100-percent undistorted modulation at the peaks.

**Distorted Output.** Distortion is usually obvious when the audio modulation is monitored. It can result from a number of causes. For example, overmodulation will cause carrier shift, severe interference with other stations, and distortion. Since the grid modulator is inherently subject to more distortion than the plate modulator, any slight change in load conditions or misadjustment will usually be indicated by an increase in distortion.

Since the grid modulator essentially supplies voltage, it is necessary for the primary of the modulation transformer to be damped with a stabilizing resistor in order to maintain a substantially constant load. With a varying load caused by an open stabilizing resistor, the distortion will be excessive. In those stages that must be neutralized, it is important that the neutralization be correct; otherwise, during the peaks of modulation, self-oscillations either will occur continuously or will start to occur on the voice peaks. In either case, the distortion produced by poor neutralization is excessive and noticeable. This condition is easily identified on the oscilloscope by a fuzzy and blurred pattern, which is indicative of oscillation (See the Basic Measurements section of NAVSHIPS 0967-000-0130, Test Methods and Practices, for typical modulation tests and waveforms.)

Distortion in the preamplifier stages can easily be detected by supplying an undistorted signal to the input and checking the output waveform of the modulator transformer with an oscilloscope. If low power and low voltages are involved, a quick but less accurate check can be made by using a speaker or set of headphones instead of an oscilloscope.

# **BASE-INJECTION MODULATOR**

# Application.

The base-injection modulator is used to produce low-level modulation in equipment operating at very low power levels. It is particularly well suited for small portable transmitters, such as walkie-talkies, and for test equipment.

#### Characteristics.

Operates by varying the base bias at the modulating frequency.

Is restricted to low-level, small-signal operation.

Uses common emitter configuration.

Modulating signal amplitude is limited to less than that of the base bias voltage.

# Circuit Analysis.

**General.** The base-injection semiconductor modulator is analogous to the control-grid modulator in electron-tube circuits. The operating conditions, however, are entirely different. For example, **since** the semiconductor operates as a true low-level device under small-signal conditions, the voltage required to produce the modulation is also very small. This means that very little modulator power is required, much

less than for comparable vacuum-tube operation. Likewise, since the transistor is operating under small-signal conditions, the r-f input (drive) is also small. Under these conditions, operation is usually class A or class AB. If operation is extended into the class B or C regions, it becomes large-signal operation. When operated large-signal fashion, the rectified r-f drive signal determines the operating bias and considerable distortion is produced by the non-linear transistor response characteristic for large signals. Because of these conditions such operation is seldom used, except for special applications; therefore, it will not be further discussed in this technical manual.

Base injection can be accomplished by a number of different methods. For example, it may be accomplished by feeding the signal either in series with the **base-emitter** circuit or in parallel with it, and can be accomplished by capacitive coupling or through means of transformers. Each of these methods will be considered in the following discussion.

**Circuit Operation.** Amplitude modulation by base injection (or emitter injection) depends upon a widely separated r-f frequency and modulation (audio) frequency. There are two basic circuits involved, namely, the r-f amplifier circuit and the gain control (bias) circuit. A simplified schematic of the basic r-f amplifier is shown in the accompanying figure. For simplicity, the r-f amplifier circuit is shown without bias supplies, and with a resistive load in place of the tank circuit. It is assumed that normal forward bias is applied to the base+ mitter junction, and that a reverse bias is applied to the collector junction. The secondary of T1 is effectively connected across the base-emitter junction, and the load is connected between emitter and collector as shown. With normal class **A** bias applied, the r-f signal will vary the base voltage equally above and below the operating point (assuming a sine-wave **signal)**, and a corresponding base current will flow. A similar but larger (amplified) collector current will flow through the load resistor, developing an oppositely polarized output voltage. This is the action of a conventional r-f amplifier circuit.



Simplified R-F Amplifier Circuit

Consider now the method by which modulation is accomplished in the bias circuit, using the accompanying simplified schematic. For simplicity this circuit is also shown without bias supplies and with a load resistor in place of the tank circuit. It is assumed that normal forward bias is supplied to the baseemitter junction, and that a reverse bias is applied to the collector junction. The modulation is injected across R1, which is also the bias resistor, having a freed dc forward bias placed across it. Since the modulation signal is effectively connected in series with the base-emitter circuit, it adds to the bias when of the same polarity. When these voltages are of opposite polarity they cancel and reduce the total effective bias. Thus' tie bias on the transistor is made to vary instantaneously above and below the fixed dc bias level in accordance with the modulation signal.

# MODULATORS



Simplified Modulator Circuit

Assuming a sinusoidal modulating signal, it is evident that the instantaneous bias will also vary sinusoidally. Since a change in bias will produce a change in gain, the instantaneous gain will also vary similarly. Consequently, the instantaneous amplification of the r-f carrier signal will vary in accordance with the modulation, but in an opposite direction. (The **common-emitter** output polarity is opposite the input polarity.) For maximum modulation the a-f signal must be slightly greater than the r-f carrier input signal. To prevent distortion produced by driving the transistor to cutoff or into saturation, the modulation signal amplitude must never exceed the dc bias value.

A simplified schematic of the series-feed method of base injection is shown in the following figure. For simplicity, the inputs are shown as r-f and a-f generators, and biasing voltages are not shown. As can be seen, the r-f driver signal is connected in series with the a-f modulating signal between base and ground. The dc bias (not shown) is such as to bias the transistor for class A operation. The bias value is chosen so that the quiescent collector current is set for half the maximum value. When the r-f input is applied, it adds to the base bias on the negative excursions and reduces the base bias on the positive excursions. The collector current follows these sinusoidal variations of bias, producing a voltage drop

across the tuned tank (LC) in series with the collector. The tank is tuned to the driver frequency and is inductively coupled to the next r-f amplifier (or output circuit). Because of the gain through the transistor, the r-f drive signal is amplified. When the a-f modulating signal is applied, it alternately adds to and subtracts from the r-f drive signal applied to the base circuit (both r-f and a-f generators are series comected). The result of combining the r-f signal with the audio modulation signal has the total effect of increasing and decreasing the bias in accordance with the modulation signal amplitude. The changing bias varies the transistor gain in accordance with the modulation signal, and an amplified and modulated r-f output signal is obtained. This signal appears in the output as an r-f carrier with an envelope which is a replica of the original modulation signal.



Series Injection

While either capacitance coupling or transformer coupling may be used to inject the modulation signal, there is essentially no difference between them in the manner in which this base injection circuit operates. In the capacitance-coupling method the modulator is isolated by the capacitor (Cl) from the d-c biasing circuit as shown in the following figure, and the modulation is applied across the base bias resistor (Rl) which also acts as the modulator load. RI is bypassed for r-f by C2. With transformer coupling either internal (contact) or emitter bias, or a combination of both are used. Whereas with capacitive
MODULATORS



#### **Coupling Methods**

coupling fixed (voltage divider) bias is usually used. In either case C2 bypasses the r-f around the audio, completing the emitter-base circuit for r-f. The two methods of coupling are illustrated in the preceding figure. Although not very prevalent, the parallel (shunt)-feed method of base injection may also be used; it is shown in simplified form in the following illustration. Blocking capacitor Cl is used to prevent r-f transformer T1 secondary from shorting the base bias and modulation signal to ground, through its very low secondary resistance. Likewise, the RFC is used to prevent the low-impedance secondary of modulation transformer T2 from shunting the r-f carrier signal to ground. Emitter bias and swamping are employed, using R<sub>E</sub> and C<sub>E</sub>. The collector circuit is identical with the series injection circuit; it contains the tank and output coupling circuit.

In the parallel-feed circuit, the bias is also caused to vary at the modulation rate. The difference is that since the two inputs are in parallel with each other, more modulation signal is required for full modulation. At low percentages of modulation (very small modulator inputs), a larger signal is also required in the parallel-feed circuit to produce the same effect as in the series-feed circuit. The addition of the r-f choke also presents an additional problem, that is, avoiding unwanted resonances in equipment operating over a large range of frequencies. Therefore,

shunt injection is not very popular with designers. The circuit of a typical capacitance-coupled seriesfeed base-injection modulator is shown in the following illustration. The r-f input is applied to the base of Q1 through r-f transformer Tl, which is shown untuned for simplicity. Assuming normal bias and operation as a conventional class A amplifier, the r-f drive signal is amplified by Q1, and appears as a larger-amplitude r-f output in r-f transformer T2.

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Transformer T2 has a tuned primary with L and C acting as the conventional tank circuit across which the output signal is developed. The secondary of T2 is connected to the next amplifier stage or to a load (an antenna in special cases). Conventional emitter swamping is employed, with resistor R3 serving as the swamping resistor, bypassed by capacitor C3. Capacitor C3 is large enough to offer a low reactance to the lowest modulation frequency employed. Thus, both rf and af are bypassed around R3, so that no degeneration is produced. Only very slowly varying temperature changes produce a voltage change across R3. (See the discussion of Bias Stabilization in the Introduction to the Amplifier Section of this Handbook for an explanation of the function of R3 and C3.)



**Base-Injection Modulator** 

Consider now the bias circuit consisting of RI and R2. This is **fixed** bias with the resistors forming a voltage divider across the supply. (See the explanation of Bias Circuits in the Introduction to the Amplifier Section of this Handbook.) The voltage appearing across RI is the effective bias applied to the base of Q1 through the secondary of r-f transformer T1. Thus, the r-f input is applied in series with the dc bias provided by RI. However, capacitor C2 bypasses RI to ground for rf and, together with C3, effectively comects the secondary of TI from base to emitter. As the r-f signal vanes between positive and negative

alternations, the emitter current varies similarly but oppositely (decreases on positive part of cycle and increases on negative part of cycle). The pulses of emitter current applied across the tank load (LC) produce an amplified sine wave of rf at the same frequency as the input.

Consider now the effect of the modulating signal. Since the modulating signal is coupled through capacitor Cl, it appears as a varying a-f voltage across R1. While C2 bypasses R1 for rf, it is not large enough to bypass the a-f modulation. Therefore, since the a-f voltage is applied across R1, between the bottom of the T1 secondary and ground, it is also effectively in series with the d-c bias voltage, and the bias is caused to vary at the modulation rate. As the bias changes under control of the modulating signal, the gain of the transistor is varied likewise. Since the transistor is not exactly linear in its base-collector relationship, the carrier envelope will not be a linear replica of the modulation. It will be similar in shape, with the peaks and troughs occurring at the same time, but somewhat distorted. A typical forwardtransfer characteristic curve for the common-emitter circuit is shown in the following figure. Because of the rounding off at the higher currents, the effective limits of modulation are for values between zero and about 92-percent modulation. Above this range the distortion tends to become excessive. Therefore, applications requiring full 100-percent modulation generally employ the collector-injection circuit, which will be discussed later in this section.



**Typical Forward-Transfer Characteristic** 

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While a resistive collector load has been assumed for ease of explanation in the simplified circuit discussions, in practice a tuned (L-C) tank circuit is necessary to select the proper output frequency. In every modulator there are sum and difference frequencies, and spurious frequencies are generated by the nonlinearity of the modulator (even in socalled linear modulators). Therefore, it is necessary to select the desired output frequency. In this case it is the frequency of the r-f carrier plus the sidebands generated in the modulation process.

#### Failure Analysis.

No Output. A defective transistor or open base circuit caused by a defective transformer or an open bias resistor, will prevent operation. Also, an open bias capacitor can produce cutoff bias through degeneration if the r-f drive and the resistance in the circuit are sufficient to block operation. Either of these conditions can be detected by means of a resistance or continuity check with an ohmmeter. An open-circuited emitter, possibly caused by a defective swamping resistor, (RE) will stop operation. An open-circuited collector will also stop operation; this condition can result from an open tank coil or a defective soldered joint, causing an extremely high resistance. Checking the collector voltage to ground will determine whether this circuit is open. Improper supply polarity will reverse the bias, stop operation, and most likely ruin the transistor. In most cases a simple resistance and continuity check combined with a voltage analysis, using a high-impedance voltohmmeter, will locate any of the no-output troubles.

Low Output. Too low or too high a bias will cause clipping of the output signal, resulting in low output and distortion. For maximum modulation, the a-f signal must be slightly greater than the r-f carrier input signal. Therefore, lack of audio gain, a defective coupling capacitor (Cl), or shorting of the a-f signal to ground through a shorted bypass capacitor (C2) can cause loss of or low audio, and produce a lowoutput indication. The use of an oscilloscope to check the waveform will indicate the point in the circuit where the waveform amplitude changes or is lost. Lack of sufficient r-f drive will also produce a low-output condition since the a-f functions merely to modulate the r-f carrier. A defective or mistuned tank circuit can cause a low-output condition since the maximum output is developed at the same frequency as that of the input (carrier).

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Where the modulation is present but r-f drive is lacking, no output will appear with normal a-f drive, since the collector load impedance (tank circuit) is too low to develop any audio voltage across it as it is tuned to the r-f signal.

Distorted or Incorrect Output. Distortion will be caused by improper bias and collector voltage, or by excessive input signals. Collector voltage and bias can be checked with a high resistance voltmeter. The r-f signal must not exceed the d-c bias; otherwise, rectification of the rf will occur and change the bias, and, as a result, clipping will occur on the peaks of modulation. If the a-f modulation is not of sufficient amplitude, the peaks of modulation will also be lost and distortion will occur. In a similar manner, too great an a-f drive will send the collector current into the saturation region, the troughs (negative peaks) will be cut off, and distortion will result. The use of an oscilloscope will permit waveform distortion to be observed and located. In the case of failure of the a-f modulation, an unmodulated r-f output will be obtained. Under special circumstances with high a-f drive and no r-f drive, it is possible that the audio waveform may be observed on an oscilloscope (because of capacitive leakage across the transistor); however, this is a rather remote possibility. In any event, the proper method of determining whether distortion exists and of locating the origin of distortion are to use an oscilloscope to observe the waveform, to make a resistance and voltage analysis to check the components, and to determine that the values of the element voltages are correct for normal operation.

If the tank circuit is too sharp (that is, has too high a Q), sideband clipping will result and the higher modulation frequencies will be lost. However, this is only of academic interest since such a condition could result only from an unauthorized modification of Navy equipment.

# CATHODE MODULATOR

#### Application.

The cathode modulator is generally employed for low-level operation where the audio power is limited and the inherent distortion of the grid-modulated circuit cannot be tolerated.

#### Characteristics.

Varies the cathode voltage to achieve modulation. Operates as a combination plate and grid modula-

tor, and can be designed to function either way. Requires an audio output of 5 to 50 percent of the r-f plate input, depending on design.

Requires only half the normal r-f drive for class C conditions.

Provides a higher efficiency than the gridmodulated types and lower efficiency than the platemodulated types, depending on the design. (For the 50 percent grid and 50 percent plate modulation condition, the efficiency is 62 percent.)

Provides better linearity than the grid-modulated types, and can be made equal to the plate-modulated type of circuit.

Can be used equally well with triodes, tetrodes, or pentodes.

#### Circuit Analysis.

General. The cathode modulator vanes the voltage of the cathode to produce the modulation envelope. Since the cathode is in series with the grid and plate circuits (and the screen circuit for tetrodes), it can be seen that changing the cathode voltage will effectively change the voltage of the other tube elements. By proper proportioning of the voltages, the injected cathode voltage can be caused to operate the tube in a form of grid modulation with relatively low efficiency, or to operate it in a form of plate modulation with high efficiency. Usually, the cathode modulator is made to perform about midway between these two classes, utilizing the advantages of each type, Thus, generalizing, it can be said that the cathode modulator normally operates at efficiencies on the order of 55 to 62 percent, and requires modulator (audio) power of about 20 to 25 percent of the rated carrier power.

As a result, more linear operation is achieved than in other types of grid modulators, with only a slight audio power increase being required to obtain it. As in all forms of AM modulation, the plate voltage and plate current vary from zero to twice normal with a peak power of four times normal at 100 percent mod-

ulation. Whereas the grid modulators vary the grid bias to produce a varying efficiency which develops the required power increase from the regular transmitter supply, and operate at half the tube capability with carrier alone, the cathode modulator operates somewhat like the plate modulator. That is, the additional power required for modulation comes mainly from the audio modulator, with the transmitter stage supplying the remaining power by a variation of efficiency. Since the cathode modulator is basically a half grid and half plate modulator, it forms a unique type of circuit. When operated mainly as a grid modulator it offers little if any advantage over other types of grid modulation, and when operated mainly as a plate modulator it offers practically no advantage over straight plate modulation for a triode; however, with a pentode or tetrode it helps achieve 100 percent modulation. When operated between the two levels it does provide a more linear output with moderate efficiency and a modest audio power requirement.

The r-f excitation requirements for the cathodemodulated amplifier are midway between those for plate modulation and for control-grid modulation. More excitation is required as the percentage of plate modulation is increased. Grid bias is always considerably beyond cutoff. Fixed bias from a supply having good voltage regulation is preferable, especially when the percentage of plate modulation is small and the amplifier is operated more nearly like a grid-biasmodulated stage. At the higher percentages of plate modulation, a combination of fixed bias and grid-leak bias can be used, since the variation in rectified grid current is smaller. The grid leak must be bypassed for audio frequencies. The cathode circuit of the modulated stage must be independent of other stages in the transmitter. When directly heated tubes are used, their filaments must be supplied from a separate transformer. The filament bypass capacitors should not be larger than about  $0.002\mu f$  to avoid bypassing the audio modulation.

The cathode modulator performs differently for each ratio of grid-to-plate modulation selected. The accompanying graph illustrates the manner in which



#### Input Power Variation

the input power requirement varies. As can be seen, with grid modulation alone the input power is about 48 percent of the normal plate power for plate modulation. At the halfway point, where equal amounts of grid and plate modulation are employed, the input power is just slightly more than 70 percent of the power for a similar plate modulator. This represents an efficiency of approximately 62 percent, as **shown** in the following graph which illustrates how the efficiency varies.



#### **Efficiency Variation**

Note that neither of the above graphs varies linearly, but that the **following** graph, showing the audio

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power requirements, does vary linearly. At the 50-percent plate modulation point, it requires only about 25 percent audio power from the modulator, as compared with 50 percent for full plate modulation. Thus, it can be seen that while higher efficiency is obtained from the cathode modulator, one must pay for this directly in terms of audio power supplied by the modulator.



Audio Powar Variation

Since the cathode modulator uses only a 15 percent change of efficiency as compared with a 50 percent change for the grid modulator, it is evident that the power supply regulation and current hanclling capacity need not be as stringent or as large as is required for grid modulation. Likewise, a reduction of distortion due to lack of these effects is realized. By similar reasoning it can be understood that since the plate modulator is rdways more linear than the grid modulator, and a 5050 ratio of gridplate modulation is employed, a 50-percent reduction in distortion is immediately realized with cathode modulators.

When tubes with indirectly heated cathodes are used, the heater-cathode breakdown voltage limita the maximum instantaneous voltage which may be applied during modulation. in this case the power employed is low and less plate modulation with more grid modulation is used. For high-powered equipment and large voltage swings, tubes with directly heated cathodes (filaments) are used.

Circuit Operation. The basic cathode modulator in the accompanying illustration is shown using sinewave generators for audio and r-f power for simplicity. In the illustration the complete biasing and neutralizing arrangements have also been omitted for ease of presentation. As shown, a freed negative bias of more than cutoff is always employed, and the r-f drive is such that the stage operates as a lightly saturated class C amplifier. (If fully saturated, it would require large grid voltage swings to obtain the desired amount of grid modulation.) The plate circuit employs a conventional LC tank circuit inductively coupled to the load. The output of the audio modulator is transformer-coupled to the cathode circuit, and is represented by the audio generator. As the modulation occurs, assuming a sine wave polarized by transformer connections so that on the positive peak the cathode voltage is positive, the effective gridcathode bias is increased, thus reducing the plate current flow. At the same time this cathode polarity opposes the plate voltage so that the plate-cathode voltage is also effectively reduced by a like amount. As the modulation is reduced to zero and goes negative, the opposite effect occurs. The cathode bias is now reduced and plate current is increased, while simultaneously the polarity of the cathode voltage. is such as to add to the plate voltage. Thus, both the instantaneous plate current and plate voltage are increased. At the 100 percent modulation level, the instantaneous (peak) plate voltage is just twice normal, and so is the peak plate current, representing a **peak** power of four times normal and a maximum efficiency of 77 percent, which is equivalent to plate modulation alone. At zero modulation (carrier condition), with the circuit operating halfway between grid and plate modulation conditions, the efficiency is about 62 percent. This represents almost the maximum efficiency obtainable from grid modulation at the peak of the modulation; thus, it can be seen that cathode modulation does provide fuller use of a given transmitting tube's capabilities.



**Basic Cathode Modulator** 

The modulating impedance of a cathodemodulated amplifier is approximately equal to: m x  $E_b/I_b$  (where m is the percentage of plate modulation expressed as a decimal, and  $E_{b}$  and  $I_{b}$  are the plate voltage and current of the modulated amplifier, respectively). This modulating impedance is the load into which the modulator must work, just as in the case of pure plate modulation, and is matched by proper choice of the transformer turns ratio. The schematic of a typical cathode modulator is shown in the following figure. A triode using a directly heated (or filament-type) cathode is shown in the illustration; this circuit is sometimes known as a center-tapped modulator because the modulation voltage is injected into the filament center tap. Otherwise, the circuit is that of a conventional r-f amplifier, being biased to beyond cutoff by the fixed negative supply and by the bias developed across  $\mathbf{R}_{\mathbf{g}}$  from the drive current. RFC1 prevents the r-f drive from being shunted to ground, and Cl provides the conventional

bypass around the bias supply for any r-f that might leak through the r-f choke. The percentage of grid modulation may be regulated by choice of a suitable tap on the modulation transformer, as shown in the illustration (or by changing the dc value of the grid bias). Capacitors  $\mathbf{C}_{\mathbf{f}}$  form the conventional center-tap arrangement of directly heated (filamentary) cathodes to provide an electrical center tap which prevents hum modulation due to unequal voltages across the sides of the filament. The plate tank uses a splitstator capacitor to tune a center-tapped coil, which provides out-of-phase voltages at the ends of the coil, Thus, a neutralizing voltage which is 180 degrees out of phase with the normal plate-to-grid feedback within the tube is provided through neutralizing capacitor  $\mathbf{C}_{\mathbf{n}}$  (since both input and output voltages are of the same frequency), preventing self-oscillation with the distortion which accompanies it. The antenna is inductively coupled to the tank, and the tank is series-plate-fed through RFC2 bypassed by C2. The modulation is applied through the secondary of T1 to the filament center tap of V1. It is evident, then, that as the modulation signal is applied to V2, considering a sine-wave input, the voltage at the secondary of T1 vanes first to a positive maximum and then to a negative maximum, returning to zero as the signal ceases. With the circuit biased so that tube VI is not driven to saturation, but just to the point where saturation will begin if driven further, only half of the normal r-f grid drive is needed, as compared with full plate modulation.



Cathode Modulator

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Consider now one cycle of operation. As the modulating signal increases in the positive direction, an increasing positive voltage is applied in series with the cathode. This cathode voltage is instantaneously added to the freed bias and to the bias produced by r-f grid drive (through grid resistor  $\mathbf{R}_{\mathbf{g}}$ ). The result is to increase the total effective grid bias by the amount of the modulating signal. Consequently, the instantaneous plate current,  $i_p$ , is reduced. At the same time, this cathode voltage is in opposition to the applied plate voltage, and reduces it accordingly. With a lower effective plate voltage, the plate current is still further reduced. This action continues sinusoidally until the modulation peak is reached, which corresponds to the point of almost zero plate current (if the plate current were entirely cut off, the output signal would be interrupted). At this time the plate current through the load impedance is at a minimum, and the output voltage is also at a minimum, as shown in the following illustration,

As the modulating signal turns in a negative direction the total effective bias is decreased, and the cathode voltage adds to the effective plate voltage. Consequently, the instantaneous plate current increases. At the completion of the positive half-cycle of modulation signal, the cathode bias (modulating signal) is zero, and the effective bias is the sum of the freed negative bias and the bias produced by the r-f drive. This is the quiescent, or resting, condition of the circuit where normal plate current is drawn and only the carrier is produced. While this plate current is about 20 percent higher than it would be in the grid modulator, and represents about 70 percent of the plate modulation rating of the tube, it is the normal value which is doubled at the modulation peak. Therefore, additional power is required when the modulation drives it above the carrier level. The increase of carrier power above that of the grid modulator is obtained from the transmitter power supply by a change in plate efficiency.



**Oparating Polarities and Wavaforms** 

As the modulation cycle progresses sinusoidally below zero toward the negative peak, the cathode bias is further reduced by the negative-going cathode voltage. Since the cathode voltage is now in a direction to add to the effective plate supply, the instantaneous plate voltage is increased. With a reduced bias and an increased plate voltage, the plate current is increased. At the peak of the cycle the instantaneous plate current is twice the normal (carrier) value. At this time the drop across the load is the greatest, and the actual plate voltage reaches its minimum value, near zero. The minimum value of plate voltage (for triodes) is kept above the maximum positive grid swing at this point to prevent excessive grid dissipation. **(If** it were zero, the grid would act as the plate

during this interval.) Once the negative modulation peak is reached, the modulation signal again goes in a positive direction toward the zero or carrier level. The cathode voltage is now going in the opposite direction (increasing positive), and once again opposes the plate voltage, increases the total effective grid bias, and reduces the plate current. Thus we can say that the modulation signal effectively drives the tube to twice the norrnrd plate voltage and current on the peaks of modulation, and to almost zero on the troughs of modulation (the negative peaks).

#### Failure Analysis.

No Output. Lack of output should first be isolated to failure of the r-f amplifier stage or the modulator and speech circuits. Even though the modulator is operative, an open rfc or tank circuit, a shorted or gassy electron tube, or lack of grid excitation to the r-f amplifier will produce a no-carrier indication. An open modulator primary will permit a earner to appear, but no modulation will occur, while an open secondary will produce neither a carrier nor any modulation. "Observation of the amplifier r-f plate current meter will determine whether the circuit has continuity, while tuning for a maximum indication with a resonant dip will determine whether sufficient drive and load and the proper bias are present for operation without modulation. Grid-drive-meter indications will also show whether there is proper r-f drive. When the tank can be resonated for a minimum dip and then loaded to maximum plate current with a normal grid-current indication, the trouble is in the modulator or speech circuits.

Lack of grid drive places the trouble in the exciter stages of the transmitter or in the coupling network to the final stage. Lack of plate current indicates possible power-supply trouble, an open-circuited r-f stage, or a defective modulation transformer; if screen grid tubes are used, lack of plate current can also be due to an open screen-voltage dropping resistor or a short-circuited screen bypass capacitor.

High transmitter plate current usually indicates short-circuited components, a lack of bias, or improper tuning; low transmitter plate current indicates excessive bias, high-resistance joints, low tube emission, lack of sufficient r-f drive, a possible lack of sufficient coupling to the load, or possible antenna or transmission -line trouble. A simple resistance analysis made with the power off and the high-voltage supply grounded for safety usually will quickly determine the defective components, using the meter indications as a guide to the most probable location of the trouble.

Low Output. Determine first whether the low output is due to lack of sufficient audio drive or to an actual reduction in the percentage of modulation. Low modulation is usually caused by lack of sufficient audio output, and may be the result of a reduced setting of the audio gain control or from trouble in the speech amplifier stages. An oscilloscope should be used to view the waveform to determine whether 100 percent modulation is being obtained. For quick, simple tests of modulation percentage, the trapezoidal waveform check is useful. The envelope or waveform check, however, will show the percentage of modulation and also waveform distortion at the same time, so that it is usually more useful. Too high a grid bias will cause a reduction of output and an inability to obtain 100 percent modulation with the same r-f drive. The grid bias can be easily checked with a voltmeter (use an rfc in series with the test prod). A reduced' screen voltage is most likely of all to produce a low output, usually with overmodulation or distortion, since the plate and screen swings will be excessive. Such a condition may be caused by too heavy a screen current, causing a large drop in the screen-voltage dropping resistor, by a defective screen voltage dropping resistor, or by a partially shorted screen bypass capacitor. Where a separate screen supply is used, the latter trouble is the most likely.

Lack of proper tuning can also cause a low output. Too light a loading or too high an excitation will cause a flattening of the upward peaks of modulation, as in grid modulation. The antema loading must be such that a further increase in loading causes a slight drop in antema current. For optimum performance, the grid excitation should also be adjusted for minimum plate dissipation with maximum power in the antenna. The cathode current will be practically constant with or without modulation when the proper operating conditions have been established.

Improper load matching by the modulation transformer will produce a lack of sufficient audio power, as well as distortion. Where taps are provided, the proper tap may be selected. Where no taps are provided and the load appears to be mismatched when checked with an oscilloscope, the tube or the transformer may be defective. Lack of sufficient **filament** emission in the final amplifier tube can cause

**peak flattening**, inability to obtain 100 percent modulation, and distortion.

**Distortad Output.** Distortion can occur from a number of causes, and is easy to detect when monitoring the audio modulation. Overmodulation will cause a chopping off of the carrier (carrier shift), producing severe interference to stations operating near the transmitter frequency, as well as distortion.

In stages operating on the same input and output frequencies, there is always the possibility of **suffi**cient internal plate-to-grid feedback to cause selfoscillations accompanied by severe distortion, particularly on the peaks of modulation. When this occurs with triodes, it indicates the necessity for readjustment and a check of the neutralization. With pentodes and tetrodes it can occur at the high frequencies, particularly if the lead dress is changed after a repair. Self-oscillation can usually be recognized on an oscilloscope by the characteristic fuzzy appearance of the display. Plate current meter indications will usually be excessive and erratic when this condition is present.

Lack of sufficient capacitance to supply the peak power requirements can occur through loss of falter capacitance, and can cause peak flattening with consequent distortion. Usually, however, such a condition will be indicated by a hum on the carrier, or in the modulation, before the distortion is excessive enough to notice unless an oscilloscope is used to monitor the transmissions.

A similar condition caused by lack of sufficient **filament** emission in the r-f amplifier stage will also cause peak flattening and resulting distortion. Sometimes this condition can be observed by noting the inability of the r-f output meter to respond to heavy modulation peaks, accompanied by a gradual reduction in plate current readings over a long period of time. Under normal conditions, the r-f ammeter will indicate approximately a 22 percent increase in output current at 100 percent modulation.

Improper bias and drive conditions will also cause distortion, and usually are accompanied by a reduction in output or an inability to attain 100 percent modulation.

# EMITTER-INJECTION MODULATOR

# Application.

Same application as Base-Injection Modulator.

# Characteristics.

Same characteristics as Base-Injection Modulator except it is operated by varying the emitter bias instead of the base bias.

### **Circuit Analysis.**

General. Emitter injection is very similar to base injection, since both methods vary the emitter-base bias. The carrier signal input is coupled to the base region of the transistor, while the modulating signal is applied across the emitter swamping resistor to regulate the gain of the transistor in accordance with the modulation. Consequently very little modulator power is required. Much iess than that required for electron tube cathode modulation which is the electron tube counterpart of this circuit. Since the transistor is operating under small-signal conditions, the r-f earner input (drive) is also small. Under these conditions the transistor is operated either Class A or Class AB. Injection of the modulation in the emitter circuit may be made by either the shunt or series method. In the series method a transformer is used in series with the emitter. Either method, however, operates similarly.

**Circuit Operation.** Amplitude modulation by emitter injection depends upon a widely separated r-f frequency and modulation (audio) frequency. There are two basic circuits involved, namely, the r-f amplifier and the modulating (bias gain control) circuit. A simplified schematic of the basic r-f amplifier is shown in the accompanying figure. For simplicity, the r-f circuit is shown without bias supplies and a resistive load in place of the tank circuit. It is assumed that normal forward bias is applied the emitter-base junction, and that a reverse bias is applied the collector junction. The secondary of T1 is effectively connected across the emitter-base junction, and the load is comected between emitter and collector as shown.



Simplified R F Amplifier Circuit

Simplified Modulator Circuit

With normal Class A bias applied, the r-f signal will vary the base voltage equally above and below the operating point (assuming a sine-wave signal), and a corresponding base current will flow. A similar but larger **(amplified)** collector current will flow through the load resistor, developing an oppositely polarized output voltage. This is the action of a conventional r-f amplifier.

Consider now the method by which modulation is accomplished in the bias circuit, using the following schematic, For simplicity, the modulator circuit is also shown without bias supplies and a load resistor in place of the tank circuit. It is assumed that normal bias is applied the emitter-base junction, and that a reverse bias is applied to the collector junction. The modulation is injected across the emitter swamping resistor. Since the modulating signal is effectively connected in series with the emitter circuit it adds to the emitter bias when of the same polarity. When this voltage is opposite in polarity to the emitter bias it partially cancels and reduces the total emitter bias.

Thus the bias on the transistor is made to vary instantaneously above and below the fixed emitter bias level in accordance with the modulating signal: Assuming a sinusoidal modulating signal, it is evident that the instantaneous bias will vary sinusoidally. Since a change in bias will produce a change in gain, the instantaneous gain will also vary similarly. Consequently, the instantaneous amplification of the r-f carrier signal will also vary in accordance with the modulation, but in a different and opposite direction. (Common-emitter output polarity is opposite the input polarity.) For maximum modulation the a-f signal must be slightly greater than the r-f carrier input signal. To prevent distortion produced by driving the transistor into cutoff or into saturation, the modulation signal voltage must never exceed the d-c bias value.

The circuit of a typical capacitance-coupled emitter injection modulator is shown in the following illustration.

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**Emitter-Injection Modulator** 

The r-f input is applied to the base of Q1 through r-f transformer TI shown untuned for simplicity. Resistor RI and R2 form a base bias voltage divider from the supply to ground, which places a freed forward bias on Q1. Capacitor C2 bypasses the divider to ground to prevent r-f feedback into the bias supply. Resistor R3 and capacitor C3 form a conventional emitter swamping resistor bypassed to prevent degeneration. Only very slowly varying temperature changes produce a voltage across R3. (See the Introduction to the Amplifier Section of this Handbook for explanations of Bias Circuits and Bias Stabilization.) Transformer T2 is the collector output transformer with tuned primary L and C4 acting as a conventional tank circuit across which the output signal is developed. The secondary of T2 is comected to the next amplifier stage, or to a load (an antenna in special cases).

The bias voltage appearing across RI is the effective bias applied to the base of Q1 through the secondary of r-f transformer T1. Thus the r-f input voltage is applied in series with the dc bias provided by R1. However, capacitor C2 bypasses R1 to ground for rf and together with C3 effectively connects the secondary of T1 from base to emitter. As the input signal varies between positive and negative alternations, the emitter current varies similarly but oppositely (decreases on the positive part of the cycle and increases on the negative part of the cycle). The pulses of collector current applied across the tank load C4 and L produce an amplified sine wave of r-f of the same frequency as the input.

Consider now the effect of the modulating signal. Since the modulating signal is coupled through capacitor Cl, it appears as a varying of voltage across R3. While C3 bypasses R3 for rf, it is not large enough to bypass the a-f modulation. Thus the emitter voltage is alternately increased and decreased by the modulation which changes the base bias accordingly, so that the bias varies at the modulation rate. Consequently, the gain of the transistor is rdso changed at the modulation rate. The transistor is not exactly linear in its emitter-collector relationships, but is more linear than the base-collector relationship. While the output is not an exact replica of the input modulation, it will be similar in shape with troughs and valleys occurring at the same time but slightly distorted. Modulation is effectively linear from about zero to 96 per cent before the transfer characteristic rounds off. Above this range the distortion tends to become excessive. Therefore, "applications requiring full 100 per cent modulation generally employ the collector injection circuit, which will be discussed later in this section.

While a resistive collector load has been assumed for ease of explanation in the simplified circuit discussions, in practice a tuned (LC) tank is necessary to select the proper output frequency. In every modulator, there are sum and difference frequencies, and spurious frequencies are also generated (even in so-called linear modulators). Therefore, it is necessary to select the desired output frequency. In this case it is the frequency of the r-f carrier plus the sidebands generated in the modulation process.

#### Failure Analysis.

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General. When making voltage checks use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of conventional voltohmmeters. Be careful also to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low-resistance reading.

No Output. A defective transistor or open base circuit caused by a defective input transformer, or an open bias resistor will prevent operation. An open bias capacitor also can produce cutoff bias through degeneration if the r-f drive and the resistance in the

circuit are sufficient to block operation. Either of these conditions can be checked by means of a resistance or a continuity check with an ohmmeter. An open-circuited emitter, possibly caused by a defective swamping resistor, R3, will also stop operation. An open circuited collector will also stop operation; this condition can result from an open tank coil or a defective soldered joint, causing an extremely high resistance. Checking the collector voltage to ground will determine if this circuit is open. Improper supply polarity will reverse the bias, stop operation, and most likely ruin the transistor. In most cases, a simple resistance and continuity check combined with a voltage analysis, using a high impedance voltmeter, will locate any of the no-output troubles,

Low Output. Too low or too high a bias will cause clipping of the output signal, resulting in a low output with distortion. For maximum modulation, the a-f signal must be slightly greater than the r-f carrier input signal. Therefore, lack of audio gain, a defective coupling capacitor (Cl), or shorting the a-f signal to ground by a defective bypass capacitor (C3) can cause loss of or low audio, and produce a low-output condition. The use of an oscilloscope to check the waveform will permit the point in the circuit where the waveform is changed or lost to be observed. Lack of sufficient r-f drive will also produce a low-output condition, since the a-f functions merely to modulate the r-f carrier. A defective or mistuned tank circuit can also cause a low output condition, since the maximum output is developed on the same frequency as that of the input (carrier). Where the modulation is present but r-f drive is lacking no output will appear with normal af drive, since the collector load impedance (tank circuit) is too low to develop any voltage across it since it is tuned to the r-f signal.

**Distorted or Incorrect Output.** Distortion will be caused by improper bias and collector voltage, or by excessive input signals. Check the collector bias and voltage with a high resistance voltmeter. The r-f signal must not exceed the dc bias; otherwise, rectification of the rf will occur, and change the bias, and, as a result, produce clipping on the modulation peaks. If the a-f modulation is not of sufficient amplitude the peaks of modulation will also be lost and distortion will occur. In a similar manner, too great an a-f drive will send the collector current into the saturation region, and the troughs (negative peaks) will be cutoff, and distortion will result. The use of an oscilloscope permits waveform distortion to be observed and located. In the case of failure of the a-f modulation an unmodulated r-f output will be obtained.

If the tank circuit is too sharp (that is has too high a **Q**), sideband clipping will also result and the higher modulation frequencies will be lost. However, such a condition is not likely to be found in military equipment that meets specifications.

# SUPPRESSOR GRID MODULATOR

#### Application.

**The** suppressor-grid modulator is employed as a low-level modulator for pentodes in applications where a minimum of audio (modulator) power is desired. It is particularly useful in portable or mobile communications equipment to reduce size and power consumption.

#### Characteristics.

Varies grid-plate transconductance to achieve modulation.

Requires less audio power than grid modulator since only voltage drive is required, and no power is needed for modulation.

Produces maximum efficiency at 100 percent modulation, and minimum efficiency with unmodulated (carrier) conditions.

Provides a carrier power of only 1/4 that available for same tube in CW operation, and about 1/3 that possible with high-level plate modulation.

#### Circuit Analysis.

General. Suppressor-grid modulation is practically identical to control-grid modulation, with the exception that the suppressor grid is used to achieve the modulation instead of the control grid. This type of modulator, like the grid modulator, uses a form of efficiency modulation. It normally operates at half the maximum current under carrier conditions with no modulation, and at full current (twice normal) at 100 percent modulation. The efficiency is approximately 33 percent with no modulation and approximately 66 percent with full modulation. The carrier power represents 1/4 the maximum power available for the same tube operation, as a class C amplifier, with a peak power of four times the carrier value at 100 percent modulation. During modulation the average power increases to a maximum of 1.5 times normal at the peaks of modulation, and this power is

obtained from the same power supply by a change of efficiency within the tube.

It requires a negative supply for biasing the suppressor grid, which, since it acts as a gate between the screen and plate and is always negative, draws no current. Thus, very low modulation power is required, since only audio voltage is needed for control of the modulation. It does have the disadvantage, however, of causing a higher than normal screen dissipation. This is due to the fact that the plate current is cut off on the negative swing of the modulation signal, and the positive screen acts as a plate, resulting **in** greatly increased screen current. Distortion is approximately of the same order as that for grid modulation, since the linearity of the grid-plate transfer characteristic determines the basic minimum distortion inherent in the tube.

Circuit Operation. The basic suppressor-grid modulator is shown in the accompanying figure; for simplicity, sine wave generators are used to represent audio and r-f excitation. It is clear from the figure that the circuit is practically identical to that of the grid modulator except for the tube element used. The r-f amplifier stage operates as a conventional class C amplifier. Screen voltage is obtained through dropping resistor  $R_{sc}$ , bypassed by  $C_{sc}$ , and a fixed control-grid bias supplemented by grid-drive bias from  $\boldsymbol{R}_{\boldsymbol{g}}$  is used. With the suppressor grid biased negative from a separate supply, the carrier value of a current is **one-half** the maximum current. As the a-f voltage from the speech amplifier (represented by the a-f generator) is applied to the suppressor, it is (considering a sine wave) alternately aiding and opposing the suppressor freed bias. Thus on the positive halfcycles, it operates to reduce the suppressor bias and allow a heavier flow of plate current, while on the negative half-cycles, it adds to the suppressor bias to reduce the plate current. Therefore, the modulation is developed by plate current flow under control of the suppressor-grid voltage; in effect, the suppressor varies the grid-plate transconductance to achieve modulation.



**Basic Suppressor-Grid Modulator** 

The schematic of a typical suppressor-grid modulator is shown in the following figure. In the figure, T1 couples the output of the speech amplifier to the suppressor grid through RFC1, which prevents any feedback of rf into the audio circuit; capacitor C<sub>su</sub> grounds the suppressor for rf. Thus the d-c suppressor bias and instantaneous audio output signal (em), connected in series, are combined to provide an effective bias value, which adds on the negative peaks to increase the total bias, and subtracts on the positive peaks to decrease the total bias. The tube is biased class C with freed grid bias  $E_{cc}$ , bypassed by Cl. The freed bias is supplemented by grid drive bias through grid leak  $\mathbf{R}_{\mathbf{g}}$ , coupled from the r-f exciter stage through Cc. RFC1 isolates the bias supply, and Cl bypasses any excitation which may leak through the choke. The effective control-grid bias is that from cathode to grid, indicated by E. Screen voltage is applied through screen dropping resistor  $\mathbf{R}_{sc}$ , bypassed by C<sub>sc</sub>, with the plate series-fed through RFC2

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and bypassed by capacitor C2 in a conventional series-feed arrangement. Tank LC is tuned to the excitation frequency applied to the grid, and is coupled inductively to the output load,  $R_L$ .



#### Suppressor-Grid Modulator

When the modulating signal is applied,  $e_m$  varies from some negative value to a positive value which **just cancels**  $E_{cc3}$ , producing a variation of suppressor bias,  $E_{sp}$ , from zero at the maximum positive peaks of modulation to some negative value at zero modulation, or carrier level; it then increases to a greater negative value which is sufficient to reduce the plate current almost to zero on the negative peaks of modulation. Thus the plate voltage varies from a small minimum to practically full plate voltage as the plate current varies from maximum to zero in accordance with the modulation. The voltage drop across the tank circuit, EL, varies **simultaneously** from zero to maximum and back to zero, and the tank current is increased during the positive peak and

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decreased during the negative peak, effectively producing the modulation envelope. Since the tank is oscillating sinusoidally, the output is also sinusoidal, and is produced by pulses of plate current which increase the tank current to form the envelope shown in the following figure. It is clearly seen from the figure that while the transfer characteristic between the grid and screen is mostly linear, it curves off at the beginning and end, which corresponds to a biased-off suppressor condition and a zero-voltage suppressor condition, respectively. This shape is similar to that of the grid modulator transfer curve, and indicates that distortion is inherent and must always be more than that produced by plate modulation.



# Suppressor-Grid Voltage and Output Voltage Relationships

Use of the series screen-voltage dropping resistor,  $\mathbf{R_{sc}}$ , tends to reduce the screen voltage more as the screen current increases. Thus when the suppressor is being biased-off to the nonconducting state between screen and plate (by the negative modulation signal) the increased current attracted to the screen (it tries to act as the plate) automatically reduces the effective applied screen voltage by the increased drop across the screen-voltage dropping resistor,  $\mathbf{R_{sc}}$ . In this manner the extra screen dissipation is reduced somewhat at just the time it is becoming excessive. Hence, fixed screen voltage is usually never employed with this type of modulator.

**Detailed Analysis.** The basic functioning of the pentode modulator depends upon the suppressor grid and its control action. Consider the basic triode, for which a set of typical plate characteristics and transfer characteristics are shown in the following figure. It is evident from the plate characteristics that



**Triode Plate and Transfer Characteristics** 

for a **fixed** bias, there is a different plate current for each change of plate voltage. Note that the curves tend to be similar and equally spaced for equal steps of bias voltage. Likewise, on examining the transfer characteristic, it is seen that for each change of bias (with fixed plate voltage) there will be a different plate current; like the plate characteristic curves, these curves are similar and almost equally spaced for equal plate voltage steps. Thus it is clear that in a triode, one can vary the plate voltage and the plate current will follow, which is what is done in plate modulation. Likewise, one can vary the grid bias and the plate current will follow, which is what is done in grid modulation. Now examine the plate characteristics and transfer characteristics of a pentode, as shown in the following figure.



Pentode Plate and Transfer Characteristics

With the inclusion of the screen grid in the pentode, the plate current no longer follows the plate voltage, but is determined mainly by the screen voltage (assuming a fixed control grid voltage). That is, for a particular screen voltage, the plate current quickly reaches a particular value, as the plate voltage is advanced from zero toward a maximum, and remains substantially constant over a large range of plate voltage. Thus, varying the plate voltage has little effect on the plate current. Since these curves are parallel and almost equally spaced (for equal screen voltage steps), it can be seen that variation of the screen voltage will produce the desired variation of plate current, which is what is done in screen modulation (to be discussed separately). Upon examining the transfer characteristic it is seen also that for a specific screen voltage and for plate voltage from a low to a high value, there is little change in plate current as the bias is changed; in fact, for at least half of the operating curve they are identical. Now examine how the grid-plate transconductance varies with a change of suppressor voltage as the control-grid bias and screen voltage remain fixed, as shown in the following figure.



**GM** Variation with Suppressor Voltage

As can be seen, the transfer characteristic is practically linear, starting from a high value of transconductance at zero suppressor voltage and ending at a very small or zero value with a large negative suppressor voltage. It follows, therefore, that variation of the suppressor voltage will produce a relatively linear change in tube output. As a result, the suppressor-grid modulator is operated with a fixed negative control grid bias and a **fixed** screen voltage. (Since the control grid bias does not vary, the r-f excitation source need

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not have as good regulation as with the grid modulator; consequently, it need not supply as much grid drive power.)

Since the suppressor is placed between the screen and the plate, it exerts complete control over the plate current; when biased sufficiently negative it will cause plate current cutoff, while at just about zero bias it will permit maximum plate current **flow**. Because the suppressor is never raised above zero and is always negative, it draws no current; thus very little modulator power is needed – less than that for any other type of modulator. The suppressor bias is usually on the order of – 100 volts, and a simple voltage amplifier will completely modulate a highpowered pentode.

As the plate current is prevented from flowing to the plate by the negative suppressor bias, the screen becomes the only collector of electrons, and the screen tends to absorb them, acting as the plate. Thus screen-grid power dissipation becomes large on the negative portion of the modulation signal (the troughs), as shown in the following figure. By obtaining the screen voltage through dropping resistor  $\mathbf{R_{sc}}$  from the plate source, the increased screen current ( $\mathbf{i_{sc}}$ ) automatically causes a lower applied screen voltage, which reduces screen current flow during this period. Even so, the maximum screen dissipation is usually excessive during this period, because plate current cannot flow and all electrons are being handled by the screen.



**Screen Circuit Conditions** 

Now consider the tube's operation under carrier conditions with no modulation. Here the dc suppressor bias is adjusted for a negative value which produces half the maximum (full class C) value of plate current). The r-f drive and grid bias are set for the optimum values to produce this maximum loaded plate current. No modulation is applied to the suppressor (only the fixed dc bias), and plate current flow is as shown in part A of the following figure.

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Typical Operating Waveforms

As the modulation signal goes negative, the effective suppressor voltage is increased to further bias off plate current flow. At the negative peak of modulation (the trough), the instantaneous suppressor voltage,  $e_{cc3}$ , is just below cutoff (part B of the figure), and no plate current can flow. This is the time at which the screen is dissipating all the cathode (space) current, as explained in the previous paragraph. During the remaining half of the negative modulation cycle the suppressor voltage rises, becoming more positive as the negative modulation cycle approaches the zero modulation (carrier) level. At no modulation the conditions are as first represented in part A of the figure, with one-half the cutoff value of suppressor bias. Each drive pulse produces an output pulse of rf and a plate current pulse. The plate current averaged over the cycle is half maximum.

During the positive half of the modulation cycle, the negative suppressor bias rises above the cutoff level and reaches zero at the maximum positive modulation peak. At this time the plate current is twice normal (maximum) and the plate voltage is reduced to its minimum value, as shown in part C of the figure, but not to less than that of the screen voltage. If the modulation is sufficient to make the suppressor voltage positive, the suppressor tends to become the plate, and so does the screen (the screen voltage is now greater than the plate voltage as shown in part D of the figure). Thus, both the screen and suppressor grids carry the space current, and their dissipation ratings are exceeded. This is why the suppressor grid is never driven positive.

Once the modulation peak is reached, considering sine wave operation, the suppressor voltage becomes negative-going, and the resting or carrier condition is again reached at zero modulation. During the time of the positive peak the drop across the load (the tank circuit) is the greatest, and the greatest output voltage **is** developed and coupled to the antenna. Also, during this interval, the tank is actually absorbing power to replace any losses present as a result of resistance in the coil and leads. Conversely, during the negative peak, the tank is supplying the output since the tube is cut off and inoperative.

It can be understood from the previous discussion, then, that varying the instantaneous suppressor voltage in accordance with the modulation signal over a complete modulation cycle will vary the plate current to twice normal, and cause the plate voltage to vary similarly. Thus, on the modulation peaks, the power output is four times that of the carrier. Since sine-wave modulation is used, the average value of plate power will vary from the carrier to 1,5 times the carrier at 100 percent modulation. Thus, the conditions for AM modulation are produced by effectively varying the tube plate current flow, using the suppressor grid to accomplish tie variation under the control of a modulation voltage. Because the power is low, this is effectively an efficiency type of low-level modulator. Actually, the suppressor varies the final load line by controlling the grid-plate transconductance to vary the efficiency from a minimum value (about 33%) at zero modulation to full value (about 68%) at 100 percent modulation, as in the grid modulator.

#### Failure Analysis.

No Output. Lack of output should first be isolated to failure of the r-f amplifier stage or the modulation signal circuit(s). Even though the modulator is operative, an open plate r-f choke (RFC2) or tank inductor (L), a defective electron tube, or a lack of grid excitation to the r-f amplifier will produce a no-carrier condition. Observation of the r-f plate current meter will determine whether the plate circuit has continuity. Tuning the tank capacitor for a maximum plate current indication with a resonant dip will determine that the tank circuit is operative, and that sufficient drive, a load, and the proper bias exist for operation without modulation. Grid drive meter indications will also show whether the proper amount of r-f drive exists. With the proper grid current, if the plate tank can be resonated for a minimum dip and then loaded to the maximum current, the trouble is in the modulator circuit.

Lack of grid drive places the trouble in the exciter stages of the transmitter or in the coupling network to the final stage. Lack of plate current indicates possible power supply trouble or an open-circuited r-f stage. Otherwise, proper performance but lack of ability to load to maximum current indicates antenna trouble, improper tuning, a weak power amplifier tube, or a defective transmission line.

With an r-f carrier existing, the trouble is definitely in the audio circuits or in the modulation transformer, r-f choke, or suppressor bypass capacitor. An open transformer secondary would remove the bias to the suppressor grid and cause an abnormal plate current reading without modulation, while a shorted transformer **would** allow the proper plate current and apparently normal carrier operation, but no modula-

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tion could occur (depending upon the effectiveness of the short circuit).

High transmitter plate current usually indicates short-circuited components or a lack of proper bias, while low plate current indicates excessive bias, highresistance joints, low tube emission, or a possible lack of sufficient coupling to the load. With open-circuited conditions indicated on the equipment meters, a simple resistance analysis made with the power OFF, and with the high-voltage supply grounded for safety, will quickly determine the defective components.

Low Output. It must first be determined whether the low output is from lack of sufficient audio drive or from an actual reduction in the percentage of modulation. While low modulation is usually due to lack of sufficient audio drive, this can also occur because of a reduced setting of the audio gain control or because of trouble in the speech stages. An oscilloscope is very useful in determining the cause of malfunctioning, since the waveform itself may be directly observed. For simple, quick tests of modulation percentage, a trapezoidal pattern is useful. A waveform check, however, will not only show percentage of modulation but will also indicate waveform distortion, so that it is usually more useful. Too high a suppressor-grid bias will cause a reduction of output and an inability to reach 100 percent modulation with the same drive. The same effect will also occur if the control-grid bias is too high. Temporarily grounding the suppressor grid will produce maximum output if the control-grid bias is satisfactory. If incorrect control-grid bias is suspected, the bias can easily be checked by a simple voltmeter indication (use an r-f choke in series with the meter probe to avoid erroneous indications). As with the grid modulator, a steadily indicating plate meter does not necessarily indicate that there is no distortion or overmodulation. Since the changing of efficiency in the plate circuit is used to obtain the modulated output, although the plate current is changing instantaneously, one condition may cancel the other. Thus, either a steady current indication or a flickering current indication can be indicative of the same condition. It has been found that satisfactory operation requires the use of an oscilloscope to properly adjust the suppressor voltage and load for 100 percent modulation with a minimum of distortion.

Because of the low power involved, a partially shorted modulation transformer will not usually indicate its condition by external burnt spots or arcing. It will probably show as an inability to obtain 100 percent modulation, with all other components checked and the circuit apparently working normally in all respects. Where available, a negative variable dc source can be used to simulate the change in bias with modulation, to quickly determine whether the stage is operating properly; if it is operating, the transformer certainly must be defective. Lack of sufficient filament emission in the r-f amplifier or modulator tube will cause peak **clipping** and a lower output because of the inability to obtain 100 percent undistorted modulation.

**Distorted Output.** Distortion can occur from a number of causes, and is easy to detect when monitoring audio modulation. Overmodulation will cause a chopping off of the carrier with carrier shift, producing severe interference to stations operating within a few hundred KHz of the carrier, and distortion. Nonlinearity in the control of the grid-plate transconductance by the suppressor grid bias will show as distortion; that is similar to the distortion caused by curvature of the grid-plate transfer characteristic in grid modulation.

In stages operating on the same input and output frequencies, there is the possibility of feedback from plate to grid, causing self-oscillation with severe distortion. Although the low plate-grid capacitance of the pentode makes this almost impossible, it does occur sometimes as a result of poor layout and extemal coupling between the tube elements, particularly at high frequencies. Self-oscillation can be easily detected by the characteristic fuzzy pattern produced on an oscilloscope. Oscilloscope connections and waveforms are shown in the Basic Measurements section of the EIMB, NAVSHIPS 0967-000-0130, Test Methods and Practices.

Since the suppressor grid does not draw current, the modulator has no trouble with changing load conditions as in the grid modulator; thus the distortion is usually limited to that caused in preceding speech amplifier stages. GeneraLly speaking, there should be less distortion present in the suppressor-grid modulator than in other types of grid modulators.

### SCREEN GRID MODULATOR

#### Application.

**The** screen grid modulator is employed as a low. level modulator for screen grid tubes (tetrodes and pentodes) in applications where it is desired to use a minimum of audio (modulator) power. It is particularly useful for portable or mobile communications equipment to reduce size and power consumption.

#### Characteristics.

Varies screen voltage to achieve modulation.

Requires slightly more power than control-grid modulator (about 1/4 the rated screen input for CW).

Produces maximum efficiency at 100 percent modulation and minimum efficiency for unmodulated (carrier) conditions.

Provides a carrier power of 1/4 that available from same tube in CW operation, and about 1/3 that possible with high-level plate modulation.

#### Circuit Analysis.

General. Screen-grid modulation is practically identical to the other types of grid modulation, with the exception that the screen grid is used to achieve the modulation instead of one of the other grids. This type of modulator, like the grid modulator, uses a form of efficiency modulation. It normally operates at half the maximum plate current in the resting or carrier condition, with no modulation, and at full current (twice normal) at 100 percent modulation. The efficiency is lowest, (about 33%) with no modulation, and highest (about 66%) with full 100 percent modulation. The carrier power represents onequarter of the maximum power available with normal class C operation, with a peak power of four times the carrier value at 100% modulation, During sine wave modulation, the average power increases to a maximum of 1.5 times normal at the peaks of modulation, and this power is obtained from the same power supply by the change of efficiency within the tube.

This type of modulator requires a screen supply with good regulation, since the load, plate, and screen L

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#### MODULATORS

currents are instantaneously varying during modulation. It has the inherent disadvantage of being unable to achieve 100 percent modulation without distortion unless special compensation is provided.

**Circuit Operation. The** circuit of the basic screengrid modulator is shown in the accompanying figure, using sine wave generators to represent audio and r-f excitation for simplicity.



**Basic Screen-Grid Modulator** 

It is clear from the figure that the circuit is practically identical to that of the control-grid or suppressor-grid modulator except for the tube grid element used. The conventional LC tank appears in the plate circuit, inductively coupled to the output load (antema). The r-f drive is simulated by the rf generator, and supplies grid drive bias through 1\$ in addition to the fixed negative bias,  $E_{\text{cel}}$ . As can be seen in the figure, the a-f generator supplies the modulation in series with the applied screen voltage. Thus as the modulation increases on the positive half-cycle (assuming a sine wave), the screen voltage and modulation add to produce a larger screen voltage. This increased screen voltage causes a greater plate current flow. On the negative half-cycles the modulation opposes the positive screen voltage, so that at the negative peak of modulation (at the trough) the screen voltage is effectively zero, almost preventing plate current flow.

Although the screen voltage is zero, the inherent construction of the tube requires that a negative

potential be applied to the screen to completely stop plate current flow. Therefore, this type of modulator provides approximately 75% maximum modulation without distortion. If completely (100 percent) modulated, considerable distortion is produced.

Basically, however, by varying the screen potential in accordance with the modulation, a corresponding change in plate current is achieved, driving the plate current to twice the normal (carrier) value at 100% modulation and to almost zero on the negative peaks. This can be recognized as the same variations of current and voltage as described in the previous forms of grid modulators to produce amplitude modulation.

A schematic of a typical screen-grid modulator is shown in the accompanying figure.





In the figure, the r-f drive is coupled through  $C_c$  to the grid of VI, producing grid current and developing griddrive bias across  $\mathbf{R_g}$ , which is effectively in series with the freed negative bias supplied by  $\mathbf{E_{cc1}}$ . (Actually, cathode bias could be used instead of  $\mathbf{E_{cc1}}$ since screen current always flows.) The plate circuit **contains** the conventional series-fed tank, isolated from the power supply by the rfc and bypassed by C3. In the grid circuit the rfc isolates the rf drive from the bias supply; it is bypassed by C1, which shunts to ground any rf leaking through the choke.

The audio modulation is coupled from the speech amplifier plate through transformer T1, whose secondary carries the d-c screen supply. Capacitor C2 serves to ground the screen grid as far as r-f variations are concerned, but is not large enough to bypass any of the audio modulation; otherwise, frequency distortion would result from a loss of the high frequencies bypassed to ground.

When the audio is applied to the screen of V1 through T1, and assuming a sine wave modulating signal, the screen voltage is increased on the positive half-cycle, and decreased on the negative half-cycle. Thus, as the positive modulating signal adds to the screen voltage, the screen current and the plate current both increase, reaching a peak at 100% modulation. Since the output voltage is the drop across the load, the output is the greatest at maximum plate current, and the actual plate voltage is at a minimum. As the modulation swings downward toward the negative half-cycle, the screen voltage is opposed by the negative modulation signal from T1. At the negative peak of modulation (the trough), there is practically complete cancellation of the screen voltage, and the screen current decreases to a minimum at this point. The output voltage is also minimum at this point, and the actual voltage,  $\mathbf{E}_{\mathbf{b}}$ , is practically equal to the applied plate voltage, Ebb. At resting or carrier value, the screen voltage is such as to produce one-half the maximum plate current obtained at 100 percent modulation (approximately one-half the value used for CW). Thus, as in other forms of grid modulation, the carrier value is one-fourth maximum, with a peak of four times the carrier value of power. The average power varies with sine wave modulation to 1.5 times the carrier value at full (100 percent) modulation. This extra power is obtained from the plate power supply. The power change is achieved by the changing efficiency of the plate circuit, produced by varying the screen voltage of the tube in accordance with the modulating signal. The following figure shows the screen voltage and output voltage relationships assuming that 100 percent modulation could be achieved, and illustrates the reason that screen-grid modulation cannot achieve 100% modulation without distortion. On the positive modulation peaks (approaching saturation), the grid-plate transfer curve flattens off so that large drive in the positive direction will flatten the peaks, causing distortion. Likewise, since zero screen voltage cannot produce plate current cutoff, the transfer curve drops off considerably at the zero screen voltage level. The effect is as though the bottom portion of the negative peak (the trough) of the modulation were cut off. To minimize this distortion, the screen must be operated between the limits where it is most linear; the practical result is to limit the modulation to about 70% for minimum distortion. In specially designed circuits where both the grid and screen are simultaneously modulated, this inherent fault can be overcome, but the modulation is no longer screen modulation; it is rather a combination of both types, and thus will not be further discussed.





**Detailed Analysis.** To understand the functioning of the screen-grid modulator, it is necessary to review the basic tube action and design. The accompanying figure shows a set of characteristic curves for a typical tetrode.

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**Tetrode Plate and Transfer Characteristics** 

First examine the plate characteristics and note that for each fixed value of screen voltage  $(E_{scl_2})$ etc) a particular plate current can be obtained, which, after the lower plate-voltage region is passed, increases constantly as the plate voltage is increased. This is not a linear relationship; it is actually considered mathematically to be a 3/2 power relationship. Note that at the higher-voltage end of the plate characteristic chart, the distances between the curves for each screen voltage are nearly the same, and the lines are roughly parallel. Hence, it can be inferred that if the plate voltage is held freed while the screen voltage is varied, there will be a somewhat linear relationship. That is, for a corresponding increase or decrease in screen voltage, there will be a proprotional change in plate current. This means, then, that as the screen voltage is changed the plate current will follow, varying in a similar fashion. Since the output voltage is produced by the flow of plate current through the plate load, it is clear that the output voltage will vary similarly with the plate current. Examination of the grid-plate transfer characteristic shows that for a **fixed** screen voltage  $(E_{sc})$  the plate current  $(i_p)$  does not vary much for low voltages (such as  $E_{b3}$  or  $E_{b4}$ ), but does change somewhat for larger voltages (such as  $E_{b1}$ ); it is affected more by control grid voltage changes (e<sub>c</sub>). Thus, basic tube action indicates that either control-grid or screen-grid modulation is possible, and that plate modulation by variation of the plate voltage alone on screen grid tubes is not feasible.

Consider now the r-f drive and bias. Since the modulated r-f amplifier is to operate as a class C stage, the bias must be approximately twice the value of cutoff for a freed screen voltage, and sufficient drive must be applied to drive the stage into light

saturation on the positive peaks of the drive signal. (Refer to Section 5, Part 5-6, RF Power Amplifiers Class B or C for background on Class C operation.) The value of bias and excitation must be such that the plate voltage never drops lower than the screen voltage on the peaks of the modulation. Otherwise, excessive screen dissipation would occur, with the screen -trying to act as the plate. The resting or carrier value of current is adjusted for exactly half the maximum load current, with the stage operating over the linear portions of its characteristics. Because of the varying efficiency and load changes, it is necessary to use an oscilloscope to determine proper operation.

Assuming perfect linearity, a typical oscilloscope presentation showing 100% modulation would appear as shown in the following figure. Note that the amplitudes between the line representing the carrier (C and



Ideal Trapezoidal Pattarn

D) and the ends of the pattern are equal, with straight sides indicating equal and linear modulation. Also, note that lines A and B extend equal distances above and below the carrier level (with  $AB = 2 \times CD$ ), and that the pattern extends to a perfect point at O, indicating 100Yo modulation. Let us now examine a similar pattern illustrating screen-grid modulation, and note the differences.

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Trapezoidal Pattarn for Screen Modulation

Note that the sides are straight from points X and Y upward, indicating linearity between these points, but between O and X-Y the curvature indicates serious distortion. The distance XY as compared with AB indicates that the distortion occurs at about 70 to 75% modulation. Thus, the carrier must be adjusted so that it is centered at the point where line segments 1 and 2 mark off equal distances over the linear portion of operation if distortion is to be avoided. The illustration graphically shows the limitations on maximum modulation percentage without distortion for screen modulation. If operation is held to the left of the indicated carrier line to achieve 100% modulation, the distortion shown between points O and XY must be accepted.

The inability of the pattern to attain a point at O indicates that the maximum negative portion of the modulation signal does not quite reach cutoff and 100% modulation is not obtained. The distortion shown between O and XY is caused by actually driving the screen negative with the modulated signal on the negative peaks, to attempt to produce the cut-off of plate current. The reason for the departure from linearity is that with zero screen voltage at points X and Y, any slight change in the negative direction of screen voltage changes the plate current much more rapidly than does a similar positive in-

crease in screen voltage. Hence, the line no longer remains straight; it has a faster slope, and curves rapidly downward toward zero or maximum negative modulation (the trough). In effect, we can say that at the zero screen voltage level, the tube no longer modulates equally above and below this point; hence the reason for the rapid change of waveform. The point of zero screen voltage is determined to some extent by the bias and grid drive. Thus, for particular value of bias it is possible to apply just sufficient drive to reach the peaks on the positive modulation cycle and move point XY to the left slightly to attain linear modulation over a greater portion of the cycle. Such an adjustment, however, must be made with an oscilloscope; it cannot be predetermined by design.

In Navy equipment, the design and adjustments are preset by the manufacturer so that by setting the operating values of plate current and voltage to those listed in the Technical Manual for the equipment, the proper results will be obtained to meet the manufacturer's specifications.

Consider now the modulator power requirements. Since the screen is being modulated, the peak screen voltage divided by the peak screen current will provide the maximum load impedance value. A rough approximation of power can be obtained by using the peak screen voltage and current and dividing by 8. Thus, for a 400-volt, 10-milliampere screen load, 500 milliwatts (1/2 watt) is required for maximum modulation. To help stabilize the constantly varying load and keep power supply fluctuations to a minimum, and to achieve good regulation of the modulator, a power capacity of three to four times this value would be used (1-1/2 to 2 watts), and the modulator would be loaded down with a swamping resistor to stabilize the load. With the 400-volt, 10-ma load, 40,000 ohms would be indicated. By providing 40,000 ohms for each half-watt, a totrd load of 10,000 ohms would be obtained with a 2-watt amplifier as modulator. Thus, reflected load changes in the screen circuit are minimized so that the modulator provides sufficient current and voltage for stable operation.

Another method of accomplishing the same thing is to use negative feedback in the modulator. This tends to reduce the plate resistance and the sensitivity to voltage changes caused by load changes. In addition, negative feedback helps improve the modulator frequency response, so that resistance loading has been generally discarded, although it may be occasionally encountered.

It is evident, then, that screen-grid modulation requires somewhat more power than the other types of grid modulation (because of screen load and regulation requirements); in turn, however, it provides better over-all linearity. In summation, it can be said that screen-grid modulation achieves its changing efficiency by operating on a different load line for each value of screen voltage, with maximum plate dissipation occurring at the carrier level.

#### Failure Analysis.

**No Output.** Lack of output should first be isolated to failure of either the modulated r-f stage or the modulator and speech circuits. Lack of a carrier output indicates failure of the r-f stage, while lack of modulation on the otherwise normal carrier indicates failure in the speech or modulator stages, or a lowered gain control. A no-carrier indication can be caused by an open plate rfc or tank circuit, a shorted or gassy electron tube, lack of grid excitation, too high a bias, or lack of screen voltage due to a defective modulation transformer, a shorted screen capacitor, or a defective screen supply.

Observation of the r-f plate current meter will determine whether the plate circuit is open, and tuning for maximum indication with a resonant dip will determine whether sufficient drive and load and the proper bias are present. Where grid current meters are part of the equipment, the obtaining of normal or greater than normal grid current indicates that the exciter stages are operating properly; with lower than normal grid current, the driver stages are at fault or the d-c bias on the control grid is too high. The bias may be determined by a simple voltage check (use an rfc in series with the voltmeter test prod, and check the grid to ground voltage). Inability to load the stage indicates a faulty antenna or a transmission line trouble.

With the r-f normal, the trouble must be in the modulation transformer, screen bypass capacitor, or the preceding speech stages. An open modulation transformer would remove the dc screen voltage, and the r-f stage would give a no-output indication. With a short-circuited transformer, the r-f stage would appear to operate normally, but no modulation would be obtained. With the low power usually involved, it is doubtful that visible evidence such as charred insulation or arcing would be apparent, so that it may be difficult to isolate modulation transformer trouble if the transformer is internally shorted. Usually a resistance analysis will check continuity. Checking the transformer for turns ratio with an ac source and a voltmeter will usually determine whether it is operating properly.

High plate current usually indicates short-circuited components or a lack of proper bias, while low plate current indicates excessive bias, high-resistance joints (poor soldering), low tube emission, or possible lack of sufficient coupling to the load. With open-circuited or short-circuited conditions indicated on the equipment meters, a simple resistance anrdysis made with the power OFF, and the high-voltage supply grounded for safety, will quickly determine the defective components.

Low Output. First determine whether the low output is due to lack of sufficient audio drive, or to an actual reduction of percentage modulation as a result of trouble in the modulator. With the speech gain control at its proper setting, low output indicates loss of audio (modulator) power or lack of r-f drive. Use an oscilloscope to determine the cause of malfunctioning. Make a trapezoidal check of modulation percentage to determine whether 100% can be obtained. Since some distortion is normal, the trapezoidal check can be used as a rough check on linearity by determining whether the sides of the pattern are straight and observing that the pattern expands equally on both sides of the carrier line; otherwise, the positive and negative peaks are unequal.

If you are unable to reach the 100% modulation mark, reduce the loading and see whether the percentage improves. Too great a load can produce too high an efficiency and make it impossible to obtain the proper output from the modulator. Under normal operation (no modulation) the tube must be drawing no more than half the maximum plate current possible in normal **class** C operation.

Since grid drive determines the efficiency to some extent, reduce the drive and see whether the percentage of modulation improves. It will probably be found that there is a point of minimum grid drive and minimum loading that will produce a completely modulated signal. At other settings the output may be greater, but it will be impossible to obtain complete modulation. Use the lower output, since loss of modulation varies as the square of the modulation factor; that is, 25% loss of modulation is actually a

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**50%** loss of usable power, and can be the difference between being heard and not heard at all.

Low output caused by lack of sufficient drive will be indicated by a flattening of the positive peaks because of inability to reach full peak power. Lack of sufficient filament emission can also cause a similar condition.

**Distorted Output.** Distortion can occur from a number of causes, and is easy to detect when monitoring audio modulation. **Overmodulation** will result in a chopping off of the carrier, with carrier shift, causing excessive distortion and severe interference at stations within a few hundred kilocycles of the carrier. Since in screen-grid modulation it is necessary] to drive the screen negative to obtain 100% modulation, it is to be expected that a large amount of distortion will occur on the peaks. For undistorted output, the screen should never be driven negative.

Because of the constantly varying load, the speech amplifier producing the audio modulation will contain excessive distortion unless swamping resistors are used to load the modulation transformer, or unless negative feedback is used. In this event, using an oscilloscope to determine linearity between the input and output signals in the modulator will quickly locate any excessive distortion in those stages. (Refer to NAVSHIPS 0967-000-0130, Test Methods and Practices, Basic Measurements Section, for oscilloscope connections and waveforms.)

Although screen-grid tubes provide sufficient gridplate isolation, so that neutralizing is unnecessary, it is possible that at the very high frequencies selfoscillation can occur in the r-f stage and cause distortion. This is particularly true if parts have been replaced and the lead dress has been disturbed. The characteristic fuzzy pattern (on an oscilloscope) produced by oscillation will quickly reveal this condition.

Inability to obtain full modulation can be due to the lack of filament emission in the r-f stage, which will cause flattening of the positive peaks and a consequent increase in distortion. This condition can be seen on an oscilloscope, but it will not normally be revealed by meter indications, except by a gradual reduction of plate current over a long period of time. A similar condition can result from drying out of electrolytic falter capacitors in the power supply, but it will usually show as hum on the carrier before the loss of peak current and voltage causes noticeable distortion. Such conditions are not apparent unless an oscilloscope is employed to monitor the waveform.

# PLATE AND SCREEN MODULATOR

# Application.

The plate and screen modulator is employed as a high-level modulator for screen-grid tubes **(tetrode** and pentode) in applications where the simplicity and fidelity of plate modulation are desired.

### Characteristics.

Varies both the plate and screen voltages to achieve modulation.

Requires a modulator power equivalent to 50 percent of rated carrier plate and screen power.

Operates at a constant efficiency of 70 percent or better.

Provides maximum carrier power for a given tube **type**.

# Circuit Analysis.

General. The plate and screen modulator is practically identical to the triode plate modulator, except for provisions to accommodate the changes caused by introduction of the screen grid into the tube. This type of modulator is not a low-level form of modulator; instead, it is a high-level constant (high) efficiency type of circuit. The modulator itself must furnish the 50 percent additional power required for the production of the side-bands. The modulated r-f stage must also have a power supply capable of supplying the additional power for the screen circuit, or have a separate screen supply to furnish the power for the screen. During sine wave modulation the plate voltage and current are doubled to provide a peak power of four times normal, and the average power is increased to a maximum of 1.5 times normal carrier value, thus providing the proper conditions for 100 percent AM modulation. The use of the screen-grid tube, with its low grid-plate capacitance and shielding effect, reduces the internal plate-to-grid feedback, minimizing the possibility of self-oscillation and the need for neutralizing circuit arrangements. The increased sensitivity of the screen-grid tube also permits less excitation and driving power to be used \_ as compared with the triode.

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**Circuit Operation.** A simplified diagram of the basic transformer-coupled plate and screen modulator is shown in the accompanying figure. The a-f modu-



**Basic Plate and Screen Modulator** 

later stage is represented as ablock, since it may be any one of a number of audio amplifier combinations as long as the proper audio power output is obtained. Likewise, the r-f output stage is also represented as a block, since it may consist of any arrangement of tubes to produce the desired carrier output to the antenna. The r-f stage is always biased so that it operates as a class C amplifier. Since class C operation requires twice the cutoff bias, a separate bias supply is usually used, with supplemental bias from grid drive through a grid leak. The total bias is a combination of the two types. In case of failure of grid drive, the freed bias provides a protective bias to prevent exceeding tube ratings and consequent damage to the tube. Thus far in the discussion the plate and screen modulator is identical with the plate modulator. The difference lies in the manner in which the modulation is achieved, that is, by also modulating the screen voltage. There are three basic methods used; each will be discussed in the following paragraphs. For the present it suffices to say that both the screen and plate voltages are varied from zero to twice normal to accomplish the modulation exactly as described for the plate modulator discussed previously.

#### ORIGINAL

Screen Voltage-Dropping Circuit. Since the screen voltage is always much lower than the plate voltage, it is necessary either to provi& the screen voltage from a separate power supply, or to obtain this voltage from the plate supply by means of a series dropping resistor. By far the simpler method, although somewhat wasteful of power, is the use of a "series drop ping resistor, as shown in the following figure. As can be seen from the illustration, the screen voltage is obtained by a series voltage dropping resistor (R<sub>sc</sub>) connected to the plate supply. The screen current through this resistor produces sufficient voltage drop to lower the plate supply voltage to the proper value for application to the screen. The actual screen voltage at **all** times is the supply voltage minus the drop across the resistor  $(E_{sc} = E_{bb} - IR_{sc})$ .



Plate-and-Screen-Modulated Pentode

As shown, the r-f grid excitation is capacitively coupled through Cc, and grid drive bias is obtained **through**  $\mathbf{R}_{g}$ , supplemented by freed negative bias. The rfc isolates the r-f drive and prevents it from feeding back through the grid supply or from shorting to ground, while Cl provides an r-f shunt to ground for any remaining rf which might leak through the rfc.

The suppressor grid is shown supplied with a small positive bias and shunted to ground for rf by C2. This connection will vary according to the type of tube. In tetrodes (since they do not have a suppressor grid) it is nonexistent. In beam-forming screen grid tubes it will be the beam-forming plates, and will be connected as recommended by the tube manufacturer. In other types of pentodes the suppressor may be internally or externally connected to the cathode directly, and C2 is not needed. In those types of pentodes which require it, the suppressor connection will appear as shown on the schematic above. In this instance the slight positive bias is added to enhance the shielding effect of the suppressor at low plate voltages, and it also 'prevents the screen from intercepting any secondary electrons and acting as a plate. At almost zero voltage, any electrons will be attracted to the more positive suppressor and returned to ground. Thus zero plate current is possible with a sharper cutoff than when the suppressor has a negative potential applied. The screen grid voltage is obtained from the plate voltage source through screen voltage dropping resistor  $\mathbf{R}_{sc}$  bypassed by C3 and C4. Capacitor C3 also insures that the screen is at ground potential to rf, permitting only dc or the relatively low-frequency modulation components to vary the screen voltage. Capacitor C4 is the conventional series plate-feed bypass capacitor. The secondary of T1 is connected in series between the plate-and-screen power supply, with the rfc isolating it from the tank circuit rf. Capacitor C4 also insures that any rf which might leak through the rfc is shunted to ground, and its reactance is high to audio frequencies in order to prevent loss of high-frequency response. The conventional tank components, C and L, are inductively coupled to the load. The audio output from the modulator appears at the secondary of T1, and is added to or subtracted from the applied dc plate voltage (and screen voltage) to produce an instantaneous effective plate (and screen) voltage which varies in accordance with the modulation.

Consider now one cycle of operation. At the resting condition, with no modulation, an unmodulated carrier is produced, and the applied plate and screen voltages at that time consist of only the dc component from the power supply. As the modulation is started, assuming a sine wave progressing from zero through the positive half-cycle, the instantaneous audio output voltage (from  $T_i$ ) adds to the positive plate and screen voltages, and both voltages are increased. The following illustration shows how the plate and modulation voltages are combined to form the composite instantaneous plate voltage. (The screen voltage is also modulated similarly.) Since a

resistor is not frequency-sensitive, equal voltage drops occur across the screen dropping resistor for all audio frequencies in the modulation; thus the screen voltage is dropped linearly and is also increased linearly with respect to the modulation signal. At the positive peak of modulation, the plate voltage is twice normal and the screen voltage is somewhere between 1.5 to 2 times normal, depending upon the screen current (usually around 1.5 times). It can be seen that, since the d-c screen voltage is increased by the addition of the instantaneous modulation component, the same result is produced as in screen modulation; that is, the plate current is increased. Because the plate voltage is also increased simultaneously and the class C output is proportional to the square of the plate voltage, the plate voltage also helps to increase the total tube current. Recalling from basic theory that the screen voltage determines the plate current much more than the plate voltage, it can be understood that variation of plate voltage alone would not produce 100ZO modulation since the tube current would not increase sufficiently on the peaks. (For an unmodulated screen, about 90 to 95 percent is the highest modulation obtainable.) Thus it is clear that variations of both the plate voltage and the screen voltage combine to produce the 100 percent modulation capability.



**Combining of Plate and Modulation Voltages** 

As the modulation proceeds toward its negative half-cycle, both the screen voltage and the plate voltage are reduced, and the plate current follows. Thus at the negative peek (the trough) of modulation the plate voltage is almost zero, and so is the screen voltage. Actually to avoid excessive screen dissipation, the plate voltage is never driven below the screen voltage. In this case, since the screen voltage is obtained from the plate source through a dropping resistor, the screen voltage is always lower than the plate voltage; thus it is practically impossible to drive the plate voltage to zero, except if the screen is driven

negative. With negative screen drive, non-linearity causes distortion, so that normally the modulation is adjusted to just keep from driving the screen below zero. Normally, the plate current is reduced to a value near zero, and **full** modulation from zero to twice normal plate current and voltage are obtained. The peak power is four times the normal carrier value, and the average power increases supplied by the modulator is 1.5 times normal, or 50 percent of the rated carrier power.

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Separate Screen SupPIY Circuit. The second and more complicated method of supplying screen voltage, but perhaps the more commonly used method, is to supply the screen voltage from a separate power source. This circuit is shown in the following figure, and is seen to be identical to that of the plate and screen modulator just discussed, except for the replacement of  $\mathbf{R}_{sc}$  with choke  $L_1$  and a separate screen supply. The screen power supply need only supply a fraction of the plate power. Most screen grid transmitting tubes use from 250 to 750 volts on the screen, with a plate voltage of 1000 to 4000 volts, and screen dissipation runs from 5 to 10 percent of the plate dissipation for high-power tubes, to 10 to 20 percent for low-power tubes, or a maximum of about 50 watts for medium power transmitters. This screen power supply provides only dc voltage; therefore, some provision must be made to increase and decrease the screen voltage in accordance with the modulation, to control the plate current. Such action is produced by the choke, L<sub>1</sub>, placed in series with the screen lead. From basic theory it is known that the electrical inertia produced by the field around the choke tends to prevent a change in the flow of current through the choke. When the current ceases or reduces, the magnetic field collapses and tends to produce a voltage from the choke which will keep current flowing in the same direction. To do this it is evident that the voltage produced must be of the same polarity as that applied originally to the choke. When the modulation signal goes positive and

increases the plate voltage, more electrons are attracted to the plate and less to the screen grid. That is, the total space current remains about the same, but the current distribution between the screen and plate changes. When the screen current reduces, an increased voltage is produced in the same direction, to add to the effective screen voltage before the modulation increased; this produces a slightly higher screen voltage, which, in turn, helps the plate current to increase. On the negative modulation swings, a similar but opposite condition occurs. As the plate current tends to reduce, the screen current tends to rise. The inertia of the choke tries to prevent the rising current and provides a negative-going voltage which decreases the effective positive screen voltage. Thus the plate current is helped to decrease. Since the screen grid controls the plate current much more effectively than changing the plate voltage, the slight changes in screen voltage produced by the choke, in turn, produce the desired effect. Capacitor C2 bypasses the screen to ground and prevents feedback of rf into the audio circuits. Capacitor C3 is the conventional plate bypass for series feed. The value of C3 is usurdly such that it has a high reactance to the audio frequencies, in order to avoid the possibility of frequency distortion due to shunting of the highs to ground. The screen bypass capacitor is usually about twice this value, since the reactance of choke  $L_1$  is effectively in series with the capacitive reactance, limiting the shunting effect of C2. The choke must have sufficient power-handling capability to carry full screen current, and is usually on the order of 5 to 10 henrys. If it is too small, 100 percent modulation will not be obtained, and if too large it will produce phase shift at the low audio frequencies and attenuation at the high audio frequencies, causing some distortion. The actual value is chosen to have a reactance which is not less than the screen impedance at the lowest desired audio frequency. The screen impedance is approximately equal to the dc screen voltage divided by the dc screen current (Z = Esc/Isc).



Plata-and-Screen-Modulated Pentode with Separate Screen Supply

With this circuit, actual cutoff bias can be obtained, so that the bias can be adjusted for twice the cutoff value for proper class C operation. (With the voltage-dropping resistor type of circuit, the screen voltage becomes so high at low plate current that cutoff can never actually be attained; thus the theoretical value specified by the manufacturer is used to determine the operating bias.) As far as modulation is concerned, the choke produces voltage variations on the screen in phase with the modulation; this causes the plate current to increase on the positive modulation excursions and to decrease on the negative excursions, assisting the plate voltage variation, since variations in screen grid voltage have more control over the plate current than do variations in plate voltage. Thus the full limits of AM modulation are obtained, exactly as if' the tube were a triode and were completely controlled by plate voltage variations. Peak power is four times the normal carrier value, and the output increases 50 percent at full modulation, being supplied from the modulator. At the peak of modulation, maximum plate dissipation and power output occurs, with the efficiency remaining relatively constant throughout the audio cycle.

**Transformer-Coupled Screen Modulator.** The third basic method of plate and screen modulation is

to provide an extra winding on the modulation transformer to provide the proper voltage ratio. In this method the dc screen voltage from a separate supply has amodulation component added which is proportional to the plate change in accordance with the transformer turns ratio. This method is costly, and is seldom used because of the simplicity of the previously described methods. The circuit operation is similar to that for the voltage-dropping method, except that the transformer, instead of the dropping resistor, supplies the proper voltage. Therefore, this method will not be further discussed.

**Detailed Analysis.** To understand the functioning of the plate-and-screen-modulated circuit, review the operation of the triode plate modulator previously discussed in this section before proceeding further. It is evident now that the only differences between the two circuits are those resulting from the addition of the screen grid to the tube. It is necessary to return to **elementary** electron tube theory to explain some of the differences in operation caused by the screen grid.

The addition of the screen grid provides a greater grid-plate transconductance, and, consequently, requires less drive power from the r-f driver to excite the modulated class C stage to saturation. Since the screen is located between the grid and the plate and always has a positive voltage applied, the problem of minimizing grid dissipation at minimum plate voltage is eliminated. (On the peak of the negative plate excursion, during modulation, the triode grid tends to become more positive than the minimum value of plate voltage. As a result, excessive grid current flows and causes the grid dissipation to increase.)

While in the preceding discussions we have spoken of having the modulation voltage reduce the screen and plate voltages to zero, during the modulation cycle, this does not exactly occur. The action which does occur can be understood more clearly if the desired action is first explained. In this instance, the object is to reduce the plate current to zero, during the conducting period of the class C cycle, coincidentally with minimum (almost zero) plate voltage, which is produced when the negative peak (trough) of the modulation effectively cancels the applied plate voltage. Since the screen voltage exercises a greater controlling factor than the plate voltage, it is possible to reduce the plate voltage practically to zero without actually reducing the screen voltage to zero. When the drop across the load makes the actual plate voltage zero, the applied voltage is still above zero by the

amount of voltage drop in the load. This is the applied screen voltage, which is still further reduced by the screen dropping resistor. However, the actual screen voltage always remains more positive than the small positive grid voltage swing. Thus grid dissipation because of low plate or screen voltage is minimized.

Consider now the effect of screen voltage on plate current, which mathematically follows a 3/2 power law as shown in the following table.

	PLATE CURRENT VALUE
MULTIPLYING FACTOR	(3/2)
.25	.125
.5	.35
.75	.65
1.0	1.0
1.25	1.4
1.5	1.64
1.75	2.3
2.	2.8

If the screen voltage exactly follows the power law, it is only necessary to vary the screen voltage to about 1.6 times normal to double the plate current. Likewise, it is only **necessary** to reduce the screen voltage to about 15 percent of normal to obtain practically zero plate current. It can be understood, then, why it is not necessary to drive the screen to zero and twice normal in order to drive the plate voltage and current to zero and twice normal. Thus it can be seen that the previous statements are not exactly true; however, since the tube does not exactly and always follow the 3/2 power law, it is not possible to make a more exact statement and be completely accurate. It is probably more accurate to say that the screen grid voltage is varied sufficiently to insure that the full plate current flow of twice normal is possible on the peaks of modulation when the plate voltage is increased twice normal. Under these conditions the requirement of a peak power of four times normal for full modulation is met, and the tube is used to its fullest capability.

Since the plate current does not vary linearly with screen voltage, it can be seen that varying the screen voltage linearly in accordance with modulation does not produce distortion-free plate components. That is, as long as the plate voltage and plate current do not vary exactly and linearly with the modulation, distortion exists. Thus the screen grid modulator inherently produces more distortion than the simple triode modulator produces, but with proper design this distortion is minimized to a low value. A comparison in this instance is the distortion products given with a simple triode audio stage as compared with pentode or beam tube audio stage. In every instance the distortion is greater, but the increased powerhandling capabilities and low grid drive requirement make it mandatory to use the triode only where the increase in distortion cannot be tolerated.

In considering the action at low screen and plate voltages, the type of tube becomes an important factor. A typical comparison of plate current variation with plate voltage for two different types of screen grid tubes, and for pentode and beam tubes, is shown in the accompanying graph. It is easy to see that the beam and pentode types of electron tubes have much less variation of plate current at low voltages than the screen grid type has. Thus, when a suppressor grid is not included, reduction of plate voltage below the screen voltage produces undesired secondary emission effects, and can even cause the plate current to go negative (reverse its direction of flow). Since on the troughs of modulation (the negative peak modulation excursions) the plate voltage was said to be reduced practically to zero, together with the screen voltage, it can be seen that some unwanted effects can occur.



Plate Current Comparisons

Consider first the beam and pentode tubes, since their action is similar. From the graph it is clear that the plate voltage can be reduced to about 10 to 15 volts before the current changes appreciably and

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suddenly drops off to zero. Thus it is possible to swing the plate voltage lower than the screen voltage without any unwanted effects. The plate current, however, does not change linearly with the plate voltage swing. Therefore, it is necessary to vary the screen voltage in order to change the plate current in accordance with the modulation, even though the plate voltage is varied. Because of secondary emission effects, it is clear from the graph that screen grid tubes (two different tubes are shown) cannot be used at low plate voltages. If they were used, extreme distortion would occur at low plate voltages, and, even though the screen voltage were varied likewise, a similar pattern would follow. Thus the screen grid tube cannot be operated with as low a plate swing as the pentode and beam tubes without excessive distortion. In considering the swing to practically zero voltage and current, it is evident that in most every case the swing is to a small minimum voltage rather than actual zero. Whether the minimum is very small or fairly large depends upon whether or not the tube is a beam-pentode or screen-grid type. It is also clear that because of the relatively high minimum plate voltage on a screen grid tube, less usable output is obtained than for a similar beam or pentode tube.

From a consideration of the small change of plate current with a large plate voltage swing, as shown in the preceding graph, it should also be clear that the screen-and-plate-modulated circuit functions primarily as a screen-modulated type of circuit with the plate voltage aiding. That is, while the' screen voltage changes the plate current, the corresponding change in plate voltage is in a direction which enhances the action. When the plate voltage is increasing, so is the screen voltage, and so is the plate current. Thus the problem of non-linearity on negative swings in the screen grid modulator is overcome because in the plate-and-screen-modulated circuit the plate voltage is reduced at the same time. Therefore, it is not necessary to swing the screen negative to get complete modulation.

# Failure Analysis.

**No Output.** Lack of output should **first** be isolated to failure of the r-f amplifier stage or the modulation signal circuit(s). Even though the modulator is operative, an open rfc or tank circuit, a shorted or gassy electron tube, or lack of grid excitation to the r-f amplifier will produce a no-carrier indication. Observation of the r-f plate current meter will deter-

mine whether the plate circuit has continuity, and tuning for a maximum indication with a resonant dip will determine whether sufficient drive, load, and the proper bias exist for operation without modulation. Grid-drive meter indications will also show whether the proper r-f drive exists. When the tank can be resonated for a minimum dip and then loaded to the maximum plate current with normal grid current, the trouble is in the modulator circuit.

Lack of grid drive places the trouble in the exciter stages of the transmitter or in the coupling network to the final stage. Lack of plate current indicates possible power supply trouble, an open-circuited r-f stage, an open screen-voltage dropping resistor (in some tube types a very small plate current may still flow), or a shorted screen bypass capacitor. In the choke-fed screen modulator, an open choke would remove screen voltage and prevent plate current flow. Otherwise, proper performance, but lack of ability to load to maximum plate current, indicates antenna trouble, improper tuning, or a defective transmission line.

With an r-f carrier existing, the trouble is definitely in the audio circuits or in the modulation transformer, rfc, and screen or plate bypass capacitor.

High transmitter plate current usually indicates short-circuited components, a lack of proper bias, or improper tuning, while low plate current indicates excessive bias, high-resistance joints, low tube emission, or possible lack of coupling to the load. When the above conditions are indicated by the equipment meters, a simple resistance analysis made with the power OFF and the high-voltage supply grounded for safety will quickly determine the defective component(s).

Low Output. Determine first whether the low output is from lack of sufficient audio drive or from an actual reduction in the percentage of modulation. Low modulation is usually caused by lack of sufficient audio output, but it can also occur from a reduced setting of the audio gain control or from trouble in the speech stages. An oscilloscope is very useful in determining the cause of malfunctioning, since the waveform itself may be directly observed. For simple, quick tests of modulation percentage, the trapezoidal waveform is useful. The envelope or waveform check, however, will show percentage of modulation and also indicate waveform distortion; thus it is usually more useful. Too high a control grid bias will cause a reduction of output and an inability

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to reach 100 percent modulation with the same drive. The grid bias can be checked simply with a voltmeter (connect an rfc in series with one of the prods). A reduced screen voltage is most likely of all to produce a low output, usually with overmodulation or distortion, since the plate and screen swing will be excessive. Such a condition can be caused by too heavy a screen current causing a large drop in the screen-voltage dropping resistor, by a defective resistor, or by a partially shorted bypass capacitor.

In the choke-fed screen circuit, a defective choke will prevent the obtaining of complete modulation and can also result in reduced output, as can a poorly soldered joint. Check the coil for the proper resistance with an ohmmeter. A partially shorted choke may give the proper indication when measured with a dc ohmmeter, but short across turns when operating. Such a condition will usually be indicated by audible noise or distortion when the signal is monitored.

Lack of sufficient **filament** emission can cause a flattening of the positive peaks, and inability to obtain 100 percent modulation. Lack of ability to reach 100 percent modulation at the high frequencies, while obtaining it at low and medium frequencies, would indicate a capacitive shunting by screen or plate bypass capacitors, provided the speech amplifier response is satisfactory.

**Distorted Output.** Distortion can occur from a number of causes, and is easy to detect when monitoring audio modulation. Overmodulation will cause a chopping off of the carrier (carrier shift), producing severe interference to stations operating near the transmitter frequency, and cause distortion.

In stages operating on the same input and output frequencies, there is always the possibility of sufficient feedback from plate to grid to cause selfoscillation, with severe distortion, particularly on the peaks of modulation. Although the low plate-grid capacitance (shielding effect) of the screen and pentode tubes makes this almost impossible, it will sometimes occur, especially at the higher frequencies, because of poor layout and external coupling between the tube elements. Such action can occur, particularly after part replacement and changed lead dress from a repair. Self-oscillation can usually be detected easily by its characteristic fuzzy oscilloscope pattern.

Lack of sufficient capacitance to supply the peak power requirements can occur through drying out of electrolytic **filter** capacitors, and cause peak flattening with its consequent distortion. Usually, however, such a condition will be indicated by hum on the carrier or in the modulation before the distortion is excessive enough to notice, unless an oscilloscope is used to monitor transmissions.

A similar condition caused by lack of sufficient emission in the r-f amplifier will cause peak flattening with noticeable distortion. This can sometimes be observed by noticing the lack of ability to respond to high modulation peaks and by a gradual decline in the plate current reading over a long period of time. Under normal conditions an r-f ammeter will indicate approximately a 22 percent increase in output current at 100 percent modulation.

#### SERIES MODULATOR (ELECTRON TUBE)

#### Application.

The series modulator is used to amplitude modulate a carrier (r-f) signal with an audio (or video) intelligence with a minimum of circuitry.

# Characteristics.

Uses two triodes connected in series.

- Has a wide bandpass.
- Is critical to adjust.

Used as either a high-level or low-level modulator. Inefficient in comparison to other methods of producing AM.

#### **Circuit Analysis.**

**General.** The series plate modulator is used in a-m transmitters where it is desired that the modulator stage pass a wide band of frequencies. Because of its inherent wideband characteristics and relatively good quality, the series modulator is employed primarily in television applications; however, because adjustments are critical, the series modulator has not been widely accepted for common usage. Basically, the circuit consists of a triode modulator and a Class C r-f amplifier connected in series using a common dc plate supply. The modulator triode may be connected in either the plate or cathode circuit of the r-f amplifier with operation remaining basically the same, regardless of which method is employed. Only the cathode connected circuit is discussed in detail.

**Circuit Operation.** A cathode connected series modulator is illustrated in the accompanying schematic diagram,



Series Modulator

Modulator tube V2 is biased Class A by cathode resistor R3. Capacitor C5 bypasses the cathode resistor to prevent degeneration and helps to maintain a constant bias voltage. Resistor R2 is the grid return resistor with C4 acting as a coupling and dc blocking capacitor.

R-f amplifier V1 is biased Class C by the series grid leak circuit comprised of RI and C3. Transformer T1 couples the r-f signal into the tuned grid tank formed by secondary winding L2 and capacitor C1. Capacitor C2 is the cathode bypass capacitor and prevents degeneration in the cathode and r-f from entering the audio circuits. C6 and L3 form a tuned plate tank (load) for V1, and L4 inductively couples the signal into the following stage.

When power is initially applied to the circuit no bias exists on either of the series connected triode tubes. As a result, plate current readily flows though the tubes to voltage source,  $E_{bb}$ . As the current flows through R3 and V2 voltage is developed across each component. The voltage dropped across R3 biases the modulator Class A so that any signal arriving on the grid will be faithfully reproduced in the plate circuit. The voltage dropped across the modulator tube, V2, protects the r-f amplifier in the event r-f drive is lost because of failure in the oscillator or multipliers. It

will be helpful to remember that placing a positive potential on the cathode has the same effect as placing an equally negative potential on the grid. For the following discussion assume that no audio modulation voltage is applied to the grid of V2 and plate voltage remains relatively stable.

R-f signals arriving from the oscillator (or multiplier) stage are impressed across Ll, the primary winding of T1. The signals are transformer coupled into the secondary tuned tank formed by inductor L2 and capacitor Cl. The grid tank is tuned to the desired r-f frequency by Cl which is variable over a short range.

On the positive excursions of the r-f signal the grid is driven positive. Grid current flows and C3 charges quickly. As the signal swings negative, grid current ceases to flow and C3 begins discharging through RI developing a negative voltage which is applied to the grid. Discharge time is much slower than charge time because of the large grid leak and consequently, the charge on C3 is not completely dissipated before the next positive excursion of the r-f signal. The cycle repeats itself and eventually, after a few more cycles, the voltage applied to the control grid stabilizes. Thus, the tube is now biased by the grid leak (signal) bias on the control grid in addition to the bias voltage applied to the cathode. The sum of the voltage applied to the cathode and control grid of V1 biases the tube Class C (below cutoff) so that only the positive peaks of the r-f input signal results in plate current flow; therefore, plate current is broken into pulses at the signal frequency. Capacitor C2 bypasses any r-f plate current variation in the cathode to ground and prevents degeneration effects. The parallel resonant tank formed by C6 and L3 oscillates (flywheel effect) every time a pulse of current flows \_ in the plate circuit. Hence, even though plate current flows in pulses, tank current flows for the entire cycle and a linear sine wave at the resonant frequency is transformer coupled into L4.

The preceding discussion describes the operation of the r-f amplifier with no modulation signal applied, and if operation was limited to this condition no intelligence could be transmitted. The following discussion concerns operation when modulating signals are applied.

A modulating signal from the finrd speech (or video) amplifier is r-c coupled through coupling capacitor C4 onto the grid of V2. R2 is the grid return resistor and provides a low impedance path for

dc return current. As the positive half-cycle of the modulating signal is applied to the grid, V2 bias is decreased and the cathode current through V2 increases. Consequently, V2 plate voltage decreases. Decreasing the plate voltage of V2 is the same as decreasing the plate voltage of V1 (since both tubes are in series) and, in effect, reduces the cathode bias from V1 to ground so that conduction in V1 is increased; this results in developing an increased output across the plate load (resonant tank). Conversely, when the modulating signal swings negative the opposite effect takes place, and the output across the plate load decreases.

Hence, in this application, the plate voltage decreases to nearly zero (with respect to the cathode) at maximum output, and increases to nearly the supply value, Ebb, at minimum output. Unlike other modulators, no voltage doubling takes place due to the absence of a reactive element (inductor) in the plate circuit. Instead, the circuit is initially adjusted so that full carrier output is obtained with half the supply voltage applied, so that swinging it from zero to the full supply value is the same as doubling the voltage in other types of modulators.

If the modulating signal is of sufficient amplitude to overdrive V1 into saturation, a loss of intelligence (clipping) results for the period of time the tube is in saturation. Hence, transmitters are usually equipped with a modulator gain control to insure that the modulating signal does not exceed design limitations. From basic theory it is known that when two signals are injected simultaneously into a non-linear device, new frequencies appear in the output. When the r-f and modulator signals are injected into V1, which is operated as a Class C (non-linear) r-f amplifier (whose output varies as the square of the applied plate voltage), two additional frequencies appear in the output; namely, the sum and difference frequencies. In transmitters these "new" frequencies are referred to as upper and lower sidebands and represent approximately 1/6 of the total power, per sideband with 2/3 of the power in the carrier. The sidebands contain the same modulation as the earner and in some transmitters, such as single-sideband (ssb) and double sideband (dsb), the sidebands are transmitted in preference to the carrier. However, in this instance the carrier and two sideband frequencies are selected

by the tuned tank and coupled into the output circuits by the transformer action of T2.

### Failure Analysis.

No Output. A loss of r-for audio signal will result in either a no output or unmodulated carrier condition. Use an oscilloscope equipped with a high impedance probe to check the r-f (across Ll) and audio (across input terminals) signrds. If either signal is absent the modulator will not function properly. and the absent signal must be secured before further troubleshooting is accomplished. Next, check each tube element on the base of the tube socket for correct operating voltages. Check the bias voltages carefully as an abnormal bias voltage may cause erroneous readings on the plate elements. If voltage are abnormal, use an ohmmeter to measure the dc resistance of R3, R1 and inductors L1, L2, and L3 also, use an in-circuit capacitor checker to check Cl, C2, C3 and C5 for a shorted or leaky condition.

Weak or Distorted Output. A weak or distorted output will be caused by: weak or distorted input signals; improper bias; improper power supply voltages; defective tubes; or improper tuning or loading of the grid or plate tank.

# DOUBLE SIDEBAND MODULATOR (ELECTRON TUBE)

#### Application.

Double sideband modulation is used in double sideband communication systems where upper and lower sideband are transmitted and the carrier frequency used to generate these sidebands is eliminated.

#### Characteristics.

Generates upper and lower sidebands at high power levels while suppressing the r-f carrier.

Utilizes two push-pull connected triodes operated class c.

Uses low level grid modulation.

Modulating signal is applied to the control grids in push-pull, while the r-f carrier is applied to the control grids in parallel.

Utilizes nonlinear characteristics of electron tubes to generate sidebands.

Even-order harmonics are cancelled through pushpull action.

#### Circuit Analysis.

General. Double sideband communications systems differ from conventional a-m systems and from single sideband systems in that both sidebands and no carrier is transmitted. It should be noted that carrier elimination is achieved in a specially designed power amplifier. The modulator is a conventional AM modulator. This discussion will pertain to the power amplifier, since the power amplifier is the ordy unit in the DSB transmitter which is significantly different from units in the conventional full carrier AM transmitter. Single sideband systems achieve the same result by transmitting only one sideband. Both DSB and SSB provide the advantage of eliminating "whistles" or beats caused by the beating of the earner with other carriers and sidebands in the receiver, since both DSB and SSB do not transmit a carrier. At first glance it may appear that a single sideband system makes more effective use of the available transmitter power, since the SSB transmitter concentrates all of the available transmitter power into one sideband while the DSB transmitter transmits two identical sidebands. However, this apparent gain of SSB over DSB is not realized at the receiver output, since double sideband signal voltages combine vectorially in the receiver detector and produce audio frequency voltage proportional to twice that produced by one sideband. For example, a double sideband r-f envelope containing 100 watts (50 watts in each sideband) produces the same receiver audio output as a 100 watt SSB r-f envelope (all 100 watts in the sideband). It has been reasoned that a double sideband system can provide results equal to or greater than that produced by a SSB system. In a conventional full carrier AM system the r-f carrier transmitted with the sidebands heterodynes with the sidebands in the receiver detector circuit and audio frequency voltages are produced. In the DSB system and in the SSB system no carrier is transmitted and an artificial carrier, generated in the receiver must be combined with the sideband, or sidebends in the case of DSB, to properly demodulate the signal. This artificial carrier frequency must be very stable and must be as close as possible to the frequency of the

earner used to generate the sidebands in the transmitter in order to keep distortion of intelligence to a minimum. One of the arguments in favor of DSB over SSB is the distortion caused by the phase shift inherent in SSB due to the loss of the opposing phase shift of the other sideband. This shift can be minimized by maintaining a sufficiently high level of carrier insertion at the receiver. This phase shift has little effect on voice transmissions but pulse and data transmissions may be seriously affected. In a DSB system the effects of this phase shift are greatly minimized since the phase shift of one sideband tends to oppose the phase shift of the other sideband. The DSB system, however, requires that the locally inserted carrier be of the same phase relationship as the originrd modulation at the transmitter. This is accomplished by the use of a phase-locked oscillator to generate the carrier to be reinserted in the receiver. Another advantage seen in DSB transmission over SSB is the possibility of greater reliability of reception under varying conditions of fading. Under such conditions one sideband may be phased out by multi-path fading while the other sideband may not be excessively attenuated. By definition, selective fading results when the various frequency components of a transmission are not received exactly as transmitted with respect to power levels and phase relationships. The adverse effects of this condition on full carrier AM is distortion of received intelligence, and decreased receiver output. It can then be said that SSB is not subject to selective fading since only one sideband is transmitted. However, if propagation conditions are such that the frequency of the sideband being transmitted is excessively attenuated the receiver output is likewise decreased, whereas a DSB system operating at the same frequency will probably maintain satisfactory communications since the other sideband will probably be unaffected. Another advantage of DSB over SSB is the simplicity of the DSB transmitter. To convert a conventional full carrier AM transmitter to a DSB suppressed carrier transmitter only the power amplifier must be modified. The modified DSB power amplifier closely resembles the balanced modulators used in SSB transmitters. The DSB power amplifier discussed here consists of two push-pull connected triodes operating class **C** with r-f carrier applied to the control grids of both tubes in parallel (in-phase), and the audio 🥧 modulating signal applied to the control grids in push-pull (180° out-of-phase). In push-pull amplifier

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## **ELECTRONIC CIRCUITS**

circuits a push-pull input is required to produce an output and an in-phase input cancels in the output. The r-f carrier and the audio modulation present simultaneously on the control grids of the tubes beat together, and four basic frequencies are present in the plate circuit of the modulator tubes. These frequencies are the original r-f carrier, the original audio modulation and sum-difference frequencies generated as a result of heterodyning. Heterodyning results when two or more frequencies are applied to any element of a non-linear resistance such as an electron tube or a transistor. If the reader desires detailed information on heterodyning he may find it in the introduction to chapter 13 of this Handbook. The r-f carrier frequency present in the plate circuit is canceled out by push-pull action in the output transformer (the r-f carrier is applied to the push-pull amplifier in parallel) and the output transformer presents a very low impedance to audio frequencies. Therefore, the original audio modulating signal is not developed in the output. The generated sidebands, which are a product of the in-phase r-f earner input and the out-of-phase audio modulation input are therefore, out-of-phase at the plates of the tubes and add in the output transformer, rather than cancel as in-phase signals do, and they are inductively coupled to the antenna circuit through the output transformer. The power amplifier described here uses two power triodes, however, the use of power tetrodes may be encountered.

**Circuit Operation. The** following schematic diagram illustrates a **final** power amplifier designed to suppress or elimimte the r-f carrier and produce a double sideband output.



**Double Sidebend Generator** 

Transformer T1 couples the audio modulation from the modulator to the grids of the power amplifier. Capacitor Cl places the centertap of T1 at a-f ground potential so that 180° out-of-phase audio voltages are developed across the top and bottom halves of the secondary of Tl, and are felt on the grids of power amplifier tubes VI and V2. Coupling capacitor C2 couples the r-f carrier from the preceding stages to the slider of carrier balance potentiometer Rl, which provides a means of varying the amplitude of the r-f carrier coupled to the grids of V1

and V2 with respect to each other. Capacitors C3 and C4 couple the r-f carrier from carrier balance potentiometer RI to the grids of V1 and V2, respectively. Power triodes V1 and V2 are the nonlinear devices used to generate upper and lower sidebands at high power levels. Resistor R2 which is shunted by inductor L1, and resistor R3 which is shunted by inductor L2 form parasitic suppressor networks intended to decrease the tendency for parasitic r-f oscillations to develop. Center-tapped transformer T2 serves as the push-pull output transformer for the power amplifier and capacitors C5 and C6 form a split-stator type of tank capacitor used to resonate T2 to the output frequency. Radio frequency choke RFC1 together with bypass capacitor C8 prevent r-f energy from entering the power supply. Tapped inductor L3, whose inductance can be varied by switch S1, together with variable capacitor C7 couple the transmitter output to a coaxial transmission line which transmits the sideband r-f energy to the antenna. Since triodes are used the circuit must be neutralized or the relatively high value of grid to plate capacitance of the triodes would provide a feedback path and the amplifier would break into self oscillations. Capacitor C9 and C10 couple r-f energy from the plate of one tube to'the grid of the other and cancel or "neutralize" the effects of grid to place capacitance and thus prevent self oscillations.

To more easily examine the operation of the DSB power amplifier assume first that only the r-f carrier is applied.

The r-f carrier is coupled from the preceding driver stage through coupling capacitor C2 to the slider of carrier balance potentiometer R1. The r-f carrier appears at both ends of RI and is coupled in-phase through capacitors C3 and C4 to the grids of VI and V2. The amplitude of the r-f carrier at the grid of each tube is controlled by the adjustment of half cycle, both plates draw an increasing amount of plate current (the input is in phase) and the voltage drop across each half of the tapped primary of the output transformer T2 is negative going, so that opposing voltages are developed in the transformer primary which cancel, and no output is produced. If the circuit is properly balanced by the adjustment of R1, these opposing signals are equal in amplitude and the carrier is effectively suppressed. Since the amplifier is operated with class C bias (approximately twice

cut-off) only the peaks of the positive half cycle of the r-f input have an effect on conduction. Neither tube conducts during the negative half cycle of r-f earner input and again no output is produced. Therefore, an output is not produced by the DSB power amplifier when only the r-f carrier is applied. When audio modulation is applied in addition to the r-f carrier, upper and lower sidebands are generated and are coupled through the output circuit to the antenna.

Audio modulation is applied to the primary of T1 and since the center tap of the secondary of T1 is placed at a-f ground potential by capacitor Cl, audio modulation signal voltages are developed across each half of the winding, which are 180° out-of-phase with each other. This modulation signal is applied directly to the grids of VI and V2. Capacitors C3 and C4 are of such a value that they present a high impedance to audio frequencies and, thus, prevent the out-of-phase audio modulation from crossing over from one grid to the other and canceling each other out. During the period when both tubes are driven into conduction by the positive half cycle of r-f carrier input, the audio modulation and the r-f carrier beat together, and sum and difference frequencies (sidebands) are generated as the result of heterodyning. Actually there are four basic frequencies present in the plate circuit of V1 and V2. There are the original r-f carrier, the original audio modulating signal, and the upper and the lower sideband. Other higher order harmonics are also present but are of little consequence. Of the frequencies present only the sidebands are developed in the output circuit since the r-f carrier cancels in the push-pull output transformer, as explained previously. The audio modulating frequency is not developed because of the low value of impedance offered by the r-f output transformer. The sideband frequencies, being a product of the out-ofphase modulating signal, are developed across the primary of the output transformer and are inductively coupled through the secondary of T2 to the output circuit. The even order harmonics present in the plate circuit are cancelled through push-pull action and the odd order harmonics are shunted around the primary of T2 to ground by capacitors C5 and C6. The sidebands are coupled through inductor L3, whose inductance can be varied by switch S1, and variable capacitor C7 to the coaxial transmission line. L3, S1, and C7 match the impedance of the power

amplifier output to the impedance of the coaxial line so that maximum power is transferred to the antema and minimum power is reflected.

## Failure Analysis.

No Output. Dangerous high voltages are present in the power amplifier and all applicable safety precautions should be taken when working with the power amplifier. Since each branch of the power amplifier performs essentially the same function, failure of one branch is not likely to cause a no-output condition to exist. Failure of the power supplies or failure of the input or output circuits are likely causes of output. If the power amplifier is at fault, make resistance checks with the equipment deenergized, and pay particular attention to the resistances measured from the plates to ground; since components having high voltages applied to them are more likely to breakdown and short than components having lower voltages applied to them. Capacitors C5, C6 and C8 would short the high voltage to ground if they broke down, and capacitors C9 and C1O would short the high voltage supply to the bias supply if either capacitor broke down. Capacitor Cl would short the bias supply to ground if it failed. Transformer T2, inductors L1 or L2 or RFC1 could become shorted to ground. This would also short the HV power supply to ground as well as a possible shorted tube. Insulation breakdown on any of the wires carrying high voltage could also be the cause of a shorted power supply.

If the no-output condition does not manifest itself in the form of blown H.V. fuses, lack of high voltage at the plates of V1 and V2 could be the trouble. Observing all applicable safety precautions, measure the plate voltage of the power amplifiers with the transmitter keyed. If there is no plate voltage on either tube, the power supply is defective or RFC1 is open. If proper plate voltage is applied but there is no output, failure of either the r-f carrier, or modulation, to reach the grids of V1 and V2 could be the cause of no output, since the DSB power amplifier, like the SSB balanced modulator, produces an output only when both inputs are present simultaneously at the grids. Presence of these signals can easily be determined by observing, with an oscilloscope, the waveform present at the grids of V1 and V2. If either input signal is missing, signal trace from the grids of VI and V2 to the preceding stage to determine the defective component. Failure of T1 is a likely cause for no modulation drive to V1 and V2. Resistance

checks of transformer windings and leakage checks to ground should reveal any defects that may exist in T1. Failure of R1, or an open C2, could prevent the r-f carrier from reaching the grids of V1 and V2, hence, no output would result. Failure of output transformer T2 could also result in a **no-output** condition. Resistance checks of transformer windings and checks for leakage to ground, and leakage between windings should reveal any defects existing in T2.

Low Output. A low output condition can be caused by defective tubes, improper power supply voltages, low amplitude inputs, or improper tuning of the output circuit. Observe all applicable safety precautions and check the high voltage applied to the plates of the power amplifier. Also check the bias voltage applied to the grids **V1** and V2. If the tubes are good and the power supply voltages are correct, low output **could** be caused by insufficient r-f carrier, or modulation drive applied to the power amplifier. This condition can be checked by observing with an oscilloscope, the amplitude of the r-f carrier and the modulating signal on the grids of VI and V2. If either input signal is weak on the grids of VI and V2, check the amplitude of that signal at the point where it enters the power amplifier, in order to determine whether the defect exists in the power amplifier, or in the preceding stages. A defect in T1 such as a partially shorted winding or excessive leakage to ground could result in a decreased amplitude modulating signal on the grids of VI and V2, and a partial failure of C2 or R1 could result in decreased amplitude r-f carrier on the grids of V1 and V2. Both situations could result in a low output. Likewise, if one of the input signals is unable to reach the grid of either V1 or V2 that branch of the power amplifier would be inoperative, since both modulating signal and r-f carrier must be present at the grid simultaneously to produce an output, and low output would result. If C3 or C4 opened, or RI opened, the r-f carrier would not be coupled to the grid of either V1 and V2. Likewise, a similar situation would arise if either the top or bottom half of the tapped secondary of T1 become shorted. In this case the audio modulation signal would not be coupled to the grid of one of the tubes and low output could, again, result. Another possible cause of low output is a defect in the parasitic suppressors networks L1-R2 and L2-R3. If the resistor in either network opened, a decreased output could result since much of the

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sideband voltage would be dropped across the inductor shunting the open resistor.

**Distortad Output.** A distorted output condition may be caused by defective tubes, improper power supply voltages, excessive input drive, or a distorted input. Check the power supply voltages taking care to observe **all** safety precautions, and make any required adjustments, if necessary. If the output is still distorted it would be wise at this point to observe, with an oscilloscope, the amplitude and waveshape of the input signals. It should be noted that if the input signals are excessive or distorted the fault lies in the stages preceding the power amplifier.

# PART 12-2. SINGLE SIDEBAND

## SINGLE SIDEBAND MODULATION (SSB)

#### General

An amplitude modulated r-f signal can be separated into three different frequencies. They are, the carrier frequency, the upper sideband frequency (USB) and the lower sideband frequency (LSB). A 100-percent modulated A-M signal utilizes two thirds of its total power in the carrier. The following diagram illustrates the frequency versus power relationships of a fully modulated AM envelope.

100% Modulated A-M Signal (100 Watt Carrier Power)

An understanding of the principles of Amplitude Modulation is essential to the understanding of SSB modulation since SSB is basically a form of AM. A brief review of the principles of amplitude modulation as discussed earlier in this Section of the Handbook will greatly facilitate the understanding of SSB modulation for the reader who is not thoroughly familiar with A-M.

Since only the AM sidebands carry all of the intelligence (modulation) the carrier can be eliminated, and the available transmitter power utilized to a much greater advantage. Both upper and lower sidebands are **identical** in waveform except for a difference in frequency. Therefore if one of the sidebands along with the carrier is suppressed or eliminated leaving only a single sideband, an even greater efficiency may be obtained.

**Normally**, an effective 6 dB power gain can be obtained from a r-f power amplifier, capable of dissipating say 400 watts of peak power, by using SSB instead of conventional DSB AM. For comparison purposes we shall use a 100 watt rated carrier power AM signal and a 400 watt peak envelope power (abbreviated PEP) SSB signal. Note that the 100-watt rated carrier A-M signal also dissipates 400 watts on audio peaks when fully modulated as shown in the following illustration.



100% Modulated AM Envelope

As can be seen from the illustration, the peak to peak voltage of a fully modulated A-M envelope is twice that of the unmodulated carrier. Peak power is four times carrier power, since  $P = E^2/R$ .

The following illustration compares a fully modulated 100 watt rated carrier power envelope to a 400 watt PEP single sideband envelope for a single sustained tone.



Comparison of A-M and SSB Modulation Envelopes

Note that while the peak power ratings of both signals are identical, the conventional AM modulated signal only reaches full peak power at the instant of 100 percent modulation. On the other hand, the single-sideband signal operates constantly at full peak power. Assuming that the AM envelope consists of a 100 kHz carrier modulated by a 1 kHz audio tone, an upper sideband at 101 kHz and a lower sideband at 99 kHz are produced, rdong with the 100 kHz basic carrier in the r-f envelope. Thus, the average sideband power is only 50 watts (25 watts in each sideband). On the other hand the 400 watt single sideband r-f envelope is either the upper sideband or the lower sideband (depending upon which sideband is selected to be transmitted), and there is no carrier frequency present. Hence all 400 watts of PEP is usable power. Consequently, there is an apparent 8-fold (9 dB) increase in usable power of SSB over conventional DSB AM. Actually this only amounts to a 6 dB gain m useful power, since a conventional DSB AM signal containing 50 watts of total sideband power produces twice the receiver output that a 50 watt PEP SSB signal produces. This is because the upper and lower sidebands of the DSB AM signal combine in the receiver detector circuit, and produce an audio voltage which is proportional to double the amplitude of each sideband. The loss of one sideband reduces the apparent 9 dB gain of the SSB transmission over conventional AM to an actual 6 dB advantage.

Up to this point we have only discussed the power advantages gained through the use of single sideband in the transmitting system. Another important advantage realized through the use of SSB is that of frequency spectrum conservation. For good intelligibility modulating frequencies up to 3 kHz are

required for voice transmissions. A conventional DSB AM contains the carrier frequency and sideband frequencies deviating 3 kHz on both sides of the carrier frequency, when the carrier frequency is modulated by a 3 kHz tone. Thus the total bandwidth of this signal is 6 kHz. With the same modulating frequency the bandwidth of the SSB system is only 3 kHz, since only one sideband is transmitted. It is apparent that a SSB system will provide twice the number of channels of a comparable conventional DSB A-M system. Still another advantage of SSB operation is reduced receiver noise, since the required bandwidth of the receiver is halved due to the reduced bandwidth of the transmitted signal. Since noise power is directly proportional to bandwidth, a 3 dB gain in signal-to-noise ratio results because of the increased selectivity. From the above discussion, it can be seen that the SSB system provides an effective 9 dB overall improvement (6 dB in the transmitter, and 3 dB in the receiver) over the conventional DSB AM system. The power comparison between SSB and AM stated previously is also based on ideal propagation conditions. Over long distance transmission paths, AM is subject to selective fading, which causes severe distortion and sometimes a weaker received signal. Only the A-M transmission is subject to this type of deterioration under poor propagation conditions, because the upper sideband, the lower sideband, and the carrier must both be received exactly as transmitted to realize full fidelity, and the full theoretical power from the signal. If one, or both, of the transmitted sidebands is attenuated more than the carrier, a loss of received signal results. The most serious and most common result is selective fading which occurs when the carrier is attenuated more than the sidebands. The effect of this type of selective fading is severe distortion of the received intelligence. Selective fading can also cause a phase shift between the relative phase positions of the carrier and sidebands. This condition also results in distortion of intelligence. On the other hand, a SSB sigral is not subject to selective fading, which varies the amplitude or phase relationship between the sidebands and the carrier, since only one sideband and no carrier is transmitted.

The following block diagram illustrates a simple SSB transmitter arrangement.



Single Conversion SSB Transmitter

The audio amplifier stage increases the speech input voltage to a level sufficient to drive the SSB modulator. An extremely stable r-f signal is provided for use in generating the desired r-f sidebands by the carrier oscillator. The SSB modulator generates both upper and lower sidebands when both audio modulation and r-f carrier are applied simulatenously. The sideband falter stage passes the selected sideband and rejects the undesired sideband. The frequency multiplier stage multiplies the r-f carrier generated in the carrier oscillator to a higher frequency for use in the high frequency mixer stage, where this multiplied frequency heterodynes with the sideband frequency from the sideband falter, and produces the desired transmitter output frequency. The linear power amplifier stage is used to amplify the signal from the HF mixer stage to a power level suitable for transmission. Since very stable oscillators and very sharp falters are much easier to produce for low frequency applications, SSB generation is made to occur at relatively low radio frequencies. The generated sideband frequency is brought to the desired high r-f output frequency by frequency conversion. Although the simple single sideband transmitter discussed above uses single conversion for ease of understanding, it is normal practice to use double conversion to obtain the desired high frequency output.

The single sideband modulator is used to generate amplitude modulated upper and lower sidebands, meanwhile suppressing or canceling the r-f carrier which was used to generate the sidebands. By beating the audio modulation against the unused carrier frequency, sum and difference frequencies are produced to provide the actual sideband frequencies. It is also important to note that the carrier frequency does not appear in the output of the modulator because circuit elements are arranged to produce this effect. All types of single sideband modulators such as the balanced modulator, the balanced-bridge rectifiertype modulator, and the product modulator produce the same end result. They differ, however, in the manner in which they achieve carrier suppression and generate sidebands. Each of these circuits is discussed in detail in the following paragraphs.

# BALANCED (PUSH-PULL CARRIER INPUT) MODULATOR (ELECTRON TUBE)

#### Application.

**The** balanced (push-pull carrier input) modulator is used to produce amplitude modulated upper and lower sidebands for use in single sideband transmitters.

## Characteristics.

Operates class C with push-push output.

Both r-f carrier and audio modulation are applied to the modulator in push-pull.

Generates upper and lower sidebands while suppressing the r-f carrier.

Utilizes two tetrodes with their plates connected in parallel.

MODULATORS

## Circuit Analysis.

General. While all modulators have the characteristic of producing sidebands the balanced modulator is unique in that it produces only upper and lower sidebands and suppresses, or cancels the r-f carrier in the output. Different types of balanced modulators differ in the manner in which they achieve carrier suppression. This discussion concerns the manner in which the balanced (push-pull carrier input) modulator achieves carrier suppression. The balanced modulator discussed here utilizes two tetrodes with their plates connected in parallel, and operated class C. The r-f carrier is applied to the modulator control grids in push-pull (out of phase) while the modulating signal is applied to the screen grids in push-pull, also out of phase. The r-f carrier signal is cancelled in the output tank circuit and upper and lower sidebands are generated. It is important to consider that carrier suppression occurs in the output tank circuit and not in the plate circuit. The parallel-plate comected modulator tubes are operated with Class C bias, and conduct only on positive-going input signrds. Since the r-f carrier input is applied to the modulator control grids push pull, the modulator tubes conduct and produce an r-f output on alternate half cycles of the r-f input. Since ordy one tube is conducting at a given instant, the r-f pulses appearing in the plate circuit of each tube are not affected by the other tube. In the tank circuit, however, the r-f pulses occur at a rate which tends to cancel rather than reinforce tank circuit oscillations. The generated sidebands do not cancel in the output, since the output tank is resonant to only the carrier frequency. The audio modulation signal is not developed in the output due to the low impedance presented to audio frequencies by the r-f output transformer. This discussion concerns the use of tetrodes in the push-pull carrier input balanced modulator. Triodes or pentodes may be used in place of tetrodes, the need being determined by system requirements.

**Circuit Operation. The** following schematic diagram illustrates a typical balanced (push-pull carrier input) modulator.



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#### Push-Pull Carrier Input 8alanced Modulator

Transformer T1 couples the r-f carrier signal from the carrier oscillator to the control grids of balanced modulators V1 and V2. Secondary L2 of T1 is effectively centertapped by RI and capacitors Cl and C2. Resistor R1 also permits fixed bias insertion for V1 and V2, and serves as a bias decoupling resistor. Potentiometer R2 provides a means for electrically balancing the circuit by varying the cathode resistance of V1 and V2. V1 and V2 are the nonlinear devices used to generate the upper and lower sidebands. Transformer T2 couples the audio modulation to the screen grids of V1 and V2. The secondary of T2 is center-tapped to forma push-pull screen circuit so that the induced audio frequency voltages will be 180 degrees out of phase at the screen grids of the modulator tubes. The audio frequencies do not appear in the output since the output transformer, T3, presents a low impedance to audio frequencies.

Capacitors C3 and C4 are screen grid r-f bypass capacitors preventing r-f from entering the screen supply. Resistor R3 is a screen voltage dropping resistor intended to keep screen voltage always lower than the plate voltage, so that the negative resistance effects inherent in the tetrode are not encountered. Transformer T3 serves as the tuned output transformer. The primary L5 of T3 together with capacitor C5 form a parallel resonant tank circuit which is sharply tuned to the carrier frequency.

To more easily understand the operation of the balanced (push-pull carrier input) modulator assume first that only the r-f carrier is **applied**. Assume that the first half cycle of r-f carrier drives the grid of V1 positive and the grid of V2 negative. Since V2 is cutoff due to class C bias, the negative signal on the grid of V2 has no effect on V2. On VI, however, the positive half cycle of r-f drives the tube into conduction and a negative going r-f signal appears in the plate circuit. Capacitor C5 charges during the period of increasing plate current. When plate current starts to decrease C5 discharges building a magnetic field around L5. When plate current ceases the magnetic field around L5 would normally collapse and charge C5 in the opposite direction. This is normal tank circuit oscillation sometimes called, "flywheel action".

At this time, however, the next half cycle of r-f input drives V2 into conduction and a negative going r-f pulse appears in the plate circuit. Capacitor C5 charges and prevents the magnetic field around L5 from collapsing. When plate current starts to decrease C5 discharges and maintains constant current through L5. With constant current through L5 the magnetic field around L5 remain unchanged, and an output is not inductively coupled to the following stages. In effect, the r-f output pulse from V2 cancels the r-f output pulse from V1. The amplitude of these pulses should be approximately equal, considering the losses in the tank circuit, for the r-f carrier signal to be effectively canceled. The relative amplitude of the r-f carrier pulses can be varied by the adjustment of potentiometer R2.

Under actual operating conditions with both the r-f carrier and the audio modulation applied, upper and lower sidebands are produced through the beating of the r-f carrier and the audio modulating signal in the non-linearly operated modulator tubes. It is important to note that the sideband frequencies, unlike the carrier frequency, are not canceled in the output tank circuit. This is because the output tank circuit is sharply tuned to the carrier frequency and the side-band frequencies will deviate sufficiently from the carrier frequency for the output tank circuit to appear non-resonant to these frequencies. Hence no sideband energy will be stored in the tank circuit from one half cycle of r-f input to the next and cancellation of the sidebands will not occur.

## Failure Analysis.

No Output. Failure of one of the modulator tubes is not likely to cause a no-output condition to exist. Failure of the power supply or a circuit component common to both branches of the balanced modulator is a much more likely cause of no output. Voltage checks of VI and V2 with a voltmeter would reveal a defective component that could be the cause of no output. Power supply voltages should be checked and adjusted if necessary. Any discrepancies found during voltage checks can be followed up, with the equipment deenergized, with resistance checks of associated circuit components to reverd the component at fault. Since both r-f carrier and modulation inputs are required to produce a sideband output, lack of either signal could be a cause of no output. Presence of these input signals can be readily determined with an oscilloscope. The r-f carrier should be present on the control grids of both tubes and should have sufficient amplitude to drive the tubes above cutoff. If the r-f carrier is not present on the grids of the modulator tubes, check for presence of the r-f carrier on the primary of T1. If no signal is present on the primary of T1 the fault likely lies in the stage, or stages, preceding the balanced modulator. If a signal is present on the primary of T1 but absent on the control grids of VI and V2 the fault likely lies in transformer T1. If the audio modulating signal is not present on the screen grids of the modulating tubes, check for presence of the modulation signal on the primary of T2. If modulation is present on the primary of T2 but absent on the screen grids of V1 and V2, transformer T2 is defective. If the modulation signal is absent at the primary of T2 the fault likely lies in the preceding stages.

Low Output. A common cause of low output is decreased emission of the modulator tubes. The power supply voltages should be checked and corrected if necessary. Voltage checks of V1 and V2 would reveal if a defective circuit component is the cause of low output. Should a discrepancy be found during voltage checks a resistive analysis of circuit components would reveal the component at fault. Another possible cause of low output could be decreased amplitude r-f carrier input or decreased amplitude modulation input. The existance of this condition can be determined by observing with an oscilloscope the amplitude of the r-f carrier signal on the control grids, and the amplitude of the modulating signal on the screen grids of V1 and V2.

Distorted Output. Distortion of intelligence in SSB systems will occur if the transmitter and receiver are not exactly on frequency. Distortion in SSB transmitter is usually caused by improper operation of the linear power amplifier or by operating any stage in the transmitter beyond its capabilities. If the balanced modulator is determined to be the cause of distortion a possible cause could be defective tubes. Check the power supply voltages with a voltmeter. If the tubes are good and the power supply voltages are correct, a resistive analysis of circuit components with the equipment deenergized would reveal a component failure that could be a cause of distorted output. Do not overlook the possibility that the audio modulation is distorted before it reaches the balanced modulator. The existance of this condition can be determined by observing, with an oscilloscope, the quality of the modulation signal on the screen grids of V1 and V2 with an audio tone from an audio signal generator applied to the transmitter.

# BALANCED (PARALLEL CARRIER INPUT) MODULATOR (ELECTRON TUBE)

#### Application

The parallel carrier input balanced modulator is used to produce amplitude modulated upper and lower sideband frequencies for use in suppressedcarrier, single sideband transmitters, commonly abbreviated as SSSC.

## Characteristics.

Utilizes nonlinear characteristics of electron tubes to produce sidebands.

Produces amplitude modulated upper and lower sidebands while suppressing the r-f carrier.

No output is produced unless both r-f carrier and modulation are present.

Modulation is accomplished at low power levels, therefore, no large modulator power supply and transformers are needed. Uses push-pull output and parallel input to cancel out the carrier.

Can provide conversion gain, i.e., sideband output greater than modulation input.

## Circuit Analysis.

General. The parallel carrier-input balanced modulator produces amplitude modulated sidebands and suppresses the r-f carrier. This is achieved by coupling the r-f carrier, in-phase, to the grids of two tubes whose output is connected in push pull (out-ofphase). The r-f carrier signal voltage is kept 8 to 10 times as large as the modulating voltage to keep distortion to a minimum. In push pull amplifiers an input signal inserted in-phase on the grids (in parallel) will cancel in the output. The modulating signal is applied in series to the grids of the balanced modulator through a transformer. This transformer is effectively centertapped by a resistance network connected across the secondary winding for bias insertion. The center tap arrangement produces a 180-degree phase different between the audio modulation signal voltages on the grids of the modulating tubes. When both r-f carrier and modulating audio signal are applied to the grids of the balanced modulators, sum and difference frequencies (side-band) are produced by the modulating frequencies beating against the carrier, since any amplitude modulation process is essentially the same as heterodyning. As in a frequency converter, any modulation which exists on one of the mixing frequencies is linearly transposed to the resultant sum and difference frequencies. The plate circuit contains the upper and lower sidebands, which are the sum and difference frequencies, respectively, the r-f carrier, and the audio modulation. The carrier is cancelled out by push-pull action in the output transformer and the output transformer also presents a low impedance to the audio modulating signal. Therefore, the original modulating signal is not developed in the output. The generated sidebands are out-ofphase with each other at the plates of the tubes, since the modulating signal is out-of-phase at the grids. These out of phase signals add in the output rather than cancel as in-phase signals do, and they are inductively coupled to the following stages through the output transformer. Tetrodes and pentodes may be used with equal or greater effectiveness, their use being determined by system requirements.

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**Circuit Operation. The** accompanying diagram illustrates a typical parallel carrier-input balanced modulator.



Parallel Carrier Input Balanced Modulator

Transformer T1 couples the audio modulation to the grids of balanced modulator tubes VI and V2. Resistors R1 and R2 provide grid bias and an effective centertap for T1. Capacitor Cl couples the r-f carrier from the carrier oscillator to carrier balance potentiometer R3. Carrier balance potentiometer R3 is adjusted to vary the relative amplitude of the carrier signrd on the grids of V1 and V2, so that the circuit may be completely balanced and the carrier suppressed in the output. Capacitors C2 and C3 couple the r-f carrier from balance potentiometer R3 to the grids of V1 and V2. Modulator tubes V1 and V2 are the nonlinear devices used for developing the modulation. Resistor R4, which is bypassed by C4, provides cathode bias for both tubes. Center-tapped plate transformer T2 provides a push-pull plate load

for the modulators. Capacitors C5 and C6 bypass any higher order harmonics that might be generated in the plate circuit to ground. Resistor R5 is a plate voltage dropping resistor, while C7 bypasses any unwanted signals to ground, and places the center tape of T2 at ground potential.

The operation of the parallel carrier-input balanced modulator can be more easily examined by first applying only the r-f carrier. The r-f carrier generated in the carrier oscillator is coupled through Cl to the slider of variable resistor R3. Thus the carrier signal appears at both ends of R3 and is coupled through C2 and C3 to the grids of V1 and V2. The carrier signal voltage is inserted in-phase on the grids of V1 and V2, and the amplitude, at each tube is controlled by adjusting R3. Assuming that the r-f input is operating on the positive half-cycle, both plates draw an increasing plate current (the grid input is in-phase), and the voltage drop across each half of the transformer winding is negative going, so that equal and opposing voltages are developed in the transformer primary which cancel, and no output is obtained from the secondary. Likewise, on the negative half-cycle less plate current is drawn and the drop across the transformer is positive going, and equal and opposing voltages are developed in the primary and also cancel out, so no carrier again is produced. If the circuit is properly balanced by the adjustment of R3, these opposing signals are equal in amplitude and the carrier is effectively suppressed.

The amount of carrier suppression obtained depends upon the degree of balance between the two legs of the balanced modulator circuit. When two tubes of the same type are used in a balanced modulator circuit (without any balancing adjustment), carrier suppression of 10 to 15 dB generally results. Since carrier suppression of at least 35 dB is usually required in suppressed-carrier, single-sideband systems, it can be seen that some type of fine balancing adjustment is required. In this circuit R3 is used for carrier brdancing, but other methods (such as varying the bias or plate voltage on the modulator tubes) may be encountered in other circuits.

When audio modulation also is applied, a different situation arises. The audio modulation is applied through transformer T1. Since the secondary of T1 is effectively center tapped by resistors RI and R2 modulation signal voltages will be developed across each half of the winding which are out of phase with each other. This modulating signal is applied directly

to the grids of V1 and V2. Capacitors C2 and C3 are of such a value that they present a high impedance to audio frequencies and prevent any audio modulation from crossing over, from one grid to the other, and canceling each other out. The audio modulating signal modulates the r-f carrier and produces upper and lower sidebands in the plate circuit of the modulator tubes. These sidebands are produced by mixing the r-f carrier frequency and the modulation signal across a nonlinear device. To illustrate the operation of the parallel carrier-input balanced modulator with both r-f carrier and modulating signal applied assume that the first half cycle of the modulating voltage applied to the grid of V1 is positive and the first half cycle of the modulating signal applied to the grid of V2 is negative. It can readily be seen that conduction of V1 will increase with negative going sideband frequencies being generated across the top half of the output transformer. At the same time, the negative half cycle of audio modulation applied to the grid of V2 decreases conduction of V2, causing positive going sideband frequencies to be developed across the bottom half of the output transformer. Push pull action thus occurs and the sideband frequencies add to each other, causing both upper and lower sidebands to be developed and inductively coupled to the secondary of T2. The r-f carrier is suppressed, as explained earlier, and the original audio modulating signal is not developed due to the low reactance of T2 to the basic audio modulation frequencies. Therefore, only the upper and lower amplitude modulated sidebands are produced by the balanced modulator.

#### Failure Analysis.

No Output. Since both modulator tubes perform the same function it is unlikely that failure of one tube or associated circuit would cause a no-output condition. A much more likely cause of no output would be failure of something common to both tubes such as the power supply, the cathode resistor or the circuits associated with the r-f carrier input or modulation input. Voltage checks on V1 and V2 with a voltmeter would reveal a defective component that could cause no output. Should all the voltages check good the cause of no output could be the lack of either r-f carrier or modulating signal. This can be easily checked with an oscilloscope. Check the grids for presence of both signals with the carrier oscillator operating and modulation applied. If the modulating signal is not present on the grids, check for presence

of the modulation signal on the primary of **T1**. This will determine whether T1 or the preceding audio stages are at fault. Should the r-f carrier be missing check the output of the carrier oscillator. If there is an output from the carrier oscillator, signal trace the components linking the carrier oscillator to the grids of the **modulator** tubes. Should all the conditions necessary for proper operation by met, i.e. proper voltages on the tube elements, proper carrier and modulation inputs, and there is still no output, transformer T2 could be defective. Check all windings of T2 for proper resistance and check all windings for leakage to ground.

Low Output. Low output can be caused by a defective tube or tubes, improper power supply voltages or by a defective circuit component. Low output could also be caused by decreased amplitude of the r-f carrier signal voltage or possibly by decreased amplitude of the modulating signal. Check the power supply voltages. If the power supply voltages are good, voltage checks of the tube elements would reveal whether or not a defective circuit component was the cause of low output. Should these voltage checks reveal a discrepancy, resistance checks, with the circuit deenergized, would reveal the component at fault. The possibility of decreased amplitude r-f carrier signal or modulating signal input can be checked by observing these signals on an oscilloscope. If all the conditions necessary for proper operation are met, i.e., good tubes, proper power supply voltages, and good circuit components, poor operation could be the result of a defective output transformer. Since the resistance of the output transformers windings are relatively low a shorted winding could easily be overlooked when making resistance checks. Check the resistance of each half of the primary winding, each half should be equal, and check the resistance of the secondary winding. With the centertap disconnected check the windings for leakage to ground.

**Distorted Output. It** should be noted that distortion of intelligence will occur if the single sideband transmitter and receiver are not exactly on frequency. Distortion in single sideband transmitters is frequently caused by improper operation of the linear amplifiers, or by operating any stage beyond its capabilities. If system distortion is determined to be caused by the brdanced modulator a likely cause could be improper voltages applied to the tubes, or defective tube or tubes, or failure of some circuit

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component. Check the power supply voltages, if they are good, voltage checks of the tube elements would indicate whether or not a defective circuit component is the cause of distorted output. Incorrect voltages found to be present on the tube elements can be traced to the component at fault with resistance checks of associated circuit components. The possibility of a distorted audio input or possibly a distorted r-f carrier should not be overlooked. The existance of these conditions can be determined by observing these signals on an oscilloscope.

# BALANCED (PARALLEL CARRIER INPUT) MO OULATOR (SEMICONDUCTOR)

#### Application.

**The** semiconductor basic balanced modulator is used to produce amplitude modulated upper and lower sideband frequencies for use in single sideband transmitters.

## Characteristics.

**Same** characteristics as electron tube version, except it uses semiconductors instead of electron tubes.

## Circuit Analysis.

General. The basic balanced modulator produces amplitude modulated upper and lower sidebands and suppresses the r-f carrier. This is achieved by coupling the r-f carrier, in-phase, to the bases of two transistors whose output is connected in push-pull, (out of phase). The r-f carrier is kept 8 to 10 times as large as the modulating voltage to keep distortion to a minimum. In push-pull amplifiers an input signal must be out of phase to produce an output since any in-phase inputs cancel in the output. The modulating signal is applied to the base of each transistor in push-pull (180 degrees out of phase) through a center tapped transformer. When both r-f carrier and audio modulating signals are applied simultaneously to the bases of the balanced modulators, sum and difference frequencies (sidebands) are produced by the modulating frequencies beating against the carrier, since any amplitude modulation process is essentially the same as heterodyning. As in a frequency converter, any modulation which exists on one of the mixing frequencies is linearly transposed to the resultant sum and difference frequencies. The collector circuit

contains the upper and lower sidebands which are the sum and difference frequencies, respectively, the r-f carrier, and the audio modulation. The carrier is cancelled out by push-pull action in the output transformer, and the output transformer also presents a low impedance to the audio modulating signal. Therefore, the original modulating signal also is not developed in the output. The generated sidebands are out-of-phase with each other at the collectors of the transistors, since the modulating signal is out of phase at the bases. These out-of-phase signals add in the output transformer rather than cancel as in-phase signals do, and they are inductively coupled to the following stages through the output transformer.

Circuit Operation. The accompanying diagram illustrates a basic semiconductor brdanced modulator.



## 8esic 8alanced Modulator (Common Emitter).

Audio transformer T1 couples the audio modulation to the bases of transistors Q1 and Q2. Resistors R1 and R2 form a base bias voltage divider which provides the proper bias for the transistor. Capacitor Cl places the center tap of **T1** at a-f ground potential to supply an out-of-phase (push-pull) input. Capacitor C2 couples the r-f carrier from the carrier oscillator to the slider of carrier balance potentiometer R3. Potentiometer R3 can be adjusted, to vary the relative amplitude of the r-f carrier signal voltage on the bases of Q1 and Q2, to provide a carrier balance control, so that the r-f carrier can be completely suppressed in the output. Capacitors C3 and C4 couple the r-f carrier from balance potentiometer R3 to the bases of Q1 and Q2, and also act as dc bias blocking capacitors to prevent base shorting. Transistors Q1 and Q2 are the nonlinear devices used for generating the sidebands. Resistor R4, which is bypassed by C5 is a conventional emitter stabilization resistor intended to prevent changes in temperature from altering transistor characteristics. Center-tapped output transformer T2 provides a push-pull collector load for the modulators. Capacitor C6 places the center-tap of the primary of T2 at **r-f** ground potential.

To more easily examine the operation of the basic balanced modulator, assume first that only the r-f carrier is applied. The r-f carrier generated in the carrier oscillator is coupled through C2 to the slider of potentiometer R3. Hence, the carrier signal appears at both ends of R3 and is coupled through capacitors C3 and C4 to the bases of Q1 and Q2, respectively. The carrier signal voltage is in-phase on the bases of Q1 and Q2 (they are parallel connected) and the amplitude of the carrier signal at the base of each transistor is controlled by the adjustment of R3. Assuming that the r-f input is operating on the negative half cycle, the negative forward base bias is increased and both collectors draw an increasing amount of collector current, (the base input is in phase). Thus, the voltage drop produced across each half of output transformer T2 is positive-going, and equal but opposing voltages are developed in each half of the transformer primary by current flowing in opposite directions which cancel, so that no output is obtained from the secondary winding. Likewise, on the positive half cycle of r-f input the forward bias is reduced and less collector current is drawn. Thus, the drop across transformer T2 primary windings is negative going and equal and opposing voltages are developed in the primary because the current flow through each primary is opposite. These voltages also cancel out (since they are out-of-phase) so no carrier again is developed in the output. If the circuit is properly balanced by the adjustment of R3, the opposing signals are exactly equal in amplitude and the carrier is completely suppressed. Thus, it can be seen that an output is not produced with only an r-f carrier input applied.

When audio modulation and the r-f carrier are both applied simultaneously, a different situation arises. The audio modulation is applied through transformer T1. Since the secondary of T1 is effectively center-tapped by Cl, R2, and the bias supply, modulation signal voltages are developed across each half of the secondary winding of T1 which are out of phase with each other. The out-of-phase modulating signals are applied directly to the base of each transistor. Capacitors C3 and C4 are of such a value that they present a high reactive impedance to audio frequencies and thus prevent any audio modulation "from feeding back from one base to the other and canceling each other out. Meanwhile, the audio modulating signal modulates the inserted r-f carrier and produces upper and lower sidebands in the collector circuit of transistors Q1 and Q2. These sidebands are produced by mixing the r-f carrier frequency and the modulation signal together across a nonlinear device. (Detailed information concerning frequency conversion, (mixing or heterodyning), can be found in the introduction to the Mixers and Heterodynes Section of this Handbook. To better illustrate the operation of the basic balanced modulator with both r-f carrier and modulation applied, assume that the first half cycle of the modulating signal voltage applied to the base of Ql is positive and the first half cycle of the modulating signal applied to the base of Q2 is negative.

The conduction of Q1 decreases as a result of the positive half cycle of modulation input opposing the forward bias of the emitter base junction. This results in negative going sideband frequencies being developed across the top half of the output transformer. At the same instant the conduction of Q2 increases as a result of the negative going half cycle of modulation input aiding the forward bias of the emitter base junction, and causing positive-going sideband voltages to be developed across the bottom half of the output transformer T2. Push-pull action occurs and the side band frequency signal voltages add to each other causing both upper and lower sidebands to be developed and inductively coupled to the secondary of T2. The r-f carrier is suppressed, as explained earlier, and the original audio modulating signal is not developed due to the low reactance of T2 to audio frequencies. Therefore, only the upper and lower sidebands are produced by the balanced modulator.

#### Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of multiplier resistance employed on the low-voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also be observe proper polarity when

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checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. Since each leg of the basic balanced modulator performs essentially the same function, failure of one leg of the balanced modulator is not likely to cause a no-output condition to exist, unless the failure occurred in a manner that would affect the power supply such as a shorted transistor or a shorted C6. Failure of the power supply itself is a likely cause of no output. If the power supply measures normal when checked separately and no collector voltage appears on Q1 or Q2, check T2 primary and C6 for a short or ground. An open or shorted R1 or R2 or a shorted Cl would remove the bias from transistors Q1 and Q2 and could also cause a no-output condition to exist. Since R4 is a common emitter resistor for both transistors a no-output condition would also result if R4 opened. Check for proper value with an ohmmeter. Since any balanced modulator produces an output only when both the r-f carrier and the modulating signal are present, absence of either of these signals on the base of each transistor would cause the **balanced** modulator to be inoperative. Presence of the input signals can readily be determined by observing, with an oscilloscope, the waveform present at these points with the carrier oscillator operating and with modulation applied to the transmitter. Absence of the audio modulation on the bases of the transistors could be caused by a defective audio input transformer, T1, or by failure of the audio stages preceding the balanced modulator. Presence of audio modulation on the primary of T1 indicates that the preceding audio stages are functioning properly. Should the modulation be present on the primary of T1 but absent on the bases of the transistors, T1 is most likely defective (check the primary and secondary for continuity with an ohmmeter). Presence of the r-f carrier at the input to coupling capacitor C2 indicates that the carrier oscillator is operating. In the event that the r-f carrier is present at the input of C2 but is absent on the bases the transistors, capacitor C2 or potentiometer R3 may be open. Check R3 for proper vahre and C2 for value with an in-circuit capacity meter. Failure of C3 or C4 would only disable one leg of the balanced modulator and an output would still result. Signal tracing from C2 to the bases of the transistors will reveal which component is at fault. Another possible cause of no output is a defect in output transformer

T2. Continuity checks of the transformer windings and checks for leakage between the primary and secondary and between each winding and ground w-ill reveal whether or not a defect exists in the transformer.

Low Output. A low output condition could be caused by a defective transistor, a faulty circuit component, a defective power supply, or by low amplitude r-f carrier or modulation input. Voltage checks should be made of the power supply voltage and of transistor elements to determine whether or not a defective power supply or a faulty component is the cause of low output. A change in value of resistors R1 or R2 or leakage in capacitor Cl would change the base bias of transistors Q1 and Q2 and could cause a low output condition. If C5 opens the resulting degeneration would lower the gain of the modulator circuits and could cause low output to result. Likewise, an increase in value of emitter stabilization resistor R4 would alter the operating bias of the transistors and could cause a decreased output. Check the value of R4 with an ohmmeter. The amplitude of the inputs to the balanced modulator can be checked by observing with an oscilloscope the waveform present at the base of each transistor. If either input signal is low in amplitude, the cause can be determined by signal tracing from the bases of the transistors to the stages preceding the balanced modulator. If either C3 or C4 opens, one leg of the balanced modulator would be inoperative and low output would result. Do not overlook the possibility that a defective output transformer can also cause low output. Check the resistance to ground with an ohmmeter.

Distorted Output. Distortion of intelligence will result in SSB systems if the receiver and transmitter are not exactly on frequency. Distortion in SSB transmitters is usually the result of improper operation of the linear power amplifier or of operating any stage beyond its capabilities. Should the distortion be determined to be caused by the balanced modulator, check the modulation level to make sure that the audio circuits are not overdriving the balanced modulator. If the modulation level is correct, distortion could still be caused by a defective transistor. If the transistors are determined to be good and distortion persists, voltage checks of transistor elements with a high resistance voltmeter would reveal whether or not a defective component or a defective power supply is the cause of distortion. Low amplitude r-f

modulator.

carrier input could also cause distortion. The r-f carrier input should be 8 to 10 times the amplitude of the modulating signal.

# BALANCED COMPLEMENTARY SYMMETRY MODULATOR (SEMICONDUCTOR)

# Application.

**The** balanced complementary symmetry modulator is used in single sideband transmitters to produce amplitude modulated upper and lower sidebands.

#### Characteristics.

Produces amplitude modulated upper and lower sidebands while suppressing the r-f carrier.

Utilizes a PNP and an NPN transistor connected in a complementary symmetry circuit.

Requires two collector power supplies (one positive and one negative supply).

Static current does not flow through the output transformer.

Utilizes the common collector configuration.

Requires two separate bias supplies.

## Circuit Analysis.

General. The balanced complementary symmetry modulator produces amplitude modulated upper and lower side-bands and suppresses or cancels the r-f carrier, which is used to generate the sidebands. Basically this is achieved by coupling the audio modulation in parallel (in-phase) to the bases of two opposite polarity (PNP and NPN) transistors connected in a complementary symmetry configuration, and simultaneously coupling the r-f carrier in push pull (180° out-of-phase) to the bases of the transistors. It should be noted that, while the transistors are of opposite polarities, they have the same-operational characteristics. The audio modulation and the r-f carrier beat together in the nonlinear resistance of the transistors, and sum and difference (sideband) frequencies are produced. The sideband frequencies are developed across the output transformer and are inductively coupled to the following stages. Circuit elements are arranged so that the r-f carrier and the original audio modulating signal do not appear in the output. For minimum distortion the r-f carrier is maintained at a level 8 to 10 times greater than the audio modulating signal.

 $R^{2}$   $R^{2$ 

Circuit Operation. The accompanying diagram

illustrates a balanced complementary symmetry

# Balanced Complementary Symmetry Modulator (Common Collector Configuration)

Audio transformer T1 couples the audio modulation from the preceding stages to the bases of Q1 and Q2 through bias resistors RI and R3. RI and R2 form a voltage divider network to bias transistor Q1 and resistors R3 and R4 form a voltage divider to bias transistor Q2. Transformer T2 couples the r-f carrier from the carrier oscillator to both sides of carrier balance potentiometer R5. Carrier balance potentiometer R5, which has its slider grounded, effectively centertaps the secondary of carrier input tramformer T2, causing 180° out-of-phase r-f carrier signal voltages to be present at the top and bottom of T2. Coupling capacitors Cl and C2 couple the r-f carrier from transformer T2 to the base of each transistor and prevent a dc path from being formed from the base of each transistor to ground through carrier balance potentiometer R5. Transistors Q1 and O2 are the nonlinear devices used to generate the sidebands, and transformer T3 serves as the output load for the balanced complementary symmetry modulator.

Since both transistors have the same operational characteristics both transistors conduct equally with no signal input, and thus both transistors have equal

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equivalent emitter-collector resistance. Thus, it can be seen that a balanced condition exists between Q1 and Q2, and the voltage drop across Q1 is equal to the voltage drop across Q2. Since the absolute value of voltage between each power supply and ground is the same and the voltage drop across the transistors is equal, there is no voltage between point A in the figure and ground, and thus no current flows through output transformer T3, and no output is produced.

When a push-pull, (180° out-of-phase) input a signal is applied, in this case the r-f carrier, the following takes place. During the period of the input cycle when the base of Q1 is driven positive and the base of Q2 is driven negative conduction of both Q1 and Q2 decreases. This is due to a reduction in forward bias applied to each transistor (PNP transistor Q1 normally has its base biased more negative than its emitter and NPN transistor Q2 normally has it base biased more positive than its emitter). This decrease in conduction of Q1 and Q2 is in effect an increase in equivalent emitter-collector resistance and, since both transistors have the same operational characteristics, both transistors decrease conduction in equal amounts. Although the equivalent emitter-collector resistance of both transistors increases, it increases equally in both transistors and, therefore, the voltage drop across Q1 remains equal to the voltage drop across Q2. Once again the balanced condition between O1 and Q2 is maintained and no output is produced, since no current flows through output transformer T3. During the next half-cycle of r-f carrier input a negative-going half-cycle of r-f is coupled from transformer T2 to the base of Q1 and increases the forward bias on Q1 causing the conduction of Q1 to increase. Simultaneously, a positive half-cycle of r-f is applied to the base of Q2, where it again increases the forward bias on Q2, causing the conduction of Q2 to increase. Both transistors increase conduction at the same rate, and the equivalent emitter-collector resistance of both transistors decreases equally. Again the voltage drop across each transistor is equal and a balanced state is maintained. Hence no output is produced. In this manner the r-f can-ier is effectively suppressed in the complementary symmetry balanced modulator. In actual practice, the slight differences in characteristic found between evenly matched pairs of transistors necessitates the use of some external method of balancing the circuit. The complementary symmetry balanced modulator achieves precise carrier balance by making it possible to vary the amplitude

of the r-f carrier coupled to the base of Q1 with respect to the amplitude of the r-f carrier coupled to the base of Q2. This is achieved by effectively centertapping the secondary of r-f carrier input transformer T2 by connecting both sides of potentiometer R5 across the secondary of T2. Varying the position of the grounded slider of R5 has the same effect as varying the position of the center-tap on a centertapped transformer.

When audio modulation in addition to the r-f carrier is applied simultaneously to the balanced modulator, upper and lower sidebands are generated as the result of the r-f carrier frequency and the audio modulating frequency beating together in the nonlinearly operated transistors. Four basic frequencies are present in the emitter circuit of the transistors. These frequencies are the original r-f carrier frequency, the original audio modulating frequency and the sum and difference frequencies (sidebands) resulting from heterodyning action. However, only the sideband frequencies are present in the output.

The audio modulation is applied to the base of each transistor in parallel (in phase) through transformer T1. During the positive half-cycle of modulation input the forward bias on Q1 is opposed by the modulating signal (Ql is a PNP transistor) and conduction of Q1 decreases. At the same time, the positive half-cycle of modulating signal aids the forward bias on Q2 (Q2 is an NPN transistor) and conduction of Q2 increases. The balance between Q1 and Q2 is now upset since the equivalent emittercollector resistance of Q1 increased causing an increased voltage drop across Ql, while the equivalent emitter collector resistance of Q2 decreased causing a decreased voltage drop across Q2. Point A in the figure is no longer at ground potential but at some positive voltage and current flows through output transformer T3 causing an output to be produced. The r-f carrier component of emitter current is cancelled as explained previously. The sideband component of emitter current and the original audio modulation component of emitter current flows through the primary of output transformer T3, but the output transformer presents a very low impedance to audio frequencies, therefore, audio frequency voltage is not developed across the primary of T3. Only the upper and lower sideband signal voltage is developed across the primary of output transformer T3 and is inductively coupled to the following stages. Overall circuit operation is the same

for the negative half cycle of audio modulation input. That is, during the negative half-cycle of modulation input the forward bias on Ql is increased and conduction of Q1 increases. At the same time, the negative half-cycle of modulation signal decreases the forward bias on Q2 (an NPN transistor) and decreases conduction of Q2. The balance between Q1 and Q2 is now upset because the equivalent emitter-collector resistance of Ql decreased, causing a decreased voltage' drop across Ql, while the equivalent resistance of Q2 increased causing an increased voltage drop across Q2. Point A in the figure, is therefore, no longer at ground potential, but is at some negative voltage so that current flows through output transformer T3, causing an output to be produced. The r-f carrier component of emitter current is cancelled as explained previously. Although both the sideband component of emitter current and the original modulation component of emitter current both flow in the primary of T3, the low impedance offered to the audio modulation is insufficient to develop an audio frequency voltage across it. Therefore, only the upper and lower sidebands are inductively coupled to produce an output in the secondary of T3.

## Failure Analysis.

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**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low vrdues of multiplier resistance employed on the low voltage range of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false **low** resistance reading.

No **Output.** Since transistor Q1 and its associated circuit performs essentially the same function as transistor Q2 and its associated circuit components, failure of either transistor or associated circuit components is not likely to cause a no-output condition to exist. Likewise, failure of either the positive or negative power supply is not likely to cause a no-output condition to exist, since each power supply serves only one branch of the modulator. Failure of a component, such as the audio modulation input transformer T1, the r-f carrier input transformer T2, or output transformer T3 all of which serve both branches of the modulator could be a cause of a no-output condition. Continuity checks of the transformer windings and resistance checks for shorts to ground or excessive

leakage between windings will reveal a defect in either Tl, T2, or T3 which could cause a no-output condition to exist. Failure of T1 or T2 could cause a no-output condition to exist by failing to couple either the audio modulation or the r-f carrier to the balanced modulator. Likewise, failure of the source of the signals (modulating signal or r-f carrier) would also create a no-output condition. To determine whether or not the signals are reaching the brdanced modulator observe, with an oscilloscope, the waveform present on the primary of audio input transformer Tl, and the waveform present on the primary of r-f carrier input transformer T2. Absence of either of these signals results in a no-output condition and indicates that the fault lies in the stage, or stages preceding the modulator.

Low Output. Failure of almost any component in the complementary symmetry balanced modulator could result in a decreased output. Failure of, or improper output from either power supply could result in low output and the power supplies should be checked and repaired or adjusted, if necessary, before any component substitutions are attempted. Deterioration of either of the transistors could also be a cause of decreased output. A low output condition could also be due to improper base bias applied to either transistor. Check the voltage present on the base of Q1 and Q2 with a vacuum tube voltmeter. If a discrepancy is found the most likely cause is a change in value of voltage divider resistors RI and R2 (for the base of Ql) or R3 and R4 (for the base of Q2). Improper base bias could also be caused by a short in coupling capacitor C 1 or C2. If Cl or C2 opened, a low output condition would result since the r-f carrier would be unable to reach the base of either Q1 or Q2. A partial failure of transformers T1 or T2 could result in decreased amplitude audio modulation, or decreased amplitude r-f carrier, reaching the bases of the transistors. This condition would likely result in decreased output. Careful resistance and leakage checks, with an ohmmeter, would usually indicate a partial failure that could be the cause of low output. Likewise, decreased amplitude r-f carrier or audio modulation before it reaches the modulator could be the cause of low output. The existence of this condition can be determined by observing, with an oscilloscope, the amplitude of the input signals on the primary of the respective input transformer. Another possible cause of low output could be due to a defect in output transformer T3. Resistance and leakage

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checks of the transformer windings should indicate a possible defect.

Distorted Output. Distortion of intelligence will occur in single sideband systems when the transmitter and receiver are not exactly on frequency. Distortion in single sideband transmitters is usually the result of improper operation of the linear power amplifier, or of operating any stage beyond its rated capabilities. If system distortion is determined to be caused by the modulator, almost any component which could cause low output can rdso be suspected of causing a distorted output. The power supply voltages should be checked first and adjusted, if necessary. A check of base bias voltage of both transistors would reveal if a fault exists in voltage divider resistors RI, R2, R3, and R4. An open or shorted carrier balance potentiometer R5 could also cause a distorted output to result. Since the r-f carrier input amplitude should, for good fidelity, be 8 to 10 times the amplitude of the audio modulating signal, a decrease in amplitude of the r-f carrier or excessive audio input could be the cause of distorted output. The amplitude of the r-f carrier input and the amplitude of the audio modulation input can be easily checked by observing, with an oscilloscope, the waveform present at the primary of the respective input transformer. Do not overlook the possibility that the audio modulating signal is distorted before it reaches the modulator.

# BALANCED BRIDGE MODULATOR (ELECTRON TUBE)

## Application.

**The** balanced bridge modulator is used in single sideband generators to produce amplitude modulated upper and lower sidebands while suppressing the r-f carrier.

## Characteristics.

Produces upper and lower sidebands while suppressing the r-f carrier.

Utilizes four diodes connected in a bridge configuration.

Produces sidebands by heterodyning action produced by nonlinear diodes.

Requires both an r-f carrier and modulation applied simultaneously to produce an output.

## Circuit Analysis.

General. The purpose of the balanced bridge balanced modulator is to produce amplitude modulated upper and lower sidebands and suppress the r-f carrier. Basically this is achieved in the balanced bridge modulator by arranging the circuit elements so that a balanced condition exists between the two legs of the bridge when only an r-f carrier is applied. This balanced condition will prevent an r-f output from being produced. Modulation is applied so that the bridge becomes unbalanced, that is, more current flows through one leg than the other. This causes current to flow through the output transformer, and an output is produced. The current flowing through the output transformer is the upper and lower sidebands generated by the heterodyning of the r-f carrier and modulating signal within the non-linear diodes.

Carrier suppression is achieved because the current through one leg represents the carrier and sideband currents plus the modulating signal current, while current through the other leg consists of only the carrier current. The overall effect is to cancel the r-f carrier currents. The audio frequency component is blocked from the output by capacitors whose reactance is high to audio frequencies. Only the sidebands are present in the output.

**Circuit Operation.** The accompanying diagram illustrates a typical balanced bridge modulator utilizing electron tube diodes.



**Balanced Bridge Modulator** 

Transformer T1 couples the modulation signal to the balanced bridge, and Transformer T2 couples the r-f carrier from the carrier oscillator to the balanced bridge. Diodes V1, V2, V3, and V4, form the balanced bridge. Capacitors C1 and C2 block audio frequencies, thereby preventing the primary of T3 from shunting the secondary of T2. This is necessary since T3 is an r-f transformer and would present a very low impedance to audio frequencies. Transformer T3 serves as an output transformer. Designations at points A, B, C, and D are used only to illustrate circuit operation.

To more easily analyze the operation of the balanced bridge modulator, assume first that only the r-f carrier is applied. Assume that during the first half-cycle of r-f, point A is positive with respect to point C. This back biases the diodes and no current flows, hence no output results, since the bridge appears as an open circuit.

When the negative half-cycle appears point A becomes negative with respect to point C. This forward biases the diodes and current flows from point A through V1 and V2 to point C. An equal current will flow from point A through V4 and V3 to point C. When the current through leg V1, V2 is equal to the current through leg V4, V3, a state of balance exists and no current will flow through winding L5 of the output transformer, T3. The following **illustration** shows the equivalent circuit of the bridge in a balanced state.



## Equivalent Circuit of Balanced Bridge Modulator With Only r-f Carrier Applied

The resistances represent the plate resistance of the diodes. Since the diodes are all of the same type and have the same characteristics, their conduction and plate resistances are the same. Resistor RL represents the load presented by the output transformer. There is no difference in potential between points B and D, and no current flows through the output transformer. Thus there is no output from the

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balanced bridge modulator when only the r-f carrier is applied.

When only the modulation signal is applied, circuit operation is as follows. Assume first that a positive half-cycle of modulating voltage is applied; causing point B to be more positive than point D. It can be seen that the instantaneous potential created by the positive half-cycle of modulation signal will cause current to flow from point D through V3 to point C. Since the plate of V2 is connected to point C, current will not flow through V2. Current will, however, flow from point C through the secondary, L4, of T2 to point A, and through VI to point B. Current also will not flow through V4 since V4 like V2 is back-biased to current flow in this direction. The return path for current flow is through secondary L2, of T1. The primary, L5, of T3 does not effect the modulation signal since Cl and C2 offer a high impedance to the relatively low modulating frequency and prevent any shunting effects of L5 on L2. When the polarity of the modulating signal reverses, current flows from point B through V2 to point C. From point C current flows through the secondary, L4, of T2 to point a and then through V4 to point D. The return path is through the secondary, L2, of T1.

Under actual operating conditions with both r-f carrier and signal applied, the balance between the upper and lower legs of the bridge caused by the equal r-f carrier currents through each leg is disrupted by the modulating signal and a sideband output results.

To examine the circuit under actual operating conditions, consider first that r-f carrier current is flowing in equal amounts through the upper and lower legs, V1 and V2, and V4 and V3 respectively. When a positive going cycle of audio modulating signal is applied to T1, modulation signal current flows from point D through V3 to secondary L4 of T2 and to point A, and then through V1 to point B and back to secondary L2 of T1. Since the diode is a nonlinear device, mixing, or heterodyning, takes place between the r-f carrier currents and the modulating signal currents flowing through V1 and V3, and both upper and lower sidebands are produced. These sideband currents follow the same path as the modulating signal except that they flow through the output transformer T3 instead of the secondary L2 of T1. This is because transformer T1 offers a high impedance to the relatively high sideband frequencies. The sidebands are inductively coupled through T3 to the following stages. The overall effect is the same for a negative half-cycle of modulation except that sideband current flow is through V2 and V4 and the flow is through the output transformer in the opposite direction.

## Failure Analysis.

No Output. A no-output condition could be caused by an open or shorted winding on any of the three transformers. With the equipment de-energized, a resistance check of the transformer windings will indicate an open or partially shorted winding. Failure of one of the diodes will not be likely to cause nooutput, however if the diode filaments are connected in series an open fdament could cause the other diodes to be inoperative. A visual check with the equipment energized will reveal whether or not any fdament failures occur. Since a balanced modulator does not produce an output unless both r-f carrier and modulation signals are present, lack of either of these signals could be a cause of no output. Presence of these signals can be determined with an oscilloscope. To check for the presence of the modulating signal, observe the waveform present at points B and D. If the modulating signal is not present at these points check for modulating signal on L1 the primary of T1. If the modulating signal is present here, but is absent at points B and D the fault most likely lies in transformer T1. If there is **no** signal present on the primary of T1 the trouble is likely to be in the preceding stages. The presence of the r-f carrier can be determined in the same manner by observing the waveform present at points A and C. If the r-f carrier is not present at A and C the trouble can be localized by signal tracing with an oscilloscope through T2.

Low Output. A common cause of low output can be from decreased emission of one or more of the diodes. If any tubes are replaced it would be good procedure to check all the tubes on a tube checker and use only tubes which have approximately the same emission. This is particularly advisable if a high degree of balance is desired within the bridge of diodes. If the tubes are good, another possible cause of low output could be insufficient modulation input or insufficient r-f carrier input. This .condition can be checked by observing the amplitude of the waveforms present at the modulation inputs to the bridge, and at the r-f carrier inputs to the bridge. If one of the inputs are low the cause can be determined by signal tracing with an oscilloscope and noting any excessive

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attenuation through the input transformers. If the amplitude of either signal is proper on the primary of the respective input transformer but low on the secondary, the transformer is defective. If the amplitude of the input signal is low on the primary of the respective input transformer the trouble likely lies in the stages preceding the balanced modulator.

**Distorted Output.** Distortion could be caused by **a** defective tube. Another cause of distortion might be a low r-f carrier input. The r-f carrier should be 8 to 10 times the amplitude of the modulating signal for distortion to be at a minimum. Do not overlook the possibility that the modulation input is distorted before it reaches the balanced modulator. Analysis of the modulation input with an oscilloscope would reveal if this condition existed.

## **PRODUCT MODULATOR (ELECTRON TUBE)**

### Application.

**The** product modulator is used in single-sideband transmitters to produce amplitude modulated upper and lower sidebands while suppressing the r-f carrier.

#### Characteristics.

The output of a product modulator is proportional to the product of the amplitudes of the input signals.

Does not require input transformers.

Utilizes three triodes with two of them operated as cathode followers.

Operates with class A bias.

## Circuit Analysis.

'General. The product modulator in single sideband applications produces amplitude modulated upper and lower sidebands while suppressing, or canceling the r-f carrier. The single sideband product modulator utilizes three triodes with two of them operated as cathode followers. It is interesting to note that all three triodes have a common cathode resistor. The r-f carrier and the audio modulation are impressed on the grids of cathode followers, and r-f carrier and audio modulation are developed across the common cathode resistor. Since the modulator tube also uses the same cathode resistor, audio modulation and r-f carrier signal voltage appear on the cathode of the modulator tube. The r-f carrier and audio modulation beat together in the modulator tube and upper and lower sidebands are generated. Carrier sup-

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pression is achieved by coupling the r-f carrier signal developed at the plate of VI to the plate of V3. Since there is 180° phase difference between the r-f carrier signrd developed at the plate of V1 and at the plate of V3, the r-f carrier is effectively canceled. The product modulator when used in single sideband applications produces a sideband output only when both the r-f carrier and the audio modulator are applied simultaneously. The use of cathode followers eliminates the need for r-f carrier and audio modulation input transformers, since the cathode followers provide the necessary impedance match between the r-f carrier oscillator and the product modulator, and also between the audio amplifying circuits and the product modulator. The cathode followers also provide isolation between the r-f carrier oscillator and the audio circuits. By eliminating the carrier suppression provision the product modulator can also be used as a low distortion A-M modulator.

The following circuit diagram illustrates a typical product modulator for use in single sideband systems.



**Product Moduletor** 

**Circuit Operation. Capacitor CI couples the audio** modulation to the grid of V2 and capacitor **C2** couples the r-f carrier to the grid of V1. Resistor R1 and R3 are grid resistor for V1 and V2, respectively. Capacitor C3 couples the r-f carrier signal voltage from the plate of V1 to the plate of V3 for the purpose of carrier cancellation. Resistor **R2** and R4 are plate dropping resistors and load for VI and V2, respectively. Resistor R5 is a common cathode resistor for all three tubes and potentiometer R6 provides a carrier balance control by varying the fixed bias on V3. VI and V2 which serve as cathode followers couple the r-f carrier input and the audio modulation input to the cathode of V3 which serves as the modulator tube. Inductor L1 is the plate load for V3, and C4 capacitively couples the generated sidebands to the following stages.

To more easily examine the operation of the single sideband product modulator, first assume that only the r-f carrier is applied to the modulator.

During the positive half cycle of r-f carrier input the conduction of VI increase and the voltage drop across plate resistor R2 increase causing a negative going r-f carrier pulse to appear at the plate of V1, and the voltage drop across common cathode resistor R5 increases, causing a positive going r-f carrier pulse to appear at the cathode of V1. Since the cathode of V3 is directly connected to the cathode of VI, the positive r-f pulse appears on the cathode of V3 and decreases the conductor of V3 causing a positive going r-f pulse to appear at the plate of V3. The negative r-f pulse on the plate of VI, is coupled through capacitor C3 to the plate of V3. If the r-f pukes from V1 are equal in amplitude to the r-f pulses from V3 there will be complete cancellation, and the r-f carrier will not appear in the output. The relative amplitude of these r-f pulses may be varied by the adjustment of R6 which varies the gain of V3. The positive half cycle of r-f input was used only to illustrate circuit operation. Circuit operation is the same for a negative half cycle of r-f input.

Thus with only the r-f carrier applied there will be no output from the product modulator.

When audio modulation is applied in addition to the r-f carrier upper and lower sidebands are generated. Audio modulation is coupled through coupling capacitor Cl to the grid of cathode follower V2. Audio frequency voltage are developed across common cathode resistor R5 and are directly coupled to the cathode of V3. The r-f carrier and audio modulation beat together in V3 and four basic frequencies appear in the plate circuit of V3. These frequencies are the original audio modulation, the original r-f carrier, and newly generated sum and difference frequencies. The r-f carrier frequency present in the plate circuit of V3 will be canceled by the 180° outof-phase r-f carrier signal coupled to V3 from VI, as explained in the previous paragraph. The audio modulator present in the plate circuit of V3 is not developed in the output since inductor L1 presents a low impedance to audio frequencies. The generated sideband frequencies, referred to earlier as sum and difference frequencies are developed across inductor L1 and capacitively coupled through C4 to the following stages.

### Failure Analysis.

No Output. Failure of almost any component could be a cause of no output in the product modulator. Check the power supply voltages to make certain that a defective power supply is not the cause of no-output. Voltage checks of tube elements will reveal if a component failure is the cause of no-output. Any discrepancies found during voltage checks can be followed up, with the equipment de-energized, by a resistive analysis of circuit components to reveal the component at fault. It should be noted that the product modulator will produce an output only when both r-f carrier and audio modulation are present on the cathode of V3. Presence of the r-f carrier and the audio modulation can be determined by observing the waveform with an oscilloscope on the cathode of V3 with modulation applied to the transmitter and the carrier oscillator operating. If either signal is missing the trouble can be localized by signal tracing from the signal source, either the carrier oscillator, or the audio amplifying circuits, to the cathode of V3.

Low Output. A likely cause of low output in the product modulator is decreased emission of the electron tubes. If proper operation is not restored, a defective circuit component could be the cause of low output. A resistive analysis of circuit components with the equipment de-energized would reveal a defective component that could be the cause of low output.

Another possible cause of low output is decreased amplitude r-f carrier input or decreased amplitude audio modulation input. The existence of this condition can be readily determined by observing the amplitude of the r-f carrier signal and audio modulation present on the cathode of V3, with an oscilloscope.

**Distorted Output. It** should be noted that distortion will occur in SSB systems if the transmitter and receiver are not exactly on frequency. Distortion in SSB transmitters usually results from improper d

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operation of the linear power amplifiers or by operating any stage beyond its capabilities.

If the modulator is determined to be the cause of distortion a likely cause of distortion would be defective tubes or a defective circuit component. The tubes can easily checked by exchanging them with tubes known to be good. Resistance checks of circuit components would reveal if a defective circuit component is the cause of distorted output. Power supply voltages should be checked and adjusted if necessary to make certain that a defective power supply is not the cause of distorted output. Don't overlook the possibility that the audio modulation may be distorted before it reaches the product modulator. To check for this condition, observe with an oscilloscope the quality of the audio modulation present on the grid of V2, with an audio tone from an audio signal generator applied to the modulation input of the transmitter.

## PART 12-3. FM



#### General.

In frequency modulation, an audio signal is used to shift the frequency of an oscillator at an audio rate. The rate at which the oscillator changes its frequency depends upon the frequency of the modulating signal, and the deviation (the amount that the frequency shifts from the center frequency) depends upon the amplitude of the modulating signal, as shown in the following illustration.



## **Frequency Modulation Waveforms**

The frequency of the carrier is called the center frequency. When this carrier is modulated by a positive signal, its frequency changes; for example, it may become higher in frequency, proportional to the

amount that the signal goes positive. Conversely, when the signal goes negative, the frequency becomes lower. Thus, when the sine wave shown in part A of the illustration is applied to a carrier, shown in part B, the carrier frequency changes from the normal center frequency to higher frequency, back to normal, to a lower frequency, and back to normal again as shown in part C. This variation is in direct accordance with the polarity and amplitude of the voltage of the sine wave. The maximum frequency change from center frequency, which depends upon the amplitude of the signal, is called the deviation. Note, in part C of the figure, that the amplitude of the modulated carrier is constant. As a result, frequency modulation is not so susceptible to static as in amplitude modulation, and it is for this reason that it is used for highquality transmission of sound, such as for music.

Since random noise usually consists of higher frequencies, the signal-to-noise ratio at the higher frequencies may be lower. It is for this reason that the audio modulation is coupled through a pre-emphasis network before being applied to the modulator circuit. The **pre-emphasis** network increases the relative signal strength of the higher frequency components of the audio signrd, and thereby compensates for any decrease in signal-to-noise ratio as caused by random high frequency noise. This creates a state of unbalance between the amplitudes of the high and low frequency components, but it is compensated for in the receiver by the use of a de-emphasis circuit, which performs the opposite function of pre-emphasis.

The primary difference between f-m and a-m is that the amplitude of the f-m signal is constant, while a-m depends upon amplitude variations for the transmission of intelligence.

The advantage of this type of modulation over a-m is its noise reducing capabilities. Most noise signals produce amplitude modulation of the carrier, or the carrier-plus-modulation signal, which is applied to the demodulating circuit in the receiver. If the receiver is responsive to amplitude variations, as in a-m receivers, this random noise is detected and amplified. If the receiver is responsive only to changes in frequency, as in f-m receivers, frequency modulation makes possible a considerable increase in the signal-to-noise ratio.

# BASIC REACTANCE MODULATOR (ELECTRON TUBE)

## Application.

**The** frequency modulator is used in fm transmitters to vary the frequency of an r-f signal in accordance with the intelligence to be transmitted.

#### Characteristics.

Output is used to change the frequency of an oscillator.

Has a high signal-to-noise ratio.

Output frequency is independent of modulating frequency.

Has relatively low inherent distortion.

#### Circuit Analysis.

**General. The** purpose of the modulator stage is to convert an audio signal into a radio frequency containing the audio intelligence.

In the basic reactance tube modulator, a tube is used to change the resonant frequency of an oscillator by an amount proportional to the amplitude of the modulating signal. The polarity of the modulation determines the direction of the frequency shift; for example, an increase in oscillator frequency for a positive polarity, and a decrease in frequency for a negative polarity. The rate at which this frequency deviation occurs is determined by the frequency of the audio modulation.

**Circuit Operation.** A schematic diagram of a basic reactance tube modulator is illustrated.



Basic Reactance Tuba Modulator

VI performs the function of the reactance tube, using cathode bias, supplied by RI and Cl. L1 is an r-f choke which acts as the plate load, and keeps the a-c component of plate current out of the power supply. Capacitor C2 and resistor R2, in parallel with the oscillator tank circuit consisting of C3 and L2, performs the function of a variable variable **reactance**. C4 and C5 are grid and plate coupling capacitors, respectively.

With no audio signal applied to the grid of VI, the only voltage present across the C2, R2, network is the voltage across the oscillator tank circuit, C3 and L2. The values of C2 and R2 are chosen so that the reactance of C2 is large in comparison to the resistance of R2. This factor permits the capacitive reactance to be the current controlling component, and causes the voltage across it to lag the current through it by approximately 90 degrees. This same current flows through R2 and another voltage drop is produced which leads the applied voltage by 90 degrees. Actually, the current and voltage at the resistor are in phase, but since the current through the resistor leads the applied voltage (because of the capacitive reactance of C2), the voltage developed by this current also leads the applied voltage by the same amount. The reactance tube is effectively in shunt with the oscillator tank (C3 and L2) and the phase shift network (C2 and R2). Capacitor C5 allows the ac component of current to pass through it, and at the same

time, blocks the dc plate voltage from the phase-shift circuit and the tank.

The relationship of the currents and the voltages in the circuit can be best explained through the use of a vector diagram, as illustrated below.



Relationships of Currents and Voltage with no Modulation Inputs

**Voltage**  $\mathbf{e}_{\mathbf{p}}$  is the alternating component of the plate to ground voltage which appears simultaneously across the reactance tube, the phase-shift network, and the oscillator tank circuit. The reactance tube receives its ac grid-input voltage,  $\mathbf{e}_{s}$ , across R2. This voltage is the voltage drop across R2 and is in phase with the plate current  $\mathbf{i}_{\mathbf{p}}$  and the grid current,  $\mathbf{i}_{g}$ . This relationship is characteristic of amplifier tubes.

Since both  $\mathbf{i_p}$  and  $\mathbf{i_g}$  are in phase with  $\mathbf{e_s}$ , and since  $\mathbf{e_g}$  leads  $\mathbf{e_p}$  by approximately 90 degrees,  $\mathbf{i_p}$  and  $\mathbf{i_g}$  also lead e, by 90 degrees. Both of these currents are supplied by the oscillator tank circuit, and since they lead the tank voltage, they act like the current in a capacitor. Thus the injection of these currents into the tank circuit accomplishes the same effect as placing a capacitor across the oscillator tank circuit. The frequency of the tank in this case is, therefore, decreased. With no audio modulation input, this frequency is the operating, or center frequency of the modulator.

Consider now the application of audio modulation to the grid of the tube. It is important to keep in mind that we are not speaking of actual capacitive

reactance or capacitance changes. Our concern here is an effective capacitance produced by the leading currents in the R2, C2, combination. If the signal applied on the grid of V1 increases in a positive direction, the plate current of VI also increases, and since this current is an effective capacitance shunt across the oscillator tank circuit, the frequency of the oscillator is decreased. Conversely, when the grid signal shifts in a negative direction under audio modulation, VI plate current decreases, and since this current is an effective reduction in capacitance across (shunting) the oscillator tank circuit, the frequency of the oscillator is increased.

The frequency of the audio modulation does not actually affect the frequency of the output. Its only effect is that it determines the number of times per second that the oscillator changes its frequency. The amount and direction of the frequency change is determined solely by the amplitude and the polarity of the modulation input. That is, a positive signal causes an increase of frequency, while a negative signal causes a decrease in frequency. Likewise, a larger amplitude signrd causes a greater frequency change than a smaller amplitude signal.

**Circuit Variations.** There are several circuit variations of the basic reactance tube modulator, but most of these variations are only differences in the arrangement of the phase shifting circuit (the R2, C2, combination in the previous example). The following illustration shows how the circuit variations cause the phase shift to be either inductive or capacitive. There is no particular advantage to any one of them over any of the others.



#### **Circuit Variations**

Part A of the figure has been explained in the previous discussion. In part B of the figure, R and C are connected in the opposite manner, and the reactance values are chosen so that the resistance of R is large in comparison to the reactance of C. Since the resistive component is so much larger, the r-f voltage applied to the plate load by the tank circuit causes the current to be in phase with the r-f voltage. The current through C, however, leads the applied voltage by 90 degrees. The voltage across C, therefore, lags

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both the current and the applied voltage by 90 degrees. This voltage is coupled to the grid of the reactance tube, and causes an r-f variation in the plate current that is in phase with the grid voltage. This r-f current is coupled to the oscillator tank and since it is in phase with the grid voltage, it must lag the current in the tank by 90 degrees. This produces the same result as injecting inductance into the tank circuit.

By substituting a small inductor in the place of C in part C of the figure, it is also possible to inject an effective capacitance into the tank circuit. The oscillator voltage applied across the plate load of the reactance tube causes a current to flow whose phase is controlled by the large resistance of R. This current is in phase with the applied voltage, since R is large with respect to L. Since tie voltage across L leads the current through it by 90 degrees, this voltage also leads the applied voltage by 90 degrees. This voltage is coupled "to the grid of the reactance tube, and r-f plate current flows which is in phase with the grid voltage and 90 degrees leading in respect to the oscillator tank voltage. The effect is, therefore, the same as injecting capacitance into the tank circuit, and the frequency is decreased.

By the same token, the reversing of R and L produces the same result as injecting inductance into the tank circuit as shown in part D of the figure. The inductive reactance of L, of course, must be large in comparison to **the** resistance of R. The r-f voltage from the oscillator tank circuit causes a current to flow through the plate load which lags the applied voltage by 90 degrees. This voltage then is applied to the grid of the reactance tube, producing an r-f plate current which is lagging the current in the tank circuit by 90 degrees, producing the effect of injecting inductance into the tank circuit.

## Failura Analysis.

**No Output. An** open or shorted L2, an open or shorted C3, or an open C4 are the only components that can cause a no output condition to exist. Check L2 for continuity and C3 and C4 for value with an **in-circuit** capacitor checker.

**Unmodulated Output. The** absence of plate voltage, an open L1, an open C5, an open RI, an open C2 or R2, or a defective V1, can cause an unmodulated output condition to exist. Check for the presence of plate voltage with a voltmeter. Check L1 for continuity and C5 for an open or short with an ohmmeter. Also check RI and R2 for proper value, and C2 for an open or short with an ohmmeter. If a modulated output is not restored, check all capacitors with an **in-circuit** capacitor checker.

# BASIC REACTANCE MODULATOR (SEMICONDUCTOR)

## Application.

The reactance modulator is used to frequency modulate low power semiconductor transmitters.

#### Characteristics.

Uses collector to emitter output capacitance to provide reactive frequency control.

Operates at relatively low power levels.

Shunts a portion of the oscillator tank coil.

Requires further limiting or clipping to eliminate a residual 10 to 15 percent amount of AM modulation.

Uses a single transistor to achieve full modulation.

## Circuit Analysis.

**General. In** an fm transistor, modulation is accomplished at the oscillator stage. The transistor oscillator is frequency modulated in the same manner as an electron tube oscillator, or by varying the gain at the modulating rate as is done with AM transistors. When the oscillator is fm modulated a slight amount of AM modulation is also inserted. Thus the modulated fm oscillator requires a limiter stage to remove the amplitude modulation before it is further amplified or multiplied in frequency. This is easily accomplished in a single stage.

**Circuit Operation.** The accompanying schematic shows the circuit of a typical frequency-modulated oscillator stage operated as a reactance modulator.



## **Reaetance Modulator**

Transistor Q1 is the FM oscillator. Resistor R1 and R2 are base bias voltage dividers. Primary L1 of transformer T1 together with capacitor C1 form the tuned tank adjusted to the oscillator output frequency. R6 is the modulator load resistor. Secondary L2 of T1 is the collector to base feedback winding of the oscillator. Tertiary winding L3 is an inductively coupled output winding which couples the FM output signal to the next stage, or in special cases to an antenna. Transformer T2 is an audio transformer which inductively couples the modulation input to the baseemitter junction of Q2, the modulator stage. Resistors R3 and R4 are base bias voltage dividers, while R5 is an emitter swamping resistor bypassed by C2 for temperature stabilization. The output capacitance of Q2 shown dotted as C<sub>a</sub> shunts a portion of the r-f oscillator coil L1. As the modulator operates the output capacitance of Q2 is varied. Thus, the frequency of the oscillator is shifted in accordance with the modulation the same as if Cl were varied instead.

When the modulation is applied to the primary of T2 it is coupled into the base circuit. Thus the

emitter-base bias changes constantly at the modulation rate. Since the bias is increasing and decreasing at the modulating rate, the collector voltage of Q2 also increases and decreases at the modulating rate. When the collector voltage increases, output capacitance  $C_{ce}$  decreases, and conversely, when the collector voltage decreases. (An increase in voltage has the effect of spreading the capacitor plates further apart by increasing the width of the PN barrier. Conversely, the reduction of collector voltage reduces the width of the PN junction and has the same effect as pushing the capacitor plates together to provide more capacitance).

When the output capacitance of C<sub>a</sub> decreases because of the increase in collector reverse bias, the resonant frequency of the O1 oscillator tank circuit increases as if Cl were decreased, and produces a higher frequency r-f output. Conversely, when the output capacitance of C<sub>cc</sub> increases because of a decrease in collector reverse bias, the resonant frequency of Q1 oscillator tank circuit decreases and produces a lower frequency r-f output because of the shunting effect of Ccc. Thus the resonant frequency of the oscillator tank circuit is increasing and decreasing at the modulating rate. Hence, the oscillator frequency is also increasing and decreasing at the modulation rate. The output of the oscillator, therefore, is a frequency modulated carrier signal. Since the audio modulation causes the collector voltage to increase and decrease, there is an AM component induced into the output. This produces both an FM and AM output. By placing a limiter stage after the reactance modulator, the amplitude variations are removed and only the frequency modulation remains, with a constant amplitude output. Frequency multipliers are then used to increase the oscillator frequency to the desired output frequency. For high power, linear r-f amplifiers are used to increase the steady amplitude signal to a particular level and power output. With the initial modulation occurring at low levels fm represents a saving in power as compared with conventional AM, with the FM noise reducing properties providing a better signal to noise ratio than is possible with AM.

## Failure Analysis.

**General.** When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of conventional voltmeters. Be careful also to

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observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

**No-Output.** Open bias resistors, open collector resistor R6, or open windings on T1, can cause a no-output condition. Check the resistors for proper value with an ohmmeter and the transformer for continuity. If satisfactory indications are obtained but **Q1** does not oscillate, the transistors may be defective. If QI operates but no modulation is obtained, Q2 is defective.

Low Output. Low collector voltage, low bias voltage, or a weak transistor may cause a low output. Check the supply voltage first to be certain it is normal, then check the collector voltage of both Q1 and Q2, and the base bias of Q1 and Q2 also, if the collector voltage is normal. Also check collector resistor R6 for proper value if the modulation appears weak. Low bias can be caused by a change in bias voltage dividers R1 and R2, and R3 and R4; check for proper resistance value with an ohmmeter. A high resistance connection in output winding L3 of T1 may also occur and course a reduced output.

# BALANCED REACTANCE MODULATOR (ELEC-TRON TUBE)

## Application.

**The** balanced reactance tube modulator is used in fm transmitters to vary the frequency of an r-f signal in accordance with the intelligence to be transmitted.

## Characteristics.

**Has** relatively high degree of frequency shift. Has low inherent distortion. Has high signal-to-noise ratio.

## Circuit Analysis.

**General. The** purpose of the modulator stage is to convert an audio signal into a radio frequency containing the audio intelligence. In the balanced reactance tube modulator, two tubes are used to change the resonant frequency of an oscillator by an amount proportional to the amplitude of the modulating signal. The polarity of the modulation determines the direction of the frequency shift, for example, an increase in oscillator frequency for a positive polarity, and a decrease in frequency for a negative polarity.

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The rate at which this frequency deviation occurs is determined by the frequency of the audio modulation.

**Circuit Operation.** A schematic diagram of a balanced reactance tube modulator is shown in the accompanying illustration.



**Balanced Resistance Tube Modulator** 

V1 performs the function of one of the reactance tubes, and operates in conjunction with V2, in a push-pull manner. Cl and R1 form a cathode bias circuit, which is common to both of the tubes. L1 and L3 are r-f chokes which act as plate loads for the tubes, and keeps the a-c component of plate current out of the power supply. The C2-R2 combination, together with the C5-R3 combination, both in parallel with the oscillator tank circuit, made up of L2 and C3, perform the function of a variable reactance. C4, C6, and C7, are grid and plate coupling capacitors, respectively.

Circuit operation can be easiest understood, if analyzed and discussed as two separate circuits. One circuit, consists of V1, L1, C7, C2, and R2, while the other circuit consists of V2, L3, C6, R3, and C5. The remaining components are common to both of the circuits.

We shall first consider the operation of the **circuit** consisting of V1 and its associated components. With no audio signal applied to the grid of **V1**, the only

voltage present across the C2-R2 network is the voltage across the oscillator tank circuit. The values of C2 and R2 are chosen so that the reactance of C2 is large in comparison to the resistance of R2. This factor permits the capacitive reactance to be the current controlling component, and causes the voltage across it to lag the current through it by approximately 90 degrees. This same current flows through R2 and another voltage drop is produced which leads the applied voltage by 90 degrees. Actually, the current and voltage at the resistor are in phase, but since the current through the resistor leads the applied voltage (because of the capacitive reactance of C2), the voltage developed by this current also leads the applied voltage by the same amount. The reactance tube, VI, is effectively in shunt with the oscillator tank and the phase shift network. Capacitor C7 allows the ac component of current to pass through it, and at the same time, blocks the dc plate voltage from the phase-shift circuit and the tank.

The relationship of the currents and the voltages in the circuit can be best explained through the use of a vector diagram. Refer to the previous discussion of the Basic Reactance Tube Modulator (Electron Tube) in this section of the Handbook for this illustration.

Voltage ep is the alternating component of the plate to ground voltage which appears simultaneously across the reactance tube, the phase-shift network, and the oscillator tank circuit. The reactance tube receives its ac grid-input voltage, eg, across Rg. This voltage is the voltage drop across Rg and is in phase with the plate current ip and the **grid** current, ig. This relationship is characteristic of amplifier tubes.

Since both ip and ig are in phase with eg, and since eg leads ep by approximately 90 degrees, ip and ig also lead ep by 90 degrees. Both of these currents are supplied by the oscillator tank circuit, and since they lead the tank voltage, they are acting like the current in a capacitor. Thus the injection of these currents into the tank circuit accomplishes the same effect as placing a capacitor across the oscillator tank circuit. The frequency of the tank in this case is therefore decreased. With no audio modulation input, this frequency is the operating, or center frequency of the modulator.

Consider now the application of audio modulation to the grid of the tube. It is important to keep in mind that we are not speaking of actual capacitive reactance or capacitance changes. Our concern here is an effective capacitance produced by the leading currents in the R2-C2 combination. If the signal applied on the grid of V1 increases in a positive direction, the plate current of V1 also increases, and since this current is an effective capacitance shunt across the oscillator tank circuit, the frequency of the oscillator is decreased. Conversely, when the grid signal shifts in a negative direction under audio modulation, V1 plate current decreases, and since this current is an effective capacitance across (shunting) the oscillator tank circuit, the frequency of the oscillator is increased.

Before attempting to **explain** the operation of the \_ circuit made up of V2, it should be pointed out that there are several minor circuit variations of the previously discussed circuit. Most of these variations concern differences in the phase shifting circuit (the R2-C2 combination in the previous example). There is no particular advantage to any one of them over any of the others. Refer to the circuit variations illustrated in the previous discussion of the Basic Reactance Tube Modulator (Electron Tube) during the following discussion.

Part A of the figure has already been explained. In part B of the figure, R and C are connected in the opposite manner, and the reactance values are chosen so that the resistance of R is large in comparison to the reactance of C. (This is the manner in which operation of V2 yet to be explained is connected.) Since the resistive component is so much larger, the r-f voltage applied to the plate load by the tank circuit causes the current to be in phase with the r-f voltage. The current through C, however, leads the applied voltage by 90 degrees. The voltage across C, therefore, lags both the current and the applied voltage by 90 degrees. This voltage is coupled to the grid of the reactance tube, and causes an r-f variation in the plate current that is in phase with the grid voltage. This r-f current is coupled to the oscillator tank and since it is in phase with the grid voltage, it must lag the current in the tank by 90 degrees. This produces the same result as injecting inductance into the tank circuit.

By substituting a small inductor in the place of capacitor C in part C of the figure, it is also possible to inject an effective capacitance into the tank circuit. The oscillator voltage applied across the plate load of the reactance tube causes a current flow whose phase is controlled by the large resistance of R. This current is in phase with the applied voltage, since R is large with respect to L. Since the voltage across L

+

leads the current through it by 90 degrees, this voltage also leads the applied voltage by 90 degrees. This voltage is coupled to the grid of the reactance tube, and an r-f plate current flows which is in phase with the grid voltage and 90 degrees leading in respect to the oscillator tank voltage. The effect is, therefore, the same as injecting capacitance into the tank circuit, and the frequency is decreased.

By the same token, the reversing of R and L produces the same result as injecting inductance into the tank circuit, as shown in part D of the figure. The inductive reactance of L, of course, must be large in comparison to the resistance of R. The r-f voltage from the oscillator tank circuit causes a current to flow through the plate load which lags the applied voltage by 90 degrees. This voltage is then applied to the grid of the reactance tube, producing an r-f plate current which is lagging the current in the tank circuit by 90 degrees, producing the effect of injecting inductance into the tank circuit.

The V2 circuit operates in the same reamer as the VI circuit, only instead of injecting a capacitive reactance into the oscillator tank, it injects an inductive reactance. Upon close examination of the V2 circuit, it can be seen that the phase shifting circuit, R3 and C5, are connected in the opposite manner to the R2-C2 combination in the first example. By referring to the illustration of circuit variations, it can be seen that this type of connection (Part B of the figure) produces the effect of inductance in parallel with the tank circuit. It should be noted here that an increase in plate current in the first example caused an increase in the capacitive reactance injected into the tank, and hence the oscillator frequency decreased. In the V2 circuit, the inductive reactance is decreased with an increase in plate current, and thus produces an increase in the oscillator frequency. Now let us see what occurs when both circuits are connected as shown, and an audio signal is applied to the transformer Tl.

When the input signal is such that the grid of VI is positive, and the grid of V2 is negative, the following action results. The negative signal on the grid of V2 drives V2 into **cut-off**, and a further negative increase produces no further change. VI, however, conducts a greater as the signal on the grid becomes more positive, and thus additional capacitive reactance is injected into the oscillator tank circuit, resulting in a decreasing frequency. As the signal on the grid reaches its positive peak, and begins decreasing towards zero,

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the oscillator frequency begins increasing, and when the grid is returned to zero, the oscillator is again at the center frequency. The signal now continues in a negative direction and V1 is driven into cut-off. V2, the grid of which is connected to the opposite end of T1, is now brought into conduction, and begins to inject an inductive reactance into the tank circuit, resulting in an increasing frequency. As the "signal on the grid reaches its positive peak, and begins decreasing towards zero, the oscillator frequency begins decreasing and as the signal reaches zero the oscillator is again at the center frequency. The overall result of one cycle of audio modulation is shown in the following illustration.

Thus, it can be seen that the frequency of the audio modulation does not actually have an effect on



**Effect of Modulation** 

the frequency of the output. The only effect is that it determines the number of times per second that the oscillator changes its frequency. The amount and direction of the frequency change is determined by the amplitude and the polarity of the modulation input.

## Failure Analysis.

**No Output. An** open or shorted L2, an open or shorted C3, or an open C4 are the only components that can cause a no-output condition to exist. Check L2 for continuity and C3 and C4 for value with an in-circuit capacitor checker.

**Distorted or Unmodulated Output.** A defective V1 or V2, a defective T1, an open or shorted L1 or L3, an open or shorted C2 or C5, or an open R2 or R3 can cause a distorted output condition to exist. With an ohmmeter, check the continuity of L1 and L3, and check R2 and R3 for proper value. Also check C2, C5, C6, and C7 for opens or shorts with an ohmmeter. Check transformer T1 for continuity, as one half of the secondary may be open. If a distorted output still exists, check all capacitors with an in-circuit capacitor checker.

An unmodulated output can be caused by a defective Tl, an open or shorted RI, or an open or shorted Cl. With an ohmmeter, check the continuity of T1 and the value of RI. Check Cl for an open or short with an ohmmeter. An unmodulated output may also be caused by components being defective in pairs, that is, VI and V2, L] and L3, C6 and C7, etc. Check ail components in this case, in the manner described in the preceding paragraph.

## PART 12-4. PHASE

#### PHASE MODULATION (PM)

## General.

In phase modulation, sometimes referred to as indirect frequency modulation, the audio signal is used to shift the phase and the frequency of the carrier frequency, resulting in a frequency variation in the output. The amount of phase deviation is directly proportional to the amplitude of the audio signal, and the amount of frequency deviation is proportional to the frequency of the audio signal. An illustration of phase modulation follows.



## **Result of Phase Modulation.**

The solid line represents the carrier frequency. If an audio signal is introduced at the beginning of time Tl, the next positive peak occurs, for example, at time T3, shown in dotted lines, instead of at a time T2, where it would normally occur. Since the peak following TI now occurs at a later time, the phase of the output is now lagging the carrier. By the same token, the phase can be changed to a leading one by the applications of a signal of opposite polarity. Thus the amount and direction of phase shift varies in accordance with the amplitude and polarity of the audio input. A frequency variation also occurs in the output, because the frequency of the modulating signal determines the rate at which the phase of the carrier deviates, and thus determines the amount of frequency deviation.

The frequency of the carrier before a phase shift occurs is called the center frequency, and is generated by a crystal controlled oscillator, which accounts for the excellent frequency stability of the phase modulator.

The phase variations, called modulation, are not applied until after the carrier frequency is generated and it is this peculiarity which allows the use of a crystal oscillator. With no audio signal applied, only the carrier frequency, is transmitted.

Since random noise usually consists of higher \_ frequencies, the signrd to noise ratio at the higher audio frequencies may be lower. It is for this reason that the audio modulation is coupled through a pre-emphasis network before being applied to the modulator circuit. The pre-emphasis network increases the relative signal strength of the higher frequency components of the audio signal, and thereby compensates for any decrease in signrd-to-noise ratio as caused by random high frequency noise. This creates a state of unbalance between the amplitudes of the high and low frequency components, but is is compensated for in the receiver by the use of a de-emphasis circuit, which performs the opposite function of pre-emphasis.

The greatest advantage of the phase modulator is, as previously mentioned, its excellent frequency stability, which results from the use of a crystal oscillator.

The advantage of this type of modulation over a-m is its noise reducing capabilities. Most noise signals produce amplitude modulation of the carrier, or the carrier-plus-modulation signal, which is applied to the demodulating circuit in the receiver. If the receiver is responsive to amplitude variations, as in a-m receivers, this random noise is detected and amplified. If the receiver is responsive only to changes in frequency, as in an f-m receiver, phase modulation makes possible a considerable increase in the signal-to-noise ratio. Actually, phase modulation is a form of f-m, the difference being that whereas f-m is responsive only to changes in amplitude, p-m is responsive to both the amplitude and the frequency of the audio modulation.

A better understanding of phase modulation can be obtained from the following descriptions of **specific** phase **modulator** circuits.

# **BASIC PHASE MODULATOR (ELECTRON TUBE)**

#### Application.

**The** phase modulator is used in transmitters to vary the frequency of an r-f signal in accordance with the intelligence to be transmitted.

#### Characteristics.

Carrier frequency is supplied by a crystal controlled oscillator.

Frequency stability is excellent.

Has a high signal-to-noise ratio.

Operates over the linear portion of the Eg – Ip curve.

#### Circuit Analysis.

**General. The** purpose of the modulator stage is to convert an audio signal into a radio frequency containing the audio intelligence.

In the basic phase modulator, a crystal controlled oscillator supplies the desired basic frequency to the grid of a triode. A modulating (audio) signal is also applied to the grid of this modulator tube, and a phase shift occurs in the r-f output. The amount and direction of the phase shift is proportional to the amplitude and polarity as well as the frequency of the audio modulating signal.

**Circuit Operation.** A basic phase modulator is shown in the accompanying schematic diagram.



**Basic Phasa Modulator.** 

The crystal oscillator r-f output is coupled through coupling capacitor Cl to the grid of VI, and it is this crystal oscillator frequency which is the center frequency of the phase modulated output. Resistors Rl, R2, and R3 forma voltage divider, across which both the oscillator r-f signal and the audio modulation is applied. R2, in conjunction with C2, also performs the function of a decoupling network, which bypasses the lower end of R1 to ground and prevents the r-f carrier frequency component from feeding back into the audio circuits through T1. In effect, it isolates the r-f from the audio, despite the apparent common connection. The audio modulation is applied through transformer T1 and through R2 and R1 to the grid of V1. Cathode resistor R4 provides degenerative feedback, and the plate tank circuit, consisting of L2 and C3, is tuned to a frequency below the lowest output r-f frequency. Because R4 is unbypassed and causes degenerative feedback, the tube gain is relatively low.

The r-f signal (the carrier) is of constant amplitude and frequency, and with both positive and negative cycles equal in amplitude, no bias change is produced

on VI grid. Thus an amplified r-f carrier appears as the reproduced output, with the normal 180 degree grid to plate phase shift. The audio modulation, however, applied through transformer T1, provides, in effect a changing bias on V1 grid as it varies in amplitude and polarity. As a result, the gain of the tube is varied in accordance with the audio signal bias. The manner in which this variation in the gain of the triode is converted into a phase shift of the carrier, can be better understood through the use of vector diagrams.

The voltage produced by normal amplifier action is represented as ep. Another r-f voltage is produced by the grid to plate capacitance of the tube, and is represented as ec, and the result of these two r-f plate voltages, which is the instantaneous plate voltage, is represented as er. Due to normal amplifier action, ep is 180 degrees out of phase with eg, the grid voltage and its amplitude is relatively low because of the degenerative effect of the unbypassed cathode resistor, R4. Since ec lags eg by some amount, er, which is the vector result of ec and ep it falls somewhere between these two voltages, as illustrated in the following diagram.





When the signal on the grid increases in a positive direction, the amplitude of the plate signal also increases, with the following result. The vectors which



Vector Diagram For Increasing Grid Voltage

change as a result of this increase in grid signal are designated as e'g, e'r, and e'p. 'Voltages eg, er, and ep are shown in order to compare this example with the previous one. It can be seen therefore, that with a larger signal on the grid (e'g), the closer e'p and e'r become in phase.

Conversely, when the grid signal (e'g)"decreases in amplitude, the plate signal, e'p decreases, as illustrated in the following diagram.



Vector Diagram For Decreasing Grid Voltage

As a result, the vector er shifts further out of phase with ep (to e'r) than it was under the first

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condition illustrated. By comparing these three illustrated circumstances, it can be seen that the phase relationship between er and eg constantly changes in phase as eg varies in amplitude and polarity.

The overall effect is that the amplitude of the modulating signal determines the amount and direction of phase deviation of the carrier in the output. The frequency of the modulating signal determines the rate at which the phase of the carrier deviates, and thus determines the amount of frequency deviation. This effect can be more clearly seen by referring to the following illustration showing the different frequencies produced by adding F1 and F2, and F1 and F3.

The carrier (oscillator) frequency is represented by F1 in part C of the figure. F2 (shown in part A of the figure) represents the modulation frequency, and the result of adding or combining F1 + F2 is shown in part E of the figure. As shown in the figure, F2 starts at 10-volts positive. Assume, for ease of explanation, that this positive 10-volts modulation causes a full 90-degree phase shift in the carrier. Now, since the carrier frequency F1 is at O at the same instant, the sum value (Fl + F2) is at +10 volts and, by assumption, leads F1 by 90 degrees. As the modulation voltage (F2) decreases to +5 volts, the phase shift is reduced to one-half maximum or 45 degrees. At this point, F1 has completed 180 degrees of its cycle and is at O voltage, except that the 45 degree advance makes the sum of F1 and F2 a minus 5-volts instead, as shown in part E of the figure. As modulation Voltage F2 continues to decrease and reaches O voltage, no further phase shift occurs and the carrier and modulator voltages are again in-phase (at this point F1 has just completed 360 degrees of its cycle and by coincidence happens to be at O voltage also). The negative modulation cycle now continues, and, when F2 reaches -5 volts it also causes a 45 degree phase shift, but this time the shift is in a lagging direction. Therefore, although F1 is actually at O, the lagging sum produces a +5 volts combined signrd as shown at E. In this manner, the phase shift follows the modulating voltage, leading on the positive half cycle of modulation and lagging over the negative half cycle, with the amount of phase shift being proportional to the im.tantaneous amplitude of the modulating signal.



## Effect of Frequency and Amplitude Changes of Modulating Signal

By following the relationship between F1 and F3 (part B of the figure) in the same manner as for F1 and F2 as just explained, we see that when a modulation frequency twice that of F2 is used, the sum shown in part D of the figure is an increasing frequency. Since frequency deviation increases with an increase in the modulation frequency, this is the result to be expected and proves our previous assumptions to be correct.

## Failure Analysis.

**No Output.** A defect in nearly any component in the circuit can cause a no output condition to exist. Check with an oscilloscope to make sure that both the oscillator and the audio modulation are present at the inputs to the circuit. If either one is missing, the modulator is probably not defective, and the output will probably be restored with the restoration of the missing input. If both inputs are present, disable the oscillator, and check for the modulation input of the

grid. If not present, check transformer T1 for continuity with an ohmmeter. Check RI, R2 and R3 for a change in value, and C2 for a short. Disable the audio input, and check for the presence of oscillator frequency **on** the grid. If absent, check Cl for an open. If both signals are present on the grid, check R4 for value, and L2 for continuity. Check for the presence of plate voltage with an voltmeter. Check C3 for a short, and C4 for an open. If a no-output condition still exists, check all capacitors with an in-circuit capacitor checker.

Low or Distorted Output. A low or distorted output can also be caused by a defect in nearly any component in the circuit. Check for the proper amplitude of each input signal on the grid of tube VI with an oscilloscope. If low, determine whether it is low due to a defective oscillator or audio stage, or if it is a defect in the modulator circuit itself. If localized to the modulator, check transformer T1 continuity and resistors R1 and R3 with an ohmmeter. Check C2 for proper value with an in-circuit capacitor checker. Check R4 for value. Check plate voltage and determine whether or not the power supply is defective. Check C3 and C4 with an in-circuit capacitor checker, and check the continuity of L2 with an ohmmeter.

## PHASITRON MODULATOR (ELECTRON TUBE)

#### Application.

**The** phasitron is used in transmitters to vary the frequency of an r-f signal in accordance with the intelligence to be transmitted.

## Characteristics.

Utilizes a special phasitron tube.

Carrier frequency is supplied by a crystal controlled oscillator.

Has a high signal-to-noise ratio.

Operates Class A.

Frequency stability is excellent.

Output modulation proportional to both amplitude and the frequency of the audio modulation.

# Circuit Analysis.

**General. The** phasitron performs the function of a phase modulator through the use of a special tube,

called the phasitron tube. The carrier frequency is generated by a crystal controlled oscillator, and coupled **through** a phase splitting network to the tube. The modulation is applied inductively to the tube through a coil arranged around the outside of the tube, and the result in the output is a phase and frequency modulated carrier.

**Circuit Operation.** A schematic diagram of a Phasitron is illustrated.



#### Phasitron Modulator.

Before attempting to understand the operation of the phasitron circuit, a basic understanding of the special tube utilized is essential. The following illustration shows the basic configuration of the structure of anode number 1, the four deflection grids, Dl, D2, D3, D4, and the electron stream, with no potential applied to the deflection plates.

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## Phasitron Anode Structure and Electron-Beam Configuration with no Potential Applied to Deflector Grids

Anode number 1 has holes punched at regular intervals above and below a dividing line. The two focusing grids, F1 and F2, are such that it shapes the electron stream into a flat disc, which strikes anode number 1 as shown. Behind anode number 1" is another anode, which receives the electrons which are permitted to pass through the holes in anode number 1. Thus, with no potential applied to the deflector grids, nearly equal current flows in each plate.

In operation, however, potentials are applied to these deflector grids, and they are each 120 degrees out of phase with each other. Upon re-examining the electron disc, but this time with the potentials applied to the deflector plates, the result is illustrated.



Phasitron Anode Structure and Electron-Beam Configuration with Potential Applied to Deflector Grids.

Now a greater portion of the stream passes through the holes in the first anode, and strike the second anode. Hence the plate current in anode number 2 is now greater than that of anode number 1. Since the potentials on D2, D3, and D4 are constantly changing (though always 120 degrees apart), the shape of the disc is also constantly changing, and shortly the disc is as shown by the dotted lines, resulting in maximum plate current in anode number 1, and minimum current in anode number 2. For any phase between these two extremes, each anode receives correspondingly more or less current. The modulation is applied to the coil around the outside of the tube, and the magnetic fields developed around this coil tends to increase or decrease the speed of rotation of the electron disc. By increasing or decreasing the speed of rotation, the frequency at which the anode current increases or decreases changes, and the output frequency is either increased or decreased.

In actual circuit operation, the carrier frequency is applied through transformer T1. The secondary of Tl, together with Cl, form a tank circuit tuned to this carrier frequency. Resistors R1, R2, R3, and R4, together with capacitors C2 and C3, form a phase splitting network, and the result is that the signals applied to D2, D3, and D4 are 120 degrees out of phase with each other. Also applied to the phase shifting network is a constant potential, tapped from the common point of R9 and R1O. Resistors R6, R7, R8, R9, and R10 perform the function of voltage dividers in order to apply the proper voltages to the respective elements of the tube. R5 is a voltage dropping resistor, and C4 is an a-c bypass. The primary of T2, together with C5, form a tank circuit, tuned to the center frequency.

Referring to the construction of the **first** anode and the shape of the electron stream, it can be seen that there is a time during which all of the electrons strike the first anode, but never a time at which all of the electrons strike the second anode. This characteristic is overcome with R5, which causes a lower potential to be applied to the first anode than to the second anode. This same resistor would also cause degeneration of the ac component of plate current however, and for this reason C4, an a-c bypass, is placed in parallel with R5. The overall effect, with no modulation applied is that the plate current is constantly rdternating between the two anodes in such a

way that when one is maximum, the other is **mini**mum, and conversely. The rate at which these currents rotate is equal to the crystal oscillator frequency, and it is to this frequency that the plate tank circuit is tuned.

When modulation is applied to the coil surrounding the tube, a magnetic field is developed, and this field advances or delays the rate of phase change of the electron stream. Thus the phase of the output leads or lags the oscillator frequency by an amount which is proportional to the amplitude and polarity of the modulation. The frequency of the modulation determines the rate at which the electron disc rotates. When the speed of disc rotation is increased, the output tank excitation frequency is higher, and when the speed of the disc rotation is decreased, the output frequency is lower.

The overall result in the output is therefore a signal which changes in phase and frequency as the audio modulation varies in amplitude and frequency.

#### Failure Analysis.

**No Output.** A no output condition can be caused by a defective VI, an open R5, a shorted Cl or C5, a defective T1 or T2, or a loss of the plate supply voltage. Check for the proper plate supply voltage with a voltmeter. Check both transformers with an ohmmeter. Check R5 for value, and Cl and C5 for a possible short with an in-circuit capacitor checker. Do not overlook the possibility of either of the tank circuits being misaligned.

Low or Distorted Output. A low or distorted output can be caused by a defect in any component in the circuit. Check for the proper value of plate supply voltage with a voltmeter. With an oscilloscope, check the presence of both the carrier and modulation inputs on their respective elements of the tube, as the obsence of either input will produce a distorted output. Check the alignment of both tank circuits. With an in-circuit capacitor checker, check the value of all capacitors, especially for a distorted output condition. Check all resistors with an ohmmeter for proper value, and the transformer for partial shorts.

## PART 12-5. PULSE

## PULSE MODULATION

#### General

Radio frequency energy in radar is transmitted in short pulses whose time duration may vary from 1 to 50 microseconds or more. If the transmitter is turned off before the reflected energy returns from the target, the receiver can distinguish between the transmitted pulse and the reflected pulse. After all reflections have returned, the transmitter can again be turned on and the process repeated. The receiver output is applied to an indicator which measures the time interval between the transmission of energy and its return as a reflection. Since the energy travels at a constant velocity, the time interval becomes a measure of the distance traveled (range). Since this method does not depend on the relative frequency of the returned signal or on the motion of the target, difficulties experienced in cw and fm methods are not encountered. The pulse modulation method is used in practically all military and naval applications.

Since most radar oscillators operate at pulse voltages between 5 Kv and 20 Kv, and require currents of several amperes during the pulse, the requirements of the modulator are quite severe. The function of the high-vacuum tube modulator is to act as a switch to turn a pulse on and off at the transmitter in response to a control signal. The best device for this purpose is one which requires the least signal power for control and which allows the transfer of power from the transmitter power source to the oscillator with the least loss. The pulse modulator circuits discussed in this section are typical pulse modulators used in radar equipments.

## SPARK GAP MODULATOR (ELECTRON TUBE)

#### Application.

The spark gap modulator is used in radar equipments to generate the pulse which controls the operation of the transmitter.

### Characteristics.

Capable of handling high peak current and voltage. Generated pulses have high peak power.

Generated pulses have low average power.

Generated pulses have a specific repetition rate.

Generated pukes have controlled duration and shape.

Output pulse is somewhat erratic in timing.

#### **Circuit Analysis.**

General. Different types of pulse modulators are used for triggering radar transmitters, depending on the particular requirements of the system. Each type contains a circuit for storing energy, a circuit for rapidly discharging the storage circuit, a pulse transformer, and an ac power source. The circuit for storing energy is essentially a short section of artificial transmission line which is known as the pulse forming line. In the spark gap modulator, the pulse forming line is discharged by a spark gap. Two types of spark gaps are in use: fixed gaps and rotary gaps. The fixed gap, discussed in this section, uses a trigger pulse to ionize the air between the contacts of the spark gap and initiate the discharge of the pulse forming line. The rotary gap is similar to a mechanically driven switch.

**Circuit Operation.** A typical freed spark gap modulator circuit is shown in the accompanying illustration.



#### Fixed Spark Gap Modulator Circuit

Between trigger pulses the spark gap is an open circuit, and current flows through the pulse transformer Tl, the pulse forming line L2, the diode Vl, and inductor LI to the plate supply voltage Ebb. These components form the charging circuit for the pulse forming line, and the entire circuit may be

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reduced to a series resonant circuit as shown in the accompanying illustration.



## Equivalent Pulse-Modulator Circuits, With Wavaforms

The impedance of the primary of T1 is negligible as far as the charging circuit is concerned, the inductance of the pulse forming line may be considered to be short circuited because of the slow charging rate, and the diode, when conducting, is effectively a short circuit; therefore, these components are omitted from the figure. In effect, then, the total capacitance (Ct) of the pulse forming line is in series with the inductor L1 across the power supply. Assuming that diode V1 and the spark gap were not present, this circuit, when shock-excited by the sudden application of voltage would produce a damped-wave oscillation. On the first peak, the voltage across the entire pulse forming line approaches twice the value of the supply voltage as shown in the illustration, and at this time the current in the inductor L1 is zero since the diode stops conducting at full charge. As the peak voltage is reached, the spark gap is triggered by a synchronous separate trigger placing the pulse-forming network in series with the primary of T1 to ground. At this time approximately half the voltage (Eps) appears across the pulse-forming network (PFN) and the other half appears across TI, since the network impedance is equal to that of T1 in this instance because of the

rapidity of discharge. The action of the pulse-forming line is such as to cause voltage Eps to continue at the same amplitude until the complete discharge of the circuit by a time interval depending upon twice its delay period. The waveforms and time relationships of the circuit action are shown in the illustration. The pulse waveform is coupled through transformer T1 to the magnetron.

The spark gap is actually triggered (ionized) by the combined action of the charging voltage across the pulse-forming line and the trigger pulse. The air between the trigger-pulse injection point and ground is ionized by the trigger voltage, and this in turn initiates the ionization of the complete gap by the charging voltage.

Coincidence between the peak of the voltage swing across Ct and the trigger pulse used to fire the spark gap is required, in order that maximum power output may be obtained from the circuit. In order to ensure correct timing diode V1 is used and the design of the charging circuit is such that its resomnt frequency is higher than half the repetition rate of the spark-gap trigger pulse. Since the diode is nonconductive when maximum charge is reached on Ct, the maximum charge is retained until the spark gap is triggered.

Inductor L1 prevents current surge through V1 when the spark gap is triggered. Where humidity or pressure may affect the ionization of the spark gap, it is enclosed in a waled container.

In some circuits a resistor and capacitor in series are comected across the primary of T1. The function of these components is to eliminate the spike (sometimes encountered on the magnetron pulse) which is caused by delay between the time the pulse is presented to the magnetron and the time the magnetron conducts.

## **Failure Analysis**

**No Output.** A no output condition can be caused by one of the following; an open Ll, a defective VI, an open L2, or a defective T1. Determine that the plate supply voltage (Ebb) and the **trigger** pulse are present. If they are not present, the trouble is in the preceding stages and the circuit is probably not at fault. If the plate supply voltage is not present on the anode of Vl, L1 is defective. If plate voltage is present on the anode of VI and no output appears, the tube is defective. Check L2 and the windings of T1 with an ohmmeter for an open or short. Low Output. A low output can be caused by a low plate supply voltage, a weak Vl, leaky or shorted capacitors, shorted windings on L1, L2, or transformer T1. Check the plate supply voltage with a VTVM, if it is not the proper value the trouble is in the preceding stages and the modulator circuit is probably not at fault. Check the **capacitors** in the circuit with an in-circuit capacitor checker. Inductors L1 and L2 and transformer T1 can be checked with an ohmmeter for shorted turns.

**Distorted Output.** A distorted output could occur if the pulse-forming line had shorted or leaky \_ capacitors or if the inductor windings became shorted or open. Check the capacitors with a capacitance checker and the inductor for continuity with an ohmmeter.

## THYRATRON (GAS-TUBE) MODULATOR

#### Application.

**The** thyratron modulator is used in radar equipment to generate the pulse which controls the operation of the transmitter.

## Characteristics.

Possesses heavy current handling capacity.

Is relatively independent of ambient temperatures.

Has positive grid control.

Has stable timing.

Can be triggered with a low amplitude pulse.

Operates over a wide range of anode voltages without readjustment.

## Circuit Analysis.

General. The hydrogen thyratron is a versatile electronic switch which requires a positive trigger of only 150 volts rising at the rate of 100 volts per microsecond. In contrast to spark devices, the hydrogen thyratron operates over a wide range of anode voltages and repetition rates. Its grid has complete control of initiation of cathode emission over a wide range of voltages. The anode is completely shielded from the cathode by the grid. Thus, effective grid action results in very smooth firing over a wide range of anode voltages and repetition frequencies. Unlike most other thyratrons, the positive grid control characteristic ensures stable operation. In addition, d the deionization time is reduced by using the hydrogen filled tube. This makes the performance of the

tube relatively independent of ambient temperature so false triggering is avoided.

The hydrogen thyratron modulator provides improved timing because the synchronized trigger pulse is applied to the control grid of the thyratron and instantaneous firing is obtained. In addition, only one gas tube is required to discharge the pulse forming line, and a low amplitude trigger pulse is sufficient to initiate discharge. A damping diode is used to prevent breakdown of the thyratron by reverse voltage transients. The thyratron requires, for a driver pulse, a sharp leading edge and depends on a sudden drop in anode voltage (controlled by the pulseforming line) to terminate the pulse and turn off the tube.

**Circuit Operation.** The schematic of a typical thyratron gas tube modulator circuit is shown in the accompanying illustration.



#### **Typical Thyratron Gas Tube Modulator Circuit**

L1 is a charging inductance. The damping circuit consists of damping diode VI, current limiting resistors R1 and R2, together with r-f bypass capacitor Cl, which hold the plate of V2 at ground level during each negative half cycle of operation, thus eliminating the possibility of a negative overshoot and the production of damped oscillations. Inductor L2 with capacitors C2, C3, C4 and C5 form the pulse-forming line which develops and shapes the output pulse. Transformer T1 couples the shaped

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pulse output of the circuit inductively to the magnetron.

With no trigger pulse applied, as the circuit is turned on, the pulse forming line charges through the primary of Tl, the pulse forming line, charging inductor L1, and the power supply to ground. When the pulse-forming line reaches maximum charge, a synchronized trigger pulse is applied to the grid of thyratron V2, ionizing the tube (which acts like a closed switch) and provides a discharge path for the primary of T1 and the pulse-forming network to discharge to ground, through V2. As the voltage across the pulse forming network discharges and falls below the ionization level of the thyratron tube, the tube shuts off like opening a switch. However, there is a tendency for the positive discharge voltage to swing negative as it is abruptly stopped and cause negative overshoot because of the inductive properties of the discharging circuit. This negative overshoot is prevented from affecting the output of the circuit by the insertion of damping diode VI and the damping circuit consisting of Rl, R2, and Cl. This damping circuit provides a path for the overshoot transient through Vl, and it is dissipated by RI, and R2. Cl is a high frequency bypass to ground to preserve the sharp leading and trailing edge of the rectangularly shaped pulse.

#### Failure Analysis.

**No Output.** The following defects can cause a no-output condition. Low plate supply voltage, an open charging choke L1, or pulse-forming line choke L2, the windings of T1 being shorted or open, a defective tube V2, or a trigger pulse of insufficient voltage to ionize V2.

Check the plate supply voltage, if it is not normal, the trouble is probably in the power supply and the modulator circuit is probably not at fault. If plate voltage is normal, check the voltage on the cathode of V1. If no voltage is present, L1 is open.

If no voltage is present on the primary of Tl, pulse-forming line inductor L2 is open.

Make a point to point check with dc voltmeter (make certain you observe all high-voltage safety regulations) for the proper voltages in the charging circuit. Should no voltage be present at any of the points, the component or components associated with that portion of the circuit is defective; check the inductors with an ohmmeter (be careful to use a shorting stick to make certain the line is discharged) and the capacitors with an in-circuit capacitor checker. With an oscilloscope, check for the proper trigger pulse (both arn'plitude and repetition rate).

Low Output. Insufficient plate voltage, an improper trigger pulse, a defective pulse-forming network, or a defective magnatron transformer, T1, can cause a low output. Use an ohmmeter for checking the inductors and transformer T1 (make certain the pulse network is discharged **first**), and an in-circuit capacitor checker for checking the capacitors in the pulse-forming line.

**Distorted Output.** With the proper trigger signal and plate supply voltage, a distorted output can be caused by shorted turns on inductors L1, and L2 or on the windings of **T1**. Use an ohmmeter to check for proper values. The pulse-forming line components, if defective, can also cause the output to become distorted. These can be roughly checked with an ohmmeter and an in-circuit capacitor checker.

### HARD-TUBE MOD ULATOR

### Application.

**The** hard-tube pulse modulator is used in radar equipments to develop the pulse which controls the operation of the transmitter.

## Charactaristk

**Needs** a shaped high-voltage pulse for operation. Biased to cutoff. Has gain of about 10.

## **Circuit Analysis**

General. The hard-tube pulse modulator operates as an amplifier tube with a gain of about 10. The modulator tube is normally biased to cutoff. The application of a positive pulse of about 1300 volts to the grid is necessary to overcome the bias, causing VI to conduct and dropping the plate-to-cathode potential from the plate supply value established by the cutoff condition. Because of the large resistance of the plate load resistor, the negative voltage pulse developed by this action is effectively applied to the output transformer and the modulator tube in series. Since the impedance of the modulator tube is about one-tenth that of the output transformer, about nineteenths of the voltage pulse appears across the output transformer. The time between pulses is known as the charging time. A damping diode is in the circuit to

damp out the oscillations produced by a negative overshoot when the positive pulse applied to the grid of the modulator is terminated. The damping is accomplished on the first oscillatory swing by shorting it to ground (the negative pulse on the cathode causes the diode to conduct).

**Circuit Operation. The** schematic of a typical hard-tube modulator is shown in the accompanying illustration.





V1 is the modulator tube, R1 is the screen voltage dropping resistor, and R2 is the plate load resistor for VI. Capacitor Cl couples the output of the modulator to output transformer T1. Tube V2 is the damping diode, and T1 is the step-up output (magnetron) transformer.

With no trigger pulse applied from the driver, coupling capacitor Cl charges to the plate supply voltage through the primary of T1, R2, the power supply and ground. Tube V1 is biased at cutoff and the plate-to-cathode potential is established by the cutoff condition. A synchronized trigger pulse from the driver circuit is applied to the grid of **V1** taking the tube out of cutoff and causing it to conduct. This is similar to closing a switch, and provides a path for Cl to discharge through both the primary of T1 and V1 to ground. This discharge occurs only for the duration of the trigger pulse applied to the grid of VI. When the trigger pulse terminates, the modulator is again cutoff and the magnetic field in the primary of T1 collapses, causing a reverse flow of electrons in the circuit. This reverse flow of electrons is prevented from causing negative oscillations by diode V2, which conducts as soon as the plate goes in a positive direction (when a negative pulse appears on the cathode). Thus, diode V2 dampens any oscillations which would effect the output pulse of the modulator circuit.

#### Failure Analysis.

**No Output.** Should plate load resistor R2 open, coupling capacitor Cl open, damping diode V2 short, or the windings of transformer T1 be open or shorted, no output would appear on the secondary winding of T1. First check for **plate** supply voltage at the source. If the supply voltage is present, a drop should appear across R1. At the junction of R2, Cl, if no voltage is present, R2 is open. Check the windings of T1 for continuity or a short, with an ohmmeter.

Low Output. An incorrect plate or screen supply voltage, a weak VI, shorted turns on transformer Tl, or any of the components in the circuit changing value could cause a low output. Check all supply voltages and the trigger voltage from the driver. If any of these voltages are incorrect, the trouble is in that stage and the modulator circuit is probably not at fault. Check screen and plate load resistors R1 and R2, respectively, with an ohmmeter. Check coupling capacitor Cl with an in-circuit capacitor checker, and transformer T1 with an ohmmeter.

**Distorted Output. Distortion** can occur from any of the following: an improper trigger pulse, a change in screen or plate supply voltage, a defective VI or Tl, a leaky coupling capacitor Cl, or load resistors R1 or R2 changing value. If the driver output puke applied to the grid of the modulator is not the proper pulse repetition rate or amplitude, the **trouble** is in the preceding stages and the modulator is probably not at fault. If the screen and plate voltages are correct, and the output is stiU distorted, determine that Cl is not leaky by using an in-circuit capacitor checker. Determine that load resistors R1 and R2 are the correct value and that output transformer T1 has no **shorted** windings.

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## SECTION 13 SPECIAL CIRCUITS

## PART 13-1. SPECIAL PURPOSE TRANSISTORS AND CIRCUITS

# TETRODE, POWER, AND SPECIAL PURPOSE TRANSISTORSAND CIRCUITS

#### General.

In this section, various types oftetrodes, power considerations, power transistors, special purpose transistors, and their basic circuitry are presented. For general information on transistors and transistor biasing, refer to the Amplifier Section of this Handbook.

#### Tetrodes.

**The** addition of a fourth element to a transistor produces a tetrode transistor. Both junction and point-contact transistors can be formed into tetrodes. In the junction transistor the fourth electrode is essentially another base electrode (B2), whereas in the point+ **ontact** type it is essentially another emitter (E2).

Junction Tetrode (Double-Besed Transistor). The junction tetrode consists of a conventional junction transistor with another base electrode (B2) added on the side opposite the BI connection. The addition of proper bias between the base electrodes decreases the collector capacitance and the base resistance, and thus improves the high-frequency response, As compared to a conventional junction transistor which has a high-frequency cutoff of approximately 30 MHz, a tetrode will have good response up to 200 MHz. A basic junction tetrode circuit is shown.



Junction Tetrode Circuit

The NPN transistor is used as an illustration for ease of explaining the operation. The tetrode is connected in the same manner as a triode, with forward emitter-junction bias and reverse collector-junction bias. Between base 1 and base 2, however, a large value of voltage is connected (on the order of volts as compared with tenths of a volt), usually about 6 volts. Since the base material is a semiconductor and the points of application are on opposite sides, there is a definite resistivity between B1 and B2 which produces a uniform drop across the base (if the base were ohmic, a short circuit would ensue). Since the applied base bias is negative and large, it blocks electron current flow through all parts of the base region, except for a small volume near the B1 connection. Thus the current is restricted to the small controlled space around the B1 terminal as shown in the following illustration. This effective reduction of the volume of the base region reduces the resistance to base current and also the base-collector capacitance through the collector junction. The over-all result

is to improve the high-frequency response of the transistor.



#### **Tetrode Action**

Since the entire base area is not available for current passage, the over-all current gain of the tetrode transistor is less than that of the triode type. At the higher frequencies (above 30 MHz) the performance of the tetrode is superior to that of the triode, and the improvement in frequency response offsets the slight loss of stage gain.

**Spacistor Tetrode. The** spacistor tetrode provides a high input impedance (up to 30 megohms) and a high output impedance (on the order of megohms), with reduced input and output capacitance and a very short transit time. It is capable of power amplification of 70 dB and a voltage gain as high as 3000. Operation is possible up to several thousand MHz, as compared to an upper limit of 300 to 400 MHz for the other types of high-frequency transistors.

A basic spacistor circuit is shown in the following illustration. The spacistor basic PN junction is reverse biased, and is manufactured so that the P-region contains a smaller depletion area than that of the Nregion. The P-region acts as the base and the N-region as the collector. By the use of a large reverse bias (on the order of 100 volts), a strong electric field is produced across the junction, but because of the reverse bias only a small reverse current flows. An emitter connection (called the injector) is made on the large N-depletion area of the junction, and it is also reverse-biased. The emitter bias is chosen so that it is less than the collector bias, and an electron current flows from the emitter to the collector electrode. The magnitude of this electron current is proportional to the difference of voltage between the emitter and collector, and, because of the intense electric field through which it flows, the transit time is very small. A fourth electrode (called the modulator) is connected to a small piece of P-type which forms another PN junction with the large Ndepletion area, and is located very close to the emitter connection. While the modulator is positively biased, it is less than the collector bias, so that the modulator is effectively reverse-biased with respect to the collector. Therefore, practically no modulator current flows, and a \_ high input resistance (several megohms) is obtained. When the modulator bias is varied, as by an input signal, the current flow between the emitter and collector is varied accordingly. Thus the modulator electrode acts similarly to the grid of an electron tube, and the emitter acts similarly to the cathode.



#### **Spacistor Circuit**

Because the emitter and modulator electrodes cover only a small area, the input capacitance is low. The collector-to-base (output) capacitance is also low because of the effect of the large N-depletion area, which reduces the total capacitance by effectively providing greater separation between the collector and base. As a result of the reduction of capacitance and the short transit time from emitter to collector, the high-frequency response is greatly improved.

**Crystal-Mixer Tetrode.** The crystal-mixer tetrode is a special four+ lement, point-contact device specially developed and constructed for use as a mixer. Although it has the same number of elements

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as the point-contact tetrode, it differs in construction and operation. This unit has approximately the same conversion gain as a **conventional** vacuum-tube mixer, but it operates better at high frequencies. It is superior to the conventional crystal-diode or triode mixer.

The mixer tetrode is constructed with two emitters and one collector as shown in the following illustration. The emitters are located at equal distances on opposite sides of the collector so that both emitters have the same effect on the collector. The collector output is equal to the sum of the outputs it would have if each emitter were operated separately, provided that the collector is not given into saturation.



crystal Mixer Tetrode

Point-Contact Tetrode. The conventional pointcontact four-element (tetrode) transistor differs from the specially constructed crystal-mixer tetrode discussed above in both operation and construction. (See the following illustration.) Emitter No. 2 in the point-contact tetrode is spaced a greater distance from the collector than emitter No. 1. Both emitters are forward-biased and the collector is reverse-biased, as in a junction transistor. When emitter No. 1 is connected and emitter No. 2 is left open, the transistor operates like a conventional triode with a current gain of 1.5" to 3. When emitter No. 2 alone is used, because of the greater spacing from the collector, the current gain is small (about 0.2). When both emitters are used together, the current gain of emitter No. 1 is enhanced considerably, from 4 to 8, which is roughly 2-1/2 times the original value. Emitter No. 2 may be used as an input control element, if desired,

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and the current gain will vary according to the input signal.



**Basic Point-Contact Tetrode Circuit** 

The increase in current gain when both emitters are properly biased and operated simultaneously results from the fact that the concentration of holes injected by the first emitter attracts electrons away from the base region, between the second emitter and the collector. This reduces the possibility of electronhole recombination and enables many of the secondemitter injected holes to reach the collector, thereby increasing the flow of collector current.

## Power Transistors and Considerations.

Power transistors use special construction and design considerations to achieve rated output. The conventional transistor is usually operated at low voltages and low values of current, whereas the power transistor is operated at relatively high voltages and high currents to produce power outputs. The classification of power transistors, however, is somewhat arbitrary, and does not include the same order of values as used for electron tubes. For example, transistors of from 2 to 50 milliwatts are classed as non-power types, from 50 milliwatts to 500 milliwatts (1/2 watt) as low-power types, from 500 to 1000 milliwatts (1-watt) as medium-power types, and all over 1 watt as high-power types.

Because the transistor is a nonlinear device, it does not respond to large signals (where variations in collector voltage and current are a significant fraction of the total range of operation) in the same manner as it responds to small signals; hence, small-signal parameters are used to define nonpower (linear) operation, and large-signal parameters are used to define power (nonlinear) operation. Small signals can arbitrarily be defined as those which are less than 1 volt, and large signals as those which are greater than 1 volt. Since it is possible to have a small signal driving a power amplifier, it can be seen that sometimes either parameter can be used to predict circuit performance with good approximations.

While both point+ **ontact** and junction transistors can be used as power amplifiers, the point-contact type is usually limited to values not greater than 1 watt. This limitation is due to the fact that the point contact is unable to carry a heavy current without excessive heating and consequent damage to the transistor.

The power transistor must be able to dissipate the internally generated heat while operating at the increased temperature resulting from its own heat. It must also be able to operate at high currents and voltages without breaking down or causing excessive non-linearity (distortion). Since the junction transistor does not concentrate the heat around a point source, but spreads it throughout the junction, it has a definite advantage for power use. Both NPN and PNP junctions may be used, and they operate fundamentally the same regardless of the method of manufacture (grown junction, diffused-junction, alloy junction, etc.).

The current rating of a power transistor is the maximum collector current that can safely be carried by the transistor, without exceeding the power rating, causing internal damage, or producing an excessive loss of current gain at higher emitter currents.

The voltage rating of a power transistor is the voltage for which a specific leakage current occurs for a specific circuit configuration and operating current.

The power rating of the transistor is the maximum permissible power which may be safely dissipated by the unit without exceeding the maximum junction temperature and causing damage instantaneously or over a period of time.

The saturation voltage is the value below which the collector voltage cannot be further reduced, even by increasing the input current.

The thermal resistance of a transistor is the ratio of the difference in actual power rating with respect to the rise of temperature of the transistor. It is commonly expressed in degrees centigrade/milliwatt, or watt.

Thermal runaway is the condition whereby a small increase of collector leakage current occurs, because of an increase in the ambient temperature of the junction, and causes an increase in junction temperature, which, in turn, causes another increase of leakage current. This action builds up in an exponential manner, until complete thermal runaway occurs, permanently damaging the transistor. The power transistor is most sensitive to thermal runaway when it is operating near its maximum collector dissipation value and no thermal compensation circuitry is used. Thermal compensation is discussed later in this section of the handbook.

Either of two general methods is used to provide for heat dissipation and improve the power-handling capability of a power transistor-the use of a so-called infinite heat sink or liquid cooling of the transistor. The heat sink consists of an integrally constructed base mount, usually made of copper, plus a physical connection from the transistor shell to the collector. The base mount usually is directly connected to the chassis, which serves as the infinite heat sink. In cases involving high power, a special heat sink is provided, including fins for heat radiation into the surrounding air, and sometimes the transistor shell is provided with fins. Where the transistor cannot be grounded directly to the chassis, it is usually insulated from the chassis by a thin mica sheet. Liquid cooling is accomplished by sealing a cooling agent in the transistor case and allowing liquid convection to the metal case to provide the transfer of the heat to the air. In extreme cases, a circulating system is provided and the transistor is immersed in the cooling liquid similar to a water-cooled electron tube.

Medium power transistors usually employ Class A amplification, whereas higher-powered units use Class AB or B amplification because of its increased **effi**ciency. See the introduction to the Amplifier Section of this handbook for an explanation of classes of operation. Class C is seldom employed because of the distortion produced, except for transmitting circuits which use the flywheel effect of the tank circuit to overcome the distortion, as in electron tube operation.

Complementary-symmetry circuits are also used to provide additional power output with a reduction in the number of components required and the over-all

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circuit cost. The following figure shows a typical complementary-symmetry, push-pull circuit using an NPN transistor for one half of the circuit and a PNP transistor for the other half. Since the polarities and currents in these transistors are opposite and equal (for matched units), it is evident that one transistor works on one half of the input cycle and that the other transistor works on the other half of the cycle. The out-of-phase outputs are added at the proper time (in-phase) to produce an output from the load resistor which is equal to the continued effect of the collector currents.



**Complementary-Symmetry Push-Pull Circuit** 

Power transistors are used in audio, video, and r-f applications where outputs are required to operate electromagnetic or electrostatic output devices, in switching circuits, and in power circuits as substitutes for relays. They are especially advantageous when used as power converters to supply high voltage dc or ac from low-voltage d-c supplies to mobile, aircraft, or marine equipment. They provide increased efficiency of conversion and eliminate maintenance, mechanical, and interference problems encountered with vibrators, generators, or dynamotors.

#### Special-Purpose Transistors and Circuits.

The special-purpose transistors and circuits discussed in the following paragraphs are representative of the present state of the art, Discussion is limited to the salient points considered necessary for the user of this technical manual in the event some of the specialpurpose devices are encountered. Emphasis has been placed on presenting functionally different types, rather than manufacturer's claims for proprietary construction and materials.

PNPN Triode (Hook Collector). The PNPN triode transistor is a four-layer semiconductor device with three junctions, and exhibits a high current gain in the common-base connection. It is illustrated in the following figure. This transistor has been used more in switching circuits than in other applications because of its higher noise level, leakage currents, and limited frequency response. The transistor essentially consists of a conventional triode two-junction PNP unit with an added N-layer at the collector end. The emitter P-area (Jl) and the collector N-area (J3) are forward-biased, the base N-area is gounded, and the second P-area is left floating between the base and the collector. As a result, the middle NP junction (J2) is effectively reverse-biased. Hence, the Pl, N1, and P2 sections are comparable in action to an ordinary triode transistor. The floating P2 region, however, causes a few unusual effects. The potential hill due to the depletion region at junction J3 has a great retarding effect on the holes from the emitter, causing a "space charge" of holes to build up on the P2 side of J3. The result of this is a reduction of the J3 junction resistance, thereby allowing increased electron movement from the N2 section into the P2 section. The complete path for this current (except the small part which recombines with some of the holes) is from the negative terminal of V<sub>cc</sub> to N2, P2, N1, base lead, and back to V<sub>cc</sub>.



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Large values of current amplification may be obtained since a relatively small accumulation of holes in the P2 section gives rise to a much larger number of electrons from the N2 region. Control of the collector current is obtained since it is determined by the number of "trapped" holes in **the** P2 region, which in turn is controlled by the emitter current; the emitter current, of course, is determined by the input signal to the transistor. The name hook collector is derived from the transistor energy diagram, which resembles a hook. NPNP transistors have also been manufactured.

The hook transistor operates as an amplifier and should not be confused with the PNPN switch or with the silicon-controlled rectifier which operates similarly to a thyratron tube. In the PNPN triode switch or controlled rectifier, the second P-area is always the gated region, whereas in the hook collector it is left floating.

**Unipolar (Fieid-Effect Transistor).** The unipolar transistor uses a unique construction to utilize the effect of an electric field to control the passage of current carriers through the basic semiconductor bar. It offers a high input resistance (about one megohm) with a relatively high output resistance and good high-frequency response.

The basic unipolar circuit is shown in the following figure. The basic N-germanium bar has a potential applied between the source-end and drain-end in series with load resistor  $R_L$ . The circular P-alloy (called the gate) which encircles the bar is reverse-biased to the **source-end** of the bar. The field effect produced by the reverse bias depletes the area beneath the P-electrode of current carriers. The input signal varies the basic conductivity of the N-bar and effectively controls the current supplied by the source. Thus, current flow through the load resistor produces a corresponding but amplified output voltage.



Unipolar (Field-Effect) Transistor

Since the predominant carrier in N-type material is electrons and they are controlled by the electric field between the gate and **source-end** of the bar, and since holes are not involved, the term unipolar was derived to indicate that only one carrier is involved.

The advantage of this type of device is that a small signal controls a much greater output, which is limited essentially only by the size of the source supply and the resistivity of the basic bar material. Applications are somewhat limited by a rather high noise figure.

Unijunction Transistor (Double-Based Diode). The silicon unijunction transistor is a threeterminal semiconductor device, sometimes called a double-based diode, which is unique in that it can be triggered on by, or an output can be taken from, each of the three terminals. Once the unit is triggered, the emitter current increases regeneratively until it is limited by the power supply, thus, the action of the transistor is similar to that of the gas thyratron tube. It can be employed in a variety of circuits, but it finds its greatest usefulness in the switching and pulse fields. The basic unijunction bias connections are shown.



**Unijunction Transistor** 

The unijunction transistor consists of an N-type silicon bar with two ohmic base contacts at the ends and a P-type emitter (PN junction) near base No. 2 (B2). A base biasing potential, applied between the two base contacts, establishes a voltage gradient along the bar; the emitter is located nearer B2, so that more than half of the base bias along the bar appears between the emitter and base No. 1. If an external potential is applied between base No. 1 and the emitter greater than the internal voltage gradient between the same points, the junction is forward-biased; if the external potential is less than the internal voltage a reverse-bias is produced. Normally, reverse bias is applied between the emitter and base No. 1 (B1) so that in the off condition the emitter current is at cutoff. When a positive trigger pulse of voltage is applied to the emitter (or a negative trigger to B1 or B2), the emitter is forward-biased. An increased hole current causes a reduction in the resistance, and a reduction in the internal voltage drop between the emitter and base one. As a result, the emitter current increases regenerativdy until it is limited by the power supply. This action is spoken of as conductivity modulation of the interbase current. The unijunction is returned to the off state by a negative trigger at the emitter. A typical circuit showing input and output points is shown in the following illustration.

Resistor R3 and R4 forma bias voltage divider for the emitter, which normally holds the circuit at



## **Unijunction Input and Output Points**

cutoff. An input applied across R4 will produce a relatively high-voltage output across R1 and a relatively low-voltage output across R2. An input across R2 will produce an output across R1 and R4. Likewise, an input applied across R1 will produce outputs across R2 and R4.

Since the silicon base bar is temperature sensitive, this device can also be used in temperature-sensitive control applications by utilizing the variation of resistivity of the base with temperature. The interbase resistance increases with temperature at a practically constant rate. A typical value is 0.8 percent per degree C.

**Surface-Barrier Transistor.** The surface-barrier transistor is a specially constructed germanium device which is quite similar to the PNP junction transistor in operation. It has a lower noise figure, an excellent high-frequency response (about 50 times that of the alloy junction), and will operate at extremely low currents.

Manufacturing is by the chemical (electrolytic) etching process, which produces cavities on opposite sides of a thin, pure N-type germanium wafer. Then the same process is reversed to electro-deposit metailic electrodes in these cavities. The thin base region (about .0002 inch) helps produce the excellent high-frequency response, and the etching and plating processes provide excellent control of transistor characteristics. Junction alloy transistors use ohmic

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non-rectifying contacts to the semiconductor. The surface-barrier transistor uses metal electrodes which are excellent rectifiers and operate efficiently as collectors or emitters for the minority carriers. The collector electrode is made larger than the emitter electrode to provide a high current gain. Operation depends upon the surface-barrier effect; that is, the electric field which exists at the surface of the germanium excludes both holes and electrons from a thin region near the surface. The addition of the metal electrode to the germanium produces a concentration of holes (minority carriers) directly under the surface. Forward-biasing of the emitter attracts the holes to the region between the electrodes, and reverse-biasing of the collector provides a means of collecting the holes as they diffuse across the thin base region.

The following illustration shows a typical CB amplifier arrangement using SBT transistor and indicates the operating voltages and gains. A voltage gain of 190 is realized, with an overall power gain of 159.



**Typical SBT Common-Base Circuit** 

**PNIP-NPIN Transistors.** These transistors operate and are connected similarly to the conventional type transistor. Their basic difference is in construction; an intrinsic area is inserted between the base and collector areas. The over-all result is to reduce the base-to-collector capacitance and permit higher-frequency operation (on the order of 900 MHz maximum).

**Drift Transistor.** This transistor uses a construction which gradually changes the resistivity of the semiconductor from a highly conducting material at the emitter to a more **resistive** material (nearly pure germanium) at the collector. When a potential is applied between the emitter and collector, an electric field effect is produced which causes the internal carriers to drift across the junctions at high velocity, instead of relying upon diffusion effects. Thus, the drift transistor can be operated at higher frequencies than the normal junction transistor.

The impurity concentration gradient for a typical drift transistor is shown in the following figure. It is also representative of the resistivity gradient and the electric field produced, which vary in the same manner. Because of the variable impurity distribution in the base region, less of the depletion area extends into the base, and the total effect is that of widening the depletion area. Shorting of the transistor by punchthrough effect as the collector voltage is raised is eliminated, because the depletion area will gradually extend into the base and collector areas and be blocked by the heavy impurity concentration near the emitter region, limiting further spread to the collector region. At the same time, the strong electric field produced, by the varying resistivity gradient from one end to the other of the transistor causes an attraction for the minority carriers and thus urges injected holes across the base region in the same direction as the diffusion currents. The result is to provide a shorter transit time for the injected carriers than would normally occur for the same base width if only the diffusion process were acting as a transport medium. With a shorter transit time, the highfrequency response is extended above that of the normal transistor.



**Drift Transistor Construction** 

**Diffused-Base (MESA) Transistor.** The diffusedbase transistor utilizes manufacturing processes to produce a physically thin diffused-base alloy on a basic germanium bar. Thus the collector-base capacitance is reduced, and the slowness of the diffusion process through the base region is minimized. Better high-frequency response results.

Silicon Controlled Rectifier, The silicon controlled rectifier is a silicon 3-junction, 3-terminal device. It is the semiconductor equivalent of the thyratron tube. It can be either a PNPN or a NPNP unit. In the PNPN unit, the anode is the P terminal and the cathode is the N terminal. The internal N region is not connected externally, but floats between the anode and the second P region or external gate terminal (see the following figure).



Silicon Controlled Rectifier

The controlled rectifier is connected as a conventional rectifier with anode to positive and cathode to negative. In this condition, both end junctions are forward-biased, but the middle junction is reversedbiased, and only a small reverse current flows (conduction is effectively blocked). When a positive gate, is applied to the gate electrode, the middle junction is forward-biased and heavy current flows; or, when a specific blocking voltage is exceeded, the silicon controlled rectifier also breaks down and operates exactly as if gated. Once conduction is initiated, it continues until either the current or the voltage drops below a small holding value or until the external circuit is interrupted. Following is a typical circuit utilizing two controlled rectifiers in a full-wave rectifier circuit. The output level is determined by the control circuit. These units are operable over ranges of from 20 to 600 volts blocking and currents of 1 to over 100 amperes, under control of gates from less than 1 volt at 1/4 milliampere to 3 to

4 volts at 10 milliamperes, with turn-on time of 1 to 5 microseconds and turn-off times of 10 to 20 microseconds.



**Controlled Rectifier Circuit** 

**Phototransistors.** The phototransistor is a **combi**nation of two junction diodes arranged as a conventional transistor, for example, in a PNP configuration, with only the two end leads brought out. The mechanical arrangement is such that light is focused on either one or both junctions to vary the conductivity of the unit. This unit is identical in operation to the photodiode, except that it is much more sensitive, from 50 to 500 times, because of transistor action.

The following figure shows that the connections are the same as for the photodiode and that the emitter junction is reverse-biased, with the collector junction forward biased and the base floating. Biasing is achieved through the internal resistance of the junctions. The emitter is more negative than the collector, and the base floats somewhere in between, being at a lower positive potential than the collector, so that it is effectively reverse-biased (assuming a PNP unit). Since the base is truly floating (it is not connected to any input or returned to ground except through the internal base-emitter resistance), it is extremely susceptible to any light impinging on the junction. Variations in light intensity cause the junction conductivity to vary, and thus act similarly to an input signal applied to a conventional emitter-base junction. Since the collector junction is forwardbiased, the changing emitter conductance causes corresponding and amplified changes of collector current, developing an output across load resistor R<sub>1</sub>.



**Phototransistor Circuit** 

Because of the large collector current control offered by the phototransistor, it may be used directly to control a relay connected to turn power on or off, or to operate a switching circuit; see the following figure.



Phototransistor Relay

The phototransistor is subject to humidity and temperature changes like the photodiode. Humidity effects are dependent upon the construction and encapsulation processes, but temperature variations may be compensated for by the use of a bridge circuit and a thermistor of equal but opposite characteristics. See the following illustration.

**Thermistor.** A thermistor is a special semiconductor device which functions as a thermally sensitive resistor whose resistance varies with temperature. Thermistors have large negative temperature coefficients; that is, as the temperature rises their



**Thermistor-Compensated Bridge Circuit** 

resistance decreases, and as the temperature drops their resistance increases. The resistance of a thermistor is varied not only by ambient temperature changes but also by heat generated internally by the passage of current.

Since the thermistor is basically a variable resistor, it is usually constructed from semiconductor material of greater resistivity than is used in transistors or semiconductor diodes. Therefore, its response to ambient temperature variations does not track equally with that of the transistor semiconductor, so that compensation is achieved only at a few points of correspondence. As a result, its greatest usage is in the field of temperature controls and measurements, and power-measuring equipment based on heating effect, such as r-f measuring microwave equipment. Although it is a semiconductor, it has no intrinsic amplification capability like the transistor, and is mentioned in this technical manual only because it is used in thermal compensating circuits for transistor stabilization.

**PNPN Switching (Four-Layer Diode).** The fourlayer diode is a two-terminal device which operates in either of two states; an open, or high-resistance, state or a closed, or low-resistance, state. It is effectively an on-off switch which can be employed as such in switching circuits, or it may be used as a relaxation oscillator or multivibrator. In the non-conducting state it presents a resistance on the order of megohms, and in the conducting state it presents a low resistance of about 200hms. The following figure shows typical biasing polarity with the  $P_{-end}$  connected to positive and the  $N_{-end}$  connected to negative, a



**PNPN Diode Bias Conditions** 

forward-biased condition. The internal NP junction, then, is reverse-biased and held in an almost nonconducting condition; this is the resting open-circuit, or high-resistance, condition. As the bias voltage is increased, it reaches a point which produces a condition similar to avalanche breakdown in the internal junction, and heavy current flows. Since there is no connection to the internal junction except through the other semiconductor material, there is a small minimum resistance at full current flow; this is the closed-circuit, or low-resistance, condition.

A basic switching diode circuit is shown in the following illustration.



**Basic Switching Diode Circuit** 

**Tunnel Diodes.** Basically the tunnel diode is a PN junction formed of a semiconductor mixture which is

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impregnated with more than the normal amount of impurities. The resulting crystrd has current-voltage transfer properties which are different from those of the normal diode junction.

The following figure shows a typical diode transfer characteristic plotted as a dashed line, with the tunnel diode characteristic superimposed in the form of a solid line. Note that diode forward current increases with applied forward-bias voltage until point A is reached, then it reverses itself and decreases with increase of applied voltage to point B; between points B and C the curve is similar to that between O and point A. The region of operation between points A and B is a negative-resistance region over which the diode may be used on an amplifier or oscillator, since negative-resistance devices are capable of supplying power to the source instead of absorbing power from it.



**Tunnel Diode Transfer Characteristics** 

The tunnel diode is also of value in switching circuits. Because three or more regions of operation are possible, it is only necessary to select the proper bias and load line to achieve different types of operation with the same circuit. A basic switching circuit utilizing the tunnel diode for three different functions is shown in the following illustration. Under condition A the load line is adjusted so that it intersects the characteristic curve at three points; two are in the positive-resistance region and the third is in the negative-resistance region. Application of a positive pulse turns the diode on, and application of a negative pulse turns it off; thus the circuit operates as an off-on multivibrator. Under condition B the diode

is operated in the positive-resistance region and functions as a one-shot multivibrator, producing a rectangular puke for each trigger pulse. Under condition C the diode load line is set so that it never intersects the positive regions of the characteristic curve, and the circuit operates in an eatable condition as a freerunning multivibrator. The tunnel diode can operate at frequencies up to 1000 MHz at high switching speeds and appears particularly adapted for computer applications.



**Tunnel Diode Operating Characteristics** 

Transistor Junction Symmetry. The low conduction resistance and low leakage currents of the fused junction transistor permit many applications using the transistor as a controlled switch. In the conducting condition these switches present a resistance of only a few ohms, and when cut off they offer impedances or resistances of hundreds of thousands of ohms to many megohms. Where the voltages and currents to be controlled are small, the inverted transistor connection offers slightly improved 'but different operating conditions. To provide the inverted comection the emitter and collector connections are interchanged (inverted), Thus, the element which normally functions as the collector now functions as the emitter, and the element which normally

functions as the emitter now operates as the collector. The changes in characteristics provided by these changes in circuit connections make it necessary to consider the inverted transistor as a special device. Such devices are especially useful in circuits where a reversal of normal current flow is desired by merely changing the applied emitter and collector polarities.

Normal transistors are manufactured with a collector of larger size than the emitter to obtain a high value of current gain (alpha). The larger collector makes certain that most of the minority carriers diffused through the base region are collected despite any radial spreading, thereby improving the overall gain. On the other hand, either the collector or the emitter can emit minority carriers into the base region, while the other electrode functions to collect these carriers (both P-elements are composed of the same material). Because of the differences in area, when the normal collector operates as an emitter and the normal emitter operates as a collector a different value of converted current gain is obtained over that of the normal current gain. While it is possible to construct transistors with symmetrical or equal current gains in either direction, the maximum normal gain would be reduced. When the emitter of a normal transistor is reverse biased, the emitter leakage current with the collector open is usually lower than the collector leakage current with the emitter open because of the smaller size of the emitter.

Thus, we can define the two types of gain possible with the normal and inverted connection (normal alpha and inverted alpha). Most commercial transistors have a normal rdpha of 0.9 to 0.999 but the inverted alpha is only from 0.3 to 0.6. Since the collector leakage current and the emitter leakage current are not independent, but are related by the alpha gain times the leakage current, the emitter leakage current can vary over a range of from 0.3 to 0.699 the value of the collector leakage current. Consequently, as the normal alpha gain is higher than the inverted alpha gain, we find that higher current gains and power handling capabilities are available from the normal transistor connection. Any advantage of the inverted connection is mainly obtained when the inverted connection is used to control low power levels. That is much lower spurious signrds are generated due to the switching action than at the higher normal levels; also higher ambient temperature levels (up to 30 degrees centigrade) are possible

because of the lower operating temperatures. Another advantage is that reversed current flow may be obtained from the same transistor by simultaneously reversing the emitter and collector polarities. The inverted connection will also provide extremely linear detection in the millivolt region.

When analyzing the operation of switching transistor circuits, it is helpful to bear in mind that a transistor will conduct in either direction as long as the base voltage is such that either junction is biased in the forward direction. The transistor will always be cut off when the base voltage reverse-biases both junctions. Hence, if the P-materials at each end of a PNP transistor were equal in physical area, the current flow in either direction through the transistor would be equal if the emitter and collector polarities were reversed. Since, however, the physical areas are different, using the inverted connection results in different values of current flowing in opposite directions, but the general statement still holds. As long as the bias on one element is reversed, the base bias controls current flow through that element, since the other element is always forward biased. This is the normal condition of operation for a transistor. When emitter and collector leads are interchanged, or their polarities are reversed, the physical construction governs the maximum current flow, and the collector then becomes the emitter, with the emitter operating as the collector. Consequently, reduced gain is obtained and the characteristics are different than normal.

## PART 13-2. LIMITERS

## SERIES, POSITIVE OR NEGATIVE LOBE DIODE LIMITER (ELECTRON TUBE)

#### Application.

**The series** limiter is used in communications equipment as a speech clipper, in electronic equipment where amplitude limiting is desired (such as FM receivers or transmitters) and in waveshaping circuits where all or a portion of the positive half-cycle of a waveform is to be clipped off. This circuit is particularly suited for squaring off a peaked waveform. It is used universally in display circuits for modifying waveforms and determining the levels at which they are clipped or limited.

#### Characteristics.

Input signal waveform contains both positive and negative signals.

Output amplitude is lower than input amplitude; no amplification is realized in the circuit.

Output amplitude is lower than input amplitude; no amplification is realized in the circuit.

Output signal is taken across a load resistor.

Output signal is in phase with input signal.

#### **Circuit Analysis.**

**General.** The series, positive or negative lobe diode limiter consists essentially of a diode connected in the signal line, in series with the signal source and the load, and polarized so that either the negative portion or the positive portion of the input signal will pass through the diode without being affected. A load resistor is connected on the load side of the diode, and the output signal is taken across this resistor. Due to the similarity between the positive lobe limiter and the negative lobe limiter, only the positive lobe limiter will be discussed in detail, with the differences being noted at the end of the discussion.

Circuit Operation. A simplified series, positive lobe diode limiter is shown in the following illustration. In this circuit, the diode conducts during the negative portion of the input signal. Conduction is accomplished' by driving the cathode negative with respect to the plate, which has the same effect from the viewpoint of the tube electrodes as driving the plate positive with respect to the cathode. When the input signrd goes negative, the diode conducts, and it presents a low value of resistance to the signal. The total resistance in the circuit, connected across the input terminals, then consists of diode VI, which has a low resistance, in series with load resistor R1, which has a comparatively high resistance. Since the voltage drop across each individual resistance in a series circuit is in direct proportion to its resistance divided by the sum of the resistances, according to Kirchhoffs laws, most of the input signal voltage will appear across load resistor R1, while a small amount will drop across diode VI and be lost insofar as the circuit output is concerned. For this reason the value of the load resistor, R1 should be many times greater than the forward resistance of the diode, VI. When the input signrd goes positive, the diode cuts off and thus limits the flow of current in the series circuit.

The voltage across load resistor RI then falls suddenly to zero, and remains at zero until the input signal goes negative on the following half cycle.



## Simplified Series, positive Lobe Diode Limiter and Input-Output Waveforms

The value of load resistor R1 affects the output of the circuit in several ways. First, for the best frequency response characteristic, RI should be as low as practicable. But in order for the circuit to function to the best advantage as a limiter, the load resistor must be severrd times the value of the forward, or conduction, resistance of the diode. The effect of various values of load resistance on the output voltage, for three characteristic tube types at V1 in the previous circuit, are shown in the following table. The three tube types are all twin-diodes, and have different values of forward resistance. The forward resistance, or resistance during the period of conduction, of a single section of each of the tubes is as follows: 6AL5, 250 ohms; 6X5, 500 ohms; 6H6, 750 ohms. The values of output voltage are listed, assuming an input voltage of 10 volts to the circuit, with the polarity of the voltage such that the diode V1 conducts to the maximum value (10 volts) on the negative half cycles.

Value of R1	Tube Type 6AL5 (250 ohms fwd res)	Tube Type 6X5 (500 ohms fwd res)	Tube Type 6H6 (750 ohms fwd res)
IK	8.0	6.66	5.71
5K	9.52	9.08	8.69
10K	9.75	9.52	9.30
50K	9.95	9.90	9.85
100K	9.97	9.95	9.92

Output Voltage of Diode Limiter Using Various Tubes and Load Resistances, at 10 Volts Input It can be seen, from the table above, that with a load resistance of IOOK, which is 400 times the value of the forward resistance of a type 6AL5 tube, practically the entire input voltage is available at the output of the limiter, with only 0.3 volt circuit loss occurring within the tube.

A simplified series, negative lobe diode limiter is shown in the following illustration. In this circuit, the diode conducts during the positive portion of the input signal. When the input signal goes positive, the diode presents a low vrdue of resistance (called the forward resistance) to the signal, and passes the signal through the circuit to the output. The remainder of the circuit operation is essentially the same as the description given above for the positive lobe limiter.



## Simplified Series, Negative Lobe Diode Limiter and Input-Output Waveforms

One application of the series, negative lobe diode limiter is given in the following illustration, which shows a series-connected peak noise limiter for use in an AM receiver. This circuit operates as follows: Assume that an input audio level (rectified dc from a diode rectifier applied between point *a* and ground of -10 volts is applied to the input terminals of the circuit. The cathode of diode VI is connected to point c and assumes a potential through resistors R3 and R4 of -10 volts with respect to ground. (Since no appreciable current flows through R3 and R4 there is no appreciable voltage drop across them.) The plate of diode VI is connected to point b and, with no current flowing, assumes a potential -5 volts with respect to ground, through the voltage-divider effect of resistors R1 and R2. The plate of the diode (point b) is thereby momentarily 5 volts positive with respect to its cathode (point c); under these conditions the d diode conducts, and its resistance becomes approximately 2000 ohms. Capacitor Cl is connected to

point d and charges through resistor R3 to a potential of approximately -7 volts with respect to ground when the diode resistance is 2000 ohms. Any considerable change in this potential would require approximately 0.1 second, because of the time constant of R3 and Cl.



Series, Negative Lobe Dioda Limiter Used in a Noise Limiter Circuit

If a noise voltage of -100 volts suddenly appears at the input to the circuit (point a) across R1 and R2. the plate of the diode (point b) will assume a poten-" tial of -50 volts instantaneously, while its cathode (point c) remains at -7 volts due to the time delay of the **R-C** circuit R3C1. This makes the plate of the diode 43 volts more negative than its cathode, and the resistance of the diode becomes almost infinite. This effectively disconnects point c and audio output capacitor C2 from point b, and the circuit momentarily has no output except that small value which passes through R3 and R4, shunted to ground at their junction point by Cl, and also shunted by the capacitance of the diode. By the time the momentary noise pulse has decayed, the cathode of the diode will have assumed a potential considerably more negative than its plate (due to its connection to point a, through R4 and R3), and will again conduct the audio input signal from point **b** to point c and the output capacitor, C2.

The time period during which the circuit limits a noise pulse depends upon the R-C time constant of R3 and Cl, while the percentage of the audio input voltage which is available at the output of the circuit depends upon the relationship of RI and R2. The

actual values of these components that may be encountered in a particular circuit depend upon the intended use and application of the circuit.

## Failure Analysis.

**No Output.** Because of the relative simplicity of the series, positive or negative lobe diode limiters, the analysis of failure is likewise simple. The failure of either component will cause trouble, but only the failure of the diode would be responsible for a no-output condition. Obviously, the failure of the applied signal at the input to the limiter should be suspected if no output is obtained from the limiter.

When the series, negative lobe diode limiter is used in a more complicated circuit, such as the noise limiter shown in the illustration, a few additional components could be responsible for no output. If RI became open-circuited or if output coupling capacitor C2 became open-circuited no output would be realized from the circuit. (If R1 became opencircuited, there is a possibility that some small value of the input signal, without limiting, would be obtained through R3 and R4, depending upon the particular input waveform.) If capacitor Cl became shorted, the cathode of the diode would be at ground potential and, since the plate of the diode is at a negative potential, the diode would be cut off; thus, no output would be obtained from the circuit. In any case, an analysis of the particular circuit would be necessary in order to isolate the faulty component.

Reduced or Unstable Output. In a series, positive or negative lobe diode limiter, a reduced value of output would most likely be due to a diode which has poor cathode emission, and therefore has a high internal, or forward, resistance. It is also possible, although less likely, that the load resistor may have decreased in ohmic value because of age or overload. If, however, the cathode emission of the diode falls off, its internal resistance will increase, and the end result will be a decrease in the output voltage. This can be seen from the previous table, which shows the dependence of the output voltage upon both the load resistance and the diode used. Consulting the table, suppose that the circuit comprised one section of a type 6AL5 diode and a IK load resistor. With a 10-volt input, the output may be expected to be on the order of 8 volts, since the 6AL5 has approximately 250 ohms forward resistance. If, however, the cathode emission decreased to the extent that the

forward resistance increased to 500 ohms (comparable to that of the type 6X5 diode), the output will also have decreased to approximately 6.66 volts, comparable to the output of the 6X5 under its normal operating conditions.

In the application of the series, negative lobe diode limiter shown in the illustration, a leaky capacitor Cl could cause both a reduced and a distorted output, while a substantial change in the value of either R3 or R4 could be the cause of distorted output, as could also a shorted coupling capacitor C2. Since the output voltage is dependent upon the comparative vahres of RI and R2, a change in the value of either R1 or R2 will affect the circuit output. If RI should increase in value, the output voltage will decrease, while if R2 should increase in value, output voltage will increase. An open capacitor Cl will prevent the circuit from limiting and, as a result, noise pukes will be present in the output; furthermore, some slight increase in output may be noticed.

## SERIES, POSITIVE OR NEGATIVE LOBE DIODE LIMITER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version.

#### Circuit Analysis.

**General.** A limiter circuit is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sine-wave signal, to eliminate the positive (or negative) portion of a waveform, or to keep the input amplitude to an FM detector at a constant value. The positive-lobe limiter is designed to effectively eliminate or reduce the positive portion of the input signal. The negative-lobe limiter eliminates or reduces the negative portion of the input signal. Due to the similarity between these two circuits, the following discussion will pertain primarily to the positive-lobe limiter. A short discussion of the negative-lobe limiter will be made at the conclusion, explaining the differences.

**Circuit Operation. A schematic** diagram of a typical series-diode positive-lobe limiter is shown in the accompanying figure.



Series-Diode Positive-Lobe Limiter

As can be seen, diode CR is connected in series between the input and output, with R1 serving as the load resistor, When a positive input is applied between the cathode and ground, the cathode is made more positive than the anode, and the diode does not conduct. Thus, for this condition only the reverse resistance of the diode (which will be discussed later) will allow any signal to pass to the load. When the input signal is negatively polarized, the cathode is more negative than the anode and the diode conducts. When the diode conducts, electrons flow opposite the direction of the arrow through R1 to ground, and the polarity of the voltage developed across R1 is negative with respect to ground, as shown in the illustration. The amount of current flow and the resistance value determine the output voltage produced. Since the forward resistance of the diode is in series with R1 to ground, together they form a voltage divider and the output voltage taken across R1 is always less than the input voltage. (The loss (voltage drop) produced by the forward resistance is shown in dotted lines on the negative portion of the waveform and identified by the symbol  $\mathbf{v}_{\mathbf{f}}$  in the illustration.) Also since the load resistor is not frequency-selective, the waveform of that portion of the signal produced by forward current flow through the resistor is the same as the waveform of the original signal (except where clipped) and of the same phase. The polarity, of course, is rdways negative. In forward conduction, the diode can be considered as a switch which connects the output to the input. Since the diode is a semiconductor, it introduces a slight amount of resistance, usually not more than 10 ohms, in series with the circuit. When the diode is nonconducting, its reverse resistance is relatively high (50K to 1 megohm, or greater), but finite (unlike the electron-tube reverse resistance which is usually infinite). In most applications, the reverse-resistance

vrdue is high enough to have little effect on circuit operation, but in a series limiter its effect may be important. The following figure shows the equivalent circuit for a diode limiter with a back resistance of 50K, plus a load resistance of 50K. As is clearly evident from the figure, the diode resistance, R1, and the load resistor,  $R_1$ , form a voltage divider across the input. Even though the diode is not conducting, in the forward direction, the small leakage current which flows through the diode reverse resistance causes it to act as a voltage divider with R1. As a result, half the applied input voltage appears in the output circuit. This illustrates the serious disadvantage of semiconductor limiters. As shown in the figure, the positive portion of the waveform is only partially clipped, whereas in a vacuum-tube circuit the entire positive waveform would have been eliminated. One of the practical results of this reverseresistance effect is that diodes of one type cannot be replaced with those of another type (even though voltage and current ratings may be adequate) unless their reverse resistances are similar. Otherwise, the amount of limiting or clipping will be different from the amount selected by the designer, and improper functioning of following circuits can occur.

ished by an amount equal to the ratio of the resistance of the diode and the load resistor, or one ten-thousandth. It is clear from this example that the forward resistance of the semiconductor diode is low enough to produce even less loss than that of the electron tube diode, which is never less than 100 ohms and is usually more. (Practically speaking, 250 ohms is the average low value with the high value being on the order of 500 to 700 ohms.)

The amount of clipping of the input waveform can be selected by using a diode which has the proper value of reverse resistance, or by placing a negative potential (E<sub>bb</sub>) in series with RI, as shown in the following figure. In the latter case, the diode will not conduct until the input signal is more negative than the applied bias  $(V_R)$ . Thus the reverse resistance loading of the diode on the input circuit is effectively nullified (the reverse resistance voltage divider action with R1 is eliminated). The complete positive lobe, in this case, is eliminated. Note, however, that the voltage divider action produced by the forward resistance and RI still remains, as indicated by v in the figure. The total negative signal amplitude is reduced by the amount of forward voltage drop and the effective negative bias.



**Reverse-Resistance Equivalent Circuit** 

Consideration of the equivalent circuit, in the preceding figure, during forward-resistance conditions reveals why the output waveform can never have the same value as the input signal. If the forward diode resistance is assumed to be 5 ohms and the load resistance 50K, then the input signal will be dimin-



#### **Bias Control of Clipping**

A schematic diagram of a typical series-diode negative-lobe limiter is shown in the accompanying illustration.

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Series-Diode Negative-Lobe Limiter

The circuit operation is the same as that of the positive-lobe limiter described above, except that all signal polarities are reversed due to the reversal of the diode in the circuit.

## Failure Analysis.

**No Output.** A no-output condition can be the result of either an open-circuit condition (a defective diode, or open connection) or a short-circuit condition (RI shorted). A resistance check of the diode and load resistor will quickly reveal the defective component.

Low Output. Lack of sufficient input signal, as well as a defective diode, can cause low output. A change in value of the load resistor with age, although not very likely to occur, can also cause a reduction of output. If the diode is biased, a change of bias voltage can cause improper output. In either case, a resistance check will determine whether the components are defective, and a voltage check will determine whether the bias is correct. Be certain to observe the proper polarity when checking the diode with an ohmmeter; otherwise misleading results will be obtained.

**Distortion.** Except for the clipping effect, a diode limiter produces no inherent distortion. If a distorted waveform is obtained, check the input with an oscilloscope to determine whether the input signal is distorted. The negative portion of the output waveform should be identical to the negative portion of the input signal; if it is not, the diode is defective. Another possibility is that the circuit following the limiter introduces distortion by feeding back an out-of-phase signal. In some cases, it may be

necessary to disconnect the limiter output to determine whether such feedback exists.

## PARALLEL, POSITIVE OR NEGATIVE LOBE DIODE LIMITER (ELECTRON TUBE)

## Application.

The parallel limiter is used in communications equipment as a speech clipper, in electronic equipment where amplitude limiting is desired (such as FM receivers or transmitters) and in waveshaping circuits were all or a portion of the positive half-cycle of a waveform is to be clipped off. This circuit is particularly suited for squaring off a peaked waveform. It is used universally in display circuits for modifying waveforms and determining the levels at which they are clipped or limited.

## Characteristics.

Input signal may contain both positive and negative signals. In special cases "it may contain only positive or negative signals, in which case only those of higher amplitude will be limited, or clipped.

Output waveform contains only negative or positive signals, or signals which are less positive or less negative than a predetermined limiting level.

Output amplitude is lower than input amplitude; no amplification is realized in the circuit.

Output is taken across a diode.

Output signal is limited when the diode conducts.

## Circuit Analysis.

**General.** The parallel, positive or negative lobe diode limiter circuit consists of a diode and a resistor connected in series with each other across the input signal. The diode is polarized so that it will conduct during the positive or negative portions of the input signal. The output signal is taken across the diode tube and is produced during the period that the diode does not conduct. Due to the similarity between the positive and negative-lobe limiters, only the positivelobe limiter will be discussed in detail. The negativelobe limiter will be discussed only briefly at the end of the discussion.

**Circuit Operation.** A simplified parallel, positive lobe diode limiter is shown in the following illustration. In this circuit, the diode, VI, conducts only during the positive portion of the input signal. When

the input signal goes positive, the diode conducts, and its internal (or conduction) resistance drops from an infinite resistance, when nonconducting, to a vahre of approximately 500 ohms. Since the resistance value of resistor R1 is very large compared to the conduction resistance of the diode, practically the entire value of the input voltage drops across load resistor R1, while only a very small voltage drops across diode V1. This voltage may become negligible when the ratio of the load resistance RI to the diode resistance is very high. Some value of voltage, however small, will still exist across diode VI, because any diode has some measurable amount of resistance. This value of voltage is shown in the output waveform as  $E_{y}$ , on the positive side of the zero-voltage baseline, and represents a loss in the circuit because the output contains this unwanted amount of positive signal. When the input signal goes negative, the diode does not conduct, and the current flow through R1 is interrupted (except for that infinitesimal current which flows through RI because of the high resistance of the load connected to the output terminals). With no (or almost no) current flowing through RI there is no voltage drop across Rl; hence, the output voltage is equal to the input voltage. It should now be obvious that the load impedance connected to the output terminals should be as high as possible in order to obtain the highest possible voltage at the output terminals. The actual value of the output voltage in the previously illustrated circuit during the negative half cycle of the input signal (neglecting the source impedance of the input signal, and assuming that the resistance of the diode when nonconducting is infinite) may be calculated by applying Ohm's law according to the proportion:

where:  $E_0: E_1 = R_0: R. + R1$   $E_0 =$  output voltage of circuit  $E_1 =$  input voltage to circuit R. = output load resistance (impedance) R1 = limiter load resistor

The proportion above can be restated and solved for  $E_0$ , as follows:

$$\mathbf{E}_{\mathbf{o}} = \begin{bmatrix} \mathbf{E}_{1} \\ \mathbf{R}_{1} \\ \mathbf{R}_{2} \end{bmatrix}$$

It can be seen from the above formula that the output voltage  $(E_{\circ})$  will be approximately equal to the input voltage (El) when the output load resistance

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 $(R_{\circ})$  is very large compared to the resistance of the limiter load resistor, **(R1)**.



## Simplified Parallel, Positive Lobe Diode Limiter and Input-Output Waveforms

A parallel, positive lobe diode limiter maybe used to limit only the peaks of the positive waveform, while allowing a given value of the positive signal to pass through the circuit to the output. This may be accomplished by applying a biasing voltage, having a value equid to the value of the positive signal to be passed by the circuit, to the cathode of the diode, as shown in the following illustration. The biasing, or limiting, voltage may be obtained from a battery, as shown in the illustration, or from a tap on a bleeder resistor connected in the output circuit of a d-c power supply. When connected as shown in the illustration, with the cathode of V1 connected to the positive terminal of the d-c source, the cathode of the diode is held more positive than the plate by the value of E in the absence of an input signal. As long as the positive cycles of the input voltage remain less positive than El, the bias voltage of the battery, the diode remains nonconducting, and the output voltage is approximately equal to the input voltage. Since all of the negative cycles of the input voltage are less positive than E, these too cause the diode to remain nonconducting, with the result that the output voltage is approximately equal to the input voltage. When the input signal increases to a value which exceeds the voltage of E<sub>1</sub>, the diode conducts during that portion of the positive cycle when the input voltage is greater than El. During this period of conduction, the output voltage of the circuit is equal to the value of  $E_{\mu}$ (on the positive cycle), while the peak of the positive input cycle which exceeds the value of E is clipped,

or limited, appearing as a voltage drop across the diode load resistor R1.





An application of the positive peak limiter is shown in the following illustration. In this circuit an input timing pulse having a pulse duration of approximately 5 microseconds and an amplitude of +120 volts, from a radar transmitter, is applied through a diode limiter to a sweep generator circuit, to produce the sweep presentation on an indicator scope. The diode limiter, which is a parallel, positive lobe diode limiter, is used to provide a fixed pulse amplitude of +38 volts output to the sweep generator circuit. This is accomplished by applying a fixed bias potential of +38 volts to the cathode of diode V1, from a voltage divider composed of R2 and R3 connected to a +400-volt power supply. When the input signal rises to a potential more positive than +38 volts, V1 conducts, and its resistance (conduction resistance) drops to a very low vrdue. Since the cathode is held at a potential of +38 volts and the resistance of V1 is negligible, the potential at the plate of V1 is also +38 volts, while the remainder of the +120-volt input pulse appears as a voltage drop across the plate load resistor, R1. The +38-volt pulse, which comprises the output of the limiter stage, is coupled through capacitor C2 to the following (sweep generator) stage. The output potential is thus held, or limited, to a maximum of +38 volts, regardless of how large the value

of the pulse is at the input to the limiter circuit. If, however, the input pulse decreased to a value less than +38 volts, the entire pulse would be passed through the circuit to the output, and no limiting would occur. In this event the voltage at the plate of the diode would be less positive than the voltage at the cathode, and the diode would not conduct.





A parallel, positive lobe diode limiter may also be used where it is desired to limit not only the entire positive peaks of the input signal, but also a predetermined level of the negative peaks, in order to furnish an output only when the negative peaks exceed this predetermined level. This may be accomplished by applying a biasing voltage to the cathode of the diode, equal to the value of the predetermined level, but of opposite polarity to that of the preceding circuit, as shown in the following illustration. In this circuit a negative potential E is applied to the cathode of diode V1, from a battery or power supply. With the cathode negative with respect to the plate, the diode is maintained in a conducting state in the absence of an input signal, and the output voltage is held at a steady (negative) dc level equal to E<sub>1</sub>. With an input signal applied to the circuit, the output voltage will continue to be held at this steady dc level, with the input signal appearing across the diode load resistor, RI, until the input signal becomes more

negative than  $E_{\mu}$ . When this point is reached, the diode will no longer conduct; its resistance will then have increased to an infinite value. As a result, the input signal, which previously appeared across R1 because RI was much greater in resistance than diode V1, now will appear across VI and the output terminals of the circuit, since V1 is now **much** greater in resistance than RI. The output signal, therefore, contains ordy the negative peaks of the input signal which are more negative than the biasing voltage,  $E_{\mu}$ .

When it is desired to limit only the negative peaks of the input signal and allow the remainder of the negative portion and all of the positive portion (if any is included) of the input signal to pass, unmodified, to the output of the limiter, the circuit shown in the following illustration may be used. Once again, the circuit operation is the same as that of the previously discussed positive-lobe diode limiter, except that the polarities at the output are reversed due to the reversal of the diode and the battery voltage in this circuit.



## Parallel, Positive Lobe Diode Limiter Used to Pass Negative Peaks

The circuit of a simplified parallel, negative lobe diode limiter is shown in the following illustration. The circuit operation is the same as that of the previously discussed positive-lobe diode limiter, except that the polarities at the output are reversed due to reversal of the diode in the circuit.



Simplified Parallel, Negative Lobe Diode Limited and Input-Output Waveforms

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Parallel, Negative Lobe Diode Limiter Used es a Negative Peak Limiter

An application of the negative peak limiter is shown in the following illustration. This circuit is used as a noise limiter following the diode detector stage in an AM receiver. The output of the detector is a negative audio signal having a maximum value of 0.2 volt rms, and this signal is applied to the input of the peak noise limiter. The resistors, R1 and R2, are connected as a bleeder to a negative 150-volt power source. The -10 volts obtained at the junction of R1 and R2 due to the voltage divider action is applied as a fixed bias to the plate of the parallel diode limiter, V1. Under normal conditions the input signal is passed through coupling capacitor Cl to the output terminals, unaffected by V1 and its associated circuit. When a noise pulse having a peak amplitude exceeding -10 volts (the value of the fixed bias applied to VI) appears at the input terminals, diode VI conducts, placing an effective short circuit across the output terminals for the duration of the noise pulse. The noise pulse is conducted to ground through the

low resistance of V1 (when in a conducting state) and the low reactance offered by C2 to a sharp noise pulse. Since the noise pulse is shorted to ground, the pulse is prevented from activating the agc circuit, which would in turn block the i-f amplifiers and interrupt the output signal for a much longer time interval than the actual time duration of the noise pulse.



## Parallel, Negative Lobe Diode Limiter Used as a **Peak Noise Limiter**

#### Failure Analysis.

No Output. In a parallel, positive lobe diode limiter circuit similar to those shown in the first two illustrations, the analysis of failure is as simple as the circuit itself. Either the failure of the diode by shorting, or the failure of diode load resistor RI or coupling capacitor C2 by open-circuiting, or the failure of the applied signal are the only possible causes of a no-output condition.

When the parallel, positive lobe diode limiter is used in a more extensive circuit, such as in the radar indicator circuit shown in third illustration, some of the additional components could be responsible for no output. In this particular circuit, which is intended to limit positive pulses to a level of +38 volts and not to completely limit positive pulses to zero potential, a shorted cathode bypass capacitor Cl would cause complete limiting to zero (ground) potential. Since the" input contained only positive pulses, complete limiting would produce no output.

The analysis of failure which results in no output from a parallel, negative lobe limiter should also be relatively simple, because of the small number of components comprising the circuit. In the first two illustrations, for example, only three conditions could be the cause of no output. Either the diode load resistor R1 may be open-circuited, the diode V1 may be shorted, or the input signal may have failed. One other condition could contribute to no output in the second circuit illustrated, but the possibility that this condition will occur is remote. If the input signal to this circuit contained only negative pulses, the peaks of which were to be limited, and the biasing voltage E<sub>1</sub> was removed (because of battery or power supply \_ failure) or the polarity of the voltage was inadvertently reversed, then the entire negative input signal would be conducted to ground through diode V1, and no output from the circuit would be obtained. In a more complicated circuit, such as that shown in the third illustration, additional causes of no output may be an open coupling capacitor Cl, a shorted bypass capacitor C2, or failure of the biasing voltage due to either power supply failure or an open resistor R1 in the voltage divider circuit.

Reduced or Unstable Output. In a parallel, positive lobe diode limiter, a reduced value of output may be due to either an increased value of the diode load resistor R1, or the result of a change in the parallel portion of the circuit, which consists of the diode itself and its cathode biasing components when applicable. In the first two illustrations, an increased value of RI due to overheating or aging or an improper value of biasing voltage E could be the cause of reduced output. In the circuit shown in the third illustration, the failure of the applied voltage to the cathode circuit or an open-circuited resistor R2 would allow the diode to almost completely limit the input pulses (assuming they are positive pulses, as shown in the illustration), and would thus cause a substantially reduced output. If, however, the low end of the cathode voltage divider, resistor R3, became opencircuited or resistor R2 becomes shorted, the full value of the bias voltage from the power supply (+400 volts) would be applied to the cathode of V1. With a +400-volt potential on the cathode, the diode would be completely cut off, and no limiting would be realized. In this case, the output signal would be the same as the input signal.

A reduced or an unstable output from a parallel, negative lobe diode limiter may be due to a substantially increased value of the diode load resistor, RI,

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resulting from overheating or aging; an intermittently shorting diode, VI; or an erratic output from the biasing voltage supply, E, when used. In a more extensive circuit, such as that shown in the third illustration, a leaky coupling capacitor, Cl, would contribute to an unstable or erratic output. In addition, if the resistor at the low end of the bleeder supplying the biasing voltage became open-circuited (R2 in the circuit illustrated), the output of the circuit would be distorted from the normal output, in that the output would contain negative signals up to a possible negative 150-volt value, and no limiting would be obtained. If, on the other hand, bypass capacitor C2 became open-circuited, a sharp negative increment of a noise pulse applied to the input to the circuit would encounter a much greater impedance to ground through R2 than would normally be offered by C2. As a result, the decay time of the noise pulse would be increased because of R2, resulting in distortion of the output waveform.

## PARALLEL, POSITIVE OR NEGATIVE LOBE DIODE LIMITER (SEMICONDUCTOR)

#### Application.

Same application as electron tube version.

#### Characteristics.

Same characteristics as electron tube version.

#### Circuit Analysis.

General. The positive or negative lobe limiter circuit is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sinewave signal, to eliminate the positive or negative portion of a waveform, or to keep the input amplitude to an FM detector at a constant value. The positive-lobe limiter is designed primarily to eliminate or reduce the positive portion of the input signal, whereas the negative-lobe limiter is intended primarily to eliminate or reduce the negative portion of the input signal. Due to the similarity between the positive-lobe and the negative-lobe limiters, only the positive-lobe limiter will be discussed in detail here. The negativelobe limiter will be discussed only briefly at the end of the discussion.

**Circuit Operation.** A parallel, positive-lobe diode limiter is shown in the following illustration. In



Positive-Diode Positive-Lobe Limiter

this circuit, diode CR conducts only during the positive portion of the input signal. When the input signal goes positive, the diode conducts, and its resistance drops from a very high reverse resistance to a very low forward resistance. The amount of resistance of the diode in the conducting (or the nonconducting state) is determined by the internal characteristics of the particular diode selected for the circuit. Since the resistance value of R is very large compared to the conducting resistance of the diode, practically the entire value of the input voltage drops across load resistor R, while only a very small voltage drops across diode CR. This voltage may become negligible when the ratio of the load resistance R to the diode resistance is very high. Some value of voltage, however, will still exist across CR, because of its conducting resistance, called the forward resistance and is shown on the illustration as  $E_{cr}$ . When the input signal goes negative, the diode does not conduct, and current flow through R almost ceases. A small reverse current still flows through CR, because of the reverse resistance of the diode and thus a small portion of the input voltage is dropped across R. The amount of reverse resistance of the diode depends upon the characteristics of the diode selected. Thus, this is one of the disadvantages of the semiconductor diode over the vacuum tube. The vacuum tube reverse resistance is considered to be infinite, whereas the semiconductor is finite. The voltage dropped across R subtracts from the output, and thus the gain of the limiter is less than unity. On the other hand, the forward resistance of the semiconductor is less than that

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of the vacuum tube, making the semiconductor better in some applications.



## Parallel, Positive Lobe Diode Limiter Used as a Positive Peak Limiter

A parallel, positive-lobe limiter may also be used to limit only the peaks of the positive waveform, while allowing a given value of the positive signal to pass through the circuit to the output. This may be accomplished by applying a biasing voltage, having a value equal to the value of the positive signal to be passed by the circuit, to the cathode of the diode, as shown in the following illustration. The biasing, or limiting, voltage may be obtained from a battery, as shown in the illustration, or from a tap on a bleeder resistor connected in the output circuit of a dc power supply. When connected as shown in the illustration, with the cathode of CR connected to the positive terminal of the dc source, the cathode of the diode is held more positive than the anode by the value of  $E_1$ in the absence of an input signal. As long as the positive cycles of the input voltage remain less positive than El, the battery bias voltage, the diode remains essentially nonconducting, because its cathode is positive with respect to the anode and the output voltage is equal to the input voltage minus the voltage developed by the reverse resistance of the diode. Since all of the negative cycles of the input voltage are less positive than El, these too cause the diode to remain essentially nonconducting, with the result that the output voltage is again equal to the input voltage minus the voltage developed by the reverse resistance of the diode. When the input signal increases to a value which exceeds the voltage of  $E_1$ , the anode becomes positive with respect to the cathode and the diode conducts, and continues conducting as long as the input remains more positive than  $E_1$ . During this period of conduction, the output voltage of the circuit is equal to the value of  $E_1$ , and that portion of the input signal which exceeds the bias voltage is clipped, or limited, appearing as a voltage drop across the diode load resistor. R.

By reversing the polarity of El, the parallel, positive lobe diode limiter may also be used where it is desired to limit not only the entire positive peaks of the input signal, but also a predetermined level of the negative peaks, in order to furnish an output only when the negative peaks exceed this predetermined level. (See the following illustration.) With the cathode negative. with respect to the anode, the diode is maintained in a conducting state in the absence of an input signal, and the output voltage is held at a steady (negative) dc level equal to El. With an input signal applied to the circuit, the output voltage continues to be held at this steady dc level, the input signal appearing across the diode load resistor, R, until the input signal becomes more negative than El. When this point is reached, the diode no longer conducts; and its forward resistance increases



Parallel, Positive Lobe Diode Limiter Used to Pass Negative Peaks

to a very high value. As a result, the input signal, which previously appeared across R because R was much greater in resistance than CR, now appears across CR and the output terminals of the circuit, since CR is now much greater in resistance than R. The output signal, therefore, contains only the negative peaks of the input signal which are more negative than biasing voltage  $E_{\mu}$ .

The circuit of a parallel, negative-lobe diode limiter is shown in the accompanying illustration. In this circuit, diode CR conducts only during the negative portion of the input signal. As long as the input signal remains positive, the diode remains in a nonconducting state, and current flow through R almost ceases. A small reverse current still flows through R and CR, because of the reverse resistance of the diode, and thus a small portion of the input voltage is dropped across the resistor. The amount of reverse resistance of the diode, just as in the positive-lobe limiter, depends upon the characteristics of the diode selected. The remainder of the circuit operation is essentially the same as the positive-lobe limiter described above.



A-949 Parallel-Diode Negative-Lobe Limiter A parallel, negative-lobe diode limiter may be also used to limit only the negative waveform peak, while allowing a given value of negative signal to pass through the circuit to **the** output. This may be accomplished by applying a negative biasing voltage, having a value equal to the value of the negative signal to be passed by the circuit, to the anode of the diode, as shown in the accompanying illustration. The circuit operation is essentially the same as the parallel, positive-lobe diode limiter used as a negative peak limiter (described previously), only with opposite polarities.



Parallel, Negative Lobe Diode Limiter Used as a Negative Peak Limiter

By reversing the polarity of  $E_{bb}$ , the **parallel**, negative-lobe diode limiter may also be used where it is desired to limit not only the entire negative peaks of the input signal, but also a predetermined level of the positive peaks, in order to furnish an output ordy when the positive peaks exceed this predetermined level. This circuit is illustrated below. The operation is essentially the same as the parallel, positive-lobe

diode limiter used to pass negative peaks (described previously), only with opposite polarities.



## Parallel, Negative Lobe Diode Limiter Used to Pass Positive Peaks

#### Failure Analysis.

**No Output.** A shorted diode or an open load resistor will cause a **no-output** condition to exist. The only other likely possibility is the absence of the input signal. Check the diode and the resistor with an ohmmeter, making certain to observe the polarities of the diode, since an erroneous indication may be obtained if the proper polarity is not observed. If both components check good, check for the presence of the input signal, making sure that it is of proper amplitude.

For the special case where the diode is not completely shorted, but reads a very low resistance of, say 200-ohms or less, the diode maybe considered defective.

In the case of the biased limiter, check the bias for proper voltage with a voltmeter. In the case of a battery bias supply the voltage will be either weak or absent, but in the case of the bias supply being a power supply, it could also be high.

**Reduced or Unstable Output.** A defective load resistor, R, or a defect in the parallel branch of the circuit, consisting of CR and the bias supply,  $E_i$ , can produce a reduced or unstable output. The only other likely possibility is a decrease in the amplitude of the input signal. The trouble can be localized in the same manner as described above for a no-output condition.

# TWO-DIODE, POSITIVE AND NEGATIVE LOBE DIOOE LIMITER (ELECTRON TUBE)

#### Application.

The two-diode, positive and negative lobe diode limiter is used where it is required to limit both the positive and negative peaks of an input signal waveform, in order to prevent the output signal from exceeding predetermined maximum values for both the positive and negative peaks. With the elimination of both peaks, the remaining signal is generally of square-wave shape; therefore, this circuit is often used as a square wave generator.

## Characteristics.

Input signal contains both positive and negative signals.

Output waveform contains both positive and negative signals, both of which do not exceed values which are preset limits in the initial design of the circuit.

Output amplitude is lower than the input amplitude; no amplification is afforded by the circuit.

Output is taken across two reverse-connected diode tubes.

#### Circuit Analysis.

**General. The** two-diode, positive and negative lobe diode limiter consists of two diodes, a source of both positive and negative voltage, and a load resistor. The load resistor is connected on the input side of the two diodes, and the diodes with their source of (bias) voltage are connected in parallel with each other and in parallel with the output terminals of the circuit. The output signal is produced as a repetition of the input signal during the interval that either diode does not conduct, and is limited at the point where either diode conducts.

**Circuit Operation.** The circuit of a simplified twodiode, positive and negative lobe diode limiter is shown in the following illustration. In this circuit the two diodes, VI and V2, each have a de voltage connected in series with them. The cathode of diode V1 has a positive potential applied which, for the purpose of illustration, has a value of +3.0 volts, as indicated in the associated waveform. The plate of V2 has a negative potential applied, which for illustration has a value of -3.0 volts. A load resistor, R1, is connected between the input terminals and the two diodes. Under conditions of no input signal, both diodes are in a nonconducting state, since the voltages

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#### **ELECTRONIC CIRCUITS**

that are applied to them are of such polarity as to oppose the flow of current through the diodes. These voltages are often termed bias voltages, since they establish the level of potential at which the diode will switch from a nonconducting to a conducting state. Now assume that an input signal, having a sine waveform with positive and negative peaks of +6.0 and -6.0 volts, respectively, is applied to the input to the circuit, as shown by the input waveform in the illustration. When the voltage on the positive cycle of the input signal reaches +3 volts, this same value of voltage appears at the plate of VI, since, with no current flow, there is no voltage drop across the load resistor RI. At this point the plate voltage is equal to the voltage applied to the cathode from the bias battery, E1. As soon as the positive cycle of input signal exceeds +3 volts, diode VI conducts, and a current flows through V1 and load resistor R1. If the voltage drop across V1 is assumed to be negligible, any value of input voltage which exceeds +3 volts will appear as a voltage drop across R1, resulting from the current flow due to the conduction of VI. This is in accordance with Kirchhoff's laws, in that the algebraic sum of the voltage drops and the applied voltage around any closed circuit equals zero. (At this moment-during the positive input cycle-the parallel path consisting of diode V2 and battery E2 is effectively out of the circuit, since it is in a nonconducting state.) The signal at the output terminals, during the positive half of the cycle, will then rise in sine-wave fashion to a value of +3 volts, at which point the voltage will be limited, or held, until the input signal passes through its peak of +6 volts and falls to +3 volts again, when it will follow the sine waveform during the decay of the positive cycle down to zero volts. Thus the positive half cycle of the output waveform will have a flat top at +3 volts. When the input signal passes through zero volts and increases in a negative direction, the output signal retains the sine waveform until the input signal reaches a value of -3volts. At this point the cathode voltage of V2 is equal to the negative voltage (-3 volts) applied to the plate of V2 from bias battery  $E_2$ . As soon as the negative cycle of the input signal exceeds (negatively) the -3volts bias, diode V2 conducts, causing a current to flow through V2 and load resistor R1. In a similar manner to that described for diode V1 and the positive cycle, any value of input voltage which is more negative than -3 volts will appear as a voltage drop

across R1, as a result of the current flow when V2

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conducts. The output signal, during the negative half cycle, will then follow the sine waveform of the input signal to a point at -3 volts, when the voltage will be limited until the input signal passes through its negative peak of -6 volts and returns to the value of -3 volts again. Then V2 will stop conducting, and the output signal will again follow the sine waveform of the input signal as the negative half of the cycle is completed.



## Simplified Two-Diode, Positive and Negative Lobe Diode Limiter and Waveforms

The point at which the positive portion of the input signal will be limited, or clipped, may be preset by applying a positive bias voltage of equal value to the cathode of diode VI, which is the positive peak limiter diode. In like manner, the point of negative limiting may be preset by applying a negative bias voltage to the plate of the negative peak limiter diode, V2. In this way the output signal maybe held within any desired positive and negative limits. Such a circuit is sometimes referred to as a gate clipper, since it acts as a gate which allows the center portion of an input signal to pass through to the output. More infrequently it is known as a slicer.

When the applied bias voltages are equally positive and negative and of a low value, while the input signal is a sine wave of a relatively high value, most of the curved portions of the sine wave at its peaks will be clipped, and the remaining positive-going and negative-going portions of the waveform w-ill have steep sides which approach the vertical. Thus a fairly accurate square wave output may be obtained, and such a circuit is often used as a square wave generator.

### Failure Analysis.

No Output. In a twodiode, positive and negative lobe diode limiter such as that previously illustrated, several conditions could be responsible for no output. Failure of diode load resistor Rl, due to an "open" resistor, or failure of the applied input signal would result in no output. Another possibility which should be investigated is the failure of both bias voltages. If individual batteries are used for both the negative and positive biases, the simultaneous failure of both is very urdikely, and thus some measure of output signal would be obtained. If, however, the bias voltages are obtained from a dc power supply operated from a power line, and the power supply failed, the diodes could then conduct through the circuit completed by the bleeder resistor in the output circuit of the power supply. Under these conditions the positive portion of the input signal would be clipped, or limited, by diode VI, and the negative portion would be limited by diode V2; thus no signal, or extremely little, would be present at the output terminals.

**Reduced or Unstable Output. In** a two-diode, positive and negative lobe diode limiter, a reduced or unstable output may be due to a defective load resistor, Rl, which may have suffered a considerable increase is resistance value. In addition, poor emission of the cathode in diode V1 or V2 may cause unstable output, as may also insufficient bias voltage  $E_1$  or  $E_2$  due to aging batteries or a defective power supply. Finally, the possibility of a reduced value of input signal, due to some defect in the preceding circuit, should not be overlooked.

# TWO-DIODE, POSITIVE AND NEGATIVE LOBE LIMITER (SEMICONDUCTOR)

#### Application.

**Same** application as the electron tube version.

#### Characteristics.

Same characteristics as the electron tube version.

### Circuit Analysis.

**General. The** positive and negative lobe diode limiter is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sinewave signal, or to eliminate the negative or positive portion of a waveform and clip the other portion. Our discussion here will primarily concern the equal clipping of both the positive and negative portions of a sine-wave, that is, the conversion of a sine-wave into essentially a square-wave.

**Circuit Operation.** The circuit of a parallel, positive and negative lobe diode limiter is shown in the following illustration. Diode CRI limits the positive half cycle of the input and CR2 limits the negative half.  $E_{bb1}$  and  $E_{bb2}$  supply the bias for their respective diodes and the resistor, R, acts as the load resistor. Reverse biases are applied to the diodes so that the cathode of CR1 is positive with respect to its anode, and the anode of CR2 is negative with respect to its cathode.



#### Parallel, Positive and Negative Loba Diode Limiter

As the signal is applied at the input and begins increasing in a positive direction, both diodes remain cut off, due to the bias, and the input signrd is reproduced at the output. The output continues to follow the input signal, until a point is reached where the signal becomes more positive than the positive bias applied to the cathode of CR1. At this point, the anode becomes more positive than the cathode, and the diode conducts. When the diode conducts, it provides a low resistance path for forward current to ground, and shunts the output through the diode instead of the external load. It is at this point that the output waveform is flattened. Actually, even during its conducting period, the diode offers a slight opposition to current flow, and a small forward voltage drop adds to the load voltage. Thus, the output voltage is slightly higher than the diode bias by the amount shown as  $V_{E}$ **1** on the output waveform.

As the input signal reaches its positive peak and begins decreasing toward zero, it again reaches a level
which is less positive than  $E_{bb1}$ , diode CRI again cuts off and the input is again faithfully reproduced at the output. The input signal continues in the negative direction, and shortly becomes more negative than  $E_{bb2}$ . When this occurs, the cathode of CR2 is made more negative than the anode, and diode CR2 conducts, duplicating the action which occurred on the positive half cycle. The forward voltage drop of the conducting diode is shown as  $V_{F2}$  on the output waveform. The input then reaches the negative peak and begins decreasing towards zero. As it becomes less negative than  $E_{bb2}$ , CR2 ceases conducting, and the remainder of the input signal is reproduced at the output.

The amount of clipping which takes place at the output is dependent to a certain extent upon the type of diodes selected, but primarily upon the value of the bias. As  $E_{bb1}$  is made more positive, less clipping occurs on the positive half cycle, and as it is made less positive, more clipping occurs. By the same token, as  $E_{bb2}$  is made less positive, more clipping occurs. By the same token, as  $E_{bb2}$  is made more negative less clipping occurs on the negative half cycle, and as it becomes less negative, more clipping occurs.

#### **Failure Analysis**

**No Output.** An open load resistor R, or the absence of the input signal are the two most probable causes of a no-output condition. Check the value of R with an ohmmeter for proper value, and check for the presence of the input signal with an oscilloscope. Note that for the diodes to produce a no-output condition, both of them must be shorted, and that the loss of both bias supplies will produce an extremely low clipped output, caused by the voltage drops across the diodes.

Low or Distorted Output. Under most circumstances, the output will be either distorted or lost completely. Distortion may be caused by a change in the bias supply, by an open or shorted diode, or distortion of the input signal. Check both bias supplies for proper voltage with a voltmeter, and both diodes with an ohmmeter. Be sure to observe proper polarities when checking the diodes, as incorrect indications could be obtained by not doing so. The input signal should be checked with an oscilloscope to determine if the input waveform is at fault.

The possibility of both half cycles of the output being decreased by the same amount is unlikely. Both bias supplies must decrease by the same amount to cause this condition. If both supplies increase, the output will increase. The only other cause of decreased output is the load resistor increasing in value.

# TRIOOE GRID LIMITER

#### Application.

The triode grid limiter is used to limit, or clip, the entire positive half cycle, or a portion thereof, of the input waveform.

#### Characteristics.

Input may be either a positive signal or a signal containing both positive and negative portions.

Output may be a negative signal with peaks clipped, or a signal having positive and negative portions in which all or a portion of the negative peaks are clipped.

Output signal is out of phase with input signal; therefore, the clipped positive half cycle of the input becomes a clipped negative half cycle of the output signal.

Output signal will contain a positive signal which is the amplified negative input signaL It may contain a negative portion, which is the result of a partially clipped positive input signal that has been amplified. The over-all output peak amplitude may be higher or lower than the input, depending upon the circuit application design.

#### Circuit Analysis.

General. The triode grid limiter is similar in its limiting action to that of the parallel, positive lobe diode limiter. An advantage of the triode grid limiter over the diode limiter, however, is that amplification of the negative portion (that part of the input signal which is not limited) is accomplished, in addition to the clipping action. In the triode grid limiter, the clipping is obtained as a result of the action of the cathode and control grid, in the same manner as the action of the cathode and plate of a diode limiter. Limiting action is obtained when conduction occurs i.e., when the grid is positive with respect to the cathode. When conduction of the "diode" (cathode to grid) does not occur, i.e., when the grid is negative with respect to the cathode, amplification and phase inversion of the input signal take place, in the manner which is characteristic of a regular triode amplifier.

**Circuit Operation.** A typical unbiased grid limiter circuit is shown in the following illustration. In this

circuit the input signal is applied to the grid of triode VI through grid resistor RI. In the circuit illustrated the **no-signal** plate current will be relatively high because the tube is unbiased; therefore, the plate voltage will be correspondingly low. For this reason, a positive input signal may have little effect upon the plate current. However, when the input signal goes positive, this positive voltage appears at the grid of Vl, and grid current begins to flow. Since the cathode of V1 is grounded, the only resistance to the flow of grid current in addition to R1 is that offered by the grid-to-cathode resistance of V1. If grid resistor R1 has a very high resistance in comparison to the grid-to-cathode resistance of V1 when grid current flows, practically the entire positive portion of the input signal will be clipped, or limited, to the voltage of the cathode (which in this particular circuit is zero voltage, or ground potential). In the same manner that the reverse resistance of a diode (the plate-to-cathode resistance when in a nonconducting state) is infiite, while the forward (or conduction) resistance is only 500 (approximately) ohms, so also is the grid-to-cathode resistance of a triode of an infinite value when in a nonconducting state (when the grid is negative with respect to the cathode); however, this resistance drops to a value of 500 to 1000 ohms when the grid becomes positive with respect to the cathode. Therefore, practically the entire value of the positive portion of the input voltage will drop across the very high resistance of R1 and is shown on the input waveform as  $E_{R1}$ . Only a very small part of the input voltage will drop across the grid-to-cathode (conduction) resistance of V1 which is a relatively low resistance; this voltage drop, although small, is shown on the input waveform as the value  $E_{ek}$ . As a result of the small positive bias on the grid of VI, a maximum value of plate current flows in the plate circuit. The high plate current, flowing through plate load resistor R2, causes a maximum voltage drop across R2, resulting in a minimum (nearly zero) voltage at the plate of V1. Because of the phase inversion within the triode, the effective grid voltage, which is the minimum positive voltage drop across the grid-to-cathode resistance of VI. becomes an inverted (negative) and amplified voltage, although still minimum, at the plate of V1.



# Typical Unbiased Triode Grid Limitar and Input-Output Waveform

When the positive half cycle of the input signal is completed and the input voltage falls to zero (the potential of the cathode), the grid current ceases to flow. As a result there is no longer a voltage drop across R1. Then, as the grid goes more negative during the negative half cycle, with no voltage drop across RI, the entire value of input voltage appears at the grid of VI, since it is applied across the (infinite) resistance between the grid and the cathode. Assuming that the negative input signrd does not drive the grid to cutoff, the negative half cycle is amplified by the triode and inverted, and this positive waveform appears at the output terminals of the circuit. In this manner, the positive portion of the input signal waveform is cut off, or limited, practically to zero, while the negative portion of the input signal is **amplified** without distortion and inverted, and passed through coupling capacitor Cl to the output terminals.

Another type of grid limiter circuit, which develops grid-leak bias to limit both the positive and negative peaks of the input signal, is the grid-leak biased grid limiter illustrated below. In this circuit, a sine wave from a master oscillator is applied to the input terminals, to produce a square wave which will be eventually used to produce trigger aud timing pulses in a radar circuit application. The triode, VI, operates without fixed bias, but develops grid-leak L

bias as a result of grid current flow. As the input voltage rises, during the positive portion of the input signal, the input coupling capacitor, Cl, charges because of the current which flows through grid return resistor RI and through grid resistor R2 in series with the grid-to-cathode resistance of V1. When the positive portion of the input cycle is completed and the input goes negative, the charge in capacitor Cl leaks off through resistor RI. During the charging cycle of Cl, the resistance in series with Cl consisted of R1 in parallel with R2 and VI. During discharge, V1 will not conduct when the grid is more negative than the cathode, and therefore the resistance in series with Cl is that of R1 alone. The resistance in series with Cl is thereby greater during discharge than it is during the charge cycle; as a result, a charge accumulates in capacitor Cl and becomes a negative bias, applied to the grid of VI (between grid and cathode).



Typical Grid-Leak Biased Grid Limiter and Input-Output Waveforms

The negative bias on the grid, produced by the flow of grid current during the charging cycle of Cl, acts in opposition to the effect of the input signal in driving the grid positive. The bias therefore establishes the average value, or baseline, about which the input sine wave varies. In the previous illustration, this bias is shown as having a value of -8 volts. Now, when the input signal during the positive portion of the cycle swings from -8 volts to zero volts, or cathode potential, the flow of grid current through the high value of the grid resistance of R1 limits the signal of approximately zero volts at the grid of V1.

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The increased flow of plate current through the plate load resistors, R3 and R4, produces an increased voltage drop across them and a minimum voltage at the plate of V1. This is shown in the output waveform as the output signal falls from +150 volts to +50volts, and is clipped at the level of +50 volts until the positive portion of the input signal, at the input terminals, passes through the crest of the waveform and falls back to zero volts. As the input signrd falls below zero volts, the plate current begins to fall, the voltage. drop in R3 and R4 decreases, and the voltage at the plate of Vi-which is the output voltage of the circuit-begins to rise. When the negative-going input signal falls toward the cutoff bias value, the plate current decreases toward zero, reaching zero when the combination of input signal and bias reaches cutoff. The plate voltage of V1, and therefore the output signal voltage, increases toward the B+ voltage, reaching this value of +250 volts at cutoff. Thus the top of the output waveform is limited, or clipped, at the level of +250 volts, as shown in the illustration.

A third type of grid limiter circuit is that in which a freed negative bias is applied to the grid, from a battery or dc power supply. A typical circuit of this type of grid limiter is shown in the following illustration. In this circuit, a fixed bias of -5 volts, dc, is applied to the grid from a bias supply, along with the input signal. As the signal increases from the negative 5-volt bias value in a positive direction, the plate current increases in accordance with the signal input, with a consequent decrease in plate voltage, until the input signal reaches the cathode potential of zero volts. When this point is reached, any further rise in grid voltage drives the grid positive with respect to the cathode, and the resulting flow of grid current through grid resistor R1 limits the voltage at the grid to approximately zero volts (disregarding the voltage drop across the grid-to-cathode resistance of Vi). The plate voltage, now at its lowest value, is clipped, or limited, at a level determined by the circuit application, which for illustration is shown as +50 volts in the output waveform. As the input signal passes through its positive crest and fills, grid current ceases to flow when the input signal falls to zero volts. During the remainder of the positive half cycle of the input signal, and through the complete negative half cycle, the flow of plate current follows in accordance with the grid voltage, without distortion, and the amplified and inverted waveform of voltage is furnished to the output terminals of the circuit. (The

amplitude of the negative portion of the input signal is not sufficient to drive the tube to cutoff.)



# Typical Fixed Bias Grid Limitar and Input-Output Waveforms

A fourth type of grid limiter circuit is the selfbiased grid limiter, in which the bias is automatically developed by the flow of plate current through a bypassed cathode resistor. A typical circuit of this type of grid limiter is shown in the following illustration. In this circuit, the grid of VI is normally held at ground potential, and the grid bias is produced by the flow of plate current through cathode resistor R2. In order to maintain the bias at a relatively constant level, so that it does not vary with the input signal waveform, R2 is bypassed with capacitor C2, which has a large value of capacitance. The flow of plate current through R2 established the cathode of V1 at a positive voltage above ground potential, thus furnishing the bias to the grid, which is at ground potential and therefore negative with respect to the cathode. When the input signal rises at the start of the positive half cycle, the plate current in VI increases with the signal, and the waveform is not limited until the grid voltage reaches a value equally positive to that of the cathode. When this point is reached, a further rise of the input voltage produces grid current, which results in the limiting 'of the voltage at the grid. This is indicated by the input waveform in the illustration, at the point of cathode bias. Grid current ceases to flow, and thereby limiting is completed, when the input signal has fallen back to the point where the voltage is equal to that of the cathode.

During the remainder of the positive hrdf cycle, and throughout the negative half cycle, the circuit operates as a Class-A amplifier, furnishing an output waveform which is an amplified and inverted reproduction of the input signal, without distortion. (The amplitude of the negative portion of the input signal is not sufficient to drive the tube to cutoff.)



# Typical Cathode-Biasad Grid Limiter and Input-Output Waveforms

# Failure Analysis.

**No Output. The** analysis of failure which results in no output from a triode grid limiter is somewhat similar to that of the parallel, positive lobe diode limiter. In the triode grid limiter, failure of triode VI, or an open-circuited grid resistor or plate load resistor, or failure of the plate supply voltage could each be responsible for a no-output condition. If the circuit utilizes cathode bias, an open cathode resistor would also be a cause of no output. If the circuit contains input and/or output coupling capacitors, an open-circuited' capacitor in either position would result in no output. Finally, failure of the applied signal, or an input signal of incorrect waveform or voltage level, could also be responsible for a nooutput condition.

**Radueed or Unstable Output.** Assuming that an input signal of correct waveform and voltage level is being furnished to the input terminals of a grid limiter circuit, a reduced value of output is probably the result of either insufficient signal at the grid terminal of the triode, insufficient voltage at the plate terminal of the triode, or a leaky coupling capacitor

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in the grid or plate circuit, when used. Insufficient signal at the grid may be due to a defective grid resistor which has increased in value or become opencircuited. Insufficient plate voltage may be due to a defective plate load resistor or insufficient plate supply voltage brought about by a defect in the power supply. A shorted plate output coupling capacitor may also be responsible for low plate voltage, with the following stage loading the plate circuit. A cathode resistor, if used, may be too low in value and cause excessive plate current, resulting in a low plate voltage. Leaky coupling capacitors, if used, may cause distortion of the waveform, in addition to placing an additional load on the circuit. Finally, a shorted or leaky decoupling capacitor in the plate supply decoupling circuit, when used, would be responsible for low, or absence of, plate voltage.

# TRIODE SATURATION LIMITER (ELECTRON TUBE)

#### Application.

**The** triode saturation limiter is used to limit, or clip, the positive peaks of an input waveform. This limiter is useful when low amplitude input signals are used, at rather low plate supply voltages.

#### Characteristics.

Same characteristics as the grid limiter circuit.

#### **Circuit Analysis.**

**General. The** triode saturation limiter differs from the triode grid limiter in its limiting action, in that the actual limiting is accomplished in the plate circuit, while in the grid limiter it is accomplished in the input, or grid circuit. In the saturation limiter the entire input signal is applied to the grid of the triode. Amplification of the entire signal is provided by the triode, up to its maximum capability insofar as its maximum plate current is concerned. When the input signal to the grid is such that maximum plate current flows, any additional vrdue of input signal has no further effect on the plate current; this additionrd value is thereby limited, or clipped, at the level of maximum current flow in the plate circuit.

The action of the triode saturation limiter is similar to that of the triode grid limiter in its end result; that is, in both cases the positive portion of the input waveform is the portion which is limited, or

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clipped. In the saturation' limiter, however, the output is generally of a higher amplitude, because the plate current is driven to its maximum value. On the other hand, since it is necessary to drive the plate circuit to its maximum conduction to produce limiting, this becomes a disadvantage because a higher input signal is required to drive the grid.

**Circuit Operation.** The circuit of a typical triode saturation limiter is shown in the accompanying illustration.



# Typical Triode saturation Limiter and Input-Output Waveforms

In this circuit the input signal, which is obtained from a low-impedance source that is capable of a relatively high power output, is applied directly to the grid of triode V1, and no grid resistor is used. The cathode is connected directly to ground, and the triode is thereby operated at zero grid bias. A voltage divider, consisting of R3 and R2, is connected in the plate supply circuit, to obtain a lower value of voltage. Capacitor C2 acts as an additional falter for the plate voltage supply, while resistor RI is the plate load resistor. If the resistance value of R1 is relatively high, and the relative resistance value of R3 and R2 are such that the voltage at their junction is relatively low, then a fairly low value of positive input signal will drive the grid to the point of plate current saturation, and limiting will occur. The reason for this is as follows: The following illustration shows the dynamic characteristics of a typical triode amplifier tube-a single section of a type 12AU7. Assume that this tube is used in the circuit previously illustrated,

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with a plate voltage (at the junction of R3 and R2) of +300 volts, and a load resistance R1 of 60K. The triode is operated at zero bias, since the cathode is grounded, and the input signal to the grid is a sine wave of 14 volts peak-to-peak. From the illustration, it may be seen that the plate current flowing in the circuit, with no signal input, is approximately 4 ma. It is rdso evident that the maximum plate current that can flow, with the fixed values of plate voltage and load resistance given, is 5 milliamperes. When the input signal rises from zero toward +7.0 volts on its positive half cycle, plate current increases from 4 ma

to 5 ma, reaching 5 ma when the input signal reaches approximately +2.5 volts. At this point the plate current is maximum, and limiting occurs. The output voltage at this point has decreased nearly to zero (there is always some value of voltage drop within the triode, because of its plate resistance). The output voltage waveform is thereby clipped on its negative half cycle, until the input signal has passed through its positive peak of +7.0 volts and fallen back to +2.5volts. At this point limiting ceases, and the plate current begins to decrease in accordance with the input signal.



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It becomes evident, from the illustration, that the point at which saturation is reached, and thereby the positive limit at which clipping of the input signal occurs, may be adjusted by adjusting the slope of the load line, which in turn may be adjusted by varying the load resistance and/or the plate voltage. On the other hand, the percentage of the positive portion of the input waveform which is clipped may be adjusted by varying the peak voltage of the input signal. Referring again to the previous illustration, it can be seen that clipping of the positive portion of the input signal occurs at approximately +2.5 volts. This is approximately 30 percent of the positive peak input waveform. If the input signal is now increased to 25 volts peak-to-peak, clipping of the 12.5-volt positive peak still occurs at +2.5 volts. The positive portion of the input signal is now clipped at 20 percent of the peak input value.

#### Failure Analysis.

**No Output. The** cause of a no-output condition in a triode saturation limiter may be one of four possibilities. Either the input signal may have failed, the triode tube may be defective, the plate supply voltage may have failed, or the output coupling capacitor may be open-circuited. Failure of the plate supply voltage may be due not only to a defective power supply, but also to an "open" resistor RI or R3 or a shorted bypass capacitor C2, in the plate circuit.

Reduced or Unstable Output. A reduced or unstable output from a triode saturation limiter could result from almost any component of the circuit which has become defective. A weak or leaky (partially shorted) triode VI or a reduced value of plate voltage may be the cause of either condition, depending upon the extent of the defect. A reduced value of plate voltage may be due to a defective power supply, or it may be due to an increase in the value of resistor R1 or R3 or a decrease in the value of R2. A leaky coupling capacitor Cl may allow some of the d-c plate voltage at VI to appear at the input to the following stage, resulting in an improper bias to that stage and probable distortion therein. Finally, in the analysis of failure of a circuit it is often assumed that the proper input signal is being supplied. This fact will bear checking, however, because an input signal of incorrect value or waveform could well be responsible for a distorted or reduced value of output signal.

# TRIODE CUTOFF LIMITER (ELECTRON TUBE)

#### Application.

**The** triode cutoff limiter is used to limit, or clip, the entire negative half-cycle, or the negative peaks, of the input waveform,

#### Characteristics.

Input may be either a negative signal or a signal containing both positive and negative portions.

Output may be positive signal with peaks which exceed a preset value clipped, or a signal having both positive and negative portions in which all or a portion of the positive peaks are clipped.

Output signal is out of phase with input signal; therefore, the clipped negative half-cycle of the input signal becomes a clipped positive half-cycle of the output signal.

Output signal will contain a negative signal which is the amplified positive portion of the input signal, if such is included in the input. It may contain a positive portion, which is the result of a partially clipped negative input signal that has been amplified. The peak amplitude of the output signal, including both positive and negative portions when applicable, may be higher or lower than the input peak amplitude, depending upon the circuit application design.

#### Circuit Analysis.

General. The triode cutoff limiter depends, for its limiting action, upon the fact that an electron current within a vacuum tube can flow only from the cathode to the plate, and not in the reverse direction. When the signal at the grid of the triode drives the grid to cutoff, the plate current is decreased to zero, and it remains at zero during the time that the grid is held at or below cutoff by the input signal. At cutoff the plate current is zero, and, regardless of how much farther the grid is driven negative, the plate current remains at zero, since the plate current cannot become a negative value. When the grid is at (or below) cutoff, since no current flows in the plate circuit, there is no voltage drop across the plate load resistor. The voltage at the plate, therefore, increases to, and is maintained at, its maximum value, which is the voltage of the plate power supply, E<sub>bb</sub>. The limiting thus attained affects the positive peak of the output waveform, whereby the positive peak is cut off, or flattened, at the voltage level  $E_{bb}$  as a result of driving the grid in the negative direction to cutoff.

Cutoff voltage is that value of negative voltage, with respect to the cathode, which must be applied to the grid to reduce the plate current to zero. This value of voltage is dependent upon the value of the **plate** supply voltage,  $E_{bb}$ . In a triode the cutoff voltage,  $E_{co}$ , is approximately equal to the plate supply voltage,  $E_{bb}$ , divided by the amplification factor,  $\mu$ , of the triode; thus:

$$(-) E_{co} = \frac{E_{bb}}{\mu}$$

The relationship expressed above is valid only for a tnode; it does not apply to tetrodes or pentodes.

**Circuit Operation.** The circuit of a typical triode cutoff limiter is shown in the following illustration.



"Typical Triode Cutoff Limiter and Input-Output Waveforms."

In this circuit the input signal is applied directly to the grid of triode Vl, and no grid resistor is used. Cathode bias is supplied by resistor Rl, bypassed by C2 to hold the bias value constant with the average value of the plate current. If the value of the cathode resistor, RI, is sufflciently large the bias developed will set the operating point of the tube near cutoff. When the input signal rises on the positive half cycle, the plate current will increase and thus produce the resultant plate voltage waveform shown in the illustration. When the input signal begins to fall, this causes a corresponding positive excursion of plate voltage, and this action continues until cutoff is reached on the negative half cycle of the input signal. At this time the plate current is zero, thus limiting (clipping) the positive portion of the plate-voltage waveform. For the purpose of illustration, assume that the resistance value of R1 is such that the no-signal d-c bias is -3.0 volts at the grid. The plate supply voltage,  $E_{bb}$ , for this illustration is +250 volts, and the maximum amplitude of the input signal is 2.5 volts. The grid voltage, with input signal, therefore swings from -0.5 volt to -5.5 volts. The dynamic conditions existing in this example are shown in the following illustration, based on utilizing the triode section of a type 6SQ7 tube.

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# Operating Characteristics of a Typical Cutoff Limiter

From the illustration, it may be seen that the no-signal plate current is approximately 0.125 ma. When the input signal rises on its positive half-cycle, the plate current increases from 0.125 to 0.95 ma, reaching this maximum value when the input signal reaches its most positive (or least negative) value of -0.5 volt. The input signal then begins to fall, completing the positive half-cycle when the voltage at the grid is -3.0 volts. As the input signal begins its negative half-cycle, the voltage at the grid continues in its negative direction until it reaches -4.0 volts. At this point cutoff occurs, and the plate current has fallen to zero. The output voltage at this point, with no plate current flowing and therefore no voltage drop through plate load resistor R2, has increased to +250 volts, the value of  $E_{bb}$ . With the plate current cut off, the output voltage remains at this value until the input signal has fallen through its negative peak of

-5.5 volts and increased to the cutoff point of -4.0 volts. As the input signrd continues to rise, the plate voltage (output signal) begins to fall; at the end of the negative half-cycle of input signal the output voltage has fallen to its no-signal value of approximately +235 volts, and the plate current has increased to 0.125 ma again.

From the preceding illustration it becomes evident that the point at which cutoff is reached, and thereby the negative limit at which clipping of the input signal occurs, may be changed by adjusting the slope of the load line and/or the no-signal grid bias. The slope of load line may be adjusted by changing the plate supply voltage,  $E_{bb}$ , and/or the load resistance; this adjustment, however, will affect the no-signal grid bias when cathode biasing is utilized. The grid bias may be further adjusted by changing the value of the cathode resistor. It should be noted that, with

cathode bias, cutoff cannot be maintained with a steady dc signal, because the bias is obtained by means of the plate current flowing through the cathode resistor. At cutoff, no plate current flows, and therefore no bias will be obtained. But with ac, and especially with pulsed signals and the use of a large capacitor bypassing the cathode resistor, the bias may be adjusted over a considerable range by changing the value of the cathode resistor, thereby adjusting the point at which cutoff is reached. When complete clipping of the negative portion of the input signal is not required, the percentage of the negative portion which is clipped may be adjusted by varying the peak voltage of the input signal. However, the maximum limit of the input signal must in no case be great enough to drive the grid into the positive region, where grid limiting would act to clip the positive peak of the input signal and thereby introduce distortion to that portion of the waveform. Refer to the previous illustration; the positive peak of the input signal is shown driving the grid to -0.5 volt, and the negative peak to -5.5 volts. Clipping occurs at -4.0 volts, and the no-signal bias is -3.0 volts. With the negative swing from -3.0 to -5.5 volts, or a total swing of 2.5 volts (of which the portion between 4.0 and -5.5 volts, or a total of 1.5 volts, is clipped), the percentage of the negative portion clipped is therefore 1.5/2.5, or 60 percent. Under the same circuit conditions, the percentage of the negative portion which is clipped may be increased, by increasing the input signal amplitude, only by the additional amount of 1.0 volt peak to peak. This increased input would drive the grid to -6.0 volts on the negative peak, and to zero volts on the positive peak, which is the absolute maximum limit without incurring grid limiting. With the additional drive on the negative swing, the percentage of the negative portion clipped would thereby be increased to 2.0/3.0, or 66 per cent.

The circuit of a triode cutoff limiter used in a specific application is shown in the following illustration. This cutoff limiter is used in the modulator circuit of Radar Set AN/SPS-10D, and in this application begins the shaping of a sine wave at a frequency of 650 Hz, obtained from a repetition rate oscillator, to a square wave. In the absence of an input signal, V1 is cut off by the positive voltage present at the cathode, obtained from the voltage divider composed of the two cathode resistors and

resistor R returned to +300 volts, dc. Resistor R in this circuit represents the conduction through another triode tube. The 0.1  $\mu$ f capacitor across the 2.2K resistor in the cathode circuit acts to maintain the cathode bias at a constant average value. The input to the grid of VI is a sine wave of approximately 90 volts peak to peak. As the input voltage increases on the positive portion of the input signal, the grid voltage overcomes the positive bias voltage at the cathode from the voltage divider, and the triode conducts. The output signal, which had maintained a flat top at +300 volts, dc during the cutoff interval, now begins to fall in accordance with the rising sine wave input signat, because of phase inversion within VI. The output signal maintains the 1550-psec pulse width of the input signal, but has a waveform which is approximately a square wave, with the positive peaks cut off sharply, and a peak voltage of 95 volts, as shown in the illustration.



Triode Cutoff Limiter Used in Modulator of Radar Set AN/SPS-10D

#### **Failure Analysis**

**No Output.** Assuming that an input signal of correct polarity and sufficient voltage is being furnished to the triode cutoff limiter, the cause of a no-output condition could be one of several possibilities. The triode tube itself should be **first** suspected. If the tube is found to be capable of operation, the input 'signal may not be present at the grid of the tube, because of an open coupling capacitor. The

# **ELECTRONIC CIRCUITS**

absence of voltage at the plate, due to an open plate load resistor, an inoperative power supply, or a shorted bypass capacitor across a plate load decoupling **circuit**, if such a circuit is used, may be responsible for no output, as may also an open cathode resistor. Finally, an open output coupling capacitor, if used, would prevent the output from the limiter from being furnished to the following stage.

**Reduced or Unstable Output. Several conditions** could contribute to a reduced or unstable output from the triode cutoff limiter. A reduced value of plate voltage, due to a defective power supply, or an aging triode tube due to low cathode emission, may be responsible for a reduced output. An open cathode bypass capacitor would be the cause of degeneration, and reduce the output signal. If a freed cathode bias is obtained from a voltage divider in the plate voltage supply line, such as shown in the second circuit illustrated herein, and if the resistor on the high side should become open-circuited, the operation of the circuit would be changed from fixed bias to self (cathode) bias, thereby changing the point of limiting, with the possibility of a distorted, or even excessive, output. An open grid resistor, if used, may cause grid "blocking" and severe distortion. In addition, the possibility of an input signal of incorrect waveform, or of insufficient amplitude, should not be overlooked in cases of reduced or otherwise faulty output.

# TRIODE OVERORIVEN AMPLIFIER LIMITER (ELECTRON TUBE)

#### Application

The triode overdriven amplifier limiter is used to limit, or clip, both the positive and the negative peaks of an input signal waveform. It is also used to steepen the sides of an input signal having a waveform which is approximately a square wave.

#### Characteristics

Input is generally a sine wave, or a partially squared wave produced from a sine wave by a preceding limiter.

Output is usually a square wave having relatively steep sides.

Output signal is out of phase with input signal.

Amplitude of output signal may be higher or lower than input amplitude, depending upon the points at which the positive and negative peaks are clipped. Amplification is afforded by the circuit to the input signal, before the peaks are clipped.

# Circuit Analysis

General. The triode overdriven amplifier limiter accomplishes its limiting action by combining cutoff limiting with saturation limiting (or with grid limiting). The principal use of this type of limiter is to produce a square wave, having steep sides which are very close to true vertical, from an input signal whose waveform is only a rough approximation of a square wave, having sides which deviate at considerable angles from the vertical. The preceding circuit which furnishes the input signal should have an output impedance which is relatively low, and therefore be capable of delivering power, because a current of some degree is drawn by the grid of the triode when it is driven positive. The preceding circuit should rdso be capable of furnishing an input signal of considerable amplitude, so that the slope of the sides of the, waveform may be as nearly vertical as possible before amplification and limiting.

Circuit Operation. The circuit of a typical triode overdriven amplifier limiter is shown in the following illustration. In this circuit the input signal is applied directly to the grid of the triode, Vl, and no grid resistor is used. Since the source of the signal has a low impedance and thereby can furnish current to the grid of Vl, no limiting is performed in the grid circuit. No cathode resistor is used; hence the grid is operated at zero bias. The input is a very large amplitude signal, often ten times the value required to drive the tube to cutoff and to saturation. When the input signal rises, the plate current also rises until the point of plate current saturation is reached. The input signal continues to rise to its peak; however, the plate current cannot increase further because it is already at maximum. During this time, the plate voltage is limited to its minimum value. As the input signal passes through its positive peak and begins to fall, it drops below the saturation point, and at this time the plate current again follows the input signal. As the input signal continues to fall, the plate current decreases accordingly to cause the plate voltage to rise until the plate current is cut off by the input signal. The plate voltage is thus limited to its maximum positive value. When the input signal passes through its negative extreme and begins to rise, it

rises above the cutoff point and, once again, plate current begins to flow.



# Typical Overdriven Amplifier Limiter and Input-Output Waveforms

The action of the triode overdriven amplifier with an input sine-wave signal of sufficient amplitude is shown in the following illustration. This illustration shows the dynamic conditions existing in the circuit, based on utilizing the triode

section of a type 6SQ7 tube, with an input signal having an amplitude sufficient to drive the grid into plate current saturation on the positive swing, and beyond cutoff on the negative swing. It may be seen that the plate current flowing, in the absence of an input signal, is 0.8 ma. When the input signal rises on the positive portion of its cycle, the plate current increases from 0.8 ma to approximately 1.4 ma, at which point plate current saturation is reached. As the input signal continues to rise to its peak, the plate current cannot increase in accordance with the input signal, because it is already at its maximum value. The plate voltage at this time is at its lowest value, with nearly all of the plate supply voltage, E<sub>bb</sub>, existing as a voltage drop across the plate load. (A small portion of the total voltage drop exists across the plate-tocathode resistance of the triode itself.) The plate current is thereby limited at the saturation value, and the output voltage is limited at its lowest value, until the input signal passes through its positive peak and falls again below the saturation point. At that time the plate current begins to frdl in accordance with the input signal, and, consequently, the output signal begins to rise. The input signal continues to fall as the positive portion of the input cycle is completed and the negative portion begins.

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Operating Characteristics of a Typical Overdriven Amplifier Limiter

As the input signal continues to fall, the plate current continues to decrease until the grid voltage reaches -2.0 volts. At this point cutoff occurs, and the plate current has decreased to zero. The output voltage at this point, with no plate current flowing and therefore no voltage drop through the plate load resistor, has increased to maximum (the value of **E**<sub>bb</sub>). The **plate** current is thereby limited at zero, and the output voltage is limited at its maximum value, until the input signal passes through its negative peak and rises again to the cutoff point. At

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that time plate current again begins to flow, and the output voltage begins to fall, until the plate current increases to 0.8 ma when the negative portion of the input cycle is completed.

It becomes evident, from the preceding illustration, that the point at which the positive portion of the input signal is clipped (plate current saturation), and the point at which the negative portion of the input signal is clipped (cutoff), may be adjusted by changing the slope of the load line and the plate load resistance. **The** slope of the load line may be

increased by increasing the plate supply voltage,  $E_{bb}$ , and at the same time increasing the plate load resistance. This will produce a larger positive output signal, because it increases the value of the negative input signal required to reach cutoff.

A practical application of a triode overdriven amplifier limiter is its use in the time circuitry of a radar transmitter. In this application the overdriven amplifier functions as one of the stages in a chain of circuits, which generate a sine wave in a master oscillator, and from it produce sync and timing pulses for the operation of the complete system. The overdrive amplifier follows after the master oscillator and a triode limiter in the chain, and it receives an input signal whose waveform is that of a sine wave which has been approximately squared by a triode limiter. The function of the overdriven amplifier is to steepen the sides of the square wave from the limiter, to produce a square wave having sides as nearly vertical as possible, which may be used in a following stage to produce a sharp trigger pulse. The circuit of the overdriven amplifier used in this application is shown in the following illustration. In this circuit, which utilizes cutoff limiting with grid limiting (instead of saturation limiting), the input signal waveform is somewhat like a square wave, and of large amplitude. As the input signal begins to rise toward its positive peak, the plate current remains at zero, since the grid voltage is below cutoff, until the grid voltage rises (becomes less negative) to the cutoff potential. The triode then conducts, as the grid voltage rises to zero (ground) potential. When the signal drives the grid to zero bias, grid current begins to flow, limiting any further rise of the grid voltage at this point. The grid current charges coupling capacitor Cl, through the relatively low grid-tocathode resistance of triode V1, to an average voltage which serves as a highly negative bias for the grid of triode V1. During this time the plate (output) voltage has fallen abruptly, decreasing nearly to zero, and it remains at that value until the grid signal falls, from its positive peak, back to zero. At zero bias, the plate current begins to fall rapidly as the grid voltage becomes more negative, until cutoff is reached, when the plate current has fallen to zero. During this time the plate (output) voltage has risen sharply to its maximum value of Ebb. From the waveforms shown, it should be noted that the negative portion of the output waveform is narrower than the positive portion; this is due to the fact that the tube conducts

only during a portion of the positive half-cycle of the input signal, while it remains nonconductive during the entire negative half-cycle.



# Overdriven Amplifier Used in Radar Timing Circuitry, and Waveforms

#### Failure Analysis

No Output. The cause of a no-output condition in the triode overdriven amplifier limiter may be defective triode tube, failure of the plate supply voltage, an open input or output coupling capacitor (if either is used), or failure of the input signal. Assuming that the tube has been determined to be capable of operation, and that an input signal of proper amplitude and polarity is present at the input to the circuit, an open plate load resistor (or plate decoupling resistor if a decoupling circuit is used) would render the circuit inoperative, and no output would be available. A shorted decoupling bypass capacitor (C2 in the second circuit illustrated), if a decoupling circuit is used, may also be the cause of a no-output condition. An open coupling capacitor in the input grid circuit, if one is used, would likewise prevent any output from being produced.

Reduced or Unstable Output. When the output of the triode overdriven amplifier becomes unstable or is of reduced value, a low value of plate voltage, due to a defective power supply, or an increased value of plate load resistance, due to a defective or "aging" resistor, may be the cause of this condition. Either a leaky input or output coupling capacitor or an open grid resistor could be responsible for unstable opera-tion. The tnode tube itself may have low cathode emission; this would produce a reduced output.

Finally, the input signal itself should be checked to ascertain whether it is of correct waveform and has sufficient amplitude, since any deficiency in the input signal would be evident in the output from the overdrive amplifier.

#### TRIO DE, BASIC COMMON-BASE LIMITER

#### Application.

A triode, basic common-base limiter is used in semiconductor circuits when it is desired to limit the amplitude of a relatively small input signal to a definite negative and positive output level.

#### Characteristics.

Cutoff and saturation limiting are used by this limiter.

Base to emitter bias and base to collector bias values determine the proper limiting level.

Low input impedance and high output impedance. No phase inversion.

#### **Circuit Analysis.**

**General. The** triode, basic common-base limiter is essentially a transistor amplifier which is operated at a level which allows it to be cutoff and saturated at certain positive and negative amplitudes of the input signal. By using a specific emitter to base voltage a specific emitter current is obtained. This emitter current determines what signal level is required to cutoff and saturate the limiter. These cutoff and saturation values are the limiting levels.

**Circuit Operation. A triode, basic** NPN commonbase limiter is shown in the accompanying illustration.



Triode, Basic Common Base Limiter (NPN)

Capacitor Cl and resistor R1 form a coupling network which couples the signal from the previous stage to the emitter of QI. Bias supply  $V_{EE}$  determines the emitter to base bias voltage. The value of base resistor R1 in conjunction with the bias supplied by  $V_{EE}$  determines the emitter current. Collector load resistor R2 and collector supply  $V_{CC}$  establish the collector current. Capacitor C2 couples the output of Q1 to the following stage. Q1 is an NPN transistor.

When the incoming signal is positive-going the positive signal voltage opposes the normal negative bias between the emitter and the base. This reduces the current flowing through the transistor. When the collector current of Q1 is reduced, the voltage drop across R2 is also reduced, and the collector voltage

approaches that of the collector supply which, in effect, makes the collector more positive. Thus, for a positive incoming signal a positive output voltage is obtained.

When the positive incoming signal becomes sufficiently large that it cancels the forward bias entirely the transistor cuts off and collector current ceases. The collector voltage of Q1 is now at the supply value and cannot increase further. Hence, for any further positive increase in signal voltage there is no change in output voltage, which stays constant for any variation of input signal voltage beyond the cut-off level.

When the incoming signal is negative-going the emitter is driven negative with respect to the base. This increases the forward bias and current flow (electron flow) from emitter to collector. An increase in voltage drop across the collector resistor R2 results, which drives the collector more negative. Thus, a negative input results in a negative output.

If the incoming signal exceeds a certain negative value, the current from emitter to collector reaches its maximum (saturation) value and the collector voltage reaches a minimum value. Any further increase in amplitude of the negative input signal does not affect the collector current or the voltage at the collector, since the transistor has attained a saturated level.

It is at these levels of saturation and cutoff that the output voltage is limited. Thus, to achieve limiting it is necessary to supply a large amplitude signal. Between the limits of cutoff and saturation the circuit will act as a conventional amplifier. Beyond these limits the peaks are cut off and the waveform is effectively "squared off".

## Failure Analysis.

**No Output.** In a triode, basic common-base limiter a no-output condition may be caused by any of the following (provided the input signal is present and correct): An open coupling capacitor Cl, an open bias resistor RI, an open or shorted supply voltage  $V_{EE}$ , an open collector to base resistor R2, an open or shorted supply voltage  $V_{ec}$ , **an** open outPut **coupling** capacitor C2, or a faulty transistor Q].

To determine which of these components is at fault first use an oscilloscope to determine if the input signal is present at the input terminals of the circuit. Then determine if the input signal is present at the emitter of the transistor. If the signal is present at the input terminals but not at the emitter, first check Cl with an in-circuit capacitor checker. If C 1 is not open check RI with an ohmmeter (after disconnecting one end of the resistor from the circuit). If RI is not open, check bias voltage V by measuring it with a high resistance voltmeter. If  $V_{EE}$  is not zero or shorted, check R2 with an ohmmeter (after disconnecting one end of the resistor from the circuit). If R2 is not open, check the collector bias voltage  $V_{cc}$  with a high resistance voltmeter. Check C2 with an in-circuit capacitor checker. If C2 is not open and all other components check out, transistor Q1 must be at fault.

Low or Distorted Out. A low or distorted out may be caused by: input capacitor Cl being shorted, resistor R1 being shorted or beyond tolerance, voltage source  $V_{EE}$  being other than the required voltage, resistor R2 being shorted or beyond tolerance, voltage source  $V_{cc}$  being other than the required voltage, capacitor C2 being shorted, and transistor Q1 being defective.

To determine which of these components is at fault, first check the voltage between one plate of Cl and ground with a high resistance voltmeter, then check the voltage between the other plate of Cl and ground. If these voltage values are equal then capacitor Cl is shorted. Check the value of RI with an ohmmeter (after first disconnecting one end of R1 from the circuit) for the proper ohmic value. Check voltage source  $V_{EE}$  with a high resistance voltmeter. Check R2 with an ohmmeter (after first disconnecting one side of R2 from the circuit) for proper ohmic value. Check voltage source  $V_{\alpha}$  with a high resistance voltmeter. Check the voltage between one plate of C2 and ground with a high resistance voltmeter, then check the voltage between the other plate and ground. If all of these components are good and the trouble still persists, the fault must be in transistor Q1.

# VIDEO LIMITER (ELECTRON TUBE)

#### Application.

The video limiter is used to amplify and limit to a specific amplitude low level video input signal voltages in radar and television equipment.

#### Characteristics.

Constant output is obtained once the limiting level is reached. Linear amplification occurs up to limiting level. Screen grid and plate voltages determine limiting level for a specific bias.

Best performance is obtained with sharp cutoff pentode-has rapid rise time, has little droop.

#### **Circuit** Analysis.

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**General. The** pentode video limiter is located between the video detector and the low level cathode follower output stage in radar and TV receivers. Cutoff type limiting, rather than grid current or plate saturation limiting, is preferred in video limiter operation. Cutoff limiting occurs when the limiting level is determined solely by the cutoff bias level. Grid current limiting occurs when sufficient grid current is drawn to produce the desired limiting bias. Plate saturation limiting occurs when the grid bias is low or at zero and the signal drives the plate current into the saturation (no current change) level at which limiting occurs.

The limiter is supplied with a negative signal from the video detector. The signal is restricted in its negative amplitude direction by biasing the limiter tube so that cutoff occurs at the point where the desired negative voltage amplitude is attained. As the negative voltage is applied to the grid of the pentode it is inverted and amplified at the plate and coupled to the cathode follower following the limiter stage.

A pentode tube is preferred in limiter applications for several reasons. The primary reason is that the pentode inherently has sharp cutoff capabilities. This allows the tube to reach cutoff bias with a less negative-going (smaller) signal than normally would be required, and thus performs better for smaller input signals.



PentOde Video Limiter

**Circuit Operation. The schematic** of a typical video limiter circuit using a pentode type of electron tube is shown in the accompanying illustration.

The input signal is capacitively coupled through coupling capacitor  $C_1$  to the grid of  $V_1$ . The combination of capacitor  $C_1$  and grid leak resistor  $R_1$  establish the bias potential. Plate load resistor  $R_2$  is used to develop the plate output voltage. The screen grid dropping resistor R3 drops the screen grid voltage to the proper value and bypass capacitor  $C_2$  places the screen at ground potential for video.

Without a signal applied, only contact bias is developed and the tube operates near zero bias. At this point the plate and screen grid voltages largely control the amount of plate current flowing.

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With the application of the negative input signal (obtained from the video detector) to Cl, grid leak bias is established by the combination of  $C_1$  and  $R_1$ . This is somewhat different than the grid leak bias explained in the Amplifier Section of this Handbook, since in this application only negative pulses are used.

When the input signal used is first applied, the current through C<sub>1</sub> is maximum and the total input voltage is dropped across R, with electron flow through R<sub>1</sub>, placing the control grid at a negative potential with respect to the cathode. C<sub>1</sub>charges through R<sub>1</sub> for the duration of the pulse. The capacitor then discharges through R<sub>1</sub> for the period between pulses. Before completely discharging, however, C begins to charge again with the application of a new pulse. After a few cycles of operation, an average negative voltage (bias) is, established at the control grid of the tube because of the relation of the time constant of  $C_1 R_1$  to the duty cycle of the input signal. This negative voltage (bias) establishes the cutoff point for limiting, which is determined from the plate current versus grid voltage characteristic curve of the particular pentode used for  $V_{I}$ . This average negative bias voltage determines where the input signal causes cutoff to occur, and thus, which portion of the input signal will be reproduced.

With the application of the input pulse, plate current flows for that portion of the pulse above cutoff. Once the tube reaches cutoff the current is at zero and remains at this point for all portions of the negative signal beyond cutoff regardless of whether or not the input signal increases. At cutoff, the plate voltage is at its maximum and, likewise, will remain at this limited amplitude for all portions of the input signal beyond cutoff. The plate voltage then decreases to a minimum value when the plate current is brought back to its maximum value by the trailing edge of the negative input pulse. Note that during the entire time the signal is less than the cutoff bias value, no limiting occurs. Thus, in the region from zero bias to cutoff, normal tube amplification action occurs. Hence, limiting occurs only for those input signals which are larger in amplitude than the value of cutoff bias. The larger the input signal, the more effective the cutoff action.

The limited voltage output level is also controlled slightly by the plate and screen grid voltages of the tube since these voltages in addition to the biasing level affect the tube characteristics and control the total amount of plate current flowing. The approximate magnitude of the limited output can be obtained from the product of load resistor  $R_2$  and the plate current (in milliamperes) with no signal applied.

**Circuit Variations.** If the plate current changes between pulses because of a duty cycle change, the effective limiter output voltage is altered accordingly. This plate current change occurs if the duty ratio of the input signal is increased.

Duty Ratio = 
$$\frac{\text{Avg Power}}{\text{Peak Power}}$$

$$\frac{\text{Pulse Width.}}{\text{Pulse Time Period}} = \text{Duty}_{\text{cycle}}$$

This increase in duty ratio decreases the amount of screen grid current flowing, thereby increasing the screen grid voltage. This results in greater plate current flow during the invervals between signals because of the increased voltage on the plate. An additional screen resistor  $R_4$  placed in parallel with  $C_2$  (as illustrated in the dotted lines in the schematic) reduces the effect of any change in plate current by voltage divider action. There will be little shift of screen voltage with increased duty ratio when the current taken by  $R_4$  and  $R_2$  is relatively large compared to the screen current, since the voltage division is fixed at that developed across  $R_2$ .

#### Failure Analysis.

No Output. In a pentode video limiter, a nooutput condition may be caused by any of the following (provided the input signal is the proper value and polarity): an open coupling capacitor C, an open bias resistor  $R_1$  or plate resistor  $R_2$ , or by absence of plate or screen voltage, or by a defective tube V<sub>1</sub>. To determine the component at fault first check the supply voltage and then the plate and screen voltages with a high resistance voltmeter. If the supply voltage is low or zero the trouble is in the power supply or primary fuse. If the supply voltage is normal but the plate voltage is low or zero plate load resistor R, may have increased in value or is open. Likewise, if the screen voltage is low or zero, screen resistor R<sub>2</sub> may have increased in value or is open. Check  $R_1$  and  $R_2$  for value with an ohmmeter Note that zero screen voltage will also occur if screen capacitor C<sub>2</sub> is shorted. Meanwhile the excessive current drain through R, will cause it to heat, smoke, and eventually burn out. Check for a shorted  $C_2$  by

measuring the resistance to ground from the screen terminal. If both plate and screen circuits are satisfactory, check for a signal on the grid of V<sub>1</sub>using a vacuum tube voltmeter or an oscilloscope. If the signal appears on the grid but no output is obtained, check R<sub>2</sub> for proper value and continuity, since an open grid resistance will cause grid-blocking. The blocked grid will be indicated by no output and a large negative grid bias which reduces as the meter is connected from grid to ground substituting for the grid resistor. As the meter is left across the circuit unblocking will occur, and when the meter is removed the grid will again block. This indicates  $R_1$  is either open or so large in value as to be useless. If coupling capacitor C<sub>1</sub> is shorted the plate voltage from the preceding stage will drive V<sub>1</sub> into plate current saturation. Such a condition will be indicated by obtaining identical voltage readings to ground from either side of C<sub>1</sub>, or by checking for a short with an incircuit capacitance checker. If all tests are normal and the trouble persists the tube is most probably at fault.

**Reduced or Distorted Output.** This condition may exist because capacitor  $C_1$  is shorted, resistor  $R_1$  is open, screen grid bypass capacitor  $C_2$  is shorted, plate and/or screen voltage is reduced, or tube  $V_1$  is defective.

With  $C_1$  shorted dc plate voltage from the previous stage will drive the grid of  $V_1$  positive into saturation and cause a reduced output. An open  $R_1$  will result in grid blocking and may cause audio oscillations at a slow rate. A shorted  $C_2$  will result in reduced screen and output voltage and may also result in the burning **out** of resistor  $R_3$  because of excessive screen currents. A reduced plate or screen grid voltage caused by an increase in the resistance of  $R_2$  or  $R_3$  will also cause reduced output voltage.

To determine the component at fault, first check the supply voltage and then plate and screen voltages with a high resistance voltmeter. If the supply voltage is low the trouble is in the power supply. If the supply voltage is normal but the plate voltage is low, plate load resistor  $R_2$  may have increased in value. Likewise, if the screen voltage is low screen resistor  $R_3$  may have increased in value. Check  $R_2$  and  $R_3$  for value with an ohmmeter. If zero screen voltage exists screen capacitor,  $C_2$  may be shorted. Check  $C_2$  for shorted condition by measuring the resistance to ground from the screen terminal. If the signal appears on the grid of the tube but the output is not limited to the proper value and the electrode potentials have been checked, check  $R_1$  for proper value with an ohmmeter. If  $R_1$  is not within tolerance this condition will exist. If  $C_1$  is shorted the DC plate voltage from the preceding stage will drive  $V_1$  into plate saturation. This condition is indicated by identical voltage readings to ground from either side of  $C_1$ , or by checking for a short with an in-circuit capacitance checker. If all tests are normal and the trouble persists, the tube is most likely at fault.

# **R-F PENTODE LIMITER (ELECTRON TUBE)**

#### Application.

**The** r-f pentode limiter is used in FM receivers to remove amplitude variations from the i-f signal prior to being applied to an FM detector circuit.

#### Characteristics.

Constant output is obtained once limiting level is reached. Linear amplification occurs up to limiting level.

Screen grid and plate voltage determine limiting level for specific bias.

Grid limiting and plate current saturation limiting are used in conjunction with cutoff limiting.

Best performance is obtained with sharp cutoff pentode-has rapid rise time-has little droop.

#### Circuit Analysis.

**General.** The pentode r-f limiter is located between the last i-f amplifier stage and FM detector stage. Grid current or the plate current saturation type of limiter operation is usually used for r-f limiters. Cutoff limiting is also used with one of the aforementioned methods, but it is not used by itself, since this method can only limit the negative halves of the alternating input waveform.

The pentode, besides offering sharp cutoff characteristics, makes available a greater range of screen grid and plate voltage. Operating the plate at a low voltage produces plate current saturation, as well as plate current cutoff, more readily. In order to do this the plate load resistor must be large enough to produce a load line below the knee of the pentode tube characteristic. Since the magnitude of the plate load resistor can not be made too large in wideband limiter design, grid current limiting must be used where a wideband limiter is required. The effective signal voltage values

that may produce current change, are those between the cutoff of the tube and the point at which grid current flow occurs or plate saturation occurs. These points, then are the limiting levels of the circuit.

**Circuit Operation.** A schematic of a typical r-f limiter circuit using a pentode type of electron tube is shown in the accompanying illustration.



Pentode R-F Limiter

The input signal is inductively coupled from the preceding i-f stages through primary L1 (of Tl) to secondary L2, with Cl and L2 providing the proper tuning and selectivity for i-f output transformer T1. The i-f signal is then capacitively coupled to the grid of V1 through coupling capacitor C2. The combination of capacitor C2 and grid leak resistor RI establishes the bias potential by grid current flow when a signal is applied. Plate load resistor R3 is used to drop the plate supply to the desired value of plate voltage. Screen grid dropping resistor R2 drops the supply voltage to the proper screen voltage value and bypass capacitor C3 places the screen grid at ground potential for i-f. C4 and L3 of (T2) form another tuned i-f circuit which enables the proper band of output frequencies to be inductively coupled by L-4 to the f-m detector. C5 in conjunction with plate load resistor R3 forms a decoupling circuit.

When a positive-going input signal is applied to the grid of limiter V1 grid current flows charging

capacitor C2. The plate of C2 closest to the grid of V1 becomes negative and the opposite plate positive. When the signal swings negative, capacitor C2 discharges through resistor RI. The capacitor discharge current develops a voltage across RI which makes the grid negative with respect to the cathode. When the input signal again goes positive, C2 has not had sufficient time to discharge completely. No further grid current is drawn until the input signal becomes sufficiently positive to overcome the residual negative charge remaining on capacitor C2. Each additional cycle adds a little to the charge that remains from the last cycle. After several cycles of operation an average bias is established, and the voltage across R1 remains relatively constant. This constant voltage across RI establishes the average bias value around which the input voltage fluctuates. This bias point is dependent on several factors, which include the vacuum tube electrode potentials, the time constant of C2 and RI (TC=R1XC2) and the amplitude of the input signal. The last factor determines the amount of limiting performed by the grid leak bias method.

Limiting is accomplished by the instantaneous bias on the vacuum tube varying at the same rate that the peak amplitude of the input signal varies. If, on the positive portion of the signal the peak signal amplitude increases to the point of zero bias level, or about where grid current flows the charge on the plate of capacitor C2 closest to the grid becomes more negative with respect to the other plate. The grid bias is then increased instantaneously by the same amount to a new level and grid current no longer flows because the input level is not large enough to drive the bias to zero or above. This point is the point where limiting occurs, because in effect it is the highest positive voltage that the grid may attain. It is, thereby the value at which constant peak plate current flow occurs and the value for which minimum plate voltage is obtained.

This stable or constant (limited) plate output voltage can also be obtained by **lowering** the screen grid and plate voltage values to where plate current saturation, rather than grid current flow occurs, when the positive portion of the input signal reaches or exceeds the desired positive peak voltage. At this point plate current is maximum and will no longer increase to signal amplitude. Since plate current is maximum, then the plate output voltage is minimum, and remains at this limited minimum for any increase in input signal amplitude. Although this method facilitates reaching cutoff with a less negative-going signal because of the lower electrode potentials, it is somewhat restricted by the magnitude of the plate load resistor. In order for plate saturation to occur before grid current flow, the plate load resistor value must be increased to decrease effective dc potential at the plate. By increasing the size of the **plate** load resistor, however, the usable bandwidth of the limiter is lowered. Grid current **limiting** is therefore preferred for wide-band applications even though in order for cutoff to occur a greater negative half cycle of voltage must be present.

When the input signal is operating over the negative half-cycle, the bias is also established by the grid RC time constant, the electrode potentials and the amplitude of the negative half cycle. If the magnitude of the negative half cycle is sufficient cutoff bias occurs. Plate current no longer flows at this cutoff point and plate voltage is at its maximum value. Thus, when the negative half cycle reaches or exceeds the cutoff bias level, plate output voltage remains at a constant limited value.

Limiting will ordy occur when the signal amplitude exceeds the voltage extremes necessary for grid current to flow on the positive **half** cycle, or (on the negative half cycle) for cutoff to occur. Any signal strength less than these amplitude extremes **will** result in plate current changes and plate voltage variations in accordance with this signal strength and no limiting. In order to have a constant limited output, then, the input (drive) signal strength must exceed the points where grid current flow and cutoff occurs.

# Failure Analysis.

**No Output.** In a pentode r-f limiter a no-output condition may be caused by any of the following (provided the signal from the previous stage is the proper value): a shorted input tank circuit capacitor Cl or output tank circuit capacitor C3, an open or shorted transformer T1 or T2, an open coupling capacitor C2, an open bias resistor R1, or by lack of plate voltage caused by an open plate resistor, R3, or a shorted plate bypass capacitor, C5, or by a defective tube VI.

To determine the components at fault, first check the supply voltage, then the plate and screen voltages with a high resistance voltmeter. If the supply voltage is normal but the plate voltage is low or zero, plate load resistor R3 may have increased in value or

opened. Check R3 for value with an ohmmeter. To check if capacitors C 1, C3, C4, or C5 are shorted, use an in-circuit capacitance checker. If the capacitor C2 is open or if T1 is defective, no signal would be present at the grid of V1. This maybe checked by an oscilloscope. If the plate circuit is satisfactory and a signal appears at the grid of V1, but there still is no output, check resistor R1 for proper value and continuity, since an open grid resistance will cause grid blocking. The blocked grid will be indicated by no output and a large negative grid bias which reduces as the voltmeter is connected from grid to ground substituting for the grid resistor. As the meter is left across the circuit the blocking action will subside. When the meter is removed the grid will again become blocked. This indicates that RI is either open or so large in value that it is useless.

If **T1** is open or shorted no input signal will be applied to the grid of **V1**. Likewise, if T2 is open or shorted no output will be obtained. Check the resistance value of the corresponding transformer primaries and secondaries with an ohmmeter (be certain to turn off the plate power before measuring). If the resistance value obtained is zero, the winding is shorted. If the value obtained is infinite, the winding is open. If all tests are normal and the trouble persists, the tube is most likely at fault.

Low or Distorted Output, This condition may exist because of capacitor C2 being shorted, capacitor Cl being open, resistor R1 being open, L1 being defective because of a partial short or tube V1 being defective.

If C2 is shorted, d-c plate voltage from the previous stage will drive the grid of VI positive, and into saturation, causing a reduced output. If Cl were open, i-f transformer T1 will not resonate at the proper i-f and loss of gain will result Thus, there will be little or no output. An open resistor RI will result in grid blocking and may cause audio oscillations at a slow rate. If screen bypass capacitor C3 is shorted, the screen and output voltages will both be reduced and eventually will result in resistor R2 burning out because of excessive screen current. If screen bypass capacitor R3 is open, resistor R2 will have dropped across it the r-f voltage occurring at the screen grid, which will produce degeneration and result in altered screen and plate currents, and plate voltage. Reduced screen or plate voltage, caused by increased resistance of R2 or R3, will also cause a reduced output voltage.

If capacitor C4 is open, the tuned circuit of L2 and C4 will not be resonant to the proper i-f frequency band. If C5 is open, the r-f voltage appearing at the plate will be fed back into the power supply through R3 and cause feedback with possible oscillation.

To determine the component at fault, first check the supply voltage and then the plate and screen voltages with a high resistance voltmeter, If the supply voltage is low the trouble is in the power **supply**. If the **supply** voltage is normal but the plate is low, plate load resistor R3 may have increased in value. Likewise, if the screen voltage is low, screen resistor R2 may have increased in value. Check R2 and R3 for proper value with an ohmmeter.

A reduced plate or screen voltage may also be caused by open capacitors C3 or C5. Check C3 and C5 with an in-circuit capacitor checker if prior checks have failed to find the fault. This same check (incircuit capacitor checker) may be used if symptoms seem to indicate open capacitors Cl or C4. If V1 is at a constant saturation level, check Cl for a short by measuring the voltage from each plate of Cl to ground with a high resistance voltmeter, or by checking for a short with an in-circuit capacitor checker. If symptoms indicate trouble in either input or output tank circuits and capacitors C 1 and C4 are not defective, remove one lead of the suspected winding and check the dc resistance value of the winding. If all tests are normal and the trouble persists the tube is most likely at fault.

# PART 13-3. CLAMPERS

# DIODE CLAMPER (ELECTRON TUBE)

# Application.

The diode **clamper** (sometimes called a dc restorer) is used where it is desired to hold, or "clamp", the positive or negative extreme of a waveform to a zero reference level (the reference **level** for this circuit must be ground potential). This circuit is commonly used in radar, television, telemetering and pulse code communications, and computers.

# Characteristics.

Input signal waveform contains both positive and negative amplitude extremes.

Output signal waveform varies between the reference level (ground) and some negative or positive value, which is determined by the peak-to-peak amplitude of the input waveform.

Input and output signals are in phase with one another.

Uses diode in conjunction with an R-C coupling network; cathode of diode is at ground (chassis) potential.

# Circuit Analysis.

**General.** The diode clamper circuit consists essentially of a diode connected in parallel with the resistor or a conventional R-C coupling network. The diode can be connected to clamp the waveform either negatively or positively. Since the two circuits are so similar, only the negative diode clamper will be discussed in detail. The positive diode clamper will be explained only briefly at the end of the discussion.

In the negative diode clamper, the diode is connected so that whenever the waveform swings in a positive direction the diode conducts to produce a short R-C time constant; whenever the waveform swings in a negative direction the diode does not conduct, and this results in a long R-C time constant. Thus, two different time constants are produced – a short time constant during the positive half cycle of the input waveform, and a long time constant during the negative half cycle. It is this difference in time constants that produces the clamping action for the output waveform.

**Circuit Operation** A negative diode clamper is shown in the following illustration, together with typical input and output waveforms. Capacitor Cl and resistor **R1** form an R-C coupling network and determine the long time constant of the circuit. Electron tube V1 is an indirectly heated cathode-type diode; it is the clamper diode and, together with capacitor Cl, determines the short time constant of the circuit. The filament (heater) circuit for the diode is not shown in the schematic.



**Negative Diode Clamper Circuit and Waveforms** 

The input waveform shown in the preceding illustration is typical of a square wave generated at the plate of a multivibrator stage. The waveform can be considered **as** the plate-voltage variation which is applied to the input of the clamping circuit. initially the plate voltage of the multivibrator stage is low (+20 volts) while the tube is conducting heavily the plate voltage rises to a high value (+100 volts) when the tube is non-conducting, or cut off. Thus when the stage is in operation a square wave is produced which has an 80 volt peak-to-peak amplitude. Coupling capacitor Cl of the **R-C** network is initially charged to a potential of +20 volts, which is the plate voltage of the multivibrator stage when the tube is conducting heavily.

The circuit conditions at this time are indicated by point A on the input and output waveforms of the accompanying illustration. Immediately following point A on the input waveform, the input to the clamper circuit suddenly rises 80 volts (from +20volts to +100 volts) to point B. Since the charge on capacitor Cl cannot change immediately, the 80-volt change appears across resistor RI and also across diode V1. This makes the plate of diode V1 80 volts positive with respect to its cathode, and the diode conducts to charge capacitor Cl through a short time constant path. When conduction begins, the output voltage drops from point B on the output waveform to zero (reference level).

At point C on the input waveform, the input signal drops 80 volts (from +100 volts to +20 volts), but capacitor C 1 is charged to **+100** volts and cannot change instantaneously; therefore, an 80-volt drop in signal voltage appears across resistor R1, causing the output to drop from zero (reference level) to -80 volts. Thus, between C and D on the waveforms, the input voltage drops from +100 to +20 volts, and the output voltage drops from zero (reference level) to -80 volts. During the time interval between points D and E on the waveforms, capacitor Cl will discharge slightly through the long time+ **onstant** path offered by resistor RI until point E is reached.

At point E on the input waveform, the input signal again rises 80 volts (from +20 volts to +100 volts) to point F on the input waveform. Once again the charge existing on capacitor Cl cannot change immediately, and the 80-volt change appears across resistor RI. However, an 80-volt change causes the output voltage to overshoot the zero reference level slightly because of a slight discharge of capacitor Cl which has occurred during the time interval between points D and E. Therefore, because of the voltage overshoot, a small positive voltage exists across resistor R1 and diode VI. The plate of the diode is positive with respect to its cathode, and the diode conducts momentarily to replace the slight loss of charge on capacitor Cl. The output quickly drops and remains at zero (reference level) until point G is reached. The input signal again drops (from +100 volts to +20 volts), and an 80-volt drop in signal voltage appears across resistor R1, again causing the output to drop from zero to -80 volts. Thus, between points G and H on the waveforms, the input voltage drops from +100 to +20 volts, and the output voltage drops from zero to -80 volts. Once again, capacitor

Cl begins to discharge through resistor R1 to complete another cycle.

The output waveform has purposely been drawn to show a substantial decrease in voltage caused by the discharge of capacitor Cl during the period of time the input waveform is at its negative extreme (point D to point E). In practice, however, the value of resistor RI is relatively large, and very little distortion results from the discharging of capacitor Cl through Rl, or from its charging through diode V1 (at point F).

From the explanation of the negative clamper operation given above, it is seen that the positive extreme of the input waveform has been held, or clamped, to the desired zero reference level and the entire waveform has been shifted negatively with respect to the reference level.

A positive diode clamper is shown in the accompanying illustration, together with typical input and output waveforms. The circuit operates in the same manner as the previously described negative diode clamper, except the diode is reversed, resulting in opposite polarities at the output, and the waveform is thus clamped positively instead of negatively.

#### Failure Analysis.

**General.** Because of the relative simplicity of the negative diode clamper circuit, the failure analysis is also relatively simple and is limited to several possible failures.

Initially, the input signal should be checked to determine whether it is present and of the correct waveshape and amplitude. The diode, VI, should be checked to determine whether it is in satisfactory condition and whether the correct filament (heater) voltage is applied to the tube. In many cases a dc potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor Cl to become ieaky (or shorted) and cuase a voltagedivider action to occur. Since capacitor Cl is in series with resistor R1, a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. Furthermore, in this case it is likely that diode V1 will conduct at all times A quick check to determine whether coupling capacitor Cl is leaky (or shorted) is to remove diode VI from the circuit and check for the presence of voltage developed across resistor R1.



Positive Diode Clampar Circuit and Waveforms

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. As a result, distortion will occur during the time required for capacitor C 1 to reach a new reference level, which results from a change in signal amplitude. If the value of resistor R1 decreases considerably, distortion of the output waveform will occur because of the decrease R-C time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since only three components are involved in the circuit (resistor Rl, capacitor Cl and diode Vi), these components are easily checked to determine whether they are defective. Resistor RI can be measured with an ohmmeter to determine its resistance, capacitor Cl can be checked with a suitable capacitance analyzer, and diode VI can be checked in a tube tester.

# **DIODE CLAMPER (SEMICONDUCTOR)**

### Application.

Same application as electron tube version.

#### Characteristics.

Some basic characteristics as electron tube version, but uses semiconductor diode instead of electron tube.

#### Circuit Analysis.

**General. The** unbiased diode clamp is usually employed as a shunt across the resistor of an R-C coupling circuit. By providing a low-resistance path during conduction periods and a high-resistance path during nonconducting periods, the diode provides different charge and discharge times for the coupling capacitor. The diode can be connected to clamp the waveform either negatively or positively. Since the two circuits are so similar, only the negative diode clamper will be discussed in detail. The positive diode clamper will be explained only briefly at the end of the discussion.

In the negative diode clamper, when the positive portion of the input waveform causes the diode to conduct, negative clamping is produced, as described in the following paragraph.

**Circuit Oparation.** The schematic of a basic unbiased diode clamp is shown in the following illustration. As shown, Cl is the coupling capacitor of an RC coupling network. Resistor R1 is the input resistor of the network and determines the long time constant (discharge period) of the circuit. Clamping diode CR1 connected in shunt with R1 determines the short time constant (charging time) of the circuit. When a positive input signal is applied it causes CRI to conduct, and Cl is quickly charged to the input potential. Since the output is taken from across R1 which is effectively short circuited by the conducting diode (forward resistance is only a few ohms), little or no output appears for the positive portion of any applied signal. During the negative portion of the input signal CRI does not conduct (except for reverse leakage current) consequently the negative portion of the input signal appears as the output across R1. This circuit acts to effectively shift the entire waveform in a negative direction by holding the positive peak of the input signal to the zero level. Therefore the input waveform can only appear as a negative output. Thus the positive portion is effectively eliminated by the clamping diode.



**Negative Clamp** 

In the following illustration, the input waveform is shown as a square wave for ease of explanation. Likewise, the input waveform level is considered to vary from +2 to +10 volts. Such an input signal is typical of the waveform generated at the collector of an NPN transistor multivibrator (or an electron tube). Although a square wave is used in the following explanation of detailed circuit operation, any wave shape applied to the clamper input will be negatively clamped without appreciably changing the shape of the wave (provided the R1 Cl time constant is long with respect to the pulse duration).

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**ClamPar Input and Output Waveforms** 

Capacitor Cl is charged as indicated in the preceding illustration to a potential of +2 volts at the negative peak of the input waveform (to). At time t<sub>1</sub>the input to the clamper circuit rises 8 volts to a +1 O volts. Since capacitor Cl cannot change its charge immediately, the 8 volt change appears across RI and CR1, producing a positive spike on the output waveform. Since the anode of CR] is now 8 volts positive with respect to its cathode, CR1 conducts and charges Cl to +10 volts. The charging of Cl occurs rapidly because of the low forward resistance of the diode, and the low forward resistance of the diode shunting RI causes any output voltage appearing across R1 to drop to zero during time  $t_1$  to  $t_2$ . Simultaneously) the diode stops conducting, and capacitor Cl remains in its charged condition for the duration of the pulse.

At  $t_2$  the input signal drops 8 volts (from +10 volts to +2 volts). Since C 1 is charged to +10 volts and cannot discharge immediately through the long time constant circuit created by R1, this negative-going voltage appears across R1 as a negative 8 volt output. (CR1 cannot conduct because its anode is now negative with respect to its cathode). Thus a

point  $t_2$  on the waveform, the input voltage drops from +10 volts to +2 volts, and the output drops from zero to -8 volts. During the time interval between  $t_2$  and  $t_3$ , capacitor C1 discharges slightly (from 8 volts to 7 volts, for example) through the long time constant path of R1.

At point  $t_3$  of the input waveform, the inPut signal again rises 8 volts (from +2 to +1 O). Once again the charge on Cl cannot change immediately and the 8 volt positive change appears across RI. Because of the assumed 1 volt discharge through R1 between times  $t_2$  and  $t_3$ , the 8 volt change now exceeds the capacitor charge voltage. Therefore, the output voltage overshoots the zero reference level and a positive (approximately 1 volt) signal appears across R1 and CR1. With the anode CR1 positive with relation to its cathode, the diode conducts momentarily to replace the slight loss of charge on Cl. As a result, the output voltage quickly drops to zero and remains at zero level until the end of the pulse at time  $t_4$ .

At time  $t_4$  the input signal again drops from +10 to +2 volts. The 8 volt drop appears as a negative output across R1 causing the output voltage to drop from zero to -8 volts. Once again, Cl begins to discharge through the long time constant circuit as explained previously.

The output waveform has been purposely drawn to show a substantial decrease in voltage caused by the discharge of Cl during the duration of the negative peak of the input waveform (times  $t_2$  to t,and t, to  $t_s$ ). In practice, however, the value of R1 is relatively large so that little distortion results from the discharging of Cl or from its charging through CR1. The semiconductor diode, however, does have a much lower reverse resistance that of the electron tube. Since this back resistance is effectively connected in parallel with RI, it lowers the overall output resistance and reduces the value of the long time constant. Therefore, more distortion is produced by the semiconductor diode clamper than the tube diode.

From the explanation of circuit operation **given** above, it is seen that the positive extreme of the input waveform has been held or clamped to zero reference level, and that the entire waveform has been shifted negatively with respect to this reference level.

'The schematic of a basic unbiased diode clamp and its associated waveforms are shown in the following illustrations. The circuit operates in the same L

manner as the previously described negative diode clamper, except the diode is reversed, resulting in opposite polarities at the output, and the waveform is thus clamped positively instead of negatively.



**Positive Clamper** 



**Clamper Input and Output Waveforms** 

#### Failure Analysii.

**General.** Because of the relative simplicity of the diode clamper circuit, there are only a few possibilities of trouble. The capacitor, resistor, and diode can be checked for shorted or open-circuited conditions with an ohmmeter. Circuit functioning, however, must be checked with an oscilloscope to determine whether the waveform is correct and the operation is normal.

No Output. An open-circuited capacitor, a lack of input signal, or a shorted or defective diode can cause a no-output indication. Use an oscilloscope to determine whether the proper input signal is present and whether it appears across RI.

**Low Output.** A leaky or partially shorted capacitor can cause other than normal output. Usually such a condition will be indicated by a change in the dc voltage measured across RI, assuming a normal input signal. A defective diode can also cause this condition, and is usually indicated by a much-lower-thannormal reverse resistance.

**Distortion.** Normally there should be no distortion of the output signal. Any distortion visible on an oscilloscope (with a frequency response high enough for the pulse used) indicates a change in circuit time constants due to defective components. Use an "incircuit" type of capacitor checker to determine whether the capacitor is leaky. The reamining elements can be checked with an ohmmeter. (Be certain to observe the proper polarity when checking the diode; otherwise, an erroneous indication will be obtained.)

**Clamping Level Changes.** A change in the clamping level could be caused by a defective diode, a leaky coupling capacitor, Cl, or a change of input pulse amplitude. As long as the input pulse amplitude is constant clamping will occur as described above. If, however, the pulse amplitude varies from pulse to pulse, the low amplitude pulses will not be properly restored. This action occurs because the low amplitude pulse is unable to reach the zero level or rise above it. Thus the diode can not operate to restore the charge lost in the discharging of capacitor Cl through the long time constant circuit between pulses. Hence the following pulse will start at some point below the zero level. If excessive, it may be possible to read a negative voltage across R1.

In the case of a leaky capacitor, the diode will conduct constantly for a positive voltage (NPN collector polarity) applied to the anode, or with a constant negative voltage (PNP collector polarity) applied it will act as a biased **type** clamp. This condition may be determined by making a voltage check with a VTVM connected across the output of the clamp.

## **BIASED DIODE CLAMPER (ELECTRON TUBE)**

#### Application.

The negative-biased diode clamper is used when it is desired to shift and hold the reference level (negative extreme for positive diode clamper, or positive extreme for negative diode clamper) of the applied signal to some negative value.

The positive-biased diode clamper is used when it is desired to shift the reference level of the applied signal in a positive direction. This type of circuit is commonly used in radar, television, and computers.

# Characteristics.

Establishes a dc reference level of a signal, but does not affect its amplitude.

"The reference level is always a negative or positive value equal to **the** negative or positive bias voltage.

Input and output voltages are in phase.

Uses a diode, an r-c network, and a bias voltage supply.

A negative-biased diode clamper may be used as either a positive or negative clamper.

#### Circuit Analysis.

**General.** A diode clamper (positive or negative) is connected so that whenever the signal **swings** in one direction (positive direction for negative clampingnegative direction for positive clamping) diode VI conducts to produce a short r-c time constant; whenever the signal swings in the opposite direction diode V1 does not conduct, and this results in a time constant dependent on a resistor in parallel with the diode and coupling capacitor Cl, which is long with respect to the time constant of the resistance of the diode and the coupling capacitor. Thus, two different time constants are produced; a short time constant when V1 is conducting and a long time constant when V1 is not conducting.

The output voltage is obtained across the parallel combination of the diode and the resistor. During the short time constant all of the input signal voltage is developed across the coupling capacitor and none is developed across the diode and resistor, and thus no output is developed. During the long time constant, practically none of the signal voltage is developed across the coupling capacitor and practically all of the signal voltage is developed across the resistor and diode, and thus practically all of the signal appears at the output.

The clamping level is dependent on the input voltage value; normally the clamping occurs at a zero voltage reference level and extends in a positive or negative voltage direction to a voltage value equal to the peak to peak input voltage. With the insertion of a negative bias voltage the reference level is shifted in a negative direction. A negative or positive diode clamper having a negative bias will have the minimum negative voltage of the output at a reference level equal to the value of the bias voltage. A negative diode clamper (biased positive) will have its highest positive value as the reference level. The reference level will be, in any case, a value equal to the value of the bias voltage.

Because of the similarity between the negatively biased and the positively biased diode clampers, only the negatively biased diode clamper will be discussed in detail. The positively biased diode clamper will be explained briefly at the end of the discussion.

**Circuit Operation.** A negatively biased negative diode clamper is shown in the following illustration. Capacitor Cl and resistor R1 form an r-c coupling network and determine the long time constant associated with the circuit. Electron tube V1 is an indirectly heated cathode type of diode. This diode during the time of its conduction, shunts R1 and together with capacitor Cl determines the short time constant of the circuit. Voltage source  $E_{\kappa}$  provides a



Negatively-Biased Negative Diode Clamper (Tuba Type)

negative bias voltage which alters the reference level from zero to a negative reference level equal to the bias potential.

The input waveform shown in the accompanying illustration is a typical square wave. Prior to  $t_i$  on the signal voltage waveform there is no input voltage.

Prior to  $t_1$  on the output voltage waveform, the output voltage is maintained at the bias voltage value. At t, first leading edge of the input square wave occurs. Since Cl cannot instantaneously charge to this value, the full signal voltage appears on the plate of V1. The output voltage at  $t_1$  is the algebraic addition of the voltage across V1 and the negative bias voltage. Capacitor Cl charges rapiclly, however, because of the very small time constant (with respect to the frequency of the input signal) of Cl and the small resistance of V1 during its conduction. The output voltage diminishes to the bias voltage at the same rate that Cl charges. This voltage diminishes well before t, is reached. Then the input signal reaches t<sub>a</sub>, capacitor Cl again cannot change its charge instantaneously, and a high negative voltage appears on the plate of V]. Therefore, diode V1 does not conduct and all the voltage appears across R1. The output voltage at t, is the algebraic sum of the negative voltage across R1 and the negative bias voltage.

During the pulse period between  $t_2$  and  $t_3$  capacitor C 1 discharges slightly through R1 for the duration of the negative pulse. Since the time constant of R1 and Cl is large, however, only a slight amount of this voltage leaks off. The amount of the voltage that discharges through RI subtracts from the voltage originally applied across **R1** at  $t_2$ . Hence, at  $t_3$ , the initial negative charge is less than at  $t_2$ , accounting for the dip in the waveform.

When t<sub>3</sub> is reached and the input signal rises in a positive direction V1 conducts, and capacitor C1 again cahnot respond instantaneously to the rapid change. Hence the full voltage appears across the diode. The output voltage this time, however, is not only the voltage across V1 plus the bias voltage but it is this algebraic addition minus the voltage that is present across RI. Since the voltage across RI has been reduced by the discharge of Cl, the voltage across R1 is less than the voltage across V1 by the amount of voltage that has leaked off Cl at t<sub>a</sub>. The output voltage at t<sub>3</sub> is then slightly more postive than the bias. This produces the slight positive peak on the waveform at t<sub>3</sub>, since the anode of V1 is more positive than the cathode, V1 conducts and quickly charges, removing the small pip caused by the initird surge across V1. The output voltage then drops to that of the bias voltage for the remainder of the pulse width, period  $t_3$  to  $t_4$  on the waveform. When  $t_4$  is reached the action is the same as that occurring at  $t_{2}$ and the cycle repeats.

By reversing the diode (see the preceding illustrated circuit), the circuit becomes a negatively-biased positive diode clamper. The positive diode clamper has a positive output and may have either a positive or negative reference level. By retaining the negative bias, the reference level remains negative; by reversing the bias, the reference level is then shifted to a positive voltage. A positively-biased positive diode clamper is shown in the following illustration.

The positively-biased positive diode clamper operates in the same reamer as the previously described negatively-biased negative diode clamper, except the diode and the battery voltage is reversed, resulting in a circuit operation that is opposite the previous discussion.



positively-Biased Positive Diode Clampar (Tube Type)

#### Failure Analysis.

**General.** Because of the relative simplicity of the positively or negatively biased positive or negative diode clamper circuit, the failure analysis is also simple and is limited to only a few possible failures.

Initially, the input signal should be checked to determine whether it is present and of correct waveshape and amplitude. If the bias battery or supply voltage should become open no output would be obtained. If the bias supply voltage should become shorted, an output would exist but the reference level would be shifted to zero instead of some positive or negative value. In many cases, a dc potential exists at

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the input of the clamper circuit; therefore, it is possible for coupling capacitor Cl to become leaky (or shorted) and cause a voltage divider action to occur. Since capacitor Cl is in series with resistor RI a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. If the value of RI decreases considerably, distortion of the output waveform will occur because of the decreased r-c time constant, and as a result, undesirable spikes will be present in the output waveform.

There should be little difficulty in determining the component at fault, since there are only four components in the circuit. Resistor RI may be measured with an ohmmeter to determine if the value is within tolerance. Capacitor Cl maybe checked with a capacitor analyzer or by measuring the voltage from each plate of Cl to ground (if the voltages measured are equal, the capacitor is shorted). If every other component has been checked and the trouble still exists, diode V1 must be at fault.

#### **BIASED DIODE CLAMPER (SEMICONDUCTOR)**

#### Application.

Same application as electron tube version.

#### Characteristics.

Essentially the same characteristics as electron tube version, but uses semiconductor diode instead of electron tube diode.

Because the reverse resistance of a semiconductor diode is lower than that of an electron tube, the type of diode used is selected to have a very high reverse resistance. This is necessary to keep the shunting effect of the reverse resistance to a minimum.

#### Circuit Analysis.

**General. The** biased diode clamper may be of either the positive or negative type, depending upon the relative connection of the diode with respect to the bias. Under all circumstances, the reference level

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of the negatively-biased diode clamper will be at some negative value, and the reference level of the positively-biased diode clamper will be at some positive value. Since these two types of biased clampers are so similar, only the negatively biased diode clamper will be discussed in detail. The positively biased diode clamper will be explained only briefly at the end of the discussion.

In a negatively-biased positive diode clamper, the output waveform will start at this negative value and extend in a positive direction. If it is a negativelybiased negative diode **clamper**, the output waveform will start at this negative reference level, and extend in a negative direction. The circuit is comprised basically of a diode and an RC network. The diode acts as a switch, closing on one hrdf cycle to provide a very short RC time for the capacitor, and opening on the alternate half cycle, to provide a long time constant which depends upon the size of a resistor in conjunction with the capacitor. The overall result at the output is a reproduction of the input, but shifted to a new reference level.

**Circuit Operation.** A typical negatively-biased negative diode clamper is shown in the following illustration.

Capacitor Cl and resistor R1 form an RC **coupling** network and determine the long time constant associated with the circuit. Diode CR1, during the time of



NeWtively-Biased Negative Diode Clamper

its conduction, together with Cl, determine the short time constant associated with the circuit. The bias supply,  $V_{cc}$  alters the reference level from zero to a level equal to the bias.

When the circuit is initially energized and with no signal applied to the input, the diode begins conducting because of the negative potential ( $V_{CC}$ ) applied to the cathode. As CR1 conducts, capacitor Cl begins charging, and when its charge is equal to  $V_{cc}$ , the diode cuts off, since its anode and cathode potentials are now equal. The voltage at the output is at this **timeequal** to the bias voltage  $V_{cc}$ , or -1 volt.

When a signal is applied, as illustrated, the following action occurs. At time t<sub>i</sub>, the voltage increases almost instantly from O volts to a +5 volts. (The voltages used here are only for ease of explanation), Capacitor Cl cannot change its charge immediately (because of the property of capacitors), and the anode of CR1 suddenly becomes more positive than its cathode and begins conducting. Because Cl cannot immediately change its charge, the entire input voltage is developed across the diode, and the output, taken from across the diode, increases 5 volts in a positive direction. Because it does not start at O volts, but at O -1 volt, as shown on the illustration, the output rises to +4 volts. The conducting state of CR1 provides a very short time constant for the capacitor, however, and Cl rapidly charges to the new voltage. As Cl charges, the voltage drop across CR1 decreases, and once again reaches -1 volt when Cl is fully charged.

The output remains at this voltage until the negative swing of the input signal at time t<sub>2</sub>. At this time the input swings from a + 5 volts to a - 5 volts. Again, Cl camot immediately change its charge, but this time the diode camot conduct, because its anode is negative with respect to its cathode. The entire input voltage is therefore developed across RI, and the output voltage changes 10 volts in a negative direction from the -l-volt reference level, or to-11 volts. Because the diode is not conducting, R1 provides a long time constant for Cl and the capacitor begins charging very slowly to the -5 volts of the input signal. The capacitor charges very slowly because of the long RC time constant, and when the input signal reaches t<sub>3</sub>, the total output has only decreased to, for example, from -11 to -10.5 volts (the capacitor has charged to .5 volt). At time t<sub>3</sub>, the input again rises to +5 volts, bringing CR1 into conduction. This sudden +10 volt rise also produces a +10 volt increase in the output. Since the total output is 10.5 volts at this time, a +10 volt increase brings it up to -.5 volts, which accounts for the small positive-going peak at t<sub>3</sub> in the output waveform. Because of the short RC

time provided by CR1, the capacitor quickly charges again to -1 volt eliminating the peak, and the output remains a -1 volt until time  $t_4$  when the cycle again repeats.

By reversing the diode, the circuit can be converted into a negatively-biased, positive diode clamper. The difference at the output then will be that the entire output waveform will be clamped above the negative bias voltage, instead of below it as in the negative clamper.

By reversing the **battery**, the circuit can be converted into a positively-biased diode clamper. The following illustration shows a typical positively-biased positive diode clamper. The operation is essentially the same as the negatively-biased diode clamper, except that with this circuit arrangement, the output voltage is always clamped at some value of positive voltage, as determined by the bias voltage. The circuit can be converted to a positively-biased negative diode clamper by reversal of the diode.



**Positively -Biasad Positive Diode Clamper** 

## Failure Analysis.

**No Output.** The absence of an input signal, or an open Cl are the only probable causes of a no-output condition. Check for the presence of the input signal with an oscilloscope. If the signal is not present, the fault lies in a preceding stage, and the cfamper is probably not defective. If a signal is present, check Cl with an in-circuit capacitor checker. There is also the possibility that two components such as CR1 and  $V_{cc}$ , or R1 and  $V_{cc}$ , are both shorted at the same time, thus producing a short circuit across the output. Check the bias supply with a high resistance voltmeter for proper voltage, and RI and CR1 with an

ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the special case where the diode is not completely shorted, but reads a very low resistance, of say 2000 ohms or less, it can be considered defective.

Low or Distorted Output. A partially shorted CR1, a leaky Cl, or RI decreasing in vrdue can cause a low output condition to exist, Actually, the output will not be low without being distorted nor will it be distorted without being low. Check Cl with an incircuit capacitor checker, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the case where the diode is not completely shorted, but reads a very low resistance of, say 2000 ohms or less, it can be considered defective,

**Change in Clamping Level.** A change in the bias supply voltage,  $V_{ee}$ , will cause the output clamping level to change. Check for the proper value of voltage with a high resistance voltmeter.

# **TRIODE** CLAMPER (ELECTRON TUBE)

#### Application.

L

A triode clamper is used where it is desired to obtain amplification of the input signal as well as clamp one extreme of the signal.

#### Characteristics.

Clamping is accomplished between the grid and the cathode, the grid acting as a diode plate.

Clamping between the grid and the cathode can only be in a negative direction, since the coupling capacitor must be connected to the grid of the triode.

Output taken from the plate of the triode will be clamped in a positive direction.

# **Circuit Analysis.**

**General. The** circuit operation of the basic singletube triode clamper is largely similar to that of the diode clamper. In the triode clamper, the control grid serves the same function as the diode plate in the diode clamper circuit. The grid-leak bias resistor and coupling capacitor in conjunction with the grid to cathode **resistance** of the triode provides a means by which two time constants may be produced. These

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time constants enable a certain bias level to be established, which **fixes** the reference level to which the output level is clamped.

The grid is maintained as a negative voltage, and since the plate voltage varies inversely and is of opposite polarity, the output voltage is clamped at a positive reference level. The action of the triode also provides amplification of the input signal.

**Circuit Operation.** A basic single-tube tnode clamper is shown in the accompanying illustration. Cl and RI are the input coupling capacitor and the grid leak bias resistor, respectively. They form the long time constant circuit associated with the **clamper**. The cathode to grid resistance of triode VI during the time of maximum conduction along with Cl form the short time constant circuit associated with the clamper. R2 is the plate load resistor, which also provides the proper dc plate voltage to the plate of V1.



Basic Single-Tube Triode Clamper

The input signal is a typical square wave, having equal positive and negative amplitudes as shown in the following illustration. Prior to the application of the square wave at time  $T_o$ , the output voltage 1s held at a certain level due to the plate voltage being developed across the plate load resistor R2. This

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voltage value **constitutes** the reference or clamping level of the output voltage. Times  $t_1$  and  $t_3$  represent the leading edges, and times  $t_2$  and  $t_4$  represent the trailing edges of the input square wave.

At time  $t_1$ , the first positive-going leading edge occurs and appears at the grid of VI. Since capacitor Cl cannot immediately change its charge the entire voltage appears across R1. Grid current immediately flows from cathode to grid and begins charging capacitor Cl. The time required to charge Cl is very short because of the low cathode to grid resistance of V1. As Cl becomes fully charged, the grid side of Cl becomes negative, and the grid is at the same negative potential. This charging action continually reduces the amount of tube conduction from the time of the initial application of the leading edge of the square wave to the time where Cl becomes fully charged. This varies the plate output voltage from some negative value to some positive value (the reference level) where it remains constant for the duration of the pulse, until the trailing edge of the input waveform is reached at time t<sub>2</sub>. At t<sub>2</sub>, the negative-going trailing edge of the input signal causes a negative voltage to appear across R1 and on the grid of V1. The negative grid swing causes the plate current to reduce, and the plate output voltage, therefore, rises to nearly the full value of the supply (goes **positive**). At this time, the input signal reaches its maximum negative swing and the output voltage reaches its maximum positive swing. For the duration of the pulse to time  $t_a$  long time constant path is offered through R1 to discharge Cl, since V1 is no longer conducting from grid to cathode (no grid current is flowing). Because of the long time constant and the relatively short pulse width time, Cl discharges only slightly before the next positive leading edge of the input signal appears at t<sub>a</sub>. Thus the output signal drops a few volts. At time t<sub>a</sub> the positive-going input signal drives the grid of V1 positive so that grid current flows. Meanwhile the increased plate current causes the plate voltage to drop below the clamping level because of the slight loss of voltage during the discharge period. Actually, during this period, the grid voltage is driven above zero bias into the positive region and conduction through the short time constant path through the grid to cathode current quickly charges Cl to the clamping level, and removes the overshoot pip on the grid waveform. Thus, the dip in current below the clamping level in the plate circuit is minimized by grid current drawn by V1, and the plate current then remains constant until the trailing edge of the input pulse at  $t_4$ . At  $t_4$  the cycle again repeats, and action is the same as described for the period between  $t_2$  and  $t_4$ . Actually, the distortion shown in the illustration of the output waveform is exaggerated to facilitate understanding circuit action. In practice the time constant of **C1** and **RI** is sufficiently large that very little distortion of the waveform occurs.



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# Failure Analysis.

**No Output.** If a square wave signal within the design limitations of the triode clamping circuit is applied to the input of the circuit a "no output" condition may be the result of no plate voltage existing at the plate of VI. This may be due to a faulty plate supply voltage source or due to an open plate load resistor, R2. The only other faulty component that would result in a "no output" condition is a faulty triode V1.

In order to determine which component is the cause of the "no output" condition, first check to see, with an oscilloscope, if the correct input signal is applied. If a correct signal is applied, check for the presence of plate voltage. If no plate voltage is present, check resistor R2 with an ohmmeter. If R2 is an acceptable value of resistance, check the plate supply voltage source with a high resistance voltmeter to determine if any plate supply voltage exists. If there is no plate supply voltage, try to adjust the source for the correct voltage value. If all these components have been checked and the "no output" condition stiU exists the triode must be faulty.

Low or Distorted Output. If a "low or distorted output" condition exists it may be due to the square wave input signal not being within the design limitations of the triode clamping circuit. This condition may also be due to any of the following component failures: open or shorted input capacitor Cl, open or shorted grid leak resistor R1, shorted plate load resistor R2, incorrect value of **plate** Ebb, Or a defective triode V1.

To determine why the output is low or distorted, first check the square wave input signal with an oscilloscope. Check the capacitor Cl with an in-circuit capacitor checker to determine if it is open, or measure the voltage from both sides of Cl to ground to determine if Cl is shorted. (If the measured voltages are equal the capacitor is shorted.) Check resistor R1 with an ohmmeter. If resistor RI has an acceptable resistance value, check resistor R2 with en ohmmeter. If resistor R2 has an acceptable resistance value, measure, the value of the plate Voltage supply,  $E_{bb}$ , with a high resistance voltmeter. If the plate supply voltage is incorrect, try to adjust the plate voltage supply source for the correct voltage value. If all these components have been checked and the "low or distorted" condition still exists, the triode must be defective.

#### TRIO DE, BASIC COMMON-BASE CLAMPER

# Application.

The basic common-base triode clamper maintains between specific voltage levels the maximum positive and negative voltages developed at the collector of the transistor used in the clamping circuit. This circuit is usually used as a switching amplifier to maintain a constant output pulse amplitude.

#### Characteristics.

Common base transistor configuration provides an output with no current amplification and no phase inversion.

Collector voltage is clamped, not the output voltage.

Two diodes provides clamping action.

Diode bias potentials establish minimum and maximum clamping levels.

# Cirouit Analysis.

General. The clamping action to be discussed occurs in the collector circuit of the common base connected transistor. Normally, the signal voltage in conjunction with the series combination of the collector load resistor and the collector supply voltage develops a certain collector voltage. If the input signal varies above some level, however, one of two diodes begins conducting. These diodes are connected in parallel with each other and with the collector supply and load. The conduction of the diode maintains or clamps the collector voltage at the bias value. If the signal varies below some level in the opposite direction the other diode conducts, causing the collector voltage to be maintained or clamped at another lower voltage level. During the time that the signal is between clamping levels, the collector voltage varies in accordance with the input signal voltage variation.

Circuit Operation. The circuit of the triode, basic common-base clamper used in this application is shown in the accompanying illustration.



Triode, Basic Common 6ese Clamper

The input signal voltage, as illustrated, is a squarewave pulse type signal which may vary from maximum to minimum amplitudes. It is applied to the emitter of transistor Q1, connected in a common base configuration. The collector voltage variation corresponds to the input voltage variation and is developed across the collector load resistor, R1, by the collector supply voltage  $V_{ccB}$ . Diode CR1 and its base voltage  $V_{cR1}$  establish a negative clamping level, below which the collector voltage cannot go. Diode CR2 and the bias voltage  $V_{CR2}$  establish a Positive clamping level above which the collector voltage cannot go.

The input signal applied to the emitter of Q1 is amplified and in-phase when it appears as the output voltage at the collector of Q1. If the output voltage developed at the collector of Q1 is between the voltage limits of VCR  $_1$  and  $V_{CR2}$  the diode cannot conduct. The collector voltage varies in accordance with V<sub>CCB</sub> minus the output voltage developed across RI  $(V_{R1})$ , which depends upon the collector current. Once the input signal varies enough to cause the positive collector voltage swing to exceed the value of  $V_{_{\mbox{\scriptsize CR2}}}$  (resumed to be -2 volts), diode CR2 conducts because the anode is driven positive and forwardbiases the diode. The collector voltage is then maintained at the value of  $V_{CR2}$  until the signal voltage drops to a point at which the the positive collector voltage swing becomes less than the voltage  $V_{CR2}$ , at which time CR2 becomes reverse biased, stops conducting, and the collector voltage is again dependent on V<sub>CCB</sub> minus V<sub>R1</sub>.

If the input signal varies enough in the opposite (negative) direction to cause the collector voltage to become the same as, or more negative than the value  $V_{CRI}$  (assumed to be -8 volts) diode CR1 is forward-biased and conducts. The collector voltage is then maintained at the value of  $V_{CRI}$  until the signal voltage increases to a value where the collector voltage becomes more positive than the voltage  $V_{CRI}$ , at which time diode CR1 is reverse biased, stops conducting, and the collector voltage is again dependent on  $V_{CCB}$  minus  $V_{R1}$ .

By clamping both the positive and negative levels, the transistor is prevented from saturating and causing hole storage effects which would increase the pulse length, or from being driven to cutoff when the input is in the other direction. It also has the advantage of not requiring **special** selection of transistors at the time of replacement, since the operating limits are made such that any transistor of the same type will operate satisfactorily in this circuit. This circuit is not used with sine-wave inputs except where clipping effects are desired.

#### Failure Analysis.

**No-Output.** A no-output condition may prevail due to any of the following defects: no input signal present at the emitter of Q1, an open or shorted **collector** supply **voltage**  $V_{CCB}$ , an open collector load resistor, R 1, or a defective transistor, Q1.

The location of the cause of the no-output condition may be found by first determining if an input signal is present with an oscilloscope. If the input signal is present, check collector supply voltage,  $V_{CCB}$ , with a voltmeter. If the collector supply voltage is present check resistor R1 with an ohmmeter. If all other possibilities have been checked and a nooutput condition still exists, transistor Q1 can be considered defective.

Low or Distorted Output. This condition may be due to a faulty input signal. If the input signal is found to be correct by an oscilloscope the low or distorted output condition may be due to any of the following conditions: improper voltage values for, collector supply voltage  $V_{CR1}$ , or bias voltage  $V_{CR2}$ ; shorted or open diodes CR1 or CR2; or a load resistance (Rl) which is not the proper resistance value; or a defective transistor, Q1.

To determine which of the possible causes of the low or distorted output condition is responsible; first,
check the voltage values  $V_{CCB}$ ,  $V_{CR1}$ , and  $V_{CR2}$ with a high resistance voltmeter. If any of these values is incorrect adjust the particular voltage source for the proper value. If these voltages are correct, check diodes CR1 and CR2 with an ohmmeter. If the diodes are good, the ohmmeter will read zero resistance when placed across the diode in a forward direction, and will read infinite resistance or a very high resistance when placed across the diode in the reverse direction. If the diodes are good, check resistor R1 with an ohmmeter. If all of the preceding items have been checked and found satisfactory, transistor Q1 must be the faulty component. input is coupled through capacitor Cl directly to the output. The series combination of triode V1, triode V2, and cathode bias resistor R2 intersects this input line (between capacitor Cl and the output) at the point where the cathode of V1 and the plate of V2 are connected. Capacitor C2 couples a series of negative synchronizing pulses to the grids of triodes V1 and V2. Resistor R1 develops a potential difference (bias) between the cathode and the grid of V2 during the time of the synchronizing pulse. Capacitor C3 is an ac bypass capacitor for cathode bias resistor R2.

# SYNCHRONIZED TRIODE CLAMPER (ELEC-TRON TUBE)

# Application.

A synchronized triode clamper is used in television and radar circuitry where it is desired to hold a signal voltage to a zero reference level and allow the signal to vary both positively and negatively from the zero reference level.

## Characteristics.

Uses two triodes connected in series. Clamping occurs between input signal variations. Synchronizing pulses are required.

# Circuit Analysis.

**General.** A synchronized triode clamper utilizes the conduction of two triodes to maintain a specific reference level during the time that no signal is present. At the time that the input signal occurs, a negative synchronizing pulse drives the triodes into a nonconducting state for the duration of the synchronizing pulse. The duration of the synchronizing pulse and the duration of the input signal are the same. Any variation in the voltage between input signals (when the triodes are conducting) changes the amount of conduction of the triodes and changes the amount of plate voltage and plate resistance is such that the output voltage is maintained at the reference level.

Circuit Operation. A typical triode clamping circuit is shown in the tollowing illustration. 'I ne



# Synchronized Triode Clamper

The input signal, in this case, is a series of positive and negative going sawtooth waveforms extending from the zero voltage reference line. There is a steady-state period with no signal variation between the sawtooth waveforms.

A synchronizing pulse signal is applied to capacitor C2. This synchronizing pulse signal consists of negative pulses equal in duration to and occurring at the same time as the sawtooth waveforms. The period between each sawtooth, therefore, is equal to the period between each synchronizing pulse. A diagram of the corresponding time and amplitude relationships of the input, synchronizing, and output waveforms is shown in the following illustration.



**Clamper** Waveforms

At the time either a positive or negative sawtooth waveform is applied to the input of capacitor C 1, a negative synchronizing pulse is applied to the synchronizing input through capacitor C2 and applied to the grids of triodes V1 and V2. This synchronizing pulse cuts off the triodes V1 and V2 for the duration of the pulse, which is equal to the period of the sawtooth waveform. When the duration of the synchronizing pulse is likewise completed, and triodes V1 and V2 return to conduction, forming a voltage divider network. This voltage divider consists of the two triodes and a cathode bias resistor R2 in a series connection, extending between **plate voltage supply** Ebb and ground.

If there should be any voltage at the input that varies from the zero reference line, at this time, the conduction of the triodes will vary in such a way as to compensate for the voltage variation and to maintain the output at the zero reference. If this voltage variation is positive, the voltage at the cathode of V1 and the voltage at the plate of V2 is made more positive. The increased plate voltage of V2, in most cases, is relatively ineffective in changing the amount of conduction of V2. The increased voltage at the cathode of VI, however, causes the grid voltage to appear more negative, thereby increasing the bias. (This positive increase in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2). The conduction of VI is then reduced causing the plate resistance of VI to increase, thereby causing a greater voltage drop across VI. With the increased voltage drop across V1,

there will be less voltage available at the plate of V2, and thus at the output. This voltage decrease at the plate of V2 and at the output is equal to the positive voltage variation occurring at the input. The output voltage is, therefore, maintained at the zero reference level.

If the voltage variation, at the time that triodes VI and V2 are in the state of conduction, is negative, the voltage at the plate of V2 and at the cathode of V1 is negative. The voltage decrease at the cathode of V1 causes the grid voltage to appear more positive, thereby decreasing the bias. (This decrease in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2.) The conduction of V1 is increased causing the plate resistance of V1 to decrease and causing the voltage drop across V1 to decrease. A more positive voltage is then present at the cathode of VI, at the plate of V2 and at the output. This voltage increase is equal to the negative voltage variation at the input. Thus output voltage is maintained at the zero reference level for a negative voltage variation as well as a positive voltage variation.

#### Failure Analysis.

**No Output.** A "no output" condition may be due to any of the following failures: an open coupling capacitor C 1, an open synchronizing pulse capacitor C2, no input signal, or no synchronizing pulse train. These failures may be located by measuring capacitors Cl and C2 with an in-circuit capacitor checker, and by observing the input signal with an oscilloscope. If either the input signal or the synchronizing pulse train is not present at the respective inputs, check the input signal source or the synchronizing pulse source with an oscilloscope. If the "no-output" condition still exists after these checks have been made, a bad connection somewhere in the circuit must be the cause.

Low or Distorted Output. A low or distorted output may be due to any of the following defects (provided the proper input signal is applied): Iow or no plate supply voltage, improper synchronizing pulse, open or shorted resistor R2, open or shorted resistor R1, open or shorted capacitor C3, shorted capacitor C 1, shorted capacitor C2, or, if the condition still exists after checking these components, triode V1, or triode V2, or both triodes must be defective.

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To determine which of these components is at fault, first check the input signal with an oscilloscope. If the input signal is correct, proceed to the synchronizing pulse input and check the synchronizing pulse train with an oscilloscope. If either the input signal or the synchronizing signal is incorrect the trouble is not in the clamping circuit, but is in same stage prior to the clamper. If the synchronizing pulse train is correct, check the plate supply voltage with a high resistresistance voltmeter. If the plate supply voltage is corcheck resistors RI and R2 with an ohmmeter. Check capacitor C3 with an in-circuit capacitor checker, or by measuring the voltage from both plates of C3 to ground. If both voltages are equal the capacitor is shorted. If all components are found to be satisfactory the fault must be in either triode V1 or triode V2, or in both triodes.

#### PART 13-4. WAVESHAPING CIRCUITS

# **R-C DIFFERENTIATOR**

#### Application.

The R-C differentiator is used to produce a pip or peaked waveform, for timing or synchronizing purposes, from a square or rectangular-shaped input signal. It is also used to perform the electrical analog of differentiation for computer applications. It may also be used to produce specifically distorted waveshapes for special applications, such as trigger and marker pulses.

#### Characteristics.

Input waveshape distorted (nonsinusoidal). Short time constant R-C network used. Functions essentially as a high-pass **filter**. Output taken from across the resistor. No amplification produced.

#### Circuit Analysis.

**General.** The output of a differentiator is proportional to the rate of change of the input **signal**. For a

rising (positive-going) input the differentiator produces a positive puke, for a falling (negative-going) input it produces a negative pulse, and, for a constant input it produces no output. The differentiator electronically simulates the mathematical operation of taking the first derivative. Second, third, and fourth derivatives may be obtained by cascading an equivalent number of differentiators. Theoretically the differentiator is accurate only when the output voltage is very small in comparison with the input voltage. In practice, this is achieved by using the shortest possible time constant for the highest frequency component involved in the waveform being differentiated. For computer, fire control, and similar operations, differentiation of the basic signal voltage produces an output voltage that represents the speed of the object, double differentiation yields the acceleration of theobject, and triple differentiation yields the rate of change of acceleration. For timing and synchronizing use, a sharp pulse is produced for each leading edge and trailing edge of the input waveform. Although the circuit provides no amplification, for a square-wave input the peak output of the differentiator is twice that of the input signal, a positive pulse being produced for the positive leading edge and a negative pulse for the negative trailing edge. For other nonsymmetrical waveforms, since no d-c component is passed through the coupling capacitor, a peak output less than the maximum is obtained, and the output waveform is arranged about the average vrdue as a zero axis. When differentiated, a triangular pulse will produce a rectangular output; a sinusoidal wave will not be changed in shape, but the signal will be shifted in phase and reduced in amplitude. The accompanying figure illustrates the various outputs for different input waveforms.

**Circuit Operation.** The basic R-C differentiator is shown in the following schematic. The input is applied between the capacitor and ground, and the output is taken across the resistor. Usually this R-C combination constitutes the input or interstage coupling network; especially where R-C coupling is used.



### **Differentiated Waveforms**

When the reactance of capacitor C at the highest frequency to be passed is negligible, the entire input voltage is applied across the resistor. The capacitor quickly charges on the leading edge of the input



## **Differentiating Network**

pulse, and this high-frequency signal is passed, essentially without attenuation, to the input of the following amplifier or control stage. When the time between the leading and trailing edges of the input signal is relatively long (greater than 10 time constants), the capacitor charges, producing a peaked waveform, and remains in the charged condition until the trailing edge occurs. The trailing edge then allows the capacitor charge to be impressed across the resistor, and the capacitor discharges, producing another peaked waveform; however, this time it is of reversed polarity, after which it remains at rest until the next input puke. The passage of the charging current through resistor R develops the voltage which is the output of the differentiator. An exaggerated version of the differentiator current and voltage waveforms is shown in the following illustration.



#### **Differentiator Current and Voltages**

The exact functioning of the differentiator is easy to understand by considering the charge on coupling capacitor C, shown in the schematic drawing. Referring to the current and voltage waveforms of the preceding figure, assume a 100-microsecond squarewave input, with a 100-volt amplitude. At time to, capacitor C is assumed to have no charge, and the leading edge of the square wave is applied. Since the charge, or voltage on the capacitor cannot change instantaneously, but takes a finite time, a high current flows through resistor R and creates a large pulse of voltage, which is in effect the leading edge of the square wave passed through the capacitor. During the interval between time t. and t., the capacitive charging current through C decreases in an exponential manner. The time required to charge or discharge the capacitor is determined by the circuit time constant. In this instance, assume that C is 100 picofarads and R is 100 kilohms; then the RC time constant is 10 microseconds. From the universal time constant chart in Section 2, it is seen that in 50 microseconds (5 time constants) the capacitor will have charged to 99.3% of the maximum possible charge, and that in

# **ELECTRONIC CIRCUITS**

100 microseconds (10 time constants) a complete charge (or discharge) is assured. The current and voltage illustration shows the capacitor charging current for the 100-microsecond period (the figure is also a representation of the output voltage of the differentiator). Between t. and  $t_1$  the square wave amplitude is constant and, since there is no change, the differentiator does not produce an output. The capacitor voltage changes from zero toward a maximum value of 100 volts (assuming no losses); the charging voltage is bucked by the capacitor voltage, thus producing the exponential charging rate. By the end of period  $t_1$  the capacitor is fully charged and the negative-going trailing edge of the input signal occurs, causing an instantaneous high flow of discharge current through R. Between  $t_1$  and  $t_2$  capacitor C discharges in a manner similar to that of the charge, and the negative differentiated spike is produced across R. To be a true mathematical derivative of the input voltage, the capacitor voltage must equal the input voltage, and the current will be proportional to the derivative of the input voltage. This condition can be approached by reducing the vrdue of R until practically all of the voltage developed appears across the capacitor instead of the resistor. At this time R is practically a short circuit and no output exists. Therefore, in practical differentiators, the time constant is reduced to as small a value as possible. Usually a time constant of 1/10th the period of the input pulse produces satisfactory output spikes. The effect of reducing the time constant can be understood by referring again to the preceding illustration of current and voltage waveforms.

Assume a time constant of only 1 microsecond; then in 10 microseconds the capacitor is fully charged, and the circuit rests for 90 microseconds until another change occurs. Actually, since usually only the top portion of the differentiated signal is selected for use, the approach to a true thin spike is practically achieved and the effective charging period occurs for only a few microseconds. For timing, marker and synchronizing uses, the width of this spike in some cases is not very critical, since the leading edge rather than the trailing edge is used. Where the trailing edge is used, the width of the spike is important. In computer use, where the mathematicrd analog is important, both R and the time constant are reduced to the lowest possible value. Practical limitations imposed on these values are the input and output resistances of the stages between which the differ-

entiator is connected, and stray capacitance across the differentiator output produces a capacitive voltage divider effect, which limits the output voltage to a lower value than the applied input voltage. Also, when the percentage change in capacitance is on the order of 20% of the value of C, the RC time constant is affected. With the example given in the figure, a stray capacitance of 20 picofarads (because of wiring, parts placement, etc) is one-fifth (or 20%) of the vahre of C, and this would effectively change the charge time. Or, considering the stray capacitance as producing a frequency-selective effect, it is clear that the high frequencies in the input signal (which cause the effect that the differentiator utilizes) would tend to be bypassed to ground, leaving only the low frequencies, which have a slow rate of change and produce little effect on the differentiator.

### Failure Analysis.

**No Output.** Since only two components are involved, it is evident that only an open circuit at the input, or a short circuit at the output, could produce a no-output condition (open capacitor or shorted resistor).

Distorted Output. Only a change in component values or associated stray capacitance and resistance values could change the time constant and waveshapes. Distorted output is usually caused by improper input signrds. When checking the waveform at the differentiator, the effect of the shunt resistance or capacitance produced by the test instrument input should be considered. When distortion is discovered in the following tube circuits, it is probably caused by improper action in these circuits. A direct check of the output as compared with the input to the differentiator using a high-impedance oscilloscope, will indicate whether the circuit is performing properly. A shorted capacitor or an open resistor would cause the output to be a duplicate of the input (no differentiation taking place).

#### **R-L DIFFERENTIATOR**

#### Application.

The R-L differentiator is used to distort an applied waveform (such as a square wave) into a peaked wave for the purpose of providing trigger and marker pulses. It is also used to electronically perform the mathematical function of differentiation in computers, and for separating the horizontal sync in television receivers.

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#### Characteristics

Produces distortion of the input waveform.

Has a short time constant.

Output is taken from across inductor.

Functions essentirdly as a high-pass falter.

Output is similar to the output of an R-C differentiator.

# Circuit Analysis.

General. The output of a differentiator is proportional to the rate of change of the input signal. For a rising (positive going) input the differentiator produces a positive pulse, for a falling (negative going) input it produces a negative pulse, and for a constant input it produces no output. The differentiator electronically simulates the mathematical operation of taking the first derivative. Second, third, and fourth derivatives may be obtained by cascading an equivalent number of differentiators. Theoretically the differentiator is accurate only when the output voltage is very small in comparison with the input voltage. In practice, this is achieved by using the shortest possible time constant for the highest frequency component involved in the waveform being differentiated. For computer, fire control, and similar operations, differentiation of the basic signal voltage produces an output voltage that represents the speed of the object, double differentiation yields the rate of change of acceleration. For timing and synchronizing use, a sharp pulse is produced for each leading edge and trailing edge of the input waveform.

**Circuit Operation.** A schematic of a basic R-L differentiator is shown in the following illustration.

The input is applied between the resistor and ground, and the output is taken across the inductor. The time constant (in seconds) of an R-L circuit is found by dividing the inductance (in Henrys) by the resistance (in ohms) TC=L/R. Thus to shorten the time constant of an LR circuit it is necessary to increase resistance R rather than decrease R as in the R-C circuit. The counter emf produced in an inductor causes it to have the property of opposing any change in current flow. By referring to the universal timeconstant chart in Section 2 of this Handbook, it is noted that the inductor voltage decreases from the applied voltage at an exponential rate to approximately zero at the end of 5L/R time intervals. Likewise, when the source is removed, a counter emf of opposite polarity is induced in the inductor, and this

tends to keep current flowing. This voltage also decreases at an exponential rate. Thus, if a square pulse having a time duration of 5L/R time intervals is applied, a peaked waveform appears as the output voltage. This output waveform has a shape that is similar to the output obtained from an R/C differentiator.



**Basic R-L Differentiator Circuit** 

The exact functioning of the differentiator maybe easier understood by referring to the following illustration.



Differentiator Waveforms

With a square wave pulse of 100 volts amplitude applied as an input signal at time to, the output is a positive 100 volts spike. At this time there is no voltage drop across resistor R, since the inductive effect of L is to build up instantly a back emf that equals the applied signal and prevents instant current flow through the inductor. Between time t. and t<sub>1</sub>current begins to flow through inductor L and a small voltage drop is developed across resistor R. As the current flow through R increases, the voltage drop (shown in dotted lines in the waveform figures) increases. Meanwhile, the voltage developed across the inductor, e<sub>L</sub>, is decreasing, and, since the output is taken across L. it is also decreasing (the decrease of voltage across coil L representa the voltage used in building up a magnetic field around L). The sum of the voltage drops across R and L equal the applied voltage. The current through inductor L increases exponentially and the voltage across resistor R increases, likewise. Since the time constant assumed in the illustration is 10 microseconds and the pulse width is 100 microseconds the steady-state condition is reached before the pulse ends. Since there now is no change in current, there is no voltage developed across the inductor and the output voltage is zero. At time t the trailing edge of the input pulse occurs and drives the signal in a negative direction. Instantly a negative 100 volt spike appears across L and at the output. At the same time, the field around the coil collapses and produces a current through L in the opposite direction. During time t to t2 the negative voltage across the inductor decreases exponentially while the current increases exponentially. As the current flow through R increases, the voltage drop across it, likewise increases, and the sum of the voltage drops across R and L equals the applied voltage. With the 10 microsecond time constant and 100 microsecond pulse width, the steady state condition is again reached before the pulse ends. Since there now is no change in current, there is no voltage developed across the inductor and the output voltage is zero. At time t<sub>2</sub>, the positivegoing leading edge of the pulse appears and the cycle repeats.

The following illustration shows the differentiated output waveforms for several different input waveforms.



Differentiating Effects upon Different Waveforms

Although the circuit provides no amplification, for a square wave input, the peak output of the differentiator is twice that of the input signal. A positive pulse is produced for the positive leading edge and a negative pulse for the negative trailing edge.

With a sine-wave input the output remains a sinewave as shown in part B of the illustration, the only differences being that the output sine-wave is of a smaller amplitude and is advanced in phase. The advance for a perfect differentiator is 90 degrees, but 89 degrees is not uncommon.

The sawtooth, shown in part C of the illustration is converted into a low amplitude square wave. Part D illustrates effect of a differentiator upon the application of a complex waveform.

Since the inductor has distributed (turns) capacitance across it, undesired resonant responses may occur in L-R circuits containing large **values** of inductance; therefore, the use of these networks is usually limited to high frequence applications.

#### Failure Analysis.

**No Output.** Since only two components are involved, it is evident that only an open circuit at the input, or a short circuit at the output, could produce a no-output condition.

Low or Distorted Output. Only a change in component values or associated stray capacitance, inductance, and resistance values could change the time constant and waveshapes. Distorted output is usually caused by improper input signals. When checking the waveform at the differentiator, the effect of the shunt resistance or capacitance produced by the test instrument input should be considered. When distortion is discovered in the following tube circuits, it is

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probably caused by improper action in these circuits. A direct check of the output as compared with the input of the differentiator using a high-impedance oscilloscope, will indicate whether the circuit is performing properly. A shorted resistor or an open coil would cause the output to be a duplicate of the input (no differentiation taking place).

# **R-C INTEGRATOR**

# Application

**The** R-C integrator is used as a waveshaping network in radio, television, radar, and **computers**, as well as many other special electronic applications.

# Characteristics.

Input waveshape distorted (non-sinusoidal).

Produces a distortion of the input waveform.

Provides a wider range of time constants than an

R-L integrator.

Has a long time constant. Output is taken from across the capacitor. Has the configuration of a low-pass falter. No amplification is produced.

# **Circuit Analysis.**

**General.** The R-C integrator circuit works in almost exact opposition to the R-C differentiator. It has a long time constant, and the output is taken from across the capacitor. The time constant of the integrator circuit should be 5 times (or more) the period of one alternation of the input waveform, for the circuit to electronically perform the mathematical operation of integration. As in the case of the differentiator, this action in practice is approximate, but the approximation can be made very close.

The higher the resistance in the R-C integrator, the more closely the output voltage follows the ideal integrator waveform. However, the higher this resistance, the smaller the output voltage. Conversely, decreasing the resistance in the R-C integrator circuit, results in a shorter time constant and a higher output voltage. However, as the resistance is reduced in value, the output voltage departs from the ideal integrator waveform. In fact if the resistance, (and time constant) of the R-C circuit is sufficiently reduced, a point will be reached where the circuit no longer acts as an integrator. The output of an integrator is in the form of a voltage that represents the average energy content of the input signrd. For example, if the input is a steady d-c voltage, the same voltage will appear at the output, but, if the input is in the form of a series of narrow, widely separated pulses, the output voltage will be only a fraction of the input pulse vrdue.

**Circuit Operation.** A schematic of a basic R-C integrator is shown in the following illustration.



**Basic R-C Integrator Circuit** 

As the square wave voltage applied to the input of the circuit goes positive, the capacitor charges exponentially at a rate determined by the time constant of the circuit. This time constant is calculated by multiplying the value of the resistor by the value of the capacitor (T=RC). For instance, a circuit contain-ing a lOOK resistor and a 50 picofarad capacitor would have a time constant of 5 microseconds, and if the value of the capacitor was increased ten times to 500 picofarads, the time constant would be ten times longer or 50 microseconds. The rise in voltage across the capacitor occurs as the voltage acorss R decreases from its maximum value. The voltage drop across the capacitor is always the difference between the input voltage and the voltage drop across the resistor. The rise in voltage across the capacitor occurs only for the duration of the applied square wave puke. When the applied voltage drops from its maximum value, the d capacitor discharges exponentially at the same rate

that it charged, due to the time constant of the circuit. This gradual decrease in voltage across C effectively causes a negative pulse across R. If a square wave is applied to an R-C integrator circuit, a nonsymmetric saw-tooth waveform is produced. The principle of integration is used in saw-tooth generators to produce the linear rise in voltage by using a long time constant circuit, and to use only the straight portion of the exponential change waveform for linearity.

The following waveform illustration shows the integrating effect of various time constants on a square wave.



## **Effects of Changing Time Constant**

As can be seen from the waveforms in the illustration, a short time constant integrator does not change the input waveform very much except to distort the high frequency portions of the waveform (leading and trailing edges), and the low frequency (flat) portion is practically unchanged. As the time constant is changed to a medium value time constant, the waveshape changes to that of a rounded-off triangle

(sweep waveform). With a moderately long time constant, the triangular waveform is equally distributed about the central zero axis and the sides are practically straight. When the time constant is made extremely long, is consists of somewhat elongated (stretched) sawtoothed waveforms of reduced amplitude which gradually approach the zero axis, and eventually, after a number of time constants, becomes symmetrically aligned around the center (zero) axis. A short time constant would be considered one which amounted to only one tenth of the pulse duration time. A medium time constant would be of the order of half the pulse duration, while a moderately long time constant would be approximately equivalent to the full pulse width. A long or extremely long time constant would be considered to amount to two or three pulse widths or longer.



Integrating Effect of Different Waveforms

The preceding illustration shows different types of inputs and their respective output for an R-C integrator circuit. The amplitudes of the waveshapes are different and bear no relation to each other as shown in the illustration. When a peaked waveform is

applied to an R-C integrator circuit, the resultant output will be a square waveform. Applying a square wave to the input of an integrator circuit produces an output waveform of triangular shape. The integration of a triangular wave results in a parabolic output wave. Integrating a sine wave with a different amplitude and phase, but with the same sinusoidal wave. shape (usually considered to be a cosine waveform).

# Failura Analysis.

**No Output. Since only** two components are involved, it is evident that only an open circuit at the input, or a short circuit at the output, could produce a no-output condition (open resistor or shorted capacitor). Both of these items could be checked for with an ohmmeter. If the resistor is open the meter will indicate infinity, and if the capacitor is shorted the meter will read zero ohms.

Distorted Output. Only a change in component values, or associated component values, could change the time constant and waveshapes. Distorted output is usually caused by improper input signrds. When distortion is discovered in the following tube or transistor circuits, it is probably caused by improper action in these circuits. A direct check of the output as compared with the input to the integrator using a high-impedance oscilloscope, will indicate whether the circuit is performing properly. A shorter resistor or an open capacitor would cause the output to be a duplicate of the input (no integration taking place). The value of the resistor can be checked with an ohmmeter. While the capacitor can also be checked for a short with the ohmmeter, it is better practice to use an in-circuit capacitance checker, and also to check the capacitor for both proper value and leakage.

# **R-L INTEGRATOR**

#### Application.

The R-L integrator is used as a waveshaping network in various types of electronic equipments such as radio, radar, television and in other special electronic application. It is also used as an **analog** in performing the mathematical function of integration in computers.

#### Characteristics.

Produces distortion of the input waveshape.

Has a long time constant.

Output is taken across the resistor.

Has the configuration of a low pass falter.

Output is in the form of a voltage that represents the average energy content of the input waveform.

#### Circuit Analysis.

Ganaral. An integrating circuit is a circuit whose output is substantially the time integral of its input waveform. The R-L integrator circuit works in almost exact opposition to the R-L differentiator. It has a long time constant and the output is taken from across the resistor. If the time constant of the integrator circuit is 5 times (or more) the period of one alternation of the input waveform the circuit will electronically perform the mathematical operation of integration. This action is approximate in practice, but the approximation can be made very accurate. Since inductor action is the heart of the operation of the R-L integrator a brief review of inductor action follows. The property of inductance is such as to oppose a change in current. This opposition (impedance) exerted by an inductor exists because a counter emf is produced across the inductor by the change in the magnetic field of the inductor, current flow does not rise to a maximum vrdue immediately. Rather, it is initially zero and increases at an exponential rate, as the inductor becomes charged and the counter e.m.f. decreases. Likewise, when the applied voltage is removed, circuit current does not fall to zero immediately, but decreases at an exponential rate as the energy stored in the magnetic field of the inductor is discharged. In the R-L integrator circuit the longer the time constant, the more closely the output waveform follows the ideal integrator waveform. However, the longer the time constant, the smaller is the output voltage.

**Circuit Operation. The** accompanying schematic diagram illustrates a typical R-L integrator.



**Typical R-L Integrator** 

This R-L integrator consists of a series R-L circuit with the output taken across the resistor. The charge and discharge time of the inductor (the time constant) is determined by the values of inductance and resistance in the circuit using the formula TC=L/R. Thus an integrator circuit consisting of a .1 henry inductor and a **10,000-ohm** resistor has a time constant of 10 microseconds.

When a square wave is applied to the input of the integrator circuit the inductor begins to charge. The impedance, caused by counter e.m.f. generated by the expanding magnetic field is initially maximum, but decreases exponentially at a rate determined by the values of L and R as the magnetic field of the inductor approaches its limit. Circuit current, therefore, begins at zero and increases exponentially as the circuit impedance decreases. It is evident that the IR drop (voltage) across the output resistor begins at zero and increases as the inductor becomes charged. If the time constant is very long the increase in output voltage is nearly linear, but the peak of the output waveform attains only a fraction of the amplitude of the input signal, since the inductor attains only a slight charge during the period when voltage is applied to the input. When the input signal falls back to its reference level, the inductor discharges exponentially at the same rate as it charged. The decreasing current induced in the circuit by the collapsing field of the inductor results in a steadily decreasing voltage developed across output resistor R. The output of an integrator circuit with a long time constant (2 or more pulse widths), therefore, is a triangular waveform, which slopes up (positive) during the period when a positive pulse is applied,

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and slopes down (negative) during the period when the input is at its reference level. Conversely, when a negative going pulse is applied to the R-L integrator the output voltage goes negative and when the input voltage returns to its reference level. the output voltage goes positive.

The following waveforms represent the integrating effects of various time constant integrator circuits on a square wave input.



Effects of Various Time constants On A Square Wave

As can be seen from the waveforms in the illustration, a short time constant integrator has little effect on the output waveform, only the high frequency components (leading and trailing edges) are attenuated. As the time constant is increased the output begins to resemble a sweep waveform. A further increase in time constant results in a more linear rise and fall of the output waveform. Notice that the output waveform of the long and very long time constant integrator does not reach the peak amplitude of the input waveform, but is rdways a much lower value.

# Failure Analysis.

No Output. Since there are only two components in the R-L integrator, a no-output condition could only be caused by an open inductor, a shorted resistor, or by no signal input. Both the inductor and the resistor can easily be checked for the above mentioned conditions with an ohmmeter. Presence of the input signal can be determined by observing the waveform present at the input to the integrator with an oscilloscope.

Distorted Output. Generally speaking, an integrator circuit will either function as designed or not at all. However, it is possible for either the inductor or the resistor to change value. This would change the integrator time constant, and the output waveshape would be altered. The resistor may be checked for proper value with an ohmmeter, and the inductor can be checked for proper value with an impedance bridge. It is also possible for the inductor to become shorted or the resistor to become open. This would result in the output being a duplicate of the input (no integration taking place). The components can be checked as explained previously. The most common cause of distorted output is probably distorted input. The quality of the input signal can be easily determined by viewing the waveform present at the integrator input with an oscilloscope.

# SATURABLE-CORE REACTOR PEAKING CIR-CUIT

# Application.

The saturable-core reactor peaking circuit is used to produce a peaked pulse of voltage from a sine wave input.

# Characteristics.

Utilizes a saturable reactor.

Output voltage pulses are in phase with the input signal.

Usually operated near resonance.

Output puke width is determined by the circuit Q.

# **Circuit Analysis.**

General. The saturable-core reactor peaking circuit produces sharp voltage pulses from a sine wave input signal by utilizing the properties of a saturable reactor. A saturable-core reactor is a type of inductor in which a relatively low value of current produces magnetic saturation of the core.

Magnetic saturation of an inductor core can be defined as the point where a further increase in current flow through the inductor windings does not result in any further increase in magnetic field. The property of inductance is such as to oppose a change in current. This opposition (impedance) exerted by an inductor exists because a counter e.m.f. is produced across the inductor, which opposes the applied voltage. If the core of a inductor were to become saturated, the counter e.rn.f. would drop to a low value, and its opposition to current flow (impedance) would also drop to a low value. It is this ability to change impedance that enables the saturable+ ore reactor peaking circuit to produce a pulse output from a sinewave input.

Circuit Oparation. The accompanying schematic diagram illustrates a typical saturable-core reactor peaking circuit.



Saturable-Core Reactor Peaking Circuit

The circuit illustrated above consists simple of conventional capacitor Cl, conventional inductor L1, and saturable core reactor L2. Component values are chosen so that the circuit appears slightly capacitive when L2 is saturated and slightly inductive when L2 is unsaturated (the inductance of L2 decreases when

L2 becomes saturated). To illustrate the capacitiveinductive relationships when L2 is saturated or unsaturated, assume for the sake of illustration that Cl has a capacitive reactance of 100 ohms at the operating frequency and that LI has an inductive reactance of 75 ohms at the operating frequency. Assume further that L2 also has an inductive reactance of 40 ohms when unsaturated and 10 ohms when saturated. The reactance of both Cl and L1 remain constant. It can be seen that during the period when L2 is unsaturated there is a total of 115 ohms of inductive reactance and 100 ohms of capacitive reactance in the circuit. The circuit, therefore, appears inductive since the effect of L1 predominates. Likewise, when L2 is saturated there is 100 ohms of capacitive reactance but ordy 85 ohms of inductive reactance, and the circuit now appears capacitive.

When a sine wave is applied to the saturable+ ore reactor peaking circuit, L2 becomes saturated by the relatively high current flowing through it, and the voltage across L2 is very low, since the inductance of L2 is also very low at this time. Since the circuit is slightly capacitive during the saturation of L2, the current in the circuit leads the applied voltage by almost 90°, and the output voltage is approximately 180 degrees out of phase with the applied voltage, since the voltage across L2 also leads the current by nearly 90°. This output voltage is very low in amplitude, since L2 offers little impedance while in the saturated state. Inductor L2 becomes unsaturated when the input voltage is at a peak, since at this time circuit current is at a minimum due to the 90° phase shift. At this time (when L2 is unsaturated) the inductance of L2 becomes high. This makes the circuit highly inductive and causes the circuit current to lag the applied voltage by almost 90°. However, the voltage across L1 (the output) leads the circuit current by ahnost 90°, since voltage leads current across an inductor and is, therefore, in phase with the input. This condition persists for only a short period of time until the circuit current increases and becomes sufficient to saturate L2. During this short period of time a large amplitude pulse which is inphase with the input is produced. The duration of this pulse coincides with the duration of the unsaturated condition of L2 and is determined mainly by the circuit Q. Thus, a large amplitude positive pulse is produced when the applied sine wave passes through its positive peak, and a large amplitude negative pulse is produced when the applied sine wave passes through its

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negative peak. Since L2 is saturated during most of the input cycle, the output is extremely low except for the short time during the peaks of voltage when L2 is in an unsaturated condition.

#### Failure Analysis.

**No Output.** A no-output condition could result if any component in the saturable reactor peaking circuit became shorted or open. Inductors L1 and L2 can easily be checked by measuring the resistance of the windings and checking for a short or leakage to ground with an ohmmeter. Capacitor C1 can be checked with an in-circuit capacitor checker. Do not overlook the possibility that a no-output condition is the result of no-input. This can easily be checked by observing if the waveform is present at the circuit input with an oscilloscope.

Low Output. Generally speaking, since there are few components involved, the saturable-core reactor peaking circuit will either function as designed or not at all. However, a low-output condition could result from a partially shorted component or from excessive leakage to ground of the windings of L1 or L2, or from a low amplitude input. Resistance checks of the inductor windings and resistance checks to ground, with the bottom of L2 disconnected, should reveal whether or not a partially shorted component or leak age to ground is the cause of low output. The amplitude of the input signal can easily be checked by observing the waveform present at the input with an oscilloscope.

**Distorted Output.** Since the duration of the output pulse is determined mainly by the Q of the circuit, a change in circuit value could alter the Q of the circuit and thus alter the output waveshape. Checks for excessive leakage to ground should be made using an ohmmeter, since leakage to ground would affect the circuit Q. Cl, L1 and L2 can be checked for proper value with an impedance bridge.

# SEMICONDUCTOR PULSE SHAPER

#### Application.

The semiconductor pulse shaper is used in computer, control, and communication equipment to reshape a pulse which has suffered deterioration of its waveshape after passing through a chain of gates. It is also used in conjunction with a multivibrator to form a 1  $\mu$  sec. pulse with sharp leading and trailing edges.

## Characteristics.

Reshapes pulses into pulses with sharp leading and trailing edges.

Utilizes two transistors connected in the commonemitter configuration.

Requires three power supply voltages.

Output pulse width is constant and is determined by circuit components.

Capable of driving several loads.

### Circuit Analysis.

**General.** The semiconductor pulse shaping circuit consists of two common-emitter amplifiers. The first stage, which employs on R-L collector load, performs the primary shaping function and controls the output pulse width. The second stage, an overdrive amplifier, serves as a buffer power amplifier, and in addition squares off the trailing edge of the output pulse.

The output pulse width is primarily determined by the *values* of the inductive load of the first stage and the input capacitor, but is also affected by transistor characteristics, as well as changes in the power supply voltage. In most instances circuit values are chosen which produce an output pulse width of 1 microsecond.

**Circuit Operation. The** accompanying schematic diagram illustrates a typical semiconductor pulse shaper using the commonanitter configuration.



Semiconductor Pulse Shaper

Capacitor Cl couples the input pulse to the base of transistor Q1. Resistor RI and diode CR1 form a voltage divider between ground and the +6 volt bias supply to apply reverse bias to the base of transistor Q1. Inductor L1 and resistor R2 form the collector load for transistor Q1, and capacitor C2 together with resistor R3 forms an interstage coupling network from the collector of Q1 to the base of Q2. Transistor Q2, which is operated as an overdriven amplifier, serves as the output stage, with resistor R4 as its collector load, and diode CR2 limiting the output to the level of the -6 volt power supply.

In the quiescent state (no signal input) transistor Q1 is reverse biased by the positive voltage at the junction of voltage divider R1-CR1. The collector of Q1 is at approximately -6 volts since Q1 forward collector current is cut off, and transistor Q2 is heavily forward biased by the negative collector voltage of Q1 direct-coupled through R3. With Q2 conducting heavily, the output voltage is very close to ground potential. When a negative pulse is applied to the pulse shaper, voltage divider diode CR1 is reverse biased and transistor Q1 is driven into conduction by the charging current flowing through the emitter-base junction of Q1 and into capacitor Cl. The rapid rise in charging current through the emitter-base junction of Q1 rapidly drives Q1 into saturation, and the voltage on the collector of Q1 rises sharply to ground potential. This rapid positive swing in collector voltage on Q1 is coupled through R3 and C2 to the base of output transistor Q2, and Q2 is rapidly cutoff. The collector voltage of Q2 (the output voltage) which was previously held at ground potential due to the heavy conduction of Q2 now rapidly falls to the -6 volt supply level. This is the beginning of the output pulse. The amplitude of the output pulse is maintained at a constant -6 volts by the action of limiting diode CR2. Transistor Q1 is maintained in a saturated state by the charging current of Cl flowing through the emitter-base junction of Q1. This current decreases as Cl becomes charged, but remains sufficient to keep Q1 saturated for the duration of the output pulse. During the period when Q1 is saturated, collector current is limited by the impedance of the load (Ll and R2). Initially, the impedance of L1 is high, but it decreases as L1 becomes charged and collector current increases. Consequently, during the period when Q1 is in saturation, collector voltage on Q1 remains constant and output transistor Q2 remains cut off. Hence, the output voltage remains at -6 volts. When the desired output pulse width is completed, the impedance of LI is so low that the base

drive caused by the charging current of Cl is insufficient to maintain collector current at the previous level. (Base drive decreases as Cl charges). Collector current then decreases rapidly and Q1 collector voltage quickly falls to -6 volts, which drives output transistor Q2 into saturation. The output voltage rises sharply to ground potential as the conduction of Q2 increases. The rapid transition of Q2 from cutoff to saturation is aided by the discharge through the emitter-base junction of Q1, of the energy stored in L1. The term "cutoff" has been used loosely in the preceding paragraphs. Actually the transistors are not cut off in the sense that a vacuum tube can be cut off, since there is always some reverse leakage current flowing, but the magnitude of this current is insignificant. The values of Cl and Ll are the determining factors affecting output pulse width, since the output pulse is completed when Cl and L1 become fully charged and cause the collector current of Q1 to begin decreasing,

## Failura Analysis.

**General.** When making voltage checks, use a vacuum tube voltmeter to avoid the low values of multiplier resistance employed on the low voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. A no-output condition could result from failure of either transistor or failure of one of the power supplies. Semiconductor circuits are generally miniaturized printed circuits. Circuits of this type are subject to shorts caused by a small drop of solder, or any conductive object that may fall across printed circuit leads, or these leads may become open by a hairline crack in the printed board. Plug-in type contacts, often employed in printed circuit boards, sometimes fail to make contact due to dirty or bent contacts. It is often wise to visually check the printed circuit board for evidence of any of the above conditions before attempting to troubleshoot the circuit. Power supply voltages should be checked with a vacuum-tube-voltmeter, and adjusted or repaired if necessary. It should be noted that deterioration with age causing lack of gain may result under high temperature conditions. Unlike vacuum

tubes, however, transistors have operated for years without noticeable deterioration under proper operating conditions. If the transistor is not at fault, a defective circuit component is likely the cause of no output. Voltage checks of transistors elements with a vacuum tube voltmeter, or resistance checks with the circuit deenergized, should indicate the component at fault. Resistors R3 or R4 could cause a no-output condition if they failed, as could diode CRI if it became shorted. Failure of other circuit components could possibly cause a no-output condition to exist, but are much more likely to cause distortion of the output waveshape. This condition will be discussed in detail in the following paragraph. Do not overlook the possibility that a no-output condition is the result of no input signal reaching the pulse shaper. The existance of this condition can readily be determined by observing the waveform present at the input to capacitor Cl with an oscilloscope.

Distorted Output. The term distorted output is used in the following paragraph to describe any output condition other than the proper output with respect to the pulse width, pulse amplitude, and pulse rise and fall time since a circuit defect usually causes more than one of these symptoms of improper output to appear. Defective transistors and improper power supply voltages are often the cause of a distorted output. The power supply voltages should be checked and adjusted if necessary, they should be within 1070 of their nominal values. If the power supply voltages are correct and the transistors are good a defective circuit component is the next most likely cause of improper output. A significant change in the vahre of any component could alter the output waveshape. Since the value of L1 and C1 determine the pulse width a change in the value of these components would, naturally, affect the output pulse width. L1 and Cl can be checked for proper value on an inductance-capacitance bridge. Resistors RI and R2 also affect pulse width but to a lesser degree than Cl and L1. Diode CR2 limits the amplitude of the output pulse to -6 volts. If CR2 opened, the amplitude of the output pulse would increase. The input pulse must be of the correct polarity, and have sufficient amplitude and duration to properly trigger the pulse shaper, if a good output pulse is to be generated. The condition of the input pulse may be checked by observing the waveform present at the input to capacitor Cl with an oscilloscope.

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# PART 13-5. TIME DELAY CIRCUITS

# **BASIC PHANTASTRON CIRCUITS**

#### Application.

The phantastron circuit is used to generate a rectangular waveform, or linear sweep, whose duration is almost directly proportional to a control voltage. Because of its extreme linearity and accuracy, this waveform is used as a delayed timing pulse, usually in radar or display equipment. It is also used to produce time-delayed trigger pulses for synchronizing purposes and movable marker signals for display. For example, it is used as a time-modulated pulse, to indicate antenna position at any instant of rotation, or as a range strobe or delay marker.

# Characteristics.

Operation is similar to the operation of a multivibrator.

Pulse width or delay varies linearly with the applied control voltage.

Requires an electron tube of the pentode or penta. grid type.

Output can be taken from the cathode, screen, or plate, and may be either positive or negative, as selected.

Provides either a low-impedance or highimpedance output, determined by output connections.

May be self-controlled or externally controlled.

# Circuit Analysis.

**General. The** operation of the phantastron circuit is breed on the use of a **Miller-type linear** sweep generator which uses a suppressor-gated pentode, as shown in the following illustration.



Miller Linear Sweep Generator

In the Miller linear sweep generator, the suppressor grid is normally biased (negative) to prevent plate current flow, while the screen conducts heavily. The grid is returned to B+ through a resistor so that it is effectively at zero potential, and the cathode is grounded. When a positive gate is applied to the suppressor, plate current flows and produces a voltage drop across the plate load resistor. This negative-swinging plate voltage is fed back through a small capacitor to the grid, and quickly drives the grid negative; thus, it maintains the plate current at a small value, and also greatly reduces the screen current. Reduction of the heavy screen current produces a large positive swing on the screen, and the tube essentially remains in this condition, producing a positive screen gate. Meanwhile the plate current flows under control of the feedback voltage applied to the grid until no further feedback is produced, During this time the platecurrent increase is linear, and the plate voltage continues to drop. (The normal discharge of C through  $\mathbf{R}_{\mathbf{g}}$  would cause the current through the tube to increase in an exponential manner, thereby causing the plate voltage to drop exponentially. However, any exponential change is fed back to the grid 180 degrees out of phase with the normal discharge of C, thereby causing a linear increase in plate current.) At a point about 2 volts above ground, however, no further plate swing is possible, and the screen again conducts heavily, returning almost to the initial operating point. When the suppressor gate ends, the plate current is cut off, the screen returns to its initial operating point, and the cycle is ready to be resumed under control of the next gate. The following schematic shows the basic Miller circuit. Observe that the screen is not coupled, that a separate bias source is used for the suppressor, and that an external sweep gate is necessary. These are the main ways in which it differs from the phantastron.

From the circuit action described previously, it is clear that changing the applied plate voltage will determine the point, and the time, at which the plate voltage "bottoms" (with respect to the leading edge of the input waveform) and the screen resumes control. Changing the values of feedback capacitor C and grid resistor R will also determine the time of operation (by controlling the speed of the grid-plate feedback action). Both methods of controlling the time are used in phantastron circuits.

**Circuit Operation.** As mentioned previously, there are two basic types of phantastron circuits in use–the screen-coupled and the cathode-coupled. The name is

derived from the manner in which the gate for the suppressor is obtained. Recall that in the Miller circuit a positive gate is developed on the screen during operation; by coupling the screen to the suppressor, either directly or through a capacitor, this gate is used in the screen-coupled phantastron to control operation. A trigger pulse is needed only to start operation, because turn-off is automatic. By inserting a cathode resistor between the cathode and ground, a negative gate is developed and used to control the cathode-coupled phantastron. Each of these circuits will be discussed more thoroughly in the following paragraphs.

Screen-Coupled Circuit, A typical monostable screen+ oupled pentode circuit is shown in the following figure. This circuit is started by a positive trigger applied to the suppressor grid, and at the end of operation it returns to the initial starting condition, ready to repeat the cycle of operation when the next trigger arrives. The output taken from the screen is a rectangular positive gate whose duration, or length, is controlled by R7. In the illustration, tube VI is the basic phantastron, and diode V2 acts as a trigger injector and also as a disconnecting diode to effectively isolate the trigger circuit after the action is started. Diode V3 sets the maximum level of plate voltage as controlled by the position of R7, and, since the turn-off level is fixed, it effectively controls the time during which the circuit produces the linear gate or sweep. Operation occurs at the rate fixed by the discharge of C through R5. In some circuits R5 is made variable to set the maximum time delay, and R7 is provided as an external control to permit selection of the exact time duration required. Feedback capacitor C provides regenerative feedback from plate to grid, to allow quick response to any changes in the plate circuit. Capacitor Cl couples the positive gate from the screen to the suppressor, thereby holding the tube in a condition where the plate current can flow.

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**Basic Screen-Coupled Phantastron** 

Circuit operation can best be understood by referring to the waveforms developed in the tube elements shown in the following illustration, while reading the description of the circuit action. Three steps are involved in the circuit action–turn-on, linear sweep development, and turn-off. Before initiation of action, the circuit is resting with the plate current cut off, because a negative voltage is applied to the suppressor element through R3. Resistors R1, R2, and R3 form a combined suppressor and screen grid voltage divider connected between B plus and C



Waveforms of Scraan-Coupled Phantastron

minus. The values are such that the screen is positive and the suppressor is sufficiently negative to cut off plate current. Since they are directly connected, both elements are dc coupled; also, through capacitor Cl they are ac coupled. Therefore, both dc and ac voltages appearing on one element also affect the other element. Since the cathode is grounded and the grid is connected through R5 to B+, the grid remains near zero bias. Thus, although the plate current is cut off, the screen current is heavy. When a positive trigger is applied to the plate of disconnecting diode V2 through coupling capacitor Cc, the diode conducts, and the positive trigger appears across R3 and is applied to the suppressor of VI. The trigger is large enough to overcome the fixed negative bias and drive the suppressor positive. Therefore, the plate current flows through R4. Since R4 is a relatively large-value resistor, the plate current quickly goes from zero to a low value, and simultaneously the negative swing produced across R4 is applied through C to the grid, driving it from zero to a negative value

of only a few volts, but sufficiently negative to reduce the total cathode current. The grid is now in full control, and the reduction of screen current produces a large positive increase in screen voltage. Through Cl the positive-going screen voltage is fed back to the suppressor so that the action is regenerative; as a result, the tube is quickly triggered from the static condition to the operating condition, which produces a screen waveform with a sharp leading edge. The linear sweep development or timing cycle now begins, with the plate current of V1 increasing steadily. Since the grid is returned to B+, the grid voltage attempts to reach the zero bias level; however, it can change only slowly because the plate side of feedback capacitor C is steadily decreasing, so that any positive grid swing is immediately counteracted by a negative plate swing fed back to the grid. Therefore, capacitor C starts to discharge and electrons flow from the plate of V1, discharging C through R5. Thus C discharges at a rate determined by the time constant of C and R5 (in some circuits R5 is made variable to permit changing the rate of operation). In discharging, the grid side of capacitor C gradually becomes most positive, causing an increased current flow through R4 and producing a constant decrease in plate voltage. The positive increment on the grid is always slightly greater than the negative plate swing it produces; therefore, the grid potential gradually rises, and the plate potential gradually drops. When the plate reaches the point where a voltage change on the grid will produce no further plate-voltage change, the turn-off point is reached. Up to this time a positive gate has been produced in the screen circuit and coupled to the suppressor. A negative gate has been developed on the grid which is smaller in amplitude from the leading edge to the trailing edge by about a volt. (The amount is dependent upon the gain of the tube.)

Since the tube plate voltage is only a volt or so above zero and the plate current can no longer increase, but the grid voltage is still rising toward zero, causing an increase in current flow, the screen

current increases. The moment the screen current increases, the screen voltage drops and feeds back a negative swing through Cl to the suppressor. The suppressor grid then resumes its original negative condition, stops any flow of plate current, and assumes control again. Since this action is regenerative, a sharp trailing edge is produced. Simultaneous with plate current cutoff, the plate voltage swings positive and feeds back to the grid a positive voltage, which helps the grid to return to normal zero bias condition. Since the charge on C cannot change instantly, the plate swing tapers off exponentially and the tube is not ready for another trigger cycle until it has completely recovered. Diode V3, a "platecatching" diode (because of the way it "catches", or arrests, the positive excursion of the plate voltage), operates to catch the plate at a specific voltage, so that with a fixed bottoming point the length of the output pulse and its time duration depend on the plate voltage fixed by V3. The cathode of V3 is biased positive by the voltage divider consisting of R6, R7, and R8, as controlled by potentiometer R7. When the plate voltage of VI is greater than the positive voltage applied to the cathode of V3, the diode conducts and quickly brings the plate voltage of V1 down to the level of the cathode voltage. Thus, the linear sweep action always starts at the voltage set by R7, and the duration of the phantastron gate (or the length of the sweep) is thereby determined. Because the amplitude of the plate sweep depends on the level at which it starts, R7 directly controls the amplitude. The amplitude of the screen gate is determined by the voltage applied and the screen current, and is only slightly affected by R7.

**Cathode-Coupled Circuits. A typical cathode**coupled pentode is shown in the following schematic. This circuit is also started by a positive trigger applied to the suppressor grid and turns itself off automatically like the **screen-coupled** circuit. The output can be taken from either the screen or cathode, or both. The screen output is a positive gate, and the cathode output is a negative gate.



**Basic Cethode-Couplad Phantastron** 

In this circuit, tube VI is the basic phantastron, with diode V3 operating to control the plate voltage level and determine the duration of the output gate. To minimize overshoot on the control grid, cathode, and screen grid (positive on the control grid and cathode, negative on the screen grid), diode V2 is connected between R1 and R2 on a voltage divider network consisting of RI, R2, and R3. (The voltage on the cathode of V2 is normally 1 or 2 volts less than the cathode voltage of V].) Note that no negative supply is needed to bias the suppressor. Cathode bias is used, end the suppressor is held at a lower positive potential than the cathode; thus, it is effectively biased negative with respect to the cathode, cutting off plate current. The screen is drawing current, which produces a positive voltage on the cathode. When a positive input trigger appears across R3, it is applied to the suppressor. This trigger is prevented from affecting the control grid by automatically reverse-biasing diode V2. The grid is normally biased near zero, being held by diode V2 at a potential determined by the voltage divider (R1, R2, and R3) connected between B+ and ground, and the cathode is positive with respect to the grid by approximately 1 or 2 volts. When the trigger is applied, it overcomes the bias between the suppressor and cathode, and plate current flows. The decrease in

plate voltage, due to the flow of plate current, is fed back to the grid through capacitor C, causing the tube current to decrease and the cathode voltage to drop. This drop in cathode voltage further decreases the bias between the suppressor and cathode, and plate current increases further. Since the total tube current is decreasing and the plate current is increasing, the screen current must decrease. This action is regenerative, and plate current will jump from zero to a value determined by the tube characteristics. (Note that the bias between the cathode and suppressor is decreasing, which is regenerative, causing the plate current to increase. The bias between the cathode and grid is increasing. This action is degenerative, which decreases the total tube current. Therefore, there must be a point where these two effects are equal and the current will stabilize for an instant.) At this instant there is no further change in plate voltage, and the grid voltage increases in the positive direction at a rate determined by C and R5, since it is returned to  $E_{bb}$  through resistor R5. This causes the plate current to increase. As the plate current increases, the plate voltage decreases, and this negative change is coupled through C to the grid. It can be seen that his signal is degenerative, and prevents the plate current from increasing rapidly. This action continues, providing a linear sweep until the plate voltage drops to a level at which it can no longer cause an increase in plate current. At this time, degenerative feedback to the grid stops, and the grid will go in a positive direction more quickly. This causes an increase in the total tube current, and thus an increase in cathode voltage, an increase in cathode-to-suppressor bias, and a decrease in plate current. With the total tube current increasing and the plate current decreasing, the screen current must be increasing. It can be seen that the action taking place is regenerative, as the plate will go positive, causing the grid to go positive, and the plate current will go rapidly to cutoff, leaving the tube in its pretriggered condition. The positive swing in the grid is limited by the "catching" diode, V2. Before the circuit is ready for the next cycle of operation, capacitor C must recharge through R3, R2, V2, and R4. As in the screen-coupled phamtastron, this circuit is also of the slow-recovery type.

As stated previously, when the phantastron is triggered there is a large drop in the screen current. This produces a positive waveform on the screen with \_ a steep leading edge. As the tube current gradually increases, producing the linear sweep in the plate

circuit, the screen current increases in the same manner, but by a smaller amount, in proportion to the plate current. The screen waveform will therefore decrease linearly by a small amount until plate current cutoff (described previously) is reached. At plate current cutoff, the screen current increases abruptly, causing a steep trailing edge. Negative overshoots at the trailing edge of the waveform will be limited by the action of diode V2.

The resultant waveform across the cathode resistor can be visualized from the previous description of tube operation, by taking into account the changes in the total tube current. This waveform will be a negative gate with steep leading and trailing edges and with the flat portion falling off in amplitude at a linear rate. Any positive overshoot at the trailing edge will be limited by diode V2.

As in the screen-coupled phantastron, resistor R5 can be made variable to set the maximum width or delay. R1 is variable, and is connected to the plate of VI through diode V3, thereby setting the level of plate voltage at which the phantastron begins its action (when triggered). It can be seen that this will determine the amplitude and thus the duration of the plate waveform. R1 is usually an external control to vary the width or delay, and R5 can be an internal adjustment to set the maximum width or delay.

tn contrast to the **screen-coupled** phantastron, the **cathode-coupled** phantastron, has a smaller range of operation. The maximum plate amplitude swing of V1 is limited by the value of the cathode resistor, in that "bottoming" of the plate voltage occurs at a more positive potential than in the case of the **screen-coupled** phrmtastron.

# Failure Analysis.

**No Output.** Lack of plate or screen voltage because of an open bleeder resistor network (consisting of R1, R2, and R3) or open load resistors will prevent operation, as will a faulty electron tube. Loss of input trigger will also render the circuit inoperative. It is also possible for excessive bias to make the circuit inoperative because the trigger amplitude is not sufficient to overcome the bias and initiate operation. Such a condition is indicated when an input trigger can be seen on the suppressor with an oscilloscope and voltage appears on all tube elements, but either the grid or cathode voltage is higher than normal. This is most likely to occur in the screen-

coupled circuit, where a negative fix supply is employed with  $\mathbf{a}$  common bleeder to obtain bias. Since the cathode-coupled circuit develops its own bias, an excessive current drain or short-circuit condition would be needed to increase bias to the nonoperating point.

Distorted Output. Distortion is indicated by a non-linear waveform or an inaccurate time delay. Linearity of sweep development is the basic property of this circuit, with the controlling elements being the applied dc control voltage and the RC time constant in the feedback circuit. Control voltage trouble may occur when the circuit uses a separate external control from a separate power supply, as power supply fluctuations can easily change the operating level and hence the pulse duration. Failure of the platecatching diode is usually indicated by lack of control over the entire range of operation, whereas partial control is more likely to result from changing power supply voltage or a defective control. Change of time constant due to changes in circuit values or to failure or partial shorting of the capacitor will change the rate of operation and hence the time delay. It should be most noticeable for the longer delay times. False triggering due to the pickup of noise or stray pulses in the control cabling (on remote units) may affect both the starting and stopping of the gate. If the disconnecting or triggering diode is used, however, such pickup will affect only the start unless it is coupled to the suppressor through stray capacitance, and this is rather unlikely to occur. Generally it is rather difficult to pinpoint trouble in this type of circuit unless an oscilloscope is used to observe the waveforms at each electrode, because there are four basic types of trouble, namely, starting trouble, stopping trouble, linearity, and recovery-time failure.

Low or Unstable Output. Low screen-gate output indicates improper screen voltage or current, which may be caused by a defective electron tube or a change in resistance value in the screen circuit. Low cathode-gate output indicates low cathode current, which is the sum of all element currents, and therefore may be due to any one of numerous causes. Usually a voltage check will indicate the defective component. Instability in the form of jitter may be caused by power supply voltage fluctuations, noise, or false triggers picked up by unshielded wiring. An oscilloscope waveform check will reveal the cause of the instability, which can then be traced to its source.

# FAST-RECOVERY PHANTASTRON CIRCUIT

# Application%

The fast-recovery phantastron circuit is used to generate a linear sweep, or rectangular-wave output, whose duration is directly proportional to a control voltage. Because of its extreme linearity and accuracy, the phantastron output waveform is used as a delayed timing pulse, to produce timedelayed trigger pulses for synchronizing purposes, and movable marker signals for display.

# Characteristics.

Same characteristics as basic Phantastron Circuit (previous discussion), except that it requires a negative trigger or gate to **the** plate, or a positive trigger or gate to the suppressor grid to be turned on; turn-off is automatic.

# Circuit Analysis.

**General.** The fast-recovery phantastron circuit is considered to be a relaxation oscillator similar to the multivibrator in operation. Whereas the multivibrator derives its timing from an exponential waveform developed by an R-C network, the phantastron uses a basic Miller-type sweep generator to produce a linear timing waveform. (The operation of the basic Miller linear sweep generator is described in the discussion of Basic Phantastron Circuits presented earlier in this Section of this Handbook.) The phantastron is usually turned on by the application of a gating or trigger pulse, and is turned off automatically by an internally generated waveform.

The rapid return to the stable operating condition at **turn-off** is the basic property of the fast-recovery phantastron circuit. The rapid recovery is accomplished by charging the feedback capacitor through

the low cathode-to-plate conduction resistance of a cathode follower, rather than through the highresistance plate-load resistor of the phantastron. The effect of the rapid charge path is to return the plate voltage of the phantastron circuit to its stablecondition level immediately in order to prepare the circuit, in as short a time as possible, for the next input trigger pulse. Although the cathode follower decreases the usable range of the control voltage and the linearity, it is necessary in order to reduce the recovery time when long-duration delays are desired. Whether the slow-recovery or fast-recovery phanta- \_ stron circuit is used in a given application is determined by the recovery time requirements; otherwise, the circuit function in the same manner and serve the same purpose. Both a positive and a negative rectangular-wave output with well-defined leading edges may be obtained from the phantastron, depending on whether the output connection is made to the screen or cathode, respectively.

Circuit Operation. The following schematic illustrates atypical pentode cathode-coupled fast-recovery phantastron circuit. The circuit is turned on by application of a negative trigger pulse to the plate; turn-off is automatic by an internally generated gate. Pentode tube VI is the phantastron proper. This tube must have the capability of providing two control elements; that is, the suppressor grid must be capable of performing the function of another control grid. A suitable tube for use as a phantastron is the miniaturetype 5725 pentode because of the sharp cutoff characteristic of its suppressor grid. Another suitable tube is the pentode type 6AS6. A pentagrid tube such as the 6SA7 can also be used in the phantastron circuit if certain modifications are incorporated in the circuit design. (A basic pentagrid tube phantastron multivibrator circuit is discussed in Section 7 of this Handbook.)



#### **Fast-Recovery Cathode-Coupled Phantastron**

The diode-comected triode, V2, functions as a trigger injector as well as a clamping diode for controlling the plate-voltage level and determining the duration of the output gate. The maximum value of operating plate voltage is clamped to a level determined by the setting of potentiometer R1 in the cathode of V2, and, since the turn-off level is fixed, the setting of this potentiometer effectively controls the time during which the circuit produces the linear gate or sweep. Triode V3 is the cathode follower circuit through which feedback capacitor C2 is rapidly charged in order to permit the phantastron plate voltage to rapidly return to the maximum operating level determined by trigger injector and clamping diode V2. Although the illustration shows two separate triodes for V2 and V3, in practical circuit applications a single twin-triode is frequently used for economy of tubes.

Potentiometer R1 and resistors R2 and R3 form a voltage divider from the positive voltage supply (tEbb) to ground. The resistance values are such that the positive voltage developed across resistor R3 is less than the positive voltage developed across cathode-bias and load resistor R6; thus, the suppressor grid is effectively biased negative with respect to the cathode, and plate current is cut off. As mentioned previously, the setting of the wiper arm of potentiometer RI establishes the voltage level at the phantastron plate, thereby determining the gate length. Resistor R4 is a decoupling resistor in the cathode of the trigger injector and clamping diode, V2. Resistor R5 is the phantastron plate-load resistor; R7 is the screen grid load resistor, and R9 is the cathode-load and coupling resistor for the cathode follower circuit.

Resistor R8 returns the phantastron control grid to the positive voltage supply, setting the bias level that initially permits the screen grid to conduct heavily. Operation of the circuit occurs at the rate determined by the discharge of feedback capacitor C2 through resistor R8; in some circuits this grid-return resistor, which usually has a value exceeding 1 megohm, is made variable to set the maximum delay or pulse width of the output gate. The action of cathode follower V3 and capacitor C2 provides feedback from the phantastron plate to its grid, to allow rapid response to any change in the plate voltage. Capacitor Cl couples the input trigger to the cathode of trigger injector and clamping diode V2; this trigger initiates (or turns on) the phantastron action. Capacitors C3 and C4 are the output coupling capacitors for the screen grid and cathode, respectively; a positive gate is obtained from the screen grid, and a negative gate from the cathode. If desired, a linear sawtooth waveform can be obtained from the plate of the phantastron circuit.

The following simplified schematic diagram shows the charge and discharge paths for capacitor C2. The charge path (part A of the illustration) is from ground through the phantastron cathode resistor, R6, and the low cathode-to-grid conduction resistance of V1 to the left side of the capacitor, and then from the right side of the capacitor through the low cathode-to-plate conduction resistance of the cathode follower and the positive voltage supply back to ground. This is the fast-recovery charge path for capacitor C2. That is, when the plate voltage of the phantastron rises, as it

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Ebb

does at the end of the gate, it is free to do so without the interference of any lumped capacitance; tube interelectrode capacitance and stray wire capacitance are the only hindrances. The resistance in the charging path is also low at this time, since it consists mainly of the low conduction resistance of the cathode follower. The discharge path (part B of the illustration) for capacitor C2 is from its left side through grid-bias resistor R8 and the positive voltage supply to ground, and then from ground through the cathode40ad resistor, R9, of the cathode follower to the right side of the capacitor. The long R-C time constant of this path causes capacitor C2 to discharge at a linear rate during the time that screen current is low (near cutoff) and the phantastron tube is drawing heavy plate current.

The operation of the fast-recovery phantastron circuit can best be understood by referring to the preceding circuit illustrations and the following waveform illustration during the following discussion. When voltage is first applied, the plate section is in cutoff end there is heavy screen grid current. The conduction of screen current is a result of the fact that the operating voltage on this electrode is sufficiently positive to attract electrons emitted by the cathode as a result of the positive bias on the control grid (positive voltage return to B+ through resistor R8); this permits the flow of cathode current at this time. The current through cathode-bias resistor R6 produces a voltage drop across this resistor. The positive potential at the top of resistor R6 is now greater than the positive potential at the suppressor grid, which is obtained across voltage divider resistor R3. A bias voltage is therefore established between the suppressor grid and the cathode; this bias is sufficient to cut off the plate current while having no effect on the screen current.





Theoretical Waveforms for Fast-Recovery Cethode-Coupled Phantastron

Charge and discharge Paths for Capacitor C2

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Because there is no plate current, the plate voltage rises to the level determined by the setting of potentiometer R1 in the cathode of the trigger injector and clamping diode, V2. This same positive plate voltage is also impressed on the cathode follower control grid, since this grid and the phantastron plate are electrically identical. The cathode follower now conducts, and the flow of current through its cathode-load resistor, R9, develops a positive potential at the top of this resistor. This positive potential is coupled through capacitor C2 to the control grid of the phantastron, where it further increases phantastron conduction. The positive potential on the phantastron control grid also causes this grid to draw current and charge capacitor C2 through the path described previously. The foregoing action is instantaneous and causes the phantastron to assume its stable state, as depicted during time interval a on the waveform illustration. The circuit remains in this condition (heavy screen current and plate current cut off) until a negative trigger is applied to the phantastron plate through trigger injector and clamping diode V2 at instant t.

When the negative trigger  $(e_{in})$  is applied through capacitor Cl to the cathode of V2, it forward-biases the diode and permits plate current to flow. This current, in turn, causes an immediate drop in the plate voltage developed across plate-load resistor R5. The negative-going signal is also on the grid of the cathode follower, V3, where it acts as a bias to reduce the conduction through V3, thereby reducing the voltage drop across its cathode-load resistor, R9. The negative-going signal at the top of resistor R9 is coupled through capacitor C2 to the control grid of the phantastron tube, V1, where it drives this grid sufficiently negative to reduce the conduction of the phantastron. Since the phantastron cathode current is reduced, the screen current is also reduced; thus a positive-going voltage is produced at the screen grid. Through cathode-follower action of the phantastron circuit, the negative-going signal on its control grid is coupled to the cathode, where it now reduces the bias between the cathode and suppressor grid. With a decrease in this bias voltage there is an increase in plate current, resulting in a further drop in plate voltage. The action just described is cumulative and instantaneous. Thus, when the negative trigger is applied to the cathode of V2 at t, there is an immediate fall in phantastron plate voltage and a sharp rise in plate current (the fall in plate voltage is fed to

the grid through cathode follower V3 and capacitor C2 driving the control grid negative), there is a sharp rise in screen voltage and a decrease in screen current, and there is a decrease in total cathode current and a sharp decrease in cathode voltage. AU of the voltage relationships are depicted at  $t_1$  on the waveform illustration.

The fact that the phantastron plate current increases while the cathode current decreases is possible because the screen current is now decreasing. Therefore, the rise in plate current results from the fact that the plate draws current which had previously gone to the screen grid. That is, the bias between the cathode and the suppressor grid is decreasing, which is a regenerative action, causing the plate current to increase. Simultaneously, the bias between the cathode and the control grid is increasing, which is a degenerative action, causing the total tube current (and screen grid current) to decrease. The screen grid current is only reduced - not cut off completely; if it were cut off completely, plate current would also be cut off and the circuit would not function. Hence. there must be a point where the regenerative and degenerative effects are equal and the current stabilizes for an instant. This is the instant (at  $t_1$  when the sharp drop in plate voltage ceases) at which capacitor C2 begins its discharge action.

As capacitor C2 discharges during the interval b, it loses electrons from its left side, in effect making this side of the capacitor (and the control grid of the phantastron) more positive to reduce the bias between the control grid and the cathode. The reduction in control grid bias permits a heavier flow of plate current through the phantastron, which gradually raises the voltage drop across cathode-bias resistor R6 (e<sub>k</sub> waveform), as illustrated during time interval b. The rate of change of tube current is governed by the discharge rate of capacitor C2 through resistor R8. Thus, in discharging, the control grid side of capacitor C2 gradually becomes more positive, causing an increase in plate current; this produces a constant decrease in plate voltage, which is fed back to the grid through cathode follower V3 and capacitor C2. The positive voltage increment on the control grid is always slightly greater than the negative-going plate signal it produces; therefore, the grid potential gradually rises and the plate potential gradually drops, as depicted by the respective control grid(eg) and plate (ep) waveforms during time interval b.

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The action described during time interval b continues until the plate voltage becomes so low (only a few volts) that phantastron tube V1 can no longer amplify the changes in plate voltage. At this instant, t<sub>2</sub>, capacitor C2 stops discharging and the control grid is rapidly driven positive, causing the tube current to increase at a very fast rate. The rapid rise of current through cathode-bias resistor R6 produces a high positive potential on the cathode, which, in relation to the positive potential on the suppressor grid, is a bias sufficient to cut off plate current. Since the total tube current is increasing at this instant, the additional current must flow in the screen grid circuit. The action now occurring is regenerative. As the plate voltage, whose swing is limited by trigger injector and clamping diode V2, goes positive because of plate current cutoff, the positive-going signal is coupled through cathode follower V3 and capacitor C2 to the phantastron control grid; this signal causes a further increase in tube current, thereby producing a higher voltage drop across cathode resistor R6 to increase the bias on the suppressor grid and further cut off plate current. The positive-going grid of the phantastron draws current and now rapidly charges capacitor C2 through the low cathode-to plate conduction resistance of the cathode follower. Thus, at instant t,, the phantastron is rapidly returned to its original state of plate current cutoff and maximum screen grid current, as illustrated during time interval  $C_1$  until the next trigger pulse at  $t_3$  again causes a cycle of phantastron action.

As mentioned previously, when the phantastron is triggered (turned on) there is a sudden drop in screen current. This produces a positive-going voltage on the screen with a steep leading edge ( $e_{sg}$  waveform). As the tube current gradually increases, producing the linear drop in plate voltage, the screen current increases in the same manner, but by a much smaller amount. The screen waveform will thus decrease linearly by a small amount until the point of platecurrent (described previously) is reached. At the instant of plate-current cutoff, screen current increases sharply, causing a sharp drop in screen voltage, as depicted by the trailing edge of the  $\mathbf{e}_{sg}$  voltage waveform; this is the positive-gate output waveform coupled through capacitor C3 to the screen output terminals. The resultant negative-gate output,  $e_k$ , taken across phantastron cathode-load resistor R6, is coupled through capacitor C4 to the cathode output terminals. This negative-gate waveform also has steep leading are trailing edges, with the flat portion falling off in amplitude at a linear rate.

From the circuit action just described, it is evident that changing the value of the voltage applied to the plate will determine the point, and the time, at which the plate voltage "bottoms", with respect to the time of application of the input trigger. Potentiometer R1 is comected to the phantastron plate through diode V2, thereby setting the level of plate voltage at which the phantastron begins its action when triggered. Changing the value of either feedback capacitor C2 or grid resistor R8 will also affect the pulse width by controlling the rate of discharge of capacitor C2. For example, increasing the value of capacitor C2 or resistor R8 will increase their R-C time constant, thereby causing capacitor C2 to discharge more slowly and increase the width of the delay gate. A decrease in the value of either capacitor C2 or resistor R8 will have the opposite effect on the width of the delay gate. In some phantastron circuits the grid resistor, R8 in this case, is made variable so as to control the maximum width of the delay gate. When made variable the grid resistor is usually an internal adjustment, whereas potentiometer R1 is usually an external control.

If it is desired to obtain several ranges of delay with the phantastron, the most satisfactory method is to leave the value of the grid return resistor (R8) fixed and switch in different values of capacitance for the feedback capacitor (C2). A cathode follower will provide a low-impedance point for the switching and minimize the effects of stray wire capacitance, in addition to providing a fast-recovery path. A disadvantage of using the cathode follower in the phantastron is that it increases the maximum error of the circuit. Ordinarily, the phantastron linearity is ob- tained by the feedback between plate and control grid, which tends to maintain a constant discharge of the feedback capacitor (C2). Since the gain of the cathode follower is less than unity, the compensation is not as linear as when the feedback occurs through the capacitor alone. However, a slight error (approximately 0.4 percent at a control voltage of 150 volts, for example) can be tolerated when it is necessary to reduce the recovery time of the circuit for longduration output gate signals.

# Failure Analysis.

**No Output.** The input trigger should be checked with an oscilloscope to determine whether it is being

applied to the circuit and whether it is of the proper polarity and amplitude. Lack of an input trigger at the cathode of trigger injector and clamping diode V2 can be due to an open input coupling capacitor, Cl, or to failure of the external input-trigger source. It is also possible for a defective trigger injector and clamping diode tube, V2, as well as excessive bias, to make the circuit inoperative; the excessive bias will prevent the fixed-amplitude input trigger from overcoming this level and initiating the phantastron action. The foregoing conditions are indicated when an input trigger can be seen with an oscilloscope on the cathode of V2 and voltage appears on all tube elements, but either the phantastron control grid or cathode voltage is higher than normal. This is most likely to occur when a negative voltage source is used with a common bleeder network to obtain the bias (as in a screen-coupled circuit). Since this cathodecoupled pentode circuit develops its own bias, an excessive current drain or short-circuit condition would be needed to increase the bias to the nonoperating point.

Failure of the positive voltage supply,  ${}^{+E}_{bb}$ , will disrupt the operation of the circuit, as will an open cathode circuit of either the phantastron or the cathode follower. With tubes installed in the circuit, the **filament**, plate, screen, and suppressor grid voltages should be measured, as well as the bias voltage developed across phantastron cathode resistor R6, to determine whether the applied voltages are within tolerance or whether an associated electrode resistor is open. If feedback capacitor C2 is open or cathode follower V3 is inoperative, there will be no feedback signal to promote the phantastron action. An open output coupling capacitor, C3 or C4, will prevent the output-gate signal from reaching the following stage.

**Reduced Output.** A reduction in output is generally caused by a defective phantastron tube; however, a low screen gate output can also be caused by a decrease in applied voltage or a change in resistance value in the screen circuit. Low cathode gate output indicates **low** cathode current, which is the sum of all tube element currents, and thus may be caused by any one of numerous conditions (decreased tube conductance, reduced plate or screen voltage, etc). Usually, a voltage check will locate the defective circuit and component. A leaky or shorted output coupling capacitor, C3 or C4, will form a voltage divider with the input resistor of the following state. If the input resistor of this next stage is returned to ground or to a negative supply, the voltage at the screen grid or cathode will be reduced, and the operation of the state will be upset by the change in voltage applied to its grid,

Distorted or Unstable Output. Distortion is indicated by a nonlinear waveform or an inaccurate time delay. Linearity and accuracy of the output gate waveform development is the basic property of this circuit, with the controlling elements being the applied d-c control voltage and the R-C time constant in the feedback circuit. Control voltage trouble may occur when the circuit uses a separate external control from a separate power supply, since power supply fluctuations can easily change the operating level and, therefore, the gate duration. A change in time constant due to circuit values or to feedback capacitor failure or leakage will change the rate of operation and, hence, the gate length; this should be most noticeable for the longer gate lengths. False triggering due to pickup of noise or stray pulses in the control cabling (on remote units) may affect both the turn-on and turn-off of the gate. This instability, or jitter, can also be caused by power supply fluctuations. An oscilloscope waveform check at each electrode is usually the best method to checking for the cause of jitter, which can then be traced to its source.

**Incorrect Frequency.** The fast-recovery phantastron circuit has no components governing the frequency of its output gate signal; this frequency is governed by the input trigger applied to the circuit. Therefore, any change in the output gate frequency is a result of improper operation of the trigger generating circuits.

# ELECTROMECHANICAL (ACOUSTIC) DELAY LINES

## Application.

An electromechanical or sonic delay line provides a means of retarding the passage of a signal or wave for a predetermined length of time without distorting the original composition of the signal or wave. This type of delay line is used in computers and in radar equipments such as moving target indicators (MTI).

#### Characteristics.

Delay line acts as a medium between electrical and sound impulses.

Delay line is composed of quartz crystal slabs and a mercury column.

Amount of time delay depends on length of mercury column.

Time delay affected by temperature variations.

#### Circuit Analysis.

**General.** The electromechanical (acoustic) delay line utilizes the piezoelectric effect of a quartz crystrd slab to convert any electrical impulses within a circuit to sonic impulses. These sonic impulses traverse a column of mercury of specific length and are reconverted to electrical impulses by another quartz crystal slab at the opposite end of the mercury column. The overall effect is a resultant decrease in velocity relative to the velocity of electrical impulses traveling an equivalent distance. Therefore, by increasing the length of the mercury column, the longer the impulses will remain in the sonic state, and the greater will be the delay of the impulses.

**Circuit Operation.** A pictorial representation of an acoustic delay line is shown in the following illustration. The delay line consists of two quartz crystal slabs and a column of mercury in a cylindrical container between the two crystal slabs. As electrical impulses are applied to the first crystal slab of the delay line, the piezoelectric effect associated with crystalline substances causes these impulses to be converted into corresponding mechanical expansions and contractions. One of the expanding and contracting surfaces of the crystal contacts the mercury column in such a way that these mechanical or sonic vibrations are conducted through the column in the same way that electrons are conducted through a wire. Sonic impulses travel at a considerably lower speed

than electrical impulses and by increasing the length of the mercury column the time is required for the impulses to travel from one end of the mercury column to the other becomes greater. The amount of time delay is proportional to the ratio of the velocity of sound in mercury to the velocity of electrical impulses through the conducting material used in the circuit, multiplied times the length of the mercury column.





Upon reaching the end of the mercury column, the sonic vibrations are converted to electrical vibrations by again applying the sonic vibrations to a crystal slab. This crystal, as the first crystal, contacts the mercury column along a plane of the crystal in which sonic or mechanical impulses can be applied or obtained (which happens to be perpendicular to the plane along which sonic impulses are applied or obtained. (See the following illustration.)



#### CROSS SECTIONAL VIEW OF CRYSTAL

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**Crystal Axis** 

#### Failure Analysis.

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**Since the** sonic delay line is a single component the failure analysis can be simplified. If no signal is obtained at the output of the delay line and the proper signal is applied at the input, the mercury might have leaked from the cylinder which is supposed to contain it. Another cause of a no-output condition may be an open crystal or a crystal shorted to the metallic case containing it. It will not be necessary to determine which part of the delay line is at fault, since any defect will make it necessary for the entire delay line to be replaced.

A distorted output may be due to the effect of temperature changes within the area where the delay line is used. If extreme temperatures occur, there is a possibility that the crystals may be damaged. In order to prevent or correct this condition constant temperature monitoring should be provided.

#### **ELECTROMAGNETIC DELAY LINES**

#### Application.

Artificial delay lines of the electromagnetic type are used to generate rectangular pulses of fixed duration (in radar receiver and transmitter applications); to produce a rectangular waveform from a step function of voltage (as used in starting and delay triggers for test equipment and video display units); to terminate a pulse produced by a regenerative device such as a blocking oscillator or multivibrator (as used in radar, timing circuits, and computers); and to duplicate on existing pulse at a later time (a simple case of time delay). These lines are commonly used for many types of waveshaping and pulse-forming applications.

#### Characteristics.

Provides a constant attenuation of signal, depending upon material and construction.

Consists of a number of equal sections (or halfsections) of lumped capacitance and inductance, providing a definite delay interval.

Provides a definite phase shift which can be repeated at specific intervals.

Possesses an inherent characteristic (surge) impedance which must be matched to input and output circuits for proper operation.

Similar in operation to a real transmission line, but greatly reduced in physical size.

## Circuit Analysis.

**General.** Delay lines are simple to construct, reliable, permanent in their characteristics, and accurately reproducible in manufacture. The delay line operates by virtue of the finite velocity with which the signal travels along the delay line. For open-wire lines there is practically no difference in the velocity of propagation of the signal as compared with the velocity of propagation in free space, so that multiples of a physical quarter-wavelength of line must be used to produce the delay. This results in long and bulky lines. Even with the standard type of line, the delay is on the order of 0.003 microsecond per foot. A special coaxial delay line is produced with a **spiral**-wound center conductor (distributed-constant line)

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to provide better results; however, measured results at 5 MHz are only on the order of 0.042 microsecond per foot. Therefore, artificial lines consisting of lumped values of inductance and capacitance (which occupy a small space) are connected together in lowpass falter arrangements to provide the desired characteristics. Since a real transmission line has uniformly distributed inductance and capacitance, artificial lines can, in a small space, provide the electrical equivalent of a long line. The basic equivalent circuit of the distributed-constant artificial delay line is shown in the following illustration.



Distributed-constant Delay Line Equivalent

The functioning of this type of line is similar to that of the lumped-constant artificial delay line in all respects. It is used mainly for small delays of 1 microsecond or less where the total length of the line is conveniently held to a range of from 6 to 30 inches, depending upon the construction. Units have been manufactured with characteristic impedances of from 200 to 4000 ohms. The characteristic impedance (Z) is determined by the total distributed constants per inch, centimeter, or foot, by means of the standard formula  $Z = \sqrt{L/C}$ ; the values are in ohms, henries, and microfarads. Time delay is given by the formula  $T = \sqrt{LC}$ ; the values are in seconds, henries, and microfarads. For a given impedance and time delay, the inductance is determined by L = TZ, and the capacitance by C = T/Z. In actual practice, the manufacturer lists these values and the microseconds per unit length. Thus for a given delay only a specified length is required, avoiding any complicated calculations. Since the distributed+ onstant type of line is not as commonly used as the lumped+ onstant type of line, but functions similarly, for practical purposes the discussion of the lumped+ onstant type of line which follows applies to both types (neglecting end effects, temperature, and frequency response).

The schematic equivalent of a simple lumpedconstant **type** of artificial transmission line is shown in the following illustration. Basically, this circuit is that of a constant k low-pass falter with half T section terminations, utilizing one full T section of delay (plus the hrdves for a total delay of two sections). Actually, the number of sections varies with the design (usually from five to eight sections are sufficient).



Lumped-Constant Equivalent Circuit

The manner in which the artificial delay line is employed in a circuit determines how it functions. Generally speaking, there are three forms of operation to be considered. One form is that of a simple delay line which delays the input pulse or signal by a period of time equal to the time it takes to traverse the line; in this case the termination of the signal initiates circuit action after a predetermined delay time. In the second form, the reflected input pulse or signal is permitted to traverse the line, be reflected, and return to the origin; circuit action is initiated after 2n delay periods. In the third form, the line is charged to a specific storage level and is then discharged to form a precise pulse with a duration equal to the discharge-delay period. In each of these forms of operation, performance is generally based upon the theory of charge and discharge of an ideal lossless transmission line.

**Circuit Operation.** Consider now the case of the simple delay line. In this instance, the line is terminated in its characteristic impedance (the input need not be terminated unless power transfer is required, since there is no reflection). Assume the simple balanced T section equivalent circuit in the following figure. As far as the input circuit is concerned, the artificial transmission line appears as though it were a resistor equivalent to the characteristic (surge)

impedance of the line ( $R_o$ ). Assume that a rectangular l-microsecond pulse is applied, and that a delay of 2 microseconds is desired. (The delay line is usually placed in series with the grid of a trigger circuit. Let us also assume that a negative trigger is required to initiate action.)



**Properly Terminated Line Action** 

At the beginning of the cycle (time  $T_1$ ), the positive pulse is applied to the line input at terminals 1-2). Immediately, the voltage across the line input rises to the pulse value (input is unterminated). At the load end of the line, however, no voltage as yet appears. Since the line constants are chosen for a 1-microsecond delay, it takes this length of time for the initird pulse to travel to the end of the line (because of the low propagation of the line). During this interval, capacitor C is being charged through left-hand inductor L/2. At time T<sub>2</sub> (1 microsecond later), capacitor C is charged and pulse voltage now appears at output terminals 34, across  $R_{L}$ . Note that this is still the leading edge of the initial pulse. At time T<sub>2</sub> the initial pulse terminates and the input voltage across terminals 1-2 drops to zero. Capacitor C now discharges through right-hand inductor L/2 until time  $T_3$ . When time  $T_3$  is reached, the capacitor is completely discharged and the voltage across  $R_{L}$ drops to zero. Thus, 2 microseconds after the start of the initial pulse, the negative trailing edge of the pulse appears at the grid of the trigger tube, and the trigger is initiated (by the trailing edge of the pulse) with a 2-microsecond delay. During the delay period, simple R-L-C charge and discharge action was postulated, as supported by simple transient theory.

In practice, a number of sections of L and C are required to provide pulse transfer and delay without distortion. All delay lines have resistance which dis-

torts the pulse by causing a reduction of current as the line is charged, with a consequent slope in the top of the pulse. The inductance opposes the change in current and affects the circuit at the very beginning when the charging current quickly assumes a high value, and then acts to maintain the current flow after the maximum current value is reached and tends to decrease, With a large inductance the rise and fall of current is more gradual; with a smaller inductance the current rises and falls more rapidly. The addition of the capacitance to the circuit causes the current to reach a definite maximum value. The smaller the capacitance, the smaller the maximum value of current and the shorter the period of time required to reach maximum current. When both inductance and capacitance are combined, and the inductance is very small and the capacitance very large, the circuit action is controlled mainly by the resistance in the circuit. Under these conditions the charging current rises very quickly and remains constant for a relatively long period of time (because a relatively long time is necessary to charge the capacitor). Thus the response curve closely resembles the input step voltage. Ideally, as L approaches zero and C approaches infinity, so that only resistance is left in the circuit, the output waveform approaches the input waveform. This is theoretically true because a purely resistive circuit has no transient response and, therefore, does not change the shape of the input voltage waveform. With only resistance in the circuit, however, there would be no delay. Consequently, a practical compromise is reached by employing a number of L-C sections having a small inductance and a relatively large capacitance.

A detailed analysis of the operation of a typical distributed+ onstant type of delay line (chosen for ease of explanation) using actual values follows. As constructed, the line consists of very fine wire (No. 40 AWG, 0.0031 inch in diameter), wound on a plastic core. This continuously wound coil has a diameter of approximately 3/16 inch, and contains 109 turns per centimeter of length to provide a rated inductance of 20 microhenries per centimeter. An insulating sleeve is placed over the coil, and an external copper braid is used to provide a shielded outer conductor, which forms a capacitance of 16.5 picofarads per centimeter with the coil. The measured time delay is 0.018 microsecond per centimeter. To produce the 1-microsecond time delay mentioned in the previous discussion, a 55-centimeter length of this

line is required. Therefore, we can consider the line to be made up of 55 sections (1 cm long), forming an equivalent ladder-type line as illustrated in the accompanying figure.



Ladder-type Delay Line Equivalent

Although in the previous discussion on ideal pulse was assumed, with zero rise time, a practical square input pulse has a finite rise time. A value of 0.03 microsecond for a 1-microsecond pulse is representative of actual rise and fall time tolerances encountered in practice. When this pulse is applied to the input of the line at time  $T_1$ , terminals 1 and 2, coil L1 provides a counter emf which slows down or opposes the passage of current flow through it. The current through L1 is the charging current for capacitor Cl and the remainder of the line sections. Capacitor Cl charges in accordance with the time constant LIC1 (0.018 microsecond). Since the rise time of the pulse is 0.03 microsecond, capacitor Cl charges quickly. During this period the voltage across L1 decreases while the voltage across Cl increases. In effect, the input voltage is applied to L2 after being delayed 0.018 microsecond. Since it takes 10 time constants to reach approximately full charge, the amplitude is less than that of the original pulse, and approximates a final value of about 0.6 that of the original value (at the end of the line). These line sections are effectively comected in series with the line, and the pulse travels progressively down the line from L1 through L55. Capacitor C55 is charged to the same value as L1 was after one time constant, and at a time  $(T_{a})$  exactly 1 microsecond later. In other words, the leading edge of the pulse reaches the end of the line at that instant.

Since the duration of the pulse is 1 microsecond, the entire line is still charging. In the next instant, however, the input pulse terminates, and the negative-going trailing edge is applied to L1. At this time,

Cl is fully charged and begins to discharge. The discharge path is the reverse of the charge path. The discharge action is similar to the charge action; that is, at the end of one time constant Cl is discharged substantially, and the effect is as if a negative voltage were applied between L2 and ground. The discharge pulse travels progressively down the line. During this time  $(T_{2} to T_{3})$  the amplitude of the output pulse remains constant, since the flat top of the input pulse is being reproduced by the constant charge voltage to which C55 is held. This action is the result of the small (fast) time constant per section (full charge is reached in approximately 0.09 microsecond). A slight rounding off of the leading edge is produced in practice (by exponential charging action); however, in the ideal case discussed previously, no such action was assumed. Practically, this rounding off effect is negligible, and the shape of the input pulse is retained as long as the pulse rise time is longer than the time constant per section. (When the rise time is less than the time constant per section, a noticeable rounding off or distortion of the pulse shape occurs.)

• Once the discharge action is started by the trailing edge of the input waveform (time  $T_2$ ), it continues until C55 is reached. The discharge of C55 through terminating resistor  $\mathbf{R}_{\mathbf{L}}$  (at time  $T_3$ ), comected across terminals 3 and 4, represents the trailing edge delayed 1 microsecond. Since the leading edge was also delayed 1 microsecond, the total delay from the leading edge to the trailing edge (or trigger) for the time period  $T_1$  to  $T_3$  is exactly 2 microseconds (within practical limits). A fewer number of sections or a change in the values of the inductance and capacitance used will change the delay time. In the case of the lumped-constant delay line, the action is identical. Instead of special construction, however, the delay line merely consists of a number of small inductors and capacitors connected in the ladder-type arrangement illustrated previously.

Open-Circuited Line. Consider now the case of the artificial delay line which is *not* terminated in its characteristic impedance. Let us assume that the line is open-circuited and is represented by the simple circuit shown in the following figure. The delay line is connected in series with load resistor R<sub>1</sub> and switch S1 to ad+ source of voltage  $E_0$ . Assume that the line at time T. is completely discharged, with S1 open. At time  $T_1$ , switch S1 is closed, and voltage  $E_0$  is applied across load resistor R<sub>1</sub> and R. in series (R. is the surge or characteristic impedance of the delay line).

Assuming that  $\mathbf{R}_{\mathbf{I}}$  and  $\mathbf{R}$ . are equal, the applied voltage divides equally, and half the applied voltage appears at terminals 1-2 (line input). The line is designed to have a velocity of propagation much less that of an open-wire line; thus, at time  $T_2$  the voltage has just reached terminals 3-4. Since the line is opencircuited, the applied voltage is reflected back in phase (with the same polarity) toward the line input. Since current will not flow through the open circuit, the current polarity is reversed, and the reflected wave cancels the current of the incident wave to give a total zero current. Thus, the voltage at terminals 34 is effectively doubled, and a reflected voltage equal to E. travels back to the source. When the source is reached at time T<sub>3</sub>, the input voltage and reflected voltage are equal, current flow ceases, and the pulse is terminated. At this time the line is charged to the applied voltage. While the output end of the line is not terminated, the input is usually matched with a resistor  $(\mathbf{R}_{\mathbf{I}})$  equal to R. so that the reflected pulse is absorbed on its return. During the interval between pulses or signals (when S1 is open), the line discharges; thus it is ready to start another cycle of operation when S1 is again closed.



**Open Circuited Delay Line Equivalent** 

The current and voltage relationships for the openunded line are shown in the following figure.



Current and Voltage Relationships of Open-Circuited Line

It can be seen that  $E_1$  is the applied voltage or step function, which at the closing of S1 jumps to its maximum value. Simultaneously, charging current 1, does likewise. Since the flow of 1, through R. produces the voltage E<sub>in</sub> applied to the line, and since equal resistors R<sub>1</sub> and R. form a voltage divider across the input, the voltage  $E_{in}$  is reduced to half of  $E_{i}$ , remains at this value during the time of two delay periods, and then returns to the source value when the line is fully charged and no further charging current flows. At the output of the line the step function E. rises to one-half maximum value after one delay period, and then to full value at the end of the remaining delay period. With the line fully charged at the end of two delay periods, it remains at the original applied value of E<sub>i</sub>until S1 is opened; the line

then discharges. In practice, this is usually accomplished through the grid resistor of the stage which it triggers (the delay line is connected in parallel across the grid resistor in place of the conventional grid capacitor). Thus we can say that an open-ended delay line operates on a step function of voltage to produce a pulse of current equal in duration to twice the length of the line. The pulse across the characteristic impedance in series with the line has one-half the amplitude of the step function.

Short-Circuited Line. Consider now the case of an artificial delay line which is terminated by a short circuit at terminals 3-4, as shown in the following figure. The illustration is identical to the illustration of the open-circuited line shown previously, except that the output is short-circuited. At time T, when S1 is closed, the applied voltage divides equally between  $R_{L}$  and  $R_{o}$ . At time  $T_{2}$  the voltage reaches terminals 34 and is inverted in polarity by the short circuit and sent back toward the source. Simultaneously, the current is reflected back in phase with the source wave. Therefore, the current doubles while the voltages of the reflected and incident wave cancel to produce zero voltage. The current wave then travels back to the source in coincidence with the oppositely polarized reflected voltage. When the source is reached at time T<sub>3</sub>, the input voltage across R. is completely canceled and is therefore zero, while the current is double the starting value. In effect, the input to the line at this time is short-circuited also, and the line is completely discharged, ready for another cycle of operation.



Short-Circuited Delay Line Equivalent

The current and voltage relationships for the shortcircuited line are shown in the following figure. In this case, I<sub>i</sub> is the step function, which at the closing of S1 jumps to its maximum value. Simultaneously, the applied voltage,  $E_i$ , does likewise. Because of volt-

age-divider action,  $E_0$  (the voltage across  $R_0$ ) is half the source vrdue, or E/2. It remains at this value for the time of two delay periods, and returns to zero when the out-of-phase reflected pulse reaches the input and produces cancellation. Voltage E<sub>1</sub> across R<sub>1</sub> is produced at half amplitude since it is equal to the input voltage across  $R_0$ ; it remains at this value for two delay periods and then rises to the source value at the termination of the pulse. The voltage  $e_{ref}$ is the reflected voltage, which does not exist until time  $T_{2}$ ; it is negative and equal in amplitude to  $E_{0}$ . Once started by the reflection, it continues to flow back to the source until time T<sub>3</sub>, when it reaches the start  $(T_1)$  and terminates output pulse  $E_0$ . Output pulse  $E_{\circ}$  originates at time T1 at half the amplitude of source voltage E continues for the time of two delay periods, and is then terminated,



#### Current and Voltage Relationships of Shorted Line

In the case of the shorted line, then, we can say that it operates on a step function of current to produce a pulse of *voltage* equal in duration to twice the length of the line. The voltage produced has half the amplitude of the step of current multiplied by the characteristic impedance. Thus, there is complete duality between open lines charged from a constantvoltage **cource**, and short-circuited lines charged from a constant-current source. The choice of the method depends upon the characteristics of the switch used to produce the step function. A thyratron switch has an impedance of less than 10 ohms and, therefore, effectively constitutes a constant voltage source. A pentode switch, on the other hand, may have an

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appreciable currents. While the discussion above has assumed ideal step function operation, in actual practice there is an effect produced by the steepness of the grid pulse and stray capacitance, which determine the slope of the leading edge of the pulse. Line attenuation also produces phase distortion; the characteristic impedance of the line and the line resistance produce a slope on the trailing edge of the pulse, and determine the total amplitude of the pulse. Accidentird resonances in the line can cause oscillation following both edges of the pulse. Unterminated open or shorted lines will tend to produce another reflection at the input end, and cause a following pulse of lower amplitude until attenuated by the losses in the line (this is effectively an oscillatory condition). The following figure shows some typical waveforms taken with different line terminations, and is indicative of typical responses of artificial delay lines. The pulse length is 1-microsecond, and the delay time is also 1 microsecond. Part A of the figure shows both input  $(e_{in})$  and output  $(e_{in})$  waveforms with the delay line properly terminated both at the input and the output. Part B shows the input waveform with the input properly terminated and the output short-circuited. Note that between times  $T_1$  and  $T_2$  the output pulse is effectively cancelled by the negative inverted pulse, whose leading edge appears at  $T_{2}$  and lasts until  $T_{2}$ . Since the amplitude of the inverted pulse is not exactly equal to that of the input pulse, slight pips appear at  $T_4$  and  $T_5$ , even though the input is properly terminated. Part C shows a partially shorted line, that is, with the load only one-half the value of the line characteristic impedance, and with the input properly terminated. In this case, since the mismatch is approximately 50% there is a reflection of approximately 1/4th the amplitude, with the remainder being absorbed. Note that because the resistance or **impednace** is lower than that of the line, the signal is inverted as with the short-circuited line. Part D shows a more nearly matched condition, at about 20% mismatch. While the reflection is still inverted, because the impedance of the load is lower than that of the line, its amplitude is very small. Part E shows the input waveform with the input and output both properly terminated. In this case the output is absorbed by the proper termination, and no reflection occurs; hence, the input pulse stands alone. Part F shows the condition for a 505% mismatch, with the load impedance twice the line impedance. In this case the

impedance of a megohm when closed, and yet switch

reflected pulse is of the same polarity as the input, acting as an open line, since the load impedance is higher than the surge impedance of the line. The amplitude is not half of the input, but approximately one-quarter, exactly as in the opposite case of 50% mismatch shown in part C. Part G shows the waveform at the input with the output open-circuited and with the input properly terminated. In this case the open line creates a complete reflection, which is not quite equal in amplitude to the input signal because of line attentuation; therefore, there is a slight reflection, causing the minor pips at  $T_{4}$  and  $T_{5}$ , even though the input is properly terminated. The final case is with the output short-circuited and the input terminated in a lower impedance than that of the line. Part H shows the input waveform for this case. Since the line is shorted, the reflected pulse is inverted, and since it is improperly terminated at the input, reflection occurs, with each succeeding waveform being further reduced in amplitude. This is equivalent t o an oscillatory condition or an undamped transient response.



Typical Delay Waveforms for Various Terminations

Pulse-Forming Line. In the two preceding cases of open and shorted delay lines, the action was considered with the line discharged and a pulse applied. In the third and final case involving the use of a delay line, the line is first charged to a specific level, is then disconnected and discharged, and finally a pulse with steep leading and trailing edges and with a time duration equal to the delay time. The following figure shows a simple schematic equivalent of such a pulse-forming circuit. As shown, the line is connected through R1, S1, and  $\mathbf{R}_{\mathbf{L}}$  to the **d-c** source voltage, E... Switch S2 is linked mechanically with S1 so that when S1 is closed S2 is open, and vice versa. The line is not terminated, but rather is open-circuited. At time T. switch S1 is closed and the line is permitted to charge until it reaches a steady-state condition with the line charged to voltage E<sub>o</sub>. (This charge consists mostly of electrostatic energy stored in the capacitors.) At time T<sub>1</sub>, switch S2 is closed, opening S1, and the line discharges through R<sub>1</sub>. The discharge current through R<sub>1</sub> produces voltage EL, which is the desired output voltage. The flow of current through  $\mathbf{R}_{t}$  produces a voltage wave which travels from terminals 1-2 of the delay line toward open end 34. Since the load resistor is placed in series with the line and the line is now acting as the source of voltage, this voltage divides between the characteristic impedance of the line and R<sub>L</sub>, which is of the same resistance. Therefore, the initial discharge voltage is half of the value to which the line is charged. Because the flow of current is now reversed, the polarity of the voltage wave is opposite that to which the line was initially charged. As this induced wave travels down the line, it cancels out the original charge by one-half the maximum charge voltage. Thus, the discharge current which flows through  $R_1$  is equal to  $E_0/2R_0$ . When the wave reaches terminals 3-4, reflection occurs. The reflected wave is now of the same polarity as the induced voltage wave and, since current cannot flow in an open circuit, the voltage doubles, becoming equal to E<sub>o</sub>. The polarity of the discharge (induced) wave is opposite the original polarity of E.; thus both voltages are equal and cancel. Since the current cannot flow further, it is inverted in polarity and travels

back to the source, wiping out the current wave as it travels. When the reflected wave reaches the input terminals, all the electrostatic energy stored in the line is completely discharged, and neither current nor voltage exists anywhere along the line. Switch S2 is then opened and S1 is closed, starting a new cycle of operation. In this instance the discharge of the line has resulted in a rectangular pulse with a duration equal to twice the delay time.





Current and voltage relationships for the charge and discharge of the delay line are shown in the following figure. At time To, when S1 is closed and S2 is open, the source voltage is applied to the line through charging resistor  $\mathbf{R}_1$  in series with R. and  $R_{L}$ . In the absence of  $R_{I}$  the line would have half the source voltage applied. However, R<sub>1</sub> is a large-value resistor (where the 1<sup>2</sup>R loss in this resistance is undesirable a choke is used instead), and only a small voltage is applied to the line. The initial voltage is reflected again and again (as shown in part A) until the line is finally charged up to the source voltage (assuming that the period of time between T. and  $T_1$  is suf-ficient). At time T<sub>1</sub>, when switch S1 is open and S2 is closed, the discharge commences and the charge voltage immediately drops to half the maximum value. The line voltage remains at this value until time  $T_{2}$  is reached, when the discharge ceases. Thus, from part B of the figure it can be seen that between  $T_1$  and  $T_2$ the line discharges at a constant current with a voltage equal to one-half the initial charge voltage.


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# Current and Voltage Relationships for Discharge Line

The ladder-type LC networks used for the delay lines discussed previously are sometimes replaced by a more sophisticated type of line which uses a twotermirud series arrangement instead of the fourterminal parallel arrangement, as shown in the following simplified schematic. In this arrangement the two sections have different values of L and C. This type of construction is similar to the m-derived falter. The theory of operation is identical to that of the ladder-type of delay line; the different construction merely provides equivalent or better puke response characteristics with fewer sections.



#### **Two-Terminal Delay Network**

An artificial delay line used with a typical pulse generator to produce an output pulse equal to the delay time is shown in the following schematic. In this application a step function of voltage is applied at the same time the input pulse (step function) is applied to another tube element. The inverted and delayed pulse stops circuit action at the end of the delay period. Transformer T1 has two secondary windings, T2 and T3. Winding T3 is comected to the bias source and the control grid of the tube. When a positive input pulse is applied to the primary, the induced pulse in the secondary of T3 causes the tube to conduct. Secondary T2 is connected across the delay line, forming a shorted line, with the opposite end properly terminated by RI and connected to the suppressor grid. In the absence of a pulse and for the initial delay period, the suppressor is essentially at ground potential, being connected through the winding to ground. When the initird pulse is applied to primary T2, a positive pulse travels along the line, is inverted, and appears as a negative shut-off gate at the suppressor grid. Conduction occurs only during the time delay period. By tube action the plate current pulse produces an inversion of the positive input pulse, and provides a negative output pulse across  $R_1$ , which appears at C<sub>c</sub>; this pulse is equal to the delay period. Because of the numerous variations in circuitry, no attempt will be made to cover any other practical circuits. The operation of the various circuits is essentially the same, with the output of the delay line controlling the circuit action.

to a delay line (which is connected to a tube element)



Typical Pulse Generator

#### Failure Analysis.

Since the artificial delay line consists of inductors and capacitors, a simple resistance or continuity

check will determine whether the line is open or short-circuited. Basically, the line either works or it does not work. If it does not, the end result is that the controlled circuit produces a pulse of the wrong width and shape. Therefore, it is necessary to observe the circuit waveforms with an oscilloscope. Usually, the delay line is applied to the grid circuit of a tube, in which event the plate waveform, being an inverted and amplified replica, may be observed to avoid shunting the line with the oscilloscope input. If the rise time is slow, it may be because the input pulse shape has too much slope. If not, the line inductance is probably excessive. When the top of the pulse slopes excessively, the resistance in the line is excessive. Normally, a slight slope is expected since the line resistance can never be zero. Usually, the line resist. ance will also place a slight tail on the pulse in shortcircuited lines. Adding additional sections will tend to sharpen the rise and fall time, but will also make the

delay time longer. Therefore, in such case, the total inductance per section wiU necessarily have to be reduced. In practice, a defective delay line is usually replaced with a new one. Otherwise it will be necessary to accurately measure the individual components in inductance and capacitance bridges to determine whether they are defective. While insertion or removal of a component or section may temporarily restore the line to proper operating condition, this will be no assurance that other components have not been damaged by the cause of the previous failure, and will themselves soon fail and cause a similar condition. Failure of the associated tube and circuit is more common than delay line failure. Check the values of the resistors in the circuit. Failure of the terminating resistor is usually indicated by the presence of additionrd reflections or by an oscillatory condition.

## **SECTION 14**

#### SYNCHROS AND SERVOS

## PART 14-1. SERVOMECHANISMS

## SERVOMECHANISM CIRCUITS

#### General

In radar systems, as well as in industrial and other widespread applications, it is often necessary to control the angular position of one shaft by the positioning of another shaft. When the two shafts are close together this control may be accomplished directly, by gears, or by some other mechanical means. However, when the controlled shaft is located some **distance** from the controlling shaft it is usually impractical to interconnect the two shafts mechanically and, as a consequence, some other method must be employed to move the controlled shaft in correspondence with the controlling shaft. Two systems used to transmit mechanical shaft angles to a remote location by means of electrical voltages are the synchro system, and the servomechanism. The synchro system accomplishes mechanical shaft transmission without power amplification. That is, mechanical power output is equal to mechanical power input, neglecting losses. In applications where the torque of the controlling shaft must be amplified before it is applied to the controlled shaft, the system used is known as a servomechanism. The synchro system employs two or more self synchronizing units, similar in appearance to small electric motors. Synchros are used extensively in remote indicator systems, where information is to be transmitted between two points. Such information includes antenna position data in azimuth, or in elevation, meter readings, and many types of computer data. Since the controlled shaft is usually fastened to a dial or pointer, the synchro system adequately supplies the small amount of torque required to move the shaft. In addition to remote indicator applications synchro devices are widely used as basic elements of servomechanisms. Synchro systems are discussed in detail in the following paragraph of this Handbook.

The servomechanism is essentially a high gain power amplifier operating on the closed loop, or error-sensitive principle. That is, the action of the power amplifier is governed by an error, which exists when there is an angular displacement between the controlling (or input) shaft, and the controlled (or output) shaft. Servomechanisms may be classified according to motive characteristics. Three types of motor drives are used extensively in positioning systems: the dc motor, the ac motor, and the hydraulic motor.

The dc servo motor is a high torque device widely used in servomechanisms where smooth control of heavy loads is desired. The dc servo motor is a specialized form of dc motor in that it is designed to provide nearly linear changes in speed with proportional changes in armature current. This feature permits the dc servo motor to change direction and speed of rotation smoothly, and with minimum mechanical stress on the controlled mechanism. A servomechanism utilizing a dc servo motor drive frequently uses a synchro system to produce an error voltage, which is indicative of the angular error between the input and output shaft. This error voltage is applied to a phase sensitive dc servo-amplifier, also called a dc servo motor-controller, which compares this error voltage to an ac reference voltage, and produces an output which drives the dc servo motor. The polarity of the servo-amplifier output is dependent upon the direction, either clockwise or counter-clockwise, of the angular displacement between the input and output shaft, and hence, the servo drive motor rotates the controlled devices in the desired direction. As the output shaft is rotated by the servo motor toward a position of alignment with the input shaft, the error voltage produced by the synchro control transformer (the synchro output device, which is mechanically coupled to the output shaft) decreases, since the amplitude of the error voltage is proportional to the amount of error between the input and output shafts.

The output of the dc servo motor-controller decreases and, therefore, the servo motor rotates slower. When the output shaft reaches a position of alignment with the input shaft, an error voltage is no longer produced, and the servo motor comes to rest. In systems where heavier loads must be positioned, thyratron servo motor-controllers are sometimes used because of their higher efficiency and power handling capabilities, which are necessary to drive the larger servo motors used with the heavier loads. In applications where very large loads are positioned, the

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servo motor-controller does not directly drive the servo motor. Instead, it excites an electromechanical power amplifier, such as a dc generator, several cascaded dc generators, a Ward-Leonard system, or an Amplidyne, which is used to drive the dc servo motor. The Ward-Leonard system may be used, either with or without the electronic servo motor-controller. Electromechanical power amplifiers provide substantial gain, and in the AmpIidyne system, which provides the highest gain of them all, a power gain of 10,000 may be realized. An important refinement that is frequently found in servomechanisms is an anti-hunt circuit. Anti-hunt provisions are necessary because of the tendency of the load to coast past its ordered position due to inertia. When the load comes to rest, there ia an angular displacement between the input and output shaft in the direction opposite to the original error, and an error voltage is produced which causes the output shaft to be rotated back toward the ordered position. Again, due to inertia, the load coasts past its ordered position and again an error voltage is produced, which again causes the servo motor to rotate the load toward its ordered position. The load is now oscillating about the ordered position. Friction losses in the servomechanism would dampen out this oscillation, or hunting, as this condition is commonly referred to, if it were not for another factor. This factor is the existence of a time delay in the positioning system which tends to cause the applied torque to be proportional to a past error, rather than a present error. The torque applied to the load by the servo motor lags the error voltage by some angle, and is thereby applied in the wrong direction for a short period of time after the load coasts past the zero-error, or ordered position. Thus, the time delay in the controller creates a regenerative action, reinforcing the oscillations each time the ordered position is passed in much the same way that regenerative feedback in an oscillator sustains oscillations. Overshoot and hunting may be eliminated by increasing the friction of the mechanical drive, by decreasing the gain of the power amplifier, or by compensating electronically for the time delay of the servo motor-controller. The first two methods mentioned are usually unsatisfactory, since increasing the friction of the drive train decreases system efficiency, and decreasing power amplifier gain leads to sluggish response. Anti-hunt circuits, therefore, suppress oscillations by compensating for the effects of the time delay of the servo motor-controller. Anti-hunt devices

for servomechanisms are many and varied. In small servos a simple inertia damper may suffice, whereas in larger applications various electronic anti-hunt circuits are used. In general, an anti-hunt circuit provides regenerative feedback when the error voltage is increasing, and degenerative feedback when the error voltage is decreasing.

Servomechanisms using ac servo motors are used where a rapid, accurate, and low cost servomechanism is required. The ac motor is, however, essentially a constant speed device and this characteristic makes it less desirable than the variable speed dc motor in some applications. A few advantages of the ac servo motor servomechanism are: no commutator or brush maintenance, and the ac servo motor-controllers, used with ac servomechanisms, are not subject to drift (development of an output signal with no signal input), which is sometimes encountered in dc servo motor-controllers. An ac servo motor servomechanism may be quite similar to the dc system. The only variations would be the type of servo motorcontroller, and the servo motor itself. This system, like the dc servo motor system and all other servomechanisms, operates on the error-sensitive principle.

The servomechanism is one type of servo system. A servo system may or may not involve mechanical motion. Automatic frequency control and automatic gain control circuits are examples of non mechanical servo systems. In all cases, however, the output of the system is fed back for comparison with the input, and the error, or difference voltage is used for control of the system. By strict definition, a servomechanism is a servo system which includes mechanical motion. However, the terms servomechanism, servo system, and servo, are often used interchangeably.

The hydraulic servomechanism is a rugged power amplifying device operating on the hydromechanical principle. This system may be used to position very large loads, and has the advantage of relatively small physical size. Hydraulic servomechanism systems are beyond the scope of this Handbook, however, they deserve mention since they are frequently controlled by relatively small electrical servomechanisms.

## SYNCHRO CONTROL SYSTEMS

#### Application.

Synchro control systems are used in radar sets, computers, and in any other system where it is necessary to indicate the angular position of a shaft, or to

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transmit mechanical shaft angles to some remote location.

Characteristics.

Electrically transmits mechanical shaft data (angular position) from one point to another.

Does not provide power amplification, i.e., mechanical power output is equal to mechanical power input.

#### Circuit Analysis.

General. Synchros are known by a wide variety of trade names such as Selsyn, Autosyn, Telesyn, Teletorque and others which are not too frequently encountered. The preferred name however, is synchro, which applies to all the various types. Synchros are devices which convert mechanical shaft angular rotation to electrical signals and vice versa. When information is in the form of a shaft position so that it is expressed in terms of the angle between the actual shaft position and some zero or reference position, it can be converted by a synchro to a set of three voltages called synchro data. In this form such information can easily be transmitted to another point where a second synchro is used to set a second (repeater) shaft to a corresponding angular position. In some instances this second synchro, directly or indirectly through gears, mechanically positions the repeater shaft. In other instances where power amplification is required, the second synchro provides only a voltage output, which drives a servo system. It is important to note that there is no power gain in a pure synchro system. Neglecting friction losses the mechanical power output of the repeater (or receiver) synchro is equid to the mechanical power input to the transmitter. There are five general types of synchro units, each classified according to function. These include transmitters, receivers, differential transmitters, differentird receivers, and control transformers.

The synchro transmitter, which is sometimes called a synchro generator consists of a rotor which carries a single winding, and a stator made up of three separate windings displaced 120°. The rotor is excited by an ac source and it is usually coupled directly or through gears to a controlling shaft. The rotor is usually so restrained that it cannot turn except under the influence of the controlling shaft. The voltages induced in the stator windings as a result of the alternating field created by the rotor winding, are representative of the angular position of the rotor at any instant.

The synchro receiver, sometimes referred to as synchro motors are similar electrically to the synchro transmitter. The rotor of the synchro receiver is, in contrast to the synchro transmitter, free to turn and usually drives a light load, such as a pointer, dial, or some other indicating device. The drive is accomplished directly, or through a light gear train. The angular position that the rotor assumes is dependent upon the stator voltages received from the syncbro transmitter.

The differential synchro transmitter (abbreviated DT), resembles the regular synchro transmitter in that the rotor is mechanically driven, and the stator is similar. However, there are three separate windings on the rotor, and these windings are electrically displaced 120 degrees. Differential transmitters are used to compensate for errors existing in various parts of a synchro system. With the insertion of a differential synchro transmitter in a synchro system, the angular position of the receiver rotor with respect to the transmitter rotor may be varied by turning the rotor of the differential transmitter.

The differential synchro receiver is similar in design to the differential transmitter, but the rotor is free to turn. It is used when it is desired to interpret the sum or difference of two angular positions. If the differential synchro receiver is connected to two synchro transmitters, the differential synchro receiver assumes a position corresponding to the angular sum or difference (depending on the connections) of the transmitter rotor positions.

The synchro control transmitter is somewhat similar to the synchro receiver. The windings of the control transformer have a higher impedance than the windings of the other synchro units, and the rotor of the control transformer is not free to turn. Voltages from a synchro transmitter produce a voltage in the rotor of the control transformer, which is representative of the angular displacement of the transmitter rotor. The control transformer is used where it is desired to obtain a voltage output only, which is indicative of angular position.

**Circuit Operation. The** synchro transmitter operates as a variable transformer with its rotor as the primary and the stator windings as **secondaries.** The voltages induced in each stator winding are proportional to the cosine of the angle between the rotor and the individual stator winding. The following

diagram illustrates a typical synchro circuit consisting of a synchro transmitter and receiver.



## Synchro Transmitter-Receiver Circuit

When ac voltage is applied to the rotor of the synchro transmitter, voltages are induced in the stator windings (S1, S2, and S3), and the magnitude and phase of these voltages are dependent upon the position of the synchro rotor. The turns ratio between the synchro rotor and stator is generally 2.2:1, so that the maximum voltage that can be induced across an individual stator winding is 52 volts when standard 115V, 60 Hz, ac is applied to the rotor. The rotor of the synchro illustrated is, by convention, in the  $0^{\circ}$ position. This reference is used throughout synchro systems. Designations S1, S2, S3, R1, and R2 are also standard designations for all synchros. When the rotor of the synchro transmitter is in the 0° position flux linkage between the rotor and winding S2 is maximum, and 52 volts is inducted across S2. Stator windings S1 and S3, however, are at 60° angles to the rotor and only half as much voltage (26 volts) is induced across S1 and across S3, since the cosine of 60° is 0.5. At this point, circuit operation can be more easily understood by assuming that the receiver rotor is removed. Since the stator windings of the transmitter are connected directly to the stator windings of the receiver, the voltage applied to each individual receiver stator winding corresponds to the voltages induced in each stator winding of the transmitter. Current flows from S2 of the transmitter through S2 of the receiver, and divides equally through S1 and S3, since equal voltages are applied to S3 and S1. Current flow will, of course, be reversed when the polarity of the input voltage reverses. Each suitor winding in me receiver generates a magnetic

field, but the important point to consider is the resultant field. The following vector diagram illustrates the direction and magnitude of each receiver stator field and the resultant field.



# Resultant Receiver Field Vector Analysis (Transmitter Rotor At 0<sup>°</sup>)

As can be seen from the vector diagram, the **result**ant field points in the same direction as the transmitter rotor. Should an iron bar rotor be placed in the receiver field it tends to line itself up with the resultant field; however, the iron bar rotor can align itself in either of two positions  $180^{\circ}$  apart as shown in the following illustration.



Behavior of Electromagnet and Iron Bar

In figure A the iron bar rotor is held in the position illustrated. The paths of the magnetic lines of force are lengthened and when the bar is released it quickly rotates to position B in accordance with the stretched rubber band concept for the behavior of magnetic lines of force. Figure C illustrates the position that the rotor would assume if it is rotated to a position, where the "Y" end of the bar is nearer to the electromagnet than the X end, and is released. Thus a synchro receiver with an iron bar rotor displays ambiguity, that is, it has two stable positions  $180^{\circ}$  apart. To avoid the possibility of this  $180^{\circ}$  error the rotors on synchro receivers are energized by the same ac source as the transmitter rotor. This makes the receiver rotor an electromagnet, and there is now only one stable condition. In addition to the advantage of having only one stable condition, the energized rotor provides much greater torque, and synchro receivers with energized rotors do not have constant stator current as an iron bar receiver would have. The following is a standard synchro transmitter receiver system with the transnutter rotor positioned at  $330^{\circ}$  and the receiver rotor held at  $O^{\circ}$ .



Transmitter 330°, Receiver Held At 0°

Voltages are induced in the synchro transmitter stator windings which are proportional to the cosine of the angle between the rotor and the stator windings. S2 and S3 are each displaced  $30^{\circ}$  from the rotor and the voltage induced in S2 and S3 is, therefore, 45 volts. S1 is now at right angles to the rotor and no voltage is induced in S1. The receiver rotor, which is being held at  $0^{\circ}$ , induces voltages in the synchro receiver stator windings, which are again proportional

to the cosine of the angle between the receiver rotor and the receiver stator windings. Receiver stator winding S2 is parallel to the rotor and 52 volts is induced in S2. S1 and S3 are displaced 60° from the rotor and 26 volts is induced across S1 and S3. The synchro transmitter receiver circuit is now unbalanced, that is, voltage differences exist between the stator windings of the transmitter and receiver, and stator current flows, setting up a stator field in the receiver in such a direction as to exert a clockwise torque on the receiver rotor. Remember that the transmitter is so constructed that the transmitter rotor cannot rotate except under the influence of the controlling shaft. When the synchro receiver rotor, which is being held at 0°, is released it rotates in a clockwise direction due to the clockwise torque applied to it as a result of the receiver stator field, generated by a stator current. As the receiver rotor approaches 330° the degree of unbalance between the transmitter and receiver diminishes, and hence, stator current decreases, since the voltages induced in the receiver stator windings by the receiver rotor approach the voltages induced in the transmittor stator windings by the transmitter rotor. When the receiver rotor reaches the same bearing as the transmitter rotor (in this case 330°) the voltages induced in the receiver stator windings are equal to the voltage induced in the transmitter stator windings. A balanced condition now exists, and stator current no longer flows, hence, torque is no longer produced, and the receiver rotor ceases to turn. It can be seen, then, that the transmitter supplies stator current to establish a field in the receiver, and produces torque only when the receiver is out of alignment with the transmitter. Torque produced in the receiver is proportional to the amount of error between the transmitter rotor and the receiver rotor. At very small error angles, the torque produced in the synchro receiver is insufficient to overcome the friction of the bearings and load. For this reason, friction is made as low as possible in the synchro receiver, and the maximum error in synchro receivers is generally less than 1°. Another important synchro unit frequently encountered is the differential transmitter. The differential synchro transmitter is used in circumstances where a correction must be inserted in the angular information being transmitted, or where the sum or difference of two angles must be transmitted. An

example of this is the conversion of the relative bearing of a target to true bearing. It has been previously stated that synchros operate as variable transformers. This statement applies to the synchro differential transmitter as well as all synchro units. In the case of the synchro differential transmitter, the stator is the primary of the variable transformer, while the rotor windings serve as the secondary. The following schematic diagram illustrates a differential transmitter inserted between a synchro transmitting and receiver.



## **Differential Transmitter Connections**

In a differential synchro transmitter the voltage ratio is one to one. With the differential transmitter at its electrical zero  $(0^{\circ})$  synchro data is passed from the transmitter to the synchro receiver without alteration. In the above illustration both the synchro transmitter and differential transmitter are mechanically positioned to O°. Since the rotor of the synchro transmitter is at 0°, 26 volts is induced in transmitter stator windings S1 and S3, and 52 volts is induced in stator winding S2. The stator windings of the synchro transmitter are directly comected to the stator windings of the synchro differential transmitter, and the voltages induced across the transmitter stator windings are developed across the differential transmitter stator windings. The differential transmitter rotor windings are directly connected to the stator windings of the synchro receiver and whatever voltages are induced in the differential rotor windings are applied to the stator windings of the receiver. When the differential transmitter rotor is positioned at  $0^{\circ}$  all three rotor windings, which are positioned electrically 120° apart, form an angle of 0° with their respective stator winding .(R1 with S1, R2 with S2,

etc) and maximum voltage is induced in each rotor winding. Since the effective turns ratio is 1:1, 52 volts is induced in R2, and 26 volts is induced in R1 and R3. Therefore, 52 volts are applied to receiver stator winding S2, and 26 volts are applied to stator windings S1 and S3. The resultant receiver stator field is in the same direction as the transmitter rotor, and the receiver rotor aligns itself with this field. As long as the DT is positioned at 0° the receiver rotor positions itself at the same bearing as the transmitter rotor. If the differential transmitter is positioned to some bearing other than 0° the receiver indicates the position equal to the transmitter bearing minus the DT bearing, or in other words, the receiver indicates the difference between the transmitter and differential positions.



#### Effect of Changing Differential Transmitter Position

In the preceding illustration the synchro transmitter is positioned at  $0^{\circ}$  and the differential transmitter rotor has been rotated to a position of 120°. Maximum voltage is now induced in rotor winding R1 which is connected to stator winding S1 of the receiver. Twenty six volts is induced in rotor windings R2 and R3, and is applied to the receiver stator windings. The resultant receiver stator field points toward 240° and the receiver rotor aligns itself toward 240°. In all cases, where the differential transnutter is directly connected between the transmitter and receiver, the receiver shaft position is equal to the position of the transmitter shaft minus the position of the differential. If it is desired to have the differential position added to the transmitter reading, it is necessary to reverse S1 - S3 and **R1** - R3 of the differential. It has been stated that the DT is effectively a 1:1 transformer. Actually there is a slight step-up ratio since

## **ELECTRONIC CIRCUITS**

extra turns are added to the rotor to bring the voltage ratio up to 1:1 to make up for transformations, copper, and core losses present in the differential transmitter. The fact that this ratio difference between the stator exists, gives rise to an electrical condition of unbalance, which occurs when a differential transformer is inserted in a synchro system. In a conventional synchro system there is no stator current when the transmitter and receiver are in a balanced data (in alignment). However, when a differential transmitter is inserted in the system, the no stator current condition no longer prevails when the system is in balance. The reason for this is that the differential stator windings can be designed to match the impedance of the transmitter stator windings, or the impedance of the differential rotor windings can be made to match that of the receiver stator windings. Since the differential transmitter cannot be made a one to one transformer in both directions, it is not possible to match both input and output impedances at the same time. As a consequence, there is current flow in both transmitter and receiver stator circuits even when the system is balanced, and the effect of this current is to reduce the accuracy of the system. Synchro capacitors may be used to reduce this stator current and hence, increase system accuracy. Synchro capacitors will be discussed in a subsequent paragraph. The differential synchro receiver is comected between two synchro transmitters, and it is used to indicate the angle between the two transmitter shaft positions.



Wiring Diagram of Synchro System Designed to ADD Transmitter Position to Differential Position

In the following illustration, synchro transmitter number 1 is mechanically positioned to a bearing of  $180^{\circ}$  and transmitter number 2 is positioned at  $120^{\circ}$ .



## Synchro Differential Receiver Inserted Between Two Synchro Transmitters

The differential receiver is electrically similar to the differential transmitter, but the DR rotor unlike the differential transmitter, is free to turn. In a simple transmitter-receiver synchro system a balanced state is achieved when the voltages applied to the receiver stator windings by the transmitter are canceled by equal and opposing voltages induced across the receiver stator windings by the receiver rotor. The synchro system illustrated above attains a balanced state when the differential receiver assumes an angular position equal to the difference between the angular positions of the two transmitters. If either, or both, of the synchro transmitters are moved the synchro system becomes unbalanced, and stator current flows, creating torque which causes the differential receiver to rotate until once again a balanced condition is reached. The synchro control transformer (CT) is used to produce an output voltage which is indicative of the error between two shafts. This output voltage is called an error voltage because it exists only when the two shafts are not in alignment.

The following illustration depicts a simple synchro transmitter CT circuit and associated drive equipment.

d



#### Simple Antenna Control System

The synchro transmitter mechanically positioned by a hand crank. The synchro transrrdtter is connected to the synchro control transformer in the standard manner, that is, S1 of the transmitter to S1 of the receiver, etc. The control transformer rotor is comected to a servo amplifier and the servo amplifier drives a drive motor, which is geared to the device being controlled; in this case, it is an antenna. The antenna is mechanically connected back to the control transformer to provide feedback. When the CT rotor is in alignment with the transmitter rotor there is no error voltage produced, and hence there is no output from the servo amplifier and the drive motor does not operate. It is important to note that the CT rotor is considered to be in alignment with the transmitter rotor when the CT rotor is displaced 90° from the transmitter rotor. In this position no voltage is induced in the CT rotor since the CT rotor is now perpendicular to the resultant CT stator field. When the synchro transmitter rotor is timed to some new

position, the resultant control transformer stator field also rotates to some new position, and this field is no longer perpendicular to the CT rotor so that a voltage is now induced across the CT rotor. his ac voltage is fed to the servo amplifier where it is compared with a reference voltage, which is of the same phase as the transmitter rotor excitation voltage, and an output is produced from the servo amplifier, which causes the antema drive motor to rotate the antenna. As the antenna rotates toward the desired position the error voltage produced by the CT diminishes, since the CT is mechanically coupled to the antenna. When the antenna reaches the desired position the rotor of the CT is now perpendicular to the resultant receiver stator field set up by the synchro transmitter and the CT output error voltage is zero. There is no longer an output from the servo amplifier and the drive motor ceases to rotate the antenna. The stator windings of a control transformer consists of many turns of fine wire, and presents a high impedance to current flow, thus reducing the load presented to the transmitter, and allowing several control transformers to be utilized in conjunction with a single transmitter. High impedance windings are also necessary since the rotor of the control transformer usually operates into a high impedance load such as a servo amplifier.

When the rotors of synchro devices turn in unison with their input and output shafts such devices are known as one-speed synchro systems. When a synchro receiver is in alignment with the transmitter no torque is developed, and with any movement of the transmitter rotor, the receiver must first overcome the restraining forces of the load before it can follow the transmitter. Even with no load the receiver must first overcome the restraining forces due to the friction of the receiver bearings before rotation occurs. This results in an angular displacement between the input and output shafts, called the no load error. Geared synchro systems are used when a high degree of accuracy is required. The following diagram illustrates the difference in error between 1-speed and 36-speed systems.



## Comparison of ERROR Between I-Speed and 36-Speed Synchro System

It can be seen in the preceding illustration that the 36-speed synchro system is far more accurate than the one-speed system. In both systems the error caused by bearing friction and resistance of the load amounts to one degree. In both systems the controlling shaft is rotated 10°. In the 1-speed system the transmitter is rotated  $10^{\circ}$  and the  $1^{\circ}$  error limits the receiver rotation to 9° and hence the output shaft rotates only 9°. In the 36-speed system, however, the transmitter is rotated 350° when the controlling shaft is rotated 10°, and the 1° error limits the receiver to 359° of rotation. This 359° of rotation causes the output shaft to rotate 9.97°. In other words, system error of the 36-speed system is only approximately .03° compared to 1° for the one-speed system. One disadvantage of geared synchro systems is that the self synchronous feature of the one-speed system is lost. When power to a one-speed system is interrupted, and the transmitter is turned the receiver of course does not follow, but when power is restored it aligns itself correctly with the transmitter. However, in a geared system, such as the 36-speed system used extensively in the Navy, 36-positions of the output shaft exist for which the receiver is in alignment with the transmitter.

The self-synchronous feature of the one-speed system and the high accuracy of the 36 speed system can be combined by making use of coarse and fme synchros connected to the same input and output shaft. Following is an illustration of this system.



## 36-Speed Synchro System Using Coarse-Fine Synchros (Dual Speed System)

In the coarse-free synchro system, incorrect alignment of the 36-speed system is prevented, because when the shaft error is large the one-speed system has control, and reduces the error to a small value. At this point the 36-speed synchro takes over, and further reduces the error to a very small value. When a dualspeed synchro system utilizes a control transformer to drive a servomechanism a cross-over system or synchronizer must be used. The function of this system is to determine whether the coarse or tine CT error voltage is fed to the servo amplifier. When the input shaft of a 36-speed system is turned 2.5° the fme CT rotor is displaced 90° from its zero voltage position. This position provides maximum induced voltage in the fine CT rotor, but, more important, this is the first maximum voltage point since the zero error position. For this reason, corss-over systems are designed so that the fme CT has control for error angles less than 2.5°. For larger error angles the synchronizer or cross-over system cuts out the fme CT and the coarse CT takes control. There are a variety of cross-over circuits in use. One system utilizes a plate-circuit relay which normally allows the 36-speed CT to control the servo system. However, when the error angle increases beyond 2.5°, increasing the output of the coarse CT, the relay is energized and the coarse (1-speed) CT assumes control of the servomechanism. Some cross-over arrangements use purely electronic switching; these usually depend upon biasing and limiting circuits.

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It has been pointed out that the differential synchro and the synchro control transformer both draw current from the transmitter, even when the system reaches a position of electrical and mechanical balance. The differential draws current because of the step-up turns ratio between stator and rotor. In the case of the control transformer current is drawn from the transmitter, because the CT rotor is not energized, and opposing voltages are not induced in the CT stator. In order to reduce the current flow when either or both of these units are used, synchro capacitors are connected into the circuit. Current flow in a synchro system is comprised of resistive and inductive current. If the inductive reactance of a differential stator winding is shunted by an equal capacitive reactance the inductive current is then effectively cancelled by the capacitive current. In this case all that the transmitter actually does is to supply power demanded by the resistive losses of the circuit. Synchro capacitors are manufactured with three capacitors contained in a single unit and are internally connected as shown in the following illustration.



#### Synchro Capacitor

The individual capacitors are matched to a tolerance of less than one percent to maintain proper current balance. Synchro capacitors are connected into **various** synchro systems as shown in the following illustration.



Synchro Capacitor Connections

Part A of the illustration shows the comections for a differential transformer as used with a transmitter and receiver, while Part B shows the connections for a control transformer and transmitter. In Part C both a differential transformer and a control transformer are used and each requires a separate capacitor unit.

Synchro capacitors are used only when it is desired to cancel or partially cancel existing current. The synchro capacitor is never used in simple transmitterreceiver circuits because in such a system the reactive component of stator current is assumed to be zero and insertion of a synchro capacitor only increases current and throws the system out of balance. However, exciting current in this type system may be reduced by connecting a capacitor across the rotor.

## Failure Analysis.

No Output. Failure of a receiver rotor to rotate when the transmitter is rotated, or no-voltage output from a control transformer are considered no-output conditions. Frozen bearings or a jammed load could restrain a receiver rotor, and lack of excitation to the transmitter rotor would disable the synchro system. Existence of the first condition can be readily ascertained by attempting to manually rotate the receiver rotor. Existence of the second condition (no transmitter excitation) can be readily checked by measuring the voltage across the transmitter rotor. If no voltage is present check for a blown input line fuse, or an open input line. If voltage is present across the transmitter rotor, but the system is inoperative, reenergize the system and check the continuity of the transmitter rotor. If any two stator lines are open the synchro system will be inoperative. Resistance checks can be used to determine continuity of stator windings and stator leads.

Improper Operation. Improper operation is the result of incorrect wiring or an open or shorted winding in any of the synchro units, or excessive friction in bearings. If any of the stator windings are reversed, the units will not overheat and they will develop normal torque, but the receiver will turn in the direction opposite to that of the transmitter and a 120° bearing error will exist. If the rotor windings are reversed, operation will be normal except that a 180° bearing error will exist. An open receiver rotor results in weak torque, receiver hum, and possible ambiguous behavior, since the receiver rotor now operates as an iron bar rotor. The transmitter supplies excessive current when the receiver rotor is not energized, and may bum out or blow line fuses. An open or shorted stator winding results in erratic operation and could possibly overheat synchro units.

In general, if the synchro units operate **smoothly**, do not overheat, and produce normal torque, but do not rotate in the proper direction and/or an error which is some multiple of  $60^{\circ}$  exists, the probable cause is incorrect wiring. Since different units of a synchro system are usually located some distance from each other, and are connected by busses or cables which often pass through junction boxes, wiring errors are frequently made during repair or during new installations, or modifications to existing installations. Symptoms such as overheating, blown fuses, hum, or erratic operation are indicative of a short or open winding within the synchro units, or open or shorted interconnecting cables. Resistance measurements are valuable in locating shorts and opens in synchro to another it should be assumed that an ohmmeter will show the same reading across rotor or across stator windings of similar units, within close tolerances. **Be** certain that all power is disconnected before resistance or continuity measurements are attempted. Typical resistance values are low, ranging from a fraction of an ohm in the rotor of large synchros, to several hundred ohms in the stator windings of smaller units.

## SERVO MOTOR-CONTROLLER-CIRCUIT

#### Application.

The dc servo motor-controller, also called a servo amplifier, is used in conjunction with a synchro system to control a servo motor which operates an indicator dial or rotates a load to a similar position.

## Characteristics.

Drives dc servo motor.

Output is proportional to magnitude of error input.

Is phase sensitive, direction of servo motor rotation is determined by phase of error input.

Use is limited to low power applications.

## Circuit Analysis.

General. 'The dc servo motor-controller receives an error voltage input from a synchro control transformer (CT) and effectively compares this error voltage with an ac reference voltage to provide an amplified dc output which drives a dc servo motor. The dc servo motor-controller circuit consists of a phase sensitive detector-amplifier, with the ac reference voltage used as plate voltage, coupled to a dc amplifier, whose output drives a dc servo motor. The magnitude of the dc output, which determines the speed of the drive motor, is dependent upon the amplitude of the error voltage. The polarity of the dc output, which determines the direction of servomotor rotation, is dependent upon the phase relationship between the error voltage input and the ac reference voltage.

**Circuit Operation.** The following schematic diagram illustrates a typical dc servo motor-controller circuit and associated synchro and drive equipment.



Servo Motor-Controller Circuit

Transformer T1 couples the error voltage in push pull ( $180^\circ$  out-of-phase), from the rotor of the synchro control transformer to the grids of detector amplifier tubes VI, and V2. Resistors R2 and R3 serve as load resistors for VI and V2, respectively. Resistors R1 and R4 provide degenerative feedback to the cathode of V1 and V2.

Transformer T2 applies the ac reference voltage in parallel (in-phase) to the plates of detector-amplifier tubes VI and V2. Capacitor Cl and C2 falter the pulsating dc developed across R2 and R3. V3 and V4 serve as dc amplifiers with R5 and R6 as their cathode resistor, and R7 and R8 as their plate load. Dc servo motor B1 is mechanically geared to the load to be positioned and is also mechanically coupled back to the synchro control transformer.

Tubes V1 and V2 conduct only on positive alternations of the ac reference voltage. When the synchro control transformer is in alignment with the synchro command transmitter there is no error signal input, and V1 and V2 conduct equally during the

positive portion of the reference signal. Thus equal voltages are developed across R2 and R3. At this point V1 and V2 are functioning as rectifiers, and the voltage across R2 and R3 is pulsating dc, which is faltered by capacitors Cl and C2, and applied to the grids of V3 and V4. Dc amplifier tubes V3 and V4 conduct equally under this condition, and the voltage developed across R7 is equal to the voltage across R8. Therefore, no difference in potential exists between the plates of V3 and V4 and, hence, no current flows through the armature of servo motor B1, and the motor will not rotate. When the synchro command transmitter is moved to some new position, the synchro control transformer is no longer in alignment with the command transmitter rotor and an error voltage output is produced by the synchro control transformer and is applied to the servo motorcontroller circuit. It is important to keep in mind that, the ac reference voltage applied to the plates of V1 and V2 is from the same source as the synchro excitation voltage, and any error voltage induced into

the control transformer rotor is either in-phase or 180° out-of-phase with the reference voltage. Assume that the angular displacement between the synchro command transmitter and the synchro control transformer is in such a direction that the error voltage induced across the CT rotor is in-phase with the reference voltage. When the reference voltage goes positive, a positive half cycle is applied to the grid of V1 and a negative half cycle of error voltage is applied to the grid of V2 (remember that TI is effectively a push-pull transformer). The conduction of V1 increases and, therefore, an increased voltage drop occurs across R2 and this voltage is faltered by Cl and applied to the grid of **d-c** amplifier V3, causing the conduction of V3 to increase. At the same time, the negative half cycle of error voltage applied to the grid of V2 decreases conduction of V2, causing a decreased voltage drop across R3, and consequently the d-c voltage coupled to the grid of V4 decreases, reducing the conduction of V4. Since the conduction of V3 increased, while the conduction of V4 decreased, a difference in potential now exists between the plates of V3 and V4 due to the increased voltage drop across R7, and the decreased voltage drop across R8. Current now flows from the plate of V3 through the armature of drive motor B1 to the plate of V4 and the motor rotates driving the load in the desired direction. VI and V2 conduct only during the positive half cycle of the ac reference input. Drive motor operation, however, is not erratic since filter capacitors Cl and C2 maintain fairly constant voltages across the grids of V3 and V4, causing the servo-motor-controller output to be fairly constant. The drive motor is also mechanically connected through gears to the synchro control transformer and rotates the synchro CT rotor toward the position of alignment with the synchro command transmitter. As the angular displacement between the CT rotor and the transmitter rotor diminishes the error voltage produced by the CT diminishes and the dc output of the servomotor-controller decreases, causing the drive motor to rotate slower. When the CT reaches the same bearing as the command transmitter, drive motor rotation ceases because no error voltage is produced by the CT, and consequently there is no longer an output from the servo motor-controller. If the synchro command transmitter is rotated in the other direction, the resulting error voltage produced by the synchro control transformer will be 180° out of phase with the reference voltage. Circuit operation

will be the same, but the polarities are reversed, V1 is driven negative causing a negative voltage to be applied to the grid of V3, and the voltage on the plate of V3 increases. V2 is driven positive causing a positive voltage to be applied to the grid of V4, and the voltage at the plate of V4 decreases. Current flows from the plate of V4 through the armature of servo motor B1 to the plate of V3, causing the servo motor to rotate in the direction opposite to the direction that it rotated previously.

## Failure Analysis.

No Output. Failure of the drive motor to rotate is considered to be a no-output condition. In a positioning system such as the dc servomotor system, no output could result from a defective synchro system, a defective servomotor-conroller or a defective servomotor, or associated mechanical drive equipment. The synchro system can be checked by measuring the voltage across the CT rotor with an ac voltmeter as the command transmitter is rotated 360°, and the servo motor-controller circuit disabled by removing V3 and V4. If the rotor voltage (called the error voltage) should vary smoothly from zero volts to about 55 volts the synchro system is operating normally. To check for a jammed gear train, load, or servo motor, attempt, with the power disconnected, to manually rotate the servo motor shaft. If the windings of the servomotor show the proper resistance when checked with an ohmmeter and there is not excessive leakage between windings the motor is most likely good. However, if a spare motor is available, substitution is a sure way of determining the merit of the servo motor. If the servo motor, gear train and synchro system is good, inability to position the load is most likely due to a defective servo motor-controller. Failure of error input transformer T1 and reference voltage transformer T2 would render the servo motor-controller inoperative. Using an ac voltmeter, check for 115 VAC on the plates of V1 and V2 to determine whether or not T2 is defective. T1 can be checked by observing the presence of an ac error voltage on the grid of VI and V2, while the synchro command transmitter is rotated. Check the voltage present at the junction of R7 and R8 to determine whether or not lack of plate supply voltage is the cause of no output. Failure of detectoramplifier tubes V1, V2, or failure of dc amplifiers V3, or V4, could cause **no-output**. Failure of an individual circuit component is not likely to cause a no-output

condition, but instead, an unbalanced condition would result between the output of dc amplifiers V3 and V4, and improper operation would most likely result.

Improper Operation. Improper operation is considered any type of operation other than proper operation, such as, sluggish or slow rotation of the drive motor, erratic or jerky rotation, or a tendency to rotate better in one direction than the other. Improper operation could result from a defective synchro system, excessive binding of the gear train or load, a defective servomotor, or defective servo motor-controller circuit. The synchro system, gear train, and servo motor can be checked as explained previously, and if these associated components are satisfactory, improper operation is likely due to a faulty servo motor-controller circuit. The servo motor-controller circuit can be thought of as consisting of two branches, V1, V3, and associated circuit components comprise the upper branch, and V2 and V4, together with their associated components, comprise the lower branch. Any component defect that alters the performance of one branch as compared to the other could result in improper operation, possibly manifesting itself as a tendency of the drive motor to rotate better in one direction than the other, or possibly continuous or erratic rotation in one direction. A possible cause of improper operation is defective tubes. It would also be advisable to check the dc power supply voltage, since low supply voltage could possibly cause sluggish operation. A change in value, short, or open of RI or R2 would, of course, affect the operation of detector amplifier V1 and, likewise, a defect in R3 or R4 would adversely affect V2. If Cl or C2 shorted, V3 or V4, respectively, would be inoperative as amplifiers and improper operation would result. A change in value or defect in either R5, R6, R7, R8, would destroy the balance between dc amplifiers V3 and V4, and improper operation could result. With the equipment deenergized all resistors can be checked for proper value with an ohmmeter, capacitors Cl and C2 can be checked w-ith an in-circuit capacitor checker.

# **RESOLVER-ORIVER CIRCUIT**

## Application.

The resolver-driver circuit is used to drive an ac resolver, which is used as a computing element in problems involving coordinate conversion, coordinate rotation, and resolution of vectors. Resolverdrivers are also used to drive sweep resolvers in radar indicators.

#### Characteristics.

Utilizes a pentode and a triode to drive a resolver. Operates on the principle of a feedback amplifier.

"Provides power amplification with minimum distortion, voltage gain is unity.

## Circuit Analysis.

**General.** The resolver-driver circuit amplifies an ac synchro voltages to a power level sufficient to drive an ac resolver with a minimum of distortion. The resolver-driver is basically a feedback amplifier consisting of a pentode voltage amplifier, coupled to a triode amplifier which drives the resolver primary winding. R-C coupling is used between the first and second amplifier stage, and distortion is minimized by the use of degenerative feedback which is obtained from a feedback winding within the resolver and is coupled back to the grid of the first amplifier.

**Circuit Operation.** The following schematic - diagram illustrates a resolverdriver circuit.



#### **Resolver Driver Circuit**

Resistor RI is the input grid resistor for pentode amplifier V1. Resistor R2 is the plate load and R3, which is bypassed by Cl, provides cathode bias for VI. Resistor R4 is the screen dropping resistor for Vl, and C2 is the screen bypass capacitor. R-C coupling consisting of capacitor C3 and resistor R7 is employed between V1 and V2. A voltage divider consisting of R5 and R6 is used to drop the plate supply voltage to the proper value of plate voltage for V1. Capacitor C4 bypasses ac voltage variations to ground and prevents unwanted degeneration. Resistor R9 which is bypassed by C5 serves as the cathode bias resistor for triode amplifier V2. The plate load for V2 is the primary winding of the resolver. The primary winding of the resolver is shunted by a series r-c network, consisting of R8 and C6, which is intended to compensate for the inductive impedance of the resolver winding and thereby maintain the power factor near unity. Degenerative feedback is developed across the feedback winding within the resolver and applied to the grid of VI through resistor R1O.

When an ac input is applied to the input of the resolverdriver it is amplified by conventional ac amplifier stage V1, and is capacitively coupled to the grid of driver stage V2. The ac synchro voltage applied to the grid of V2 is amplified and developed across the primary of the resolver, and is inductively coupled to the resolver feedback winding and the resolver secondary windings. R-C network, R8-C6, cancels the effects of the inductive reactance of the resolver windings and makes the output load appear resistive, thus bringing the power factor of the output load to unity, Degenerative feedback developed by the resolver feedback winding is attenuated by resistor R1O and is applied to the grid of V1. The value of R1O is such that the amplitude of the degenerative feedback is great enough to reduce the closed loop voltage gain of the resolverdriver to unity. The degenerative feedback improves the fidelity and stability of the resolverdriver. Stability is improved since a decrease in emission of the tubes, which would normally reduce the output (if feedback

were not present), instead tends to decrease the magnitude of the present feedback and results in increased closed loop gain, since there is less degenerative feedback (which is  $180^{\circ}$  out-of-phase with the input) present at the grid of VI.

## **Failure Analysis**

No Output. A no-output condition in the resolverdriver circuit could result from failure of the power supply or failure of one of the tubes. Check the power supply voltage with a voltmeter, and also check the tubes. If operation is not restored, a defective circuit component is most likely the cause of no output. Voltage checks of tube elements may be helpful in localizing the fault to a stage. Keep in mind that a fault in one tube element circuit such as the grid or cathode circuit, may effect the voltage present on other tube elements. Voltage checks are, therefore, only a means of localizing the trouble, and further resistance measurements are usually necessary to locate the component at fault. Improper plate and screen voltage on V1 could be caused by a defect in voltage divider R5, R6 or capacitor C4. Check R5 and R6 for proper value and check C4 for a possible short with an ohmmeter. If either plate voltage or screen voltage is incorrect check for proper value plate load resistor R2 and also check C3 for a possible short. Also check screen resistor R4 and its bypass capacitor C2 for a possible short or excessive leakage with an ohmmeter. Improper cathode bias could be caused by a defect in cathode resistor R3 or bypass capacitor Cl. Check R3 for proper value with an ohmmeter, and check Cl for a possible short or excessive leakage, also with an ohmmeter. Improper grid bias could be caused by a defect in RI or possibly a defect in the feedback circuit, consisting of the feedback winding within the resolver and R1O, or by a defect in the output circuit of the preceding stage. Check the resistors in question with an ohmmeter and also check the continuity of the resolver winding. Improper grid bias on amplifier V2 would result if coupling capacitor C3 becomes shorted or if there is a significant change in the value of grid resistor R7. No output would also result if capacitor C3 opens, since the ac signal would not reach the grid of V2. Check R7 for proper value with an ohmmeter and check C3 with an in-circuit capacitor checker, since both a short or an open could cause a no-output condition. Improper cathode voltage on V2 could be caused by a defect in R9 or a short in bypass capacitor C5. Check

R9 for proper vrdue and check C5 for possible leakage or a short. If the primary of the resolver opened there would be a no-output condition. This can easily be detected since there would be no plate voltage on V2. Various defects within the resolver could cause a nooutput condition to exist. The resolver may be checked by measuring the resistance of its windings and by checking for excessive leakage between windings.

Low Output. The resolver-driver is basically a feedback amplifier. A prime characteristic of a feedback amplifier is the ability to maintain their gain at a predetermined level regardless of variations in tube characteristics with age. This characteristic exists because a tendency for the output amplitude to decrease also results in a decrease in the amplitude of the degenerative feedback, which is developed in the output circuit. This decrease in degenerative feedback has the same effect as increasing the input amplitude, and the overall effect is for the gain to remain constant. However, if the components deteriorate beyond the limits of feedback control low output could result. Check the power supply voltage and adjust if necessary. If proper operation is not restored a defective circuit component is most likely the cause of decreased output. A decrease in value of R1O would result in a greater amount of negative feedback reaching the grid of VI and result in decreased closed loop gain, hence, decreased output would result. Check R1O for proper value with an ohmmeter. Voltage checks of tube elements should reveal whether or not a change in operating levels caused by a defective component is the cause of low output. Any discrepancies found during voltage checks can be followed up with resistance measurements of suspected components, as explained in the previous paragraph, to locate the component at fault. A decrease in value of R8 or a shorted C6 could shunt a portion of the output signal around the primary of the resolver, resulting in decreased output. Check R8, with an ohmmeter, for proper value and C6 with an incircuit capacitor checker. A defective resolver can also cause a low output condition to exist. Measure the resistance of all resolver windings being alert for a lower than normal reading which would indicate that some of the turns on the winding in question are shorted. Also check for excessive leakage between windings and to ground.

**Distorted Output.** A defect in the feedback circuit is a prime cause of distorted output in resolver-driver

circuits. Measure the resistance of the resolver feedback winding and check the ungrounded end of the feedback winding for a possible short to ground. Also check feedback resistor R1O and V1 grid resistor RI for proper value. If the feedback circuit checks out good, check the power supply voltage and check the tubes by exchanging them with tubes which are known to be good. If the resolver-driver output is still distorted a defective component could be altering the operating level of one of the stages and causing distortion to occur. Voltage and resistance checks may be made, as explained previously, to locate the component at fault.

## PHASE SENSITIVE NULL DETECTOR CIRCUIT

## Application.

The phase sensitive null detector is used in servo control circuits to operate a dc relay when the input error voltage is in phase with the reference voltage.

#### Characteristics,

Output (position of dc relay) is dependent upon phase relationship between an input error voltage and a reference voltage.

Circuit may be connected so that the output relay is energized when both signals are in-phase, or when they are out-of-phase.

Use a pentode and two triodes.

#### Circuit Analysis.

**General.** The phase sensitive null detector consists of a two stage ac amplifier, a phase sensitive detector, and a relay control tube with a dc relay in its plate circuit. Basically the phase sensitive null detector compares ac error voltage to a reference ac voltage and determines whether or not they are in phase. The ac amplifiers provide sufficient gain so that very small error voltages may be effectively compared with the reference voltage, allowing an output to be produced almost immediately after the error voltage becomes in phase with the reference voltage. The amplified ac error voltage is applied to the phase sensitive detector stage through a transformer. The amplitude and polarity of the phase detector output is dependant upon the amplitude of the error voltage input and the phase of the error input with respect to the reference voltage. With the circuit connected in the standard manner the phase sensitive detector stage produces a positive voltage output when the error signal and reference signal voltages are in phase. The detector stage output voltage is faltered and applied to the grid of the final stage, a dc relay control tube. When the detector output voltage is positive, as it is when the error and reference voltages are in phase, conduction of the relay control tube is increased and the relay becomes energized. If the error voltage is out-of-phase with the reference voltage, the detector output voltage is negative and the relay control tube does not energize the output relay.

**Circuit Operation.** The following schematic diagram illustrates a phase sensitive null detector.

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Resistor R1 serves as the input grid resistor for pentode amplifier VI. Resistor R2 serves as the plate load for VI while R3 which is bypassed by Cl functions as the cathode bias resistor for VI. Resistor R4 is a series screen dropping resistor, and capacitor C2 is the screen bypass for V1. R-C coupling between V1 and triode amplifier V2 is pronded by capacitor C3 and grid resistor R5. Resistor R8 which is bypassed by C6 serves as the cathode bias resistor for V2, while the primary L1, of transformer T1 which is shunted by C5 serves as the plate load for V2. Resistors R6 and R7 form a voltage divider between the plate supply and ground to provide the proper plate voltage to V1 with capacitor C4 functioning as a bypass capacitor. Transformer T1 couples the error voltage to a phase sensitive detector consisting of diodes CR1 and CR2 and resistors R9 and R1O. The reference voltage is coupled to the phase detector stage via a centertap on the secondary of T1. The output of the phase detector is applied to a filter network "consisting of resistors R11, R12 and capacitor C7. The filtered phase detector output is applied to the grid of relay control tube V3. Resistor R13 serves as an unbypassed (degenerative) cathode bias resistor for V3, while dc relay K1 forms the output load for V3.

The ac error voltage is applied to the grid of amplifier VI, and the large amplitude error voltage devel-

oped across plate resistor R2 of amplifier V1 is coupled through capacitor C3 to the grid of amplifier V2. Amplified error voltage is developed across the primary of transformer T1 and is inductively coupled to the secondary of T1. The ac reference voltage is applied to the phase sensitive null detector through a center top on the secondary of T1. For ease of explanation assume for a moment that only the ac reference voltage is applied to the phase detector stage. During the positive half cycle of the ac reference voltage, current flows from ground, through R1O, through CR2, and back to its source, the secondary of T1. Diode CRI is reverse-biased for the positive half cycle of ac reference voltage and does not conduct. Voltage is developed across R1O and the junction of R1O, and R12 is above ground potential. During the negative half cycle of the reference voltage, reference diode CR2 is reverse-biased and does not conduct: However, diode CR1 is forward biased and current flows from the transformer centertop through the top half of the winding, through CR1 and through R9 to ground. A voltage is developed across R9 and the junctionofR9andR11 is below ground potential. The positive voltage produced by the rectifying action of CR2, and the negative voltage, produced by the rectifying action of CR1, deviate since CR1 and CR2 have the same

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operational characteristics and resistors R9 and R10 are of equal value. The negative voltage is filtered by RI 1 and C7 and the positive voltage is filtered by R12 and C7. The dc level applied to the grid of relay tube V3 is, therefore, zero volts, when only the reference voltage is applied to circuit. The relay control tube V3 is self biased by its cathode resistor to a conduction level insufficient to energize output relay K1. Since in effect there is no output from the phase detector portion of the phase sensitive null detector when only the ac reference voltage is applied, conduction of V3 does not increase and the output relay remains deenergized. When an ac error voltage is applied in addition to the ac referenced voltage, there is an output from the detector circuit. The polarity of this output is dependent upon the phase relationship between the error and reference signals. Only a positive output from the detector causes the output relay to become energized. When the a-c reference voltage and the error voltage are in phase the output relay becomes energized in the following manner. During the period of the positive half cycle of input signal, a positive half cycle of reference voltage is applied to the centertop of T1, and is applied equally to both diodes. The error voltage, after being amplified by V1 and V2, is applied to primary winding L1 of T1. A negative half cycle of error voltage is induced across the top half of L2 while a positive half cycle of error voltage is induced across the bottom half of L2. The ac reference voltage and the ac error voltage add across the bottom half of L2 while across the top half of L2 they oppose. The result is a positive detector output during the positive half cycle of inputs, since diode CR2 conducts more heavily than CRI and the resultant voltage drop across RIO exceeds that of R9. When the input signal swings negative, the voltages across the top half of L2 again oppose while across the bottom half they add, but they are of such a polarity that CR2 is back biased and does not conduct. There is therefore a positive output from the detector portion of the phase sensitive null detector when the input signals (error and reference) are in phase. After being faltered by R12 and C7 this positive voltage is applied to the grid to relay control tube V3, causing conduction of V3 to increase, and thereby energizing output relay KI. If the error voltage developed across T1 is of greater amplitude than the reference voltage, a negative voltage is developed across R9 during the positive alternation of the error input. However, the positive

voltage developed across R1 O due to the conduction of CR2, is of greater magnitude than the voltage developed across R9 since the reference voltage opposes the error voltage applied to CR1 while it aids the error voltage applied to CR2. The dc level after faltering remains positive and the output relay remains energized. When the error voltage is out-ofphase with the reference voltage, circuit operation is basically the same, except that a negative output is produced by the detector stage and is applied to the grid of V3. The negative output is produced because the two signals applied to the detector stage now add across the top half of L2, and oppose across the bottom hrdf. The magnitude of the current through R9 exceeds that of RIO, and the resultant negative voltage developed across R9 exceeds the positive voltage developed across R1O. The negative voltage applied to the grid of V3 reduces rather than increases conduction of V3 and output relay K1 is not energized. The phase sensitive null detector may also be connected so that the relay becomes energized when the error voltage and the reference voltage are out-of-phase. This may be done simply by reversing either the primary or secondary windings of T1 or by reversing the diodes.

## Failure Analysis.

**No Output.** Failure of the output relay to become energized when the proper conditions are met, i.e., error and references voltages either in or out-of-phase depending upon how the circuit is connected, is considered to be a **no-output** condition. Failure of any of the three stages (the ac amplifier, the phase detector, or the relay control tube) of the phase sensitive null detector could cause a no-output condition to exist. Failure of the power supply would of course disable the circuit and no output also would result. Check the plate supply with a high resistance voltmeter and likewise check the tubes. If the power supply voltage is satisfactory and the tubes are good, a defective circuit component is most likely the cause of no-output. With an error voltage applied to the input and the reference voltage removed check with an oscilloscope for presence of amplified error voltage on the secondary winding L2 of T1. Also observe the waveform present at the grid of V1 to make sure that the no-output condition is not caused by no input. If there is no error voltage present at the secondary of T1 check the primary of TI to determine whether or not T1 is defective. If the ac error voltage is present

in sufficient amplitude at the plate of V2 the ac amplifier stages may be assumed to be good. If the error voltage is not present at the plate of V2 a defect likely exists in the ac amplifier stages. Voltage checks of tube' elements, which should give an indication of the locality of the faulty components may be made, and then with the circuit deenergized, resistance measurements of suspected components may be made to determine the component at fault. Improper grid bias on V1 could be caused by a defect in R1, or in the output circuit of the preceding stage, while improper cathode bias could be caused by a defect in R3 or a shorted Cl. A defect in voltage divider R6, R7 or a shorted or leaky bypass capacitor C4 would rdter both plate and screen voltage on V1. A change or defect in R2 would alter the plate voltage on V1, and a defect in R4, or a short in C2, would affect screen voltage on VI. Keep in mind that improper grid or cathode bias would also alter plate voltage on an amplifier stage. Improper grid bias on ac amplifier stage V2 could be caused by a shorted coupling capacitor C3 or a defective grid resistor R5, while improper cathode bias could be caused by a defect in cathode resistor R8, or a shorted cathode by pass capacitor C6. Lack of plate voltage on V2 could be caused by an open primary winding, L1 of T1. Capacitor C5 should be checked since the ac error signal would be shunted around T1 if C5 shorted. If the ac reference voltage is not present check the source of the ac reference. If the ac amplifier is operating normally, and the reference voltage is applied to the detector stage, a no-output condition could be caused by a defective phase detector stage or relay control stage. The relay control stage may be easily checked by measuring the resistance of R13, the cathode resistor for V3, and by checking the continuity of relay coil K1. Also check the mechanical action of relay K1 since it could become jammed. Diodes CRI and CR2 of the phase detector stage should be checked by disconnecting one lead of each diode and measuring the front to back ratio of each diode. In general the back ratio of most diodes should be greater than 10:1. The other components of the phase detector stage, resistors R9, R1O, R11, and

R12, may be checked by measuring their resistance. Filter capacitor C7 may be checked for proper value with an in-circuit capacitor checker.

Improper Operation. Erratic operation, failure of the output relay to energize, or any type of operation rather than proper operation could be caused by improper plate voltage, a decrease of gain of the ac amplifiers, an unbalance of the phase detector stage, or it could be caused by decreased emission of the relay control tube, or a mechanical defect in output relay K1. Check the power supply voltage and adjust or repair it if necessary. If proper operation is not restored, the tubes may be at fault. If the phase sensitive null detector still does not function properly, the various stages may be checked individually to localize the trouble. The gain of the ac amplifier may be checked .by comparing the amplitude of the error voltage input with the amplitude of the error voltage developed across the primary, L1 of T1 using an oscilloscope. For small error voltages the gain should be around 3000. Be sure to remove the reference voltage when making the previous check since the reference voltage applied to the secondary of T1 could be inductively coupled to the primary of T1 and cause a possible erroneous reading. If the ac amplifier is determined to be defective, the faulty component may be located as explained in the preceding paragraph. The phase detector stage may be checked by removing either V1 or V2 (this disables the ac amplifier) and measuring the voltage on the grid of V3. Any voltage reading other than zero volts indicates an unbalance of the phase detector stage. Check the components as explained in the previous paragraph paying particular attention to the front to back ratio of CR1 compared to CR2 and the resistance of R9 compared to R1O and R11 compared to -R12. Filter capacitor C7 should be checked for proper value with an in-circuit capacitor checker, since a change in value of C7 can adversely affect circuit performance. Relay control stage V3 may be checked by measuring the dc resistance of the output relay winding and by checking the mechanical operation of the relay and also checking the resistance of cathode resistor R13.

# SECTION 15 COUNTERS

## PART 15-1. DIODE

## **POSITIVE OIODE COUNTER (ELECTRON TUBE)**

#### Application,

The positive diode-counter circuit is supplied uniform input pulses, representing units to be counted, and produces a positive output voltage, the average value of which is proportional to the frequency of the applied pulses. Counter circuits are employed in the frequency-indicator circuits of electronic timing or counting devices.

#### Characteristics.

input pulses must be of constant amplitude and of equal time duration; a counter circuit must be preceded by limiting and shaping circuits to ensure uniform amplitude and width of input pulses.

Output-pulse polarity is positive; average dc output voltage level is determined by input pulse-repetition frequency.

## Circuit Analysis.

General. The positive counter circuit is used in frequency-indicator (timing or counting) circuits which depend upon the output pulse amplitude and time duration for accurate indications; therefore, the input pulses applied to the counter circuit must be of constant pulse amplitude and pulse width (time duration). The counter circuit is preceded by limiting and shaping circuits so that the only variable element in the counter-circuit output is the repetition frequency of the input signal, enabling input-frequency variations to be measured accurately. A relationship is thereby established between input frequency and average output voltage; as the input frequency increases the output voltage also increases and, conversely, as the input frequency decreases the output voltage decreases. Thus, the positive counter circuit, in effect, "counts" the number of positivegoing input pulses and produces an average dc output voltage which is proportional to the input repetition frequency.

The output of the positive counter circuit can also be used to produce positive trigger pulses to synchronize the frequency of blocking-oscillator or multivibrator circuits with the input pulse-repetition frequency. The basic positive counter circuit can be easily modified to change it to a step-by-step counter circuit (described later in this section) by substituting a capacitor for the resistor across the output terminals. This modified circuit is referred to as a frequency divider, because the output trigger frequency is usually made a submultiple of the input pulserepetition frequency; the circuit is used in triggergenerator circuits of radar modulators and indicators.

**Circuit Operation.** A basic positive diode counter circuit is shown in the following illustration, together with typical input and output waveforms. Capacitor Cl is the input coupling capacitor and also serves as a dc blocking capacitor; resistor RI is the load resistor across which the output voltage is developed. Electron tubes VI and V2 are indirectly heated diodes; the **filament** (heater) circuit for the diodes is not shown on the schematic,



Basic Positive-Diode Counter Circuit and Waveforms

Initially, capacitor Cl assumes a charge (reference level) which is determined by the dc voltage (if present) of the preceding stage. Once capacitor Cl is charged to the level of the applied dc voltage, the circuit remains in a quiescent condition until an input is **applied**; the output voltage at this time is zero.

Pulses applied to the input of the counter circuit must have constant amplitude and equal time duration, since the counter circuit is intended to produce an output voltage which is proportional to the input pulse-repetition frequency. For the purpose of this discussion, assume that the input waveform shown in the accompanying illustration is applied to the input of the counter circuit.

When the positive-going leading edge of the input waveform occurs, the voltage rises suddenly. The charge on coupling capacitor Cl cannot change instantaneously; therefore, the plate of diode V2 becomes positive with respect to its cathode, and the diode conducts. Current flows through the series circuit consisting of load resistor R1 and diode V2 to charge the capacitor, Cl. Since the charging current flows through the load resistor, RI, a pulse voltage is developed across the resistor and is supplied as the output of the counter circuit.

When the negative-going trailing edge of the input waveform occurs, the voltage drops suddenly. Once again the charge on coupling capacitor Cl cannot change instantaneously; therefore, a negative voltage appears across diode VI. (This negative voltage is equal to the charge previously obtained by capacitor Cl from the conduction of diode V2.) Since the cathode of diode VI is now negative with respect to its plate, the diode conducts and discharges capacitor Cl to its initial value. The circuit then remains in a quiescent condition until another pulse is applied to the input.

If it were not for the fact that diode V1 discharges the capacitor each time a pulse is applied to the input, capacitor Cl would soon charge to the peak value of the input waveform as consecutive positive pulses were applied. As a result, no output would be obtained because the circuit would be rendered inoperative.

The charge time of capacitor Cl is determined by the value of resistor R1 and the low internal resistance of diode V2 when conducting. The discharge time of capacitor Cl is determined primarily by the low internal resistance of diode VI when conducting. Thus, the time constant of the discharge path is always less than that of the charge path; therefore, within certain limits imposed by the R-C time constant and the applied pulse-repetition frequencies, the circuit is always in condition to accept the next positive-going input pulse.

From the discussion given in the previous paragraphs, it is evident that there is an average current flowing through resistor RI whenever pulses are applied to the input of the circuit; also, a pulse voltage is produced across resistor R1 for each input pulse applied to the circuit. Thus, an average voltage is produced across resistor R1 which varies in accordance with the repetition rate of the input pulses; the average voltage increases as the input frequency increases, and vice versa. Since the output voltage level changes in proportion to changes in the repetition frequency of the applied input pulses, the output voltage can be fed to a succeeding stage which controls a suitable indicating device. The indicating device, in turn, can be calibrated in units of time, frequency, revolutions per minute, etc., based upon the relationship of output voltage to input frequency.

## Failure Analysis.

**General.** The positive diode counter circuit is a relatively simple circuit consisting of only four components-diodes VI and .V2, capacitor Cl, and resistor R1. For this reason, failure analysis is somewhat limited.

initially, the input signal to the counter circuit should be checked to determine whether it is present and has the correct amplitude and pulse width.

A visual check should be made to determine whether the filaments (heaters) of diodes V1 and V2 are lit and whether the filament circuit is complete. The diodes should be checked in a tube tester. If diode V1 is open and fails to conduct, capacitor Cl will charge to the peak value of the applied input pulse and, once the capacitor is fully charged, no output will be developed across the load resistor, R1; if diode V1 shorts, no output will be developed across the load resistor. If diode V2 is open or fails to conduct, no output will be developed across the load resistor; if diode V2 shorts, a positive output pulse will be developed across the load resistor, together with a small negative output pulse which will coincide with the negative-going trailing edge of the input waveform.

The counter circuit is normally preceded by  $\checkmark$  limiter-shaper stages; therefore, in some cases a dc

potential exists at the input to the circuit. If coupling capacitor Cl should become leaky (or shorted), a voltage-divider action will occur. For this condition, it is likely that diode V2 will conduct at all times, and a dc potential which is above normal will be developed across resistor RI. Capacitor Cl can be checked with a suitable capacitance analyzer; resistor R1 can be measured with an ohmmeter to determine its resistance.

## POSITIVE DIOOE COUNTER (SEMICONDUCTOR)

#### Application

The positive diode-counter circuit is used to count pulses and provide frequency indication. It is mainly used in electronic timing and counting devices, but it is sometimes employed as a frequency divider and in elementary types of computers.

#### Characteristics.

Requires an input pulse of constant amplitude and time duration.

Provides a positive output voltage with an average dc level that is proportional to the **input** pulse repetition frequency.

May be used to synchronize a blocking oscillator at a submultiple of original frequency.

Requires an output circuit to provide a directreading output indication.

Requires that limiting and shaping circuits precede it.

## Circuit Analysis.

General. The positive diode-counter circuit is used in timing or counting circuits which depend upon a proportional relationship between the output voltage and the number of input pulses. It may indicate frequency, it may count the rpm of a shaft or other device, or it may even register the number of operations. (This circuit is not the same as the binary or decade counter which is used in computers.) The counter establishes a direct relationship between the input frequency and the average d-c output voltage. As the input frequency increases the output voltage also increases; conversely, as the input frequency decreases the output voltage decreases. In effect, the positive diode-counter counts the number of positive input pulses by producing an average d-c output voltage which is proportional to the repetition frequency of the input signal. For accurate counting, the

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pulse repetition frequency must be the only variable parameter in the input signal. Therefore, careful shaping and limiting of the input signal is essential to ensure that the pulses are of uniform width, or time duration, and that the amplitude is constant. When properly faltered and smoothed, the dc output voltage of the counter may be used to operate a directreading indicator. With slight modifications, the circuit can also be used to control a blocking oscillator and cause it to provide a trigger output which is synchronized at a submultiple of the original repetition frequency. (This modification is discussed under the Step-by-Step Counter circuit, which appears later in this section.)

**Circuit Operation.** The basic positive diodecounter circuit is shown in the following illustration. Capacitor Cl is the input coupling and **d**-c blocking capacitor. CR1 and CR2 are semiconductor diodes, and resistor RI is the load resistor, across which the output voltage is developed. For the purpose of circuit discussion, it is assumed that the input pulses are of constant amplitude and time duration, and that only the pulse repetition frequency changes.



## **Positive Diode Counter**

Once capacitor Cl is charged, it assumes a reference level as determined by the dc voltage applied to the preceding stage, and the circuit remains in a quiescent condition until an input signal is applied. Prior to the application of the input pulse, the output voltage is zero.

As shown in the following illustration, at time t. the positive-going input pulse is applied to Cl and causes the anode of CR2 to go positive. As a result, CR2 conducts and current i flows through RI and CR2 to charge Cl. Current i develops an output voltage (e,) across R1 as shown in the illustration.

The initial heavy flow of current produces a large voltage across R1, which tapers off exponentially as Cl charges. The charge on Cl is determined by the time constant of load resistor RI and the forward diode resistance, in series, times the capacitance of  $C_{i}$ . For ease of explanation, it is assumed that Cl is charged to the peak value before time  $t_i$ .

At time  $t_1$  the input signal reverses polarity and becomes negative-going. Although the charge on Cl cannot change instantly, the applied negative voltage is equal to or greater than the charge on Cl so that the anode of CR2 is made negative, and conduction ceases. When CR2 stops conducting, output pulse  $e_0$ is at zero, and Cl quickly discharges through CR1, since its cathode is now negative with respect to ground (anode is grounded). Between times  $t_1$  and  $t_2$ the input pulse is again at zero level, and CR2 remains in a non-conducting state. Since the very short time constant offered by the forward resistance of CR1 and Cl is much less than the long time constant offered by CR2 and R1 during the conduction period, Cl is always completely discharged between pulses. Thus, for each input pulse there is an exact amount of charge deposited in Cl. For each charge of Cl an identical output pulse is produced by the flow of i through R1. Since this current flow always occurs in the direction indicated by the solid arrow, the dc output voltage is positively polarized.



At time  $t_2$  the input signal again goes positive, and the cycle repeats. The time duration between pulses is the interval represented by the period between  $t_1$  and  $t_2$  or between  $t_3$  and  $t_4$ . If the input pulse frequency is reduced, these time periods become longer. On the other hand, if the frequency is increased, these time L

intervals become shorter. With shorter periods, more pulses occur in a given time and a higher average (de) output voltage is produced; with longer periods, fewer pulses occur and a lower output voltage is produced. Thus, the dc output is directly proportional to the repetition frequency of the input-pulses. If the current and voltage are sufficiently large, a direct-reading meter can be used to indicate the count; if they are not large enough to actuate a meter directly, a dc amplifier may be added. In the latter case, a Pi-type smoothing falter is inserted at the output of RI, to absorb the instantaneous pulse variations and produce a smooth direct current for amplification.

Consider now some of the limits imposed on circuit operation. Since the semiconductor diode has a finite reverse resistance, there is a flow of reverse current during the periods when the diode is supposedly in a nonconducting condition. Although this reverse flow is small at normal temperatures (on the order of microampere), it increases as the temperature rises. Therefore, at high temperatures and high repetition rates, the average output voltage will tend to decrease because of the effects of diode CR2. Similarly, diode CR1 will tend to shunt some of the input signal to ground. Thus, the net over-all effect with increasing frequency is a progressive decrease in the linearity (that is, a reduction in the proportionality of input frequency to output voltage), and at very high repetition rates the circuit may become inoperative. Fundamentally this is a design problem which can be minimized by proper choice of components; it is mentioned here merely to indicate why semiconductor circuits sometimes do not perform as well as their electron tube counterparts.

## Failure Analysis.

**No Output.** A **no-output** condition maybe caused by an open-circuited coupling capacitor, by defective diode CR2, or by a short-circuited condition (defective diode CR1, grounded CR2, or shorted load resistor RI). This condition can be easily resolved by a resistance check. Observing the proper polarity, check the diodes for a high reverse resistance and a low forward resistance. As a general rule, the reverse resistance should be 50K or greater, and the forward resistance should not be more than 10 ohms (these values vary with different types of diodes). Also, observe the input signal with an oscilloscope to make certain that it is present; the point at which the signal disappears will generally locate the defective component.

Low Output. If CR2 develops a high forward resistance, the output voltage will be reduced. If coupling capacitor C becomes leaky, either a negative or a positive bias will be placed on CR2, depending upon the polarity of the previous stage collector or plate voltage. A negative bias on CR2 will prevent it from conducting, and will also act as a forward bias for CR1, causing it to conduct continually. Under these conditions, C<sub>1</sub>will constantly be discharging and the pulse will be reduced in amplitude (depending on the amount of leakage). Heavy leakage may result in no output at all, but it is more likely that the leakage will be light and only reduce the output. To check Cl for leakage, connect a dc voltmeter between the output terminal of Cl and ground. If Cl is leaky, a constant negative or positive voltage will be present.

**High Output.** (For a positive leakage voltage through  $C_i$ , CR2 will conduct continually, and a higher-than-normal voltage will most probably be indicated.) If CR1 develops a high forward resistance, Cl will not be completely discharged at the termination of the input pulse. As a result, the output voltage will rise to a value equal to the dc potential applied to Cl and remain constant regardless of pulse frequency changes.

# NEGATIVE DIODE COUNTER (ELECTRON TUBE)

#### Application.

The negative diode counter supplies a negative voltage output directly proportional to the repetition rate of incoming pulses. The negative diode counter is commonly employed in radar timing circuitry.

#### Characteristics.

Input pulses must have uniform width and amplitude; only repetition rate may vary.

Usually preceded by limiting and shaping circuitry.

Develops a negative voltage output directly proportional to the repetition rate of incoming pulses.

Always returns to quiescent state between pulses.

## COUNTERS

## Circuit Analysis.

**General.** The negative diode counter circuit is used as a frequency indicating device in radar timing circuitry. With some modification, the diode counter may also be used as an f-m detector, a frequency divider or, when used in conjunction with a blocking oscillator or multivibrator, as a synchronizer.

Briefly, the negative diode counter furnishes a negative voltage output directly proportional to the repetition rate of the incoming pulses, provided pulse width and amplitude does not vary. If the repetition rate of the pulses increases, current flow through the load resistor also increases (occurs more times per second) and consequently the total voltage developed also increases.

Basically the diode counter utilizes the characteristics of a capacitor and diode to perform its function. The fact that a capacitor takes a finite time to charge and that a diode only conducts when its cathode is negative with respect to its plate, allows a voltage to be developed across the load resistor which is proportional to the repetition rate.

**Circuit Operation. A basic** negative diode counter, along with input and output waveforms, is shown in the following schematic diagram.



**Basic Negative Diode Counter** 

Capacitor Cl is the input coupling capacitor and RI is the load resistor. Diode VI is in series with the load resistor and it can easily be seen that as long as V1 conducts there will be an ouput, conversely, diode V2 is connected in parallel with the load, and as long as V2 conducts there will not be an output. Thus, V1

acts as an off-on switch, while V2 operates as a discharging diode. Since the circuit is to function as a frequency indicating device, it is necessary that pulse amplitude and duration remains the same for each pulse, with only the time between pulses (or repetition rate) being allowed to change. Hence, the negative diode counter is usually preceded by limiting and shaping circuits to ensure that each pulse is uniform.

As the negative leading edge of the initial incoming pulse appears at the input, capacitor Cl begins to charge; however, it is known from basic theory that a capacitor is unable to charge instantaneously. Consequently, at the first instant the signal is applied, the peak negative voltage appears on the cathode of V1, causing the tube to conduct. As the tube conducts, current flows through the load resistor, R1 to ground, developing a negative output voltage. As Cl charges, the voltage applied to the cathode of VI becomes less negative and tube condition decreases, causing less voltage to be developed across load resistor R1, forming the curved portion of the output waveform as the capacitor charges.

As the positive going trailing edge of the pulse is applied to the input, Cl again cannot instantly change in potential. Consequently, the cathode of V1 instantaneously becomes positive with respect to its plate (because of the charge on Cl) and current flow through the diode and series load resistor ceases, instantly dropping the output voltage level to zero. Simultaneously; since V2 plate is now positive, V2 conducts discharging the capacitor. The circuit is returned to the initial quiescent condition with a discharged capacitor awaiting the next input pulse.

It is essential to remember that the circuit is returned to a quiescent condition each time the incoming input pulse returns to zero level, regardless of the pulse repetition rate. Referring to the schematic diagram it can easily be seen that charge current, (current flowing in the circuit whale Cl is charging) flows through the combined resistance of V1 and R1, while discharge current (current flowing in the circuit while Cl is discharging) flows only through the conducting resistance of V2. For example, if we assign the load resistor and the conducting resistance of the identical diodes a resistance of 10 thousand ohms and 100 ohms, respectively, it may easily be seen that charge current flows through 10,100 ohms, while discharge current flows through a mere 100 ohms. Hence, the time constant of the charging cycle is very large with

respect to that of the discharging cycle (approximately 100 to 1), and any voltage stored in Cl during change is immediately discharged through V2, returning the circuit to its quiescent state.

From the preceding discussion it is evident that the voltage across the output varies in direct proportion to the input pulse repetition rate. Hence if the repetition rate (frequency) if the incoming pulses increases, the voltage across RI also increases. In order for the circuit to function as a frequency counter, some method must be employed to utilize this frequency – voltage variation to operate an indicator. The following schematic diagram represents one simple circuit which may be used to perform this function. In this circuit the basic counter is fed into a low pass smoothing falter, which controls an electron tube with a cathode current meter calibrated is units of frequency.



#### **Circuit Application**

The negative output voltage developed across counter load resistor R1 is applied to the grid of V3 through a pi-falter network consisting of C2, R2 and C3. In this application the purpose of the falter is to smooth out any rapid increase or decrease in output voltage thus providing continuously smooth operation.

The faltered negative counter voltage is applied as bias to the grid of V3 and varies the plate current

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which flows through a meter in the cathode of V3. The meter is linearly calibrated on the front panel to indicate changes in current as a linear frequency change. For example, assume the circuit is operating and a specific frequency is indicated on the front panel meter. As the repetition rate of the pulses increases, the average voltage across the load resistor also increases and a larger bias is applied to V3. Plate current through V3 decreases, and as current through the meter decreases, a higher frequency indication is evident on the calibrated meter scale on the front panel of the equipment. If the applied frequency were to decrease, the opposite effect would occur and a greater plate current flow would produce a lower frequency indication on the meter.

## Failure Analysis.

**No Output.** Because the basic circuit only incorporates four components and operation is relatively simple, detailed trouble analysis is not necessary. If trouble is experienced with the circuit use an oscilloscope to check the input pulse train for uniform width and amplitude. Also check both diodes. If the trouble persists, check the dc resistance of R1 with an ohmmeter. Also check the coupling capacitor Cl with an in-circuit capacitor checker.

Weak Output. If a weak (or incorrect) output condition exists, check the input pulse train for uniform width and amplitude using an oscilloscope. Also check both diodes. Check the dc resistance of R1using an ohmmeter and also check Cl with an incircuit capacitor checker.

# NEGATIVE DIODE COUNTER (SEMICON-DUCTOR)

#### Application.

The negative diode-counter circuit is used to count pulses and provide frequency indication. It is mainly used in electronic timing and counting devices, but it is sometimes employed as a frequency divider and in elementary types of computers.

#### Characteristics.

Requires an input pulse of constant amplitude and time duration.

Provides a negative output voltage with an average dc level that is proportional to the input pulse repetition frequency. May be used to synchronize a blocking oscillator at a submultiple of original frequency.

Requires an output circuit to provide a direct. reading output indication.

Requires that limiting and shaping circuits precede it.

# Circuit Analysis.

General. The negative diode-counter circuit is used in timing or counting circuits which depend upon a proportional relationship between the output voltage and the number of input pulses. It may indicate frequency, it may count the rpm of a shaft or other device, or it may even register the number of operations. The diode counter establishes a direct relationship between the input frequency and the average dc output voltage. As the input frequency increases the output voltage also increases; conversely, as the input frequency decreases; the output voltage also decreases. In effect, the negative diodecounter counts the number of negative input pulses by producing an average dc output voltage which is proportional to the repetition frequency of the input signal. For accurate counting, the pulse repetition frequency must be the only variable in the input signal. Therefore, careful shaping and limiting of the input signal is essential to ensure that the pulses are of uniform width, or time duration, and that the amplitude is constant. When properly faltered and smoothed, the dc output voltage of the counter may be used to operate a direct-reading indicator. With slight modifications, the circuit can also be used to control a blocking oscillator and cause it to provide a trigger output which is synchronized at a submultiple of the original repetition frequency. (This modification is discussed under the Step-by-Step Counter circuit, which appears later in this section.)

**Circuit Operetion.** The basic negative diodecounter is shown in the following illustration. Capacitor C 1 is the input coupling and dc blocking capacitor.



#### Negative Diode Counter

CR1 and CR2 are semiconductor diodes, and resistor R1 is the load resistor, across which the output voltage is developed. For the purpose of circuit discussion, it is assumed that the input pulses are of constant amplitude and time duration, and that only the pulse repetition frequency changes.

Once capacitor Cl is charged, it assumes a reference level as determined by the dc voltage applied to the preceding stage, and the circuit remains in a quiescent condition until an input signal is applied. Prior to the application of the input pulse, the output voltage is zero.

As shown in the following illustration, at time t. the positive-going input pulse is applied to Cl and causes the anode of CRI to go positive. As a result, -CR1 conducts and charges Cl.

capacitor voltage and the applied voltage now aid each other, and they produce a current flow through CR2, down through RI, to ground, the result being as

illustrated in the diagram. As Cl begins charging through RI, the voltage across RI, and hence the output voltage, begins to decrease towards zero at an RC rate, and at some time between  $t_1$  and  $t_2$ , the capacitor is charged to the new voltage, producing

At time t<sub>2</sub> the input signal again goes positive, and the cycle repeats. The time duration between pulses is

the interval represented by the period between  $t_1$  and  $t_3$ , or between  $t_3$  and  $t_4$ . If the input pulse frequency

is reduced, these time periods become longer. On the other hand, if the frequency is increased, these time intervals become shorter. With shorter periods, more pulses occur in a given time and a higher average (de) output voltage is produced; with longer periods, fewer pulses occur and a lower output voltage is produced. Thus, the dc output is directly proportional to the repetition frequency of the input pulses. If the

current and voltage are sufficiently large, a directreading meter can be used to indicate the count; if they are not large enough to actuate a meter directly,

zero volts at the output.



#### **Circuit Waveforms**

Cl charges very rapidly because of its short time constant with CR1, but there is no output at this time because there is no current flow through R1. At time  $t_1$ , the input amplitude suddenly drops from maximum positive to maximum negative. The capacitor cannot discharge through CR1, because the anode of the diode is negative with respect to its cathode. The anode of CR2, however, is now positive with respect to its cathode and begins to conduct. The

a dc amplifier may be added. In the latter case, a Pi-type smoothing falter is inserted at the output of Rl, to absorb the instantaneous pulse variations and produce a smooth direct current for amplification.

> Consider now some of the limits imposed on circuit operation. Since the semiconductor diode has a finite reverse resistance, there is a flow of reverse current during the periods when the diode is supposedly in a nonconducting condition. Although this reverse flow is small at normal temperatures (on the order of microampere), it increases as the temperature rises. Therefore, at high temperatures and high repetition rates, the average output voltage will tend to decrease because of the effects of diode CR2. Similarly, diode CRI will tend to shunt some of the input signal to ground. Thus, the net over-all effect with increasing frequency is a progressive decrease in the linearity (that is, a reduction in the proportionality of input frequency to output voltage), and at very high repetition rates the circuit may become inoperative. Fundamentally this is a design problem which can be minimized by proper choice of components; it is mentioned here merely to indicate why semiconductor circuits sometimes do not perform as well as their electron tube counterparts.

## Failure Analysis.

**No Output.** A no-output condition maybe caused by an open coupling capacitor, by defective diode CR2, or by a short-circuited condition (defective diode CR1, grounded CR2, or shorted load resistor Rl). These conditions can be easily resolved by a resistance check. Observe the proper polarity, and check the diodes for a high reverse resistance and a low forward resistance. As a general rule, the reverse resistance should be 50K or greater, and the forward resistance should be 50K or greater, and the forward resistance should not be more than 10 ohms (these values vary with different types of diodes). Also, observe the input signal with an oscilloscope to make certain that it is present; the point at which the signal disappears will generally locate the defective component.

Low Output. If CR2 develops a high forward resistance, the output voltage will be reduced. If coupling capacitor Cl becomes leaky, either a negative or a positive bias will be placed on CR2, depending upon the polarity of the previous stage collector or plate voltage. A positive bias on CR2 will prevent it from conducting, and will also act as a forward bias for CR1, causing it to conduct continually. Under these conditions, Cl will constantly be discharging and the pulse will be reduced in amplitude (depending on the amount of leakage). Heavy leakage may result in no output at all, but it is more likely that the leakage will be light and only reduce the output. To check Cl for leakage, connect a dc voltmeter between the output terminal of Cl and ground. If Cl is leaky, a constant negative or positive voltage will be present.

**High Output.** (For a negative leakage voltage through Cl, CR2 will conduct continually, and a higher-than-normal voltage will most probably be indicated.) **If** CR1 develops a high forward resistance, Cl will not be completely discharged at the termination of the input pulse. As a result, the output voltage will rise to a value equal to the dc potential applied to Cl and remain constant regardless of pulse frequency changes.

## STEP-BY-STEP COUNTER (ELECTRON TUBE)

## Application.

The step-by-step counter is used as a voltage divider in electronic equipment when it is necessary

to provide a stepped voltage output to a relaxation oscillator or any other device requiring a stepped voltage trigger.

#### Characteristics.

Provides a stepped voltage output.

As the number of input pulses increases for one pulse of output, the counting accuracy decreases.

Utilizes two diodes.

One step out occurs for each cycle of input.

## Circuit Analysis.

**General.** The step-by-step counter (commonly referred to as simply a step counter) provides an output which increases exponentially in such a way that the output increases by a one step increment for each cycle of input. At a predetermined level, the output voltage reaches a point which causes some circuit, such as a relaxation oscillator, to be triggered.

**Circuit Operation.** A schematic diagram of a step counter is illustrated in the following figure.



#### **Basic Step-by-Step Counter Circuit**

With no signal applied at the input, there is no output. As the input signrd is applied, and increases in a positive direction, the plate of V2 becomes more positive than its cathode, and the tube conducts, When V2 conducts, capacitors Cl and C2 begin

## **ELECTRONIC CIRCUITS**

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charging. The action of the counter can be best understood by referring to the following figure. Since C2 is larger than Cl (for the sake of explanation, we will assume it to be ten times as large, and that the peak voltage of the input is 100 volts). Cl assumes nine tenths of the input voltage and C2 assumes only one tenth, or in this example, 10 volts. At time t, the input drops to a negative value, and V2 is driven into cutoff. At the same time, the cathode of V1 becomes more negative than its plate, and conducts, discharging Cl. The charge on C2 remains, however, because it has no discharge path. Thus, there is a dc voltage at the output which is equal to one tenth of the input. At time t<sub>2</sub>, the input again increases positively, but this time V2 cannot conduct until the input becomes greater than 10 volts, the charge on C2. At this level, V2 conducts and C2 again charges to one tenth of the total available voltage. The total available voltage at this time, however, is no longer 100 volts, but 100 volts minus the 10 volt charge on C2. Thus, the first cycle of input produced a ten volt charge on C2, but the second cycle added only an additional 9 volts, which is one tenth the quantity of 100 volts minus the 10 volt charge on C2. By the same token, the third cycle adds only one tenth of 81 volts, which results from 100 volts minus the 19 volt charge on C2. Each additional cycle provides an exponential increase in the same manner. It is for this reason that the accuracy decreases as the ratio increases, because as the ratio becomes too great, the higher steps become almost indiscernible.



Waveform of Step Voltage

When the counter is used to trigger a relaxation oscillator. the oscillator bias is adjusted to cause triggering at a specific step. When the relaxation oscillator draws grid current, it discharges C2 and the cycle repeats. The step counter therefore becomes a frequency divider, supplying one output trigger for a number of input triggers,

As previously mentioned counting stability is dependent upon the exponential charging rate of capacitor C2. When it is desired to count by a large number, for example, 24, a 6:1 counter and a 4:1 counter connected in cascade may be used. A more stable method of counting 24 would be to use a 2:1, a 3:1, and a 4:1 counter in cascade. Most step counters operate on ratios of 5:1 or less.

## Failure Analysis.

**No Output**, A shorted VI, a non-conducting V2, an open or shorted C2, or a shorted Cl may cause a **no-output** condition to exist. Check both capacitors with an in-circuit capacitor checker.

Inaccurate **Output Ratio.** A low emission or shorted tube V1 or V2, or a leaky Cl or C2, can produce an inaccurate count. Check the tubes and if an accurate count still exists, check both capacitors with an in-circuit-capacitor checker.

## STEP-BY-STEP COUNTER (SEMICONDUCTOR)

## Application.

**The** step-by-step counter is used as a voltage divider in transistorized equipment when it is necessary to provide a stepped voltage output to a relaxation oscillator or any other device requiring a stepped voltage trigger.

## Characteristics.

Provides a stepped voltage output which increases exponentially.

As the number of input pulses increases for one output pulse, the counting accuracy decreases.

Utilizes two semiconductor diodes.

One step of output voltage is obtained for each cycle of input voltage.

## Circuit Analysis.

**General.** The step-by-step counter (commonly referred to as simply a step-counter) provides an output which increases exponentially in such a way that the output increases by one-step increments for each cycle of input. At a predetermined level, the output voltage reaches a firing point which causes some circuit, such as a relaxation oscillator, to be triggered.

**Circuit Operation. A** schematic diagram of a stepcounter is shown in the following illustration.



Basic Step-Counter Circuit

With no signal applied to the input, there is no output. As the input signal is applied, and increases in a positive direction, the anode of CR2 becomes more positive than its cathode, and the diode conducts. When CR2 conducts, capacitors Cl and C2 begin charging. The action of the counter can be best understood by referring to the following figure. Since C2 is larger than Cl (for the sake of explanation, we will assume it to be ten times as large, and the peak voltage of the input is 100 volts), Cl assumed nine tenths of the input voltage while C2 assumes only one tenth, or in this example, 10 volts. At time t<sub>2</sub>, the input drops to a negative value, and CR2 is driven into cut-off. At the same time, the cathode of CR1 becomes more negative than its anode, and conducts, discharging Cl. The charge on C2 remains, however, because it has no discharge path. Thus, there is a dc voltage at the output which is equal to one tenth of the input. At time t<sub>2</sub>, the input again increases positively, but this time CR2 cannot conduct until the input becomes greater than 10 volts, the charge on C2. At this level, CR2 conducts and C2 again charges to one tenth of the total available voltage. The total available voltage at this time, however, is no longer 100 volts, but 100 volts minus the 10 volt charge on C2. Thus, the first cycle of input produced a ten volt charge on C2, but the second cycle added only an additional 9 volts, which is one tenth the quantity of 100 volts minus the 10 volt charge on C2. By the same token, the third cycle adds only one tenth of 81 volts. which results from 100 volts minus the 19 volt

charge on C2. Each additional cycle provides an exponential increase in the same manner. It is for this reason that the accuracy decreases as the ratio increases, because as the ratio becomes too great, the higher steps become almost indiscernible.



Waveform of Step Voltage

When the counter is used to trigger a relaxation oscillator, the oscillator bias is adjusted to cause triggering at a specific step. When the relaxation oscillator draws grid current, it discharges C2 and the cycle repeats. The **step-counter**, therefore, becomes a frequency divider, supplying one output trigger for a number of input triggers.

As previously mentioned, counting stability is dependent upon the exponential charging rate of capacitor C2. When it is desired to count by a large number, for example, 24, a 6:1 counter and a 4:1 counter connected in cascade may be used. A more stable method of counting 24 would be to use a 2:1, a 3:1 and a 4:1 counter in cascade. Most step counters operate on ratios of 5: 1 or less.

In actual theory, the reverse resistance of the diode will allow a portion of the charge of C2 to leak off. This leakage, however, in a practical circuit, will be negligible, because the diodes which are selected for use are types which will have a very high reverse resistance, so that the ratio between the charge time and the discharge time will be very large.

## Failure Analysis.

**No Output.** A shorted **CR1**, a non-conducting (open) CR2, an open or shorted output capacitor C2, or a shorted coupling capacitor C1, may cause a nooutput condition to exist. Check both capacitors with an in-circuit capacitor checker. Check the diodes with an ohmmeter, being sure to observe the proper polarities, since an erroneous indication may otherwise be obtained. For the special case where the diode is not completely shorted, but reads a very low reverse resistance of, say 2000 -obms or less, the diode may be considered defective. In good condition, the diode reverse resistance should be 50,000 -ohms or better, with a forward resistance of about 10 ohms (these values will vary from type to type).

**Inaccurate Output Ratio.** A low conducting, or a complete or partial short of CRI or CR2, or a leaky Cl or C2, can produce an inaccurate count. Check both capacitors with an in-circuit capacitor checker. If an inaccurate count still exists, check both diodes with an ohmmeter, being sure to observe the proper polarities, since an erroneous indication may otherwise be obtained. For the special case where the diode is not completely shorted, but reads a very low reverse resistance of, say 2000-ohms or less, the diode may be considered defective.

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# SECTION 16 LOGIC CIRCUITS

## PART 16-0. INTRODUCTION

# LOGIC POLARITY

#### General.

Computer logic is expressed by a form of twovalue logic which is easily adaptable to the binary number system. Thus computer elements (circuits) have only two states, such as: the conduction or nonconduction of a circuit, the presence or absence of a hole on a card or paper, or the presence or absence of a magnetic field. The use of two-value logic also means that, basically, these states may assume a value of either O or 1. (While true or false could also be used, the numeric values lend themselves readily to computations and algebraic manipulations.)

In any electrical circuit, any two distinct voltages or currents can be used to represent the two logic states of O and 1. For example, a negative voltage could indicate O and a positive voltage could indicate 1, or vise versa. Likewise, current flow into the circuit could indicate O, and current flow out of the circuit could indicate 1. Similar results could be obtained with amplitude control, using small and large voltages or currents. Pulses could also be used in a like fashion, with a negative pulse indicating O and a positive pulse indicating 1; or O could be indicated by the absence of a pulse, in which case the presence of a pulse could signify 1. Many combinations of logic expressions are possible; they can also be used interchangeably, since each logic element (circuit) or operating entity can actually function independently as long as the desired result is achieved. Mixed logic systems are not used in large computers, however, since this practice would cause expensive circuit complications. Most presentday logic systems utilize polarity to define the circuit state, since positive and negative voltages are easily obtained and manipulated, regardless of whether the actual logic element (circuit) employs relays, switches, diodes, or transistors. Logic circuits can be divided into two generrd classes, according to polarity, namely positive and negative logic. As employed on logic diagrams, a signal may assume either the "active (or true)" state (logic 1), or the "inactive (or flase)" state (logic O).

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The electrical signal levels used and a statement concerning whether positive or negative logic applies are **usually** specified explicitly on the individual logic diagrams by the manufacturer of the logic designer.

In practice, many variations of logic polarity are employed: for example, from a high-positive to a low-positive voltage, or from positive to ground; from a high-negative to a low-negative voltage, or from negative to ground; and mixed polarity, from a high positive to a negative (below ground) potential, and vice versa. A brief discussion of the two general classes of polarity is presented in the following paragraphs. Each of the logic circuit discussions also given in this section will be based upon the form of logic polarity best suited for simple explanation of the circuit action.

# Positive Logic.

Positive logic polarity is defined as follows: when the **logic** 1 state has relatively more positive electrical level than the logic O state, and the circuit is activated (operated) by the logic 1 signal, the logic polarity is considered to be positive. The following typical examples illustrate the manner in which positive logic may be employed.

Example 1:	Logic $1 = +10$ volts
	Logic $o = o$ volts
Example 2:	Logic $1 = o$ volts
	Logic $\rho = -\log volts$

In both examples the logic 1 state is always more positive than the logic O state, even though in example 2 the logic O state is negative. The previous statements and definitions are particularly appropriate for dc switching circuits, but also apply to ac circuits as well. For example, a positive pulse can be used to simulate a positive voltage, and a negative pulse can be used to simulate a negative voltage. However, such complexity is unnecessary, since the absence of a pulse can signify the logic O state and the original **definition** of positive polarity will still apply. That is, the logic 1 state is more positive than the no signal (or logic O) state.

As normally used, positive logic is more adaptable to NPN type transistors because of the NPN polarity requirements. Since a positive collector voltage is

required to reverse-bias the NPN transistor, operation of the transistor produces either a low or a high positive output voltage. Thus by using direct coupling, a fully transistm-ized, positively polarized 'dc system can be developed, thereby eliminating interstage coupling capacitors and any possible waveform distortion effects. The functioning of direct-coupled transistor logic (DCTL) circuits is discussed later in this section. The use of positive logic, however, is not restricted to NPN transistors, since PNP transistors can be used in ac systems using the common-emitter (CE) configuration, which inverts the input polarity in the output circuit. The use of NPN transistors merely makes the design of dc positive logic circuits easier and simpler, so that normally positive logic is associated with NPN transistors, while negative logic is associated with PNP transistors. At present, however, it is unimportant which type of logic polarity (positive or negative) is used, since logic components and circuits are available for all types. In fact, by using a form of mnemonic (symbolic) notation, such as H for the high or active state (1), and L for the low or inactive state (0), logic design may be completed and circuitry devised without concern for the polarity or levels used. Once the logic design is completed, standard circuits of the proper type and polarity for the components and level to be used are selected, and the unit is constructed.

# Negative Logic.

Negative logic polarity is defined as follows: when the logic 1 state has relatively more negative electrical level than the logic O state, and the circuit is activated (operated] by the logic 1 signal, the logic polarity is considered to be negative. The following typical examples illustrate the manner in which negative logic can be employed.

Example 1:	Logic $1 = 0$ volts
	Logic $o = +10$ volts
Example 2:	Logic 1 <sup>=</sup> -lo volts
	Logic o o volts

In both examples the logic 1 state is always more negative than the logic O state, even though in example 1 both states are in the positive region. While the above definitions of logic polarity are particularly applicable for dc switching circuits, they also apply to ac circuits as well. For example, a negative pulse can be used to simulate a negative voltage, and a positive pulse can be used to simulate a positive voltage. Such complexity is unnecessary, however, since the absence of a pulse can be assumed to indicate the logic O state. Thus only a negative pulse is necessary, and the above **definitions** will still apply.

As normally used, negative logic is more adaptable to PNP type transistors because of the PNP polarity requirements. Since a negative collector voltage is required to reverse-bias the PNP transistor, operation of the transistor produces either a low or a high negative output voltage. By using direct coupling, a completely negatively polarized dc system can be developed, and interstage coupling capacitors can be eliminated. Thus, besides the saving of the cost of a component, waveform distortion due to phase shift through the coupling capacitor can be minimized. Operation may also be speeded up, since it is no longer necessary to wait for the charge and discharge of the capacitor. Direct-coupled transistor logic (DCTL) circuits are discussed later in this section. Negative logic is not limited to PNP transistors, since the common emitter configuration (in an ac coupled circuit) can invert the polarity of the input signal and provide a negative output from an NPN transistor. The use of PNP transistors merely makes the design of dc negative logic circuits easier and simpler, so that negative logic is normally associated with PNP transistors, while positive logic is associated with NPN transistors. Since logic circuits and components are available for all types of polarity, there is no particular reason why negative logic should be used in preference to positive logic. In fact, for design reasons some special computers use both (mixed) positive and negative polarity. The usual practice is to design the logic without regard to polarity or levels. Once designed, the proper type of polarity and levels for the standard logic circuit and components to be used is selected, and the unit is constructed.

#### GATING CIRCUITS

#### General.

A gating circuit is a switch with two or more inputs that allows information to flow when certain input signals are present. The input signals may be in the form of numbers, control instructions, and timing pulses. Gating circuits are used to perform AND, OR, INHIBIT, and NOR operations of logic. *AND-gate* circuits produce an output ordy when signals are

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present at all inputs. When signals are not present at all inputs, no output is obtained from an AND-gate circuit. **OR-gate** circuits produce an output when one or more input signals are present. When signals are not present at any of the OR-gate circuit inputs, no output signal is obtained. **INHIBIT-gate** circuits allow a signal to pass only when certain signals are present and other specific signals are not present at the inputs. Thus, an INHIBIT-gate is the same as an AND-gate with one or more inputs inverted. **NORgate** circuits pass a signal only when no signals are present at the inputs. The NOR operation can therefore be obtained by using an OR-gate circuit with an inverted output.

The polarity and level of AND-gate and OR-gate output signals are generally the same as the polarity and level of the input signals. For example, when a negative 10-volt output signal is to be obtained from an AND gate or OR gate, negative 10-volt signals are applied to the gate inputs. The time durations of the input signals can vary greatly, and combinations of signal levels and pulses are often applied to a gate circuit.

Gate circuits usually include one or more of the following circuit parts: relays, semiconductor or electron-tube diodes, electron-tube triodes or pentodes, transistors, and magnetic cores.

## LOGIC COMPUTATION

#### General.

The flow of information through computer equipment and control of the computer arithmetic section are accomplished by gating circuits in conjunction with inverter circuits. These circuits are called *logic circuits* because their operation can be described by simple statements of formal logic using the connective words *and*, *or*, and *not*. In computer equipment, the basic logic circuits are AND-gate, OR-gate, and NOT circuits.

Statements of formal logic can be written in symbol form and manipulated in a manner similar to the mathematical operation of ordinary algebraic symbols. The branch of symbolic logic that is used extensively for binary computer applications is called **Boolean algebra. In** ordinary algebra the following four basic operations are used: addition, subtraction, multiplication, and division. Only the three basic operations of AND, OR, and NOT are necessary for Boolean algebra. In statements of logic in mathematical form, the AND operation is indicated by the multiplication sign (0), the OR operation is indicated by the addition sign (+), and the NOT operation is indicated by a bar over a symbol. Thus, these operations of logic are written as follows:

A •B'means A AND B  
A + A means A OR B  
A •
$$\overline{B}$$
 means A AND (NOT B)  
 $\overline{A}$  + B means (NOT A) OR B

The symbols 1 and O are used in Boolean algebra to indicate logic actions that are binary in nature. Common binary logic actions that can be represented are: yes or no, true or false, and on or off. You must remember that the symbols 1 and O used for Boolean algebra and the symbols 1 and O used for binary arithmetic are handled differently. The relationships for the AND operation are as follows:

0∘0 <del>–</del> 0
0•1 = 0
1"o ⁼o
$1 \cdot 1 = 1$

The relationships for the OR function are as follows:

0	+	0	=	0
0	+	1	=	1
1	+	0	=	1
1	+	1	=	1

In binary logic any digit must be either of two symbols; therefore, the condition NOT 1 is the same as the condition O, and the condition NOT O is the

same as the condition 1. This relationship is as follows:

$$\overline{1} = 0$$
  
 $\overline{0} = 1$ 

Logic circuits do not perform the actual computer computations, but only control the flow of information through the computer circuits. Counter, accumulator, and adder circuits are used for arithmetic computations.

## **INPUT SIGNALS**

# General.

For operation of logic circuits, the conditions 1 and O can be represented by two different values of voltage or current. For example, the condition 1 may be represented by a positive 10 volts, and the condition O may be represented by a negative 6 volts. Input signals are usually referred to as either *pulses* or levels. Pulses are electrical signals of short duration, and levels are signals of relatively long duration. For example, if 1-microsecond timing signals occur at 1-millisecond intervals, the 1-microsecond timing signal lasting 1 millisecond or longer maybe called a level.

In a digital computer, numbers and instructions are represented by trains of pulses. In a pulse train, the individual pulses are referred to as *bits* or char*acters*, and the entire pulse train is referred to as a word. Large digital computers may use words that contain many bits of information. The bits in such words can be divided into groups, with each group containing information or control data.

# FAILURE ANALYSIS

## General.

Since logic circuits, as used in modem computers, generally are modularized, failure analysis of logic circuits requires a quite different approach than that for the other types of circuits discussed in this Handbook. No failure analysis is provided for circuits in this section of the Handbook on an individual basis; it is given very briefly here only for general discussion.

By the use of lights and special programming in modern military computers, the operator quickly can determine in which area a failure exists, and substitute a new module, or group of modules, when needed. In some instances, it may be considered economical to throw away the module; in other instances, local or factory repairs are made.

In large computer repair centers, test jigs usually are available, and the module is inserted in the jig and simulated test signals are applied to the inputs; the outputs or lack of outputs are noted. Thus the defective part and circuit are quickly located. For small computers, when authorized, a similar procedure may be followed. The computer can be used to supply the necessary inputs, and the outputs can be observed on either a voltmeter, a VTVM, or an oscilloscope. Lack of output when the proper trigger is applied, or a continuous output with no trigger applied, usually will isolate the trouble to the circuit and part at fault.

Many modules consist of several identical but independent circuits on the same printed-circuit board. Once it is determined which output is defective, failure analysis is required only for that single defective circuit. On the circuit level, semiconductor devices (both transistors and diodes) function as switches; they are either in a state of cutoff or saturation-on or off. This factor makes failure analysis much less complex than most other electronic circuits, as fewer voltage levels are involved; outputs from a logic circuit are generally at one of two levels - high or low (Logic 1 or logic O). Once it is determined, therefore, that an output is in a wrong state (with a known input), it is a relatively simple matter \_ to trace back, component by componerit, to find at which point the voltage first appears at the wrong level. When a defective component is found, whether by test procedure or visual observation, it should never be replaced without first checking other related components of the circuit. Many times a defective component is not in reality the cause of the trouble, but the result of yet another undetected trouble, such as a cracked printed circuit board or a defective connector.

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# PART 16-1. SWITCH LOGIC

## SWITCH LOGIC (GENERAL)

Switch logic presents basically two states of action; that is, a switch is either off or it is on. Thus the connected circuit is either inactive or it is activated, and it can represent either the logic state of O or 1. When the switch is off, the circuit is not energized (no voltage or current is present), and it represents the inactive state of O. When the switch is turned on, the circuit is energized (voltage or current is present), and it represents the active state of 1. The opposite condition may also be assumed, if desired.

Actually, switching logic has been used for years prior to the advent of computers and logic circuits. For example, when lights at different locations are operated by one-way, two-way, or three-way switches, a form of elementary switch control logic is represented. Likewise, elevators have been controlled for years by instructions from switches located on different floors. Not only is the elevator started and stopped, it is directed to go up or down and to proceed to different floors. When calied upon to operate in two different directions, it selects a sequence of operation and carries it out, in turn, as each command is **sequentially** followed in accordance with the basic design.

Basically, there are three forms of switching used in logic circuits; the manually operated switch, the mechanically operated switch, and the electromagnetically operated switch. Manually operated switches included knife switches, toggle switches, push-button switches, key switches, rotary switches, and many other variations. Mechanically operated switches are similar to manually operated switches, but are operated by mechanisms such as cams, linkages, hydraulic or pneumatic cylinders, and other means. These are generally used in analog computers where the state of some physical quantity is indicated when the quantity is at a maximum or a minimum, or as it reaches a series of predetermined values. The electromagnetically operated switch is simply a mechanical switch operated by the passage of electric current through a magnet coil. This type of switch commonly known as a relay, finds widespread use today, if an additional set of contacts is added, it can also be used to control another relay; thus numerous combinations of open

and closed circuits can be contrived and automatically controlled to produce logic operations. Relays and switches used in logic circuits differ from the basic electrical relay in construction and size because they need not carry heavy currents or break high voltages; they are usually operated at very low currents and voltages. As normally constructed, the armature of the relay is held in the open position by spring action and closed by the magnetic attraction of the coil for the armature when current is applied. The contacts may be numerous, either normally open or normally closed, or the relay may consist of a stack of contacts containing various combinations. While the selection of the type of coil and relay is basically an engineering problem, the logical designer must be familiar with the types of contacts and coils available for efficient design. There are about five standard types of contact arrangements available (types A, B, C, D, and E which are make, break, break and make, make before break, and break before make continuity-transfer, respectively). Similarly, there are about five different combinations of coils, such as the single coil, the two or more independent winding type, the two or more cooperative type (two or more windings must be energized simultaneously for operation), other combinations with holding windings, and differential types which can alternately energize or simultaneously reenergize the relay. Since this article is devoted to switch logic rather than component design, it is suggested that the interested reader, obtain further data on relays and contacts by consulting manufacturers' catalogs containing design and operating specifications. Further mention of contacts and coils will be made only when pertinent to the logic design or circuit operation.

Let us now consider simple switch logic. First, it must be understood that in applying switch logic all operations are treated first in elementary form, that is, as simple make and break contacts. Later, after the logic is firmed up, the contacts are counted and various relay contact stack arrangements are considered in **order** to determine the minimum number and types of contacts and relays. This summation is known as *simplification*, which will be discussed later in the section.

Examine the simple series switching circuit formed by two relay contacts connected in series, as shown in the following figure. For simplicity, actuating coils



# Series Switching Circuit

are not shown. Part A of the figure shows an elementary normally open circuit; when the coil of each B c O 0 1 0 o 0 1 1

Α

0

0

?

1

# **AND Truth Table**

Consider now a parallel arrangement of contacts, as shown in the following figure. It is evident from an examination of the figure that current flows in the load circuit when either contact A or contact B is closed, or when both contacts A and B are closed



**Parallel Switching Circuit** 

Note that current will flow when A is closed, regardless of whether B is closed, and vice versa. This action is indicated by logic notation as follows: C = B (A+A') + A (B + B') which can be reduced to: C = AB +A'B + AB + AB'. As interpreted logically, this expression says that the load will draw current if A and B are closed, or if B is closed and A is not closed, or if A and B are closed, or if A is closed and B is not closed. Since AB + AB = AB, the expression for C may be simplified to: C = A'B + AB' + AB. A truth table for the preceding function follows: This table is

4	В	С
<b>b</b>	0	0
)	1	1
1	0	1
1	1	1

## Inclusive OR Truth Table

recognized as a typical OR table. Since it includes operation when A and B are both closed, it also represents the inclusive OR logic state. In general, then, we may say that parallel switching contacts **represent** the logic OR **state** (addition). The exclusive OR logic **state** is indicated when either A or B activate the

contact is actuated, the relay switch is closed. Thus, in order for current to flow in the load circuit, coils A and B must both be actuated, thereby, closing contacts A and B and completing the circuit. If contact A is closed and contact B is open, no current flows. The same condition follows with B closed and A open (the closed condition is indicated by printing the contact, e.g., B' instead of B). With both contacts open a similar condition exists, so that one, and ordy one, condition will produce current flow into the load, namely when both contacts are closed. Let us tabulate these conditions using O to represent open contacts and 1 to represent closed contacts. Such a table, commonly called a *truth table* or a *table of combina*tions is shown below. This truth table is easily identified as the typical AND logic operation (multiplication). In part B of the figure, contact A is normally closed when the relay is de-energized, and, since it is closed it is represented in logic notation by priming the letter, thus making it A' (indicating "not" open) instead of A. Forgetting for the present whether the coils are energized or not, consider only the contacts. For each opening and closing combination the AND truth table still applies. A similar condition exists for part C of the figure, except that B' is the primed contact (normally closed). Thus, we may say in general that a series arrangement of relay contacts produces the AND logical function. The circuit of part A is simpler to comprehend and follow in logic design, since the circuit operates only to produce current when both relay coils are energized; in parts B and C only one relay need be energized at a time to produce the desired condition.

 $\smile$ 

circuit, but the circuit remains inactive when both A and B are operated. Such a condition is shown schematically in the following figure. A truth table for the



#### **Exclusive OR Circuit**

circuit above is shown below. It is recognized as the classic exclusive OR truth table, proving our contention that the schematic is that of the exclusive OR circuit by perfect induction.

Α	В	С
o	0	0
0	1	1
1	0	1
1	1	0

#### Exclusive OR Truth Table

In addition to the schematic form of relay circuit drawings shown above, a kind of short-hand notation (diagram) is sometimes used, as shown in the following figure. In this form of notation the horizontal line@represent normally closed (or primed) contacts, while the diagonal lines represent the normally open (or unprimed) contacts. The contacts shown in a particular column are all operated by the same relay. The figure illustrates relay logic notation as applied to the circuit of the series-parallel switch contacts representing the exclusive OR circuit shown by the preceding schematic. The abbreviations N.C. (normally RELAY A RELAY B B' (N.C.) IN A' (N.C.)

closed) and N.O. (normally open), shown in parenthe-

ses in the diagram, are not normally included.

**Relay Logic Notation Diagram** 

While this discussion of switching logic has presented the basic AND and OR switching circuits, the discussion is limited to logic concepts alone. The circuit action of specific logic circuits is discussed in the latter part of this section.

## **OR CIRCUITS**

## Application.

The OR circuit is used in mechanical computers and switching circuits to perform logic addition.

#### Characteristics.

May use positive, negative, or combined logic.

Consists of a series of switching contacts connected in parallel.

Performs logic addition.

Switch may be electrically or mechanically operated; usually consists of a group of relays.

No amplification is produced.

L

**CHANGE 1** 

## Circuit Analysis.

**General.** In switch logic, a basic OR circuit consists of a group of parallel connected single pole, single throw switches connecting the power source to the output load, as shown in the accompanying schematic.



Basic OR Switching Circuit

As can be seen from a study of the schematic, in the inactive condition all switches are open, and since the load and output are not connected to the power source there is no output, representing a logic O. Conversely, when any of the switches are turned <sup>On</sup>, either separately or in combination, the power is connected to the load and the output voltage is the same as the input voltage, representing a logic 1. The logic diagram for this circuit is shown symbolically in the following illustration, with a truth table.



OR Logic Diagram

Truth Table

From the symbolic logic diagram it is evident that there is no difference between the mechanical and electronic circuit, the symbol is functional. Since it is necessary to operate each switch by hand in the example given, and switches are not affected by polarity, the level indicators are omitted from the logic diagram. Because little advantage is obtained by requiring manual manipulation of the switches, the mechanical computer uses relays. Applying the proper potential to the relay coil pulls in the relay armature and closes the circuit. Thus by using another relay to control a series of switching operations, performed by groups of relays arranged in the proper switching sequence, electro-mechanical computers which operate at high rates of speed are formed. Speed of operation is limited by the time it takes the relays to open and close. Since relays are expensive and require more power and space than transistors or diodes, these types of computers find limited use.

**Circuit Operation.** The schematic of a typical relay-type of OR switching circuit is shown in the following illustration.



#### Three-Input OR Relay Circuit

The inputs are applied to the coils of relays K1, K2, and K3. When energized, these relays close and complete the circuit from the power source through common load resistor  $R_L$  to ground. When no input signal is applied either A, B, or C, the circuit through the load resistor to ground is open, no current flows through  $R_L$ , and the potential at the output is the relatively high positive level of the power source. Assuming a negative voltage (a positive voltage could also be used) representing a logic 1 is applied to input terminal A, relay K1 closes and the current flowing through  $R_L$  to ground produces a voltage drop which lowers the output to the zero level. The output stays at the zero level for the duration of the input pulse and

CHANGE ]

then returns to the normal high positive level when the input signal ceases and K1 opens. Thus, a negative output pulse is generated. If inputs B or C are activated the same sequence of operation occurs, except that relays K2 or K3 are energized instead of KI, In either case a negative output is developed. If two inputs are activated simultaneously, an output also will be generated. This represents the case of the *inclusive OR* where the output is A + B + C + AB + AC+ BC + ABC. This type of OR circuit allows several independent signals of different origins to perform the same switching function without any interaction between the signal sources. The relay in the OR circuit thus acts as a buffer or isolating element. To perform logic addition, this circuit must be used together with other OR or AND circuits arranged to produce the desired logic function. Should inversion or the NOR type of operation be desired, it is only necessary to control these relays with another relay, which when activated temporarily shorts the second relay coil causing it to deactivate. In this special case, the input signal does not produce an output signal.

To accomplish the exchrsive OR operation it is necessary to prevent operation of the other relay when one relay is already activated.

This is accomplished by adding a back contact on each relay which is normally closed. The logic symbol and truth diagram for this circuit is shown in the following illustration.



Exclusive-OR	Logic	Diagram	Truth	Table

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In this instance, the logic symbol changes slightly to indicate that this is the exclusive-OR function and not the inclusive OR function. The circuitry, however, may be solid state, electron tube, or mechanical without change of symbol as long as the same function is achieved. The schematic of the mechanical exclusive-OR circuit is shown in the following illustration.

Likewise, when B is activated relay K2 closes and produces an output only if contact A' is closed. Since activating the relay opens the normally closed contact, whenever two relays are activated the circuit to the power supply, load, and output will be opened and an output cannot be produced. Thus, a negative pulse is generated only when one of the inputs is activated at a time, and never when more than one is activated simultaneously. Thus, the exclusive OR function is accomplished as shown in the truth table.

## AND CIRCUITS



The AND circuit is used in mechanical computers and switching circuits to perform logic multiplication. It is sometimes called a coincidence circuit in other publications.

# Characteristics.

May use positive, negative, or combined logic. Consists of a group of switching contacts connected in series.

Switch may be mechanically or electrically operated, usually consists of a group of relays.

No amplification is provided. Performs logic multiplication.

#### Circuit Analysis.

General. In switch logic, a basic AND circuit consists of a group of single pole, single throw switches connected in series, as shown in the accompanying schematic.



**Basic AND Switching Circuit** 

B' C = AB' + BA

#### **Exclusive-OR Relay Circuit**

A simplified schematic of this circuit showing only the relay contacts is shown in the following illustration to simplify the discussion. Note that for any circuit to produce an output, the other relay must be resting in the normally closed position, as indicated by the primed symbols. Thus, when input A is activated, relay K1 closes and produces an output only if contact B' is closed.



Simplified Contact Arrangement

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As can be seen from the schematic, in the inactive condition all switches are open, and since the load and output are not connected to the power source there is not output, representing a logic O. Conversely, when all the switches are turned on, the load is connected to the power source, and an output is developed across load resistor RL by the current flowing through the circuit, representing a logic 1. The logic diagram for this circuit is shown symbolically in the following illustration, with a truth table.



#### AND Logic Diagram Truth Table

From the symbolic logic diagram, it is evident that there is no difference between the mechanical and electronic circuit, the symbol is functional. Since it is necessary to operate each switch by hand in the example shown, and switches are not affected by polarity, the level indicators are omitted from the logic diagram. Because advantage is obtained by requiring manual manipulation of the switches, the mechanical computer uses relays. Applying the proper potential to the relay coil pulls in the relay armature and closes the circuit. By using one relay to control a series of switching operations performed by groups of relays arranged in the proper switching sequence, electro-mechanical computers which operate at high rates of speed are formed. Operating speed is determined by the time it takes the relays to open and close (from 1 to milliseconds on the average). Since relays are expensive and require more power and space than transistors or diodes, these types of computers find limited use.

**Circuit Operation.** The schematic of a typical relay-type of AND switching circuit is shown in the following illustration.



#### Three-Input AND Relay Circuit

The inputs are applied to the coils of relays K1, K2, and K3. When closed, these relays connect common load resistor RL to ground. In the deenergized position, the load circuit and output float at the supply voltage, and this high positive output level is considered to represent a logic O. When all three inputs are activated simultaneously, relays K1, K2, and K3 close and connect the load resistor and output to ground. The high positive output voltage is dropped to zero by the current flowing through the load resistor and the output is effectively a large negative-going pulse. For the duration of the input signal or pulse, the output remains at zero and then rises to its normal high positive level when the input terminates, completing the negative output pulse.

Because of the series arrangement of relay contacts the circuit is only completed when all contacts are closed. Thus, as shown in the truth table previously, all outputs are zero, except when all the inputs are simultaneously activated to produce a "one" signal.

## FLIP-FLOP CIRCUITS

#### Application.

Relay type flip-flop circuits are used in mechanical computers and switching circuits to supply off-on

triggering pulses and provide a signal and its complement simultaneously, they are also used as storage elements. It forms the basic circuit used in most registers.

## Characteristics.

May use positive, negative, or combined logic.

No amplification is produced.

Consists of two operating and two control relays.

Provides two output signals (one is the inverse of the other).

Usually requires two inputs (an "off" trigger and an "on" trigger).

# Circuit Analysis.

**General.** The relay type of flip-flop is the mechanical switching equivalent of the transistor or electron tube bistable multivibrator (it is sometimes known as a "toggle switch" circuit). It has two stable states, one the inactive or zero-state, and the other the active or one-state. Once triggered, one relay is held in the active position until it is released, meanwhile the other relay rests in the inactive condition until a trigger appears. Thus, this type of circuit provides a limited amount of storage. It will retain either a zero or a one indefinitely, and without attention, until it is triggered into the opposite state of operation. The logic diagram for this circuit is shown symbolically in the following illustration, together with a truth table.





Truth Table

It is evident there is no difference in the logic symbol between electronic and mechanical flip-flops, since the symbol is functional. When the symbol bears the designations C and Son the unidentified leads it indicates a clear (reset) input for C and a set input for S. The clear input always returns the flip-flop to the zero or inactive state, while the set input always triggers the flip-flop into the active or one condition. It is not necessary to label these inputs, but they may be labelled, if desired.

**Circuit Operation.** The schematic of a typical relay flip-flop is shown m the following illustration. The outputs are X and Y, and the inputs are **A** and B which operate control relays K3 and K4. The flip-flop operating relays are K1 and K2.



**Relay Flip-Flop Circuit** 

When no power is applied, both relays K1 and K2 rest in the deenergized position and no output is produced. When power is applied, both relays will try to close since their coil is connected between the power source and ground. The first relay to close will lock out the other relay and prevent it from closing, and the circuit will rest in one of the two possible conditions. Assume for the moment that relay K1 is closed, then relay K2 is open and output Y is connected to ground via the contacts of KI. Current flow to ground through RL, will drop the voltage at terminal Y to zero and simulate a O. Meanwhile, RL<sub>1</sub> and the coil resistance of K1 form a voltage divider from +V to ground, and output X will be a positive voltage determined by the ratio of the resistances in the voltage divider, but is always less than the supply voltage. As long as K1 remains closed, the X output will be a positive voltage representing a 1. When input A is activated by a "set" signal, relay K3 closes and grounds the coil of K1 by shunting it to ground and

causing K1 to open. As soon as K1 opens, current flow through RL, and the coil of K2 to ground pulls in relay K2. The output of terminal X is now O, since it is grounded, while the Y output is the voltage developed across K2 coil (K2 and RL, form a voltage divider between +V and ground). The conditions are now exactly reversed, and the Y output is a positive voltage less than the source value, while the X output is O. When a "clear" pulse is applied to relay K4 by energizing B input terminal, relay K2 is shorted out and K1 operates and resumes control. Thus the flipflop may be made to change state by alternately energizing control terminals A and B. (The trigger is only momentary it is not continuous.) As a result, the flip-flop produces two outputs, one the inverse of the other as shown in the waveforms, and will rest in one state until triggered into the opposite state.

Circuit arrangements may be made to produce negative output voltages if desired, and the control relays may be triggered by either positive or negative voltages, since the relays are not polarized. The output voltage will be determined by the values of relay coil resistance and load resistance used for a specific source voltage and will never exceed the source, except possibly for the switching transients shown by the pips on the output waveforms. With proper design these transients can be practically eliminated,

#### TWO-WAY AND THREE-WAY CIRCUITS

## Application.

Two-way and three-way circuits are used in computers and switching devices to apply to outputs of two or three other logic circuits to the input of a single logic circuit, and control its output.

#### Characteristics.

May use positive, negative, or combined logic. Uses combinations of OR and AND circuits. Has a number of inputs, but only a single output.

#### Circuit Analysis.

**General.** Two-way and three-way circuits provide a means of combining logical operations so that the result can be handled by simple off-on switching circuits. Combinations of AND and OR gates offer a convenient and easy method of fanning-in a large number of inputs to a single output line. Besides being convenient for binary and digital use they are also useful for control functions. For example, if it is necessary for three switches to be placed "on" before another switch can be operated, a simple three-input AND circuit will control this operation. Likewise, the turning on of a transmitter from two separate locations is accomplished by a simple OR gate. In digital logic it is the arrangement of these two-way and three-way circuits (or four- or five-way circuits) which form the arithmetical or logic circuit used as an adder or subtracter, or otherwise to produce the desired function(s).

**Circuit Operation.** A basic two-way circuit consisting of two AND gates and an OR gate is shown in the following logic diagram.



Two-Way Circuit Logic Diagram

Note that the logic diagram is functional and does not indicate the actual circuit, so that diodes, transistors, relays or switches could be used as long as the proper function was performed. Note also, that the actual circuit diagram or schematic is not needed in understanding circuit logic. When inputs A AND B exist the first AND gate produces output AB. Likewise, when inputs C AND D exist the second AND gate produces output CD. These inputs can be at two different levels and supplied from separate logic circuits. When either input combination is applied to the OR gate a single output is produced, and, since it also represents the inclusive OR function, when both combinations simultaneously exist an output is also produced from the OR gate. Thus the output of this circuit is AB + CD + ABCD, and the two level input is expressed as a single-level output.

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A typical schematic diagram using relay switching to accomplish the logic explained above is shown in the accompanying illustration.



through RI drops the output to zero. When these relays are released, output F again assumes a high positive level. Thus the OR gate output effectively is a negative pulse representing a 1, and negative logic is employed.

A three-way or three-level logic circuit merely provides an additional input level over the two-way circuit. Therefore, by adding another AND circuit as shown in the following logic diagram, a three-way circuit is obtained.



#### **Two-Way Circuit Schematic**

Relays K1 and K2 form one AND gate, while relays K3 and K4 form the other AND gate. Both AND gate relay contacts are connected in series to ground, and actuate relays K5 and K6 of the OR gate when appropriate inputs are applied. When either K1, K2, K3, or K4 alone are actuated, the circuit to ground for the OR gate relay coil is open since only one set of contacts is closed. However, when both K1 and K2, or K3 and K4, or all relays are activated simultaneously, the OR gate is activated. Therefore, when an output such as AB is obtained from the AND gate by closing relays K1 AND K2, relay KS is closed and output F is at ground potential. Normally, with KS and K6 open, output F is at a high positive level since no voltage drop occurs across RI. However, when K5 AND K6, or K5, or K6 is closed, current flow to ground

## Three-Way Circuit Logic Diagram

Examination of the new logic diagram reveals that when input A AND B exist, the first AND gate produces output AB. Similarly, when inputs C AND D are present the second AND gate produces output CD; and finally, when inputs E AND F are present, the third AND gate produces output EF. When any of the AND gate outputs are applied to the OR Gate input a single output is produced. Since this circuit also includes the inclusive OR function, when all combinations simultaneously exist an output is also produced from the OR gate. Thus the output of the three-way circuit is AB + CD + EF + ABCDEF+ABCD+ABEF+CDEF, and the three-1 evel input is expressed as a single-level The schematic diagram for out put . the three-way circuit is shown in the following illustration, using relay switching to accomplish the logic indicated and explained above.

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#### Three-Way Circuit

Relays K1, K2, K3, and K4 operate identically with the previously described two-way circuit and the new relays K7 and K8 have their contacts connected in series to ground, controlling new OR gate relay K9. Since the contacts of K9 are connected in parallel with those of KS and K6, operation of the OR gate drops output F to zero level when K9 is closed. Therefore, when relays K7 and K8 are simultaneously activated, relay K9 is closed, producing an effective negative output for a logic 1.

## SIMPLIFICATION PRINCIPLES

#### Application.

Simplification is used to reduce the number of logic or switching circuits necessary to obtain a desired functional result.

# Characteristics.

Circuit is reduced to simplest form.

Unnecessary or excessive components are eliminated.

Usually employs Boolean Algebra.

Function is not changed.

# Circuit Analysis.

General. The process of simplification is generally to reduce any given circuit to its simplest form without changing the logic. This is accomplished by eliminating unnecessary switches or by substituting one switch for duplicate switching. There are two basic methods which can be used; the first method involves pure reasoning, while the second method uses the mathematical manipulations of Boolean Algebra to reduce the unsimplified expression to its simplest form. Examples of each method will be given. Since simplification and the intricacies of Boolean logic are mainly of use to the logic designer, and the equipment encountered in Naval use will already be in simplified form, the subject is only briefly discussed in this Handbook in elementary form. For more information on this subject the interested technician should consult the text books on logic design available from commercial sources and public libraries.

**Procedures.** A simple switching circuit involving AND and OR operations is shown in the following illustration, with its simplified equivalent.



Switching Network Simplified Representation

Since switch NOT B (B') is normally closed, while switch B is normally open, the path from X to Y will always be completed when switch A is closed. Thus both B and B' switches may be removed and a closed wire connection made between switch A and output Y, leaving switch A as the only one in the circuit. When represented in Boolean notation, multiplication of A AND B or A AND B' is indicated because of the series ANDing of the switches, and the summing of these quantities is also indicated because of the parallel connection (ORing) of switches. Thus the original expression is  $(A \cdot B) + (A \cdot B')$ . If we factor A from both terms we can rewrite the expression as  $A \cdot (B + B')$ . However, the quantity (B + B') is equal to 1 by the first law of complementation in the Boolean postulates. Therefore, we write expression as A(1) which is equal to A, proving the simplified version and reasoning are correct.

Let us now take a more complex switching arrangement where it is desired that point X be connected to point Y through independent elements A, B, C, D, E, AND F, as shown in the following illustration.



**Complex Switching Circuit** 

We may now reason as follows. Since switch A' is normally closed and any path between X and Y must have switch A closed, switch A' will always be open and may be eliminated to produce the simpler circuit. (See following illustration.)



First Simplification

Note that the circuit now consists of a series group of switches forming an AND circuit, and feeding a group of series and parallel switches. Further simplification is desirable. Since B and C switches must be closed for the AND gate to operate, duplicate switches B and C may be eliminated and wired across, producing the second simplified circuit. (See following illustration.)



#### Second Simplification

Finally, we may reason that switch F provides an independent path, which if F is open has an alternative path offered through D' or E AND F'. Therefore, D' and E may be directly wired to Y and F' disposed of. Thus the final circuit version is obtained, as shown in the following illustration, consisting of an AND gate feeding an OR gate.



#### Final Simplification

By elementary reasoning the 13 switch circuit is reduced to 6 switches and retains the original desired function. This is proven with Boolean algebra as follows. The overall expression for the unsimplified network is:

A(A' + BC) [ (D'+ E) • C • F'+ DA'F + BF]  ${}^{=}F$ , - and F = 1

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Combine the terms in the following manner:

$$(AA' + ABC)$$
  $[D'CF' + ECF' + DA'F + BF] = F$ 

since AA' in the first expression is equal to O, therefore

$$(ABC) [D'CF' + ECF' + DA'F + BF] = F$$

and we have by further combining

$$ABCD'F + ABCEF' + AA'BCDF + ABCF = F$$

but AA' in the third term is equal to O eliminating the term, and

ABCD'F + ABCEF' + ABCF = F

combining the last two terms gives

$$ABCD'F' + ABC (F+F'E) = F$$

since F + F' equals 1 we have

ABCD'F' + ABC (F + E) = F

eliminating the parentheses we get

$$ABCD'F' + ABCF + ABCE = F$$

combining the first two terms gives

$$ABC (F+F'D') + ABCE = F$$

since F + F' equals 1 we have

$$ABC (F+D') + ABCE = F$$

recombining terms we get

$$ABCF + ABCD' + ABCE = F$$

which can be written as

ABC (F + D' + E) = F), which agrees with the final simplification

arrived at by a simple reasoning.

# PART 16-2. DIODE LOGIC

# **DIODE LOGIC (GENERAL)**

Diode logic is the simplest type of logic, corresponding, in general, to switch operation. Either the switch is ON (diode conducting) or it is OFF (diode non-conducting). It is usually used where signals of only two levels are involved (the off level and the on level) although three-level circuits may be arranged, if desired. Either negative or positive logic maybe used with the same circuit arrangements, except that the diode connections must be reversed. While it is important that the forward resistance of the diode be low, it is more important that the reverse resistance be very high. Thus when diodes are parallel-connected their paralled reverse-resistance is still high, and leakage and operating power requirements are low; also, false triggering will not occur. Another advantage to the use of diode logic is that no inversion of the output signal occurs. Thus it may be unnecessary to add an inverter circuit to return the signal to its original polarity; this helps simplify computer design.

The diode also lends itself to multiple arrangements where a combination of inputs is used to produce a single output, usually called a decoding matrice or matrix. Conversely, an arrangement with single inputs producing a multiple output is known as an encoder matrice or matrix. In general, when arranged in a rectangular arrangement the matrice becomes a rectangular matrice, regardless of function, that is, it may be either an encoder or decoder. Each of these basic circuits and arrangements are fully discussed in the following paragraphs.

# OR GATE

## Application.

The diode OR gate is a basic logic circuit which produces an output when either input is activated, and when both inputs are simultaneously activated (inclusive OR). It replaces the relays and electron tubes used in earlier computers.

# Characteristics.

May use either positive or negative logic.

A signal at any of the inputs produces an output. Output never exceeds the input (no amplification is obtained).

### Circuit Analysis.

**General. Logic** circuits differ from basic electronic circuits in their general treatment. Through the use of standard logic symbols (see Graphic Symbols for Logic Diagrams, ASA Y32.14-1962 for a complete list), a block-diagram type of presentation may be \_ used, instead of the conventional schematic representation with which the ET is more familiar. Thus the signal path and operation can be followed, or considered, without regard to the actual electronic circuit operation. Typicrd standard symbol used to represent a positive logic OR circuit are shown in the following illustration, accompanied by a truth table of possible combinations.



# Positive OR Gate Symbols Table of Combinations

A high level or positive logic is indicated by the **filled-in** (or solid) right triangles in the symbol. The inputs are A or B. The output F shows in Boolean algebra notation the result (A+B), where the + sign indicates OR (addition). The table of combinations shows every possible combination of input and output and is therefore, called a truth table. When either input A or input B (or both) are at a relatively high level, the output, F, is also at a relatively high level. When both A and B are at a low level, so is output F.

When negative logic is used, the following symbol and truth table apply.



#### Negative OR Gate Symbol Table of Combinations

A low level or negative logic is indicated by the open right triangles in the symbol. The table of combinations shows that for all inputs but one, the output is low. When both inputs are high, then the output is also high.

**Circuit Operation.** A two-input positive OR gate is shown in the following illustration. The gate consists of two diodes, CR1 and CR2, and current limiting resistor, R, connected as shown in the schematic.



### **Two Input Positive OR Gate**

When the OR gate is inactive (no inputs) it is forward biased by the large negative voltage applied the cathode, and usually a small negative voltage, representing O, is applied to the anode and a small current flows through either CR1 or CR2. Actually, a reverse

current may also flow depending upon the reverse leakage of the diode. This current, however, is so small in most cases that it may be neglected. Thus if sufficient diode current flow through R to drop the bias supply to zero, no output is produced at F. When an input is applied to either A or B, more current flows through R depending upon the amount of voltage applied, and its polarity. If a voltage of exactly -V, is applied both sides of the diode will be at equal potentials and no current will flow. If negative, but less than -V a current equal to that produced by an equivalent positive voltage will flow. That is with -20 volts applied and assuming V to be -30 volts the anode will be effectively 10 volts positive with respect to the cathode. Similarly, if 5 volts positive is applied to A or B, the effect will be as if the anode of the associated diode were at +35 volts. A larger current will flow and a greater voltage will be dropped across R. The output is taken from the diode end of R to ground. Thus, if sufficient voltage is applied to either A or B the entire bias source will be dissipated across R. Hence the only voltage existing as an output will be the input voltage applied the anode. If +5 volts is applied to either A or B, the output at F will be +5 volts, which is considered to be a logic 1 in this example. It can be seen that no gain results. Actually, the conducting diode has some slight resistance, and the examples discussed above are for the idealized case where the diode is considered to have zero resistance. Thus, at all times, the actual OR gate output is always slightly less in value than the input, when using diode logic. This is to be expected, since the diode itself has no inherent gain. Note, also that the input signal is not inverted (this is true of all diode logic circuits and helps simplify design).

When both diodes are activated simultaneously, the output will be the highest voltage applied to CR1 or CR2. Since in every case a positive input signal is required to produce an output, positive logic is used. The output pulse will continue for the duration of the trigger pulse and be of approximately the same shape. Because the input pulse appears as the output pulse, a reverse bias of this value is applied the nonconducting diode. Therefore, when signals are applied to inputs A and B, simultaneously, the larger amplitude signal determines which diode shall conduct. For exactly equal amplitude signals, both diodes will conduct. The difference between logic circuits and

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conventional electronic circuits is that in the logic circuit, distortion which would be intolerable in the communications circuit is acceptable. Thus it is only necessary for the logic circuit to provide a signal of sufficient amplitude and of the proper phase (or polarity) for actuating the next logic circuit.

The positive OR circuit is sometimes referred to as a negative AND circuit, because if the polarity of the input trigger is **reversed** so that a negative signal represents a 1 and a positive signal a zero, a combined input will produce a negative output, but separate inputs will **not**. Because of the interchangeability of the OR and AND functions with polarity it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals produce a O, we may call the OR circuit previously discussed above a positive OR gate. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

A two input negative OR gate is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, comected as shown in the following schematic.



## **Two Input Negative OR Gate**

The negative OR gate operates inversely to the positive OR gate. Thus, when inactive, it is held so by inputs approximately equal to +V and no conduction occurs. This represents the O state. When a negative 1 is applied either A or B, the respective diode is

forward biased and current flows through R. Electron flow is in such a direction that the output end of resistor R is negative, and the input signal appears as the output. While one diode is conducting, the other diode is reverse biased by the amount of the output signal; thus it cannot conduct unless a greater negative voltage is applied its input. When both inputs are simultaneously activated with a negative signal, if equal in amplitude both diodes conduct. This is the case of the inclusive OR. If the polarities of the O and 1 are reversed, the negative OR gate will function as a positive AND gate. Thus the proper conventions must be used to produce the desired function. When the 1 input is relatively more negative than the O input, the above discussion, the symbol, the schematic, and the truth table for the negative OR gate apply.

### AND GATE

#### Application.

The diode AND gate is a basic logic circuit which produces an output only if all of its inputs are simultaneously activated. It represents the basic logic circuit for binary multiplication, and the dot symbol is used to indicate this (A B = C). It replaces the relays and electron tubes used in earlier computers.

## Characteristics.

May use either positive or negative logic.

A signal is required at both inputs to produce an output.

Output never exceeds the input (no amplification is obtained).

### Circuit Analysis.

**General.** Logic circuits differ from basic electronic circuits in their general treatment. Through the use of standard logic symbols, a block diagram type of presentation may be used, instead of the conventional schematic circuit representation with which the ET is more familiar. Thus the signal path or operation may be followed, or considered without regard to the actual electronic circuit operation. Following is a typical standard symbol used to represent a positive logic AND circuit accompanied by a truth table of possible combinations.



output is low. For any single input, the gate remains inactive and rests in the high state.

**Circuit Operation.** A two-input positive AND gate is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, and current limiting resistor, R, connected as shown in the following schematic.

#### Positive AND Gate Symbol — Table of Combinations

A high level or positive logic is indicated by the **filled-in** (or solid) right triangles in the symbol. The inputs are A and B. The output, F, shows in Boolean algebra notation the result  $(A \cdot B)$ , where the dot sign indicates AND. The table of combinations shows every possible combination of input and output, and is, therefore, called a truth table. When inputs A and B are both at a relatively high level, the output, F, is also at a relatively high level. When both A and B are at a low level, so is F. For a single input the gate remains inactive.

When negative logic is used, the following symbol and truth table apply.



#### Negative AND Gate Symbol - Table of Combinations

A low level or negative logic is indicated by the open right triangles in the symbol. The table of combinations shows that for all inputs but one, the output is low. When both inputs are low, then the

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When no inputs are applied, the cathodes of CR1 and CR2 are at a relatively low level with respect to their anode. Thus the cathodes are effectively negative with respect to the anode and the diodes conduct. The diode current flowing through resistor R produces a voltage drop equid to that of the supply and of opposite polarity. Therefore, at the output end of R the potential is zero, and no output signal exists between F and ground.

Should a positive input be applied to either A or B alone, either CR1 or CR2 will cease conducting. However, the other diode will then conduct more heavily and keep output F at zero. Thus if only one input is activated there will be no output. On the other hand, if both A and B inputs are activated simultaneously by a high level or positive signal, the cathodes become more positive than the anodes and both diodes cease conducting. When conduction ceases, the voltage drop across resistor R no longer exists, and output F rises to the full value of the

supply voltage (becomes highly positive). Thus a **posi**tive output is produced when both inputs are simultaneously activated by a relatively high level input representing a 1.

A positive AND gate is sometimes referred to as a negative OR gate, because if the polarity of the input trigger is reversed so that a negative signal represents a 1, and a positive signal represents a zero, a single input will produce a negative output, but combined inputs will not. Refer to the OR gate schematic in the previous discussion earlier in this Chapter and observe they are identical. Because of the interchangeability of the AND and OR functions with polarity it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals a O, we may call the AND circuit discussed previously above a positive AND gate. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

In some systems, O's and 1's are represented by the absence or presence of a pulse. If the pulse is absent it represents a O, if present, a 1. The AND gate produces a pulse at its output only when all inputs are present. Thus in a three input AND gate, inputs A, B, and C must all be activated before an output can be produced. Where both **d-c** and pulse levels are used, all must also be activated. If two levels are dc and the third is a pulse, then both dc levels must be positive and a positive pulse must appear at the third level before the circuit will operate. Absence of the pulse would be a O exactly as though a negative signrd were applied instead, and the circuit would not operate.

A two input **negative AND gate is** shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, connected as shown in the following schematic.



#### Two Input Negative AND Gate

The negative AND gate operates inversely to the positive AND gate. Thus, when inactive, the anodes are at a relatively high level (positive) with respect to the cathodes, which are connected to the negative supply through R, and they conduct. The voltage drop across R is opposite the supply and equal so that no voltage exists at the output end of resistor R, thus no output is obtained from F. When either input A or B is activated (with a negative 1 signal) the associated diode stops conduction, but the other diode maintains the output at zero. However, when both inputs are simultaneously activated by a low level or relatively negative input the anodes become more nega-. tive than the cathode and the diodes cease conduction. Since no current now flows through R, the voltage at the output terminal rises to the value of the supply voltage, and a negative output representing a 1 is produced. When the inputs cease, the output again terminates and the gate is considered inactive, even though this is the period during which the diodes are active and conducting.

If the polarities of the O and 1 are reversed, the negative AND gate will function as a positive OR gate (see schematic in previous OR gate discussion in this section of the Handbook). Thus the proper conventions must be used to produce the desired function. When the 1 input is relatively more negative than the O input, the above discussion, the symbol, the schematic and the truth table for the **negative AND gate** apply.

## **RECTANGULAR MATRICES**

#### Application.

A rectangular diode matrice (matrix) is used in computers to perform a specific function, such as supplying a single output when supplied with multiinputs or vice versa. It may also be known by its functional name instead. Thus, although arranged as a rectangular array it may be known as an encoding or decoding matrice. Actually it is a generic name for a class of circuits which are also named for the function they represent.

#### Characteristics.

May use positive or negative logic.

Consists of an orderly rectangular array of diodes. When many inputs are supplied only one or a very few outputs are produced, and vice versa.

Gain is less than 1 (no amplification is provided).

## **Circuit Analysis.**

**General.** Rectangular diode matrices have no specird characteristics or functions of their own other than an ordered array of diodes. The matrix arrangement does not make it a logic circuit. It is the manner in which the matrix elements are connected that determines the logic function produced. Thus to describe a computer as containing a rectangular matrice is of no significance unless the associated function is also described.

**Circuit Operation.** A simple rectangular matrice composed of two AND gates and one OR gate, which

perform the logic function (AB + CD) are first shown symbolically, then as a matrix diagram, and finally, in schematic diagram form.





As shown in the preceding logic diagram, the diode AND gates are AG1 and AG2, and the diode OR gate is OG1. Inputs A and B are provided for AGI, and C and D for AG2; the output of both circuits is combined by the OR gate at F. Thus output F is active whenever AGI output (**A'B**) is active, or when AG2 output (**C''**D) is active, or when both AG1 and AG2 are active. The output function is written symbolically as AB+CD, which is read as A AND B, or C AND D, or both A AND B and C AND D. The last mentioned condition is the inclusive OR function.

The diode matrix representation of the function, F = AB + CD is shown in the following illustration. AND gate AG1 consists of diodes CR1 and CR2, with current limiting resistor R1. AND gate AG2 consists of diodes CR4 and CR5, with current limiting resistor R2. OR gate OG1 consists of diodes CR3 and CR6, with current limiting resistor R3. h-r the drawing, zero volts represents a logic O and +V volts represents a logic 1, thus positive logic is used, and output F is active (logic 1) when it is at +V volts relative to ground. It is inactive (logic O) when it is at zero volts relative to ground.



#### Matrix Representation

Assume that all inputs (A,B,C, and D) are at zero volts (logic O). With the anodes of CR1, CR2, and CR4, CR5 connected to the positive bias supply through RI and R2, respectively, the diodes are forward biased and conduct. The supply voltage is dropped across resistors RI and R2 so that the anodes of OR gate diodes CR3 and CR6 are also at approximately zero volts. Because the cathodes of the OR gate diodes connect to ground via R3, there is no difference in potential across these diodes and no conduction occurs. Thus, the output of the OR gate remains at zero volts (a logic O). The conditions stated above are shown on line 1 of the table of combinations following. That is, all inputs and the output are at a low level (L).

		IN	PUT		ουτρυτ
		А	в	c D	F = (AB + CD) (H)
1	L	L	L	L	L
2	L	L	L	н	L
3	L	L	н	L	L
4	L	L	н	н	н
5	L	н	L	L	L
6	L	н	L	н	L
7	L	н	н	L	L
8	L	н	н	н	н
9	н	L	L	L	L
10	н	L	L	н	L
11	н	L	н	L	L
12	н	L	н	н	н
13	н	н	L	L	н
14	н	н	L	н	н
15	н	н	н	L	н
16	н	н	н	н	І н
Table of Combinations					

Assume now that the condition on line 13 is true. That is, inputs A and B are active at +V volts (relatively high), and inputs C and D are inactive at zero volts (relatively low). With inputs A and B both at +V volts, diodes CR1 and CR2 are held in the nonconducting state (reverse biased), while CR3 anode is positive with respect to ground and conducts, current flow is from ground through R3, diode CR3, and RI to the supply. Thus, output F is equal to the supply voltage minus the drop across R1, and the small drop through the diode, or approximately +V volts, a logic 1. Meanwhile, inputs C and D are inactive at zero volts, and diodes CR4 and CR5 conduct because of the high positive anode potential. The current flow through R2 drops the supply voltage to zero, with respect to ground, at the anode of diode CR6 (the OR gate). With the cathode of CR6 connected to ground through R3, no potential exists across the diode, it is reverse biased by the positive output voltage across R3, therefore CR6 does not conduct.

Assume now, that conditions are reversed, that is, inputs C and D are activated by a positive voltage, and inputs A and B are inactive at zero volts, this is combination number 4 in the table above. OR gate

d

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diode CR6 now conducts, while CR3 remains nonconducting, and the output at F is again at +V volts, and produces a logic 1 while in this active state. It is evident from the table of combinations, above, that if each of the input combinations is performed, only combinations number 4, 8, 12, 13, 14, 15, and 16 will cause an active (high) output to be produced at F.

The schematic representation of the circuit described above is shown in the accompanying illustration. While this drawing and the matrix representation are identical, the arrangement is slightly different. Thus the schematic representation shows the more familiar AND and OR gate arrangements at a glance, However, the matrix drawing is usually used for matrices because it essentially conforms to the physical and wiring arrangement of the matrice, and it is clearer and easier to follow signal path flow when a large number of cascaded circuits are used. Both circuits are identical, however, so you may use whichever seems easier to follow or understand. The circuit explanation is applicable to both drawings. To fully understand operation of this circuit, you should apply each input condition shown in the table of combinations and verify that an identical result is obtained. Once established, the truth table makes it necessary to know how the circuit operates in determining a particular result. If the inputs are known, then the output can be determined at a glance.



Schematic Circuit

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# **ENCODING MATRICES**

# Application.

Encoding matrices (matrix) are used to change data from one form into another. For example, the conversion of conventional decimal or english notation into a form usable in a digital computer. The decimal numbers, letters, and punctuation marks are converted to binary form for use in the digital computer.

# Characteristics.

Consists of many input lines, but only a few output lines.

Only one input line is activated at a time to produce a unique output.

May use positive or negative logic, or combined logic,

Gain is less than 1 (no amplification is provided).

The matrix may be arranged in any suitable geometric form (rectangular, square, pyramid etc.).

## **Circuit Analysis.**

**General.** A decimal-to-binary encoder matrice changes a voltage level which represents a specific decimal number into a unique set of voltage levels representing the binary form of the decimal number. The following table shows decimal numbers from O through 9 with their binary equivrdents.

DECIMAL NUMBER	BI	NARY	NUMB	ER
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Note that the decimal digit requires four binary digits (or bits) to represent it. Therefore, the circuit which performs the decimal to binary encoding must have 10 input lines, one for each decimal digit input, and 4 output lines, one for each binary output.

**Circuit Operation.** The logic diagram for a typical decimal-to-binary encoder is shown in the following illustration.



#### Decimal to Binary Encoder Logic Diagram

Examination of the logic diagram reveals that four OR gates are employed. OR gate number 1 has three inputs and one output. OR gates numbers 2 and 3 have five inputs and one output, and OR gate number 4 has six inputs with one output. The open triangles indicate that negative logic is used. Therefore, a logic O (inactive state) is represented by a relatively high voltage level (H), while logic 1 (the active state) is represented by a relatively low voltage level (L).

The following table of combinations shows the specific decimal number input and level, and the unique output level for each of the inputs.

INPUT	ι Ουτρυτ				
F	А	В	С	D	
0	L	L	L	L	
1	н	н	н	L	
2	н	н	L	н	
3	н	н	L	L	
4	н	L	ΗI	i	
5	н	L	н	L	
6	н	L	L	н	
7	н	L	L	L	
В	L	н	ΗI	- 1	
9	l L	н	н	L	

Table of Combinations (Truth Table)

Examination of the table of combination reveals that the listed gate output is activated when the input is the decimal number(s) shown in the following matrix truth table; note that the number of inputs correspond to those shown on the logic diagram.

> A = 0,8,9 8 ° 0,4,5,6,7 C = 0,2, 3,6,7 D = 0, 1,3,5,7,9

The following illustration shows the complete matrix schematic representation of the encoder.



Matrix Representation

Examination of the matrix schematic reveals that OR gate number 1 (output A) consists of diodes CR1 through CR3, with current limiting resistor R1. OR gate number 2 (output B) consists of diodes CR4 through CR8, with current limiting resistor R2. OR gate number 3 (output C) consists of diodes CR9 through CR13, with current limiting resistor R3. And OR gate number 4 (output D) consists of diodes CR14 through CR19, with current limiting resistor R4. As shown in the schematic, the anodes of all diodes are connected to a positive bias supply through the current limiting resistors. When their

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cathodes are connected to a less positive voltage, or placed at zero (ground) potential they will conduct. When left unterminated (no input) the circuit from the supply through the diode to ground is open, and no conduction occurs. When no conduction occurs, no current flows through the associated current limiting resistor and the gate output is +V, the supply voltage. Since negative logic is employed, a positive (relatively high) output represents a O and the circuit is then considered inactive. When a zero voltage (negative or relatively low) input is applied, all diodes on this line will conduct. The normally high (positive) output will be dropped to zero by the current flowing through the associated current limiting resistor, thus zero voltage or no output represents a 1, that is, an active negative output.

For example, assume the decimal number 7 is applied by grounding that input line (a relatively low (L) input is applied). The cathodes of diodes CR8, CR13, and CR18 are, therefore, more negative than their anodes, and these diodes will conduct. Thus at gate outputs B, C, and D, no voltage will appear, and these OR gates will all be at a relatively low (L) output. At the same time, since gate A output is not connected to line 7 it will remain highly positive at +V volts creating a relatively high (H) output. Thus by activating the number 7 line (through grounding it) the output will be HLLL, representing the binary number 0111 or the decimal number 7. By following the table of combinations, number for number, in a similar fashion and applying each input in turn, the outputs shown in the table of combinations will be obtained. Only one decimal number input at a time is permitted, with all the remaining lines resting in the inactive state. If two or more input ines were simultaneously activated, one of the numbers might be produced correctly and the others masked out, or else the wrong number would be produced. Thus in an encoder of this type a series input must be used, since a parallel input would produce a false indication. Conversely, the decoder which works just the opposite, requires a parallel input. Thus the coding time for a series of decimal digits in a simple computer represents a finite time, since only one can be produced at a time. However, the operating time for each digit is only a few microseconds, so that the coding is usually accomplished as fast as the information can be inserted, and appears to be instantaneous.

While the above explanation assumes the use of d-c voltage levels, the same action can be obtained with

pulses using appropriate coupling circuits, when needed. Because of the inherent loss in the diode (although assumed zero for ease of discussion in these paragraphs), when large numbers of diodes are used, considerable power is required. Thus diode logic is usually used together with transistors, and diodetransistor logic (DTL) circuits are used in large computers.

# **DECODING MATRICES**

# Application,

**Decoding** matrices (matrix) are used to change data from machine (computer) language to ordinary decimal or english notation. The binary representation of a decimal or an english character (machine language) is automatically converted by the matrix into a straight-forward reading character or digit easily recognized by the reader.

## Characteristics.

Consists of many input lines, and many more output lines.

Several inputs are activated simultaneously to produce a unique output.

May use positive or negative logic, or combined logic.

Gain is less than 1 (no amplification is provided).

The matrix may be arranged in any suitable geometric form (rectangular, square etc.).

# Circuit Analysis.

**General.** A binary-to-decimal decoder matrice changes a unique set of input voltage levels representing a binary number into an output which represents a single decimal number. The following table shows binary numbers from O through 9, with their decimal equivalents.

BIN	BINARY NUMBER		IBER	DECIMAL NUMBER	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	9	

Note that each decimal digit requires four binary digits (bits) to represent it. Thus this type of decoder is sometimes called a "many-to-one" decoder, since many inputs are converted to a single output. To perform the binary decoding 8 inputs are required (four inputs for binary 1's and four inputs for their complement, binary O), with 10 outputs representing the decimals from O through 9.

**Circuit Operation.** A logic diagram for a typical binary-to-decimal decoder is shown in the accompanying illustration.

**ELECTRONIC CIRCUITS** 



Binary-to-Decimal Decoder Logic Diagram

Examination of the logic diagram shows that 1O-AND gates having 4-inputs and four diodes in each gate (AGO through AG9) are used. The closed triangles indicate that positive logic is employed. Therefore, the inactive state (a logic O) is represented by a relatively low voltage level (L), while the active state (a logic 1) is represented by a relatively high level (H). Thus, in the inactive state, logic O represents an (L) condition at inputs A, B, C, and D, and an (H) condition at inputs  $\dot{A}$ ,  $\vec{B}$ ,  $\vec{C}$ , and  $\vec{D}$ .

The following table of combinations shows the various binary input levels and the unique output level for each of the possible input combinations.

	BINARY	INP	UT I	DECIMAL	OUTPUT
Α	В	С	D	F	
L	L	L	L	н	(0)
L	L	L	н	н	(1)
L	L	н	L	н	(2)
L	L	н	н	н	(3)
L	н	L	L	Н	(4)
L	н	L	н	Н	(5)
L	н	н	L	Н	(6)
L	н	н	н	Н	(7)
н	L	L	L	Н	(8)
н	L	L	н	Н	(9)
			•		

**Table of Combinations** 

Examination of AG8 reveals that in the inactive condition, three of its inputs are in the (H) condition (inputs B, C, and  $\overline{D}$ ); only the fourth input to AG8 (input A) need be activated to produce an output decimal number 8. While the gate that is activated for each binary input is shown by the preceding table of combinations, if it is converted into a Truth Table by substituting the O and 1's corresponding to the decimal number as shown in the following table, operation becomes easier to follow. It is also evident that this is the same as the binary-decimal equivalent numbers previously listed. When the gates are activated it is by means of a logic 1 signal. In the logic zero state the gate remains inactivated. When the gate input is activated, the input signal stops the associated gate diodes from conducting, and an output is produced as the output level rises to the +V supply voltage. When the gate input is inactivated, the cathode of the associated diode is at a lower potential than the anode and the diode conducts. The current flow through the associated current limiting resistor drops the supply voltage to zero so that no output is obtained. Thus when input A is activated a positive voltage is applied to block off or reverse bias any diodes connected to that line. When  $\overline{A}$  (A-bar) is activated it is a "NOT A"; thus, it is not a logic 1 but a logic O, and all the diodes associated with that line conduct because of the forward bias applied by the relatively-low (L) input signal.

BINARY		NUMBER		DECIMAL NUMBER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

This operation may be followed more easily if the accompanying matrix schematic is examined in conjunction with the truth table inputs as the discussion continues.



Decoder Matrix Schematic

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For example, assume that inputs B and D are active (H) and  $\overline{A}$  and  $\overline{C}$  are inactive (therefore also high (H)); this places a +V volts (H) at each of the four inputs to AG8. The truth table shows that the corresponding combination 0101 must activate gate number 5 and produce a high positive output. Examination of the matrix schematic shows that gate 5 consists of CR21 through CR24 with current limiting resistor R5. When input line A is inactive (H), diode CR21 ceases conduction; likewise, as B,  $\overline{C}$  and D, respectively, are also made high the diodes CR22, CR23, and CR24 are also reverse biased. Thus all the diodes of AND gate 5 stop conduction simultaneously, and output F which is assigned the decimal number 5 rises to the supply voltage level creating a positive output pulse, as required by the table. Note that if any one of these inputs were not high (H), but were low (L) instead, then that one diode would conduct and the high output could not occur. Thus one, and only one particular combination will activate each of the AND gates. To prove this, examine each of the input lines which are at a relatively low value. We find, then, that line A forward biases diodes CR33 and CR37 and decimrd outputs 8 and 9 are, therefore, at zero. Likewise, for input line **B** diodes CR2, CR6, CR1O, and CR14 conduct and outputs O, 1, 2, and 3 are low or zero. For line C diodesCR11, CR15, CR27, and CR31 conduct so that outputs 2,3, 6, and 7 are zero. Finally, input **D** causes conduction of diodes CR4, CR12, CR20, CR28, and CR36, with outputs O, 2, 4, 6, and 8 at zero. Thus, while gate 5 is high, all the other outputs are low or zero since at least one of the associated diodes is conducting. Sometimes two or more diodes will be conducting, but only one is necessary to prevent the gate from operating, and producing an output.

If you follow the truth table combinations, applying high and low inputs as indicated and noting the output, or lack of output, you will see that the truth table shows the proper combination for the desired output, and no other combination will produce the same results.

### TWO-LEVEL AND-OR GATE

## Application.

Combinations of AND-OR gates which form a two-level logic circuit can be used to apply the out-

puts of two or more logic circuits to the input of another logic circuit to produce logic addition, subtraction and other functional operations.

#### Characteristics.

May use positive or negative logic, or combined logic.

Has not less than four inputs for one output, and may have six or eight inputs with only one output, if desired.

The actual input levels may be different, however, the outputs are always at the same level.

Output never exceed the input (no amplification is obtained).

## **Circuit Analysis.**

General. Two-level logic circuits have two basic input circuits and a single output circuit. The input circuits may have a number of input lines, each controlled by a diode, but there is only one output line. Thus it is common practice to make the input circuits AND gates, and the output circuit an OR gate. Although this logic may be changed to exactly the opposite by applying negative logic inputs. Thus, the AND gates become OR gates, and the OR gate becomes an AND gate without changing any circuitry. This allows complete flexibility in combining logic operations, and, therefore, two-level logic circuits are universally used throughout computers. The logic diagram for a combination of two positive AND gates, and a positive OR gate is shown in the following illustration.



Two-Level Positive AND-OR Gate

**Circuit Operation.** The schematic for a typical two-level AND-OR gate is shown in the following

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illustration. Although only two inputs are shown for each branch circuit for ease of discussion, a large number of inputs may be accommodated.



**Two-Level AND-OR Gate Schematic** 

It is evident from the schematic that AND gate number 1(AG1) is identical to AG2. Two different inputs are applied to each AND gate. The **output** of the AND gates are applied through CR3 and CR6, and are summed across R2. A table of combinations shows that the following truth table is applicable, where O is ground or zero level, and 1 is a +5.

INPUTS					OUTPUT
A	В	С	D		s
0	0	0	0		0
0	1	0	1		0
1	0	1	0		0
1	1	1	1		1

**Truth Table** 

Thus with no input applied, diodes CR1, CR2 and CR4, CR5 conduct since they are forward biased, and the voltage across RI and R3 is dropped to zero. OR

diodes CR3 and CR6 are also conducting (anode is more positive than cathode) so that this output is also zero. When either A or B, or C or D is made a 1 (by applying plus 5 volts) the associated diode is reversebiased and stops conducting. However, circuit operation remains unaffected since the other diode of the pair still conducts and holds the gate in the zero state. However, whenever both inputs are applied simultaneously to either AND gate, both diodes are reverse biased, conduction ceases, and the voltage at the bottom end of R1 or R3 is the same as the supply, if the reverse bias is equal to or greater than the supply. If the reverse bias is only a portion of the supply voltage, (as is the case) conduction above that level holds the output at the value of the reverse bias. Thus with a 10 volt supply and a 5-volt reverse bias, the output is +5 volts. This output of the AND gate when applied to the OR gate passes through either CR3 or CR6 and appears as the output sum (AB + CD). When +5 volts appears at the output the inactive OR diode is reverse-biased by that same amount, so that the other AND output has no effect. That is the exclusive OR function is represented, where either one or the other (AG1 or AG2) appears but not both. In this respect, the truth table appears erroneous. However, it is just the manner in which it is arranged. Thus this circuit is sometimes called a onequarter adder, since it only represents the sum of two digits. When another AND gate is added to indicate the carry where both OR gate inputs are present simultaneously, the circuit then is known as a half-adder (discussed separately later in this section of the Handbook).

# HALF-ADDER CIRCUITS

## Application.

Half-adders are used to form the sum of two incident binary digits. "They are used as the basic circuit for a full-adder (two half-adders make a **full**adder). Thus full binary adding networks used in computers consist of a number of half-adders, and associated circuitry.

# Characteristics.

May use either positive or negative logic, or combined logic. Usually has four input lines with two output lines. Consists of three AND gates and one OR gate. Gain is less than 1 (no amplification is provided.)

Circuit Analysis.

**General.** Since the half-adder performs binary (arithmetic) addition it is necessary that its output be identical to the results of the binary addition table as follows:

A + B	0 0	0 1	1 0	ı 1
SUM	0	1	1	0
CARRY	O	0	0	1

We see from the table that two outputs are needed, since there is a carry of 1 when two 1's are added. It is evident that to add three binary numbers another carry output is needed. Hence to add more than two binary bits it is necessary to employ more than one half adder so that full-adders (consisting of two or more half-adders) are usually used in adder networks.

**Circuit Operation. A** typical half-adder is shown in the accompanying logic diagram.



Half-Adder Logic Diagram

**Examining the diagram we see that three twodiode** AND gates AG1, AG2, and AG3 are used, together with a single two-diode OR gate OG1. The logic equation at the output shows that the sum output (S) is high (H), and active whenever the two inputs A and B are unlike, and is inactive low (L) whenever the two inputs are alike. The output equation  $S = \overline{AB} + A\overline{B}$  is read as "A or B, but not both"; this is the **axclusive OR** function. The carry output is active and high (H) whenever the two inputs A and B are equal to binary l's, and is inactive low (L) for all other conditions. The following table of combinations shows the proper output for any particular input combination.

INPUTS		OUTPUTS		
Α	в	S	С	
L	L	L	L	
L	н	н	L	
н	L	н	L	
н	н	L	н	

# Table of Combinations For Half-Adder

When the table of combinations is converted into a truth table by substituting the O's and 1's, as shown in the following table, it is evident that it corresponds to the preceding binary addition table, and that the circuit is performing the desired function.

INPUTS		OUTPUTS		
Α	В	SUM	CARRY	
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	

### Half-Adder Truth Table

Circuit details are shown in the following matrix schematic (the half-adder may also be considered as a rectangular or square matrice).



Half Adder Matrix Diagram

Examination of the matrix diagram reveals that AND gate number 1 consists of diodes CRI and CR2 with current limiting resistor RI; AND gate number 2 consists of diodes CR3 and CR4, with current limiting resistor R2, and the carry gate is AND gate number 3 with diodes CR7 and CR8, and current limiting resistor R3. The OR gate consists of diodes CR5 and CR6, with current limiting resistor R4. Zero volts represents logic O (L), and +V volts represents logic 1 (H).

Assume that inputs A and B are logic l's, thus their input line is at a high level (H). Therefore, associated diodes, CR3, CR7 on line A, and CR2, CR8 on line B are reverse-biased and will stop conduction. Thus output C of AND gate number 3 (the carry gate) will rise to +V volts and also be at a high level, which is the output expressed by the formula C=AB. With inputs A and B high, their complement inputs  $\overline{A}$ and  $\overline{B}$  (NOT A and NOT B) are low, causing diodes CR1 and CR4 to conduct. Therefore, OR gate diodes CR5 and CR6 will not conduct, since the potential at the anode end of R1 and R2 will be zero, and with the diode cathodes connected to ground through R4 no potential exists across these diodes. Thus there is no output from the S output line, and it is a logic O.

In a similar manner, it is evident that for the sum output (S) to be high (H), inputs  $\overline{AB}$  or  $A\overline{B}$  but not both must be a logic l(H). For these conditions, either diode CR7 or diode CR8 is held inoperative by reverse bias from the logic 1 input, while the other diode conducts because of the lack of an input (both diodes must be reverse biased to produce an output). Therefore, carry output, C, remains inactive and low or a logic O. By following the table of combinations (or truth table) for each input condition, and by using the matrix diagram to determine which diodes are activated and which are not, you can verify operation of the circuit against each unique output listed in the table. Normally, when inputs A and B are alike, the sum output is always O(L), and when unlike it is always l(H). The carry output, C, is always O (low) except when both A and B inputs are high (1), in which case it is also high (H), and a logic 1.

# FULL ADDER

#### Application.

The full-adder is used in digital computers to add two or more digital characters containing any combination of bits. The full adder may be a specially designed circuit or it may be formed from two or more half adders.

### Characteristics.

May use either positive or negative logic, or combined logic.

Consists of four inhibit gates, three OR gates, and - two AND gates.

Has three input lines and two output lines.

#### Circuit Analysis.

**General.** The full-adder performs the binary addition of two characters that can not be added by a single half adder. The conventional adder consists of two half adders and an OR gate. The first half-adder combines the augend and addend of the applied characters, and the second half-adder combines the resulting sum of the first half-adder and any carry pulses received from other full-adders. The sum output from the second adder is the sum output of the

**ELECTRONIC CIRCUITS** 

full-adder. The separate OR gate receives carry pulses from each half-adder to produce a carry pulse for application to other full-adders.

Each full-adder is connected in a series, or a parallel, or a series-parallel arrangement, to produce the true sum of the applied digits or bits by the most desirable mode of operation. If the adder is connected in series it is necessary to use more than one full-adder, but if the adder is connected in parallel, a single full-adder plus additional elements are used to produce a true sum. The following figure is a typical example of binary addition showing the resultant binary sum that is produced from a binary augend and binary addend.

Addend	1101
Augend	1011
Sum	0110
Carry	1001

**Circuit Operation.** A typical full-adder is shown in the following logic diagram. The circuit consists of four inhibit gates, two AND gates and three OR gates. Each gate is identified by a number for ease of explanation. Since the full-adder provides for the application of a carry pulse as well as the addend and the



#### Full-Adder Logic Diagram

augend pulses, the logic equations for the sum and carry outputs of the full-adder (as shown in the logic

diagram) become more involved than the sum and carry equations for the half-adder. The following table of combinations shows the proper output for any combination of inputs.

Α	В	C <sub>in</sub>	s	c out
L	L	L	L	L
L	L	Н	н	L
L	н	L	Н	L
н	L	L	н	L
L	н	Н	L	н
н	L	Н	L	н
н	н	L	L	н
н	н	Н	н	н

# **Table of Combinations**

**A** truth table that corresponds to the table of combinations is shown in the following table.

Α	В	C in	s	<sup>c</sup> out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
0	1	1	0	1
1	1	0	0	1
1	1	1	1	1

## **Truth Table**

The schematic representation of a diode full-adder is shown in the following illustration. The three inputs to the adder are labeled A, B, and C<sub>in</sub>; the two outputs are labeled S and Cout. Diodes contained in the full-adder inhibit gates are: CRI, CR2, CR3, CR4, CR9, CR10, CR11 and CR12. Resistors Rl, R2, R3, R4, R5, R7, R9 and RIO are inhibit gate load resistors, Transformers T1, T2, T3 and T4, consisting of coils L1 through L8, provide inversion of pulses applied to the inhibiting input of the inhibit gates. Diodes CR5, CR6, CR7, CR8, CR17 and CR18 make up the OR gates of the full-adder; resistors R6, R8, and R13 are associated OR gate load resistors. Diodes CR13, CR14, CR15, and CR16 make up the AND gates; resistors R11 and R12 are associated AND gate load resistors.



**Full-Adder** 

The diode full-adder shown in the schematic, operates with positive logic; that is, positive pulses must be applied to the full-adder inputs to produce any circuit response. A positive pulse, then, represents a logic 1, and a negative pulse (or lack of a pulse) represents a logic O. Assume that a logic character of 101 is applied sequentially to the full-adder A input, while a logic character of 110 is applied sequentially to the full-adder C<sub>in</sub> input. The first augend bit (first bit of the character applied to input A) is then a positive pulse; the first addend bit (first bit of the character applied to input B) is a

negative pulse (or lack of a pulse) and the **first** carry input bit (first bit of the character applied to input  $C_{in}$ ) is likewise a negative pulse (or lack of a pulse). The positive augend bit is applied to primary L1 of transformer T1 which induces a corresponding negative voltage in secondary L2 of T1. This negative pulse causes inhibit gate diode CR1 to conduct at a greater rate, causing greater current to flow through inhibit gate load resistor R1 and a larger voltage drop across R 1. The anode end of resistor R1 then becomes negative. The positive augend bit **also** appears at the cathode of inhibit gate diode CR10. In this case, the positive input pulse cancels the effect of
the negative supply voltage applied through resistor R9 to the cathode of CR1O. Since a negative input is applied to input B and inverted by T3, diode CR9 is reverse biased and does not conduct. There is now no current flowing through inhibit gate load resistor R5, and likewise no voltage drop across resistor R5. The voltage at the anode end of R5 is the value of the positive supply voltage. The positive augend bit also appears at the cathode of AND gate diode CR13, canceling the negative supply voltage applied to the cathode, and preventing diode CR13 from conducting. AND gate diode CR14, however, remains conducting because of the forward bias supplied by the negative voltage applied to the cathode of CR14 and the positive voltage applied to the anode of CR14. Current flows through AND gate load resistor R11, producing a voltage drop across R11 which makes the anode end of R 11 negative. This negative voltage represents a logic O first half-adder carry output.

The negative voltage previously produced at the anode end of R1 appears at the anode of first halfadder sum output OR gate diode CR5. Since a diode w-ill not conduct if a negative voltage is applied to reverse bias the anode, CR5 does not conduct. The positive voltage produced at the anode end of inhibit gate load resistor R5, also appears at the anode of OR gate diode CR6. With a positive voltage appearing on the anode of CR6 from the inhibited B input, CR6 conducts, causing current flow through OR gate load resistor R6 and produces a voltage drop across the resistor. The voltage at the cathode end of R6 is positive. This is the sum output (S1) of the first halfadder.

The carry input pulse ( $C_{in}$  which is a logic O, is the augend input of the second half-adder. The sum output of the first half-adder, which is a logic 1, is the addend **input** of the second half-adder. This logic 1 pulse appears simultaneously at the cathode of inhibit gate diode CR4, at primary coil L7 of transformer T4, and at the cathode of AND gate diode CR15. The positive pulse appearing at the cathode of CR4 provides a reverse bias which prevents diode CR4 from conducting, and prevents voltage from being developed across load resistor R2. Hence, the anode end of resistor R2 rises to the positive supply voltage value. The positive pulse applied through primary coil L7 of transformer T4 induces a negative pulse into secondary coil L8. This negative pulse then appears at

the cathode of inhibit gate diode CR11, causing CR11 to conduct more heavily, and increasing the flowing through load resistor R7. An increased voltage drop appears across resistor R7, making the anode end of R7 negative. The negative voltage appears at the anode of second half-adder sum output OR gate diode CR8. The positive voltage previously produced at the anode end of resistor R2 simultaneously appears at the anode of output OR gate diode CR7. Although diode CR8 does not conduct, diode CR7 does conduct, causing current to flow through the full-adder sum output OR gate load resistor R8 and develop a voltage drop across R8, which leaves the cathode end of R8 positive. This positive (logic 1) pulse is the sum output of the second half-adder (S) for the duration of the first bit.

The (logic 1) positive addend pulse appears at the cathode of second half-adder carry AND gate diode CR15, preventing diode CR15 from conducting. Second half-adder carry output AND gate diode CR16 conducts, however, because of the negative voltage at the cathode of CR16 and the positive voltage applied to the anode of CR16 through the AND gate load resistor R12. As a result, current flows through load resistor R12 and the voltage drops across resistor RI 2, leaving the anode end of resistor R12 at zero voltage. This zero voltage appears at the anode of carry output AND gate diode CR17. Due to the lack of previous carry, the zero voltage produced at the anode end of resistor R1 1, appears at the anode of carry output AND gate diode CR18. Neither diode CR17 nor diode CR18 conduct because of the negative voltage (or lack of positive voltage) at their anodes. No current flows through load resistor R13 and no voltage drop appears across R13. The voltage at the cathode end of RI 3 is the applied negative voltage value; the carry output of the full-adder is then a logic O for the duration of the first logic bit.

The second augend bit (A input) is a logic O; the second addend bit (B input) is a logic 1, and the second carry input bit ( $C_{in}$  input) is a logic 1. The logic 1 bit or positive pulse applied to the B input appears at the cathode of inhibit gate diode CR2 and coil L5 of transformer T3. At the cathode of CR2, the positive pulse prevents CR2 from conducting, preventing current from flowing through load resistor R1, and preventing any voltage dropping across resistor R1. The anode end of resistor R1 is then at the same potential as the positive supply voltage applied

to resistor R1. At primary coil L5, the positive voltage pulse causes a negative pulse to be induced into secondary coil L6, of transformer T3. The negative pulse appears at the cathode of inhibit gate diode CR9, causing CR9 to conduct more heavily and in increased current flows through load resistor R5. The voltage drop across R5 is increased making the anode end of resistor R5 negative.

The logic 1 bit or positive pulse applied to the B input also appears at the cathode of first half-adder carry AND gate diode CR14, preventing diode CR14 from conducting. First half-adder carry output AND gate diode, CR13, still conducts, however, since a negative voltage is applied to the cathode of CR13 and a positive voltage is applied through the AND gate load resistor, RI 1, to the anode of CR13. The conducting of CR13 causes current to flow through load resistor RI 1 and the voltage to drop across RI 1. The anode end ofR11 remains at a zero or effectively negative potential. This negative potential represents a logic O carry output of the first half-adder.

The logic O (zero or negative voltage) pulse produced at the anode end of resistor R5 appears at the anode of first half-adder sum output OR gate diode CR6, and the logic 1 (positive pulse) produced at the anode end of resistor R1 appears at the anode of first half-adder sum output OR gate diode CR5. Diode CR6 does not conduct because of the negative voltage appearing at the anode of CR6; however, due to the positive potential on the anode of diode CR5 and the negative potential on its cathode, OR gate diode CR5 conducts. Current then flows through the OR gate load resistor, R6, producing a voltage drop across it. The cathode end of resistor R6 then swings positive. This positive potentird swing represents a logic 1 sum output of the first half-adder.

The logic 1 (positive) pulse applied to the  $C_{in}$  input is the augend of the second half-adder; the logic 1 (positive) **pulse** applied from the cathode end of R6, (the sum output of the **first** half-adder) is the addend of the second half-adder. Because of both inputs being positive, a positive pulse appears at each of the following points: primary coil L3 of transformer T2, the cathode of inhibit gate diode CR4, primary coil L7 of transformer T4, the cathode of inhibit gate diode CR12, the cathode of the second half-adder carry output AND gate diode, CR15, and the cathode of the second half-adder carry output AND gate diode CR16.

In both second half-adder inhibit gates, current is prevented from flowing through the non-inhibiting diodes of the inhibit gate (CR4 and CR12) by the positive voltage appearing at their cathodes. The positive voltage pulse appearing at the primary coils (L3 and L7) of transformers T2 and T4, however, causes negative voltage pulses to be induced into the secondary coils (IM and L8) of these transformers, placing a negative voltage on the cathodes of inhibit gate diodes CR3 and CR11. As a result, diodes CR3 and CR11 conduct, creating current flow through the diodes and their load resistors, R2 and R7. The current flow through the load resistors causes a voltage drop across them, leaving the anode ends of both load resistors at zero, producing a negative swing. This negative swing at the anode end of resistor R2 appears at the anode of second half-adder sum output OR gate diode CR7, and the negative swing produced at the anode end of resistor R7 appears at the anode of second half-adder sum output OR gate diode CR8. With either zero or a negative voltage appearing at the anodes of both diodes they are reverse biased, and neither diode conducts. As a result, no current flows through either diode or through the second half-adder sum output OR gate load resistor, R8, and no voltage drop appears across resistor R8. The voltage at the cathode end of resistor R8 is the negative supply voltage value. This negative voltage represents a logic O sum output of the second half-adder and the total sum of the full adder during the duration of the second bit.

The positive (logic 1) pulse appearing at the cathodes of each of the second half-adder carry output AND gate diodes CR15 and CR16, reverse biases the diodes. Hence, no current flows through either diode, or the AND gate load resistor R12, and no voltage drop appears across resistor R12. The voltage at the anode end of resistor R12 is the vahre of the positive supply voltage. This voltage appears at the anode of full-adder carry output OR gate diode CR17. The logic O (negative) pulse produced at the anode end of tirst half-adder carry output load resistor R11 appears at the anode of the other full adder carry output OR gate diode, CR18. The logic O pulse at the anode of CR18 has no effect, but the logic 1 (positive) pulse at the anode of CR17 causes current to flow through diode CR17 and load resistor R13, developing a positive voltage drop across resistor R13. The resulting positive voltage at the cathode end

of resistor RI 3 represents a logic 1 full-adder carry output for the second bit time period.

The third augend bit (A input) is a logic 1; the third addend bit (B input) is a logic 1, and the **third** carry input bit ( $C_a$  input) is a logic O. Because both augend and addend inputs are positive, a positive pulse appears at each of the following points: primary coil **L1** of transformer T1, the cathode of inhibit gate diode CR2, primary coil L5 of transformer T3, the cathode of inhibit gate diode CR10, the cathode of **first** half-adder carry output AND gate diode CR13, and the cathode of **first** half-adder carry output AND gate diode CR14.

In both first half-adder inhibit gates, current is prevented from flowing through the non-inhibiting diodes of the inhibit gate (CR2 and CR1O) by the positive pulse appearing at their cathodes. The positive voltage pulse appearing at the primary coils (Ll and L5) of transformers T1 and T3, however, causes negative voltage pulses to be induced into the secondary coils (L2 and L6) of these transformers, placing a negative voltage on the cathodes of inhibit gate diodes CR1 and CR9 and they conduct. Thus current flows through the diodes and associated load resistors, RI and R5. The current flow through the load resistors produces a voltage drop across them, leaving the anode end of both load resistors zero or effectively negative. The effective negative pulse voltage at the anode end of resistor R1 appears at the anode of first half-adder sum output OR gate diode CR5, and the effective negative puke voltage at the anode end of resistor R5 appears at the anode of first half-adder sum output OR gate diode CR6. With the effective negative pulse voltage at the anodes of both diodes they are reverse biased, and neither diode conducts. Therefore, no current flows through either diode, or through first half-adder sum output OR gate load resistor R6, and no voltage drop appears across resistor R6. The voltage at the cathode end of load resistor R6 is the negative supply voltage value. This negative voltage represents a logic O sum output of the first half-adder.

The third positive bit (logic 1) pulse appearing at the cathodes of each of the first half-adder carry output AND gate diodes CR13 and CR14, reverse biases the diodes. This prevents current flow through either diode, or AND gate load resistor RI 1, and no voltage drop appears across resistor RI 1. The voltage at the anode end of resistor R1 1 is the value of the positive supply voltage. This positive voltage represents a logic 1 first half-adder carry output.

The third logic O (negative or zero) pulse applied to the  $C_{in}$  input is the augend of the second halfadder; the logic O (negative or zero) pulse applied from the cathode end of R6 (the sum output of the **first** half-adder) is the addend of the second halfadder. Since both addend and augend bits applied to the second half adder are a logic O, there is no circuit action in the second hrdf-adder. The second halfadder produces a logic O sum output, which is the output for the full adder during the time that the third sequence of bits is applied. For the same reason, there is a logic O carry output for the second half-adder during the time that the third sequence of bits is applied.

The logic 1 (positive) pulse output of the first halfadder carry output appears at the anode of full-adder carry output OR gate diode CR18, while the logic O (positive) pulse output of the second half-adder carry output appears at the anode of full-adder carry output OR gate diode CR17. Diode CR17 does not conduct because there is no positive voltage on the anode. (Diodes CR15 and CRI 6 conduct and drop the voltage across R12 to zero). The positive carry pulse voltage applied to the anode of diode CR18 causes CR18 to conduct, producing a current through the diode and load resistor R13. This voltage drop appears across resistor R13, making the cathode end of resistor R13 swing positive. This positive voltage swing represents a logic 1 full-adder carry output at the time that the third sequence of bits is applied.

When it is necessary to obtain the true sum from a single full-adder stage, a delay line is placed after the  $C_{out}$  output. The delay line moves each digit of the carry output one significant place to the left to establish the correct time relationship for the sum of the S output and the  $C_{out}$  output.

# PART 16-3. TRANSISTOR LOGIC

## TRANSISTOR LOGIC (GENERAL)

Like the diode, the transistor may be employed in logic circuits. While some of the basic circuits such as the AND and the OR circuit perform the same operation as in diode logic, numerous advantages are obtained, and in addition, circuits not possible with diodes can be utilized, such as NAND, NOR, and similar not operations. The additional element in the transistor provides the ability to provide an inherent inversion similar to that normally obtained in the electron tube. Of much greater importance, however, are the improvement in operating speed possible with the transistor, plus the possibility of obtaining a gain through the circuit. For stages that require a heavy current output for operating relays and other electronic devices the transistor emitter-follower connection provides power output with reduced gain. Because of the high input and output impedances possible with the transistor, the shunting effect of parallel inputs or outputs is not as great a problem as it is with diodes. Thus an entire new field of logic circuits and application was open by the use of transistors. In turn, other new circuitry was developed by combining diode and transistor logic (DTL), or by using direct coupling (DCTL). Basic circuits using transistor logic, DTL, DCTL, and RTL (resistortransistor logic), will be discussed in this Section of the Handbook.

## OR GATE

## Application.

The transistor "OR" gate is used in applications where an output gate is desired with the presence of a pulse at only one (or more) of its inputs.

# Characteristics.

May use positive, negative, or combined logic. Provides additional gain.

May be either single transistor or multiple transistor type (multiple type provides a transistor for each input).

## Circuit Analysis.

General. There are many types of transistor OR gates. When the common-emitter configuration is used, the circuit usually becomes a NOR circuit because of the polarity inversion. The commoncollector configuration has the same polarity at input and output, but falls within the class of Emitter-Follower circuits which are separately discussed. Thus the common-base connected OR circuit is the only remaining circuit which does not fall within another circuit classification and has the same polarity output as input. Consequently, the following discussion mainly concerns the common-base circuit, though other representative OR circuits may be briefly shown for completeness. It should be realized that in logic operations identical logic circuits have many forms which vary with design. For example, where one designer may use a single transistor OR gate to perform logic addition, another designer may use three or four transistors to accomplish the same purpose. This is why the logic designer usually uses the block diagram type of logic diagram representation rather than the schematic, since the function performed denotes the type of circuit, while the parts and actual circuit connections or arrangement are of no consequence as long as the desired logic operation is performed.

The symbolic logic representation of a positive transistor OR circuit is shown in the following illustration, together with a table of combinations. When the values of O and 1 are substituted in the table of combinations for L and H, respectively it is recognized as a standard OR truth table. Thus it is clear that in logic notation and representation both the diode and the transistor OR circuits are identical (see discussion of Diode OR-Cate in this section of the \_ Handbook).



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The fdled-in triangle indicates high level operation or positive logic. With a positive signal representing 1, a positive output is obtained.

**Circuit Operation.** The schematic diagram of a typical two-input, positive, single-transistor OR-gate is shown in the following illustration.



#### Two-Input, Common-Base, Positive OR Gate

In the circuit shown, the emitter is left floating and reverse bias is applied to the collector. Therefore, with no signal applied either RI or R2, simulating a O, transistor Q1 rests in the cutoff condition, Collector current cannot flow (because of reverse collector bias) and the output voltage is the same as the collector supply voltage (-6 volts as shown on the waveform). When a +3-volt signal is applied either R1 or R2 simulating a 1, forward bias is applied to the emitter, and collector current flows through R3 producing a positive-going output. In this case it is assumed that the input voltage is sufficient to drop the collector potential to O, and a 6-volt positive output is obtained. When the input signal is removed, the transistor returns to its quiescent state, with no collector current flowing and the O level at -6 volts. There is, of course, a reverse current flow (Icbo) due to thermal effects inherent in transistor operation. However, this reverse current is so small (usually less than a few microampere) that it may be neglected. Since there is no signal inversion in the common base circuit, the output signed is an amplified replica of the input signal (except for distortion produced during turn-off). This circuit will not operate as a negative OR gate by reversing the polarity of the input signal since it is already at cutoff. The circuit is only slightly

affected when both OR signals are applied simultaneously (the case of the inclusive OR). In this instance, the application of both input signals merely increases the minority carriers released in the transistor and it takes Q1 longer to recover from the operating pulse, thus producing slightly longer output pulse than when individually triggered. Input resistors RI and R2 are large valued and are used to isolate the two inputs, since they are both connected to the same emitter.

**Circuit Variations. A** typical 3-transistor OR gate is shown for comparison in the accompanying illustration.



Three-Stage OR Gate

A study of the schematic reveals that the circuit arrangement is that of the emitter-follower, and that the three outputs are parallel comected using common load and bias resistor R<sub>E</sub>. In the O or inactive state a positive voltage is applied to the base of Q1, Q2, and Q3 and they rest in a cutoff state. When a 1 signal, consisting of a negative voltage is applied to any transistor, the base is forward biased and emitter current flows. The emitter current flow through  $R_{E}$ develops a negative output signrd, and the emitter resistor also determines maximum current flow in the triggered transistor. Once the input signal is removed, the stage again resumes its cutoff condition. An output trigger results when any of the inputs are energized or when all of the inputs are energized, simultaneously, representing inclusive OR function. Since a negative input produces a negative output, negative logic is employed.

## AND GATE

## Application.

The transistor "AND" gate is used in applications where an output gate is desired only when pukes are applied to rdl inputs at the same time.

## Characteristics.

May use either positive, negative, or combined logic.

Provides gain and higher speed than the diode "AND" gate.

Can consist of a single stage with multiple inputs, or a number of similar stages with separate inputs.

## **Circuit Analysis.**

General. The AND gate, like the OR gate previously discussed in this section of the Handbook, can consist of a single stage with multiple inputs, or a number of similar stages with separate inputs. The AND logic function requires that an output be produced only when all the inputs are applied simultaneously. No output is obtained for any other combination of inputs.

Circuit Operation. The logic diagram for a typical AND circuit using the common-base configuration is shown in the accompanying diagram, together with a truth table.





The open triangles indicate that negative logic is used, and the symbol for the transistor AND gate is the same as that for the diode AND gate. The truth table is recognized as a standard AND table, where an output only occurs when both inputs are applied simultaneously. The schematic for this negative ANDgate is shown in the accompanying figure.



# Negative Transistor AND-Gate Schematic, **Common-Base Circuit**

As shown in the schematic, transistor QI is forward biased by the positive voltage applied to the emitter. Thus with a reverse collector bias applied through R4, and a forward bias applied through R3, the transistor conducts heavily in the quiescent or inactive state, and the collector voltage is dropped to zero across load resistor R4. Thus, there is no output and a logic zero is represented. When an input signal such as a negative pulse or step-voltage is applied to either input A or B, but not to both, the forward bias is reduced. This slight reduction in bias changes the collector current very little so that the input still remains effectively at the zero output level. When the negative input is applied to both inputs simultaneously, twice the current produced by a single input flows through base resistor R3 and drops the forward base-bias to below the cutoff point. Collector current now ceases flowing through R4 and since the voltage drop across R4 is now zero, full reverse collector voltage appears at the collector, producing a negative output voltage. When the input signal ceases, collector current flow through R4 resumes, and again drops the collector voltage to zero. Thus, the output voltage rises and falls as both inputs rise and fall together.

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**Circuit Variations.** A typical schematic for a three-input AND-gate, using separate transistors for each input is shown in the accompanying illustration.



Three-Stage AND Gate

Examination of the schematic reveals that the emitter-follower connection is used, with the transistor outputs connected in parallel across a common load and bias (emitter) resistor. Since the emitters are connected to a positive bias voltage, forward bias causes each of the transistors to conduct. With no input applied, emitter current flow through resistor  $R_{\rm F}$  (because of forward biased emitter) drops the output voltage to zero. Thus, the emitter voltage is effectively reduced to zero level. When a "1" signal of say +5 volts is applied to either O1, O2, or O3 the transistor is reverse biased and ceases conduction, meanwhile, the other two transistors continue to conduct and keep the output at zero level. When all three inputs are applied simultaneously, current flow through them is reduced and the emitter voltage rises toward the bias supply, creating a positive output voltage. When the positive output voltage rises to +5volts, the emitter voltage is again at zero bias level and stays at this point until the input pulse ceases, whereupon once again heavy forward conduction causes the emitter voltage to be reduced to zero. Thus any positive input signal level less than the total emitter bias voltage, will effectively pass through the transistor(s) and appear as the output voltage (the actual output amplitude is a fractional amount less than the full amplitude of the input signal because of ohmic drop in the transistor, however, this drop is so low as to be considered negligible).

# NOT GATE

#### Application.

**The** transistor NOT gate is used in computer and high speed switching circuits to provide signal inversion and high gain.

## Characteristics.

Either positive, negative, or combined logic may be used.

Gain is possible.

Fixed-bias is usually employed.

Output signal is inverted in phase and polarity from input signal.

On a logic basis, the output is the complement of the input.

# Circuit Analysis.

**General.** When the common-emitter configuration is used, the output polarity is always inverted by inherent transistor action similar to the electron tube grounded cathode circuit. In logic operation it is sometimes desired to produce a signal which is identical but opposite that of the input signal. This is the logical NOT operation, and the circuit is also known as an inverter, which produces the complement of the input signal. This discussion will be limited to the use of a single stage operating as an inverter or NOT circuit. Other circuit variations will be discussed with the other circuits in which they are employed. The voltage gain obtained through this circuit also makes it useful as a level restorer.

**Circuit Operation. The logic representation of a** typical NOT (inverter) circuit is shown in the accompanying illustration.



The open triangle on the input side and the closed triangle on the output side indicate that with a negative input, an inverted or positive output is produced. The actual schematic of a typical inverter is shown in the following figure.



**Transistor NOT Gate** 

In the quiescent condition (the "O" state) with a positive base bias applied, transistor Q1 is at cutoff and no current flows (reverse collector current flow, Iceo, is considered negligible). Since no voltage drop to oppose the supply and the collector and output voltage fall to almost the value of the negative supply, representing a logic zero output. When a negative (1) input signal is applied, the base bias is changed from a reverse to a forward bias and causes emitter current to flow. Collector current flow through R3 drops the negative supply voltage to approximately zero so that a positive going output is developed. With sufficient forward base bias (drive) to cause saturation, the output rests at the zero voltage level until the input signal is terminated. When the input signal stops, the collector voltage does not change immediately because of the minority carriers inserted into the base during saturation (in the PNP transistor these are holes). Therefore, collector current flow continues for the duration of the storage delay time until the minority carriers are drained out, whereupon the collector voltage becomes negative-going and falls to approximately the same value as the supply voltage. The relationships between input pulse and rise and fall times (tr and tf) on the output pulse and storage

delay time (ts) are shown in the following waveforms. The output waveform is slightly exaggerated to clearly show the delayed and deformed pulse which is produced. Since the circuit function is merely that of on or off, the pulse distortion is of no consequence except for the slight delay in operating time which ensues. Resistors R1 and R2 function as a base bias divider, with R1 also acting as a base current isolating resistor, so that the base cannot be shorted by connecting the input to ground when producing a logic zero input. Rise time, tr, is also known as turn-on time and is defined as the period from the start of the square wave until it reaches 90 percent of steady state amplitude. The turn-on delay is caused by the finite time it takes the carriers produced by emitter action to travel to the collector. The fall time, tf, is also known as the turn-off time, and is the time which elapses from the start of the falling off period until it falls to within 10 percent of the final signal level. Storage relay time, ts, is defined as the time from the ending of the input pulse to the start of the trailing edge of the output pulse.



Input and Output Waveform Relationships

Fixed bias and large driving pulses are usually used to produce a sharp turn-on time, and other forms of logic such as DTL and RCTL are used to decrease the

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## LOGIC CIRCUITS

turn-off times. These circuit variations will be discussed in more detail with the appropriate logic and in the circuits in which they occur. Since the transistor design also determines the turn-on and turn-off characteristics, a special group of transistors of various types classified as "switching transistors" are employed to obtain greater speed and cleaner switching operation.

# NOR GATE

#### I NPuT OUTPUT INPUT OUTPUT Α в Ô ο 0 ١ . O (A + B) 0 I. 0 ٥ 1 0 0 NOR LOGIC OLAGRAM TRUTH TABLE

NOR Logic Diagrams

Truth Table

## Application.

The transistor NOR gate is used in computers and switching devices to supply an inverted OR (that is a complemented OR) output.

## Characteristics.

May use positive, negative, or combined logic. Usually uses fixed bias.

Provides an inverted or complemented output.

Has a high impedance and a low output impedance.

#### Circuit Analysis.

**General.** The NOR gate provides a standard OR output but in inverted or complemented form. Thus a NOT OR output is supplied from a single stage. Since the transistor common-emitter configuration produces an inverted output signal, it is only necessary to change the common-base OR circuit to a common-emitter arrangement to produce a NOR circuit.

**Circuit Operation.** The logic diagram for a typical NOR circuit and its associated truth table is shown in the following illustration.

The open triangles in the logic diagrams denote that negative logic is used. Thus the 1 -state requires a negative input signal for activation. Since the output is inverted in the NOR circuit, this is indicated by the small circle (in the upper diagram) adjacent to the triangular output level indicator. This indicates that with a negative input a positive output is obtained. The same condition could also be indicated by omitting the small circle and using a filled-in triangle at the output as shown in the lower (alternate) diagram. In this case the input and output levels are indicated as being different or inverted, and since the input is indicated as negative in the activated state by the open triangles, the logic is also negative. It should be noticed that the circle when used to express inversion must be located at the symbol. The small circles at the input and output terminals represent terminal connections and have no logic significance.

The schematic for a typical single stage transistor NOR circuit is shown in the accompanying illustration. Note that the PNP commonanitter configuration is used.



**PNP** Transistor NOR Gate

A positive (reverse) fixed bias is applied to the base to keep the transistor cut off in the inactive state. With logic "O" (in this case O volts) applied at inputs A and B, and reverse bias applied to the base and collector, no conduction occurs; therefore, the collector and output voltage is approximately the same as the collector supply voltage (in this case -6 volts), This output voltage represents a logic "1" at the output, verifying the first condition in the truth table.

When a negative input (logic "1") is applied to A or B, or to both A and B, it forward biases the base and causes collector current flow. The voltage drop caused by collector current flow through R4 reduces the collector voltage (and the output to zero). Thus a high input signal produces an inverted or low (positive) output signal. Resistors RI and R2 function as isolation resistors to prevent loading on the separate inputs A and B. Since the input resistors are connected in series with R3 to ground, they form a voltage divider which places the larger voltage across R3 and the base of Q1. Both R3 and either R1 or R2 also protect against shorting of the base bias or input circuit respectively, when a zero level input is applied. The high resistance of the input resistors requires that a relatively high voltage be used to cause base current

**to flow.** Hence, operation of this type is known as voltage mode operation. (In DCTL logic the resistors and bias are omitted and only a fraction of a volt input is necessary to drive the base into conduction, and this is called the current mode of operation.)

When both inputs are simultaneously applied, the larger negative input assumes control. When Q1 is driven into collector saturation by the activating signal, excess carriers are inserted into the base and the turn off time is extended by the storage time needed to drain the transistor of these excess holes. Because the full operating range of the transistor from cutoff to saturation is available, relatively high and power output can be obtained from this common+mitter arrangement.

# NAND GATE

## Application.

The transistor NAND gate is used in computers and switching devices to supply an inverted AND (a complemented AND) output.

## Characteristics.

May use positive, negative, or combined logic. Usually uses fixed bias.

Provides an inverted or complemented output.

Has a high input impedance, and a low output impedance.

#### Circuit Analysis.

**General.** The NAND gate provides a standard AND output but in inverted or complemented form. Thus a NOT AND output is supplied from a single stage. Since the transistor common-emitter configuration produces an inverted output signal, it is only necessary to change the common-base AND circuit to a **common-emitter** arrangement to produce a NAND circuit. This circuit is also sometimes referred to as a coincidence circuit or an all circuit in other publications.

**Circuit Operation.** The logic diagram for a typical NAND circuit, with its associated truth table is shown in the following illustration.



The closed triangles in the logic diagram indicate that positive logic is employed. **That is a** positive input signal represents an active 1. The inversion of output produced by the NAND **circuit is indicated by using an** open **triangle at the output, as** shown in the logic diagram.

The schematic of a two-input, single-stage transistor NAND gate is shown in the following illustration. Note that the common-emitter configuration is used.



**PNP Transistor NAND Gate** 

A negative, fixed base bias is applied to transistor Q1 to provide forward bias, and make the transistor conduct heavily in the so-called inactive state. With no input signal applied, and with forward base bias the transistor operates in the saturation region. Heavy collector current flow through R4 produces a voltage drop which reduces the negative collector voltage to zero. Since reverse collector bias is applied, a positive output is produced (absence of the input signal in this case represents a zero input). Thus the first

combination in the truth table is verified. When a positive (one) input signal is applied to either input A or B, but not both, the voltage developed across RI or R2 by base current flow is insufficient to stop conduction, and a zero or positive output still occurs. However, when the input signal is applied simultaneously to both A and B terminals, base current flow through R3 is twice that produced by single input signal, and, since it is in a direction which produces a polarity opposite to the forward base it cancels the bias, reducing it to zero. With no forward bias applied to the base and a reverse bias applied to the collector, transistor Q1 ceases conduction. With no collector current flow through R4, no voltage drop is produced, and the collector voltages falls to approximately the negative supply vahre. Thus a negative output is produced indicating a zero. Input resistor R1 and R2 act as isolating resistors for the separate AND inputs, and together with base resistor R3, preventing shorting of either the base or the bias when zero (grounded) input is applied. Since Q1 normally operates in the saturation region, excess carriers are inserted into the base, and the turnoff time is extended by the storage time needed to drain the transistor of these excess holes. Because the full operating range of the transistor from saturation to cutoff is available, relatively high gain and power output can be obtained from this common+vnitter arrangement.

# INHIBIT GATE

# Application.

The inhibit gate is used in digital computers to produce an output pulse when a signal is applied to one input, but not the other.

## Characteristics.

The inhibit gate uses a transistor NOT circuit to control a diode AND gate.

The circuit produces no amplification.

Uses PNP transistor.

Uses negative logic.

## Circuit Analysis.

**General.** An inhibit gate produces an output pulse if a signal is applied to only one of two possible inputs. If a signal is applied to the inhibit input, no

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output occurs. No output is produced since the inhibit input signal is inverted by the transistor, and cancels the effect of any signal supplied to the other AND gate input.

**Circuit Operation. The** schematic of a typical inhibit gate is shown in the accompanying illustration.



inhibit Gate

Diodes CR1 **and CR2** form a negative diode AND gate controlled by transistor NOT gate Q1. Resistors R1 and R3 form a base bias voltage divider. Resistor R4 is the collector load resistor for transistor Q1. Resistor R2 is the AND gate voltage dropping resistor from which the output is taken.

The following truth table indicates the desired output for the different input combinations. A "1" indicates the presence of a pulse and "0" indicates the lack of a pulse.

INPUT	INPUT	OUTPUT	
Α	В	F	
0	0	0	
1	0	1	
1	1	0	
0	1	0	
Truth Table			

In the quiescent or inactive state, with no inputs applied, diode CRI is forward-biased, and current flow through load resistor R2 drops the source voltage to zero. Thus, the output voltage is zero. At this time, transistor Q1 is reverse-biased by a positive bias voltage from a separate supply applied to the base of QI through R3. Hence, no current flows through Q 1 or collector load resistor R4 (reverse leakage current  $I_{CEO}$  is considered negligible). Consequently, Q1 has no effect on the output of AND gate diode CR2, since it is reverse-biased by the negative collector supply voltage applied to the anode.

When a negative input signal pulse is applied to input A (time  $t_1$ ), reverse bias is applied to the anode of CR1 and prevents any current tlow from source -V. Since no IR drop exists across R2, became of lack of current flow, the output end of R2 is at the full potential of the negative supply voltage. The output voltage remains negative until the negative input pulse ends at time  $t_2$ . From time  $t_2$  to  $t_3$  n o input is applied to A and the source voltage is dropped to zero across R2, producing no output. At time t<sub>3</sub>, a negative (inhibit) pulse is applied to input B, forward biases transistor Q], and emitter to collector current flows. Collector current flow through collector resistor R4 reduces the voltage at the collector of QI, and produces a positive swing. The positive voltage swing developed across R4 is applied to the anode of CR2 to forward-bias the diode. At time t3, another negative input pulse is also applied to input A. The positive pulse developed by the signal applied to input B, forward biases CR2, and causes the source voltage to drop across R2, producing an effective zero output voltage. Thus, there is no output voltage developed between times  $t_3$  and  $t_4$ . The only effective output that developed, is the negative output which occurs between times  $t_1$  and  $t_2$ , during the time that only a negative input pulse is applied to input A, and no input is applied to B.

# **DUAL** TYPE (AND-OR) GATE

# Application.

The dual type AND-OR gate is used in digital circuits to produce two outputs simultaneously; one

output is produced only when all input pulses are applied, and the other output is produced when any or all of the input **pulses** are applied.

# Characteristics.

Three inputs and two outputs are provided.

The circuit uses six PNP transistors.

Three transistors function as an OR gate.

Three transistors function as an AND gate.

Produces positive logic output for negative logic input.

## Circuit Analysis.

**General.** In some cases it is desirable to obtain an AND gate output and an OR gate output simultaneously from inputs common to both gates. The dual gate makes this possible. Two or more inputs to the circuit, then produce two outputs, one being the AND output and one being the OR output. Just as in the single logic OR gate, any combination of applied signals produces a high output (logic 1). By the same reasoning, all input signal pulses must be

applied before a high output (a logic 1 output) can be obtained from the AND gate of the dual circuit. If all input signals are applied, a high output is obtained from both the AND and the OR gate output terminals, The following truth table shows the input and output signal relationships for a three terminal input.

INPUT	INPUT	INPUT	OUTPUT	OUTPUT	
Α	В	С	AND	OR	
0	0	0	0	0	
1	0	0	0	1	
0	1	0	0	1	
0	0	1	0	1	
1	1	0	0	1	
1	0	1	0	1	
0	1	1	0	1	
1	1	1	1	1	
Truth Table					

**Circuit Operation.** The schematic of a dual type AND-OR gate is shown in the accompanying illustration. Transistors Q1, Q3, and Q5 form the OR gate of the circuit.



Dual Type And-Or Gate

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Transistors Q2, Q4, and Q6 form the AND gate of the circuits. Resistors RI, R4, and R7 are input and bias resistors to the bases of the OR gate transistors. Resistors R2, R5, and R8 are base bias resistors for Q1, Q3, and Q5, respectively. Resistor R1O is the collector load resistor for the OR gate transistors, Q1, Q3, and Q5. Resistor R1I is the collector load resistor for the AND gate transistors, Q2, Q4, and Q6. Resistors R3, R6, and R9 are emitter stabilizing resistors for OR gate transistors Q1, Q3, and Q5. Voltage sources  $V_{BB1}$ ,  $V_{BB3}$ , and  $V_{BB5}$  provide the base bias for the OR gate transistors. Resistors R3, R6 and R9 are also bias return resistors for the AND gate.

The circuit is arranged to develop positive output pulses when negative input pulses are applied. When no input pulses are applied the biasing networks of Q1, Q3, and Q5 provide a reverse bias which prevents these transistors from conducting. Since no current flows through these transistors, **no** current flows through collector load resistor R9. The output and collector potentials of these transistors are then at the negative collector supply voltage values. This represents a logic O output.

When no current flows through the OR gate transistors, the base bias of transistors Q2, Q4, and Q6 is provided by leakage current ICBO flowing through R3, R6 and R9. Since these emitter stabilizing resistors for Q1, Q3 and Q5 are small in value and the leakage current is negligible, the bases of Q2, Q4 and Q6 are effectively at zero and these transistors are prevented from conducting. Since no current flows through these AND gate transistors, no current flows through the AND gate collector load resistor, R1 1, and the output of the AND gate is at the negative supply voltage value, or a logic O.

When a single negative pulse is applied to any of the inputs (a, b or c) the transistor base to which the input pulse is applied is forward biased and conducts. The increasing emitter to collector current of the transistor causes an increasing collector current to flow through resistor R1O. The current flow through collector resistor R1 O produces a voltage drop across the collector resistor and makes the collector and output end of R1O more positive. This positive output voltage swing constitutes a logic 1.

The emitter current flow of the single OR gate transistor, drives the base of the coupled AND gate

transistor in a forward biased direction. This has no effect on the output of the AND gate, however, since, all three series connected AND gate transistors must conduct simultaneously for a complete current path to exist for any one of the transistors. If no current flows through the AND gate, no current flows through the AND gate load resistor RI 1. The output voltages of the AND gate is then the negative collector supply voltage value. This negative voltage is a logic O.

When negative pulses are applied to any two of the three inputs, for example to inputs a and b, the reverse bias of transistors Q1 and Q3 is cancelled. Transistors Q1 and Q3 are forward biased and conduct. The emitter to collector current of Q1 and Q3 increases and causes current to flow through collector resistor R1O and produces a voltage drop across resistor R1O. Thus, the output of the OR circuit is a positive pulse (a logic 1).

The current flowing through transistors Q1 and Q3, and R3 and R6, causes the base of Q2 and Q4 to be driven negative. The negative voltage forward biases transistors Q2 and Q4. Normally, Q2 and Q4 would conduct if they had a complete current path to the collector supply source. However, since transistor Q6 is not conducting, the series current path for transistors Q2 and Q4 is not complete and they cannot conduct. The voltages at the output of the AND circuit is again the value of the collector supply voltage. This voltage is a logic O.

When negative signal pulses are applied to each of the three inputs, the reverse base bias of each OR gate transistor is cancelled by the negative input pulse causing all of these transistors to be forward biased and conduct. Emitter to collector current flow through these transistors causes current to flow through collector load resistor R1O, producing a voltage drop across R1O and a positive pulse output for the OR circuit. This positive pulse is a logic 1. Negative emitter voltage produced by the conduction of Q1, Q3, and Q5 forward biases the bases of Q2, Q4, and Q6, series AND gate transistors Q2, Q4, and O6 not conduct, since they are forward biased and the series current path is completed. The conduction of Q2, Q4, and Q6 allows current to flow through R11 and produce a voltage drop across it. Hence, the voltage at the collector end of R1 1 becomes positive, and the output is a positive pulse (a logic 1). A dual output now exists.

FLIP-FLOP CIRCUIT

## Application.

The transistor flip-flop is used in electronic computers to supply an output and its complement simultaneously, as an off-on trigger, and for storage purposes. It forms the basic circuit used in most registers.

# Characteristics.

May use positive, negative, or combined logic.

Usually employs self-bias.

Provides two outputs (one is the inverse of the other).

Requires a turn-off or reset trigger to change state. Has two stable states, sometimes called off and on (or O and 1).

## **Circuit Analysis.**

transistor flip-flop is General. The basic sometimes considered as two transistor inverters placed back-to-back. However, by far the simplest arrangement, the dc flip-flop uses a minimum of parts and corresponds closely to the mechanical form of "relay flip-flop" described earlier in this section of the Handbook. Actually, the flip-flop is considered to be a multivibrator, and the various types of transistor multivibrators are fully discussed in the Multivibrator Section of this Handbook (including the binary M.V.). The flip-flop circuit is included here for the sake of completeness of the logic section since most computers contain many flip-flops. Consequently, logic considerations will be stressed, and the overall operation may not be as detailed as might be found in the Multivibrator Section circuit discussions. However, sufficient detail will be given to satisfy the logic student. The symbolic logic diagram and truth table are shown in the following figure.



Like the other logic symbols, the flip-flop logic symbol is functional and is the same regardless of internal circuit. Thus any number of types of multivibrator may be indicated by the same logic symbol. Input and output level indicators are not shown since, in most instances, they may be determined from the levels shown on the outputs of driving or following circuits. The designation of clear (reset) or (C) and set (S) inputs are not required to be shown. However, the C input is always placed on the left of the diagram with the O output terminal, and the S input is placed on the right of the diagram with the 1 output in accordance with American and Military Standard usage (other arrangements may be found in other texts). The truth table shows inputs A and B with outputs X and Y. In most instances, these are the same terminals, and the table merely indicates that when one transistor is in the zero state the other transistor of the flip-flop is in the 1 state, and vice

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versa.

**Circuit Operation.** The schematic of a typical DCTL flip-flop **1S** shown in the following illustration;

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Direct-Coupled Transistor Logic Flip-Flop

Resistor R1 is the collector load resistor for inverter transistor Q2; resistor R2 is the collector load resistor for inverter transistor Q3. Transistor Q1 is a set transistor, by which the ffip-flop is switched to the second steady state condition. Transistor Q4 is a reset transistor, by which flip-flop is returned to the original steady-state condition.

Both transistors conduct when power is first appfied, since the negative supply voltage of the collectors is fed to the opposing bases. Because of slight variations in parts and transistors, one transistor tends to conduct more heavily than the other. As this occurs, positive feedback from this collector to the other base produces a rapid switching action. Thus, one transistor is driven towards saturation and the other transistor is driven toward cutoff. A stable state is reached when one transistor is essentially at saturation. Assume that Q3 is the saturated transistor and O2 is the cut off transistor. Collector resistance values are such that saturation current does not drop the source potential to zero, but leaves it slightly negative (about 0.1 volt). Hence a small negative forward bias is fed back to Q2, which conducts very lightly at afmost cutoff. The conduction is so slight that it can be assumed that Q2 is cut off. With Q2 at effective cut-off, the collector voltages rises toward the supply vafue sufficiently to keep the base of Q3 heavily forward biased. Normally, Q3 would be

completely saturated. However, the low base to emitter resistance of heavily conducting transistor O3 effectively clamps the coffector potential of Q2 to only a few tenths of a volt negative (approximately 0.3 volt) instead of the fufl negative supply voltage. Hence, instead of being completely saturated (as initiaffy assumed for ease of discussion) O3 remains heavily conducting, but is not slowed up by minority-carrier storage effects that would normafly occur if saturation had occurred. (This base of a saturated transistor cannot be quickly changed from forward to reverse bias until the excess charge of electrons has leaked off.) Thus, the output level of T Q2 is held down to only a few tenths of a volt (0.2 volt) peak-to-peak swing. The transistors stay in this initial steady state condition until a switching pulse is applied to conducting transistor Q3.

When a negative pulse appears at the set input, it is applied to the base of Q1. The negative set-pulse forward biases Q1 into conduction; a large base current is initiated, and a large coffector current flows through resistor R1. The large current flowing through resistor R1 causes much of the colfector supply voltage to be dropped across R1, leaving the collectors of Q1 and Q2 near zero volts. Thus, Q1 and Q2 are nearly saturated. The slightly negative coffector voltage of Q2 now appears at the base of Q3, causing Q3 to be reverse biased. The reverse bias of Q3 causes Q3 to be driven nearly to cutoff; very little current flows through Q3 or resistor R2. There is then very little voltage dropped across resistor R2, and the voltage at the collector of O3 rises toward the negative supply voltage vafue. This negative voltage supports the forward bias of Q2 and causes it to conduct heavily. The negative ffip-flop output at the co flector of Q2 which represented a logic one, is now reduced to a nearly zero voltage output at the collector of Q2 and now represents a logic zero. The effectively cut-off condition of Q3 produces a low negative voltage at the coflector, by the clamping action of the low base to emitter resistance of O2 (as previously occurred for Q3), and Q3 now produces a logic one output. The ffip-flop remains in this second steady state until a triggering or gate pulse is appfied to the reset input.

When a negative pufse is applied at the reset input, it appears at the base of Q4. Q4 is forward biased by the negative pulse. Thus, Q4 conducts heavily, causing a large base current to flow and a large

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collector current to flow through resistor R2, the collector load resistor of Q3 and Q4. The current through resistor R2 produces a voltage drop which makes the collectors of Q1 and Q2 only slightly negative. The small negative voltage at the collector of Q3 appears at the base of Q2, and reduces the forward bias of Q2. As a result, little collector current flows through resistor Rl, and very little voltage is dropped across R1. The collector of Q2 then rises toward the negative supply voltage. This negative voltage appears at the base of Q3 to increase the forward bias of Q3 and switch operation back to the original state (Q3 conducting heavily and Q2 effectively cut off). The relatively large negative voltage output at the collector of Q2 represents a logic one, and the small negative voltage output at the collector of Q3 represents a logic zero. The flip-flop remains in this steady state until a triggering or gating pulse is again applied to the set input.

# **RESISTOR-TRANSISTOR LOGIC FLIP-FLOP**

## Application.

The resistor-transistor logic flip-flop is used in digital computer circuits to produce alternate logic 1 and logic O rectangular pulses when triggered.

## Characteristics.

Requires an external trigger pulse. Operating speed is relatively slow. Consists of two cross-coupled inverter stages.

#### Circuit Analysis.

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**General.** The resistor-transistor flip-flop employs two cross-coupled transistor inverters to form a triggered multivibrator circuit. The collector output of each transistor is coupled to the base of the other transistor; thus, the collector voltage of one inverter supplies a feedback voltage to drive the other inverter. The circuit produces two simultaneous rectangular pulse outputs (logic 1 and logic O), one output is 180 degrees out of phase with the other (of opposite polarity). The change in logic state from one output to the other is dependent upon the application of an external trigger pulse.

**Circuit Operation.** The schematic of a typical resistor-transistor logic flip-flop is shown in the following illustration. Resistors RI and R2 are collector load resistors. Feedback resistor R4 couples

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the collector of transistor Q] to the base of transistor **Q2**; **and** feedback resistor R3 couples the collector of transistor Q2 to the base of Q1. Resistors R7 and R8 are base bias resistors, through which the fixed bias supply voltage,  $+ V_{BB}$  is applied to the bases of Q1 and Q2, respectively. Resistors R5 and R6 are input resistors across which the A and B driving pulses are applied to trigger the bases of Q1 and Q2, respectively. The outputs of the flip-flops are obtained from terminals C and D.



**Resistor-Transistor Logic Flip-Flop** 

Assume that Q1 is initially conducting heavily (at saturation), and transistor Q2 is cutoff. The large collector current of Q1 flowing through collector load resistor RI, develops a large voltage drop (positive swing) across R6, which drops the collector voltage of Q1 to zero. Since Q2 is cut off, no collector current flows, and no voltage is dropped across collector load resistor R2. The collector of O2 then rises to the negative collector supply voltage value. The negative collector voltage swing of Q2 coupled to the base of Q1 through R3, produces a negative driving pulse which increases the forward bias of Q1 making QI conduct heavily. Similarly, the zero collector voltage of Q1 coupled to the base of Q2, provides a positive-going reverse bias for Q2, which effectively increases the reverse bias voltage

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supplied from the +  $V_{\rm B}B$  fixed bias supply, and Q2 is held at cutoff.

If a negative pulse simultaneously appears at input A it is dropped across resistor R5, and is applied to the base of Q1. The forward bias of Q1 is increased, but, since Q1 is already conducting at maximum (at saturation), the increased forward bias of Q1 has no effect. On the other hand, if a negative pulse appears at input B, the pulse voltage is dropped across resistor R6 and is applied to forward bias the base of Q2. The forward bias of Q2 produces a collector current flow through resistor R2. The collector current flow through resistor R2 causes the collector supply voltage to be dropped across R2, producing a positive swing at the collector of Q2. This positive-swinging voltage coupled to the base of Q1 through R3, reduces the forward bias on Q1, and the fixed positive bias voltage +VBB assumes control and cuts off Q1. With Q1 cut off, no current flows through resistor R1, and no voltage is dropped across it. As a result the collector of Q1 rises to the negative collector supply voltage value. This negative voltage swing, coupled to the base of Q2 through R4, drives Q2 into saturation. A steady state now exists, with the collector of Q1 (output C) at the negative supply source voltage value (logic 1), and collector of Q2 (output D) at zero volts (logic O). This steady state condition remains constant until a negative driving pulse is applied to input A.

When a negative driving pulse is applied to input A, it appears at the base of Ql, after being dropped across resistor R5. The fixed reverse bias of Q1 is overcome, and Q1 is forward biased, causing collector current to flow through resistor R1. The heavy current through resistor R1 causes all of the collector voltage to be dropped across R1, leaving the collector of Q1 at zero volts. The loss of negative drive voltage on the collector of Q1 is applied through R4 to the base of Q2, reducing the forward bias of Q2 to zero. The reverse bias  $+V_{BB}$  supplied through resistor R8 then resumes control and biases Q2 into cutoff. When Q2 is at cutoff no collector current flows through resistor R2 and no voltage is dropped across it, causing the collector of Q2 to be at the negative supply voltage value. A second steady state now exists, with the collector of Q1 (output C) at zero volts (logic O) and the collector of Q2 (output D) at the negative supply voltage value (logic 1). This is the same state that existed prior to any actuating pulses

being applied. The flip-flop remains in this state until another negative driving pulse is applied to input B.

# INVERTER

# Application.

The transistor inverter is used in digital computers to provide an inverted pulse which is the reciprocal of the applied pulse, and is opposite in polarity to the input pulse.

## Characteristics.

Can be made to produce a positive pulse output from an applied negative pulse, or produce a negative pulse output from an applied positive pulse.

Inversion is provided by the circuit transistor.

The diodes of the diode-transistor inverter increase the operating speed of the circuit.

## Circuit Analysis.

General. The transistor inverter is used in logic circuits to produce a voltage output which is 180° out-of-phase with the input to the inverter. Since a voltage applied to the base of a PNP type transistor produces the reciprocal of the applied voltage at the collector, a transistor will provide the required inversion. By clamping the collector of the transistor at a voltage greater than the saturation voltage with one diode, the transistor is prevented from going into saturation. By also clamping the collector of the transistor at another lower voltage level, the voltage that the collector reaches between applied pulses becomes well defiied. The use of the diode increases the operating speed of the circuit, since the operating range is effectively reduced.

**Circuit Operation. The** schematic of a **typical** transistor inverter is shown in the accompanying illustration. The input is applied to the base of inverting transistor Q1, through resistor R1. Forward bias is applied to the base of the transistor through base bias resistor R2. Capacitor C1 provides overdrive current during the rise time and fall time of the applied pulse. This reduces switching time and increases the operating speed of the circuit. Resistor R3 is the collector load resistor for Q1. Diodes CR1 and CR2 are collector voltage clamping diodes. Resistor R4 is the emitter stabilization resistor for the circuit.



#### **Transistor Inverter**

A positive voltage pulse is applied to the base of transistor Q1 through input resistor R1. The positive pulse decreases the forward bias supplied by  $-V_{BB}$ through resistor R2. Since the forward bias of Q1 is reduced, the collector current and voltage across load resistor R3 is reduced, causing the collector potential to reduce also, The anode of diode CR1 is at a negative potential, preventing CR1 from conducting until the cathode of CR1 becomes more negative than the anode potential. Once the cathode of CR1, which is at the collector potential of Q1, becomes more negative than the anode potential, CR I conducts. Then, regardless of any further decrease in the conduction of Q1, the cathode potential of CR1 and the collector potential of Q1 remains constant at a negative potential slightly less than V1.

When the applied positive pulse ends, the voltage at the base of transistor Q1 falls to the fixed negative base bias potential of  $-V_{BB}$ . The forward bias of Q1 increases, causing the collector current of Q1 to increase, and the voltage drop across R3 to increase. The collector voltage of Q1 therefore rises in a positive direction. Once the collector voltage of Q1 goes positive and exceeds V2 (the slightly negative voltage at the cathode of CR2) diode CR2 conducts, keeping the collector voltage of Q1 constant during any further tendency of the collector current of QI to increase.

As a result, then, of an applied positive pulse, a negative pulse is developed at the output of the inverter. Furthermore, by making the proper choice of clamper voltages V1 and V2, the reciprocated output voltage is clamped over a fixed range. This enables the inverted pulse voltage to be kept to the same magnitude as the applied voltage pulse, in addition to increasing the operating speed of the circuit.

## EMITTER-FOLLOWER CIRCUITS

## Application.

The transistor emitter-follower circuit is usually used in computers and switching circuits to provide a high output current to drive other transistor circuits. This circuit is also used for impedance matching, driving coaxial lines, and for isolating input and output stages.

## Characteristics.

May use either positive, negative, or combined logic.

May use either fixed or self bias, depending on the circuit arrangement.

Because of the low output impedance, a high current gain is obtained, but the voltage gain is always less than 1 (output smaller than input).

## Circuit Analysis.

General. The emitter-follower or commoncollector transistor configuration is usually (but not always) operated in the active region. Bias is normally such that the stage operates as a class A amplifier, as opposed to operating in the entirely saturated or cutoff region. Thus the emitter-follower will usually respond to either a positive or a negative input signal. Since the output is in-phase with the input a negative input will produce a negative output, and a positive input will produce a positive output. Operation is similar to the cathode-follower type of electron tube circuit. In the electron tube cathode-follower, there is a large difference in voltage between the grid input level and the cathode output level. However, in the emitter-follower, there is only a slight difference in dc input and output levels (usually less than 0.5 volt). Therefore, the emitter-follower makes a very useful

dc current-amplifier, capable of large current amplification without shifting the level between the two stages to any noticeable extent.

Circuit Operation. There is no special symbolic representation for an emitter-follower circuit. The logic diagram uses functional symbols only, regardless of circuit configuration. Thus an OR gate (or and AND gate) may be formed of either common-base, common-emitter, or emitter follower (commoncollector) arrangements, and they would be drawn identically in the logic diagram, although the schematic representation would be different. Operation of the common-collector circuit is described for sinusoidal input in the introduction to the Amplifier Section of this Handbook. Operation of the emitter-follower in response to pulse input is discussed in the following paragraphs, and then typical OR and AND circuits are analyzed.

In the following figure, three emitter-follower types of operation are illustrated. Part .4 shows a negative bias applied to the collector and no bias applied to the base, the emitter is returned to ground through load resistor RL.



**Emitter-Follower Circuits** 

With a reverse collector bias and no forward base bias the transistor rests in an essentially cutoff condition

with no collector current flow. With no input there is not output. A positive input signal would only bias the base further in a reverse direction and no output would occur. However, with a negative input signal the base is quickly driven into conduction by the forward bias, and both emitter and collector currents flow. Electron flow is from the emitter through RI and back to the collector, and a negative output voltage is developed across load resistor RL. Thus the output voltage follows the input voltage. When the input signal is terminated the transistor stops conducting and the output pulse is completed as shown by the waveforms in the illustration. In Part B of the figure the opposite condition is shown, the collector is connected to ground and the base is again left open, but the emitter is forward-biased by a positive voltage to ground. With no base bias, and forward emitter bias, heavy emitter current flows and produces a voltage drop across RL which opposes the forward bias and drops the output to approximately zero. Application of a negative input signal cannot increase the emitter current any appreciable amount so the output remains at zero. However, when a positive input pulse is applied, the base is biased more positive than the emitter (reverse bias), and collector and emitter current flow ceases. As a result, the output voltage rises to the value of the positive emitter bias, since no voltage drop is produced across RL to reduce the output. In Part C of the figure, both forward emitter bias and negative (reverse) collector bias are applied, and the transistor is biased at the center of its active region (Class A operation). With no signal applied, the quiescent vrdue of collector current represents zero level. When a negative input is applied, the forward bias is increased, a larger collector current flows, and a negative voltage drop appears across RL and at the output. In a similar manner, when a positive input signal is applied, collector current flow is reduced by the increasing reverse bias, and the emitter voltage rises towards the bias value, producing a positive output. Thus the emitter output follows the input signal, and operates entirely in the active region (this is the same operation as occurs in regular amplifier operation).

A typical emitter-follower OR-Gate is shown schematically in the following illustration. The inputs are separate and the outputs are connected in parallel. In the quiescent condition, with no signal applied, both Q 1 and Q2 are nonconducting since collector current is prevented from flowing by reverse



Emitter-Follower OR Gate

base bias applied through R2 and R4 from a fixed bias source. When the A input is activated by a negative one signal, Q1 is forward biased and emitter current flow through R5 develops a negative going output voltage across R5. The output voltage is slightly less than the input voltage by the base+ mitter voltage. Capacitor Cl helps speed up action by applying the leading and trailing edges of the pulse trigger instantiy to the base, bypassing R1 so that only the low frequency components representing the flat-top portion of the pulse are attenuated by RI. In addition, R1 and R2 form a dual voltage divider. When input A is at ground potential representing a zero input, the base is isolated from the input by R1 preventing it from being shunted to ground, and maintaining the desired high input impedance. When Q1 is conducting the base-collector resistance is low, but is prevented from shunting the bias source by R2. Thus the bias remains unaffected by any input signal shunting effect. As a result of base current flow through R1 a negative input voltage is developed, and the bias and signal voltages add algebraically, to produce a forward (negative) bias. When the input signal is removed, the fixed positive bias again resumes control, biasing the base in a reverse direction and stopping conduction.

When an input signal is applied to input B, identical operation occurs. Capacitor C2 now passes the leading (and later the trailing) edges to Q2, while resistors R3 and R4 form a similar input voltage divider and bias divider as explained for RI and R2 previously. When Q2 conducts, the output voltage is developed across emitter load resistor R5. A negative input produces a negative output. When the input signal is removed the transistor again returns to its normal cutoff condition and output ceases. When an output is developed by either Q1 or Q2, this negative voltage is applied as a reverse emitter bias to the non-conducting transistor so that it is prevented from being triggered. Should an input be appLied to both A and B simultaneously, the signal with the larger negative amplitude will prevail and cause only that circuit to operate.

By reversing the input polarity and bias an emitter-follower AND gate is obtained, as shown in the following schematic.



**Emitter-Follower AND Gate** 

By comparing the emitter follower OR-Gate schematic shown previously with the emitter-follower AND-gate shown above, it is seen that the circuits are

identical. By changing the base bias to a forward bias, Q1 and Q2 conduct in the absence of an input signal, and emitter current flow through R5 develops a negative voltage drop which holds the output to a steady negative level and produces a zero. When a signal is applied to either A or B but not to both inputs simultaneously, the input to which no signal is applied continues conduction and holds the output at zero. However, when an input is simultaneously applied to both A and B, both transistors are cut off and Q1 and Q2 stop conduction. The output rises in a positive direction to zero and produces an equivalent positive (one) output. When the input pulse ceases, both transistors resume conduction, and the output falls to the normal steady negative output level representing a zero.

Although the emitter-follower output voltage is always smaller in amplitude by the amount of base+ mitter bias, a current and power gain are achieved. Current amplification is obtained by using a small amount of base current (usually in the microampere range) to control the large emitter current flow (usually in the milliampere range). Average current gains on the order of 25, or more, are obtained. Since the power output is the voltage times the current, it is easily seen why a power gain is obtained even though voltage amplification is not produced. Although the common-base and commonemitter connections also can provide a power gain, the emitter-follower arrangement is unique in that it provides a low impedance and high current output. Therefore, it is usually employed as a driver stage capable of operating two or three other transistor stages without dropping to a very low level, or for operating relays, or lamps, which require high current at low voltage.

## LAMP DRIVERS AND RELAY PULLERS

# Application.

Lamp drivers and relay puller circuits are used in computers and switching circuits to supply the power

and voltage necessary to drive indicator lamps and operate relays indirectly by triggering a transistor.

# Characteristics.

Provides large voltage or power output, as needed. Is controlled by a small voltage or current.

May be self-biased or fixed biased.

Usually provides a high input impedance and a moderate or low output impedance.

#### Circuit Analysis.

General. There are a number of circuits used to control the indicator lamps and relays used in computers and switching circuits. It is rather difficult to specify a basic circuit since there are so many variations. Therefore, a circuit capable of controlling high voltage and low current devices, and another one capable of controlling low-voltage, high-current devices are selected as typical circuits for discussion. The single transistor type of circuit usually requires that the trigger hold the stage in the "off" or the "on" state, whereas the two transistor circuit requires only an "off-on" trigger be applied to change its state. Since the advent of thyratron semiconductor devices, using pnpn four layer diodes or similar controlled rectifier devices, it is possible to have a single stage trigger itself in a "holding" condition until the shut-off trigger arrives. While it is also possible to use diodes for control elements, the transistor finds universal use since it may easily be "turned on" or turned off" without elaborate circuitry.

**Circuit Operation.** The schematic for a typical high-voltage circuit capable of operating neon indicator lamps is shown in the following schematic. The source of collector voltage is also used to supply the neon indicators. Each of the lamps is



High-Voltage Neon Lamp Driver

controlled by a separate transistor, and resistors R1 through R5 are collector voltage dropping resistors. Resistor R6 is a current limiter, and is also used to drop the lamp voltage during operation to avoid overload on the transistors. Normally, when no input is applied, the transistors rest in a cut-off state. No collector or emitter current flows (except that due to reverse current flow) and the neon indicator lamps remain out because they are only connected to one side of the line. The "cut-off' condition is obtained by leaving the transistor base floating, and applying collector bias. Because there is no reverse forward-bias, and the collector is reverse-biased no emitter current may flow. In the active state, a negative input signal is applied which produces a forward bias on the base of the activated transistor. Assume for the sake of discussion that Q1 is activated and that emitter current flows. Current flow through resistors R6 and R5 keep the collector voltage within transistor ratings, while heavy conduction to ground through Q1 offers a low resistance path for indicator lamp DS1. As long as the voltage across the lamp is high enough to ionize the lamp (55 to 65V for neon), it is illuminated. Once illuminated, the lamp continues to glow until the voltage across it drops below 15 volts, or transistor Q1 stops conducting. When the forward bias is removed from the base of Q1 by turning off the trigger pulse, conduction through Q1 ceases, lamp DS1 is disconnected from ground, and is extinguished.

Each of the lamps maybe illuminated by applying a negative trigger. Note that this circuit is designed for sequential operation of the lamps, and once conduction is produced in any lamp, the voltage across all lamps will drop to a low value (just above 15 volts) because of the shunting effect of the lamp being triggered. For parallel operation, R6 is eliminated and a separate resistor is connected in series with each indicator lamp, thus allowing the full source voltage to ionize each lamp when triggered.

A typical schematic of a relay puller or lamp driver circuit for low-voltage, high-current applications is shown in the following illustration. Two transistors and a diode are employed in a bi-stable arrangement where the relay or lamp is turned on by a negative trigger and then held in that position until turned off by a positive trigger. Transistor Q1 is used



**Relay Puller-Lamp Driver Circuit** 

to control Q2. Resistors RI and R2 are emitter bias resistors, while R4 and R5 are base bias resistors for Q1. Bias values are such that in the "off" condition Q1 is held at cutoff, so no current flows through collector resistor R3. Thus the base of Q2 is held positive, which produces a reverse bias for the PNP transistor and prevents emitter current from flowing and actuating the relay or lamp. When a negative trigger is applied, the base of Q2 is driven negative and this forward bias causes emitter flow through Q2 thereby operating relay K1 or illuminating indicator lamp DS1, whichever is used. In the quiescent condition, complementary NPN transistor QI is held in the nonconducting state because the base bias voltage produced across voltage divider R4 and R5 is smaller than the emitter bias produced by divider R1 and R2, thus the base is effectively reverse biased and Q1 does not conduct. Since relay Kl, or lamp DS1, are connected in series with the base voltage' divider consisting of R4 and R5, whenever Q2 conducts the voltage across this load raises the bias on Q1 base by a like amount and thus supplies a forward bias. With the forward bias controlling Ql, it now conducts and produces a collector current flow through R3. Electron flow is in the direction which produces a negative drop across R3, which holds the base of Q2 in a forward biased condition, and keeps collector current flowing when the input trigger ceases. Operation is initiated by a negative trigger, causing Q1 to conduct, and, in turn, QI holds Q2 in the conducting state; this action continues until a positive trigger is applied to the input to turn it "off".

When a positive "off" trigger is applied to the base of transistor Q2, it momentarily produces a reverse bias, and causes Q2 to stop conduction. Immediately, the voltage developed across the relay or lamp by Q2 collector current flow drops to zero, and the base of transistor Q1 drops to a lower voltage (that produced across R5) than the emitter, to produce an effective negative or reverse base bias for the NPN unit. Thus conduction through Q1 is stopped, and both transistors rest in the cutoff state. Diode CR1 ensures that current may only flow in the proper direction and prevents initiation of a reverse current flow during switching operations. Diode CR2 operates as a discharge diode across the windings of relay Kl, so that any transients caused by the inductive kick in the coil when it is turned off cannot harm the transistor. Capacitor C 1 bypasses R5 so that any load

change is reflected immediately as a bias change on the base of Q1, and produces quicker turn-on and turn-off operation.

# PARALLEL ADDER

## Application.

**The** parallel adder is used in computers to produce the sum of two binary characters, each containing several bits, by the simultaneous application and addition of all bits.

#### Characteristics.

A single full-adder is used for each bit of the applied characters, except for the least significant digit.

A half-adder is used for each least significant applied bit.

Can use either positive or negative logic.

For every two inputs there is a single output.

## **Circuit** Analysis.

General. A parallel adder is formed by individual full-adders (each full-adder being the combination of two half-adders) and a single half-adder. The single half-adder is the initial stage of the parallel-adder, the carry output of which is applied to the carry input of the full adder that follows it. The carry output of this full adder is applied to the carry input of the next full adder that follows it. This type of connection is used between the first half-adder stage and each subsequent full adder stage. The last full-adder stage, however, uses the carry output as the last bit in the resulting sum character of the parallel adder. The remaining sum character bits are the logic pulses produced at the sum outputs of each stage. The pulses produced by the consecutive stages (from right to left) represent progressively significant bits of the resulting sum character. In this way, the parallel adder performs the addition of two applied binary characters simultaneously.

**Circuit Operation.** The logic diagram of a typical two stage parallel adder is shown in the following illustration. A logic diagram is used rather than a schematic diagram, since the amount of circuitry needed to form a parallel adder becomes extensive and would tend to obscure understanding the basic operation of the adder. For a detailed description of the circuit action that occurs in each individual gate refer to the circuit explanations of the OR Gate, the

AND Gate, and the Inhibit Gate, previously described in this section of the handbook.



# Parallel Adder

The logic diagram of a typical parallel adder shown on the accompanying illustration is composed of five AND gate, numbered sequentially (1 through 5) from right to left, seven OR gates, numbered sequentially (1 through 7) from right to left, and ten Inhibit gates, numbered sequentially (1 through 10) from right to left. The logic gates are arranged in three adder stages, each stage represents in right to left order, applied input and output pulse bits in the input and output characters. The stages have subscripts assigned to the inputs and outputs of each stage according to the significance of the place in the input and output characters. Gates are considered parts of a full-adder stage if they react to inputs to

that stage, and aid in producing the output of that stage. That is, all gates that react to first stage augend and addend (Al and B1, respectively) inputs and aid in producing the sum output (S1) of the first stage are considered as part of the first adder stage. Each stage with the exception of the first adder stage, consists of two half-adders. The first half-adder reacts to the applied augend and addend bits, and the second half-adder reacts to the sum output of the first half-adder of that stage and the carry output of the preceding stage.

If an augend character (a set-of-digits to which another set-of-digits is to be added) of 111 and an addend character (a set-of-digits to be added to another set-of-digits) of 101 are applied to the inputs of the parallel adder, logic 1 pulses appear at the following inputs: both inputs of inhibit gate number 1, both inputs of inhibit gate number 2, both inputs of AND gate number 1, the inhibiting input of inhibit gate number 3, the non-inhibiting input of inhibit gate number 4, the augend input of AND gate number 2, both inputs of inhibit gate number 5, both inputs of inhibit gate number 6 and both inputs of AND gate number 3. The two logic 1 inputs to both inhibit gates numbers 1 and 2 develop a logic O output from both gates. These two logic O outputs are applied to the two inputs of OR gate number 1, which, in turn, produces a logic O output. This logic O is the first place bit (least significant) digit of the sum output character (S1).

The logic 1 pulse appearing at the inhibiting input of inhibit gate number 3, causes a logic O to be developed at the output. The logic 1 pulse appearing at the non-inhibiting input of inhibit gate number 4, causes a logic 1 pulse to be developed at the output of inhibit gate number 4. The logic O output of inhibit gate number 3, and the logic 1 pulse output of inhibit gate number 4, appear at the two inputs of OR gate number 2. A logic 1 pulse is developed at the output of OR gate number 2. At the same time, the two logic 1 pulses appearing at the inputs of AND gate number 1 produce a logic 1 pulse output, which becomes the augend input of the second half-adder of the second state. The logic 1 pulse developed at the output of OR gate number 2 becomes the addend input of the second half-adder of the second state. The logic 1 augend pulse to the second half-adder of the second stage, and the logic 1 addend pulse to the second half-adder of the second stage, appear at the

inputs of inhibit gates number 7 and 8, and at the inputs of AND gate number 4. The two inhibit gates (7 and 8) develop logic O outputs, which are applied to OR gate number 4; OR gate number 4, also develops a logic O output. This logic O is the second place digit of the sum output character (S2).

The original second stage (first half-adder) augend and addend bits of logic 1 and logic O, consecutively, appear at AND gate number 2, which develops a logic O output to be applied to OR gate number 5. The second stage, second half-adder logic 1 addend and augend pulses appearing at AND gate number 4 produce a logic 1 pulse output from AND gate number 4. This logic 1 pulse output is also applied to OR gate number 5. OR gate number 5 then produces a logic 1 pulse to be used as the augend to the second half-adder of the third stage.

The third stage augend and addend bits of logic 1 appearing at the inputs of inhibit gates 5 and 6, result in a logic O output pulse from each inhibit gate. The third stage augend and addend bits of logic 1 appearing at the inputs of AND gate number 3, produce a logic 1 pulse at the output of this gate. The logic O outputs of inhibit gates 5 and 6 appear at the two inputs of OR gate number 3, which also produces a logic O output. The logic O output of OR gate number 3 is the addend to the second half-adder of the third stage. The logic 1 pulse produced by OR gate number 5 of the second stage adder is the augend to the second half-adder of the third stage, and appears at the inhibiting input of inhibit gate number 9, at the non-inhibiting input of inhibit gate number 10, and at the augend input to AND gate number 5. The logic O addend pulse to the second half-adder of the third stage, appears at the non-inhibiting input of inhibit gate number 9, the inhibit input of inhibit gate number 10, and the addend input to AND gate number 5. As a result, inhibit gate number 10 produces a logic 1 output, while inhibit gate number 9 and AND gate number 5 produce a logic O output. The logic 1 output of inhibit gate number 10, and the logic O output of inhibit gate number 9 are the inputs to OR gate number 6, which, because of the applied logic 1 pulse, produces a logic 1 output. This logic 1 pulse is the third pulse digit of the sum output character (S3).

The logic 1 pulse output of AND gate number 3 of the first half-adder of the third stage, and the logic O output of AND gate number 5 of the second half-adder of the third stage, are applied to OR gate number 7. OR gate number 7 produces a logic 1 output which becomes the fourth place digit of the sum output character (S4). The resulting parallel adder sum output is then 1100, as shown in the rectangular block at the output area of the parallel adder logic diagram. The following binary and equivalent decimal addition table show that this is the true sum.

Decimal



Series Adder

Augend	111	7
Addend	101	5
Sum	1100	12

Binary

## SERIES ADDER

## Application.

The series or serial adder, as it is more frequently referred to, is used in digital computer circuitry to perform the addition of two binary characters sequentially, or in the order of the application of each bit to the adder.

## Characteristics.

The series adder is formed by the combination of two half adders.

One OR gate, one AND gate, and one Inhibit gate form each half-adder.

A delay line used between the half-adders to establish the proper time relationship between bits.

## Circuit Analysis.

**General.** The series adder performs the addition of two binary characters in the time order in which the bits of each character are applied. This is in contrast to the parallel adder which accomplishes the addition of all the bits of each character simultaneously. The logic diagram of the series or serial adder is shown in the accompanying illustration.

The two binary characters are applied to the first half-adder OR gate and the AND gate. If the first digit of both characters is a logic 1, the OR gate and the AND gate both produce a logic 1 output. The output of the OR gate is applied to the non-inhibiting input of the first Inhibit gate. The output of the AND gate is applied to the inhibiting input of the first Inhibit gate. Since an input is applied to both input lines of the Inhibit gate, no output is produced by the Inhibit gate. The output of the first hrdf-adder AND gate, however, is also applied through a diode to a delay line, where the pulse is retarded for the time period of one pulse before being applied to the next half-adder. Since there is no input to the second half-adder, there is no output (zero logic output) from the second half-adder. By the time the pulse applied to the delay line appears at the second half-adder, another binary digit from each character is being applied to the input of the series adder. If the second bit of each character is again a logic 1, the first half-adder AND and OR gates both produce logic 1 outputs. These outputs are again applied to the Inhibit gate inputs, where they are again prevented from developing an output. The second output of the first half-adder AND gate is also applied through a diode to the delay line where it is also retarded for

the **time period** of one pulse. The first bit applied to the delay line is now delayed one pulse and is applied to the second half-adder OR gate and AND gate. As a result of this bit, the OR gate produces an output, but the AND gate does not. Since there is no pulse applied to the Inhibit input of the second half-adder Inhibit gate, from the second half-adder AND gate, the pulse applied to the non-inhibiting input of the Inhibit gate, from the second half-adder OR gate, is reproduced at the output of the series adder, as a logic 1.

When the second pulse applied to the delay line appears at the second half-adder, the third bit of each character is simultaneously applied at the input. If the third bit applied to the first half-adder A input is a logic 1, and the first half-adder B input is a logic O, the first half-adder OR gate produces an output pulse, but the first half-adder AND gate does not produce an output pulse. Since the only pulse applied to the first half-adder Inhibit gate is applied to the noninhibiting input, an output pulse is produced. This pulse is applied to the second half-adder OR and AND gates, along with the second delayed pulse from the delay line. The second half-adder OR gate and AND gate produce output pulses which are applied to the second half-adder Inhibit gate. The presence of both pulses at the Inhibit gate prevents any output

from occurring. The output of the second half-adder AND gate, however, is also returned to the beginning of the delay line where it is delayed for the time of one pulse. Since the other inputs have ceased, the delayed pulse is the only one applied to the second half-adder OR gate and AND gate, and there is only an output from the OR gate. This pulse is applied to the second half-adder non-inhibiting input of the Inhibit gate, and is reproduced at the output. The output now has one more digit than either of the applied input characters. The following truth tables show the binary augend, addend, and sum of the \_ series adder. To the right of the binary character are the decimal equivalents. From the decimal equivalents of the augend, addend, and sum, it can be seen that the sum produced by the series adder is a true sum.

	Binary	Decimal
Auguend	111	7
Addend	011	3
Sum	1010	10

## Truth Table

**Circuit Operation.** The schematic of a full series adder, corresponding to the symbols of a given logic diagram is shown in the following illustration.



Series Adder

Transistors QI, Q7, Q4, and Q12 are inverting transistors, and Q2, Q8, Q5, and Q9 are OR gate transistors. Transistors Q11, Q14, Q10, and Q13 are AND gate transistors, while Q3 and Q6 are Inhibit gate transistors. Resistors R1, R8, RI 1, R20, R19, and R27 are base biasing resistors, and  $V_{BB1}V_{BB2}$ ,  $v_{BB3} \cdot v_{BB4}, v_{BB5}$ , and  $V_{BB6}$  are base bias' voltage sources. Resistors R2, R4, R9, R12, R14, R18, R21, R23, R24, R28, R30, and R31 are emitter stabilization resistors. The collector load resistors are R3, R5, R10, R13, R15, R17, R22, R25, R26, and R29. Resistors R6, R7, R16, and R32 are interstage coupling resistors, which also serve as a protection

against the possible short to ground caused by a failure in the preceding stage. Diodes CR1 and CR2 control the direction of current flow from the AND gates to the delay line, and prevent the current of one AND gate from flowing into the output of the other AND gate. Capacitor Cl and inductor L1 form a delay line. Voltage source  $V_{\rm cc}$  is the collector supply for all transistors in this circuit.

Assume that the first bits applied to the A input and B input are logic 1's, or positive pulses. These pulses cause the forward bias of Q1 and Q7 to decrease the emitter to collector current of Q1 and Q7, and thus, decrease collector current flow through

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resistors R3 and R22. The voltage at the collectors of O1 and O7 then approaches the negative collector supply voltage. The negative-going voltage at the collector of Q1 is directly coupled to the bases of Q2 and Q11, and the negative-going voltage at the collector of Q7 is directly coupled to the bases of Q8 and Q14. The negative going voltage at each of the four transistor bases causes these transistors (O2, O8, Q11, and Q14) to be further forward biased and they increase conduction. When these transistors conduct, collector current flows through resistors R5 and R26. This collector current flow produces a voltage drop across both collector load resistors, and produces a positive swing on the collectors of Q2 and Q3 (the output of the first OR gate) for the time period of the applied pulse, and the collector of Q11 (the output of the first AND gate) also swings positive for the time of the applied pulse. The positive output of the first OR gate is applied through coupling resistor R6 to the collector of Q3. The positive output of the first AND gate is applied through coupling resistor R7 to the base of O3, where it decreases the forward bias of Q3 so that it does not conduct. With no emitter current flow in Q3, no collector current flows through collector load resistor R1O, leaving the collector of Q3 at the negative collector supply voltage value. This effect, however, is canceled by the positive pulse applied through R6 from the OR gate output. Thus, there is no voltage output at the collector of Q3, and no input to the base of inverting transistor C4

Besides being applied to the Inhibit gate, the positive output of the first AND gate (the collector of Q11) is also applied through diode CR1 to the delay line consisting of Cl and L1. The capacitance of Cl retards the voltage for the time of one pulse; it takes this time for the capacitor to become charged. Simultaneously, the inductance of L1 causes the current to lag for the time period of one pulse. Since the pulse applied to the delay line is retarded for one pulse period, it cannot affect the subsequent circuitry during the time period of the first applied bit. Since there is also no output from the Inhibit gate during this time period, the additional circuitry is not affected, and the output of the adder remains in the same state as if no input pulses had been applied (a logic o output).

**Assume now that** the second bits applied to the A input and B input are also logic 1's, or positive pulses.

These pulses produce an effect identical to the two previously applied positive pulses. There is a difference in the circuit action during the time period of the second set of bits, however, since the first pulse retarded by the delay line now makes its appearance at the second half-adder inverting transistor, Q12. This positive pulse decreases the forward bias of Q12, decreasing the collector current flow through collector load resistor R29 and the voltage drop across it. The voltage at the collector of Q12 rises toward the collector supply voltage. This voltage, negative for the time of the pulse from the delay line, is applied to the bases of Q13, of the second AND gate, and Q9, of the second OR gate. There are no other pulses applied to either of the two gates; and, since the AND gate requires the presence of a pulse at each of its inputs for a complete current path for either of the two AND gate transistors to exist, no output is produced by the AND gate. The delay pulse applied to the base of OR gate transistor, Q9, however, caused an output. The negative delay pulse increases the forward bias of O9. and causes collector current to flow through collector load resistor R15, producing a voltage drop across RI 5. The collector end of R15 swints positive by the amount of voltage dropped across R15. This voltage is coupled through resistor RI 6 to the collector of O6. Since there is not output, or a logic O output, from the second AND gate there is no positive pulse applied to the base of inhibiting transistor Q6. The positive pulse applied through coupling resistor R16 to the collector of Q6 then becomes the output, which is a logic 1. Since it was mentioned that the action of the series adder was the same for the application of the second set of bits as it was for the first set, the delay line again retains a pulse to be used with the application of subsequent bits.

Assume that the third and final bit applied to the A input is a logic 1, or positive pulse. The third bit applied to the B input, however, is a logic O, or lack of a pulse. The positive pulse applied to the A input again reduces the forward bias of Q1 reducing the emitter current of Q1 and collector current through collector load resistor R3. Hence, the collector rises toward the potential of the negative collector supply voltage. This negative voltage is coupled to the bases of Q2 (of the first OR gate) and Q1 1 (of the first AND gate). The AND gate requires a negative pulse to also exist on the base of Q14, so that both Q11 and Q14 will be forward biased and so that a complete

current path can exist for each of the AND gate transistors and resistor R26. However, since no positive pulse is applied to Q7, the fixed forward bias of Q7 remains at a level that permits emitter current and collector current flow through collector resistor R22 to drop the collector supply voltage across R22, making the collector voltage of Q7 zero. Since there is no negative voltage applied to the bases of OR gate transistor Q8 and AND gate transistor Q14, they remain reverse biased. Since there is only a negative voltage available at the base of QI 1 and not at the base of O14, the first AND gate cannot produce an output. The voltage at the collector of Q1 1 is then the negative supply voltage value, which is the same as a zero output, since this negative voltage reverse biases diode CR1 and has no appreciable effect on the normal forward bias applied to Q3.

The negative pulse from the collector of QI applied to the base of OR gate transistor Q2 causes the forward bias of Q2 to increase, resulting in an increased collector current through collector load resistor R5, and an increased voltage drop across R5. This voltage drop leaves the collector of Q2 positive. This positive pulse voltage is coupled through resistor R6 to the collector of inhibiting transistor Q3. This voltage is applied directly to the base of inverting transistor Q4, where it reduces the forward bias of O4, the emitter current of O4, the collector current through collector load resistor R13, and the voltage drop across R13. Hence, the collector end of R13 rises to the negative collector supply voltage value. At the same time, the second positive pulse remaining in the delay line now appears at the output of the delay line, and is applied to the base of inverting transistor Q12. The delayed positive pulse reduces the forward bias of Q12, the emitter current of Q12, the collector current flowing through collector load resistor R29, and the voltage drop across R29. The voltage at the collector of Q12 then rises to the negative supply voltage value.

The negative pulses produced by inverting transistors Q4 and Q12 are applied directly to the bases of transistors Q5 and Q9 (the second OR gate) and the base of Q1O and Q13 (the second AND gate). The forward bias of each of these transistors is increased, thereby increasing the emitter currents, the collector currents through the AND gate collector load resistor and the OR gate collector load resistor, and the voltage drop across these collector load resistors. The voltage at the collector ends of both AND gate collector load resistor R25, and OR gate collector load resistor R15 is then positive, thus, making the outputs of both the second AND gate and the second OR gate positive. The positive AND gate pulse is applied through coupling resistor R32 to the base of the Inhibit gate transistor Q6. At the same time, the positive AND gate pulse is applied through diode CR2 to the delay line consisting of Cl and LI, where the pulse is retarded for the time period of one pulse. The positive pulse appearing at the base of Inhibit gate transistor O6 reduces the forward bias, the emitter current, and the collector current through Q6 collector load resistor R17. Thus, the voltage drop across R17 is reduced, leaving the collector of Q6 at the negative collector supply voltage value. This negative voltage is canceled, however, by the positive output voltage of Q5 applied through coupling resistor R16 to the collector of Q6. The collector voltage, Inhibit gate output, and, finally, the series adder output is then zero volts (or a logic O).

There are no more bits applied to the input; however, the positive pulse applied from the second AND gate (during the time period of the third applied bit) to the delay line emerges from the delay line one pulse later. The delayed positive pulse appears at the base of Q12, where it decreases the forward bias of Q12, the emitter current, the collector current through collector load resistor R29, and the voltage drop across R29. The voltage at the collector end of R29 then rises to the negative supply voltage value. This negative voltage is coupled to the bases of AND gate transistor Q13 and OR gate transistor Q9. The negative voltage has no effect on AND gate transistor Q13, since, Q13 cannot conduct regardless of the voltage applied to base, unless the other AND gate transistor, Q1O, is conducting to provide a complete current path for Q13; and, in this case, Q1O is not conducting because no negative pulse is applied to its base. On the other hand, Q9 can conduct with the proper bias voltage, since Q9 has a complete current path from collector supply source to ground. When the negative pulse is applied to the base of Q9, then, the forward bias of Q9 is increased, emitter current is increased, collector current through collector load resistor RI 5 is increased, and the voltage drop across R15 is increased. The collector side of R15 thus becomes positive. This positive voltage swing, which is the output of the OR gate, is coupled through

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resistor RI 6 to the collector of the Inhibit gate transistor, Q6, where it appears as the output of the series adder as a logic 1. Hence, when a three bit character of 111 (three positive pulses) is applied to the A input, and a three bit character of 011 (one lack of pulse and two positive pulses) is applied to B input, a four bit character of 1010 (a positive pulse, a lack of a pulse, a positive pulse, and a lack of pulse) is obtained at the output.

# SERIES-PARALLEL ADDER

#### Application.

The series-parallel adder is used to add decimal numbers consisting of many bits when expressed in binary from, thus affording the benefit of increased speed through parallel addition, and using a smaller number of circuits by combining it with series addition.

## Characteristics.

The series-parallel adder consists of six full binary adders, two half-adders, and an OR gate.

The binary equivalent of each decimal digit is handled and grouped in parallel.

The decimal place is handled sequentially.

## Circuit Analysis.

General. The series-parallel adder is a parallel arrangement of full serial adders and half serial adders. By using this arrangement fewer circuits are required than for a completely parallel arrangement, but by using a parallel grouping the benefits of greater speed are available. The binary equivalent of one decimal digit (1 through 9) of the addend and one decimal digit of the augend are applied to four addend and four augend lines. This is the parallel phase of operation for the adder. The binary equivalent of the next (more) significant place decimal digit of the addend and augend is applied one pulse time-period later to the four addend and four augend lines. This is the serial phase of operation. When the sum of the digits of the addend and augend are combined to produce a decimal equivalent sum that is greater than "9", the pulses that correspond to a second place digit are returned to the input through another carry line.

**Circuit Operation.** Rather than illustrate all of the circuits and circuit components involved in the composition of the series-parallel adder schematically, a block diagram approach is shown in the following illustration. This simple type of presentation is used to prevent confusion, avoid complexity and avoid duplication of effort, since the complete explanation of a series adder and a parallel adder is given separately earlier in this section of this handbook.

In the illustration, the A inputs represent the inputs to which the augend bits are applied. The B inputs represent the inputs to which the addend bits are applied. The inputs are arranged from right to left as 1 - 2 - 4 - 8, representing the decimal number equivalent of a pulse applied to that input. There is a corresponding series full-adder for each pair of numbered inputs. The adders are numbered in increasing order from right to left, as follows:



Series-Parallel Adder

full-adder No. 1 for inputs A-1 and B-1, full-adder No. 2 for inputs A-2 and B-2, full-adder No. 3 for inputs A4 and B4, full-adder No. 4 for inputs A-8 and B-8. Full-adders 1, 2, 3 and 4 are connected in parallel, having carry lines between each adder and

## **ELECTRONIC CI RCUITS**

the following adder. The sum output of each of these full-adders, with the exception of full-adder No. 1, has its sum output applied to series full-adder No. 5. The sum output of full-adder No. 2 is also applied to half-adder No. 2; the sum output of full-adder No. 3 is also applied to full-adder No. 6, and the sum output of full-adder No. 4 is also applied to the input of half-adder No. 1. The sum outputs of half-adders No. 1 and No. 2, and full-adder No. 6 along with the sum output of full-adder No. 1 are the final outputs of the series-parallel adder. The carry output of series full-adder No. 5 and the carry output of series full-adder No. 4 are applied to OR gate No. 1. The output of the OR gate is returned to the carry inputs of full-adders No. 1 and No. 6 and half-adder No. 2. A carry line exists between half-adder No. 2 and full-adder No. 6, and a carry line exists between full-adder No. 6 and half-adder No. 1.

For ease of explanation, the binary equivalent of the decimal number "463" is used as the augend, and a decimal number "852" is used as the addend to be applied to the series-parallel adder. Since there are three digits or three places to each decimal character, there are three sequential pulse applications. In this case, the binary equivalent of the first-decimal augend digit, which is 0011, and the binary equivalent of the first decimal addend digit, which is 0010, are applied during the time period of the first sequence. The binary equivalent of the second decimal augend digit. which is 0110, and the binary equivalent of the second decimal addend digit, which is 0101, are applied during the time period of the second sequence. The binary equivalent of the third and final decimal augend digit, which is 0100, and the binary equivalent of the third and final decimal addend digit, which is 1000, are applied during the time period of the third sequence.

During the time period of the first sequence, then a logic 1 pulse is applied to the A inputs of full-adders No. 1 and No. 2, and a logic 1 pulse is applied to the B input of full-adder No. 2. As a result, full-adder No. 1 produces a logic 1 sum output with a logic O carry output pulse, and full-adder No. 2 produces a logic 1 carry pulse output with a logic O sum output. The logic 1 sum output of full-adder No. 1 appears at output D1 of the series-parallel adder as a logic 1. The logic 1 carry output of full-adder No. 2 is applied to the input of full-adder No. 3, which, in turn, produces a logic 1 sum output and logic O carry output. The logic 1 sum output of full-adder No. 3 is applied to the inputs of full-adder No. 5 and full-adder No. 6, each of which produce a logic 1 sum output and logic O carry output. The logic 1 sum output of full-adder No. 5 is not used, but the logic 1 output of full-adder No. 6 appears at output D4. The binary logic sum output of the series-parallel adder for the first time sequence is then 0101, which is equivalent to the decimal number 5.

During the time period of the second sequence, a logic 1 pulse is applied to the A inputs of full-adders No. 2 and No. 3, and a logic 1 pulse is applied to the B inputs of full-adders No. 1 and No. 3. As a result, full-adder No. 1 produces a logic **1** sum output pulse with a logic O carry output pulse. Full adder No. 2 produces a logic 1 sum outpulse, with a logic O carry output pulse. Full-adder No. 3 produces a logic 1 carry output pulse with a logic O sum output pulse, and (from the carry output of full adder No. 3, which is applied to the input of full adder No. 4). Full-adder No. 4 produces a logic 1 sum output pulse with a logic O carry output pulse. The logic 1 sum output of full-adder No. 1 appears at output D1 of the seriesparallel adder as a logic 1. The logic 1 sum output of fuU-adder No. 2 is applied to an input of half-adder No. 2 and to an input of full-adder No. 5. The logic 1 sum output of full-adder No. 4 is applied to an input of full-adder No. 5 and an input of half-adder No. 1. Since there are pulses applied to two inputs of full-adder No. 5, there is a logic 1 carry output pulse produced, which is applied to OR gate No. 1.

OR gate No. 1 produces a logic 1 output, which is applied to fuU-adder No. 6, half-adder No. 2, and (after being delayed for the time period of one pulse sequence) is returned to full-adder No. 1. Since there is a logic 1 pulse applied to half-adder No. 2 from full-adder No. 2, and a logic 1 pulse applied to half-adder No. 2 from OR gate No. 1, half-adder No. 2 develops a logic 1 carry pulse with a logic O sum output pulse. The logic 1 carry pulse from half-adder No. 2 is applied to the input of full-adder No. 6, to which a logic 1 pulse is also applied from OR gate 1. Full-adder No. 6 then develops a logic 1 carry pulse with a logic O sum output pulse. The logic 1 carry pulse from full-adder No. 6 is applied to an input of half-adder No. 1, to which a logic 1 pulse has been applied from full-adder No. 4. Half-adder No. 1 produces no carry pulse, since there is no carry line, and produces a logic O sum output pulse, since it has

**two** logic 1 pulses applied to its inputs. The binary logic sum output of the series-parallel adder for the second time sequence is then 0001, which is the equivalent of decimal number 1.

During the time period of the third sequence a logic 1 pulse is applied to the carry input of full-adder No. 1, a logic 1 pulse is applied to the A input of full-adder No. 3, and a logic 1 pulse is applied to the input of full-adder No. 4. Full-adder No. 1 produces a logic 1 sum output with a logic O carry output pulse; full-adder No. 3 produces a logic 1 sum output pulse, and full-adder No. 4 produces a logic 1 sum output. The logic 1 sum output of full-adder No. 1 appears at output D1 of the series-parallel adder as a logic 1. The logic 1 sum output of full-adder No. 3 is applied to an input of full-adder No. 6, and to an input of fulladder No. 5. The logic 1 sum output of full-adder No. 4 is applied to an input of full-adder No. 5 and an input of half-adder No. 1. Since there are pulses applied to two inputs of full-adder No. 5, there is a logic 1 carry output pulse produced which is applied to OR gate No. 1. OR gate No. 1 produces a logic 1 output, which is applied to full-adder No. 6, halfadder No. 2, and (after being delayed for the time period of one pulse sequence) is returned to fulladder No. 1. The pulse applied to the input of half-adder No. 2 appears at the output of half-adder No. 2, (output D2) as logic 1. Since there is a logic 1 pulse applied to full-adder No. 6 from full-adder No. 3, and a logic 1 pulse is applied to full-adder No. 6 from OR gate No. 1, full-adder No. 6 develops a logic 1 carry pulse with a logic O sum out-pulse. The logic 1 carry pulse from full-adder No. 6 is applied to the input of half-adder No. 1. Half-adder No. 1 produces no carry pulse, since there is no carry line, and produces a logic O sum output pulse, since it has two logic 1 pulses applied to its inputs. The binary logic output of the series parallel adder for the third time sequence is then 0011, which is equivalent to the decimal number 3.

The logic 1 pulse returned to the carry input of full-adder No. 1 appears when a fourth time sequence would normally occur. This logic 1 input to full-adder No. 1 appears at output D1 as a logic 1. Since there are no logic 1 A or B pulses applied during the fourth

time sequence, the binary logic output of the seriesparallel adder for the fourth time sequence is then 0001, which is equivalent to a decimal 1.

During the four time sequences the output of the series-parallel adder is shown in the accompanying diagram. This output is correct, since the decimal sum of 463 and 852 is equal to 1315.

	4th Time Sequence	3rd Time Sequence	2nd Time Sequence	1st Time Sequence
Binary output	0001	0011	0001	0101
Decimal Equivalent	1	3	1	5

Series-Parallel Binary and Decimal Outputs

## HALF SUBTRACTOR

# Application.

The half subtracter is used in digital computers to subtract two binary digits, or it may be combined with other half subtracter circuits to form full subtracters which subtract characters containing more than two binary digits.

## Characteristics.

Two inhibit gates are used.

One OR gate is used.

Two inputs produce two outputs, a difference and a borrow output.

Uses negative logic, but can be arranged for positive logic.

## **Circuit Analysis.**

**General.** The half subtracter will produce the difference between two binary characters, each containing two-binary digits or bits. This is accomplished by applying the binary characters to each of two inhibit gates with opposite inhibit inputs. The outputs of the two inhibit gates are applied to an OR gate. The following logic diagram illustrates the relationship between the required gates, and the truth table shows the possible input and output combinations.



INPUT INPUT		OUTPUT	BORROW
A	В	0	Р
0	0	0	0
I	0	I	0
o	I	I	I
I	I	0	0

#### Half Subtracter

In the preceding diagram, the signal applied to A is always the minuend (the number from which another is subtracted) and the signal applied to B is always the subtrahend (the number being subtracted).

If two binary digits or bits are applied to each input, and the minuend is always larger than the subtrahend, the circuit will produce the difference between the character applied to input A and the character applied to input B. This difference may or may not be a true difference. If it is not a true difference, additional half subtracter stages are necessary.

When the first A input bit is a logic 1 and the first B input bit is a logic 1, neither inhibit gate produces an output pulse; thus, there is no negative pulse applied to either of the OR gate inputs. There is, then, neither a difference pulse nor a borrow pulse produced when pulses are applied to inputs A and B simultaneously. In other words, the output is a logic o.

When the second A input bit is a logic 1 and the second B input bit is a logic O, the first inhibit gate produces an output, and the second inhibit gate produces no output. The OR gate is activated by the output of the first inhibit gate. The OR gate in turn,

illustration.

Circuit Operation. The schematic of a typical

half-subtracter circuit is shown in the accompanying

produces a logic 1 output. Since the second inhibit gate does not produce an output, no borrow pulse is produced.

The following illustration shows the binary subtraction of the two characters and the equivalent decimal subtraction.

	Binary	Decimal
Minuend	11	3
Subtrahend	01	1
Remainder	1 0	2
Borrow	0 0	0



#### Half Subtracter

Resistor RI is the input resistor for the A input to input 1; resistor R2 is the base input resistor for the corresponding B input; resistor R4 is the input resistor for the B input to input 2; resistor R5 is the base input and biasing resistor for the corresponding A input. Transistors Q1 and Q2 invert the applied pulses so that the pulses applied on the other inputs are inhibited. Transistors Q3 and Q4 comprise the OR gate. Resistors R3, R6, R9, and R1O are the corresponding base bias resistors for transistors Q1, Q2, Q3, and Q4. Voltage sources  $V_{BB1}$ ,  $V_{BB2}$ ,  $V_{BB3}$ , and  $V_{BB4}$ , are the fixed base bias voltage for transistors Q1, Q2, Q3, and Q4, respectively. Resistors R7 and R8 are collector load resistors for Q1 and Q2,
respectively. Resistor R1 1 is the collector load resistor for OR gates transistors Q3 and Q4. Transistor Q5 inverts the output of the OR gate, so that the output pulses of the subtracter are negative. Resistor R12 is the base bias resistor for Q5, and  $V_{BB5}$  is the base bias voltage source for Q5.

With no input pulses applied, the forward bias on the bases of Q1 and Q2 allow Q1 and Q2 to conduct. The conduction of Q1 and Q2 develops emitter to collector current, and current flows through collector resistors R7 and R8. Consequently, a voltage drop is produced across R7 and R8 sufficient to drop the collector potentials of Q1 and Q2 to zero. A negative pulse (logic 1) is applied to input A, causing the voltage at the collector of Q1 to become negative and, since the base of Q2 receives the negative pulse applied to the A input, the forward bias of O2 is increased. In turn, Q2 conducts, and increases the collector current through collector load resistor R8. Thus, a voltage drop is developed across R8 which reduces the collector voltage of Q2, and produces a positive swing. At the same time that a negative pulse is applied to input A, a negative pulse is applied to input B. The negative B input pulse increases the forward bias of QI since it is directly applied to the base of Q1, causing the emitter to collector current of Q1 to increase, and the collector current through R7 to increase. Thus, the voltage drop across R7 is increased. This causes the collector of Q1 to swing positive, canceling the negative pulse applied at the A input. The negative pulse applied to input B also appears at the collector of Q2. This pulse, however, is canceled by the positive voltage swing developed on the collector of Q2, as a result of the negative pulse applied to input A.

Since the pulses applied to inputs A and B effectively cancel each other, no pulses are applied to the OR gate. Transistors Q3 and Q4 remain nonconducting since they are reverse biased. When no current flows through Q3 and Q4, no current can flow through resistor R11. The output of the OR gate is then the negative collector supply voltage value. This negative voltage applied to the base of Q5 forward biases Q5 and emitter current flows, producing a collector current flow through resistor R13. Thus, the collector voltage is dropped across R13, and the output at C is then a logic O. There is also no borrow pulse produced, since the inhibit gate responsible for providing the borrow pulse (Q2) also has no output.

When another negative pulse is applied to the A and A inputs, it causes the voltage at the collector of Q1 to become negative and causes Q2 to conduct because of the increased forward bias applied to the base of Q2. The emitter to collector current of Q2 is increased, the collector current through **R8** is increased, dropping the voltage across R8, making the collector of Q2 swing positive. Since there are no negative pulses applied to the B inputs at this time, the negative A input, applied through resistor R1, appears on the base of Q3, and overcomes the reverse bias on the base of Q3, making Q3 conduct. The emitter to collector current of Q3 increases, which in turn, causes the collector current through resistor **R1** 1 to increase, and develop a voltage drop across R11. The positive-going collector voltage of Q3 is directly coupled to the base of Q5, and decreases the forward bias of Q5. The decreasing forward bias of Q5 decreases emitter to collector current of Q5, reduces collector current flow through resistor R13, and decreases the voltage drop across R13. The output voltage at C then rises to the negative collector supply voltage value, and effectively produces a logic 1.

The negative pulse applied to Q2 through input resistor R5, forward biases Q2, increases current flow through resistor R8, and makes it more positive. Since, there is no B pulse applied through R4 to oppose the output of Q2, the positive-going voltage on the collector of Q2 appears at the base of Q4, and also appears at borrow output D. The **positive-going** voltage applied to the base of Q4 biases it further into cutoff, and no output is produced by Q5. The positive-going voltage appearing at output D is a logic O. Hence no borrow pulse is produced by the application of the second negative pulse to input A.

In the case of the applied binary minuend and subtrahend, there is no borrow pulse produced. To describe the conditions where a borrow pulse is produced it is necessary to use an additional minuend bit and subtrahend bit. These two bits are not part of the original characters. Here, a minuend bit of a logic O is applied and a subtrahend bit of a logic 1 is applied, The minuend bit is applied to input 1-A and

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input 2-A. Since this bit is a logic O, there is no actual pulse applied. At the same time a logic 1 is applied to input 1-B and input 2-B. This is a negative pulse. A negative pulse applied to the B input is coupled through resistor R2 to the base of Q1 where it increases the forward bias, and collector current through collector load resistor R7, producing a voltage drop across R7 which leaves the collector of Q1 positive. This positive voltage, directly coupled to the base of Q3, has no effect on the conduction of Q3, since Q3 is already biased off by the fixed positive bias voltage, this positive pulse only biases it further out of conduction. The negative pulse applied to the B input is coupled through resistor R4 to the borrow output D. The negative pulse applied to B input is also coupled through resistor R4 to the base of Q4, where it increases forward bias of Q4, causes emitter current to flow through Q4, collector current to flow through collector load resistor RI 1, and the collector voltage to drop across R11. The collector end of resistor R1 1 is now positive. This positive voltage is directly coupled to the base of Q5, where it decreases the forward bias of Q5, decreases the emitter current of Q5, decreases the collector current through collector load resistance R13, and decreases the voltage drop across R13. The collector and collector end of R13 thus rise to the negative potential of the collector supply voltage. This is a logic 1 output. For the application of a minuend bit of O and a subtrahend bit of 1, then, a difference bit of 1 is obtained and a borrow bit of 1 is obtained. The borrow bit has no function in the half subtracter; it must be applied to the circuitry of an additional half subtracter to obtain the proper binary answer involving bits that would produce a borrow pulse.

# **FULL SUBTRACTOR**

## Application.

The full subtracter is used in digital computers to subtract a number of binary digits from another group of binary digits. The full subtracter may consist of two or more half-subtracters, or may consist of other special circuit arrangements.

## Characteristics.

Three inhibit gates are used.

Two OR gates are used.

One delay line is used.

Three inputs produce two outputs.

Uses negative logic, but can be arranged for positive logic.

## **Circuit Analysis.**

General. The full-subtracter must be used in a parallel or series configuration, usually consisting of other full-subtracters, to produce the time difference between applied characters. Each full subtracter, by itself, produces an incomplete difference of characters and borrow pulses. The full-subtracter performs subtraction by having the minuend (character being subtracted from) and the subtrahend (character which is subtracted from the minuend) applied to separate inhibit gates with opposite inhibit inputs. The outputs of the two inhibit gates are applied to an OR gate. One inhibit gate output is, however, applied to a delay line, where any applied pulse is retarded for the time period of one pulse. The output of the first OR gate and the output of the delay line are applied to a second OR gate, the output of which is applied to the non-inhibiting input of a third inhibit gate. Any borrow pulses from a preceding stage are applied to the inhibiting input of this inhibit gate. If a logic 1 pulse appears at the non-inhibiting input of the third inhibit gate, and there are no borrow pulses applied from preceding subtracters, a logic 1 difference results at the output of this full-subtracter. If, however, when a logic 1 pulse appears at the noninhibiting input of the third inhibit gate, a logic 1 borrow pulse is applied from a preceding fullsubtractor, a logic O difference results at the output. Any pulse that develops at the output of the delay line, besides appearing at the input of the second OR gate, appears at the borrow input of the following full-subtracter stage.

The following logic diagram illustrates a typical full-subtracter.

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**Full Subtracter** 

**Circuit Oparation. The** schematic of a typical full-subtracter is shown in the accompanying illustration. In the circuit QI, Q7, and Q6 are inhibit gate transistors; Q2, Q8, Q4 and Q9 are OR gate transistors; Q3 and Q5 are inverting transistors. Input resistors are R1, RI 3, R16, and R19. Biasing resistors are R3, R5, R7, R14, R15, R18, R20, and R21. *Voltage* sources  $V_{BB1}$ ,  $V_{BB2}$ ,  $V_{BB3}$ ,  $V_{BB4}$ ,  $V_{BB5}$ ,  $V_{BB6}$ ,  $V_{BB7}$ ,  $V_{BB8}$ , and  $V_{BB9}$ , are bias voltage sources. Resistors R2, R4, R6, R8, R10, R12, and R17 are collector load resistors. Capacitor C1 and inductor L1 form a delay line.





At time  $t_1$  in the accompanying waveform chart, a negative pulse is applied to the B inputs, but no pulse is **applied to the A** inputs. One B-input pulse is coupled through resistor R13 to the base of inhibit transistor Q1. The negative input pulse forward biases Q1, causes collector current to flow through collector load resistor R2, and the voltage to drop across R2. As a result of the voltage drop across R2, the collector of Q1 swings positive. This positive pulse swing appears at the base of Q2, and, since a negative pulse is required at the base of Q2 for this transistor to be biased into conduction, Q2 remains in the nonconducting state. Thus, the positive pulse produced at the collector of Q1 has no effect on the output.

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#### Waveform Chart

The other B input pulse, coupled through input resistor R16 to the base of OR gate transistor Q8, forward biases Q8. Hence, the emitter current of Q8 increases, and the voltage drop across collector resistor R4 increases. The positive voltage pulse swing developed at the collector of Q8 appears at the base of inverting transistor Q3, where it causes a reduction of forward bias. Therefore, the collector current of Q3 is reduced through collector load resistor R6, and the potential at the collector end of R6 rises toward the negative supply voltage value. This negative voltage appears at the base of OR gate transistor Q4, and forward biases Q4. As a result of the forward bias, the collector current through collector load resistor R8, and the voltage drop across resistor R8 increase. A positive-going voltage puke is now produced at the collector of Q4. This pulse appears at the base of inverting transistor Q5, and reduces the forward bias of Q5. Thus, the collector current through load resistor RIO is reduced, and the voltage drop across resistor R1O is also reduced. The potential at the collector end of R1O now rises toward the negative supply voltage value. This voltage coupled through resistor R11 is the output voltage, which is equivalent to a logic 1.

The input pulse applied to the base of Q8 through resistor R16 is also applied to the delay line composed of capacitor Cl and inductor L1. The delay line retards the applied pulse for the time period of one pulse, so that it emerges from the delay line at time  $t_2$ . This pulse is the borrow output pulse which is applied to another full subtracter.

At time t<sub>2</sub>, no input pulse is applied, so that the pulse emerging from the delay line is the only pulse affecting circuit action. This negative pulse is a borrow output pulse (Cout) to be applied to the borrow input of a subsequent subtracter, but also appears at the base of Q9. The forward bias of Q9 is increased because of the applied delay pulse. The collector current through load resistor R8 and voltage drop across R8 increase. The potential at the collector of Q9 then swings positive, making the potential at the base of Q5 positive. As a result, the forward bias of Q5 is reduced, the collector current through resistor R1O is reduced, and the voltage drop across R1O is reduced. The collector of Q5 then rises toward the negative collector supply voltage value. This negative voltage swing is coupled through resistor R11 to the output, and is equivalent to a logic 1 output.

At time  $t_3$ , a negative pulse is applied to the A inputs, and a negative pulse is applied to the borrow input ( $C_{in}$ ) of the full-subtracor. One of the A inputs is coupled through resistor R19 to the base of inhibit transistor Q7. This negative pulse establishes forward bias, causes collector current to flow through collector load resistor R17, and causes the voltage to drop across resistor R17. As a result, the collector of Q7 swings positive. This positive pulse swing appears at the base of Q8, and, since a negative pulse is required at the base of this transistor to bias it into conduction, Q8 remains in the non-conducting state. For this reason, the positive swinging pulse produced at the collector of Q7 does not affect the output.

The negative input pulse applied at A also appears at the base of Q2, forward biases Q2, increases collector current flow through load resistor R4, and increases the voltage drop across R4. The collector voltage of Q2 now swings positive. This positive voltage swing appears at the base of Q3, and decreases the forward bias of Q3. The emitter current of Q3, the collector current through collector load resistor R6, and the voltage drop across R6 are thereby reduced. The potential at the collector end of R6 then rises toward the negative collector supply voltage value.

## **ELECTRONIC CIRCUITS**

This negative voltage appears at the base of Q4, causing the forward bias of Q4 to increase, Because of this, the emitter current increases, the collector current through collector load resistor R8, increase, and the voltage drop across R8 increases, making the collector voltage of Q4 positive. The voltage at the base of Q5 swings positive, reducing the forward bias of Q5, the emitter current of Q5, and the collector current through resistor R1O, thus, causing the voltage drop across resistor R1O to be reduced. The voltage at the collector of Q5 then rises toward the negative supply voltage value. This negative voltage would normally be coupled through resistor R1 1 to the output; however, the negative pulse applied to the full-subtracter borrow input appears at the base of Q6. The borrow pulse increases the forward bias of Q6 and the collector current through collector load resistor RI 2, producing a voltage drop across RI 2. As a result, the collector of Q6 swings positive canceling the negative pulse voltage applied from the collector of Q5, and no output is produced, resulting in a logic о.

#### **RETIMING AND RESHAPING CIRCUIT**

#### Application.

The retiming and reshaping circuit is used in digital computers to develop, sharp, clean, square-wave pulses from deformed pulses which may have suffered distortion and timing displacement after circulating through delay lines, and numerous coupling circuits.

#### Characteristics.

Circuit consists of a combination of three separate basic circuits. An OR circuit, an AND circuit, and an amplifier.

Uses four diodes and a transistor.

Uses positive feedback.

Employs a clock pulse for retiming.

#### **Circuit Analysis**

**General.** A general description of the retiming and reshaping circuit can be more easily understood by use of the following logic block diagram. As shown, the complete circuit consists of an OR circuit, an AND circuit, and a non-inverting amplifier stage.



Retiming and Reshaping Circuit Block Diagram

The input signal which is reshaped and retimed, is usually taken from a delay line. This input signal is applied to the OR circuit, and produces an OR output signal. The OR output signal is applied to the AND circuit together with a clock pulse of the proper frequency. The OR output signal normally arrives at the AND circuit input slightly before the clock input pulse. The AND circuit only produces an output when coincidence occurs between the OR output signal and the clock input signal. The output of the AND circuit is applied to a non-inverting amplifier, from which the output signal and a positive feedback voltage is obtained. The positive feedback voltage is applied to the OR input circuit, and causes any degeneration present in the other input pulse to be reduced so that the output of the OR circuit is a clean pulse.

**Circuit Operation.** The schematic of a typical retiming and reshaping circuit is shown in the following illustration. Diodes CR1 and CR2, together with resistor R1, form an OR circuit. Diodes CR3 and CR4, together with resistor R2, form an AND circuit. Resistor R3 couples the output of the AND circuit to the base of Q1, one of two transistors used in the non-inverting amplifier. Resistor R4 and R7 provide base bias for transistors Q1 and Q2. Resistors R6 and R9 are emitter stabilization resistors for Q1 and Q2, respectively. Capacitors Cl and C2 are emitter bypass capacitors. Resistors R5 and R8 are collector load resistors for Q1 and Q2.



**Retiming And Reshaping Circuit** 

When no input is applied current flows from the negative supply source through **R1** and through either or both diodes CR1 and CR2. The small current flow is just enough to drop the voltage at the junction of CR1, CR2, and R1 to zero volts, which is applied to the cathode of CR3. Since, when there is no input to CR3, current flows through CR3 and R2 due to the positive supply voltage applied to R2. The current flow is enough to drop the voltage at the junction of CR3, CR4, and R2 to zero volts, whether or not any pulses are applied to CR4. The voltage at the CR3, CR4, R2 junction is applied to the amplifier input; since this voltage is zero, there is no amplifier output.

When a positive pulse is applied to the anode of CR2, it increases current flow through resistor R1. During the period of increased current, the voltage developed at the junction of CR1, CR2, and R1 is positive and varies proportionally with the shape of the applied pulse.

The positive pulse developed at this junction is applied to the cathode of CR3, reverse biases the diode and prevents current from flowing through CR3. The output of the AND circuit is unaffected by this pulse, however, unless a positive pulse is also applied to CR4 at the same time. The pulses that are applied to CR4 are produced by a clock oscillator at a

frequency which corresponds to the central timing frequency of the computer. If the input pulse at CR2 occurred at the proper frequency, it would occur at CR2 slightly before the clock pulse appears at CR4, so that by the time it also appears at CR3, it coincides with clock pulse applied to CR4. When they do coincide. the diodes are back-biased and current is prevented from flowing through R2, CR3, and CR4. The voltage at the junction of CR3, CR4, and R2 now rises to the positive supply voltage value (+ V), as long as both pulses coincide. The positive voltage at the CR3, CR4, and R2 junction, is coupled directly through resistor R3 to the base of Ql, and reduces the forward bias of Q1. As a result, the emitter to collector current of Q1 is reduced, current through collector resistor R5 is reduced, and the voltage at the collector of Q1 approaches the negative supply voltage. This negative-going voltage is directly applied to the base of Q2, and increases the forward bias of Q2. Hence, the emitter to collector current of Q2, increases and then increased collector current flows through R8. The increased current through R8 decreases the voltage on the collector of Q2, and develops a positive output swing. A portion of this output voltage is fed back to diode CR]. The feedback voltage reinforces the next input pulse if it is distorted. If the input pulse occurs at an improper frequency, only that portion of the pulse which occurs during the feedback pulse is reinforced. Timing is restored by the trailing edge of the clock pulse, which stops the AND gate output, and simultaneously ends the feedback pulse. In this way, the output pulse of the OR circuit, made up of CRl, CR2, and RI is assured of occurring at the proper frequency and being undistorted. This pulse then proceeds through the AND gate and the amplifier controlled by the clock pulse, as previously described during the application of the first input pulse. The resulting output of the retiming and reshaping circuit is a clean positive pulse occurring, at the proper frequency.

## **CURRENT STEERING GATE**

## Application.

The current steering gate is used in digital computers for gating serial counters, pulse steering networks, and for other gating applications.

## Characteristics.

Two PNP type transistors are used.

The emitters of both transistors are coupled together.

The bases of both transistors are grounded.

A single input may produce two outputs.

## Circuit Analysis.

**General.** The current steering gate divides the current of the applied signal between two or more paths. The input signal is applied to the emitters of two or more transistors through a common emitter resistor. This allows for current division based on collector supply voltage of each transistor, and produces corresponding output voltages on the collectors of the transistors. The output can then be used to gate serial counters, steer pulses to required circuits, or provide other similar digital operations.

Circuit Operation. The schematic of a typical current steering gate is shown in the accompanying illustration. Resistor R1 is an emitter resistor common to both transistor Q1 and Q2. Resistors R2 and R3 are collector load resistors for Q1 and Q2, respectively. A positive square wave signal is applied at the input terminals, and is coupled to the emitters of Q1 and Q2 through emitter resistor R1. At this point, the current is divided between the two transistor paths in accordance with the two collector supply voltages and circuit resistances. If both collector supply voltage are equal and the circuit resistances are equal the division of current is rdso equal. In this case, it is assumed that the collector supply voltages are unequal. With the application of a positive square wave pulse, the forward bias of both transistors is increased. This causes the emitter to collector current of both transistors to increase, and the current through both collector load resistors to increase. The increase of current through the collector load resistors develops a large voltage drop across the two collector load resistors and thus, both outputs

become more positive. The increase in the positive value of each output is not equal, since the collector supply voltages of each transistor are different.





When the square wave input signal swings negative, the forward bias of the transistors is reduced. The emitter to collector currents are then reduced, and the currents through resistors R2 and R3 are reduced. The reduction of current flowing through the collector load resistors causes the collector and output voltages to approach the collector supply voltage values. These output voltages are different values, since the collector supply voltages are different values. Thus a single input signal may be used to supply two different control outputs of the same phase or polarity but of unequal amplitude.

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# DIODE - TRANSISTOR MATRIX SWITCH

## Application.

The diode-transistor matrix switch is used in digital computer circuits to provide a single output, from any one of several available outputs, and to resolve any combination of more than one input.

## Characteristics.

The switch consists of transistors, diodes, and resistors.

The diode provide switching action, and transistors, in emitter follower configuration, provide minimum reflection and maximum impedance match.

Positive and negative inputs are available from three sources.

Eight outputs are available.

#### Circuit Analysis.

**General.** The diode-transistor matrix switch resolves a specific set of input conditions by producing a logic 1 output at any one of eight outputs when the specific combination of input conditions exist. This concept can be seen from the following illustration.



**Diode-Transistor Switching Matrix** 

In the illustration, the block represents the switching matrix, the lines to the left of the block represent input lines and the lines extending from the bottom of the block represent output lines. The input lines are divided into three pair of input groups, each pair (designated A and B) corresponds to two possible input states of either positive or negative signals. The eight outputs correspond to the eight possible output conditions which are shown in the following logic table, where logic 1 refers to positive pulses.

_												
INPUT					οι	OUTPUT						
	0	2	3	1	2	3	4	5	6	7	8	
	1	0	0	1	0	0	0	0	0	0	0	
	1	0	0	0	1	0	0	0	0	0	0	
	0	1	0	0	0	1	0	0	0	0	0	
	1	1	0	0	0	0	1	0	0	0	0	
	0	0	1	0	0	0	0	1	0	0	0	
	1	0	1	0	0	0	0	0	1	0	0	
	0	1	1	0	0	0	0	0	0	1	0	
	1	1	1	0	0	0	0	0	0	0	1	

I	NPU	Т	OUTPUT							
Ι	2	3	1	2	3	4	5	6	7	8
0	0	0	I	0	0	0	0	0	0	0
Т	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	1	0
I	I	I	0	0	0	0	0	0	0	1

DIODE-TRANSISTOR SWITCHING MATRIX TABLE OF COMBINATIONS

# Diode-Transistor Switching Matrix Table of Combinations

The fact that the block diagram there are two input lines for each group and in the logic table there is no separate line distinction for each input group, may appear contrasting. It is not, however, since in the logic table input numbers correspond to the A lines of each group.

**Circuit Operation.** The schematic of a typical diode-transistor matrix switch is shown in the accompanying Illustration. In the circuit resistors RI through R8 are load resistors for the diodes. The three diodes connected to each of the eight vertical lines are AND gates. CR5, CR13, and CR21 form the first AND gate; CR1, CR14, and CR22 form the

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**Diode-Transistor Matrix Switch** 

second AND gate; CR6, CR9, and CR23 form the third AND gate; CR2, CR10, and CR24 form the fourth; CR7, CR15, and CR17 from the fifth AND gate; CR3, CR16, and CR18 form the sixth AND gate; CR8, CR11, and CR19, form the seventh AND gate, and CR4, CR12, and CR20 form the eighth AND gate. Transistors Q1 through Q16 form complementary emitter-follower circuits. Resistors R9 through R16 are emitter load resistors.

Assume that the first series of inputs are such that line A of input number 1 is a positive or logic 1 pulse, line B of input number 2 is a positive pulse, and line B of input number 3 is a positive pulse. The positive pulse applied to line A of input 1 prevents diodes CR1, CR2, CR3 and CR4 from conducting. The positive pulse applied to line B of input 2 prevents diodes CR13, CR14, CR] 5, and CR16 from conducting, and the positive pulse applied to line B of input 3 prevents diodes CR21, CR22, CR23, and CR24 from conducting. Diodes CR1, CR14, and CR22 are the

only diodes connected to a common vertical line that are prevented from conducting. Diodes CR1, CR14, and CR22 remain reverse biased and no positive voltage applied from voltage +V1 is dropped across R2. The positive voltage from +V1 is, therefore, applied to the base of Q2 and Q1O. On the base of NPN transistor Q2 the positive voltage increases the forward bias and increases emitter current through emitter resistor R1O, leaving the emitter end of R1O positive. On the base of PNP transistor Q1O the positive voltage from supply +Vl decreases the forward bias and, since the transistor is already cutoff, no current flows through this transistor. As a result of the positive voltage appearing at the emitter end of R1O, then, a positive or logic 1 exists at output number 2.

On all of the other vertical lines, there is at least one conducting diode connected to each of these lines, because of the positive voltage that exists on

the anode of the diode and the lack of positive voltage that exists on the cathode. As a result, the positive voltage supply, Vl, is dropped across the series load resistor and the conducting diode, and the vertical line to which it is connected effectively swings negative. As this negative swinging voltage appears at the bases of the two transistors, neither transistor conducts, since the NPN transistor is effectively reverse-biased, and the PNP transistor is prevented from conducting because of the negative supply voltage, -V3, applied to reverse-bias the emitter. The -V3supply voltage is not dropped across the emitter resistor and is, in effect, the output voltage. This equivalent to a logic O output.

Assume the second series of inputs are such that line B of input number 1 is a positive or logic 1 pulse, line A of input number 2 is a positive pulse, and line B of input number 3 is a positive pulse. The positive pulse applied to line B of input 1 prevents diodes CR5, CR6, CR7, and CR8 from conducting; the positive pulse applied to line A of input number 2 prevents diodes CR9, CR10, CR11, and CR12 from conducting, and the positive pulse applied to line B of input number 3 prevents diodes CR21, CR22, CR23, and CR24 from conducting. In this case, diodes CR6, CR9, and CR23 are the only diodes connected to a common vertical line that are prevented from conducting. The load resistor in series with vertical line to which they are connected (R3) then, does not drop any of the positive voltage applied from voltage source +V. Hence, the positive voltage from +Vlappears at the base of Q3 and Q1 1. On the base of NPN transistor Q3 the positive voltage produces a forward bias, and produces emitter current flow through emitter resistor R11, making the emitter end of R1 1 swing positive. On the base of PNP transistor O11 the positive voltage from +V1 decreases forward bias and, since the transistor is already cutoff causes no change in current through this transistor. As a result of the positive voltage swing appearing at the emitter end of R11, then, a positive or logic 1 exists at output number 3.

On all of the other vertical lines, there is at least one conducting diode connected to each of these lines, because of the positive voltage that exists on the anode. As a result, the positive supply voltage, V1, is dropped across the series load resistor by the conducting diode, and the vertical line to which it is connected becomes zero or effectively swings negative. As this negative voltage appears at the bases of the two emitter-follower transistors (one being a PNP transistor and the other being an NPN transistor) neither transistor conducts, since the NPN transistor is reversed biased and the PNP transistor cannot conduct because of the fixed negative reverse bias voltage, -V3, appearing at its emitter. The -V3 voltage is, in effect, the output voltage. This is equivalent to a logic *o* output.

Thus, a various inputs are applied, corresponding outputs are produced, representing either logic 1 or logic O, as described above, depending upon the input pulse combinations.

## **DIODE-TRANSISTOR FLIP-FLOP**

#### Application.

The diode-transistor flip-flop produces logic 1 and logic O pulses to be used in digital computer circuits.

# Characteristics.

Circuit is basically an astable multivibrator. Uses two transistors and six diodes. Uses diodes to provide faster operation.

Uses undes to provide faster operation.

Circuit provides two outputs of opposite polarity.

## Circuit Operation.

**General.** The diode-transistor flip-flop, develops a logic 1 at one output and a logic O at the other output. One transistor conducts initially while the other is cut off. The greater conduction of one transistor holds the other transistor, at cut off until the pulse terminates. The second transistor is then driven into conduction, and the first transistor is cut off. Normally, this action continues until one transistor becomes saturated and the other transistor prevents saturation of either transistor, and reduces the base recovery time, causing the conducting and non-conducting state of the transistors to occur more quickly.

**Circuit Operation.** The schematic of a typical diode-transistor flip-flop is shown in the accompanying illustration. In the circuit, resistors R1 and R2 are collector load resistors; resistors R3 and R4, along



**Diode-Transistor Flip-Flop** 

with diodes CR3 and CR4, dc couple the collectors of transistors Q1 and Q2 to the bases of Q2 and Q1, respectively. Capacitors Cl and C2 ac couple the collector to the opposite base and provide a pulse switching action by which the flip-flop is automatically made to change state. Bias voltages  $+V_{BB1}$  and  $+V_{BB2}$  are applied to the bases of Q1 and Q2 through base bias resistors R5 and R6. Diodes CR5 and CR6 prevent either of the outputs from going highly negative by clamping them to the  $-V_{cc2}$  potential.

Assume that transistor Q2 is initially in the conducting (logic 1) state and Q1 in the non-conducting (logic O) state, because of slight differences between the transistors and values of associated circuitry. Since Q2 is initially conducting, diode CR3 is conducting because of the high negative voltage on its cathode (the collector voltage of Ql) and the low negative voltage on its anode (Q2 base is near zero since the emitter to base drop is small). The negative supply voltage  $-V_{ccl}$  is applied across C1 to the base of Q2, providing a negative pulse to forward bias Q2. As the collector voltage drops across R2 it eventually reaches a low negative value which permits diode CR2 to conduct, and prevents Q2 from saturating. By using a silicon diode for CR3 and a germanium diode for CR2 the collector of Q2 is kept at a negative 0.2 volt value, and cannot saturate (go positive). During

the steady state, capacitor Cl charges toward the negative collector supply voltage value, and gradually reduces the forward bias pulse on the base of Q2. By the time that capacitor Cl is almost fully charged, the forward bias of Q2 is reduced sufficiently to allow the fixed reverse bias  $V_{BB2}$  t. assume control and cut off Q2. When Q2 is cut off, collector current ceases to flow through resistor R2, and no voltage is dropped across resistor R2. The collector voltage of Q2 then rises toward the value of  $-V_{ccl}$ , but is clamped to the value of  $-V_{cc2}$  when the cathode of CR6 becomes more negative than the anode. As a result diode CR2 stops conducting. The negative pulse produced by the rising collector voltage of Q2 is coupled to the base of Q1 through coupling capacitor C2. The negative pulse voltage applied to the base of Q1 overcomes fixed bias  $+V_{BB1}$  and forward biases Q1. Hence the base current and collector current increases. The large collector current flow through resistor RI produces a large voltage drop across R1, leaving the collector of Q1 at some small negative value. Q1 is prevented from going into saturation, however, when the collector voltage of Q1 falls sufficiently to allow diode CR1 to conduct and shunt some of the base drive current through diode CR4 to the collector of Q1. This constitutes the other steady state of the flip-flop, where Q1 is conducting heavily (logic 1 output at the collector of Ql), and Q2 is not conducting (logic O output at the collector of Q2).

During this steady state, capacitor Cl discharges through diode CR3 and resistor R3. At the same time, capacitor C2 is charging toward negative supply voltage -V<sub>CC1</sub> through resistor R5. As C2 charges, the forward bias of QI is gradually reduced. By the time capacitor C2 is almost fully charged, the forward bias of Q1 is reduced sufficiently to cause Q1 to be cut off. As a result, base current, collector current through resistor RI, and the voltage drop across RI cease. The potential of the collector of Q1 then rises toward the negative collector supply voltage value and is clamped to the value of  $V_{CC2}$  by CR5. The negative collector voltage appears across resistor R3, diode CR3, and the base of Q2, and the sharp collector negative pulse is coupled by capacitor Cl to the base of Q2. This large negative pulse voltage forward biases Q2 so that collector current flow through resistor R2 produces a voltage drop across R2. The collector voltage of Q2 falls to a very small negative value, which is sufficiently positive with respect to

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-vCc1 to cause diode CR2 to conduct. As CR2 conducts, the base current of Q2 is shunted to the collector of Q2 through CR2, and prevents sufficient base drive to cause saturation. This is again the original steady state condition where Q2 is conducting heavily (logic 1 output at the collector of Q2), and Q1 is not conducting (logic O output at the collector of Q1).

During this steady state, capacitor C2 discharges through diode CR4 and resistor R4. At the same time, capacitor Cl charges to the negative supply voltage  $-v_{eet}$  through resistor R6. As capacitor C1 becomes charged, the cycle repeats resulting in a steady state where Q1 is again conducting heavily, and Q2 is not conducting. Note that when the switching action occurs it is regenerative, with the collector of one transistor feeding back a forward biasing pulsing to the other base. Thus a fast rising and sharp switching pulse is produced. By preventing the delay normally caused by saturation, and restricting the range of operation to lower levels, faster operation is obtained.

# PART 16-4. COUNTERS

## LOGIC COUNTERS (GENERAL)

Logic counters use appropriately connected logic flip-flops and logic gates which perform binary or decimal counting functions. The gates and flip-flops in the form of logic counters are used in digital computers to regulate digital operating sequences, and to facilitate interpretation and recording of binary or decimal information.

The counters can be classified according to their function, according to the manner in which they are connected, and according to the manner in which they store numbers. In the first category, counters are classified as up-(or forward) counters if they are made to increase in count for every applied pulse; as down-(or reverse) counters if they are made to decrease linearly in count for every applied pulse, and as combination up-down (reversible, or bilateral) counters if for every pulse applied to an input the count increases and for every pulse applied to another input the count decreases. In the second category, counters are classified as serial counters if the gates and flip-flops comprising the counter are connected in series; or as parallel counters if the gates and flipflops comprising the counter are connected in parallel. In the third category, counters are classified as binary counters if the counter stores binary numbers, as a decimal counter if the counter stores decimal numbers, or as a binary-coded decimal digit counter if the counter stores decimal numbers in binary code.

The operational counter, ring counter, and decimal counter are described in the following paragraphs to describe typical counter operation. Various combinations of these basic circuits may be found in different computers.

## **OPERATIONAL COUNTER**

#### Application.

Operational counters are used in digital computers to produce a desired output sequence regardless of the sequence of input pulses. They may be used to count only even numbers, every other number, or some specific combination thereof.

#### Characteristics.

A three-stage operational counter consists of three flip-flops, four AND gates and an OR gate.

An external clock pulse is used to control the output.

An external reset pulse is used to set the flip-flops to their initial state.

### Circuit Analysis.

**General.** The operational counter uses logic flipflops as bi-stable output elements, and both AND gates and OR gates to control the desired output sequence, depending upon the connection of these logic circuits in relation to each other, and in relation to the output flip-flops. The control gates and flipflops may be arranged to produce a sequence to consecutively increasing even numbers with the aid of a clock pulse. The pulse width of the clock pulse determines how rapidly the counting sequence occurs, and the number of flip-flop elements determines the highest number that can be produced before the sequence begins again.

**Circuit Operation.** A block (logic) diagram of the operational counter is shown in the accompanying illustration.



**Operational Counter** 

The counter uses three bi-stable elements, flip-flop A, flip-flop B, and flip-flop C, to produce either logic 1 or logic O outputs. Each flip-flop has a set input (S) actuated by pulses from the preceding AND or OR gate, and each flip-flop has a clear input (C) actuated by a reset pulse. The counter uses four AND gates, AG1, AG2, AG3, and AG4 to provide a gating (S) pulse to the corresponding flip-flop, when all inputs are applied to the proper AND gate. One OR gate, OG1, is used to trigger flip-flop C by either AG3 or AG4. None of the AND gates can be activated until a clock pulse is simultaneously applied. If the counter must be placed in its initial state at any time during the sequence, a reset pulse must also be applied. The outputs of the flip-flops are applied to the inputs of the AND gates together with the clock inputs.



**Operational Counter Waveform Chart** 

The counter initially rests in a stable state where outputs A, B, and C are logic O, and outputs A', B', and C', are at a logic 1. This corresponds to time t. shown in the preceding operational counter waveform chart. The overall output at time t. is then 000, corresponding to the A, B, and C outputs.

At time  $t_1$  a logic 1 clock pulse is applied. This logic 1 pulse complements the A', B', and C' logic 1 pulses at the inputs of AND gate No. 3. As a result, AND gate No. 3 develops a logic 1 output, which in turn provides a logic 1 input to OR gate No. 1. In turn, OR gate No. 1 produces a logic 1 output, which changes the state of flip-flop C; the C output is now a logic 1, and the C' output is now a logic O. Since the A, B, and C outputs of the flip-flops previously were **at** logic O, none of the inputs to AND gates Nos. 1,2, " and 4 (except the clock and C pulse) are at logic 1. The outputs of these AND gates, thus, are a logic O and do not produce any further change of state in the flip-flops. Flip-flops A and B provide a logic O at outputs A and B, and provide a logic 1 at outputs A' and B'. The overall output at time  $t_1$  is then 001.

At time  $t_2$ , the clock pulse returns to logic O, and flip-flop C remains at 1, eliminating any possibility of supplying all logic 1 inputs to the AND gates. Hence, the output remains at 001.

The clock pulse again becomes a logic 1 at time  $t_2$ . This logic 1 pulse is complemented by the logic 1 C-output of flip-flop C at the input of AND gate No. 2. With all logic 1 pulses at the input of AND gate No. 2, AND gate No. 2 develops a logic 1 output, which is applied to the input of flip-flop B and causes flip-flop B to change state. The B output of flip-flop B is now a logic 1; the B' output of flip-flop B is now a logic O. Each of AND gate Nos. 1, 3, and 4, however, do not have all logic 1 inputs; therefore, the logic 1 clock pulse does not cause logic 1 pulses to be developed at the output of these AND gates. Consequently, flip-flop A remains in the initial state, and OR gate No. 1 is not activated to change the state of flip-flop C. Hence, the A output of flip-flop A is still a logic O, and the A' output of flip-flop A is still a logic 1; the C output of flip-flop C is still a logic 1, and the C' output of flip-flop C is still a logic O. The overall output of the counter at time  $t_3$  then is011.

At time  $t_4$  the clock pulse again returns to **logic 0.** As **a** result, none of the flip-flops change state, and the output remains at011.

When the clock pulse again becomes logic 1 at time  $t_5$ , AND gate Nos. 1 and 2 are provided with all logic 1 pulses. Since AND gate No. 1 has the logic 1 clock pulse applied together with a logic 1 pulse from the B output of flip-flop B and a logic 1 pulse from the C output of flip-flop C, AND gate No. 1 develops a logic 1 output, which causes flip-flop A to change state. The A output of flip-flop A now becomes logic 1, and the A' output of tlip-flop A now becomes logic O. Since AND gate No. 2 has the logic 1 clock pulse applied, and a logic 1 pulse from the C-output of flip-flop C, AND gate No. 2 then develops a logic 1 output, which is applied to flip-flop B, causing it to change state. The B-output of tlip-flop B now is a logic O, and the B' output of flip-flop B now is a logic 1. On the other hand, AND gates Nos. 3 and 4 do not

have all logic 1 pulses applied, and cannot develop logic 1 outputs. As a result, no inputs are applied to OR gate No. 1 and it cannot develop a logic 1 output to change the state of flip-flop C. The C-output of flip-flop C then remains at logic 1, and the C' output of flip-flop C remains at logic O. At  $t_s$ , then, the overall output of the counter is 101.

At time  $t_6$  the clock pulse returns to a logic O, and there is no change in state of the flip-flops. The output therefore remains at 101.

At time  $\mathbf{t}_{\eta}$  a logic 1 clock pulse is again applied. AND gate No. 2 is provided with all logic 1 pulses, the logic 1 clock pulse, and a logic 1 pulse from output-C of flip-flop C. As a result AND gate No. 2 develops a logic 1 output, which causes flipflop B to change state. The B-output of flip-flop B now is a logic 1, and the B' output of flip-flop B now is a logic O. However, AND gate Nos. 1, 3, and 4 are not provided with all logic 1 inputs, since AND gates Nos. 1 and 4 require a logic 1 from the B output of flip-flop B, which is not at logic O, while AND gate No. 3 requires a logic 1 from the A' output of flip-flop A, which is now logic O, and a logic 1 from the C' output of flip-flop C, which is also a logic O. As a result, the logic O output of AND gate No. 1 prevents flip-flop A from changing state; the A output of flip-flop A remains a logic 1, and the A' output of flip-flop A remains logic O. As a result of the logic O output of AND gate Nos. 3 and 4, OR gate No. 1 is not provided with a single logic 1 input and, therefore, cannot develop a logic 1 output. Flip-flop C therefore remains in the same state, a logic 1 pulse from the A output of flip-flop A and a logic O from the A' output of flip-flop A. The overall output at time  $t_7$  is then 111.

At time  $t_s$  the clock pulse ends and the AND gates cannot be activated. The output thus remains at 111.

The application of a clock pulse at time  $t_9$  provides activation of AND gate Nos. 1, 2, and 4, since, all other inputs to these AND gates are a logic 1. Each of the AND gates then produces a logic 1 output, which causes flip-flops A and B to change states, and causes OR gate No. 1 to develop a logic 1 output, which changes the state of flip-flop C. Flip-flop A develops a logic O at output A and a logic 1 pulse at output A'; flip-flop B develops a logic Oat output B and a logic 1 pulse at output B', and flip-flop C develops a logic O at output C and a logic 1 at output C'. The overall counter output at time  $t_9$  is 000, the same as the overall output of the first sequence. This is the beginning of the next sequence of operation, which repeats in the same order described previously.

## **RING COUNTER**

#### Application.

**Ring** counters are used in digital computers to produce a progressive binary logic output. Each consecutive stage triggers the next stage to produce a logic 1 output, and all other stages produce logic O outputs. This property of ring counters provides sequential time relationships for use with other circuitry.

## Characteristics.

Counter consists of several flip-flop stages.

Delay lines separate adjoining flip-flops.

A common external pulse is applied to each flipflop stage.

The output of the final stage is fed back to the input of the first flip-flop stage through a delay line.

## Circuit Analysis.

General. A ring counter consists of a series of flipflops, with each output connected to the input of the following flip-flop. The output of the last flip-flop is fed back to the input of the first stage flip-flop. Each flip-flop also receives a triggering pulse directly from an external triggering source. The triggering pulse, however, does not trigger each flip-flop, since the direct connection between stages restricts the action (change of state) of all but one flip-flop. The change of state of the one flip-flop when set into action by the triggering pulse establishes a logic 1 output; the same set-pulse causes the preceding flip-flop to be reset to logic O. After the last stage has been set to the logic 1 state, the subsequent trigger pulse will reset this stage to logic O and again set the first stage to logic 1, which starts the next counting sequence.

The logic diagram of a three stage ring counter is shown in the accompanying illustration. Three flipflops, flip-flop A, flip-flop B, and flip-flop C, are bistable elements.



Three-Stage Ring Counter Scheinatic Program

Three AND gates, AND gate No. 1, AND gate No. 2, and AND gate No. 3 produce pulses which trigger the proper flip-flop to a logic 1 state, and reset the preceding flip-flop to a logic O state. Delay lines, DL-1, DL-2, and DL-3, retard the logic 1 output of the corresponding flip-flop from appearing at the input of the associated AND gate until a subsequent trigger pulse appears at the other AND gate input one bit later.

**Circuit Operation.** The schematic diagram of a two stage ring counter is shown in the accompanying illustration. Transistors Q2 and Q3, and Q6 and Q7 are flip-flop transistors. Transistors QI, Q4, Q5, and Q8 **are AND gate** transistors. Transistor Q9 is a trigger input transistor which complements each of the AND



Two-Stage Ring Counter Schematic Program

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gate transistors to provide the AND function. Resisters R1, R2, R3, and R4 are collector load resistors. Resistors R5, R6, R7, and R8 provide base bias for the AND gate transistors and provide a time constant for the charging of capacitors Cl, C'2, C3, and C4. These capacitors provide a delay between the output of the flip-flops and the inputs to the next flip-flops and also provide a delay between the output of the flip-flops and the reset pulses.

Assume that a negative pulse appears at the base of Q1 at the same time a negative trigger pulse appears at the base of trigger input transistor Q9. Both Q1 and Q9 are forward biased by the negative voltage, and both transistors conduct. The collector current of

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transistor Q1 flows through collector load resistor, RI, of Q1 and Q2, and produces a voltage drop across RI; thus, the collectors of Q1 and Q2 are left at O volts. The O voltage level at the collector of Q2 appears at the base of Q3, causing Q3 to be reversebiased to cutoff. No collector current then flows through resistor R2, and no voltage is dropped across R2. The voltage at the collector of Q3 then rises to the negative collector supply voltage. This represents a logic 1 output of the first flip flop stage, while the second stage is in the logic O state. The negative supply voltage also appears at the collector of Q4, and at the junction of resistors R6 and R7. The negative collector supply voltage is immediately dropped across resistors R6 and R7 by the charging current to capacitors C2 and C3 so that the bases of Q4 and Q5 are at zero voltage level, biasing the transistors to cutoff. Capacitor C2 charges at a time constant rate equal to the value of resistor R6 times the capacitor value. As C2 charges, the voltage drop across it increases, and, at the same time the voltage drop across resistor R6 decreases gradually, and causes the forward bias on the base of Q4 to gradually increase. The RC combination acts as a delay line (DL1 in the logic diagram) for one trigger pulse. Capacitor C3 also charges to the negative supply voltage at a time constant rate equal to the resistance value of resistor R7 times the capacitance value of C3. The charging time constant of C3 is equal to the charging time constant of C2 (and is a part of delay line DL1). As C3 is charged, transistor Q5 is forward biased. When C2 and C3 are fully charged, forward biasing transistors Q4 and Q5, a negative trigger pulse occurs, forward biasing transistor Q9. The simultaneous forward biasing of transistors Q9 and Q4, and the simultaneous forward biasing of transistors Q9 and Q5 permits the three transistors, Q9, Q4, and Q5, to conduct, since there are two complete current paths: from the negative supply voltage source, 'V<sub>ce</sub>, through collector load resistor R2, through transistor Q4, and through transistor Q9 to ground; and, from the negative supply voltage source,  $-V_{cc}$ , through collector load resistor R3, through transistor Q5, and through transistor Q9 to ground.

The current which flows through Resistor R2 produces a voltage drop across R2, causing the collector of Q3 and the base of Q'2 to be at zero volts. The zero volts on the base of Q2 reverse biases Q2, so that Q2 is cutoff. There is then no current flow through resistor RI and no voltage drop is developed

across resistor R1. The collector of Q2 then rises to the negative supply voltage value; the base of Q3 is, thus, also at the negative supply voltage value. Hence, the base of Q3 is forward biased, causing Q3 to conduct. Even after the negative trigger pulse is removed and there is no further current path for transistor Q4, the voltage at the collector of Q3 is maintained at zero volts, since the collector current of Q3 develops a voltage drop across resistor R2. This state of the flip-flop represents a logic O output from this stage.

The current which flows through resistor R3, when the trigger pulse is applied, produces a voltage drop across R3, causing the collector of Q6 and the base of Q7 to be at zero volts. The zero volts at the base of Q7 reverse biases Q7 so that Q7 is cutoff. Because of this, no current flows through resistor R4 and no voltage is dropped across R4. The collector of O7 then rises to the negative supply voltage value, placing the base of Q6 also at the negative supply voltage value. In this case, the base of O6 is forward biased, so that Q6 will conduct and produce a current path through resistor R3, even after the negative trigger pulse is removed. The voltage at the collector of Q6 is thus maintained at zero volts. The zero volts at the collector of Q6 and the negative supply voltage at the collector of Q7 represent a logic 1 output of this second stage. With the application of the second trigger pulse, then, the first stage is brought to a logic O state from a logic 1 state, and the second stage is brought to a logic 1 state from a logic O state. (If additional stages were used, they would also be in the logic O state.)

During and after the application of the second triggering pulse, the negative collector supply voltage at the collector of Q7 is dropped across resistor R8 and resistor R5, so that the bases of Q8 and Q1 are at a zero potential, reverse biasing Q8 and Q1 to cutoff. Capacitors C4 and Cl then charge toward the negative supply voltage value through resistors R8 and R5. This R-C combination acts as delay line DL2 in the logic diagram, since no third stage is shown in the schematic. As capacitor C4 becomes charged the base of Q8 becomes forward biased, and as capacitor Cl becomes charged the base of Q1 becomes forward biased. With the application of the next negative trigger pulse, Q9 is forward biased. The simultaneous forward biasing of transistors Q9 and Q1, and the simultaneous forward biasing of Q9 and Q8 permits the three transistors (Q9, Q], and Q8) to conduct, since there are two complete current paths. One path

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is from the negative collector supply voltage source,  $-V_{CC}$ , through collector load resistor R1, through transistor Q1, and through transistor Q9 to ground; and the other path is from the negative supply voltage source,  $-V_{ee}$ , through collector load resistor R4, through transistor Q8, and through transistor Q9 to ground.

The current flowing through resistor RI develops a voltage drop across R1, causing the collector of Q2 and the base of Q3 to be at zero volts. The zero volts bias at the base of Q3 reverse biases Q3 to cutoff. No current flows through resistor R2, and no voltage drop appears across resistor R2. The collector of Q3 rises to the negative supply voltage value, and the base of Q2 is also at the negative supply voltage value. Thus, the base of Q2 is forward biased, causing Q2 to conduct heavily. The voltage at the collector of Q2 is maintained at zero volts, since the collector current of Q2 develops a voltage drop across resistor R1, even after the trigger pulse is ended and there is no further current path for Q1. This flip-flop state represents a logic 1 output.

The current which flows through resistor R4, when the trigger pulse is applied, produces a voltage drop across R4, causing the collector of Q7 and the base of Q6 to be at zero volts. The zero volts bias at the base of Q6 reverse biases Q6 to cutoff. As a result, no current flows through collector resistor R3 and no voltage drop appears across R3. The collector of Q6 rises to the negative supply voltage value, placing the base of Q7 also at the negative supply voltage value. The base of Q7 is forward biased and conducts, producing a current path through resistor R4, even after the end of the negative trigger pulse. The voltage at the collector of Q7 is maintained at zero volts. The zero volt collector voltage of Q7, and the negative collector supply voltage at the collector of Q6 represents a logic O output of the second stage. With the application of the third trigger pulse, then, the first stage is brought to a logic 1 state from a logic O state, and the second stage is brought to a logic O state from a logic 1 state, and the cycle described above now repeats. (If three stages were used )as shown in the logic diagram), the third stage would have been

driven to a logic 1 state, and stages 1 and 2 would be at logic O.)

#### DECIMAL COUNTER

#### Application.

The decimal or decade counter is used in digital circuitry to count the numbers 1 through 9 (the base 10 system) in binary form. The tenth pulse resets the counter to zero.

## Characteristics.

Four flip-flop stages are required.

PNP transistors are used.

Diode steering is used to trigger the flip-flops.

Flip-flops are capacitively coupled.

The scale of the counter changes from 16 to 10.

Counter is reset to zero by the IOth input pulse.

#### Circuit Analysis.

General. The decimal or decade counter counts binary numbers sequentially up to a decimal equivalent of the number 9 (at the count of 10 the counter is reset to zero). This is accomplished by capacitively coupling a series of four flip-flops to perform the counting function and providing feedback to two stages to prevent the decimal equivalent count from increasing to a value more than 10, since the binary count with four flip-flops would normally be 15 when all are at logic 1. The counting process occurs when positive trigger pulses are applied through diodes to the collectors and directly coupled to the opposite bases of the flip-flop transistors. Each trigger pulse causes the first flip-flop to change state; every other trigger pulse causes the second flip-flop to change state; every fourth trigger pulse causes the third flip-flop to change state; and, every eighth pulse causes the fourth flip-flop to change state. When the fourth flip-flop and the first flip-flop are triggered on, or when the equivalent to the decimal number 9, their logic 1 output pulses supply two inputs to an AND gate. The output of the AND gate trigger the second and third flip-flop stage so that they also produce logic 1 outputs. This allows the next trigger

pulse to change the states of all flip-flop stages to logic O and renew the counting cycle at the IOth trigger pulse.

**Circuit Operation.** The schematic of a typical decimal counter is shown in the following illustration. Transistors Q1 and Q2, Q3 and Q4, Q5 and Q6, Q7 and Q8 form four flip-flop stages. Transistors Q9 and Q1 O are series AND gate transistors, which apply feedback to the second and third stage. Diodes CR1, CR2, CR3, and CR4 prevent negative triggering of the flip-flops, and diodes CR5 and CR6,

CR7 and CR8, CR9 and CR10, together with diodes CR11 and CR12, are steering diodes for the flip-flops, which permits the trigger voltage to change the state of the tlip-flops. Capacitors Cl, C2, C3, and C4 couple trigger pulses to each flip-flop stage; capacitors C5 and C6 couple the AND gate feedback voltage to the input of the second and third flip-flop stage; and capacitors C7 and C8 couple the outputs of the first and fourth flip-flop stages to the series AND gate transistors Q9 and Q10. Resistors R1 through R9 are collector load resistors.





If, initially, all of the flip-flops are in a logic O state transistors Q 1, Q3, Q5, and Q7 are not conducting, and transistors Q2, Q4, Q6, and Q8 are conducting. When a positive pulse is applied to the trigger input, it is coupled through capacitor Cl to forward bias diode CR5. Since the cathode of CR5 is connected to a negative voltage, the diode conducts. The positive trigger pulse is applied to the collector of Q1 (which forward biases Ql), and is also fed directly to the base of Q2. Transistor Q2 is thus reverse-biased stopping collector current flow, and causing the collector voltage of Q2 and the base voltage of Q1 to rise

ORIGINAL

toward the negative collector supply voltage. Transistor Q1 is then forward-biased and conducts. The collector current of Q1 develops a voltage drop across R1, which drops the collector voltage of Q1 to zero. Thus, a logic 1 negative output is obtained from the first stage flip-flop at transistor Q2. The negative voltage swing at the collector of Q2 is coupled to the next flip-flop stage through capacitor C2. Since the negative pulse is provided with a current path through diode CR2, it is absorbed by the supply, but diodes CR7 or CR8 will not conduct with a negative anode potential. As a result, the second, third, and fourth flip-flop stages are not triggered and do not change state. The counter output after one trigger pulse is then a logic 1 from the first stage, and a logic O from the remaining stages. The output is read as 001, which is equivalent to the decimal number 1.

The accompanying waveform chart shows the relationship of the input and output waveforms for the sequence of operation described in the following paragraphs.



Waveform	С	h	а	r
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When the second positive trigger pulse is applied to the trigger input diode CR6 conducts and drives the collector of Q2 and the base of Q1 positive. The positive voltage pulse on the base of Q1 reverse-biases Q1 to cutoff, no collector current flows through resistor R1 and no voltage drop appears across R1. The voltage at the collector of Q1 then rises to the negative supply voltage value. This negative collector voltage also appears at the base of Q2, and increases the forward bias of Q2. Transistor Q2 now conducts heavily and collector current flows through resistor R2, producing a voltage drop across R2. The voltage at the collector of Q2 now swings positive rising to the zero voltage level. The first stage flip-flop output at FF1 is now at logic O. The positive voltage swing at the collector of Q2, however, is coupled across capacitor C2 to the junction of diodes CR2, CR7, and CR8. Diode CR2 does not conduct because the positive voltage reverse biases the cathode; diode CR8 does not conduct because the zero collector voltage of Q4 appears at the cathode of CR8 and no potential appears across the diode. Diode CR7, however, conducts, since the negative collector supply voltage at the collector of Q3 is applied to the cathode of CR7 and forward biases the diode.

When diode CR7 conducts, the positive voltage swing from the collector of Q2 forward biases the collector of Q3 and reverse biases the base of Q4. Transistor Q3 conducts and Q4 is thus biased to cutoff. The collector voltage of Q4 then rises to the negative collector supply voltage value and supplies a logic 1 output at FF2. This negative voltage is also fed back to the base of Q3, further biasing Q3 into conduction. Saturation current flows through collector load resistor R3, and drops the collector voltage. The collector voltage of Q3 then swings positive toward the zero voltage level. The negative voltage rise at the collector of Q4 is coupled to the next stage through capacitor C3, and this negative pulse is absorbed by the supply as diode CR3 conducts. Since the anodes of diodes CR9 and CR10 are reverse biased, the third and fourth stages are not triggered and no not change state. The output after two trigger pulses is a logic O from the first stage, a logic 1 from the second stage, and logic O from the third and fourth stages. The output is read as 0010, which is equivalent to the decimal number 2.

When a third positive trigger pulse is applied to the trigger input, diode CR5 conducts and drives the collector of Q1 and the base of Q2 positive. The positive voltage on the base of Q2 reverse-biases Q2 to cutoff. No collector current flows through R2 and no voltage drop is produced across resistor R2. The voltage at the collector of Q2 then rises to the negative supply voltage value. This negative voltage also appears at the base of Q1, causing the forward bias of Q1 to increase. Transistor Q1 then conducts, and collector current flows through resistor R1, producing a voltage drop across RI. The voltage at the collector of Q1 is now at the zero voltage level, and the first stage flip-flop now produces a logic 1 output at FF1. The negative voltage rise at the collector of Q2 is coupled to the second flip-flop stage through capacitor C2, and is absorbed by the supply as CR2 conducts. Since diodes CR7 and CR8 are reverse-biased and do not conduct, the second, third, and fourth flip-flop stages do not change state. Because the second flip-flop still remains in the 1 state, the output after the third trigger pulse is then a logic 1 from the first and second stages, and logic O from the third and fourth stages. This output is read as 011, which is equivalent to the decimal number 3.

A fourth positive trigger pulse, similarly, causes the first stage flip-flop to change state from logic 1 to logic O. The positive voltage swing at the collector of Q2 is coupled across capacitor C2, through diode CR8 to the collector of Q4 and the base of Q3, resulting in the negative collector supply voltage appearing at the collector of Q3 and zero voltage appearing at the collector of Q4 and at output FF2. This represents a logic O output from the second flipflop. The positive voltage swing produced at the collector of Q4 is coupled across capacitor C3, through diode CR9 to the collector of Q5 and the base of Q6. As a result, Q6 is cutoff and Q5 is driven into saturation. The voltages at the collector of O5 is now zero and the voltage at the collector of Q6 rises to the negative supply value. This represents a logic 1 output from the third stage flip-flop at FF3. Since the collector of Q6 is at a negative voltage, there is no positive pulse generated by the collector of Q6 to drive the next flip-flop stage. The fourth stage thus remains in the initial logic O output state. The output after the fourth trigger pulse is a logic O from the first, second, and fourth flip-flop stages, while the third flip-flop is in the logic 1 state. This output is read as 0100, which is equivalent to the decimal number 4.

When a fifth positive trigger pulse is applied, it causes the first stage flip-flop to change state from logic O to logic 1. None of the other stages change state, however, since the collector voltage swing of Q2 is negative and will not drive the second flip-flop stage. The output after the fifth trigger pulse is a logic 1 from the first and third stages, and a logic O from the second and fourth stages. This output is read as 0101, which is equivalent to the decimal number 5.

The first stage flip-flop again changes state when the sixth positive trigger pulse is applied. The change of state from a logic 1 to a logic O of the first flip-flop causes a positive voltage swing to be developed at the collector of Q2. This positive pulse voltage is coupled through capacitor C2 and through diode CR7, to the collector of Q3 and the base of Q4. Consequently Q4 is cutoff and the collector voltage of O4 rises to the negative supply value. Meanwhile, Q3 becomes saturated causing zero voltage to appear on the collector of Q3. Thus, a logic O output is produced by the second state at FF2. This negative output voltage on the collector of Q4 will not drive the third flip-flop stage, so the following flip-flop stages do not change state. The output after the sixth trigger pulse is a logic O from the first and fourth stages, and a logic 1

from the second and third stages. This output is read as 0110, which is equivalent to the decimal number 6.

A seventh trigger pulse again changes the state of the first flip-flop stage from logic O to logic 1. The collector of Q1 becomes zero and the collector of Q2 rises to the negative collector supply voltage value. The remaining flip-flops do not change state, however, since the negative voltage on the collector of Q2 will not drive the second stage flip-flop and cause it to change state. The output, then, after the seventh trigger pulse is a logic 1 from the first, second, and third flip-flop stages, and a logic O from the fourth flip-flop stage. This output is read as 0111, which is equivalent to the decimal number 7.

The eighth positive trigger pulse again causes the first stage flip-flop to change state from a logic 1 to a logic O. The positive voltage swing developed on the collector of Q2 of the first flip-flop stage is coupled across capacitor C2 and through diode CR8 to the collector of Q3 and the base of Q3, which changes the state of the second flip-flop from logic 1 to logic O. The positive collector voltage of O4 is coupled across capacitor C3 and through diode CR10 to the collector of Q6 and the base of Q5, which changes the state of the third flip-flop from logic 1 to logic O. The positive swinging collector voltage of Q6 is coupled across capacitor C4 and through diode CR11 to the collector of Q7 and the base of Q8. The positive voltage on the base of Q8 reverse biases Q8 to cutoff. The negative collector supply voltage on the collector of Q8 also appears at the base of Q7, forward-biasing Q7 to saturation. A zero voltage on the collector of Q7 and a negative voltage on the collector of Q8 represents a logic 1 output from this fourth flip-flop at FF4. The output after the eighth pulse is then a logic 1 from the fourth stage flip-flop and a logic O from the first, second, and third stages. The output is read as 1000, which is equivalent to the decimal number 8.

The ninth positive trigger pulse changes the state of the first flip-flop from logic O to logic 1. The negative voltage at the collector of Q2 is not capable of driving the following flip-flop stages, so the second, third, and fourth flip-flop stages remain in their previous states. The output thus becomes 1001 after the ninth trigger pulse, or a decimal equivalent of the number 9. However, the logic 1 outputs of flip-flop: no. 1 and no. 4 also appear at the two inputs of the series AND gate (the bases of Q9 and QIO) through

capacitors C7 and C8. As a result both Q9 and Q10 are forward biased into conduction. The current flowing through resistor R9 develops a voltage drop across R9, and produces a positive-going voltage at the collector of Q9. This positive-going voltage is coupled through capacitors C5 and C6 to the second and third flip-flop stages. As a result, the second and third flip-flops change states from logic O to logic 1, and all of the flip-flops are in the logic I state at some time between the ninth and tenth trigger pulse. This output, since it occurs between the trigger pulses, does not appear as an output, but merely prepares the counter to be triggered to an all logic O output with the application of tenth trigger pulse.

The tenth positive trigger pulse changes the state of the first flip-flop from logic 1 to logic O. The positive swinging voltage at the collector of Q2 is coupled through capacitor C2, through diode CR7 to

the collector of Q3, and the base of Q4, which brings Q3 to saturation and Q4 to cutoff. The state of the second flip-flop stage changes from logic 1 to logic O. The positive voltage at the collector of Q4 is coupled through capacitor C3, through diode CR9 to the collector of Q5 and the base of Q6, which biases Q6 to saturation, and bring Q5 to cutoff. The state of the third flip-flop stage changes from logic 1 to logic O. The positive voltage at the collector of Q6 is coupled across capacitor C4 through diode CR11 to the collector of Q7 and the base of Q8, which biases Q8 to saturation and brings Q7 to cutoff. The state of the fourth flip-flop stage then changes from logic 1 to logic O. The output of the counter is now read as 0000. At the tenth trigger pulse application, then, the counter returns to its original state of O and the cycle begins again.

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# PART 16-5. REGISTERS

### LOGIC REGISTERS (GENERAL)

A logic register is used to digital computers to temporarily store the logic of one binary word. The storage or memory elements of a register may be magnetic cores of flip-flops, and the latter is most commonly used. The logic 1 or logic O state of the storage elements of a register represents bits; the combined bits form a word. The number of bits in a word determines how many storage elements are required, and thus determines the size of the register. The stored word is produced by input potentials from accompanying circuitry for each bit. The series of logic bits remain in the register with altering or blocking any signal applied to accompanying circuitry. When the word is to be used in the performance of a specific operation, such as multiplication or division, it may be completely removed from the register to operate a circuit (destructive read out), or the word may be used by a circuit and still remain in the register (non-destructive read out). Non-destructive read out can also be used to sample single bits of a stored word without removing the bit from the register. Non-destructive read out register must also be provided with a clear input, which permits each flip-flop in the register to be returned to the initial all logic O state.

The various types of registers and their circuit operation are discussed in detail in the following paragraphs. Generally speaking, the clear register is used as a temporary storage device to clear a group of flip-flops and return them to their original state. The shift register moves over or shifts the output one place for each input pulse, and the complement register is used to trigger or complement a series of flip-flops into the next state of operation. A doubleline transfer register is used to transfer information from one line to another, and the circulating register is used to insert information into a register and continuously circulate it, or to introduce a specific delay for each trigger. The accumulator register usually stores numbers and adds them together to form a new sum for each bit introduced. Although functionally and schematically registers may appear similar, each is named and used specifically to perform a definite operation in the computer.

## **CLEAR REGISTER**

#### Application.

A clear register is used in digital computers as a temporary storage device for a one or more bit word. Each memory element in the register is capable of being **set** to logic 1 by individual circuits, but is capable of being cleared by only a single reset source.

#### Characteristics.

Register uses three flip-flops.

Each flip-flop has two inputs and two outputs.

Each flip-flop is triggered by an individual setsource.

Each flip-flop is cleared by a common reset source.

#### Circuit Analysis.

**General.** A clear register consists of a series of individual flip-flops which have nothing in common except for a common clear input. Each flip-flop has a separate set-input which is connected to an individual triggering circuit. When the triggering circuit supplies a **trigger** pulse to the set-input of a tlip-flop, the flip-flop produces a logic 1 output; when the triggering circuit does not supply a trigger pulse, however, the associated flip-flop develops a logic O output. When a pulse is applied to the common clear input of the register, all outputs of the register change to logic O, regardless of the state of the out-puts prior to application of the common reset pulse. The block diagram of a typical three stage clear-register is shown in the following illustration.



**Clear Register** 

#### ORIGINAL

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Circuit Operation. The schematic diagram of a typical three-stage clear-register is shown in the following illustration. In the first flip-flop stage, resistors R1 and R2 are collector load resistors.

Resistors R3 and R4 are the second stage flip-flop collector load resistors, and resistors R5 and R6 are collector load resistors of the third stage. Transistors



**Clear Register** 

Q1 and Q2 are the first stage flip-flop transistors; transistors Q3 and Q4 are second stage flip-flop transistors; and transistors Q5 and Q6 are third stage flip-flop transistors.

In the initird state, the three flip-flop stages produce a logic 1 at their O outputs. A logic 1 from each O output is obtained when the first transistor of each stage, QI, Q3, and Q5, are conducting heavily, and the second transistor of each stage, Q2, Q4, and Q6, are not conducting. As a result of the heavy conduction of Q1, Q3, and Q5, current flows through collector resistors R1, R3, and R5 and the negative supply voltage is dropped across these resistors, leaving the collectors of Ql, Q3, and Q5 at the O volt level. As a result of Q2, Q4, and Q6 not conducting, no current flows through resistors R2, R4, and R6, and no voltage is dropped across them, leaving the collectors of Q2, Q4, and Q6 at the negative supply voltage value. This negative collector voltage is also applied to the cases of Q1, Q3, and Q5 keeping them forward biased and heavily conducting.

When a negative pulse is applied to the set inputs of the first and third stages, the collectors of Q1 and Q5 are driven negative by the applied trigger pulse. This negative voltage also appears at the bases of Q2 and Q6, which forward biases Q2 and Q6. Collector

current then flows through resistors R2 and R6, dropping the negative collectors supply voltage across these resistors and the collectors of transistors Q2 and Q6 swing positive to the O-volt level. Since the bases of Q1 and Q5 are directly coupled to the collectors of Q2 and Q6, respectively, the positive collector swing reverse-biases on the bases of Q1 and Q5. As a result, Ql and Q5 do not conduct, no current flows through the collector load resistors, and no voltage is dropped across the resistors. The voltage at collectors of Q1 and Q5 then rises to the negative collector supply voltage. The negative voltage at the collectors of QI and Q5 represents a logic 1 output. The output of the register is then logic 1 from the first and third stage 1-outputs and a logic O output from the second stage 1-output. The register output remains in this state until a negative reset or clear pulse is applied.

When a negative clear pulse is applied, it appears at the collectors of each of the second flip-flop transistors, Q2, Q4, and Q6. The negative clear pulse also appears at the bases of Q1, Q3, and Q5, forward biasing each of these transistors. Q3, however, is already forward biased, since the flip-flop stage containing this transistor was not changed from logic O to logic 1 at the 1-output when the other stages previously were triggered, and the clear trigger has no

effect on this stage. Q1 and Q5, on the other hand, conduct and produce a collector current flow through resistors RI and R5, which drops the voltage across these resistors. The voltage at the collectors of Q1 and Q5 then swing positive to the O volt level. This positive swing appearing at the bases of Q2 and Q6 reverse-biases them and represents the removal of all forward bias to these transistors, resulting in the nonconduction of Q2 and Q6. Because Q2 and Q6 no longer conduct, no current flows through collector load resistors R2 and R6, and no voltage drop appears across these resistors. The voltage on the collectors of Q2 and Q6 then rises to the value of the collector supply voltage. The collectors of Q1, Q3, and Q5 are now at O volts, and the collectors of O2, O4, and O6 are at the collector supply voltage. These same conditions existed for the initial state. Therefore, the application of a negative clear or reset pulse causes the register return to its initial state of all logic O output at the 1-outputs.

# SHIFT REGISTER

## Application.

The shift register may be used for temporary bit storage in a computer, and to shift in or out a series of pulses. It can also supply a predetermined time delay for a digital operation, or be used to **insert** characters into the computer.

### Characteristics.

Either series or parallel outputs maybe employed. Series operation requires a train of pulses equal to the number of stages to provide an input. A similar number of pulses is required to clear the register.

Flip-flop stages are used for pulse storage.

Delay "lines are used to prevent coincident triggering by input and shift pulses.

A shift occurs when a preceding flip-flop changes state from 1 to O output, and a shift pulse is applied.

Each flip-flop is triggered sequentially.

The shift progresses from left to right, but the output is read from right to left.

## Circuit Analysis

General. The shift register uses a series of flipflops for temporary storage of a binary word. Each information bit of the binary word appears in the register after the application of a shift trigger pulse to the shift and clear input. Each subsequent trigger pulse moves the previously applied bits one place to the right in the register and allows room for another bit to be accepted by the last (or input) stage of the register. The number of trigger pulses is equal to the number of stages minus one so that the first bit of the binary word appears in the first stage of the register and each succeeding bit appears in each succeeding stage of the register. The word then remains in the register until additional trigger pulses are applied to the clear input to remove the word from the register. One bit of the stored word is removed for each additional trigger pulse applied after the amount required to situate the word properly in the register.

**Circuit Operation.** The logic diagram of a series shift register is shown in the accompanying illustration.

The series shift register consists of four tlip-flops (FF1 through FF4) corresponding to four binary places. A delay line is connected between the 1-output of each flip-flop and the set-input of the following flip-flop (DL1 through DL3). A train of three short shift pulses is applied to the shift and clear pulse input, and occur midway between the binary word pulses to produce the step-by-step or sequential shifting of the flip-flops.

Assuming that the logic word to be stored is a binary 1101, a logic 1 corresponding to the extreme right digit of the word, appears at the serial set-input of flip-flop no. 4 at the start of operation. Flip-flop no. 4 which is initially in the O state, assumes a logic 1 state, and remains in this state even after the first





binary input pulse ends. A shift and clear pulse is applied at a time midway between the end of the first stored bit pulse and the beginning of the next word bit. This shift and clear pulse changes the logic 1 pulse appearing in flip-flop no. 4 to a logic O, and clears it from this flip-flop. Meanwhile, the logic 1 pulse which was applied to the input of delay line DL-1, is delayed for the remainder of the shift and clear pulse. After the short shift and clear pulse has ended, the logic 1 pulse in DL-1 emerges and appears at the set-input of flip-flop no. 3. Flip-flop no. 3 then assumes a logic 1 state. Thus, the initial bit is now shifted from FF-4 to FF-3.

A short time later the next digit of the binary word appears at the input of flip-flop no. 4. This digit, is a logic O, and has no effect on the logic O state of flip-flop no. 4. After the logic O pulse ends another shift and clear pulse occurs. The logic 1 appearing in flip-flop no. 3 is now cleared from the flip-flop and made to appear at the input of the second delay line, DL-2, by the second shift and clear pulse. After the end of this shift and clear pulse, the logic 1 pulse emerges from the delay line, and changes the state of flip-flop no. 2 from logic O to logic 1. The initial bit is thus transferred from FF-3 to FF-2, and the second bit (a logic O) is transferred to FF-3.

The next digit of the binary word, logic 1, appears at the serial input to flip-flop no. 4, changing the state of flip-flop no. 4 from logic O to logic 1. Another (the third) shift and clear pulse again occurs after the word pulse ends. The logic 1 appearing flipflop no. 4 is thus cleared again and is applied to the input of DL-1, while the logic 1 appearing in flip-flop no. 2 is also cleared and is applied to delay line DL-3. The logic 1 present in each delay line is retarded until after the end of the final shift and clear pulse, at which time all the delayed logic ones emerge, and appear at the input to the following flip-flops. The logic 1 delayed by DL-3 appears at flip-flop no. 3, which changes state from logic O to logic 1, and the logic 1 delayed by DL-3 appears at flip-flop no. 1, which also changes state, from logic O to logic 1. Flip-flop no. 1 now contains a logic 1, FF-2 a logic O, and FF-3 a logic 1.

The final digit of the binary word now appears at the serial input of flip-flop no. 4. Since this digit is a logic 1, flip-flop no. 4 again assumes the logic 1 state.

Since no more shift and clear pulses are applied at this time, the register now contains the binary word made up of the bits 1101, which is equivalent to the decimal number 13. To remove the word from the shift register, a pulse train of four shift and clear pulses is required.

## COMPLEMENT REGISTER

#### Application.

A complement register is used in digital computer circuitry to temporarily store a logic word or the complement of a logic word applied to the register.

## Characteristics.

Flip-flops are used to provide bistable operation states.

Each flip-flop has a separate set and clear input.

AU flip-flop stages are complemented simultaneously by a single trigger pulse.

# Circuit Analysis.

General. The logic diagram of a typical three stage complement register is shown in the following illustration. The register consists of three flip-flops, each having three inputs: set (S), complement (T), clear (C), and two outputs-one and zero. Each of the flip-flops are activated individually to a logic 1 or logic Ooutput state depending upon the individual set input trigger voltages of each stage. Each flip-flop is, likewise, individually cleared by pulses applied to the individual clear inputs of each stage. The word stored in the register, however, can only be complemented when a single complement trigger pulse is applied to the complement trigger pulse input. This trigger pulse appears simultaneously at one input of three individual AND gates. The other input of each AND gate is a logic 1 obtained from the zero or one output of each flip-flop. The output of the AND gate then is applied to the other half of the flip-flop, resting in either the one or zero state, which did not produce a logic 1. Thus, by simultaneously triggering the clear and set inputs, the flip-flops are all changed in state, or complemented.



Complement Register

**Circuit Operation.** The schematic of a typical three stage complement register is shown in the following illustration. Resistors R1 through R6 are collector load resistors: resistors R7 through R18, in conjunction with voltage source –V, form a voltage divider networks for providing anode voltages for triggering diodes CR] through CR6. Resistors R19 through R24 drop the voltage from voltage source +V to AND gate diodes CR7 through CR18. Transistors Q1 through Q6 are flip-flop transistors.



Complement Register

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Prior to any input pulses being applied, all of the flip-flops are in the logic O state. In this condition, transistors Q2, Q4, and Q6 are conducting, and transistors Q1, Q3, and Q5 are not conducting. Assume a positive input is then applied to the set inputs of the first and the last flip-flop stage, representing a logic 1 input. A logic O input is represented at the second flip-flop stage, since no positive pulse is applied to the set input of the second flip-flop stage.

The positive pulse applied to the set input of the first stage flip-flop is coupled across capacitor C3, is greater in amplitude than the negative anode supply voltage of diode CR2, and forward biases CR2 causing CR2 to conduct. Thus, a positive reverse bias voltage appears on the base of transistors Q2. As a result, Q2 stops conducting, collector current no longer flows through load resistor R2, and no voltage drop appears across R2. The collector of Q2 then rises to the supply voltage and the base of Q1 is forward biased, hence, transistor Q1 conducts. Collector current flows through collector load resistor R1, producing a voltage drop across R], and the collector voltage of Q1 rises to the zero volt level. The state of the fLip-flop is now opposite to the initial logic O state; a logic 1 output state is now represented.

The positive (logic 1) pulse applied to the set input of the last flip-flop causes a reversal of state in the same manner. Since there is no positive (logic 1) pulse applied to the set input of second flip-flop stage, the second stage remains in the initial logic O state.

At the end of the first series of applied set input pulses: Q1 is conducting, Q2 is not conducting, Q3 is not conducting, Q4 is conducting, Q5 is conducting, and Q6 is not conducting. The positive going (zero) voltage on the collectors of Q1, Q4, and Q5 appear at the cathodes of diodes CR8, CR13, and CR16, respectively. These diodes are thus prevented from conducting while the flip-flops are in this state. When a positive pulse is applied to the complement trigger input, didoes CR7, CR10, CR11, CR14, CR15, and CR18, can not conduct. At this time, a coincidence of positive pulses exists at the cathodes of some of the AND gate diodes. Diodes CR7 and CR8 of the first AND gate have positive cathodes voltages, thus preventing them from conducting. As a result, no current flows through resistor R19 and no voltage is dropped across R19. Therefore, the positive supply voltage, +V, overcomes the negative voltage on the anode of CR1, allowing CR1 to conduct. A positive

voltage appears on the base of Q1, reverse biasing Q1 so that it does not conduct. No collector current flows through resistor RI, and no voltage drop occurs across R1. The negative collector supply voltage which now appears at the collector of Q1 also appears at the base of Q2, forward biasing Q2 into conduction. The state of this **first** flip-flop in the complemented position now corresponds to the initial logic O state.

Diodes CR13 and CR14 of the third AND gate have positive voltages applied to their cathodes, reverse biasing them and preventing current flow through resistor R22. The voltage applied to C8 rises "" towards the positive supply voltage, +V, and this positive swing is applied to the anode of diode CR4, which now conducts and applies a positive swinging voltage to the base of transistor Q4. Transistor Q4 is thus held reverse-biased so it will not conduct. Consequently, no collector current flows through collector load resistor R4, allowing the collector of Q4 and the base of Q3 to rise to the negative collector supply voltage. Transistor Q3 is now forward biased and conducts. Collector current now flows through resistor R3, and the supply voltage is dropped across R3. The state of the complemented second flip-flop now corresponds to a logic 1.

Diodes CR15 and CR16 of the fifth AND gate have effectively positive voltages applied to their cathodes resulting in a change of state of the last flip-flop from logic 1 to logic O by reverse biasing Q5 through CR5 and capacitor C9 in the same way that the first flip-flop changed state. The logic of each stage is, therefore, reversed with the application of a single complement trigger pulse.

If it is necessary to clear the register, a positive clear pulse must be individually applied to each stage containing a logic 1. Since the second flip-flop stage is the only one in a logic 1 state, a positive clear pulse must be applied to the second stage clear input, across capacitor C6, through diode CR3 to the base of Q3. Q3 is thus reverse biased so that it does not conduct. No collector current flows through resistor R3, and no voltage is dropped across it. The collector of Q3 and the base of Q4 then rise to the negative collector supply voltage. Q4 is then forward biased, so that it conducts heavily. The second flip-flop stage is now returned to the logic O state, and the register is completely cleared.

# DOUBLE-LINE TRANSFER REGISTER

# Application.

The double-line transfer register used in digital computers, when it is desirable to retain a logic word in one register, but also to be able to transfer the logic word to another register with the application of a single pulse.

## Characteristic.

**Two** single registers make up the double-line register.

Each single register consists of a series of flip-flops. A series of AND gates couple one register to the other.

A transfer pulse input is required to complete the transfer of the logic word from one register to another.

## Circuit Analysis.

**General.** The double line transfer register consists of two single flip-flop registers connected by means of a series of AND gates. A logic word is originally recorded in one logic register. The logic of the word is applied to one input of the applicable AND gate. With the application of single transfer pulse, certain AND gates will have the required simultaneous presence of two input pukes, and conduct. The conduction of the AND gate applies a pulse to an input of a flip-flop in the second register, corresponding to the output of the first register flip-flop. In this way, the second register logic corresponds to the first register logic.

**Circuit Operation.** The logic diagram of a typical double-line transfer register is shown in the accompanying illustration. The primary register consisting of flip-flops FFY-1, FFY-2, and FFY-3 is the storage input register to which the logic word is applied. AND gates AG1, AG2, AG3, AG4, AG5, and AG6 transfer the logic stored in the input register to the second register, flip-flops FFX-1, FFX-2, and FFX-3.



**Double-Line Transfer Register** 

A logic 1 pulse applied to the set input of flip-flop FFY-1, and FFY-2, and a logic 1 pulse applied to the clear input of flip-flop FFY-3, develops a logic word of 110 in the input register. Logic pulses then appear at AND gates AG no. 2, AG no. 4, and AG no. 5 from the input register. When a transfer pulse is applied, it appears simultaneously at the other input of each of the AND gates. Since AND gates AG no. 2, AG no. 4, and AG no. 5 now have pulses simultaneously applied to both inputs they each produce an output. The output of AND gate AG no. 2 is applied to the set input of flip-flop FFX-1; the output of AND gate AC no. 4 is applied to the set input of flip-flop FFX-2; and output of AND gate AG no. 5 is applied to the clear input of flip-flop FFX-3. The second register now has a logic word of 110 inserted, which corresponds to the stored logic word of the input register. If it is desired to clear the second register, individual clear pulses must be applied to each flip-flop of the input register, and a transfer pulse must be applied to activate AND gates AG no. 1, AG no. 3, and AG no.

5 which are coupled to the logic zero output of the input register. The outputs of AND gates AG no. 1 AG no. 3, and AG no. 5 are coupled to the clear inputs of the second register flip-flops FXX-1, FXX-2, and FFX-3. Thus, each of the second register flip-flops is cleared to a logic O state.

### CIRCULATING REGISTER

## Application.

**The** circulating register is used in digital circuitry as a dynamic storage device to continuously circulate a logic word through the register until another logic word is applied.

## Characteristics.

A shift register, two AND gates, an OR gate, and a flip-flop form a circulating register.

Three inputs and one output are provided.

A separate train of pukes operates the shift register.

Circulation continues as long as a circulate input is applied.

A read-in input will clear the register.

The output may be used over and over again.

## **Circuit Analysis.**

**General. The** circulating register, consisting of a control flip-flop, a shift register, two AND gates and an OR gate. Also, it retains a logic word when the applied word occurs at the same time that a pulse is applied to the read-in input of the flip-flop. The logic word is then retained in the shift register portion of the circulating register. This word continues to circulate through the register once an input is applied to the circulate input of the control flip-flop. When the flip-flop changes state again the shift register is cleared, and will accept a new logic word if it is applied to the word-input terminal.

**Circuit Operation.** The logic diagram of a typicrd circulating register is shown in the accompanying illustration. The two states of the control flip-flop determine whether or not a new logic word will be accepted in the register, or if the word already inserted in the register will be recirculated. AND gate no. 1 has one its two inputs supplied with pulses from the output of the shift register, and the other input is supplied with pulses from the zero output of the control flip-flop. An output from AND gate no. 1

applied to OR gate no. 1 causes the recirculation of a logic word in the register.



#### **Circulating Register**

One input to AND gate no. 2 is from the one output of the control flipflop, and the other input to AND gate no. 2 consists of the pulses or bits of the new logic word which is to be inserted into the register. The output from AND gate no. 2 applied to OR gate no. 1 then, causes the word in the shift register to be replaced with a new logic word. OR gate no. 1 allows an output from either AND gate no. 1 or AND gate no. 2 to be used to operate the shift register, and to either circulate the word, or to insert the new word, respectively.

If a logic word of 1011 is applied to the word input, a logic 1 output must be generated by the control flip-flop at the one output, and last for the entire period of the applied word pulses. The control flip-flop produces this logic 1 output when a logic 1 pulse is applied to the set input (S) of the control flip-flop. The logic 1 output of the control flip-flop and the 1011 applied logic word appear at the two inputs of AND gate no. 2 and produce a 1011 output from AND gate no. 2, which also appears at the input of OR gate no. 1. OR gate no. 1 then produces a 1011 output. The logic word 1011 thus is serially applied to the shift register, and it may then continue to circulate the logic word, accept a new logic word, or be cleared. To continue to circulate the logic word, logic 1 pulses must continually be applied to the shift pulse input to serially move the logic word of 1011 through the shift register to the output, and then to one input of AND gate no. 1. The control flipflop is

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then made to change state by applying an input pulse to the circulate (C) input of the flip-flop, so that a logic 1 is now produced at the zero output. The logic 1 at the zero output of the control flip-flop also appears at the other input of AND' gate no. 1. As a result, AND gate no. 1 produces a serial output of 1011, which appears at one input of OR gate no. 1. Hence, OR gate no. 1 applies the logic word 1011 to the shift register, which flop, so that a logic 1 is now produced at the zero output. Serially accepts the word as soon as three shift pulses are completed. Continuous application of the shift pulses causes the word to be read-out into AND gate no. 1 again and back through OR gate no. 1 into the shift register. This circulation continues as long as the control flipflop zero output remains at a logic 1 and shift pulses continue to be applied to the shift register.

When a new logic word, say 1100, is to be inserted into the register, it is applied to the word input of AND gate no. 2 and a read-in pulse is applied to the (S) input of the control flipflop. Hence, the flip-flop changes state so that a logic 1 is produced at the one output of the flip-flop and is simultaneously applied to the other input of AND gate no. 2. Meanwhile, AND gate no. 1 no longer produces an output, since one of its inputs from the zero output of the control flip-flop is no longer a logic 1 and circulation ceases. AND gate no. 2 now produces an output of 1100, which passes through OR gate no. 1 to the shift register. With the application of three shift pulses this word is accepted in the register. Additional shift pulses bring the logic word of 1100 to the output of the register and apply it as one input to AND gate no. 1. If the control flip-flop remains in the same state (a logic 1 from the one output) and there is no new logic word applied, the circulating register is cleared. If the flip-flop is made to change state again, the logic word 1100 is now circulated.

## ACCUMULATOR REGISTER

#### Application

The accumulator register is used in digital circuits to store a given binary number, or to add another binary number to the stored number, and store the sum of the two binary numbers.

#### Characteristics.

The accumulator register consists of a series fulladder and a shift register.

With a two stage adder and a three stage shift register, two OR gates, two inhibit gates, two AND gates, three delay lines, and three flipflops are used in the accumulator register.

The output of the full-adder is the input to the shift register, and the output of the shift register is the augend input of the adder.

#### **Circuit Analysis**

**General. The** accumulator register consists of a combination of two logic circuits previously discussed in this section of this handbook-the series full-adder and the shift register. A logic word or binary number is applied to the addend input of the series full-adder. If there is no logic word or binary number applied to the augend input of the series full-adder, the word applied to the addend appears at the output of the adder as the sum. The logic word is then sequentially read into the shift register by applying the required number of shift pulses to the shift register. This logic word or binary number then remains in the shift register until additional shift pulses remove it.

A binary number which is stored in the shift register may be added to another binary number. It is ordy necessary to apply the proper number of shift pulses to the shift register to remove the binary number, and simultaneously apply it to the augend input of the adder when the number to be added appears at addend input of the adder. The two numbers are then added together in the adder and appear at the sum output of the adder. This sum is read into the shift register by applying the proper number of shift pulses to the shift pulse input.

**Circuit Operation. The** logic diagram of a three-bit accumulator register is shown in the following illustration. One half of the series full-adder is made up of OR gate no. 1, AND gate no. 1, and inhibit gate no. 1. Diodes CR1 and CR2 and delay line DL-1 separate the first half-adder from the second half-adder consisting of OR gate no. 2, AND gate no. 2, and inhibit gate no. 2. The shift register consists of flip-flops FF-1, FF-2, and FF-3, and delay lines DL-2 and DL-3.

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#### Accumulator Register

If a logic word of 101 is applied to the accumulator register, it appears at the addend input. OR gate no. 1 passes the logic word on to the non-inhibiting input of inhibit gate no. 1. Since AND no. 1 does not have simultaneous logic inputs, no output is produced. Therefore, no input is applied to the inhibiting input of inhibit gate no. 1; likewise, no input is applied to diode CR1. Inhibit gate no. 1 now passes the logis word 101 to one input of OR gate no. 2, and AND gate no. 2. Since there is nothing applied through diode CR1 to delay line DL1, no input appears at the other inputs to OR gate no. 2, and AND gate no. 2. OR gate no. 2 therefore passes the logic word of 101 to the non-inhibiting input of inhibit gate no. 2. Since there is no input applied to the inhibiting input of inhibit gate no. 2, the logic word emerges from the inhibit gate and appears at the set input of flip-flop FF-3. Since a flip-flop is only capable of reacting to one pulse at a time, flip-flop FF-3 becomes a logic 1 as a result of the first logic 1 pulse of the logic word. A shift pulse is timed to occure between the first and second word bit pulse. This shift pulse returns FF-3 to logic O and passes the logic 1 pulse to flip-flop FF-2 after a slight delay, caused by delay line DL-3. The delay is used to prevent the bit from appearing at FF-2 while the shift pulse is still being applied. Flip-flop FF-3 remains in the logic O state even after the second pulse of the logic word appears at FF-3, since the second pulse is a

logic O. Some time after the second word pulse, another shift pulse is applied to the clear input of all flip-flops. Flip-flops FF-2 and FF-3 shift the word pulses retained in them to the subsequent flip-flop stage after another short delay, so that flip-flop FF-1 is now a logic 1, FF-2 is a logic O, and FF-3 is a logic O and awaiting the next word pulse. The third and final word pulse of logic 1 appears in FF-3, The word is then retained in the shift register until additional shift pulses are applied to the shift register.

If a binary number is to be added to the binary number already in the register, the number is applied to the addend input of the series full-adder. Shift pulses are applied to the shift register to move the binary number to the augend input. The first shift pulse is applied so that the first bit of the stored word appears at the augend input when the first bit of the applied word appears at the addend input. Subsequent shift pulses are timed so that additional bits of the stored word coincide with additional pulses of the applied word. Assume that a binary number 010 is to be applied to the addend input of the series full-adder and the binary number 101 is stored in the register. When a shift pulse is applied to the flip-flop stages of the shift register it moves each pulse of the stored word one place to the left, causing the first logic 1 bit of the stored word to appear at the augend input; the first bit of the applied word (logic O) appears at the addend input at the same time. Since the addend bit is a logic O and the augend bit is a logic 1, only the OR gate will produce a logic 1 output. This logic 1 appears at the non-inhibiting input of inhibit gate no. 1. Since AND gate no. 1 produces no logic 1 output, there is no logic 1 applied to the inhibiting input of inhibit gate no. 1. Inhibit gate no. 1, therefore, develops a logic 1 which then passes through OR gate no. 2, and inhibit gate no. 2, in the same way it passed through the first half of the adder. The logic 1 emerges from the adder and appears at the set input of flip-flop FF-3 changing the state to logic 1. Another shift pulse is then applied to the shift register, and moves each pulse of the stored word one place to the left. The next bit of the stored word (logic O) appears at the augend input of the adder. The logic 1 bit, developed by the adder and accepted by FF-3, is shifted to FF-2. When the logic O stored

word bit appears at the augend input, the second bit of the applied word also appears at the addend input. In this case, as in the case of the first augend and addend bit, there is only one logic 1 applied to the adder. As a result, another logic 1 is developed at the output of the adder, and appears at the set input of FF-3, changing flip-flop FF-3 to logic 1. Another shift pulse moves the bits stored in the accumulator register one place to the left. The last logic 1 bit of the originally stored word now appears at the augend input of the adder. At the same time, the last bit of the applied word (logic O) appears at the addend input of the adder. Since, as in the first and second addend and augend bits, there is only one logic 1 appearing at the inputs of the adder, the output of the adder is a logic 1. This logic 1 now appears at the set input of flipflop FF-3 resulting in all flip-flops being a logic 1. The resulting logic word is the sum of the initially applied word -101, which was also the first word stored in the register, and the second applied word -010. The following examples of a logic sum indicates the validity of the sum of the two applied words.

#### **Binary Decimal**

	1st	2nd	1st	2nd
	Addition	Addition	Addition	Addition
Augeno	1 0 0 0 E	101	0	5
Addend	101	010	5	2
Sum	101	111	5	7

## PART 16-6. MEMORY DEVICES

## **MEMORY DEVICES (GENERAL)**

Memory is a term which describes the ability of circuits used in computers to retain binary logic in electrostatic, ferroelectric, magnetic, acoustic, optical, chemical, electronic, electrical, or mechanical form. In addition to storing binary information, the memory device must readily provide logic information to other circuits in the computer; this ability is referred to as access. The amount of binary information which is capable of being stored is referred to as capacity. The access time, as well as the degree of capability of the memory to retain binary information when no power is applied to the computer is called *volatility*. *Permanence* is the degree by which binary information can be removed. Access time can be further broken down into random (static) access or sequential (dynamic) access. Random or static access provides information to a desired circuit from any portion of the memory without requiring the physical movement of the memory device. On the other hand, sequential access only provides information after the physical movement of the memory device, whether it be cyclic or progressive.

The magnetic core memory, which is a random access memory and the magnetic drum, the magnetic disc, and the magnetic tape memories, which are sequential access memories and fully discussed in the following paragraphs. The memory driver circuit and the data memory circuit, which are merely related memory operating circuits are also discussed.

# MAGNETIC CORE MEMORY

## Application.

A magnetic core memory is used for the retention and storage of binary logic information until it is needed by other sections of the computer.

#### Characteristics.

Each core is capable of retaining a single bit of logic information.

A typical magnetic core memory may retain between 10 and 100,000 characters of logic information. The core memory provides low access time (rapid access).

The access is either static or random.

The stored logic information may be erased.

Logic information is not removed if power is removed.

Memory core consists of ferromagnetic material threaded with four conductors.

#### Circuit Analysis.

**General.** The core type of memory consists of a number of ferromagnetic cores arranged in matrix planes.

Every core within the memory has four conducting wires extending through it. One wire extends through every core in a horizontrd line, another wire extends through every core in a vertical line as shown in the following illustration. There are then as many vertical wires as there are vertical lines of cores, and as many horizontal wires as there are horizontal lines of cores. These vertical and horizontal lines are called address wires. A current flowing through one horizontal and one vertical wire induces magnetic lines of force about one core. The lines of force may be produced in either of two directions, depending upon the direction of current flowing through the address wire. Lines of force in one direction represents a logic 1, and lines of force in the other direction represents a logic O. Once the lines of force are produced they remain about the core, even after the activating current is removed. Cores through which either, but not both, conducting wires extend do not react, since one wire supplies only half of the current needed to change the direction of the lines of force. In addition to the address wires there are two other wires which pass through the core. One of these wires is the sense wire, which is used to read out logic information. The other wire is the inhibit wire which prevents cores in other planes, that also have the conducting address wires passing through them, from simultaneously changing the direction of their magnetic lines of force. By using more than one memory plane a logic word can be stored in the core matrix either vertically, horizontally, or through the planes (one bit of a logic word in each plane). If a single plane is used, the logic word may only be stored vertically or horizontally. An inhibit wire is not necessary in a single pkme matrix.



## **Typical Memory Core**

**Circuit Operation.** The representation of a magnetic core memory plane utilizing single cores is shown in the following illustration. The complete plane contains eighty-one ferromagnetic cores. The wires X1 through X9 are the vertical address wires; wires Y1 through Y9 are the horizontal address wires; and the dotted line running through every core represents the sense wire or winding.





#### **Core Memory Plane**

In the case of the single-core memory plane, shown in the preceding illustration, nine 9-digit logic words may be stored horizontally or vertically. If the memory consisted of nine planes, eighty-one nine digit

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#### Hysteresis Loop

Assume initially that the core has no magnetism. This is represented by point X (the origin). If sufficient current is now passed in the positive direction the magnetic flux increases along the dotted line and eventually reaches saturation at point a. (The core is said to be saturated when an increase in current does not result in an increase in magnetic flux.) If the

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current is then removed, a slight decrease in magnetism occurs, causing the magnetic flux point to move from a to b, where it is held by residual magnetism. If the core is now magnetized by a current flowing in the negative direction, the magnetism will be reversed. The magnetic flux will now reduce and traverse around the knee of the curve down to point c. This point corresponds to saturation in the opposite direction. When the pulse is removed, the point on the curve will change to d which represents the residual magnetism induced by that pulse. From here on, when the magnetism is switched (reversed) in either direction, the change in flux will follow the path a, b, c, d.

If a binary word of 101111001 is to be stored along the Y5 horizontal address line, a positive current is applied to Y5 and to vertical address lines Xl, X3, X4, X5, X6, and X9. Since the current of each of these address points (the core where the conducting X and Y wires would intersect) is positive the flux density increases to point a on the hysteresis curve representing a logic 1 state (regardless of the previous state of the cores, since those already saturated positively will not change). Hence, all the ones are inserted at once. A negative current is then applied to Y5 and to the vertical address lines X2, X7, and X8 of the matrix. Since the current at these address points is negative, the flux density decreases to point d on the hysteresis curve, presenting a logic O state. All the zeros are now inserted and the logic word now exists in the memory. The logic word remains in the memory until removed by applying negative current to the horizontal Y5 wire and to each of the vertical X wires. This allows the stored logic word to be applied to some other area of the computer, but removes the logic word from the memory completely. In this way, use of the stored logic word destructs the stored word in the memory. In order to avoid this destructive read-out, additional citcuitry must be used to return the logic word to the same position in the memory.

# MEMORY DRIVER CIRCUIT

## Application.

The memory driver circuit provides a means of reinserting any logic word, read out of a core memory, into the same address in the memory, for further storage.

#### Characteristics.

Each vertical address line has a separate memory driver circuit.

The memory driver circuit consists of three transistors, a center tapped transformer an AND gate, and an OR gate.

Requires simultaneous application of a read-out pulse and an output from the memory core.

## Circuit Analysis.

General. A memory-driver circuit re-inserts the stored logic word into a magnetic core memory after it is read out into the sense winding for use elsewhere in the computer. The circuit, consisting of three transistors, a center-tapped transformer, an AND gate and an OR gate, provides the necessary feedback action to return the digit flip-flops, which are connected to the vertical address rows, to the previous storage logic state. Two of the Transistors respond to the state of the flip-flop, after being gated on by the other transistor and, in turn, activate an address winding of a memory core to correspond to the flipflop state. When the logic in a core is to be read out, the associated flip-flop is placed in the zero state, and the gating transistor activates the other two transistors to respond to the logic O state. If the core is in the logic 1 state the current flow through the transformer and the address winding develop a logic 1 in the sense winding. This would normally leave the core in a logic O state; however, the logic 1 from the sense winding is fed back through the AND gate and the OR gate to the logic 1 input of the flip-flop. The core is then returned to the logic 1 state. If the core was originally in the logic O state there is no change in the state of the core and, thus no need to activate the output of the sense winding to change the flip-flop state.

**Circuit Operation.** The schematic of a typical memory driver circuit is shown in the following illustration, along with one vertical and two horizontal address lines. Windings L] and L3 are sense


**Memory Driver Circuit** 

windings of the two memory cores; windings L2 and L4 are address windings of the two cores; L5 and L6 are the primary and secondary windings of a centertapped transformer used to couple logic information from the flip-flop through either of transistors Q3 or Q4 to the data memory circuits consisting of transistors Q1 and Q2 (this circuit is discussed later in this section of this handbook). AND gate no. 1 couples the output of a sense winding through OR gate no. 1 to the flip-flop when a readout signal is applied to the other input of the AND gate. OR gate no. 1 allows the flip-flop to be activated to a logic 1 state by either a pulse applied to the input or a re-insertion signal.

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If, initially, the flip-flop is placed in a logic 1 state by a negative pulse applied to the 1-input of the flipflop through OR gate no. 1, the flip-flop develops a negative pulse at its l-output. This negative pulse forward biases transistor Q3. Q3 ordy conducts if a negative demand signal pulse is applied to the base of Q5, so that Q5 conducts to provide a complete current path for Q3. The conduction of Q3 allows current to flow from  $-V_{cc}$ , through L5, through Q3, and through Q5 to ground. As a result of current flow through L5, L6 develops a current flow 180° out of phase (or in the opposite direction) to the current flow in L5. The current then flows from ground through one half of L6, from the collector of Q2 or Q1 to the emitter, and through L4 or L2 and the other half of L6 to ground. The activated address line determines the current flow through Q1 and L2 or Q2 and L4. As a result of the current flow through L2 or L4, the associated core is driven to a logic 1 state. The current developed in the sense winding of the activated core is 180° out of phase with the current of the address winding; the sense winding, then, produces a logic O output.

When the logic 1 is to be read-out of the activated core, the flipflop is placed in the logic O state by a negative pulse applied to the O input, and a negative demand signal is applied to the base of Q5 to cause Q5 to conduct. A negative pulse is produced at the O output of the flip-flop and appears at the base of Q4. Q4 is thus forward biased into conduction, and provides a current path for half of transformer primary winding L5. Current then flows from  $-V_{cc}$  through half of L5, through Q4 and Q5 to ground. The current flow through L5 induces a current through L6 which is 180° out of phase with the current through L5.

Note that the polarity of the voltage induced in winding L6 is now reversed and that transistors Q1 and Q2 have a positive voltage applied to the collector from one side of L6, and a negative polarity applied to the emitter through L2 and 1A and the other side of L6. This corresponds to the special condition (discussed in section 3 of this handbook) where the transistors act as if they were connected in the inverted condition (emitter connected to what would normally be the collector lead, and the collector connected to what would normally be the emitter lead). As a result there is a change from normal operation. When operated as a switch, a transistor will

conduct in either direction, depending upon the applied polarity. Normally, the emitter is forward biased and the collector is reverse biased, and the electron current flow is in the direction opposite the arrow on the schematic symbol. When operated in the inverted condition, the normal emitter and collector leads may be transposed, or, the biasing polarities are reversed. Thus forward biasing the collector and reverse biasing the emitter produces exactly the same result as the transposed connection. Likewise, when inverted, the collector actually acts as an emitter, while the emitter serves as the collector. Both functions are interchanged and current flows in the opposite direction just as if the schematic symbol was reversed. The reverse current flow is usually from 0.3 to 0.6 times the normal value. (When analyzing the switching operation of transistor circuits bear in mind the fact that the transistor will always conduct in either direction as long as the base bias is such as to bias either junction in a forward direction. Similary, the transistor will be cut off only when both junctions are biased in the reverse direction.)

As a result of the reversed polarity connection, current now flows from ground through half of L6, through L4 and L2, from emitter to collector of Q1 or Q2, through L2 or L4 and through the other half of L6 to ground. The direction of current flow through L4 or L2 now is opposite in direction to the normal flow when a logic 1 was developed. The associated core is driven to a logic O, and the 180° outof-phase current through the sense winding represents a logic 1 in the sense winding. This logic 1 (negative) pulse appears at one input of AND gate no. 1. If a negative readout signal pulse appears at the other input of the AND gate, a logic (negative) pulse output is developed and appears at the re-insertion input of OR gate no. 1. OR gate no. 1, in turn, develops a logic 1 output, causing the flip-flop to develop a logic 1 (negative) output. Q3 then conducts when Q5 conducts to provide Q3 with a current path as a result of the negative pulse appearing at the base of Q3. The conduction of Q3 develops a current flow through L5, which develops an opposite current flow through L6 (by induction) and produces a logic 1 in the address winding (L2 or L4) which formerly was activated to logic O, so that a logic 1 is developed in the associated sense winding.

If the state of the core (and the flip-flop) is originally in the logic O state, there is no need to activate the output of the sense winding to the flip-flop when reading-out, since the flip-flop is put in the logic O state and will read out a logic O.

## DATA MEMORY CIRCUIT

## Application.

The data memory circuit is used to insert (writein) and read out logic information in a magnetic core of a computer memory bank.

## Characteristics.

**The** circuit primarily operates as a transistor current switch.

The y-axis pulses are supplied by flip-flops.

The y-axis pulses are applied to either the emitter or the collector of the driving transistor.

The x-axis pulses are applied to the base of the transistor.

#### Circuit Analysis.

**General.** A data memory circuit uses a single PNP type transistor to control each magnetic core in the memory. The x-input is applied to the base of the transistor, and the y-input is applied to either the emitter or collector of the transistor. The transistor then produces a logic 1 or logic O output (which is stored in the core). Thus, this circuit provides a means of controlling the state of the memory core by an external input signal, which requires only a single address winding through the core to produce this result.

**Circuit Operation.** A typical three-line data memory circuit is shown in the following illustration. Resistors RI through R6 are flip-flop load resistors. Transistors Q1 through Q9 are connected as emitter-follower transistors which are capable of conducting in either direction to activate the logic core winding to a logic 1 or logic O state. Windings L2, L4, L6, L8, L1O, L12, L14, L16, and L18 are the address windings for memory cores; windings L1, L3, L5, L7, L9, L11, L13, L15, and L17 are the sense windings. X1, X2, and X3 are the three horizontal address lines. Y1, Y2, and Y3 are vertical address lines. Flip-flop 1 supplies vertical address line Y1; flip-flop 2 supplies vertical address line Y2; and flip-flop 3 supplies vertical address line Y3.



**Data Memory Circuit** 

To write a logic word into the core memory, the states of the memory flip-flop must correspond to the applied logic word. If a logic word of 101 is to be stored in the memory, flip-flop 1 must be in the logic 1 state, flip-flop 2 in the logic O state, and flip-flop 3 in the logic 1 state. The state of the flip-flops are controlled by inserting either a 1 or a O (the O input is opposite in polarity to the 1 input) into the respective 1 and O inputs. The flip-flop states do not affect the memory, however, until one of the horizontal (x) address lines is activated by a negative logic 1 pulse, since zero base bias exists without an x-input. If, for example, line X2 is activated by a negative pulse, the bases of Q4, Q5, and Q6 are forward biased and conduct. Transistor Q4 has a negative pulse applied from the 1 output of flip-flop 1 to the collector, while a zero or effective positive voltage is applied to the emitter

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from the O-output. Thus, Q4 conducts from collector to emitter producing an electron current flow through address winding L8, which causes the associated memory core to become a logic 1.

Note that transistor Q5 now has a negative pulse applied to the emitter from the O output of flip-flop 2, while the collector of Q5 has an effective positive pulse or a O applied from the l-output, since flip-flop 2 is in the opposite state to flip-flop 1. This corresponds to the special condition discussed in section 3 of this handbook where the transistor acts are if it were connected in the inverted condition (emitter connected to what would normally be the collector lead, and the collector connected to what would normally be the emitter lead). As a result there is a change from normal operation. When operated as a switch, a transistor will conduct in either direction, depending

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upon the applied polarity. Normally, the emitter is forward biased and the collector reverse biased, and the electron current flow is in the direction opposite the arrow on the schematic symbol. When operated in the inverted condition, the normal emitter and collector leads may be transposed, or, the biasing polarities are reversed. Thus, forward biasing the collector and reverse biasing the emitter produces exactly the same result as the transposed connections. Likewise, when inverted, the collector actually acts as an emitter, while the emitter serves as the collector. Both functions are interchanged and current flows in the opposite direction just as if the schematic symbol was reversed. The reverse current flow is usually from 0.3 to 0.6 times the normal value. (When analyzing the switching operation of transistor circuits, bear in mind the fact that the transistor always will conduct in either direction as long as the base bias is such as to bias either junction in a forward direction. Similarly, the transistor will be cut off only when both junctions are biased in the reverse direction.)

As a result of the inverted polarity, Q5 now conducts in the opposite direction from emitter to collector producing an electron current flow through address winding L1O (in a direction opposite to that in L8) which causes the associated memory core to become a logic O. Because of the negative logic 1 pulse applied to the collector of Q6 from flip-flop 3, Q6 conducts in the normal direction from collector to emitter making the memory core associated with L12 a logic 1. This logic word remains in the core memory until the word is read out of the memory.

When the word is to be read from the memory, a negative pulse is applied to the X2 line, and a negative pulse is developed by the O output of each flip-flop. Current flows in the inverted direction from emitter to collector in each of the X2 transistors, and the original direction of current flow in L8 and L12 is reversed. This current reversal induces a current in sense windings L7 and L11, which is 180° out of phase with the original direction of current through L8 and L12. Since L8 and L12 are now a logic O, sense windings L7 and L1 1 now produce a logic 1. Since there was no change in the direction of current through L1O, no current is induced in the associated sense winding, L9, and a logic O is read out. The logic word read out then corresponds to the logic word which was stored in the memory. Once the logic word is read out, however, no logic word remains in the core memory along with X2 address line. This is

known **as a** destructive read-out, since the X2 memory cores are now effectively empty.

## MAGNETIC DRUM MEMORY

## Application.

The magnetic drum memory is used in computers to provide an inexpensive means of storing large amounts of binary information.

### Characteristics.

Magnetic drum memory has sequential and cyclic access capabilities at medium speeds.

The magnetic drum memory has large storage capabilities.

Stored logic is not lost when power is removed, but stored logic may be erased.

#### Circuit Analysis.

General. A magnetic drum memory consists of a large metal cyclinder, which is dipped or sprayed with an oxide coating to provide magnetic hysteresis characteristics similar to those of magnetic cores, and external magnetic core heads for writing in and reading out binary logic. The drum is arranged in radial rows (around the drum) and horizontal rows of cells. The radial rows of cells are called tracks, and the horizontal rows are called slots. Each cell is capable of storing one bit of logic. The drum continually rotates under but does not touch the horizontally aligned cores. (The number of cores corresponds to the number of cells in a slot). Conducting wires extend through and are wound around each core. When binary digits are to be read into certain cells of the drum, current is applied through the core windings at the time a particular slot of cells passes under the heads. The current through the core windings causes a magnetic flux to be developed through and around the core which, in turn, polarizes a cell surface of the dmm to a logic 1 or a logic O. The magnetic flux about all of the cores then causes all of the cells in a specific slot to retain the appropriate logic in the memory.

When the binary logic in a slot is to be read-out the precedure is reversed. The slot appears under the horizontal row of read-out heads, where the magnetic polarization of the cells develops the appropriate direction of magnetic flux about and through the cores, which, in turn, induces a current through the conducting wires would around the cores. The direction of current flow through the conducting wire determines if the bit being read-out is a logic 1 or logic O.

**Circuit Operation.** A pictorial representation and a one-line diagram of a typical magnetic-drum memory is shown in the following illustration.





The pictorial representation shows the magnetic drum with its arrangement of cells and magnetic core heads. The one-line diagram shows the magnetic drum, the write head used to write-in binary data to the cells of the magnetic drum, and the read head used to read-out data from the cells of the magnetic drum. AND gate no. 1 is used to supply logic-l write pulses to the write head when write logic-l pulses and write timing-pulses are applied to the AND gate inputs at the same time. AND gate no. 2 is used to supply write logic-O pulses to the write head when logic-O pulses and write timing-pulses are applied to the AND gate inputs at the same time. Flip-flop no. 1

provides logic-l data and logic-O data to AND gates 1 and 2. Transformer T1, consisting of primary L1 and secondary L2, couples the logic data from AND gate nos. 1 and 2 to the write head and the drum through L3. Winding L4 couples logic data read from the magnetic drum to transformer T2. Transformer T2 provides logic-l and logic-O pulses to flip-flop no. 2 The logic-l pulses developed by flip-flop no. 2 are applied to AND gate no. 3, which develops an output when the read timing-pulses appear at the other input of AND gate no. 3 at the same time the logic-l pulses are applied. The logic-O pulses developed by flip-flop no. 2 are applied. The logic-O pulses developed by flip-flop no. 2 are applied. The logic-O pulses developed by flip-flop no. 2 are applied to AND no. gate 4, which develops

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an output when the read timing-pulses appear at the other input of AND gate no. 4 at the same time the logic-O pulses are applied.

If a logic word of 101 is to be read-in on a track of cells, a positive pulse is first applied to the set input of flip-flop no. 1, which develops a positive pulse at the l-output. If this positive pulse appears at one input of AND gate no. 1 at the same time a write timing-pulse is applied, AND gate no. 1 conducts and produces current flow through half of winding L1 to voltage source +V. The current flow through L1 induces a current 180° out of phase with the L1 current winding L2. The current induced in L2 flows through winding L3, which develops a flux in the write head. The flux of the write head causes a cell on the magnetic drum, which happens to be directly under the write head as the flux is developed, to become polarized. The polarization of the cell represents a logic 1.

The next bit of the applied word is a logic O. In this case a positive pulse is applied to the clear input of flip-flop no. 1, causing the O-output of the flip-flop to develop a positive pulse. If this positive pulse appears at one input of AND gate no. 2 while a write timing-pulse is still being applied, AND gate no. 2 conducts and produces a current flow through the other half of winding L1 to voltage source +V. The current flow through L1, which is now in the opposite direction from when a logic 1 pulse was applied, induces a current 180° out of phase with the L1 current in winding L2. This current flows through L3, which develops a flux in the write head and causes the next cell in the same track to become polarized (in an opposite direction to the preceding cell) and this cell represents a logic O.

The final bit of logic word is again a positive pulse representing a logic-l. The positive pulse applied to the set input of flipflop no. 1 allows AND gate no. 1 to produce a positive logic-l pulse output, and causes current to flow through half of L2 to +V. The current then induced in L2 flows **through** L3, developing flux in the write head and causes the third consecutive cell in the track to become polarized to a logic 1.

The drum continues to rotate with the stored logic bits until the cells containing the stored logic pass under the read head for that track. As the cell containing the first stored logic bit passes under the read head, the read head develops flux according to the polarization of the cell. The flux of the read head causes current to flow through L4 and winding L5 of transformer T2. The current through L5 induces a current in half of L6, which is  $180^{\circ}$  out of phase with the current through L5. The current through half of L6 flows from ground to the set input of flip-flop no. 2, developing a positive pulse at the l-output of the flip-flop. This positive pulse appears at one input of AND no. 3. If the pulse appears at the same time a positive read timing-pulse appears at the other AND gate input, AND gate no. 3 produces a positive (logic-1) voltage pulse at its output.

As the next cell containing a stored logic bit appears under the read head, the read head develops a current according to the polarization of the cell. The induced flux causes current to flow through L4 and in turn, through L5, also inducing current in half of L6 which is  $180^{\circ}$  out-of-phase with the current through L5. Current in half of L6 flows from ground to the clear input of flip-flop no. 2, developing a positive voltage at the O-output. This positive pulse appears at one input of AND gate no. 4, while the positive read timing-pulse appears at the other AND gate input, causing a positive pulse to be developed at the output of AND gate no. 4, which represents **a** logic o.

The next cell, which contains the last bit of stored logic, induces a current in the read head, and causes current to flow through L4 and L5. Current is induced in half of L6, flowing from ground to the set-input of flip-flop no. 2, which produces a positive pulse at the l-output of the flipflop. The positive pulse appears at AND gate no. 3 with the read timing-pulse, producing a positive pulse at the output of AND gate no. 3, which represents a logic-l. The logic word of 101 is thus written into the memory drum and read-out as 101.

### MAGNETIC DISC MEMORY

#### Application.

The magnetic disc memory is used in a computer to store a large quantity of binary information at medium access speeds.

#### Characteristics.

The magnetic disc memory resembles an automatic record player in appearance and operation.

Logic is stored on iron-oxide coated discs.

Logic is entered on and removed from the disc by writing and reading brush-type heads.

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This memory is capable of storing up to 5,000,000 bits.

#### Circuit Analysis.

General. The magnetic disc memory consists of a number of vertically stacked iron-oxide coated discs which continually rotate. Each disc contains a number of circular tracks for storing binary logic. These circular tracks are similar to the spiral tracks of phonograph records. The track which contains a specific binary word is the address of word. A word is written on to a disc by placing a brush write head, to which the logic information is applied, directly on the specific track of a specific disc. As the disc rotates below the write head, the lines of force of the track change in accordance with current applied to the write head. The lines of force, and thus the logic word, remain on the track of the disc until the word is to be read out. At that time, a read head is placed on the track containing the logic information stored on the disc.

**Circuit Operation.** A pictorial diagram of a magnetic disc memory is shown in the following illustration. The metal oxide coated discs are stacked vertically on a rotating cylindrical spindle. Movable brushtype heads are placed on the tracks of discs where logic information is to be stored or obtained.



Magnetic Disc Memory

If a logic word of 101 is to be stored on the first track of the upper disc in the memory, a series of three current pulses (one positive, one negative, and another positive) are applied to a write head which is placed on the first track of the upper discs. The current flowing through the write head develops lines of force around a certain amount of the track, depending on how fast the disc is moving and how long the current pulse is applied. The first positive current pulse (1) applied through the write head develops magnetic lines of force in the portion of the track below the write head at the time the pulse is applied. Magnetic lines of force are not developed on the section of the track below the write head when the pulse ends. The second current pulse (0) applied through the write head is negative. This pulse also develop lines of force on the section of the track below the write-head. In this case, however, the magnetic lines of force are oriented in the opposite direction to those of the first applied pulse. The third current pulse applied through the write head is a (1) which is again positive. This pulse causes lines of force to be developed on the section of the track below the write head in the same direction as those developed for the first applied pulse. The disc then continues to rotate with the lines of force of oriented sections remaining on the disc until they are read out.

If a binary number of 011 is to be read from the first track of the second disc a read head is positioned on this track. As the first stored bit approaches the read head, the lines of force representing the bit, develop a current in the read head. This current is positive, since the lines of force were oriented to represent a logic 1. As the disc continues to rotate, the lines of force col!apse, representing the end of the logic pulse. The next stored bit is again a logic 1; the section of the track appearing below the head then has lines of force oriented in the same direction as the first bit lines of force. These lines of force end as the disc continues to rotate past the read head and represent the end of the bit, the third stored bit is a logic O; the section of the track now appearing below the head has lines of force oriented in a direction opposite to those developed for the two logic 1 bits. This concludes the reading out of the logic word stored on the first track of the second disc. This word has to be recentered into the memory if it is to be used again, since it is erased from the memory when read out.

ORIGINAL

# MAGNETIC TAPE MEMORY

## Application.

The magnetic tape memory is used in computers as an inexpensive method of storing extremely large amounts of logic information, but at the coast of long access time.

## Characteristics.

The magnetic tape memory has a sequential and progressive type access mode.

The logic information is erasible, but it is not removed when the power is shut off, and it will not fade away.

The magnetic tape memory provides only slowspeed, external storage and long access time.

## **Circuit Analysis.**

General. The magnetic tape memory uses a unit similar to an audio tape recorder. The tape is passed across a set of read and write heads and is moved across the heads by means of rotating shafts and capstans. As the tape is moved across the heads it is wound around one reel and taken (unwound) from another reel. The magnetic tape memory, however, operates at higher speeds than audio tape recorders, and the memory tape is started and stopped much quicker. The tape used for a magnetic tape memory is, therefore, much stronger than audio tape, since it is exposed to the greater stress of rapid starting and stopping. The use of vacuum columns relieves some of the stress by providing several feet of slack as the tape enters and leaves the area of the heads. In this way, immediate movement of the tape occurs before the reels begin their rotation.

**Circuit Operation.** A pictorial drawing of a typical magnetic tape memory is shown in the following illustration. The magnetic tape is originally wound on the feed reel. The tape then extends around one tape guide, which keeps the tape taut and untangled. The tape is given slack but is prevented from tangling by its passage over a vacuum column. The tape passes over a rotating shaft and capstan, across the read and write heads, and around another rotating shaft. Depending upon which one of two tension rollers is pressed to the tape across from where a rotating shaft contacts the tape, the tape moves from feed reel to takeup reel or vice versa. The reel to which the tape is

directed rotates, so that the tape is reeled in. After the tape passes over the second rotating shaft, it passes across a second vacuum column, across a second tape guide and on to the take up reel.



#### Magnetic Tape Memory

If a logic word of 100 is to be written into the memory, a negative current pulse (representing logic O) is first applied to the write head. As a result of the applied current pulse, the iron oxide particles on the .portion of the tape appearing below the write head from magnetic lines of force, oriented toward one direction. The tension roller presses against the tape across from the point where the clockwise rotating shaft contacts the tape. As a result, the tape moves from the feed reel toward the take up reel. After the tape has moved a small distance, another negative current pulse (representing logic O) is applied to the write head, causing the iron oxide particles on the area of the tape now below the write head to become oriented in the same direction as the lines of force of the first bit. The tape continues to move from the - feed reel toward the take up reel. After the tape has again moved a short distance a positive pulse (representing a logic 1) is applied to the write head. The particles on the section of tape below the write head are now oriented along magnetic lines of force in an opposite direction to those of the first two pulses. The tape then continues to move from the feed reel to the take up reel until the tape is completely wound on the take up reel. When the logic word is to be read out, the tension roller pressed against the tape on the other side of the clockwise rotating shaft is released, and the other roller is pressed against the tape across from the point where the counterclockwise rotating shaft contacts the tape. The tape now rewinds on the feed reel from the take up reel. After most of the tape is wound on the feed reel, the roller accompanying the counterclockwise rotating shaft is released from the tape and the other tension roller is again pressed against the tape across from where the clockwise rotating shaft contacts the tape. The tape then

moves from the feed reel to the take up reel across the read and write heads. If the read head is activated as the magnetized sections of tape pass by the heads, currents are induced into the read head from the magnetized particles on the tape. The first section of magnetized tape represents a logic O. As this section of tape appears under the read head, a negative current pulse is induced into the read head. As the second section of magnetized tape, representing a logic O, appears under the read head, another negative current pulse is induced in the read head. The remaining section of magnetized tape represents a logic 1. In this case, a positive pulse is induced in the read head as that section of tape appears under the read head. The current pulses read out of the memory then represent the logic word of 100. It should be noted that the last bit of a logic word is written in last and is read out of the memory first, and the first bit of the logic word is written in first and read out of the memory last.

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