SD-73094-01

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4
SHEET INDEX SUPPORTING INFORMATION	A1	1	2	3	4
FS 1-DATA TEST SET NO. 911NA	B1	1	1	1	1
	B2	1	2	2	2
	B3	1	2	3	3
	B4	1	2	3	4
	B5	1	2	3	4
APP FIG. 1	C1	1	2	3	4
CIRCUIT NOTES EQUIPMENT NOTES	D1	1	2	3	4
INFORMATION NOTES	D2	1	2	2	2
	D3	1	2	2	2
	D4	1	1	1	1
	D5	1	2	2	2
	D6	1	2	2	2
	D7	1	2	2	2
	D8	1	2	2	2
	D9	1	2	2	2
	D10	1	1	1	1
	D11	1	2	2	2
	D12	1	2	2	2
	D13	1	2	2	2
	D14	1	2	2	2
	D15	1	2	3	4
	D16	1	2	3	4

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4
CPS 1- TEST SENTENCE GENERATOR	J1A	1	2	2	2
	J1B	1	2	3	4
	J1C	1	2	2	2
	J1D	1	2	2	2
	J1E	1	2	3	4
CPS 2 - DISTORTION MEASURING SET	J2A	1	2	2	2
	J2B	1	1	1	1
	J2C	1	2	2	2
	J2D	1	1	1	1
	J2E	1	2	2	2
	J2F	1	2	2	2
CPS 3 - CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS	J3A	1	2	3	3
	J3B	1	2	2	2
	J3C	1	2	3	3
CPS 4-PART OF POWER SUPPLY	J4		2	2	2

DWG ISSUE	CD ISSUE	DATE ISSUED	DRAWN	APPD
1	1	10-25-73	ESG AEZ	PE ALM RTK
2D	2D	9-13-76	BDH AEZ	PE ACM RTK
3A	2D APP 1A	1-17-77	ZEN JMF	PE ACM RTK
4B	2D APP 2B	1-17-77	ZEN JMF	PE JES RTK

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING, ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

SUPPORTING INFORMATION

CATEGORY	NO.
EQUIPMENT DESIGN REQUIREMENTS	807-462-152
MANUFACTURING TEST REQUIREMENT	X-78827
BSP-DESCRIPTION, OPERATION AND MAINTENANCE	103-813-110 103-813-510

ISSUE 4B

REPLACES SD-70937-01 & SD-70938-01.

SD-73094-01 1L02

DATA SYSTEMS STATION

DATA TEST SET NO. 911NA

AT&TCO STANDARD

(2) SD-73094-01-A1
38 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

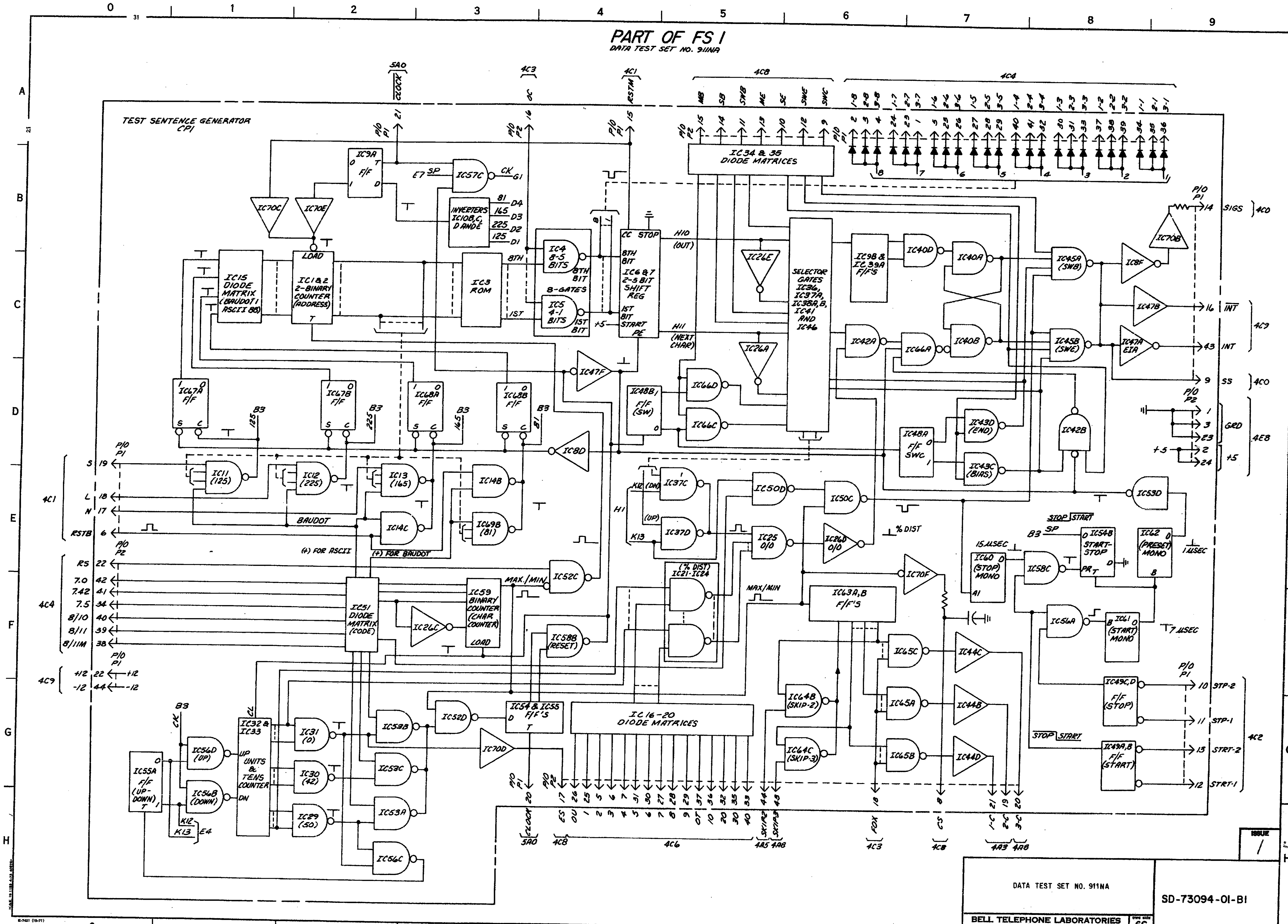
DWG SIZE 6S

PRINTED IN U.S.A.

SD-73094-01-A1

PART OF FS 1

DATA TEST SET NO. 911NA



DATA TEST SET NO. 911NA

SD-73094-01-B1

BELL TELEPHONE LABORATORIES INCORPORATED

ISSUE 1

PART OF FS 1

DATA TEST SET NO. 911NA

DISTORTION MEASURING SET CP2

IC29A IC29B IC30 & IC31 DECADE COUNTERS IC29 D,E,F IC24 A,D,E,F IC21 IC23 IC25 DIODE MATRIX IC2B IC35A IC35B DC H3 IC18 & 20 STORE IC26 & 27 COMP IC23B X C1 C6 IC28A X C4 IC40 & IC41 DIODE MATRICES IC37 B,E IC17 A-D IC176,F IC22A IC20 IC22 B,C,D IC53B 1 F/F IC53A F/F IC52C IC52B UP DN IC62B IC60 (0) IC58A IC59 (50) IC54 & IC55 UP & DN DECADE DN (COUNTER) (ELEMENT UP FRAMER) IC61 4-BIT BINARY COUNTER (@HARACTER FRAMER) LD RT T IC56 4-BIT BINARY COUNTER (AUTO SYNC) IC37C IC63B F/F IC6A, B,C,F IC7A, B,C,F IC5 DIODE MATRIX IC9 IC28B IC1B F/F IC15C IC1A F/F IC2C MS CO MSI C4 L IC10B IC10A IC10C,D F/F IC38B IC38A IC6 MONO A1 1.5 μSEC IC39B F/F IC37B IC39A F/F IC2D IC44 8 BIT SHIFT REG IC42A IC42C IC45B F/F IC47 8-BIT SHIFT REG IC46C IC46A IC43C IC48 5-BIT SHIFT REG SER IN IC49B IC51E IC50D IC51D IC3A IC2A MSI IC11B (SB) IC11A (MB) IC12A (SE) IC12B (ME) IC14 STORE IC15E IC15F IC15B IC15A

P/O P4 GRD +5 P/O P3 P/O P5 P/O P2 P/O P4 P/O P3 P/O P4

4E8 4F7 4E2 5A8 5A1 4E2 4E5 4E1 4E2 4E4 4E5

CNT PK PAR TOT AUTO (4F9) — PWR AD 0 3 5 7 100 15 CL1 RST CL2 (4E1, 4E2, 4E3, 4E5, 4E6, 4F5)

4E3 4F2 4E0

DATA TEST SET NO. 911NA

SD-73094-01-B2

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U. S. A.

ISSUE 2D

SD-73094-01-B2

PART OF FS!

DATA TEST SET NO. 911NA

CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS CP3

P10 P5

5A3 EXT 7
NC 13
NC 14
5A2 11B 6
5A3 13B 4

IC5E IC6B
IC5D IC6C
IC5C IC6D
IC5A IC6F

IC7B F/F 2.4 MHZ
IC7A F/F
Y1 XTAL OSC 9.6 MHZ
IC8C
IC12 DECADE COUNTER (÷10)
IC11B F/F 960KHZ
IC11A F/F
IC17,18,19 DECADE COUNTERS
IC13-16 DIODE MATRICES

P/O P5
11 1B
3 2B
12 3B
2 4B
10 5B
1 6B
9 7B
8 8B
19 9B
20 10B
5A2

NC 18 17B 5A3
NC 21 12B 5A2
NC 17 18B 5A3
NC 22 NC
NC 15 14B
NC 16 15B 5A3
NC 5 16B
23 EXT CLK 5A4
24 CLOCK
25 $\overline{\text{CLOCK}}$ 5A1

480KHZ

Y2 XTAL OSC 180.000KHz
Y3 XTAL OSC 105.000KHz
IC4B
IC4C
IC9D
IC8A
IC10
IC9B
IC9C
IC5F

480KHZ
960KHZ

P8

5A9 A2 5 IN FILTER
B2 4 OUT

5A7 R 14
5A9 IN2 3
IN1 13
5A7 I 1
H 15
G 2
VOLTAGE INPUT CIRCUIT

5A6 12 NC
5A3 E1 16
B1 23
A1 24
5A6 C 8
D 7
E 20
F 21
5A8 J 9
K 19
CURRENT INPUT CIRCUIT

P6
-12 5 -12 4B9
+12 4 +12
10 INT1 4C9

VOLTAGE OUTPUT
7 HUB
NC 3
CURRENT OUTPUT
8 CM
9 CB
2 CA
NC 1
5A4

P7
+5 1 2 11 12 +5
+12 4 +12
-12 3 -12
5H2
GRD 8 9 10 18 19 20

ISSUE 3A

DATA TEST SET NO. 911NA

SD-73094-01-B3

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-B3

TC-7621 (10-71)

PART OF FSI

DATA TEST SET NO. 911NA

S1 1-1 SW
S2 1-2 SW
S3 1-3 SW
S4 1-4 SW
S5 1-5 SW
S6 1-6 SW
S7 1-7 SW
S8 1-8 SW
S9 2-1 SW
S10 2-2 SW
S11 2-3 SW
S12 2-4 SW
S13 2-5 SW
S14 2-6 SW
S15 2-7 SW
S16 2-8 SW
S17 ON-SKIP SW
S18 3-1 SW
S19 3-2 SW
S20 3-3
S21 3-4 SW
S22 3-5
S23 3-6 SW
S24 3-7 SW
S25 3-8 SW
S26 ON-SKIP SW
P/O S36 TYPE DIST SW
P/O CA1 CORD
P/O CA2 CORD
P/O CA3 CORD
P/O CA4 CORD
P/O CA6 CORD
P/O J1
P/O J2
P/O J3
P/O J4
P/O J6
CR1 SIGS
S27 SPACE SW
S28 LINE LENGTH SW
S29 RESET SW
S30 SW STOP
STEP (NL) NO
START (L) NO
SECT A
SECT B
S31 FOX CHAR SW
S32 REPEAT SW
P/O S33 CODE SW
SECT 1
SECT 2
S34 DIST 10% SW
S35 DIST 1% SW
P/O S36 TYPE DIST SW
S41 DISCR % SW
S42 NORM-REV SW
R1 619
T 588
J3 VOLT OUT EIA
C9 1800 PF
S37 ASYNC-SYNC SW
CR2 MB
CR3 SB
CR4 ME
CR5 SE
CR7 SIGS
CR8 POWER
S39 RESET SW
CR6 PARITY ERROR
S38 PARITY SW
EVEN
ODD
S40 PARITY SW
CR9 1-1
CR10 1-2
CR11 1-3
CR12 1-4
CR13 1-5
CR14 1-6
CR15 1-7
CR16 1-8
CR17 2-1
CR18 2-2
CR19 2-3
CR20 2-4
CR21 2-5
CR22 2-6
CR23 2-7
CR24 2-8
S43 CHAR DISPLAY SW
UNITS
TENS
DISPLAY
S44 DIST PKS SW
S45 DISPLAY SW
NO.20 AWG STRANDED
1A7
1B9
1C9
1D9
1E0
1F0
1G0
1G9
1H4
1H5
1H6
1H7
1H8
1A3
1A4
1A5
1H7
2A2
2A3
2A6
2A7
2A8
2B9
2C9
2D0
2D9
2E0
2E9
2F0
2G0
2G9

ISSUE
4B

DATA TEST SET NO. 911NA

SD-73094-01-B4

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-B4

PART OF FS1
DATA TEST SET NO. 911NA

P/O CA1 CORD
P/O CA3 CORD
P/O CA5 CORD
P/O CA9 CORD
P/O CA7 CORD
P/O CA8 CORD
P/O CA6 CORD
P/O CAG CORD
P/O CAB CORD
P/O SECT 1
P/O SECT 2
P/O 533 CODE SW
547 BAUDS SW
J5 EXT CLK
J6 VOLT OUT LV HUB
J7 T+ LP DRIVER
J8 T- LP DRIVER
CR25 OVER LOAD CURRENT INPUT
J9 T+ CURRENT INPUT
J10 T- CURRENT INPUT
+12
548 INPUT SW
546 FILTER SW
J4 VOLT. INPUT

POWER SUPPLY

CP 4
P/O POWER SUPPLY

IC2 VOLTAGE REGULATOR -12
CASE BOLT
IC1 VOLTAGE REGULATOR +12
IC 3 VOLTAGE REGULATOR +5
CR1
CR26
Q1
T1
F1
DS1
R2 68.1K Ω
R5
C1 800
C2 5600
C3 1000
C4 1000
C5 100
C6 100
C7 .1
C8 .1
TP1
TP2
TP3
TP4
TSB 1
TSB 2
TSB 4
TSA 4
ON OFF 549 POWER SW
TO 117V AC
PWR CORD
J11 GRD
CA7 CORD
J7
3GO

NO. 18 AWG STRANDED
NO. 16 AWG STRANDED
NO. 16 AWG
NO. 20 AWG STRANDED
NO. 18 AWG

ISSUE 4B

DATA TEST SET NO. 911NA

SD-73094-01-B5

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-B5

APP FIG. 1

CIRCUIT PACK

EQPT LOC			
DESIG	CP1	CP2	CP3
CODE	ED-73551	ED-73552	ED-73553
OPTION			
ELEM IDENT	TERM.	TERM.	TERM.
TERM.FS LOC			

CORD

DESIG	LOC	CODE
CA1	4B0,4C0,4C9,5A0	ED-73550, GROUP 1 (E/W CONN J1)
CA2	4B9,4C9,4E9	ED-73550, GROUP 1 (E/W CONN J2)
CA3	4E0,4E5,4F0,5A0,5A8	ED-73550, GROUP 1 (E/W CONN J3)
CA4	4E3,4E7,4F9	ED-73550, GROUP 1 (E/W CONN J4)
CA5	5A1,5A4	ED-73550, GROUP 1 (E/W CONN J5)
CA6	4B9,4C9,5A5	ED-73550, GROUP 1 (E/W CONN J6)
CA7	5H4	ED-73550, GROUP 2 (E/W CONN J7)
CA8	5A3,5A8,5A9	ED-73550, GROUP 1 (E/W CONN J8)
PWR CORD	5E7	~~DELDEN,17239~~, KS-20340,L1

SEE CONNECTOR

CORD (CONT)
PATCHING

DESIG	LOC	CODE
—	—	2P1D
—	—	2P1D
—	—	W1B8
—	—	W1B8
—	—	P1N
—	—	P1N
—	—	2W44B
—	—	2W44B

CONNECTOR

DESIG	J1	J2	J3	J4	J5	J6	J7	J8
CODE	AMP INC., 1-86148-7	AMP INC., 1-86148-7	AMP INC., 1-86148-7	AMP INC., 1-86148-7	AMP INC., 86148-5	AMP INC., 1-86148-3	AMP INC., 86148-1	AMP INC., 86148-3
OPTION								
TERM.								
1	4C7	4E8	4E2	4E8	5A2	5A4	5H3	5A7
2	4C2	4E8	4E2	4E7	5A2	5A5	5H3	5A7
3	4C5	4E8	4E0	4E8	5A1	5A5	5H1	5A9
4	4C8	KEYED	4E1	SPARE	5A3	4C9	5H0	5A9
5	4C1	4C6	KEYED	4F6	SPARE	4C9	UNEQUIPPED	5A9
6	4C1	4C6	SPARE	4F6	5A2	SPARE	UNEQUIPPED	SPARE
7	KEYED	4C6	SPARE	4F7	5A3	5A4	UNEQUIPPED	5A6
8	SPARE	4C9	4E3	4F9	5A2	5A5	5H2	5A6
9	4C0	4C8	4E1	4F9	5A2	5A5	5H2	5A8
10	4C2	4C8	4E1	4F9	5A2	4C9	5H2	UNEQUIPPED
11	4C2	4C8	4E6	4F9	5A1	KEYED	5H3	UNEQUIPPED
12	4C3	4C8	4F3	4E4	5A2	SPARE	5H3	5A6
13	4C3	4C8	4F3	4E4	UNEQUIPPED		KEYED	5A9
14	4C0	4C7	4F4	4E5	UNEQUIPPED		UNEQUIPPED	5A7
15	4C2	4C7	4F2	4E5	SPARE		UNEQUIPPED	5A7
16	4C9	4C3	4F3	UNEQUIPPED	SPARE		UNEQUIPPED	5A3
17	4C0	4C8	4E5	UNEQUIPPED	5A3		UNEQUIPPED	SPARE
18	4C1	4C3	4F0	UNEQUIPPED	5A3		5H2	KEYED
19	4C1	4A5	4F0	4F7	5A2		5H2	5A8
20	5A0	4A8	4F0	4F8	5A2		5H2	5A7
21	5A0	4A2	4F1	4F8	5A2			5A7
22	4C9	4C3	4F2	4F8	UNEQUIPPED			UNEQUIPPED
23	4C4	4E9	4E0	4E8	5A4			5A5
24	4C2	4E8	4E0	4E8	5A1			5A6
25	4C4	4C6	4F5	4E4	5A1			
26	4C7	4C6	4E2	4E4	KEYED			
27	4C1	4C7	4E2	4F9	UNEQUIPPED			
28	4C4	4C7	5A1	4E3	UNEQUIPPED			
29	4C7	4C7	5A1	4F7				
30	4C0	4C7	5A8	4F5				
31	4C3	4C6	4F5	4F6				
32	4C6	4C5	4F4	4F6				
33	4C6	4C5	4F4	4F5				
34	4C0	4C4	4E1	SPARE				
35	4C3	4C5	4E2	SPARE				
36	4C6	4C5	4E6	SPARE				
37	4C0	4C5	4E7	SPARE				
38	4C3	4C5	4E7	UNEQUIPPED				
39	4C6	4C4	4E7	KEYED				
40	4C1	4C4	4E6	UNEQUIPPED				
41	4C3	4C4	4E6	4F8				
42	SPARE	4C4	4F1	4F8				
43	4C9	4A8	4F1	4F8				
44	4C9	4A5	4F2	4F8				

CAPACITOR

DESIG	LOC	CODE
C9	4D9	KS-20977 ,L4, 1800PF

DIODE

DESIG	LOC	CODE
CR1	4D0	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
[3] CR2-CR4	4E0	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR5	4E1	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR6	4E3	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR7	4E2	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR8	4E2	(Z) HEWLETT PACKARD,5082,4882,
[3] CR9-CR11	4F0	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
[3] CR12-CR14	4F1	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
[3] CR15-CR17	4F2	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
[3] CR18-CR20	4F3	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
[3] CR21-CR23	4F4	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR24	4F5	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A
CR25	5C4	(Z)(Y) HEWLETT PACKARD,5082-4882, 541A

DISPLAY

DESIG	LOC	CODE
DISPLAY	4G6	DIALIGHT COPR, 739-0200

JACK

DESIG	LOC	CODE
J1	4D8	KS-14523,L7
J2	4D9	KS-14523,L7
J3	4D9	KS-14523,L2
J4	5B9	KS-14523,L2
J5	5B4	KS-14523,L7
J6	5B4	KS-14523,L2
J7	5C4	KS-21546,L1
J8	5C4	KS-21546,L1
J9	5B5	KS-21546,L1
J10	5B5	KS-21546,L1
J11	5G6	KS-14523,L3

LAMP

DESIG	LOC	CODE
(Y) DS1	5D6	MARCO OAK,22-353B0-6P19-211 E/W AIB NEON LAMP

POWER SUPPLY PANEL ASSEMBLY

DESIG	LOC	CODE
POWER SUPPLY	5D3	ED-73554
E/W		

CAPACITOR

DESIG	LOC	CODE
C1	5F3	KS-19658,L28, 800
C2	5F3	KS-20446,L39, 5600
C3	5E3	KS-19658,L9, 1000
C4	5D3	KS-19658,L9, 1000
C5	5G0	KS-19658,L43, 100
C6	5G1	KS-19658,L43, 100
C7	5D4	SPRAGUE, 196P10496S4, .1
C8	5F5	SPRAGUE, 196P10496S4, .1

CIRCUIT PACK

DESIG	LOC	CODE
CP4	5D1	ED-73579

DIODE

DESIG	LOC	CODE
CR26	5E4	MOTOROLA, MDA 952-1

FUSE

DESIG	LOC	CODE
F1	5D5	BUSMAN, MDL 1/2 AMP

POWER SUPPLY PANEL ASSEMBLY (CONT)

POWER SUPPLY (CONT)
E/W

TERMINAL

DESIG	LOC	CODE
E2	5G5	CAMBION CORP,160-2380-01-05-00
[4] E3-E6	5E3	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
E7	5G0	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
[3] E8-E10	5G1	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
[4] E11-E14	5F3	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
E15	5D4	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
E16	5F5	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
E17	5E4	CAMBION CORP, ~~571-4115-1-0519~~,151I-01-10
E18	5F4	CAMBION CORP,160-2380-01-05-00
E20	5F5	CAMBION CORP,1511-01-10
(X) TP1	5F5	CAMBION CORP,511-4115-1-0519
(X) TP2	5E3	CAMBION CORP,511-4115-1-0519
(X) TP3,TP4	5G1	CAMBION CORP,511-4115-1-0519

TRANSFORMER

DESIG	LOC	CODE
T1	5E4	SIGNAL TRANSFORMER CO,7482

TRANSITOR

DESIG	LOC	CODE
Q1	5B3	MOTOROLA,2N3055

RESISTOR

DESIG	LOC	CODE
R1	4D9	KS-20289,L6C, 619
(Y) R2	5D6	KS-20289,L6C,68.1KΩ

SWITCH

DESIG	LOC	CODE
S1	4B0	C&K COMPONENTS, 7101SYPZB
S2	4B0	C&K COMPONENTS, 7101SYPZB
S3	4D0	C&K COMPONENTS, 7101SYPZB
S4	4B1	C&K COMPONENTS, 7101SYPZB
S5	4B1	C&K COMPONENTS, 7101SYPZB
S6	4B1	C&K COMPONENTS, 7101SYPZB
S7	4B2	C&K COMPONENTS, 7101SYPZB
S8	4B2	C&K COMPONENTS, 7101SYPZB
S9	4B3	C&K COMPONENTS, 7101SYPZB
S10	4B3	C&K COMPONENTS, 7101SYPZB
S11	4B3	C&K COMPONENTS, 7101SYPZB
S12	4B4	C&K COMPONENTS, 7101SYPZB
S13	4B4	C&K COMPONENTS, 7101SYPZB
S14	4B4	C&K COMPONENTS, 7101SYPZB
S15	4B5	C&K COMPONENTS, 7101SYPZB
S16	4B5	C&K COMPONENTS, 7101SYPZB
S17	4B5	C&K COMPONENTS, 7101SYPZB
S18	4B6	C&K COMPONENTS, 7101SYPZB
S19	4B6	C&K COMPONENTS, 7101SYPZB
S20	4B6	C&K COMPONENTS, 7101SYPZB
S21	4B7	C&K COMPONENTS, 7101SYPZB
S22	4B7	C&K COMPONENTS, 7101SYPZB
S23	4B7	C&K COMPONENTS, 7101SYPZB
S24	4B8	C&K COMPONENTS, 7101SYPZB
S25	4B8	C&K COMPONENTS, 7101SYPZB
S26	4B8	C&K COMPONENTS, 7101SYPZB
S27	4D0	GRAYHILL, 46-101B
S28	4D1	OAK, 399-999-118D, SEE NOTE 1

SWITCH (CONT)

DESIG	LOC	CODE
S29	4D2	GRAYHILL, 46-101R
S30	4C2	MICROSWITCH, 13AT403-T2
S31	4D3	C&K COMPONENTS, 7101SYPZB
S32	4D4	C&K COMPONENTS, 7101SYPZB
S33	4D5,4D6,5B1	OAK, 399-999-120D
S34	4D6	OAK, 399-999-119D
S35	4D7	OAK, 399-999-124D
S36	4A9,4D8	OAK, 399-999-122D
S37	4D1	C&K COMPONENTS, 7301SYPZB
S38	4E4	C&K COMPONENTS, 7101SYPZB
S39	4E3	GRAYHILL, 46-101R
S40	4E5	C&K COMPONENTS, 7201SYPZB
S41	4D7	OAK, 399-999-121D, SEE NOTE 1
S42	4D9	C&K COMPONENTS, 7101SYPZB
S43	4G3	C&K COMPONENTS, 7203SYPZB
S44	4G8	OAK, 399-999-123D
S45	4G9	OAK, 399-999-119D
S46	5B9	C&K COMPONENTS, 7201SYPZB
S47	5B3	GRAYHILL, 53M15-01-1-24NC
S48	5B9	OAK, 399-999-117D, SEE NOTE 1
S49	5D7	CUTLER HAMMER, SF1SCY191

SEE NOTE 1

TERMINAL

DESIG	LOC	CODE
E1	5H6	SHAKEPROOF, 2104-06-00
E19	5H6	SHAKEPROOF, 2104-06-00

TERMINAL STRIP

DESIG	LOC	CODE
TS A	4F5,5F6, 5G6	CINCH MFR CORP,326-20-04-004 BLK
TS B	4D6,5F6, 5G6	CINCH MFR CORP,326-20-04-004 BLK

NOTES:

1. OAK SWITCHES CODED 399-999-1XXD MAY BE OBTAINED FROM DRW ELECTRONICS, FARMINGDALE, L.I., N.Y.

ISSUE 4B

DATA TEST SET NO. 911NA

SD-73094-01-CI

BELL TELEPHONE LABORATORIES INCORPORATED

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SD-73094-01-CI

CIRCUIT NOTES:

101.

DESIG	FUSE AMP	POTENTIAL	ONE PER
F1	0.5	115V AC	APP FIG.1

102.

FEATURE OR OPTION	PROVIDE		
	APP FIG	APP OR WRG	QUANTITY
DATA TEST SET SEE NOTE 105	1		1 PER CKT

103.

RECORD OF APP. FIGURES, WIRING AND APPARATUS CHANGES							
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT			
				STD	A&M	MD	
4B	Z,Y	Z		Y		Z	
4B	X	NONE		X			
4B	W,V	W		V		W	

CIRCUIT NOTES: (CONT)

104. FOR TESTING ACCESS TO CP1, CP2 & CP3 WHEN THEY ARE REMOVED FROM CHASSIS, TEST CABLE ASSEMBLIES (ED-73550,G10) ARE REQUIRED.

105.

106. WHEN AN EXTERNAL CLOCK SOURCE IS USED ITS WAVEFORM MUST BE A SQUARE WAVE. THE AMPLITUDE OF THIS WAVEFORM MUST BE +5±0.5 VOLTS TO GROUND. THE DUTY CYCLE OF THE WAVEFORM SHOULD BE SYMETRICAL TO 50±10 PERCENT. THE OSCILLATOR FREQUENCY MUST BE 100 TIMES THE DESIRED BAUD RATE AND MUST NOT EXCEED 960KHZ.

107. THE 911P (SD-73112-01) EIA TEST ADAPTER UNIT IS AVAILABLE AS AN AID IN TESTING DATA SET MODEMS AND ASSOCIATED EQUIPMENT WHICH USE STANDARD EIA STANDARD RS-232 TYPE INTERFACES. PIN JACKS AND SWITCHES ARE PROVIDED TO ENABLE A TEST PERSON TO USE EITHER A 911A OR 911NA DATA TEST SET TO MONITOR, MEASURE OR TO CHECK VARIOUS FUNCTIONS OF THE CIRCUITRY, DATA SET AND TERMINAL EQUIPMENT. THE 911P FITS IN THE COVER OF EITHER 911A OR 911NA DATA TEST SET.

EQUIPMENT NOTES:

201. CONTACTS CLOSE IN DIRECTION OPPOSITE TO LEVER OPERATION-FOR SWITCHES S1-S26, S31, S32, S37, S38, S40, S43, S46, S49.

202. POLARITY INFORMATION FOR CR1-CR25 (Ⓩ ONLY) IS AS FOLLOWS:

203. GROUND AND +5 LEADS ON FRONT PANEL ASSEMBLY SHALL BE NO. 20AWG.

204. UNLESS OTHERWISE SPECIFIED, ALL WIRING ON THE FRONT PANEL ASSEMBLY SHALL BE NO. 24 AWG.

205. UNLESS OTHERWISE SPECIFIED, ALL WIRING ON THE POWER SUPPLY PANEL ASSEMBLY (ED-73554) SHALL BE NO. 18 AWG. WIRING TO TEST POINTS Ⓧ TP1 THRU Ⓧ TP4 SHALL BE NO.24 AWG OR HEAVIER WIRE.

206. THE FOLLOWING TERMINALS SHALL BE INSULATED TO PREVENT POSSIBLE HAZARD FROM 120VAC LINE VOLTAGE:

A. TRANSFORMER T1, TERMINALS 1 & 2;
B. FUSE F1, BOTH TERMINALS;
C. CAPACITORS C7 & C8;
D. TERMINAL STRIP TSB, TERMINALS 1 & 2;
E. SWITCH S49;
F. RESISTOR R2, LAMP DS1.

207. ALL SPARE LEADS ON CONNECTORS J1-J8, AS SHOWN IN APP FIG. 1, SHALL BE LEFT AT ORIGINAL LENGTH AND TAPED AND STORED.

SD-73094-01-DI

ISSUE 4B

DATA TEST SET NO. 911NA

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

SD-73094-01-DI

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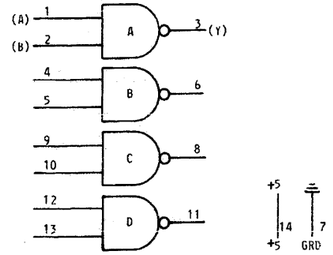
INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR -(MINUS) ARE IN VOLTS.

302. INTEGRATED CIRCUIT DEVICE CIRCUIT ELEMENTS:

(A) QUADRUPLE 2-INPUT GATES, KS-20968 L1, SN74L00 AND KS-20968 L9, SN74L03, SEE NOTE 1.



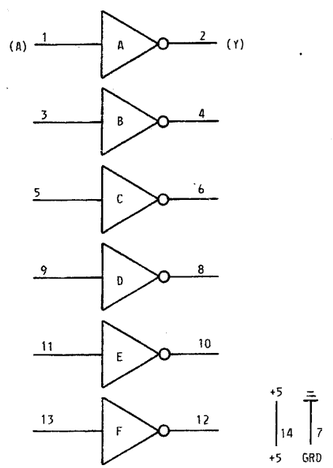
CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS FOUR 2-INPUT POSITIVE NAND GATES, EACH PERFORMING THE LOGIC FUNCTION:

$Y = \overline{AB}$

A LOGICAL 0 OUTPUT IS OBTAINED ONLY IF INPUTS A AND B ARE LOGICAL 1. ALL OTHER INPUT COMBINATIONS CAUSE THE OUTPUT TO BE LOGICAL 1.

(B) HEX INVERTERS, 6 PER DEVICE, KS-20968 L2, SN74L04 AND KS-20967 L6, SN7405, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS SIX INVERTERS, EACH PERFORMING THE LOGICAL FUNCTION:

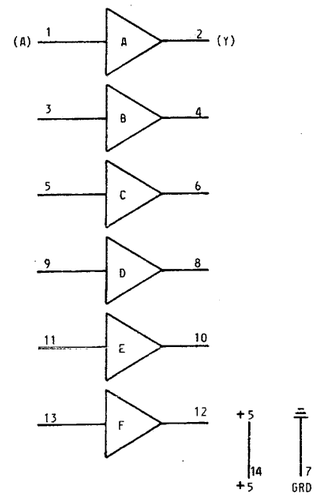
$Y = \overline{A}$

A LOGICAL 0 INPUT CAUSES A LOGICAL 1 OUTPUT AND A LOGICAL 1 INPUT CAUSES A LOGICAL 0 OUTPUT.

INFORMATION NOTES (CONT)

302. (CONT)

(C) HEX BUFFER DRIVER, 6 PER DEVICE, KS-20967 L7, SN7407 AND KS-20967 L8, SN7417, SEE NOTE 1.

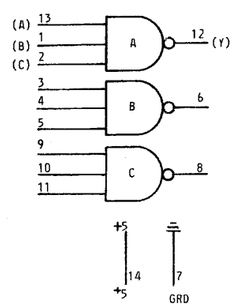


CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS SIX BUFFER DRIVERS WHICH HAVE OPEN COLLECTOR, HIGH VOLTAGE OUTPUTS. EACH PERFORMING THE LOGICAL FUNCTION:

$Y = A$

(D) TRIPLE 3-INPUT NAND GATES, KS-20968 L3, SN74L10, KS-20967,L4, SN7410, AND KS-20967,L5, SN7412, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS THREE 3-INPUT POSITIVE NAND GATES, EACH PERFORMING THE LOGICAL FUNCTION:

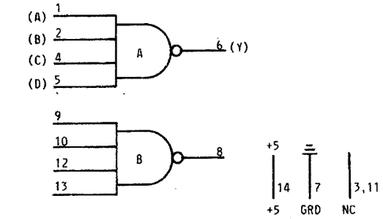
$Y = \overline{ABC}$

A LOGICAL 0 OUTPUT IS OBTAINED ONLY IF INPUTS A AND B AND C ARE LOGICAL 1. ALL OTHER INPUT COMBINATIONS CAUSE THE OUTPUT TO BE A LOGICAL 1.

INFORMATION NOTES (CONT)

302. (CONT)

(E) DUAL 4-INPUT POSITIVE NAND GATES, SN74H22, SEE NOTE 1.



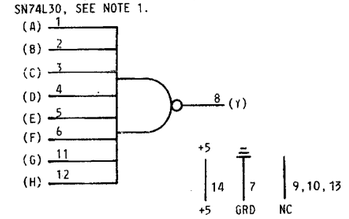
CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS TWO 4-INPUT POSITIVE NAND GATES, EACH PERFORMING THE LOGICAL FUNCTION:

$Y = \overline{ABCD}$

A LOGICAL 0 OUTPUT IS OBTAINED ONLY IF INPUTS A AND B AND C AND D ARE LOGICAL 1. ALL OTHER INPUT COMBINATIONS CAUSE THE OUTPUT TO BE A LOGICAL 1.

(F) 8-INPUT POSITIVE NAND GATE, KS-20968 L8, SN74L30, SEE NOTE 1.



CIRCUIT DESCRIPTION

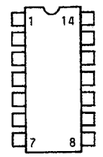
THIS DEVICE CONTAINS ONE 8-INPUT POSITIVE NAND GATE, PERFORMING THE LOGICAL FUNCTION:

$Y = \overline{ABCDEFGH}$

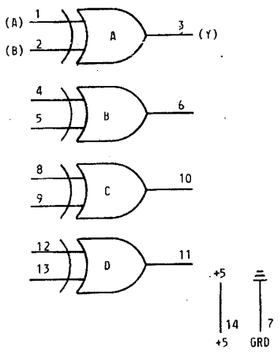
A LOGICAL 0 OUTPUT IS OBTAINED ONLY IF INPUTS A AND B AND C AND D AND E AND F AND G AND H ARE LOGICAL 1. ALL OTHER INPUT COMBINATIONS CAUSE THE OUTPUT TO BE A LOGICAL 1.

NOTES:

1. PIN NUMBERING, TOP VIEW



(G) QUAD 2-INPUT EXCLUSIVE OR GATES, KS-20968 L6, SN74L86, 4 PER DEVICE, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS FOUR 2-INPUT EXCLUSIVE - OR GATES, EACH PERFORMING THE LOGICAL FUNCTION:

$Y = A \oplus B = \overline{A}B + A\overline{B}$

WHEN THE INPUT STATES ARE COMPLIMENTARY, THE OUTPUT GOES TO A LOGICAL 1. IF BOTH INPUTS ARE THE SAME, THE OUTPUT GOES TO A LOGICAL 0.

ISSUE 20

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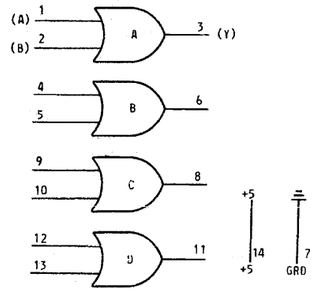
INFORMATION NOTES: (CONT)

302. (CONT)

(H) QUAD 2-INPUT OR GATES, KS-20967 L11, SN7432,, 4 PER DEVICE, SEE NOTE 1.



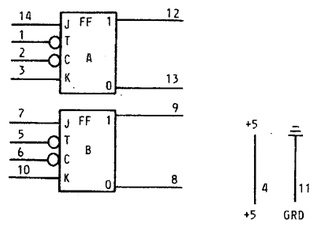
CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS FOUR 2-INPUT OR GATES, EACH PERFORMING THE LOGICAL FUNCTION:

$Y = A+B$

A LOGICAL 0 OUTPUT IS OBTAINED ONLY IF EITHER OR BOTH INPUTS ARE LOGICAL 0. IF BOTH INPUTS ARE LOGICAL 1, THE OUTPUT GOES TO LOGICAL 1.

(I) DUAL CLOCKED J-K MASTER SLAVE FLIP-FLOPS, KS-20970 L5, SN74L73, 2 PER DEVICE, SEE NOTE 1.



CIRCUIT DESCRIPTION

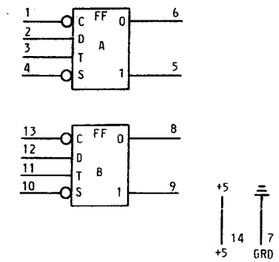
THIS DEVICE CONTAINS TWO CLOCKED J-K MASTER SLAVE FLIP-FLOPS. EACH OF THE FLIP-FLOPS HAS DIRECT CLEAR INPUT WHICH IS INDEPENDENT OF THE CLOCK.A LOW INPUT TO C CLEARS THE 1 OUTPUT TO A LOGICAL 0. INPUT INFORMATION IS TRANSFERRED TO THE 1 OUTPUT ON THE NEGATIVE EDGE OF THE CLOCK INPUT T, ACCORDING TO THE TRUTH TABLE.

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

INFORMATION NOTES: (CONT)

302. (CONT)

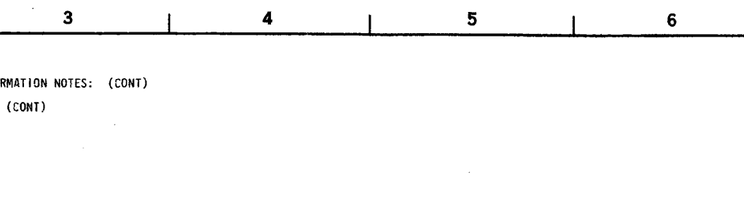
(J) DUAL, D-TYPE, POSITIVE EDGE TRIGGERED FLIP-FLOPS, KS-20970 L1, SN74L74, 2 PER DEVICE, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS TWO, D-TYPE, POSITIVE EDGE TRIGGERED FLIP-FLOPS, EACH WITH DIRECT SET AND CLEAR INPUTS WHICH ARE INDEPENDENT OF THE CLOCK. A LOW INPUT TO S SETS THE 1 OUTPUT TO A LOGICAL 1. A LOW INPUT TO C CLEARS THE 1 OUTPUT TO A LOGICAL 0. INPUT INFORMATION ON D IS TRANSFERRED TO THE 1 OUTPUT ON THE POSITIVE EDGE OF THE CLOCK INPUT T.

(K) 4-BIT BISTABLE LATCH, KS-20969 L23, SN7475, 1 PER DEVICE, SEE NOTE 2.

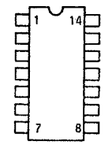


CIRCUIT DESCRIPTION

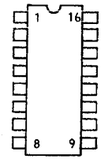
THIS DEVICE CONSISTS OF FOUR D-TYPE FLIP-FLOPS. THIS LATCH IS USED AS TEMPORARY STORAGE FOR BINARY INFORMATION. INFORMATION PRESENT AT A DATA (D) INPUT IS TRANSFERRED TO THE (Q) OUTPUT WHEN THE CLOCK IS HIGH, AND THE (Q) OUTPUT WILL FOLLOW THE DATA INPUT AS LONG AS THE CLOCK REMAINS HIGH. WHEN THE CLOCK GOES LOW, THE INFORMATION (THAT WAS PRESENT AT THE DATA INPUT AT THE TIME THE TRANSITION OCCURRED) IS RETAINED AT THE (Q) OUTPUT UNTIL THE CLOCK IS PERMITTED TO GO HIGH.

NOTES:

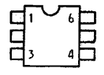
1. PIN NUMBERING, TOP VIEW.



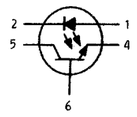
2. PIN NUMBERING, TOP VIEW.



3. PIN NUMBERING, TOP VIEW.



(L) OPTICALLY COUPLED ISOLATOR, TIL111, 1 PER DEVICE, SEE NOTE 3.



CIRCUIT DESCRIPTION.

THIS DEVICE CONTAINS ONE OPTICALLY COUPLED ISOLATOR WHICH PROVIDES AN OPTICAL COUPLING BETWEEN INPUT AND OUTPUT WHILE MAINTAINING A HIGH DEGREE OF ELECTRICAL ISOLATION. IT HAS APPLICATIONS FOR USE AS A SOLID-STATE RELAY FOR VOLTAGE ISOLATION, AS AN INTERFACE DEVICE BETWEEN SYSTEMS, AS WELL AS LINE DRIVER/RECEIVER COMBINATIONS.

ISSUE 2D

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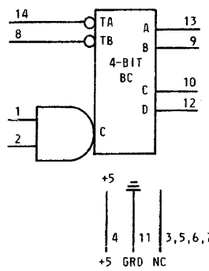
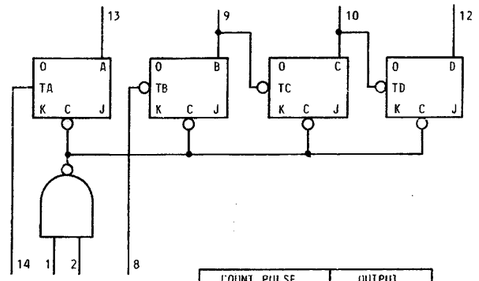
INFORMATION NOTES: (CONT)

302. (CONT)

(M) 4-BIT BINARY COUNTER, KS-20970 L2, SN74L93, 1 PER DEVICE, SEE NOTE 1.





COUNT PULSE TO TA	OUTPUT			
	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

OUTPUT A CONNECTED TO INPUT TB

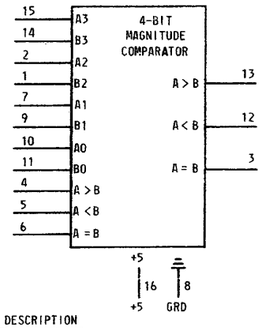
CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS ONE 4-BIT BINARY COUNTER, CONSISTING OF FOUR MASTER SLAVE FLIP-FLOPS WHICH ARE INTERNALLY INTERCONNECTED TO PROVIDE A DIVIDE-BY-TWO AND A DIVIDE-BY-EIGHT COUNTER. WHEN USED AS A 4-BIT RIPPLE-THROUGH COUNTER, OUTPUT A MUST BE EXTERNALLY CONNECTED TO INPUT TB. A GATED DIRECT RESET LINE IS PROVIDED WHICH INHIBITS THE COUNT INPUTS AND SIMULTANEOUSLY RETURNS THE FOUR OUTPUTS TO A LOGICAL 0. EITHER OR BOTH RESET INPUTS MUST BE AT A LOGICAL 0 TO COUNT. THE OUTPUTS PROVIDE A BCD REPRESENTATION OF THE INPUT COUNTS.

INFORMATION NOTES: (CONT)

302. (CONT)

(N) 4-BIT MAGNITUDE COMPARATOR, KS-20970 L6, SN74L85, 1 PER DEVICE, SEE NOTE 2.



CIRCUIT DESCRIPTION

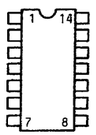
THESE 4-BIT MAGNITUDE COMPARATORS COMPARE TWO 4-BIT WORDS AND DETERMINE THEIR RELATIVE MAGNITUDE WITH THE RESULT BEING INDICATED BY A HIGH-LEVEL VOLTAGE AT THE A > B, A < B, OR A = B OUTPUT. WORDS OF GREATER LENGTH MAY BE COMPARED BY CONNECTING COMPARATORS IN CASCADE. THE A > B, A < B, AND A = B OUTPUTS OF A STAGE HANDLING LESS SIGNIFICANT BITS ARE CONNECTED TO THE CORRESPONDING A > B, A < B, AND A = B INPUTS OF THE NEXT STAGE HANDLING MORE SIGNIFICANT BITS. THE STAGE HANDLING THE LEAST SIGNIFICANT BITS MUST HAVE A LOW-LEVEL VOLTAGE APPLIED TO THE A > B AND A < B INPUTS AND A HIGH-LEVEL VOLTAGE APPLIED TO THE A = B INPUT.

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	0	1	0
A3 = B3	A2 > B2	X	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1

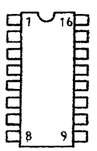
X - IRRELEVANT, 1 - HIGH LEVEL, 0 - LOW LEVEL

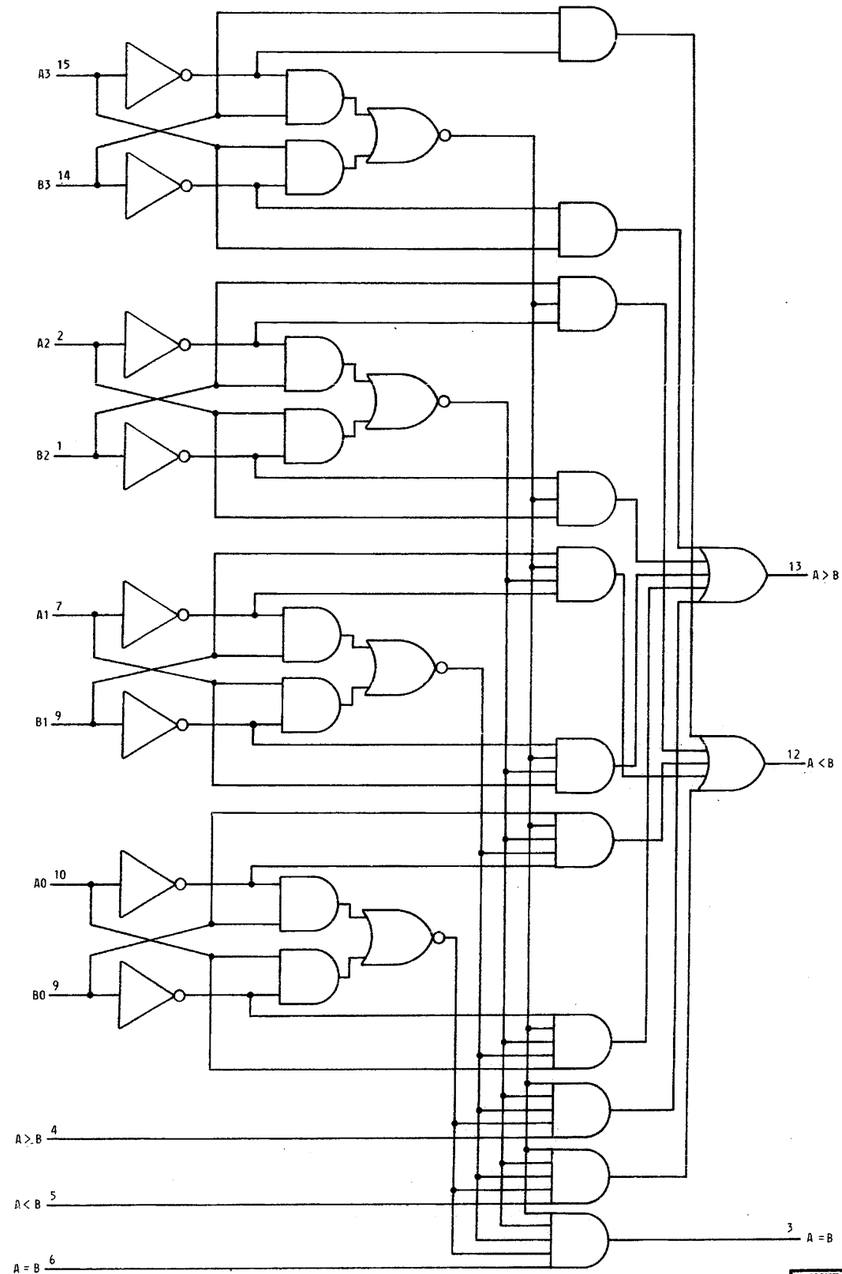
NOTES:

1. PIN NUMBERING, TOP VIEW.



2. PIN NUMBERING, TOP VIEW.





ISSUE 1

DATA TEST SET NO. 911NA

SD-73094-01-D4

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

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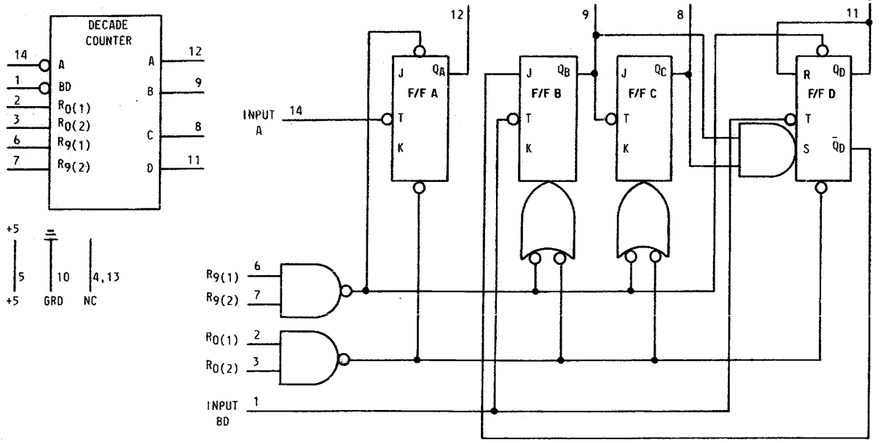
SD-73094-01-D4

INFORMATION NOTES: (CONT)

302. (CONT)

(O) DECADE COUNTER, SN7490, 1 PER DEVICE, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS ONE DECADE COUNTER, CONSISTING OF FOUR MASTER SLAVE FLIP-FLOPS WHICH ARE INTERNALLY INTERCONNECTED TO PROVIDE A DIVIDE-BY-2 COUNTER AND A DIVIDE-BY-5 COUNTER. GATED DIRECT-RESET LINES ARE PROVIDED TO INHIBIT COUNT INPUTS AND RETURN ALL OUTPUTS TO A LOGICAL 0 OR TO A BINARY-CODED-DECIMAL (BCD) COUNT OF 9. AS THE OUTPUT FROM FLIP-FLOP A IS NOT INTERNALLY CONNECTED TO THE SUCCEEDING STAGES, THE COUNTER MAY BE OPERATED IN ANY ONE OF THREE INDEPENDENT COUNT MODES:

1. WHEN USED AS A BINARY-CODED-DECIMAL DECADE COUNTER, THE BD INPUT MUST BE EXTERNALLY CONNECTED TO THE Q_A OUTPUT. THE A INPUT RECEIVES THE INCOMING COUNT, AND A COUNT SEQUENCE IS OBTAINED IN ACCORDANCE WITH THE BCD COUNT SEQUENCE TRUTH TABLE SHOWN BELOW. IN ADDITION TO A CONVENTIONAL ZERO RESET, INPUTS ARE PROVIDED TO RESET A BCD COUNT FOR NINE'S COMPLEMENT DECIMAL APPLICATIONS.
2. IF A SYMMETRICAL DIVIDE-BY-TEN COUNT IS DESIRED FOR FREQUENCY SYNTHESIZERS OR OTHER APPLICATIONS REQUIRING DIVISION OF A BINARY COUNT BY A POWER OF TEN, THE Q_D OUTPUT MUST BE EXTERNALLY CONNECTED TO THE A INPUT. THE INPUT COUNT IS THEN APPLIED AT THE BD INPUT AND A DIVIDE-BY-TEN SQUARE WAVE IS OBTAINED AT OUTPUT Q_A IN ACCORDANCE WITH THE BI-QUINARY TRUTH TABLE BELOW.
3. FOR OPERATION AS A DIVIDE-BY-TWO COUNTER AND A DIVIDE-BY-FIVE COUNTER, NO EXTERNAL INTERCONNECTIONS ARE REQUIRED. FLIP-FLOP A IS USED AS A BINARY ELEMENT FOR THE DIVIDE-BY-TWO FUNCTION. THE BD INPUT IS USED TO OBTAIN BINARY DIVIDE-BY-FIVE OPERATION AT THE Q_B, Q_C, AND Q_D OUTPUTS. IN THIS MODE, THE TWO COUNTERS OPERATE INDEPENDENTLY; HOWEVER, ALL FOUR FLIP-FLOPS ARE RESET SIMULTANEOUSLY.

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

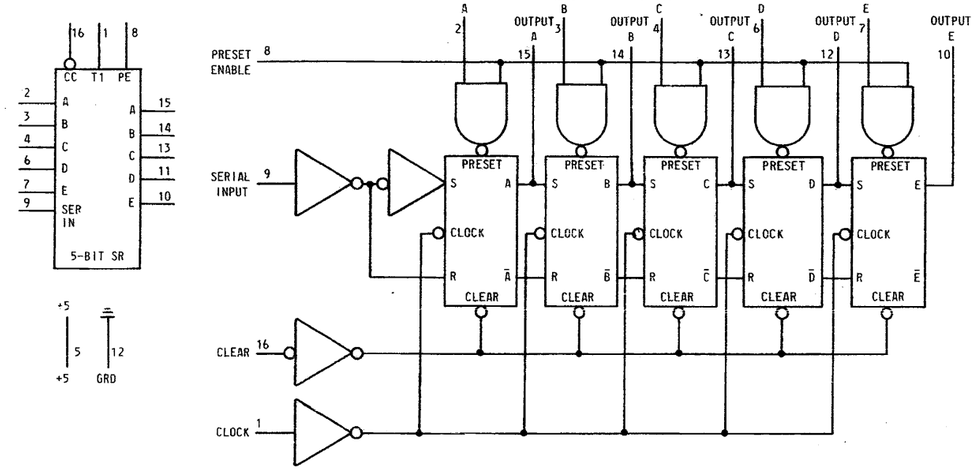
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$F_{9(1)}$	$R_{9(2)}$	D	C	B	A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES: A. OUTPUT Q_A IS CONNECTED TO INPUT BD FOR BCD COUNT.
B. OUTPUT Q_D IS CONNECTED TO INPUT A FOR BI-QUINARY COUNT
C. H = 1, L = 0, X = IRRELEVANT.

INFORMATION NOTES: (CONT)

302. (CONT)

(P) 5-BIT SHIFT REGISTER, SN7496, 1 PER DEVICE, SEE NOTE 2.



CIRCUIT DESCRIPTION

THIS DEVICE CONSISTS OF FIVE R-S MASTER-SLAVE FLIP-FLOPS CONNECTED TO PERFORM PARALLEL-TO-SERIAL OR SERIAL-TO-PARALLEL CONVERSION OF BINARY DATA. SINCE BOTH INPUTS AND OUTPUTS TO ALL FLIP-FLOPS ARE ACCESSIBLE, PARALLEL-IN/PARALLEL-OUT OR SERIAL-IN/SERIAL-OUT OPERATION MAY BE PERFORMED.

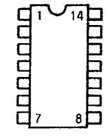
ALL FLIP-FLOPS ARE SIMULTANEOUSLY SET TO LOGICAL 0 STATE BY APPLYING A LOGICAL 0 VOLTAGE TO THE CLEAR INPUT. THIS CONDITION MAY BE APPLIED INDEPENDENT OF THE STATE OF THE CLOCK INPUT.

THE FLIP-FLOPS MAY BE INDEPENDENTLY SET TO THE LOGICAL 1 STATE BY APPLYING A LOGICAL 1 TO BOTH THE PRESET INPUT OF THE SPECIFIC FLIP-FLOP AND THE COMMON PRESET INPUT. THE PRESET-ENABLE INPUT IS PROVIDED TO ALLOW FLEXIBILITY OF EITHER SETTING EACH FLIP-FLOP INDEPENDENTLY OR SETTING TWO OR MORE FLIP-FLOPS SIMULTANEOUSLY. PRESET IS ALSO INDEPENDENT OF THE STATE OF THE CLOCK INPUT OR CLEAR INPUT.

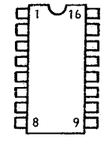
TRANSFER OF INFORMATION TO THE OUTPUT PINS OCCURS WHEN THE CLOCK INPUT GOES FROM A LOGICAL 0 TO A LOGICAL 1. SINCE THE FLIP-FLOPS ARE R-S MASTER-SLAVE CIRCUITS, THE PROPER INFORMATION MUST APPEAR AT THE R-S INPUTS OF EACH FLIP-FLOP PRIOR TO THE RISING EDGE OF THE CLOCK INPUT VOLTAGE WAVEFORM. THE CLEAR INPUT MUST BE AT A LOGICAL 1 AND THE PRESET INPUT MUST BE AT A LOGICAL 0 WHEN CLOCKING OCCURS.

NOTES:

1. PIN NUMBERING, TOP VIEW.



2. PIN NUMBERING, TOP VIEW.



ISSUE 2D

DATA TEST SET NO. 911NA	SD-73094-01-D5
BELL TELEPHONE LABORATORIES INCORPORATED	DWG SIZE 6S PRINTED IN U.S.A.

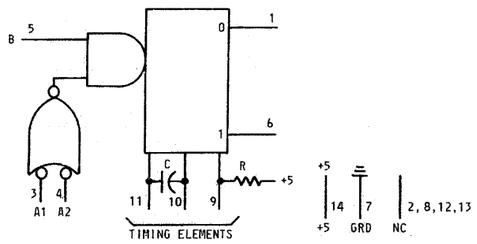
SD-73094-01-D5

E-7421 (10-71)

INFORMATION NOTES: (CONT)

302. (CONT)

(Q) SINGLE SHOT MONOSTABLE MULTIVIBRATOR, KS-20969 L8, SN74121, 1 PER DEVICE, SEE NOTE 1.



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS 1 SINGLE SHOT MONOSTABLE CIRCUIT.

ONCE FIRED, THE OUTPUTS ARE INDEPENDENT OF FURTHER TRANSITIONS ON THE INPUTS AND ARE A FUNCTION ONLY OF THE TIMING ELEMENTS. INPUT PULSES MAY BE OF ANY DURATION RELATIVE TO THE OUTPUT PULSE. OUTPUT PULSE LENGTHS MAY BE VARIED FROM 40 NANOSECONDS TO 40 SECONDS BY CHOOSING APPROPRIATE TIMING COMPONENTS. WITH NO EXTERNAL TIMING COMPONENTS (I.E., PIN (9) CONNECTED TO PIN (14), PINS (10), (11) OPEN) AN OUTPUT PULSE OF TYPICALLY 30 NANOSECONDS IS ACHIEVED WHICH MAY BE USED AS A D.C. TRIGGERED RESET SIGNAL. OUTPUT RISE AND FALL TIMES ARE TTL COMPATIBLE AND INDEPENDENT OF PULSE LENGTH.

A1 AND A2 ARE NEGATIVE-EDGE-TRIGGERED LOGIC INPUTS, AND WILL TRIGGER ONE SHOT WHEN EITHER OR BOTH GO TO LOGICAL 0 WITH B AT LOGICAL 1.

B IS A POSITIVE INPUT FOR SLOW EDGES OR LOW LEVEL DETECTION, AND WILL TRIGGER THE ONE SHOT WHEN B GOES TO LOGICAL 1 WITH EITHER A1 OR A2 AT LOGICAL 0.

EXTERNAL TIMING CAPACITOR (C) MAY BE CONNECTED BETWEEN PIN 10 (POSITIVE) AND PIN 11. WITH NO EXTERNAL CAPACITANCE, AN OUTPUT PULSE WIDTH OF TYPICALLY 30 ns IS OBTAINED.

TO USE THE INTERNAL TIMING RESISTOR (2K NOMINAL), CONNECT PIN 9 TO 14.

TO OBTAIN VARIABLE PULSE WIDTH CONNECT EXTERNAL VARIABLE RESISTANCE (R) BETWEEN PIN 9 AND 14.

TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

X - 0 OR 1 MAY BE PRESENT

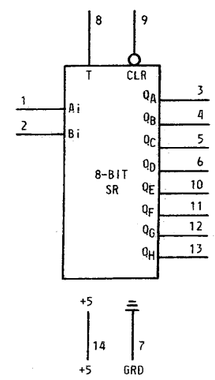
tn - TIME BEFORE INPUT TRANSITION

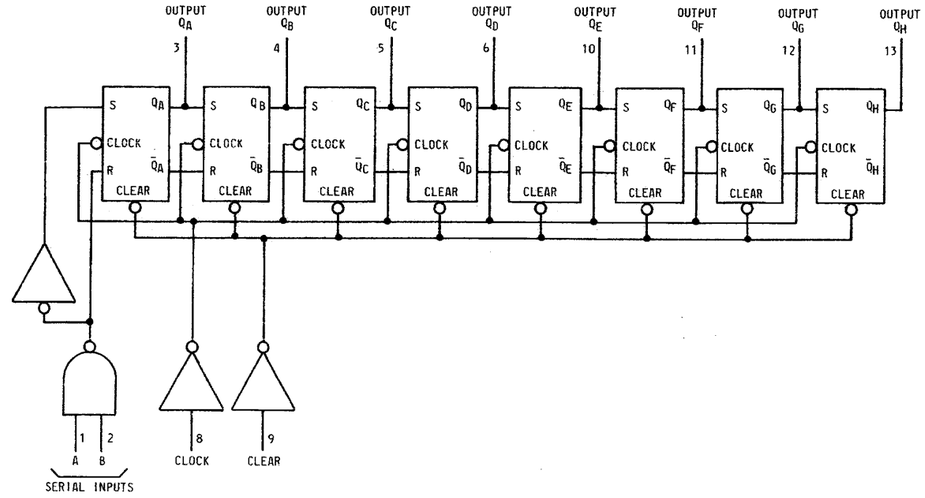
tn+1 - TIME AFTER INPUT TRANSITION

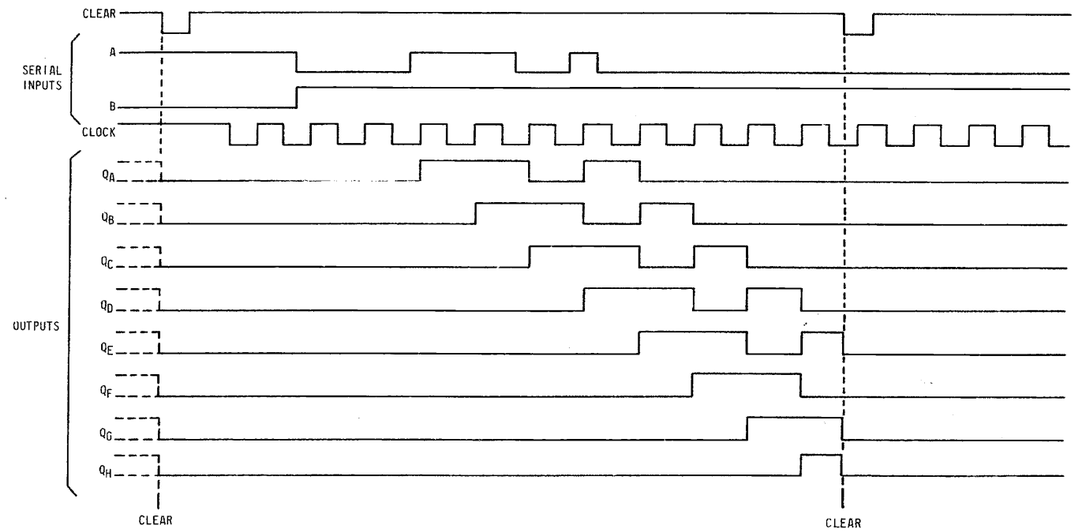
INFORMATION NOTES: (CONT)

302. (CONT)

(R) 8-BIT SHIFT REGISTER, KS-20969 L25, SN74164, 1 PER DEVICE, SEE NOTE 1.







CIRCUIT DESCRIPTION

THIS DEVICE CONSISTS OF EIGHT R-S MASTER-SLAVE FLIP-FLOPS CONNECTED TO PERFORM SERIAL-TO-PARALLEL CONVERSION OF BINARY DATA.

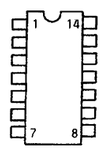
THESE 8-BIT SHIFT REGISTERS FEATURE GATED SERIAL INPUTS AND AN ASYNCHRONOUS CLEAR. THE GATED SERIAL INPUTS (A AND B) PERMIT COMPLETE CONTROL OVER INCOMING DATA AS A LOW AT EITHER (OR BOTH) INPUT(S) INHIBITS ENTRY OF THE NEW DATA AND RESETS THE FIRST FLIP-FLOP TO THE LOW LEVEL AT THE NEXT CLOCK PULSE. A HIGH-LEVEL INPUT ENABLES THE OTHER INPUT WHICH WILL THEN DETERMINE THE STATE OF THE FIRST FLIP-FLOP. DATA AT SERIAL INPUTS MAY BE CHANGED WHILE THE CLOCK IS HIGH, BUT ONLY INFORMATION MEETING THE SETUP REQUIREMENTS WILL BE ENTERED. CLOCKING OCCURS ON THE LOW-TO-HIGH-LEVEL TRANSITION OF THE CLOCK INPUT.

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

NOTES:

1. PIN NUMBERING, TOP VIEW.



ISSUE 2D

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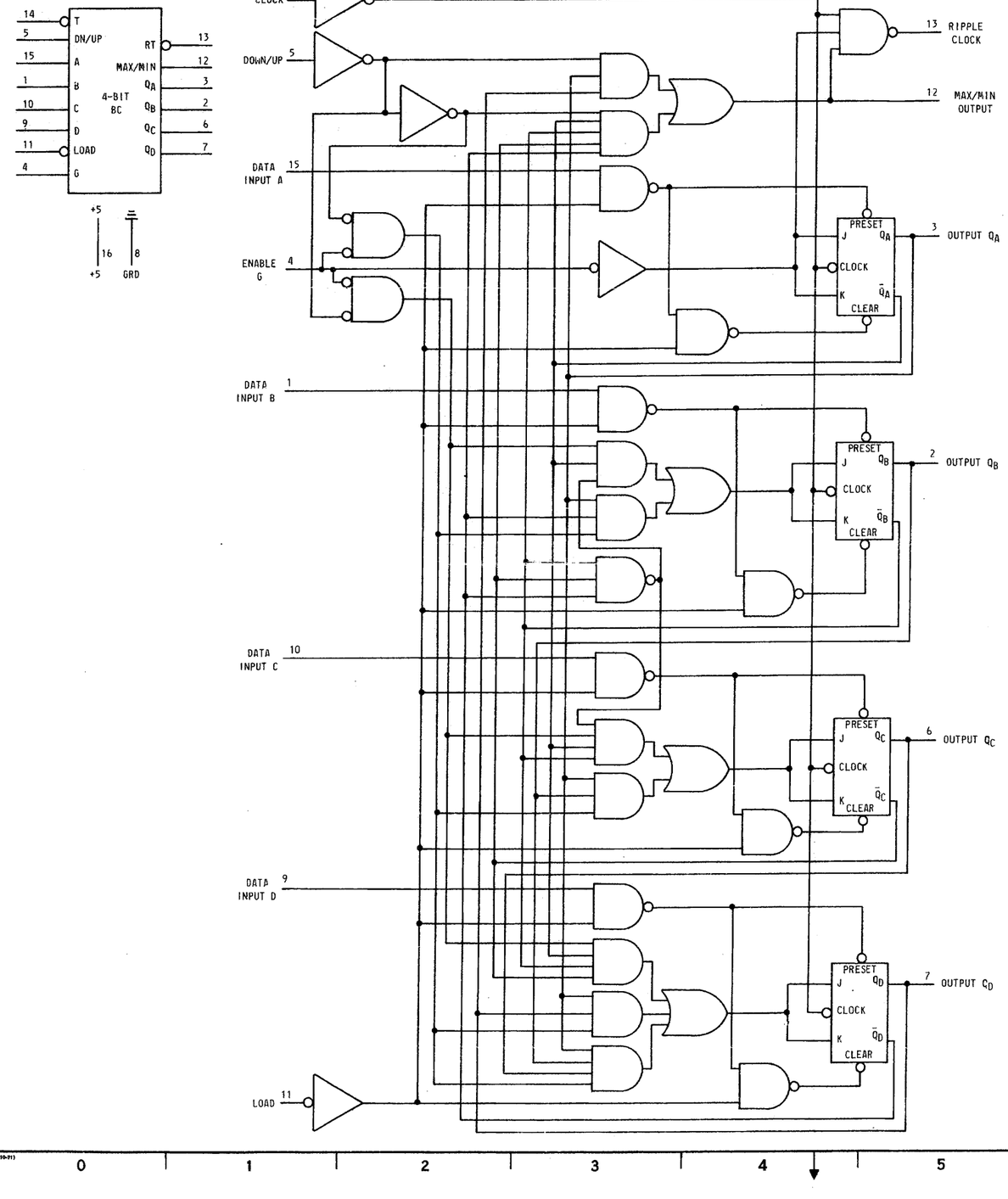
INFORMATION NOTES: (CONT)

302. (CONT)

(S) 4-BIT SYNCHRONOUS, REVERSIBLE UP/DOWN BINARY COUNTER, KS-20969 L9, SN74191, 1 PER DEVICE, SEE NOTE 1.



INFORMATION NOTES: (CONT)

302. (CONT)

(S) (CONT)

CIRCUIT DESCRIPTION

THIS DEVICE CONSISTS OF FOUR J-K MASTER-SLAVE FLIP-FLOPS AND ASSOCIATED GATES INTERNALLY CONNECTED TO PROVIDE 4-BIT SYNCHRONOUS, REVERSIBLE UP/DOWN BINARY COUNTER. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENT WITH EACH OTHER WHEN SO INSTRUCTED BY THE STEERING LOGIC. THIS MODE OF OPERATION WILL ELIMINATE THE OUTPUT COUNTING SPIKES WHICH ARE NORMALLY ASSOCIATED WITH ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS.

THE OUTPUTS OF THE FOUR MASTER-SLAVE FLIP-FLOPS ARE TRIGGERED ON A LOW-TO-HIGH-LEVEL TRANSITION OF THE CLOCK INPUT IF THE ENABLE INPUT IS LOW. A HIGH AT THE ENABLE INPUT INHIBITS COUNTING. LEVEL CHANGES AT THE ENABLE INPUT SHOULD BE MADE ONLY WHEN THE CLOCK INPUT IS HIGH. THE DIRECTION OF THE COUNT IS DETERMINED BY THE STATE OF THE DOWN/UP INPUT. WHEN LOW, THE COUNTER COUNTS UP AND WHEN HIGH, IT COUNTS DOWN.

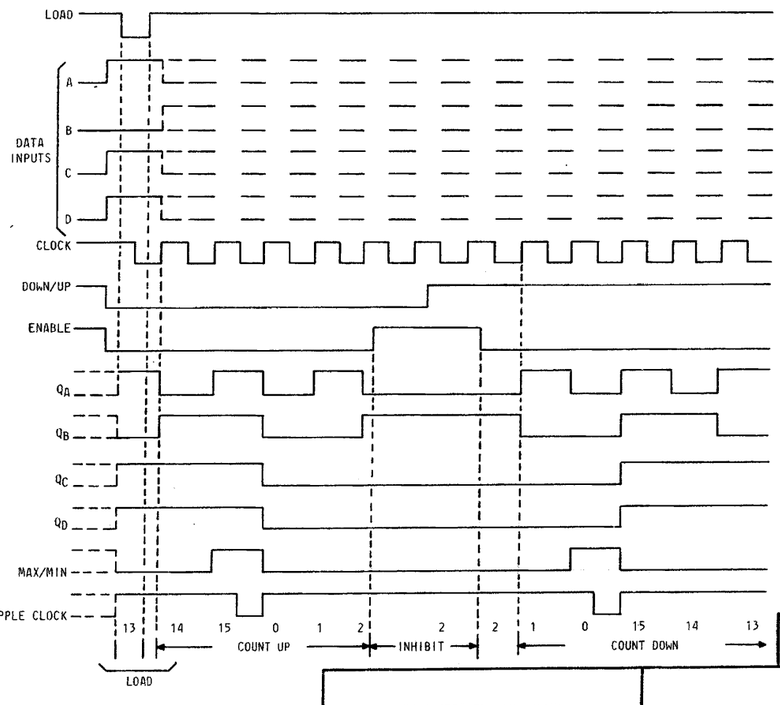
THESE COUNTERS ARE FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAY BE PRESET TO ANY STATE BY PLACING A LOW ON THE LOAD INPUT AND ENTERING THE DESIRED DATA AT THE DATA INPUTS. THE OUTPUT WILL CHANGE TO AGREE WITH THE DATA INPUTS INDEPENDENTLY OF THE STATE OF THE CLOCK INPUT. THIS FEATURE ALLOWS THE COUNTERS TO BE USED AS MODULO-N DIVIDERS BY SIMPLY MODIFYING THE COUNT LENGTH WITH THE PRESET INPUTS.

TWO OUTPUTS HAVE BEEN MADE AVAILABLE TO PERFORM THE CASCADING FUNCTION: RIPPLE CLOCK AND MAXIMUM/MINIMUM COUNT. THE LATTER OUTPUT PRODUCES A HIGH-LEVEL OUTPUT PULSE WITH A DURATION APPROXIMATELY EQUAL TO ONE COMPLETE CYCLE OF THE CLOCK WHEN THE COUNTER OVERFLOWS OR UNDERFLOWS. THE RIPPLE CLOCK OUTPUT PRODUCES A LOW-LEVEL OUTPUT PULSE EQUAL IN WIDTH TO THE LOW-LEVEL PORTION OF THE CLOCK INPUT WHEN AN OVERFLOW OR UNDERFLOW CONDITION EXISTS. THE COUNTERS CAN BE EASILY CASCADED BY FEEDING THE RIPPLE CLOCK OUTPUT TO THE ENABLE INPUT OF THE SUCCEEDING COUNTER IF PARALLEL CLOCKING IS USED, OR TO THE CLOCK INPUT IF PARALLEL ENABLING IS USED. THE MAXIMUM/MINIMUM COUNT OUTPUT CAN BE USED TO ACCOMPLISH LOOK-AHEAD FOR HIGH-SPEED OPERATION.

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

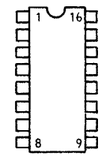
ILLUSTRATED BELOW IS THE FOLLOWING SEQUENCE:

1. LOAD (PRESET) TO BINARY THIRTEEN.
2. COUNT UP TO FOURTEEN, FIFTEEN (MAXIMUM), ZERO, ONE, AND TWO.
3. INHIBIT.
4. COUNT DOWN TO ONE, ZERO (MINIMUM), FIFTEEN, FOURTEEN, AND THIRTEEN.



NOTES:

1. PIN NUMBERING, TOP VIEW.



ISSUE 2D

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DWG SIZE 6S

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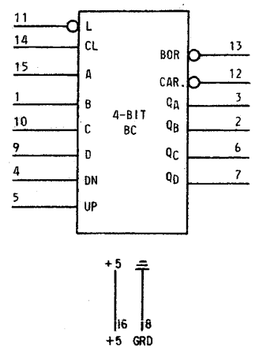
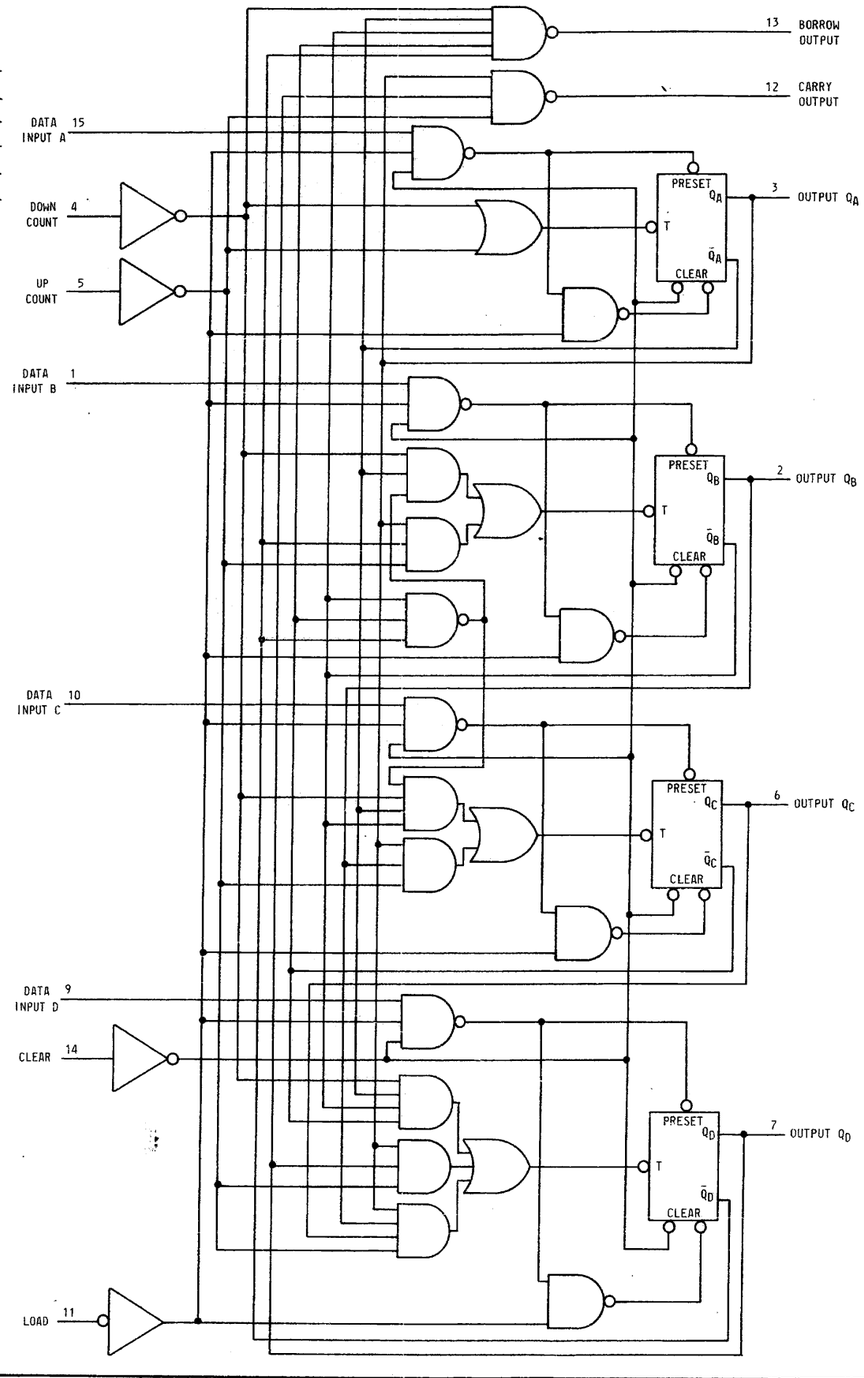
INFORMATION NOTES: (CONT)

302. (CONT)

(T) 4-BIT SYNCHRONOUS, REVERSIBLE UP/DOWN DECADE COUNTER, KS-20969 L10, SN74192, 1 PER DEVICE, SEE NOTE 1.





INFORMATION NOTES: (CONT)

302. (CONT)

(T) (CONT)

CIRCUIT DESCRIPTION

THIS DEVICE CONSISTS OF FOUR MASTER-SLAVE FLIP-FLOPS AND ASSOCIATED GATES INTERNALLY CONNECTED TO PROVIDE 4-BIT SYNCHRONOUS, REVERSIBLE UP/DOWN DECADE COUNTER. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT OUTPUT CHANGES **COINCIDE WITH EACH OTHER** WHEN SO INSTRUCTED BY THE STEERING LOGIC. THIS MODE OF OPERATION ELIMINATES THE OUTPUT COUNTING SPIKES WHICH ARE NORMALLY ASSOCIATED WITH ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS.

THE OUTPUTS OF THE FOUR MASTER SLAVE FLIP-FLOPS ARE TRIGGERED BY A LOW-TO-HIGH-LEVEL TRANSITION OF EITHER COUNT (CLOCK) INPUT. THE DIRECTION OF COUNTING IS DETERMINED BY WHICH COUNT INPUT IS PULSED WHILE THE OTHER COUNT INPUT IS HIGH.

ALL FOUR COUNTERS ARE FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAY BE PRESET TO ANY STATE BY ENTERING THE DESIRED DATA AT THE DATA INPUTS WHILE THE LOAD INPUT IS LOW. THE OUTPUT WILL CHANGE TO AGREE WITH THE DATA INPUTS INDEPENDENTLY OF THE COUNT PULSES. THIS FEATURE ALLOWS THE COUNTERS TO BE USED AS MODULO-N DIVIDERS BY SIMPLY MODIFYING THE COUNT LENGTH WITH THE PRESET INPUTS.

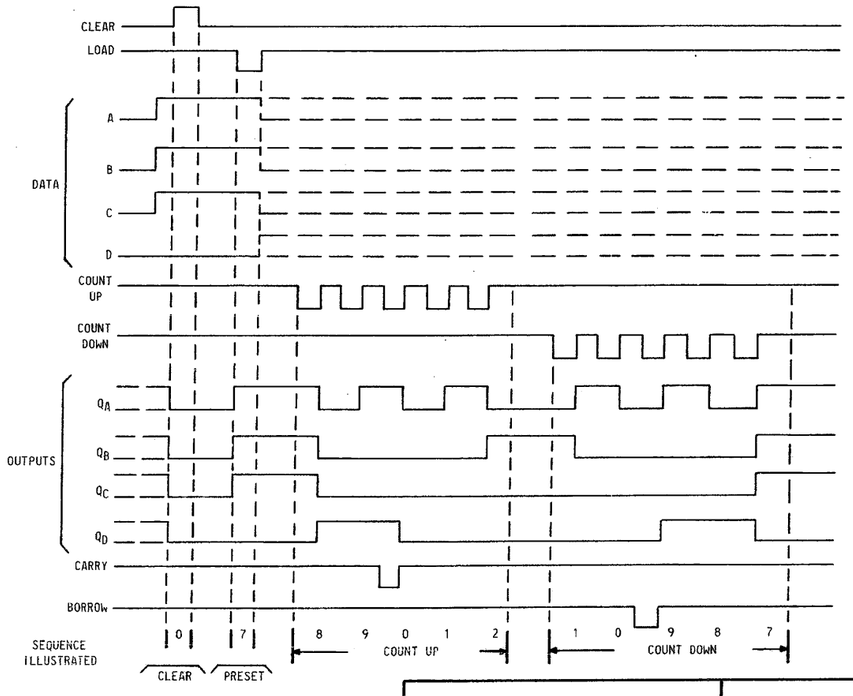
A CLEAR INPUT HAS BEEN PROVIDED WHICH FORCES ALL OUTPUTS TO THE LOW LEVEL WHEN A HIGH LEVEL IS APPLIED. THE CLEAR FUNCTION IS INDEPENDENT OF THE COUNT AND LOAD INPUTS.

THESE COUNTERS WERE DESIGNED TO BE CASCADED WITHOUT THE NEED FOR EXTERNAL CIRCUITRY. BOTH BORROW AND CARRY OUTPUTS ARE AVAILABLE TO CASCADE BOTH THE UP- AND DOWN-COUNTING FUNCTIONS. THE BORROW OUTPUT PRODUCES A PULSE EQUAL IN WIDTH TO THE COUNT-DOWN INPUT WHEN THE COUNTER UNDERFLOWS. SIMILARLY, THE CARRY OUTPUT PRODUCES A PULSE EQUAL IN WIDTH TO THE COUNT-UP INPUT WHEN AN OVERFLOW CONDITION EXISTS. THE COUNTERS CAN THEN BE EASILY CASCADED BY FEEDING THE BORROW AND CARRY OUTPUTS TO THE COUNT-DOWN AND COUNT-UP INPUTS RESPECTIVELY OF THE SUCCEEDING COUNTER.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

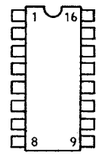
ILLUSTRATED BELOW IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUTS TO ZERO.
2. LOAD (PRESET) TO BCD SEVEN.
3. COUNT UP TO EIGHT, NINE, CARRY, ZERO, ONE, AND TWO.
4. COUNT DOWN TO ONE, ZERO, BORROW, NINE, EIGHT, AND SEVEN.



NOTES.

1. PIN NUMBERING, TOP VIEW.



ISSUE 2D

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DWG SIZE 6S

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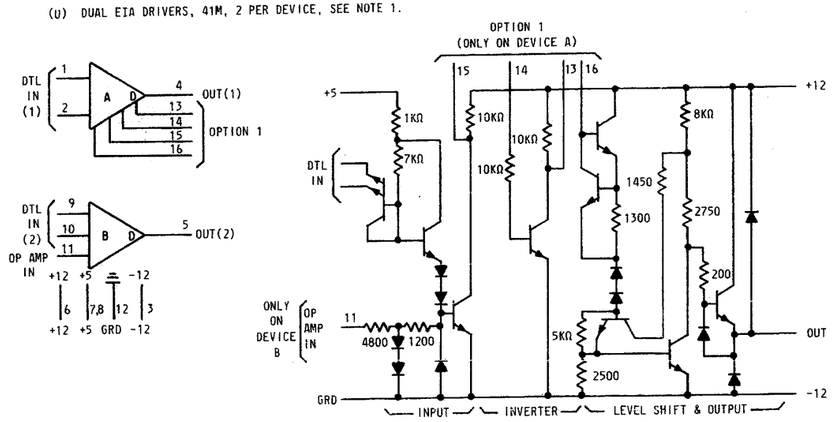
SD-73094-01-D8

INFORMATION NOTES: (CONT)

302. (CONT)

(U) DUAL EIA DRIVERS, 41M, 2 PER DEVICE, SEE NOTE 1.

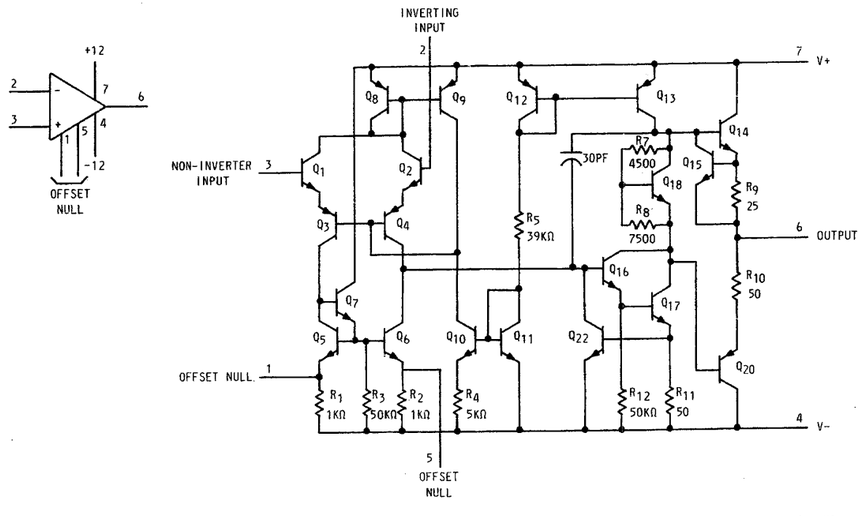


CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS TWO EIA DRIVER CIRCUITS WHICH CONVERT DATA SET LOGIC LEVELS TO PRESCRIBED EIA SIGNAL LEVELS. DEVICE A ALLOWS INVERSION OR NON-INVERSION OF SIGNALS BY APPROPRIATELY STRAPPING THE OPTION 1 PINS (SEE TABLE). DEVICE B DOES NOT HAVE THE OPTION PROVISION; NON-INVERSION OF INPUT-OUTPUT SIGNALS IS PROVIDED. INPUT-OUTPUT SIGNAL RELATIONS ARE GIVEN BY THE NON-INVERTING OPTION OF THE TABLE. INSTEAD OF USING LOGIC SIGNALS, DEVICE B PROVIDES FOR SIGNAL CONTROL BY AN OPERATIONAL AMPLIFIER VIA THE OP AMP IN INPUT (PIN 11).

LOGIC INPUT		OUTPUT PIN 4	OPTION 1 CONNECTIONS	MODE
PIN 1	PIN 2			
1	1	>+6.8V	PIN 15 TO PIN 16 PIN 14 TO PIN 12 (OPTIONAL)	NON-INVERTING
1	0	<-7.5V		
0	1			
0	0			
1	1	<-7.5V	PIN 15 TO PIN 14 PIN 13 TO PIN 16	INVERTING
1	0	>+6.8V		
0	1			
0	0			

(V) OPERATIONAL AMPLIFIER, 741TC, 1 PER DEVICE, SEE NOTE 2.

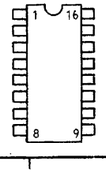


CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS AN OPERATIONAL AMPLIFIER CONSTRUCTED ON A SINGLE CHIP. IT IS INTENDED FOR A WIDE RANGE OF ANALOG APPLICATIONS. HIGH COMMON VOLTAGE RANGE AND ABSENCE OF "LATCH-UP" TENDENCIES MAKE THE OPERATIONAL AMPLIFIER IDEAL FOR USE AS A VOLTAGE FOLLOWER. THE HIGH GAIN AND WIDE RANGE OF OPERATING VOLTAGES PROVIDE SUPERIOR PERFORMANCE IN INTEGRATOR, SUMMING AMPLIFIER, AND GENERAL FEEDBACK APPLICATIONS.

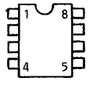
NOTES:

1. PIN NUMBERING, TOP VIEW.



NOTES: (CONT)

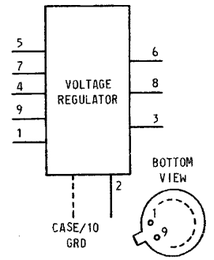
2. PIN NUMBERING, TOP VIEW.



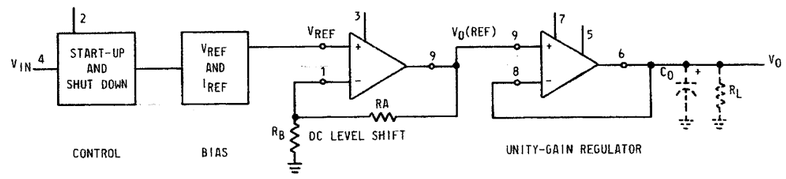
INFORMATION NOTES: (CONT)

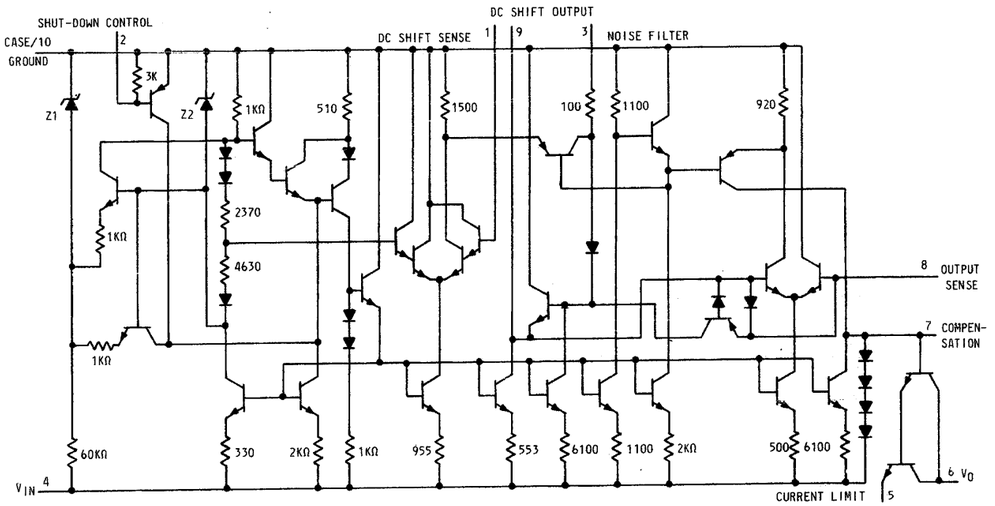
302. (CONT)

(W) NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR, MC1463, 1 PER DEVICE.



SIMPLIFIED CIRCUIT SCHEMATIC OF VOLTAGE REGULATOR





CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS A VOLTAGE REGULATOR CONSTRUCTED ON A SINGLE CHIP. THE SIMPLIFIED CIRCUIT SCHEMATIC SHOWS FOUR BASIC SECTIONS OF THE VOLTAGE REGULATOR: CONTROL, BIAS, DC LEVEL SHIFT, AND OUTPUT (UNITY GAIN REGULATOR). EACH SECTION IS DETAILED IN THE FOLLOWING PARAGRAPHS.

CONTROL

THE CONTROL SECTION INVOLVES TWO BASIC FUNCTIONS, START-UP AND SHUT-DOWN. A START-UP FUNCTION IS REQUIRED SINCE THE BIASING IS ESSENTIALLY INDEPENDENT OF THE UNREGULATED INPUT VOLTAGE. IT MAKES USE OF TWO ZENER DIODES HAVING THE SAME BREAKDOWN VOLTAGE. A FIRST OR AUXILIARY ZENER IS DRIVEN DIRECTLY FROM THE INPUT VOLTAGE LINE THROUGH A RESISTOR (60KΩ) AND PERMITS THE REGULATOR TO INITIALLY ACHIEVE THE DESIRED BIAS CONDITIONS. THIS PERMITS THE SECOND, OR REFERENCE ZENER TO BE DRIVEN FROM A CURRENT SOURCE. WHEN THE REFERENCE ZENER ENTERS BREAKDOWN, THE AUXILIARY ZENER IS ISOLATED FROM THE REST OF THE REGULATOR CIRCUITRY BY A DIODE DISCONNECT TECHNIQUE. THIS IS NECESSARY TO KEEP THE ADDED NOISE AND RIPPLE OF THE AUXILIARY ZENER FROM DEGRADING THE PERFORMANCE OF THE REGULATOR.

THE SHUT-DOWN CONTROL, IN EFFECT, CONSISTS OF A PNP TRANSISTOR ACROSS THE REFERENCE ZENER DIODE. WHEN THIS TRANSISTOR IS TURNED "ON", VIA PIN 2, THE REFERENCE VOLTAGE IS REDUCED TO ESSENTIALLY ZERO VOLTS AND THE REGULATOR IS FORCED TO SHUT-DOWN. DURING SHUT-DOWN THE CURRENT DRAIN OF THE COMPLETE IC REGULATOR DROPS TO V_{IN}/60KΩ OR 500 uA FOR A -30V INPUT.

BIAS

A ZENER DIODE IS THE MAIN REFERENCE ELEMENT AND FORMS THE HEART OF THE BIAS CIRCUITRY. ITS POSITIVE TEMPERATURE COEFFICIENT IS BALANCED BY THE NEGATIVE TEMPERATURE COEFFICIENT OF FORWARD BIASED DIODES IN A RATIO DETERMINED BY THE RESISTORS IN THE DIODE STRING. THE RESULT IS A REFERENCE VOLTAGE OF APPROXIMATELY -3.5V DC WITH A TYPICAL TEMPERATURE COEFFICIENT OF 0.002%/°C. IN ADDITION, THIS CIRCUIT ALSO PROVIDES A REFERENCE CURRENT WHICH IS USED TO BIAS ALL CURRENT SOURCES IN THE REMAINING REGULATOR CIRCUITRY.

CIRCUIT DESCRIPTION (CONT)

DC LEVEL SHIFT

THE REFERENCE VOLTAGE IS USED AS THE INPUT TO A DARLINGTON DIFFERENTIAL AMPLIFIER. THE GAIN OF THIS AMPLIFIER IS QUITE HIGH AND IT THEREFORE MAY BE CONSIDERED TO FUNCTION AS A CONVENTIONAL OPERATIONAL AMPLIFIER. CONSEQUENTLY, NEGATIVE FEEDBACK CAN BE EMPLOYED USING TWO EXTERNAL RESISTORS (R_A AND R_B) TO SET THE CLOSED-LOOP GAIN AND TO BOOST THE REFERENCE VOLTAGE TO THE DESIRED OUTPUT VOLTAGE. A CAPACITOR, C_N, IS INTRODUCED EXTERNALLY INTO THE LEVEL SHIFT NETWORK (VIA PIN 3) TO STABILIZE THE AMPLIFIER AND TO FILTER THE ZENER NOISE. THE RECOMMENDED VALUE FOR THIS CAPACITOR IS 0.1 uF AND SHOULD HAVE A VOLTAGE RATING IN EXCESS OF THE DESIRED OUTPUT VOLTAGE. SMALLER CAPACITORS (0.001 uF MINIMUM) MAY BE USED BUT WILL CAUSE A SLIGHT INCREASE IN OUTPUT NOISE. LARGER VALUES OF C_N WILL REDUCE THE NOISE AS WELL AS DELAY THE START-UP OF THE REGULATOR.

OUTPUT REGULATOR

THE OUTPUT OF THE SHIFT AMPLIFIER IS FED INTERNALLY TO THE NON-INVERTING INPUT OF THE OUTPUT ERROR AMPLIFIER. THE INVERTING INPUT TO THIS AMPLIFIER IS THE OUTPUT SENSE CONNECTION (PIN 8) OF THE REGULATOR. A DARLINGTON CONNECTED NPN POWER TRANSISTOR IS USED TO HANDLE THE LOAD CURRENT. THE SHORT-CIRCUIT CURRENT LIMITING RESISTOR, R_{SC}, IS CONNECTED IN THE EMITTER OF THIS TRANSISTOR TO SAMPLE THE FULL LOAD CURRENT. THIS CONNECTION ENABLES A FOUR-DIODE STRING TO LIMIT THE DRIVE CURRENT TO THE POWER TRANSISTORS IN A CONVENTIONAL MANNER.

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-D9

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

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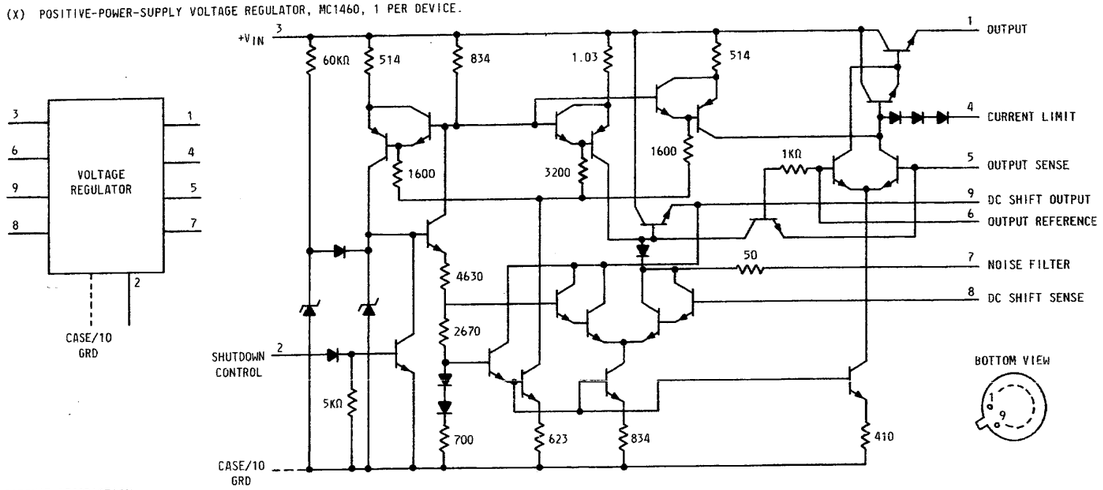
SD-73094-01-D9

INFORMATION NOTES: (CONT)

302. (CONT)

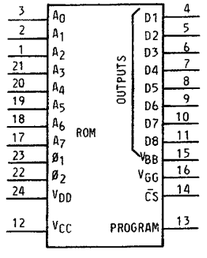
(X) POSITIVE-POWER-SUPPLY VOLTAGE REGULATOR, MC1460, 1 PER DEVICE.

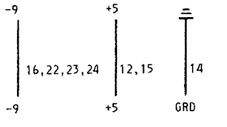


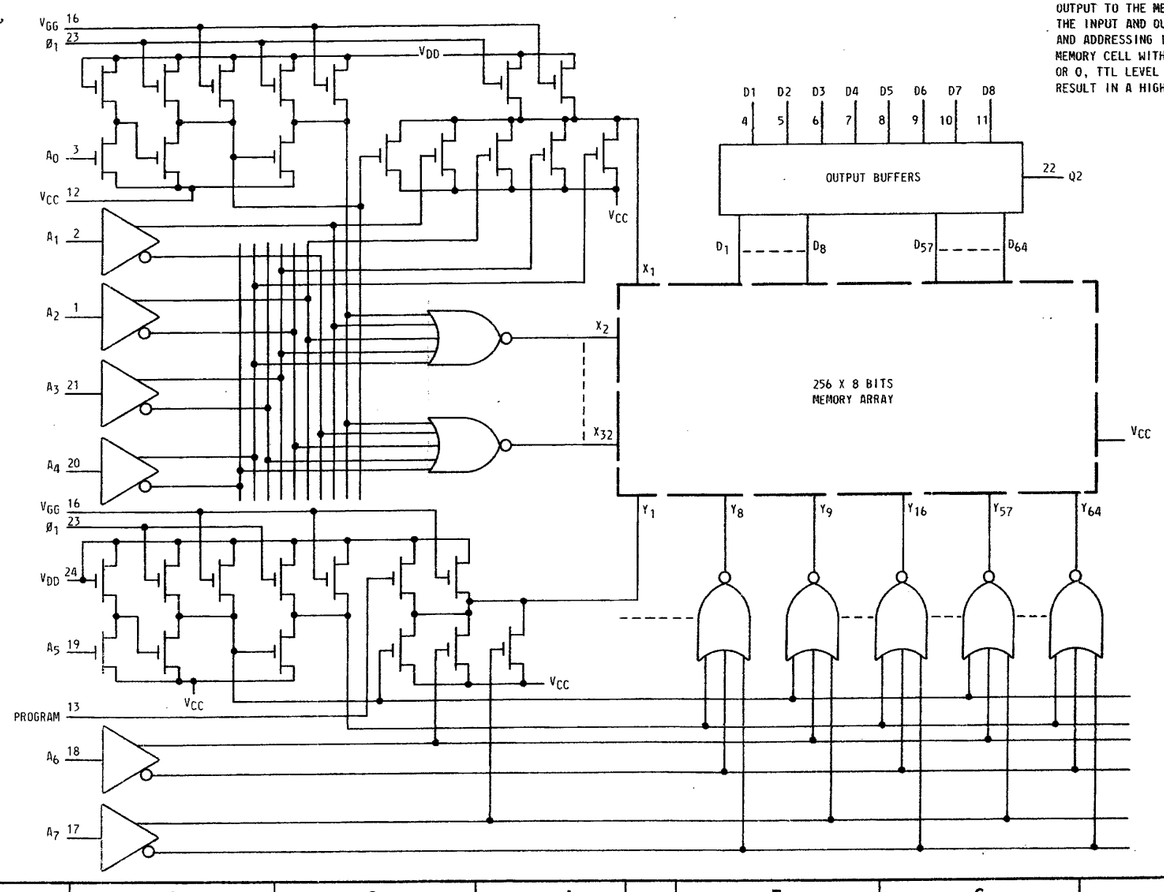
CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS A VOLTAGE REGULATOR CONSTRUCTED ON A SINGLE CHIP. FOR DESCRIPTION SEE NOTE 302 (W).

(Y) ROM, KS-21247,L1,1602, 1 PER DEVICE, SEE NOTE 1.





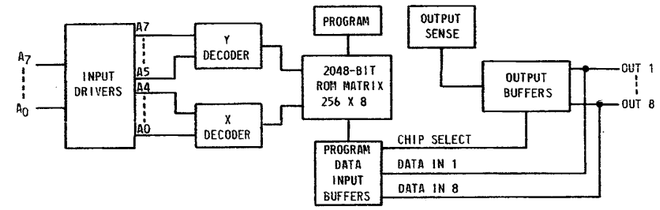


INFORMATION NOTES: (CONT)

302. (CONT)

(Y) (CONT)

SIMPLIFIED CIRCUIT SCHEMATIC OF ROM



CIRCUIT DESCRIPTION

THIS DEVICE CONTAINS 1 ROM.

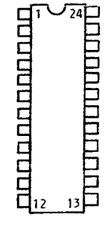
THIS CELL DESIGN IS ORGANIZED INTO 256 WORDS OF 8 BITS IN THE 2,048-BIT ROM. ALL CIRCUIT BLOCKS ARE COMMON TO BOTH PROGRAM AND READ MODES, WITH THE EXCEPTION OF THE PROGRAM DATA INPUT BUFFERS, WHICH ARE PART OF THE PROGRAM CIRCUIT ONLY.

AS THE SIMPLIFIED CIRCUIT SCHEMATIC SHOWS, IN THE PROGRAM MODE, THE EIGHT OUTPUT TERMINALS ARE USED AS DATA INPUTS TO DETERMINE THE INFORMATION PATTERN IN THE EIGHT BITS OF EACH WORD; WORD ADDRESS SELECTION IS PERFORMED BY THE X AND Y DECODERS THROUGH THE INPUT DRIVERS. INITIALLY ALL 2,048 BITS ARE IN THE 1 STATE, CORRESPONDING TO NORMALLY OFF, OR UNCHARGED STORAGE ELEMENTS. BY CHARGING THE STORAGE ELEMENTS FROM THE PROGRAM TERMINAL, 0s ARE SELECTIVELY ENTERED IN THE PROPER BIT LOCATIONS.

IN THE READ MODE, THE PROGRAM DATA INPUT BUFFERS ARE INSTRUCTED BY THE CHIP SELECT SIGNAL TO CUT OFF THE FEEDBACK PATH FROM THE OUTPUT TO THE MEMORY ARRAY ESTABLISHED IN THE PROGRAM MODE. THE INPUT AND OUTPUT BUFFERS PROVIDE FULL TLL COMPATIBILITY, AND ADDRESSING IS ACCOMPLISHED BY THE X AND Y DECODERS. A SELECT MEMORY CELL WITH CHARGED STORAGE ELEMENT WILL SHOW UP AS A LOW, OR 0, TTL LEVEL AT THE OUTPUT, WHILE A MEMORY BIT NOT CHARGED WILL RESULT IN A HIGH, OR 1, TTL LEVEL.

NOTES:

1. PIN NUMBERING, TOP VIEW.



ISSUE
1

DATA TEST SET NO. 911NA

SD-73094-01-D10

BELL TELEPHONE LABORATORIES INCORPORATED

CODE IDENT 6S

PRINTED IN U. S. A.

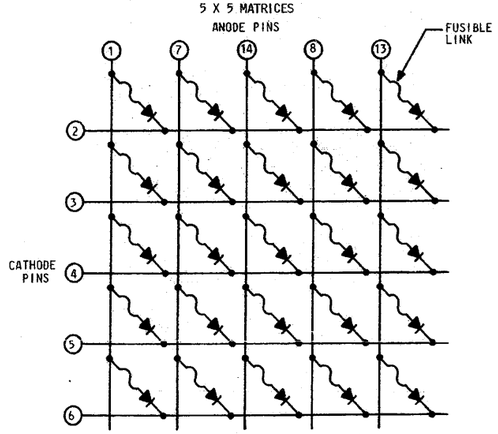
SD-73094-01-D10

INFORMATION NOTES: (CONT)

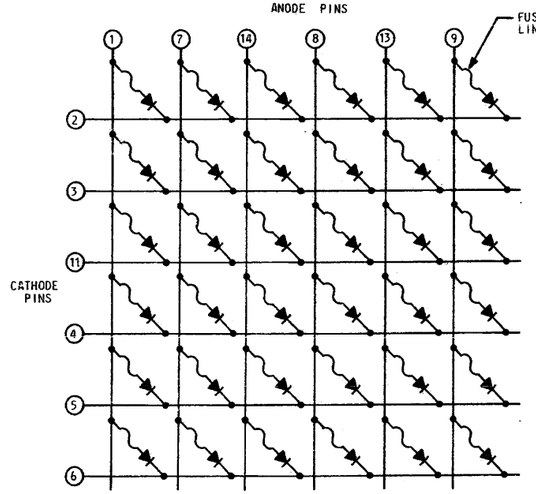
302. (CONT)

(Z) DIODE MATRICES, 1 PER DEVICE, SEE NOTE 1.

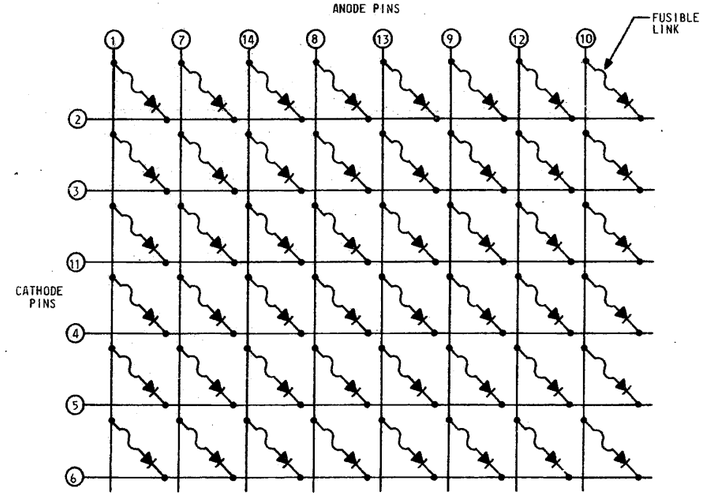
5 X 5 MATRICES
ANODE PINS



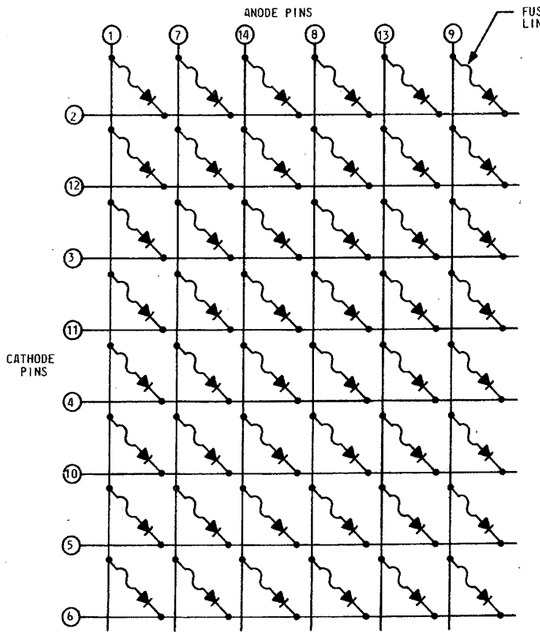
6 X 6 MATRICES
ANODE PINS



6 X 8 MATRICES
ANODE PINS



3 X 6 MATRICES
ANODE PINS



CIRCUIT DESCRIPTION

DIODE MATRICES CONSISTS OF ARRAYS OF PASSIVATED SILICONE DIODES, FABRICATED IN DIELECTRICALLY ISOLATED MOATS. USE OF IMPROVED EPITAXIAL TECHNIQUES ALLOW CONSTRUCTION OF ARRAYS USING THE EPITAXIAL LAYER AS THE COMMON CATHODE CONNECTION FOR ALL DIODES IN A ROW. COLUMN CONNECTIONS TO THE ANODE SIDE OF THE DIODES ARE MADE TO METALIZED INTERCONNECT LINES VIA FUSIBLE LINKS. BY SELECTIVELY OPENING FUSES, DIODES ARE EFFECTIVELY REMOVED FROM THE CIRCUIT TO FORM ANY DESIRED MATRIX PATTERN.

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-D11

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-D11

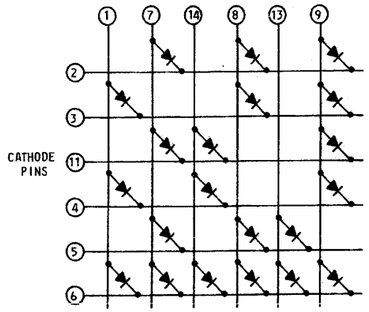
INFORMATION NOTES: (CONT)

302. (CONT)

IC20,CP1

6 X 6

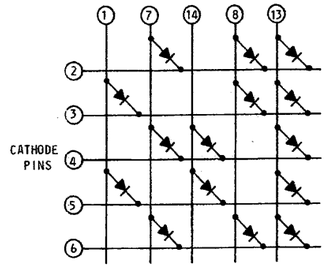
ANODE PINS



IC16,CP1

5 X 5

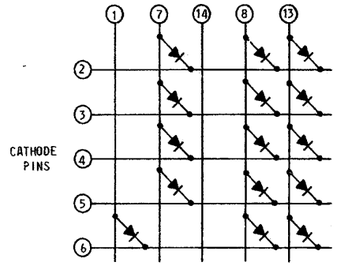
ANODE PINS



IC17,CP1

5 X 5

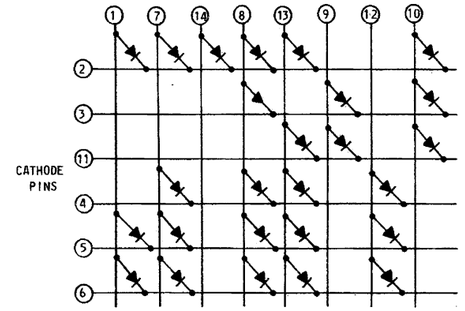
ANODE PINS



IC51, CP1

6 X 8

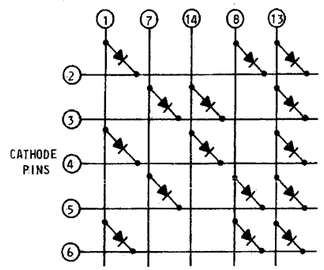
ANODE PINS



IC18,CP1

5 X 5

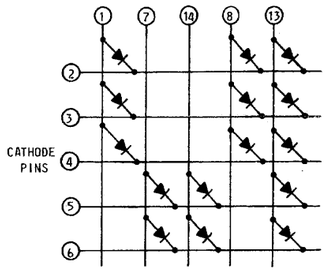
ANODE PINS



IC19,CP1

5 X 5

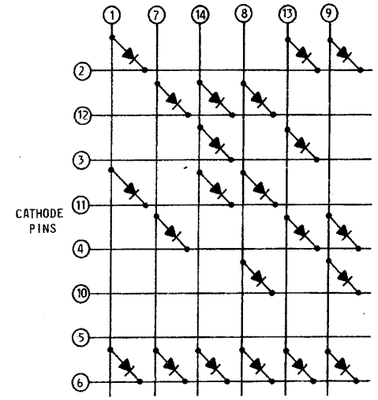
ANODE PINS



IC35, CP1

8 X 6

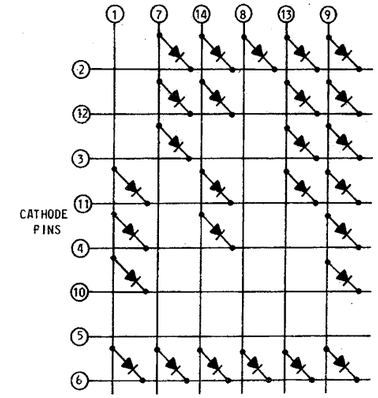
ANODE PINS



IC34, CP1

8 X 6

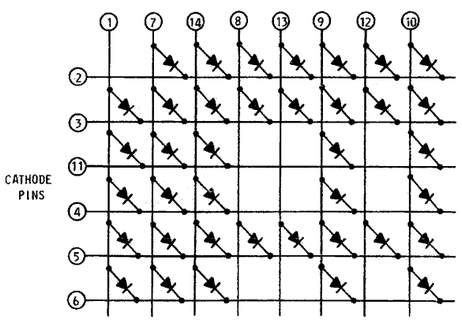
ANODE PINS



IC15, CP1

6 X 8

ANODE PINS



ISSUE 20

DATA TEST SET NO. 911NA

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BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U. S. A.

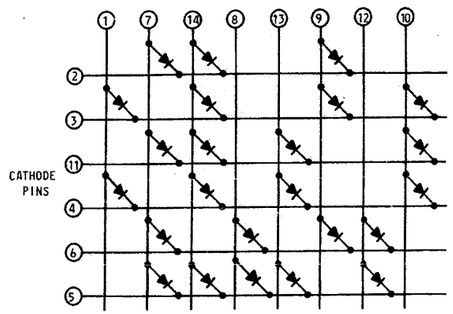
SD-73094-01-D12

E-7421 (10-71)

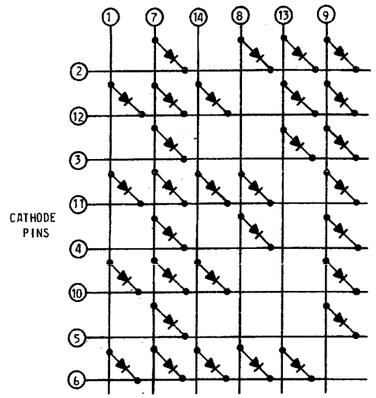
INFORMATION NOTES: (CONT)

302. (CONT)

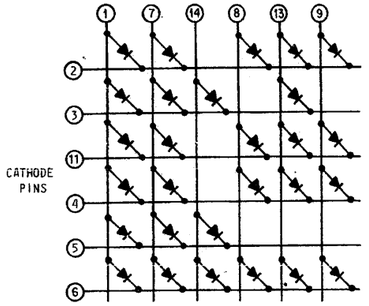
IC5, CP2
6 X 8
ANODE PINS



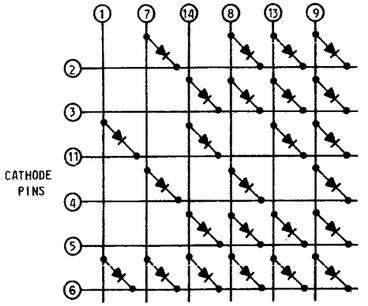
IC25, CP2
8 X 6
ANODE PINS



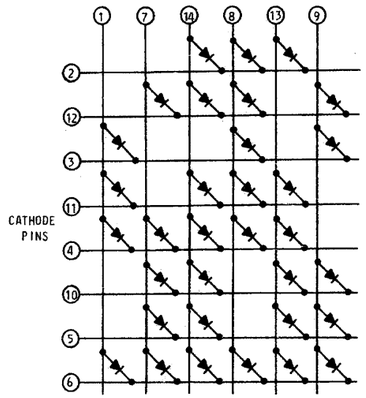
IC40, CP2
6 X 6
ANODE PINS



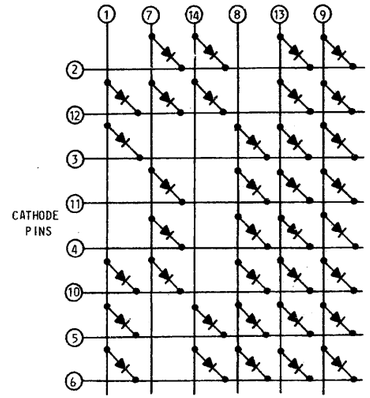
IC41, CP2
6 X 6
ANODE PINS



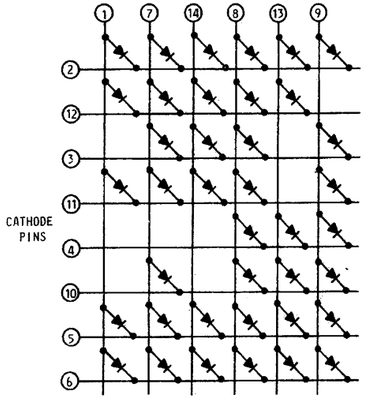
IC13, CP3
8 X 6
ANODE PINS



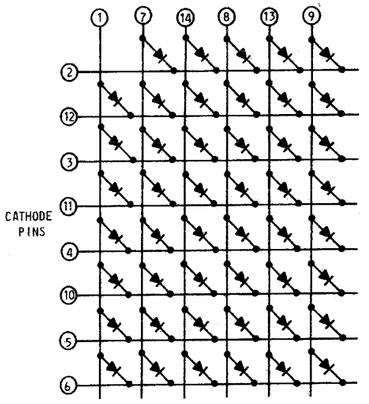
IC14, CP3
8 X 6
ANODE PINS



IC15, CP3
8 X 6
ANODE PINS



IC16, CP3
8 X 6
ANODE PINS



ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-D13

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-D13

INFORMATION NOTES: (CONT)

302. (CONT)

(Z) (CONT)

THE FUSIBLE LINKS LISTED IN THE TABLE HAVE BEEN OPENED BY TEXAS INSTRUMENTS CO. TO ACHIEVE THE DESIRED MATRICES.

CPS	DESIG	CODE	TERMINALS HORZ.	TERMINALS VERT.
1	IC15	DMA414	2	1
			11	8
			11	13
			11	12
			4	8
			4	13
			4	12
			6	8
			6	13
			6	12
	IC16	DMA416	2	1
			2	14
			3	7
			3	14
			4	1
			4	8
			5	7
			5	8
			6	1
			6	14
	IC17	DMA417	2	1
			2	14
			3	1
			3	14
			4	1
			4	14
			5	1
			5	14
			6	7
			6	14
	IC18	DMA418	2	7
			2	14
			3	1
			3	8
			4	7
			4	8
			5	1
			5	14
			6	7
			6	14
	IC19	DMA419	2	7
			2	14
			3	7
			3	14
			4	7
			4	14
			5	1
			5	8
			6	1
			6	8
	IC20	DMA403	2	1
			2	14
			2	13
			3	7
			3	14
			3	13
			11	1
			11	8
			11	13
			4	7
			4	14
			5	1
			5	14
			5	9

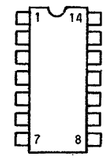
CPS	DESIG	CODE	TERMINALS HORZ.	TERMINALS VERT.
1	IC51	DMA413	2	9
			2	12
			3	1
			3	7
			3	14
			3	13
			3	12
			11	1
			11	7
			11	14
			11	8
			11	12
			4	1
			4	14
			4	9
			4	10
			5	14
			5	9
			5	10
			6	14
			6	9
			6	10
	IC34	DMA407	2	1
			12	1
			12	8
			3	1
			3	14
			3	8
			11	7
			11	8
			4	7
			4	8
			4	13
			10	7
			10	14
			10	8
			10	13
			5	1
			5	7
			5	14
			5	8
			5	13
			5	9
	IC35	DMA406	2	7
			2	14
			2	8
			12	1
			12	13
			12	9
			3	1
			3	7
			3	8
			3	9
			11	7
			11	13
			4	9
			4	1
			4	14
			10	8
			10	1
			5	7
			5	14
			5	8
			5	13
			5	9

CPS	DESIG	CODE	TERMINALS HORZ.	TERMINALS VERT.
2	IC5	DMA415	2	1
			2	8
			2	13
			2	12
			2	10
			3	7
			3	8
			3	13
			3	12
			11	1
			11	8
			11	9
			11	12
			4	7
			4	8
			4	9
			4	12
			5	1
			5	9
			5	10
			6	1
			6	14
			6	13
			6	10
	IC25	DMA408	2	1
			2	14
			12	8
			3	1
			3	14
			3	8
			11	13
			4	1
			4	14
			4	13
			10	8
			10	13
			5	1
			5	14
			5	8
			5	13
			6	9
	IC40	DMA404	2	14
			3	8
			3	9
			11	14
			4	14
			5	8
			5	13
			5	9
	IC41	DMA405	2	1
			2	14
			3	1
			11	7
			11	7
			4	8
			4	1
			4	14
			5	13
			5	1
			5	7

CPS	DESIG	CODE	TERMINALS HORZ.	TERMINALS VERT.
3	IC13	DMA409	2	1
			2	7
			2	9
			12	1
			12	13
			3	7
			3	14
			3	13
			11	7
			11	9
			4	9
			10	1
			10	8
			5	1
			5	8
	IC14	DMA410	2	1
			2	8
			12	8
			3	7
			3	14
			11	1
			11	14
			4	1
			4	14
			10	14
			5	7
			6	7
	IC15	DMA411	12	9
			3	1
			3	13
			11	13
			4	1
			4	7
			10	14
			10	1
				14
	IC16	DMA412	2	1

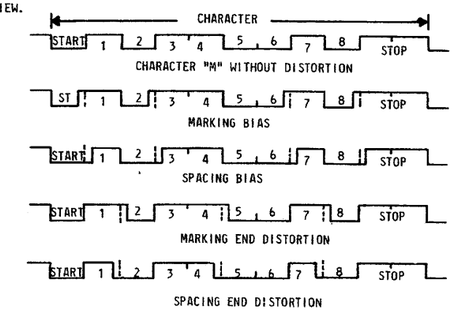
NOTES:

1. PIN NUMBERING, TOP VIEW.



INFORMATION NOTES: (CONT)

303. WAVEFORMS. TYPES OF DISTORTION.



ISSUE 2D

DATA TEST SET NO. 911NA

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

SD-73094-01-DI4

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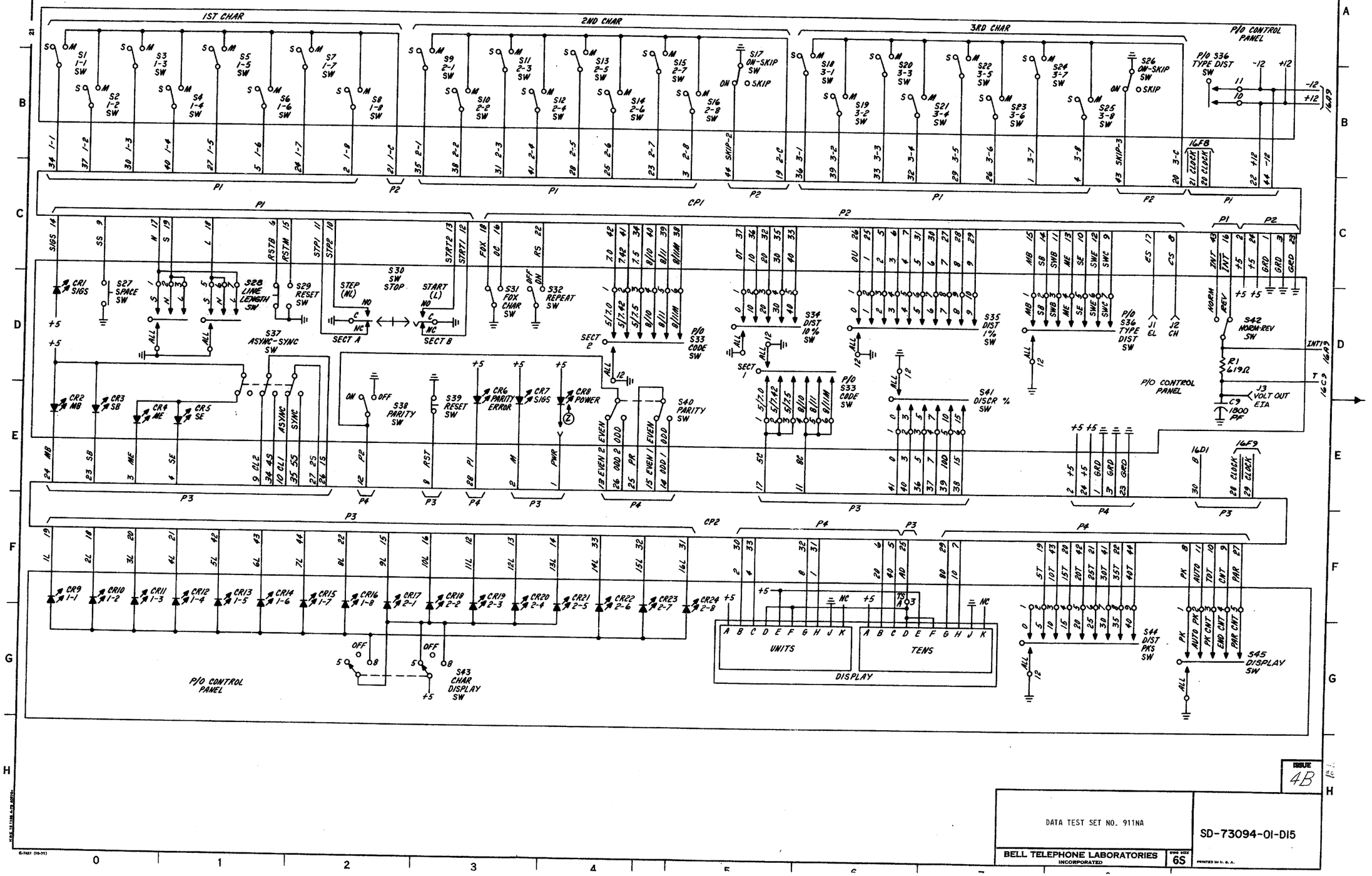
SD-73094-01-DI4

E-74321 (10-71)

INFORMATION NOTES: (CONT)

304.



SD-73094-01-D15

ISSUE 4B	
DATA TEST SET NO. 911NA	SD-73094-01-D15
BELL TELEPHONE LABORATORIES INCORPORATED	DWG SIZE 6S

INFORMATION NOTES: (CONT)

304. (CONT)

P7 P8 P5 CP3 P8P5 P6 P8 P5 P6

F7 CLOCK 25 CLOCK 24

1589 15D9 +12 -12 INIT 4 5 10

P7 1 2 11 12 3 4 13 14 5 6 15 16 7 8 9 10 18 19 20

15 -12 GND GND GND GND GND

P8 4 5 3 13 B2 A2 IN2 IN1

P5 11 3 12 2 10 1 9 8 19 20 6 21 4 15 16 5 18 17 7 EXT

CP3 P8P5 16 23 E1 EXT CLK

P6 7 1 HUB

CB 9 CM 8 CA 2 3 T D2 P D2

A1 24 B1 23 12

P8 8 1 20 21 14 C D E F R

P5 2 15 1 19 9 G H I K J

I 15D9

S46 FILTER SW IN OUT IN OUT

J4 VOLT INPUT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 ALL

S47 BAUDS SW

J5 EXT CLK

J6 VOLT OUT LVHUB

J7 T+ LP DRIVER

J8 T- LP DRIVER

J9 T+ CURRENT INPUT

J10 T- CURRENT INPUT

CR25 OVERLOAD CURRENT INPUT

HV HUB EIA HI EIA LO 4N 4R 10N 10R 20N 20R 60N 60R 11 12 TST

SECT 1 ALL +12

S48 INPUT SW

SECT 2 ALL

J11 GRD E19

TSB 4 TSA 4

P10 SECT1 10

P10 SECT2 10

P10 S33 CODE SW

P10 CONTROL PANEL

15E9

S49 POWER SW OFF ON TSB 1 TSB 2 TSA 1 TSA 2 TSA 3 TSB

R2 68.1KΩ DS1

POWER SUPPLY

F1

PWR CORD W B G TO 117V AC E1 GRD

CLOCK CLOCK CLOCK CLOCK CLOCK CLOCK

AB 15B9 15E9

CP4 P/O POWER SUPPLY

IC2 VOLTAGE REGULATOR -12 CASE BOLT

IC1 VOLTAGE REGULATOR +12

IC3 VOLTAGE REGULATOR +5

-12 R5 +12 +5

CR1 CR2G

E2 -V E5 C4 1000 E6

E1 3T1 E4 +V E3 C3 1000 E4

E3 5T1 E5 BQ

T1 3 4 5 1 2 6 7

Q1 E13 C2 5600 E14

E11 C1 800 E12

GRD

E15 C7 .1 E17 C8 .1 E18

E16 E20 +5

+12 E6 -12 E7 +5 E8 +5

C5 E8 E7 100 C6 E10 E9 100

ISSUE 4B

DATA TEST SET NO. 911NA

SD-73094-D16

BELL TELEPHONE LABORATORIES INCORPORATED

DRG SIZE 6S

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PART OF CPS 1
TEST SENTENCE GENERATOR

P10 P2 16 ← OC

J18/G7 D

R17 3010 +5

J10/D0

J10/D4 G

IC1 IC2 IC3 IC4A IC4B IC4C IC4D IC5A IC5B IC5C IC5D IC6 IC7 IC8D IC9A IC10A IC10B IC10C IC10D IC10E IC11 IC12 IC13 IC14A IC14B IC14C IC15 IC67A IC67B IC68A IC68B IC69B IC70C IC70E

C1 C2 C3 C4 C5 C6 C8 C9 C10 C11 C12 C13 C14 C20 C62 C63 C64 C65 .01

R1 R2 R3 R4 R5 R6 R7 R8 10KΩ

R9 2260

R10 R11 R95 R14 R15 R16 R18 3010

R12 R68 R91 18,200

R13 1620

R19 2210

R20 R21 R22 R23 R24 R25 R26 2260

RV1 RV2 RV3 RV4

Q1 Q2 Q3 Q4

CR1 CR28 CR29 CR30

CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25

P/O P1 5 19 L 18 N 17 RSTM 15 RSTB 6

J1D/D1 CK

J1D/F7 RSTM1

J1D/B9 AA

J1D/B4 C

J1C/A1 A

J1C/D3

J1D/82 F E

AA G1

P/O P1 1-1 2-1 3-1 1-2 2-2 3-2 1-3 2-3 3-3 1-4 2-4 3-4 1-5 2-5 3-5 1-6 2-6 3-6 1-7 2-7 3-7 1-8 2-8 3-8

-12 +5

ISSUE 2D

PART OF CPS 1

DATA TEST SET NO. 911NA

SD-73094-01-JIA

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-JIA

PART OF CPS 1

TEST SENTENCE GENERATOR

P/O P2

IC16 IC17 IC18 IC19 IC20

R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 10K Ω

+5

IC21B IC21C IC21A IC21D IC22D IC22C IC23C IC23B IC23D IC23A IC24B IC24A IC24C IC24D

C16 C17 C18 .01

J10/D8 M

IC28B IC28D IC28F IC28E IC27F IC27E IC27D

C22 .01

IC29 IC30 IC31

J J1C/F5

K J1D/C2

L J1D/D2

C39 C66 C67 560PF

C23 C24 .01

IC33

QC QB QA

IC32

CAR BOR UP DN CL

J1D/D8 N O

J1A/A4 J1C/D7 D

IC25 IC26

C69 560PF

C19 .01

J1C/E4 I

J1C/C3 H

PART OF CPS 1

ISSUE 4B

DATA TEST SET NO. 911NA

SD-73094-01-J1B

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-J1B

PART OF CPS I

TEST SENTENCE GENERATOR

P/O P2 — MB, SSB, SWB, MC, SF, SWC, SYNC

IC34, IC35

J1A/C8

IC26E, IC26A

R48 10KΩ, R49 10KΩ, R50 10KΩ

R51 5110, R52 2260, R53 5110, R54 2260

R55 10KΩ, R56 10KΩ, R57 10KΩ, R58 2260, R59 2260, R60 2260, R61 10KΩ, R62 10KΩ, R63 5110, R64 5110, R65 2260, R67 2260

C28 .01, C29 .01, C31 .01, C32 .01, C33 .01, C34 1000PF, C35 .01, C36 .01, C37 .01, C38 .01, C41 .01, C42 .01

IC36A, IC36B, IC37A, IC38A, IC38B, IC41A, IC41B, IC42A, IC46A, IC46B, IC46C, IC36C, IC37C, IC37D, IC50D, IC50C, IC66A, IC66B, IC66C, IC66D, IC43C, IC43D, IC8A, IC8E, IC40A, IC40B, IC40D, IC45A, IC45B, IC42B, IC47A, IC47B, IC8F, IC70A, IC70F

IC39B J FF 1 K, IC39A J FF 1 K, IC98 S FF 1, IC98A J FF 1 K, IC98B J FF 0 K

Q J10/C8

C15 3900PF

J1B/G7, D — J10/C8

P/O P1 — 43 INT

9 SS

16 INT

R70 2260

J1B/H6 I

J1D/D7 U

J1D/D7 T

J1D/B1 V

J1D/B8 S

J1B/B9, J10/C3 J

J1D/H1 W

J10/B3 R

J1D/E8 DX

J1D/D3 S1

R97 3010, R66 3010, C21 1000PF

P/O P2 — 8 CS

R69 221 — 14 SIGS

+5, +12, -12

SD-73094-01-JIC

PART OF CPS I

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-JIC

BELL TELEPHONE LABORATORIES INCORPORATED

6S

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PART OF CPS I

TEST SENTENCE GENERATOR

P/O P2 → 17 ES

P/O P1 → 20 CLOCK

P/O P2 → 20 3-C

P/O P2 → 19 2-C

P/O P2 → 21 1-C

PART OF CPS I

ISSUE 20

DATA TEST SET NO. 911NA

SD-73094-01-JID

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PRINTED IN U.S.A.

SD-73094-01-JID

PART OF CPS I
TEST SENTENCE GENERATOR

COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	KS-19774,L1,.01
C2	KS-19774,L1,.01
C3	KS-19774,L1,.01
C4	KS-19774,L1,.01
C5	KS-19774,L1,.01
C6	KS-19774,L1,.01
C7	KS-19774,L1,.01
C8	KS-19774,L1,.01
C9	KS-19774,L1,.01
C10	KS-19774,L1,.01
C11	KS-19774,L1,.01
C12	KS-19774,L1,.01
C13	KS-19774,L1,.01
C14	KS-19774,L1,.01
C15	KS-19774,L1, 3900PF
C16	KS-19774,L1,.01
C17	KS-19774,L1,.01
C18	KS-19774,L1,.01
C19	KS-19774,L1,.01
C20	KS-19774,L1,.01
C21	KS-19774,L1,1000PF
C22	KS-19774,L1,.01
C23	KS-19774,L1,.01
C24	KS-19774,L1,.01
C25	KS-20676,L1,560PF
C28	KS-19774,L1,.01
C29	KS-19774,L1,.01
C31	KS-19774,L1,.01
C32	KS-19774,L1,.01
C33	KS-19774,L1,.01
C34	KS-19774,L1,1000PF
C35	KS-19774,L1,.01
C36	KS-19774,L1,.01
C37	KS-19774,L1,.01
C38	KS-19774,L1,.01
C39	KS-20676,L1,560PF
C40	KS-19774,L1,.01
C41	KS-19774,L1,.01
C42	KS-19774,L1,.01
C43	602A
C44	KS-19774,L1,.01
C45	KS-19774,L1,.01
C46	KS-20736,L4,.01
C47	KS-19774,L1,.01
C48	KS-19774,L1,.01
C49	KS-19774,L1,.01
C50	KS-19774,L1,.01
C51	KS-19774,L1,.01
C52	KS-19774,L1,.01
C53	KS-19774,L9,1
C54	KS-19774,L1,.01
C55	KS-19774,L1,.01
C56	KS-19774,L1,1000PF
C57	KS-19774,L1,.01
C58	KS-19774,L1,.01
C59	KS-19774,L1,.01
C60	KS-19774,L1,.01
C61	KS-19774,L1,.01
C62	KS-19774,L1,.01
C63	KS-19774,L1,.01
C64	KS-19774,L1,.01
C65	KS-19774,L1,.01
C66	KS-20676,L1,560PF
C67	KS-20676,L1,560PF
C68	KS-20676,L1,220PF
C69	KS-20676,L1,560PF

CONNECTOR

DESIG	CODE
P1	AMP INC., PART NO.86479-1 & 86479-7
P2	AMP INC., PART NO.86479-1 & 86479-7

COMPONENT LIST (CONT)

DIODE

DESIG	CODE
CR1	458C
CR2-CR27	KS-16986,L2M1
CR28-CR30	458C

INDUCTOR

DESIG	CODE
L1	BP-2657, 2.4UH DELEVAN CORP, EAST AURORA, N.Y.

INTEGRATED CIRCUIT

DESIG	CODE
IC1	KS-20969,L9
IC2	KS-20969,L9
IC3	KS-21247,L1
IC4A-D	TEXAS INST,SN7403N
IC5A-D	TEXAS INST,SN7403N
IC6	TEXAS INST.,SN7496N
IC7	TEXAS INST.,SN7496N
IC8A-F	TEXAS INST.,SN7404N
IC9A,B	KS-20970,L1
IC10A-E	KS-20967,L7
IC11	KS-20968,L8
IC12	KS-20968,L8
IC13	KS-20968,L8
IC14B,C	KS-20967,L5
IC15	TEXAS INST.,DMA414
IC16	TEXAS INST.,DMA416
IC17	TEXAS INST.,DMA417 [SEE NOTE 302 (Z)]
IC18	TEXAS INST.,DMA418
IC19	TEXAS INST.,DMA419
IC20	TEXAS INST.,DMA403
IC21A-D	KS-20968,L9
IC22C,D	KS-20968,L9
IC23A-D	KS-20968,L9
IC24A-D	KS-20968,L9
IC25	KS-20968,L8
IC26A,B,D,E	KS-20968,L2
IC27C-F	KS-20968,L2
IC28A-F	KS-20968,L2
IC29	KS-20968,L8
IC30	KS-20968,L8
IC31	KS-20968,L8
IC32	KS-20969,L10
IC33	KS-20969,L10
IC34	TEXAS INST.,DMA407 [SEE NOTE 302 (Z)]
IC35	TEXAS INST.,DMA406
IC36A-C	KS-20967,L5
IC37A,C,D	KS-20968,L9
IC38A,B	KS-20967,L5
IC39A,B	KS-20970,L5
IC40A,B,D	KS-20968,L1
IC41A,B	TEXAS INST., SN74H22N
IC42A,B	KS-20968,L3
IC43C,D	KS-20968,L1
IC44B,C,D,F	KS-20967,L7
IC45	TEXAS INST., SN74H22N
IC46A-C	KS-20967,L5
IC47	41M
IC48A,B	KS-20970,L5
IC49A-D	KS-20968,L1
IC50C,D	KS-20968,L1
IC51	TEXAS INST., DMA413 [SEE NOTE 302 (Z)]
IC52A-D	KS-20968,L1

COMPONENT LIST (CONT)

INTEGRATED CIRCUIT (CONT)

DESIG	CODE
IC53A-D	TEXAS INST.,SN7403N
IC54A,B	KS-20970,L1
IC55A,B	KS-20970,L5
IC56A-D	KS-20968,L1
IC57C	KS-20968,L3
IC58A-C	KS-20967,L5
IC59	KS-20969,L9
IC60	KS-20969,L8
IC61	KS-20969,L8
IC62	KS-20969,L8
IC63A,B	KS-20970,L5
IC64B,C,D	KS-20968,L9
IC65A-C	KS-20968,L3
IC66A-D	KS-20968,L1
IC67A,B	KS-20970,L1
IC68A,B	KS-20970,L1
IC69B	TEXAS INST.,SN74H22N
IC70A,C,D,E,F	KS-20967,L7

RESISTOR

DESIG	CODE
R1	KS-20616,L1A,10KΩ
R2	KS-20616,L1A,10KΩ
R3	KS-20616,L1A,10KΩ
R4	KS-20616,L1A,10KΩ
R5	KS-20616,L1A,10KΩ
R6	KS-20616,L1A,10KΩ
R7	KS-20616,L1A,10KΩ
R8	KS-20616,L1A,10KΩ
R9	KS-20616,L1A,2260
R10	KS-20616,L1A,3010
R11	KS-20616,L1A,3010
R12	KS-20616,L1A,18,200
R13	KS-20616,L1A,1620
R14	KS-20616,L1A,3010
R15	KS-20616,L1A,3010
R16	KS-20616,L1A,3010
R17	KS-20616,L1A,3010
R18	KS-20616,L1A,3010
R19	KS-20616,L1A,2260
R20	KS-20616,L1A,2260
R21	KS-20616,L1A,2260
R22	KS-20616,L1A,2260
R23	KS-20616,L1A,2260
R24	KS-20616,L1A,2260
R25	KS-20616,L1A,2260
R26	KS-20616,L1A,2260
R27	KS-20616,L1A,10KΩ
R28	KS-20616,L1A,10KΩ
R29	KS-20616,L1A,10KΩ
R30	KS-20616,L1A,10KΩ
R31	KS-20616,L1A,10KΩ
R32	KS-20616,L1A,10KΩ
R33	KS-20616,L1A,10KΩ
R34	KS-20616,L1A,10KΩ
R35	KS-20616,L1A,10KΩ
R36	KS-20616,L1A,10KΩ
R37	KS-20616,L1A,10KΩ
R38	KS-20616,L1A,10KΩ
R39	KS-20616,L1A,10KΩ
R40	KS-20616,L1A,10KΩ
R41	KS-20616,L1A,2260
R42	KS-20616,L1A,2260
R43	KS-20616,L1A,2260
R44	KS-20616,L1A,2260
R45	KS-20616,L1A,2260
R46	KS-20616,L1A,2260
R47	KS-20616,L1A,2260
R48	KS-20616,L1A,10KΩ
R49	KS-20616,L1A,10KΩ
R50	KS-20616,L1A,10KΩ
R51	KS-20616,L1A,5110
R52	KS-20616,L1A,2260
R53	KS-20616,L1A,5110
R54	KS-20616,L1A,2260
R55	KS-20616,L1A,10KΩ
R56	KS-20616,L1A,10KΩ

COMPONENT LIST (CONT)

RESISTOR (CONT)

DESIG	CODE
R57	KS-20616,L1A,10KΩ
R58	KS-20616,L1A,2260
R59	KS-20616,L1A,2260
R60	KS-20616,L1A,2260
R61	KS-20616,L1A,10KΩ
R62	KS-20616,L1A,10KΩ
R63	KS-20616,L1A,5110
R64	KS-20616,L1A,5110
R65	KS-20616,L1A,2260
R66	KS-20616,L1A,3010
R67	KS-20616,L1A,2260
R68	KS-20616,L1A,18,200
R69	KS-20616,L1A,221
R70	KS-20616,L1A,2260
R71	KS-20616,L1A,3010
R72	KS-20616,L1A,10KΩ
R73	KS-20616,L1A,10KΩ
R74	KS-20616,L1A,10KΩ
R75	KS-20616,L1A,3010
R76	KS-20616,L1A,5110
R77	KS-20616,L1A,10KΩ
R78	KS-20616,L1A,10KΩ
R79	KS-20616,L1A,2260
R80	KS-20616,L1A,2260
R81	KS-20616,L1A,2260
R82	KS-20616,L1A,2260
R83	KS-20616,L1A,2260
R84	KS-20616,L1A,5110
R85	KS-20616,L1A,3010
R86	KS-20616,L1A,3010
R87	KS-20616,L1A,3010
R88	KS-20616,L1A,5110
R89	KS-20616,L1A,10KΩ
R90	KS-20616,L1A,10KΩ
R91	KS-20616,L1A,18,200
R92	KS-20616,L1A,2260
R93	KS-20616,L1A,2260
R94	KS-20616,L1A,18,200
R95	KS-20616,L1A,3010
R96	KS-20616,L1A,3010
R97	KS-20616,L1A,3010
R98	KS-20616,L1A,3010
R99	KS-20616,L1A,3010

TRANSISTOR

DESIG	CODE
Q1	51B
Q2	51B
Q3	51B
Q4	51B

VARISTOR

DESIG	CODE
RV1	100G
RV2	100G
RV3	100G
RV4	100G

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	CP 1

SYMBOL

SHOWN IN FS

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.

HIGHEST CAPACITOR USED ON THIS DRAWING
C68
NOT USED
C26,C27,C30

PART OF CPS I

ISSUE 4B

DATA TEST SET NO.911NA

SD-73094-01-JIE

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

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SD-73094-01-JIE

PART OF CPS 2

DISTORTION MEASURING SET

CLOCK P/O P3 28
CLOCK J2C/F2
J2D/G2 MSI
MS J2C/E3
CLOCK J2E/H8
CLOCK 29
B 30
J2C/D0 J2C/F1
J2E/F4 50
C3 1000PF
IC1B IC1A IC2A IC2B IC2C IC3C IC3D
MAT I IC5
0 41
3 40
7 37
15 38
100 39
8 36
J2B/F0 J2E/D7 J2B/C0 J2E/B7 J2B/C0 J2E/B7 J2B/C0 J2E/B7 J2E/A7 J2E/D7 J2E/C7
IC6A IC6C IC6F IC6B IC7C IC7F IC7A IC7B IC6F IC6E IC6B IC6E IC7B IC7E IC7D IC8D
R2 10KΩ R3 10KΩ R52 10KΩ R53 10KΩ R54 10KΩ R55 10KΩ R56 10KΩ R57 10KΩ
C7 C8 C9 C10
IC9 IC8D C11 220PF
J2E/D2 DOWN
J2B/D6 L
IC2C
C1 C2 C4 C5 C6 C12 C13 C15 C16 C17 C18
IC4 IC10A IC10B IC10C IC10D
R1 6980 470PF
J2B/F9 RST
IC11A IC11B IC12B IC12A IC13A IC13B IC13C IC14 IC15D IC16A IC16B IC15B IC15E IC18F IC18A IC16C IC15C
J2C/D8 A1
J2B/E5 RCB
J2B/E7 RSTI
T1-2 T3-4 1D 2D 3D 4D 1Q 2Q 3Q 4Q
R4 221 R5 3010 R6 8110 R7 221 R8 221 R9 221 R10 221
P/O P3 2 M 35 SS 34 4S 24 MB 23 SB 3 ME 4 SE
J2C/B6 B
C68 C19 L1 2.4MH
P/O P4 2 24 1 3 23
+5 GRD

PART OF CPS 2

DATA TEST SET NO. 911NA

SD-73094-01-J2A

BELL TELEPHONE LABORATORIES INCORPORATED

TYPE NO. 6S

PRINTED IN U. S. A.

ISSUE 2D

SD-73094-01-J2A

PART OF CPS 2

DISTORTION MEASURING SET

IC17D IC17A IC17B IC17C IC17E IC17F IC18 IC19 IC20D IC20B IC20C IC20A IC21D IC21C IC21A IC22D IC22C IC22B IC22A IC24B IC24C IC26 IC27 IC24E IC24D IC24A IC24F IC21B IC23B IC28A IC28B IC28C IC29A IC29C IC29D IC29F IC29E IC23A IC23C IC23D IC25 MAT 2

J2A/F0, J2E/D7
J2A/G0, J2E/D7
J2A/E0, J2E/D7
J2E/D7
J2C/E5 D1
J2C/E6 D
J2E/E7
J2E/F7
J2A/E0, J2E/E7
J2E/C8
J2C/B2
J2A/D4, J2C/C6
J2A/E7
J2A/G7, J2C/F0
J2C/E0
J2C/B0
J2A/F4
J2C/D6
J2C/B3
P/O P4
P/O P3

R11 5110
R12 5110
R13 10KΩ
R14 5110
R15 10KΩ
R16 10KΩ
R17 10KΩ
R18 10KΩ
R19 5110
R51 5110
RST1 25
RST2

C20 .01
C21 .01
C22 .01
C23 .01
C24 .01
C25 .01
C26 .01
C27 .01
C28 .01
C29 .01
C30 .01
C31 .01
CL9 2200PF

T3-4
T1-2

RST
RST

ISSUE 1

PART OF CPS 2

DATA TEST SET NO. 911NA

SD-73094-01-J2B

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U.S.A.

SD-73094-01-J2B

PART OF CPS 2
DISTORTION MEASURING SET

IC30 IC31 IC32 IC33C IC34B IC33D IC33B IC29B IC29A IC35B IC33A IC34A IC64A IC2D IC38C IC39B IC38A IC37B IC39A IC38B IC37F IC37A IC40 MAT 3 IC41 MAT 4 IC36C IC36F IC36B IC37D IC37E IC36A IC36E IC35A

J2B/F9 RST
J2B/E9 RST2
J2A/C1, J2D/C1 IS
J2B/E7, J2E/B3 25
J2B/E8 B
J2B/E9 N
J2B/D6 L
J2A/C2 Y
J2R/A0, CLOCK J2E/C2
J2D/C0 C4
J2B/A2 D
J2B/A3 M3
J2B/F6 M
J2B/F0 E
J2B/H6
J2B/B6
J2A/E6 A1
J2B/A2 D
P/O P4 P2 12
P2 24
P2 25
ODD2 26
EVEN2 13
P/O P4 29 30
CNT 9
PK 8
TOT 10
AUTO 11
PAR 27
P1 28
EVEN1 15
ODD1 14

C30 .01 C31 .01 C32 .01 C33 .01 C34 .01 C35 .01 C36 .01 C37 .01 C38 .01 C39 .01 C40 .022 C41 1000PF C42 .01 C43 .01 C64 .01 C70 .01 C72 470 PF

R20 5110 R21 5110 R22 10KΩ R23 3010 R24 5110 R25 10KΩ R26 5110 R27 5110 R28 5110 R29 5110 R30 221 R58 10KΩ R59 10KΩ R60 10KΩ R61 10KΩ R62 10KΩ R63 10KΩ R64 3010

PART OF CPS 2

DATA TEST SET NO. 911NA

BELL TELEPHONE LABORATORIES INCORPORATED

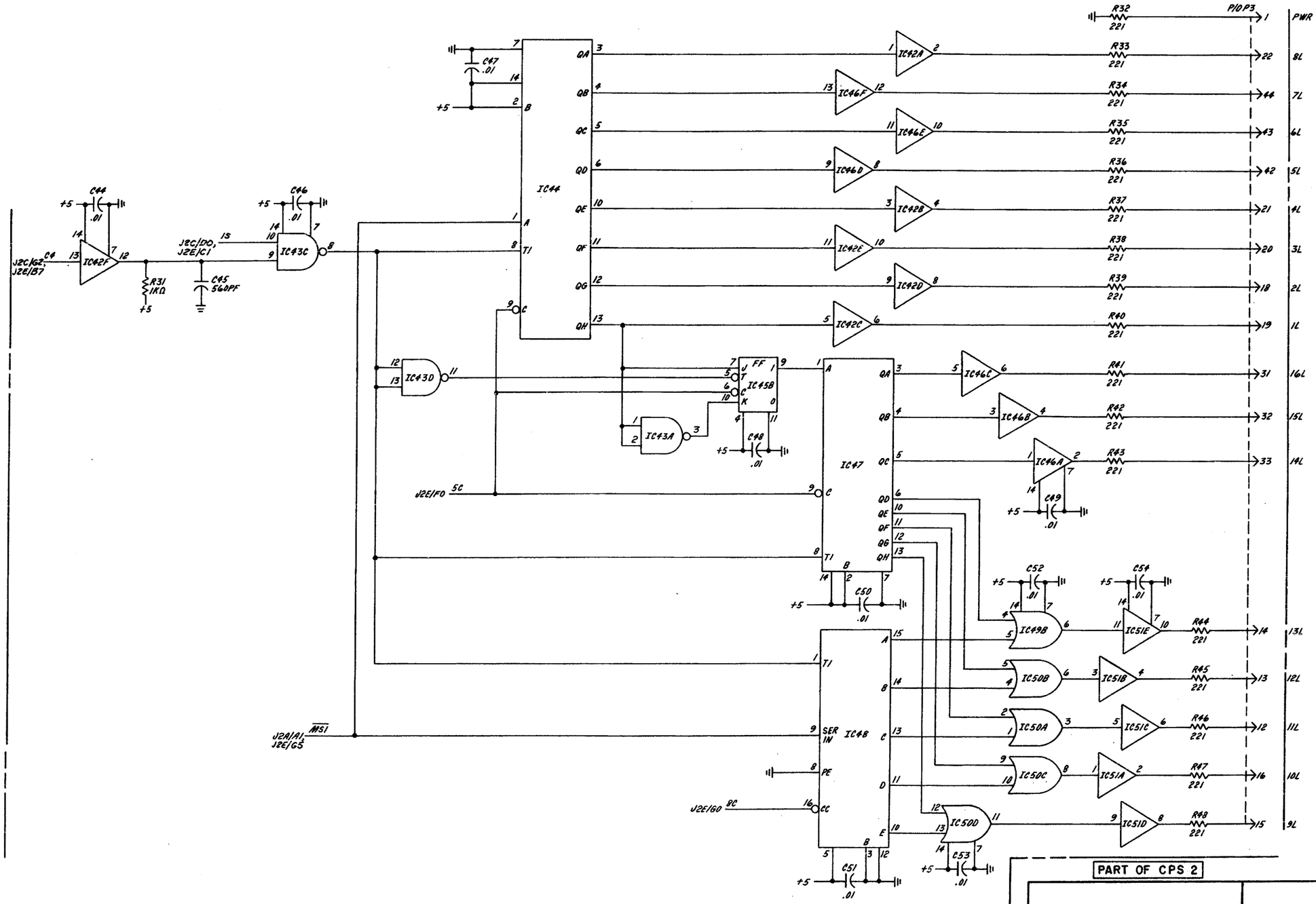
SD-73094-01-J2C

ISSUE 20

SD-73094-01-J2C

PART OF CPS 2

DISTORTION MEASURING SET



PART OF CPS 2

ISSUE 1

DATA TEST SET NO. 911NA

SD-73094-01-J2D

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-J2D

PART OF CPS 2

DISTORTION MEASURING SET

J2C/F2 CLOCK

J2D/C1

J2A/H3 DOWN

J2A/E3 UP

J2D/E3 5C

J2D/G5 8C

J2G/F0 26

J2A/C1 50

J2D/G2 MEI

J2A/B0 CLOCK

P/O P3

J2B/H0 J2A/F0 J2A/G0 J2A/F0 J2D/C0 J2A/H0 J2A/G0 J2A/H0 J2B/C0 J2B/E0 J2B/F0

P/O P3 CL2 CL1

IC57D IC57E IC57F IC57A IC57C IC57B IC58D IC58C IC58B IC58A IC52A IC53A IC52B IC52C IC53B IC56 IC37C IC62B IC61 U1 IC54 U2 IC55 B1 IC59 B2 IC60 IC63B

C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C71

R49 5110 R50 5110

220PF

PART OF CPS 2

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-J2E

BELL TELEPHONE LABORATORIES INCORPORATED

DWG SIZE 6S

PRINTED IN U. S. A.

SD-73094-01-J2E

PART OF CPS 2

DISTORTION MEASURING SET

COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	KS-19774,L1,.01
C2	KS-19774,L1,.01
C3	KS-19774,L1,1000PF
C4	KS-19774,L1,.01
C5	KS-19774,L1,.01
C6	KS-20676,L1,470PF
C7	KS-19774,L1,.01
C8	KS-19774,L1,.01
C9	KS-19774,L1,.01
C10	KS-19774,L1,.01
C11	KS-20676,L1,220PF
C12	KS-19774,L1,.01
C13	KS-19774,L1,.01
C14	KS-19774,L1,.01
C15	KS-19774,L1,.01
C16	KS-19774,L1,.01
C17	KS-19774,L1,.01
C18	KS-19774,L1,.01
C19	602A
C20	KS-19774,L1,.01
C21	KS-19774,L1,.01
C22	KS-19774,L1,.01
C23	KS-19774,L1,.01
C24	KS-19774,L1,.01
C25	KS-19774,L1,.01
C26	KS-19774,L1,.01
C27	KS-19774,L1,.01
C28	KS-19774,L1,.01
C29	KS-19774,L1,.01
C30	KS-19774,L1,.01
C31	KS-19774,L1,.01
C32	KS-19774,L1,.01
C33	KS-19774,L1,.01
C34	KS-19774,L1,.01
C35	KS-19774,L1,.01
C36	KS-19774,L1,.01
C37	KS-19774,L1,.01
C38	KS-19774,L1,.01
C39	KS-19774,L1,.01
C40	KS-19774,L5,.022
C41	KS-19774,L1,1000PF
C42	KS-19774,L1,.01
C43	KS-19774,L1,.01
C44	KS-19774,L1,.01
C45	KS-20676,L1,560PF
C46	KS-19774,L1,.01
C47	KS-19774,L1,.01
C48	KS-19774,L1,.01
C49	KS-19774,L1,.01
C50	KS-19774,L1,.01
C51	KS-19774,L1,.01
C52	KS-19774,L1,.01
C53	KS-19774,L1,.01
C54	KS-19774,L1,.01
C55	KS-19774,L1,.01
C56	KS-19774,L1,.01
C57	KS-19774,L1,.01
C58	KS-19774,L1,.01
C59	KS-19774,L1,.01
C60	KS-19774,L1,.01
C61	KS-19774,L1,.01
C62	KS-19774,L1,.01
C63	KS-19774,L1,.01
C64	KS-19774,L1,.01
C65	KS-19774,L1,.01
C66	KS-19774,L1,.01
C67	KS-20676,L1,220PF
C68	KS-20736,L4,.01
C69	KS-19774,L1,2200PF
C70	KS-19774,L1,.01
C71	KS-16958,L32,221PF
C72	KS-20676,L1,470PF

COMPONENT LIST (CONT)

CONNECTOR

DESIG	CODE
P3	AMP INC., PART NO. 86479-1 & 86479-7
P4	AMP INC., PART NO. 86479-1 & 86479-7

INDUCTOR

DESIG	CODE
L1	BP-2657, 2.4UH, DELEVAN CORP. EAST AURORA, N.Y.

INTEGRATED CIRCUIT

DESIG	CODE
IC1A,B	KS-20970,L1
IC2A-D	KS-20968,L6
IC3A-D	KS-20968,L1
IC4	KS-20969,L8
IC5	TEXAS INST., DMA415 [SEE NOTE 302(Z)]
IC6A-F	KS-20967,L6
IC7A-F	KS-20967,L6
IC8A-F	KS-20968,L2
IC9	KS-20968,L8
IC10A-D	KS-20968,L1
IC11A,B	KS-20968,L7
IC12A,B	KS-20968,L7
IC13A-C	KS-20968,L3
IC14	KS-20969,L23
IC15A-F	KS-20967,L8
IC16A,B	KS-20970,L1
IC17A-F	KS-20968,L2
IC18	KS-20969,L23
IC19	KS-20969,L23
IC20A-D	TEXAS INST., SN7403N
IC21A-D	KS-20968,L1
IC22A-D	TEXAS INST., SN7403N
IC23A-D	KS-20968,L1
IC24A-F	KS-20967,L8
IC25	TEXAS INST., DMA408 [SEE NOTE 302(Z)]
IC26	KS-20970,L6
IC27	KS-20970,L6
IC28A-C	KS-20968,L3
IC29A-F	KS-20967,L8
IC30	KS-20969,L10
IC31	KS-20969,L10
IC32	KS-20970,L2
IC33A-D	KS-20968,L1
IC34A,B	KS-20969,L1
IC35A,B	KS-20968,L7
IC36A-F	KS-20967,L6
IC37A-F	KS-20967,L6
IC38A-C	KS-20968,L3
IC39A,B	KS-20969,L1
IC40	TEXAS INST., DMA404 [SEE NOTE 302(Z)]
IC41	TEXAS INST., DMA405 [SEE NOTE 302(Z)]
IC42A-F	KS-20967,L8
IC43A,B,C,D	KS-20968,L1
IC44	KS-20969,L25
IC45B	KS-20970,L5
IC46A-F	KS-20967,L8
IC47	KS-20969,L25
IC48	TEXAS INST., SN7496N

COMPONENT LIST (CONT)

INTEGRATED CIRCUIT (CONT)

DESIG	CODE
IC49B	KS-20967,L11
IC50A-D	KS-20967,L11
IC51A-E	KS-20967,L8
IC52A-C	KS-20968,L3
IC53A,B	KS-20970,L5
IC54	KS-20969,L10
IC55	KS-20969,L10
IC56	KS-20970,L2
IC57A-F	KS-20968,L2
IC58A-D	KS-20968,L1
IC59	KS-20968,L8
IC60	KS-20968,L8
IC61	KS-20969,L9
IC62B	KS-20968,L1
IC63B	KS-20969,L1
IC64A	TEXAS INST.,SN7403N

RESISTOR

DESIG	CODE
R1	KS-20616,L1A,6980
R2	KS-20616,L1A,10KΩ
R3	KS-20616,L1A,10KΩ
R4	KS-20616,L1A,221
R5	KS-20616,L1A,3010
R6	KS-20616,L1A,5110
R7	KS-20616,L1A,221
R8	KS-20616,L1A,221
R9	KS-20616,L1A,221
R10	KS-20616,L1A,221
R11	KS-20616,L1A,5110
R12	KS-20616,L1A,5110
R13	KS-20616,L1A,10KΩ
R14	KS-20616,L1A,5110
R15	KS-20616,L1A,10KΩ
R16	KS-20616,L1A,10KΩ
R17	KS-20616,L1A,10KΩ
R18	KS-20616,L1A,10KΩ
R19	KS-20616,L1A,5110
R20	KS-20616,L1A,5110
R21	KS-20616,L1A,5110
R22	KS-20616,L1A,10KΩ
R23	KS-20616,L1A,3010
R24	KS-20616,L1A,5110
R25	KS-20616,L1A,10KΩ
R26	KS-20616,L1A,5110
R27	KS-20616,L1A,5110
R28	KS-20616,L1A,5110
R29	KS-20616,L1A,5110
R30	KS-20616,L1A,221
R31	KS-20616,L1A,1KΩ
R32	KS-20616,L1A,221
R33	KS-20616,L1A,221
R34	KS-20616,L1A,221
R35	KS-20616,L1A,221
R36	KS-20616,L1A,221
R37	KS-20616,L1A,221
R38	KS-20616,L1A,221
R39	KS-20616,L1A,221
R40	KS-20616,L1A,221
R41	KS-20616,L1A,221
R42	KS-20616,L1A,221
R43	KS-20616,L1A,221
R44	KS-20616,L1A,221
R45	KS-20616,L1A,221
R46	KS-20616,L1A,221
R47	KS-20616,L1A,221
R48	KS-20616,L1A,221
R49	KS-20616,L1A,5110
R50	KS-20616,L1A,5110
R51	KS-20616,L1A,5110
R52	KS-20616,L1A,10KΩ
R53	KS-20616,L1A,10KΩ
R54	KS-20616,L1A,10KΩ
R55	KS-20616,L1A,10KΩ
R56	KS-20616,L1A,10KΩ
R57	KS-20616,L1A,10KΩ
R58	KS-20616,L1A,10KΩ
R59	KS-20616,L1A,10KΩ

COMPONENT LIST (CONT)

RESISTOR (CONT)

DESIG	CODE
R60	KS-20616,L1A,10KΩ
R61	KS-20616,L1A,10KΩ
R62	KS-20616,L1A,10KΩ
R63	KS-20616,L1A,10KΩ
R64	KS-20616,L1A,3010

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	CP 2

SYMBOL

SHOWN IN FS

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. CONNECT PINS OF UNUSED INTEGRATED CIRCUITS AS SHOWN IN THE TABLE.

IC'S	PINS	CONNECT TO
15	2	GROUND
49	1,2,9,10,12,13	+5V
51	13	GROUND
62	1,2,9,10,12,13	GROUND
63	1	GROUND

CIRCUIT DESCRIPTION

INPUT/OUTPUT INFORMATION

PART OF CPS 2

ISSUE 2D

DATA TEST SET NO.911NA

SD-73094-01-J2F

BELL TELEPHONE LABORATORIES INCORPORATED

SYS SIZE 6S

PRINTED IN U.S.A.

SD-73094-01-J2F

PART OF CPS 3

CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS

P7
14
16
13
17
NC
+12 4 +12
-12 3 -12
15 NC
1 +5
2
11
12
+5
5
6
7
8
9
10
18
19
20
GRD
L2 2.4μH
L1 2.4μH
C27 .01
+5
+B Y2 OSC OUT
CASE, B-
C5 .01
IC4B
R25 3010
P/O P5 4 13B
IC5A
IC6F
C9 .01
R26 3010
6 D 11B
IC5C
IC6D
+B Y3 OSC OUT
CASE, B-
IC4C
R27 3010
R28 3010
L3 2.4μH
+5
C28 .01
C29 40
IC8A
IC9D
IC11B
R24 3010
R80 3010
C11 .01
C12 .01
C13 .01
NC 13
IC5E
IC6B
IC8B
IC10
IC9C
IC5F
F NC 14
IC5D
IC6C
R82 3010
C10 .01
IC11A
IC9A
IC9B
TP3
Y1 OSC RF
IC7A
Q1
CR2
IC8C
IC12
C7 .01
R83 3010
C8 .01
IC7B
R84 2710
R86 1K Ω
C6 .01
R85 5620
TP1
P/O P5 7 EXT
23 EXT CLK
24 CLOCK
25 CLOCK
VC J3B/C3
IC13
R12 10KΩ
R13 10KΩ
R14 10KΩ
R15 10KΩ
R16 10KΩ
R17 10KΩ
R18 10KΩ
R19 10KΩ
R20 10KΩ
IC14
R21 10KΩ
R22 10KΩ
R23 10KΩ
IC15
IC16
IC17
IC18
IC19
BOR
C14 .01
C23 .01
C24 .01
P/O P5
11 1B
3 2B
12 3B
2 4B
10 5B
1 6B
9 7B
8 8B
19 9B
20 10B
NC 18 17B
21 12B
NC 17 18B
22 NC
NC 15 14B
NC 16 15B
NC 5 16B

SD-73094-01-J3A

PART OF CPS 3

ISSUE 3A

DATA TEST SET NO. 911NA

SD-73094-01-J3A

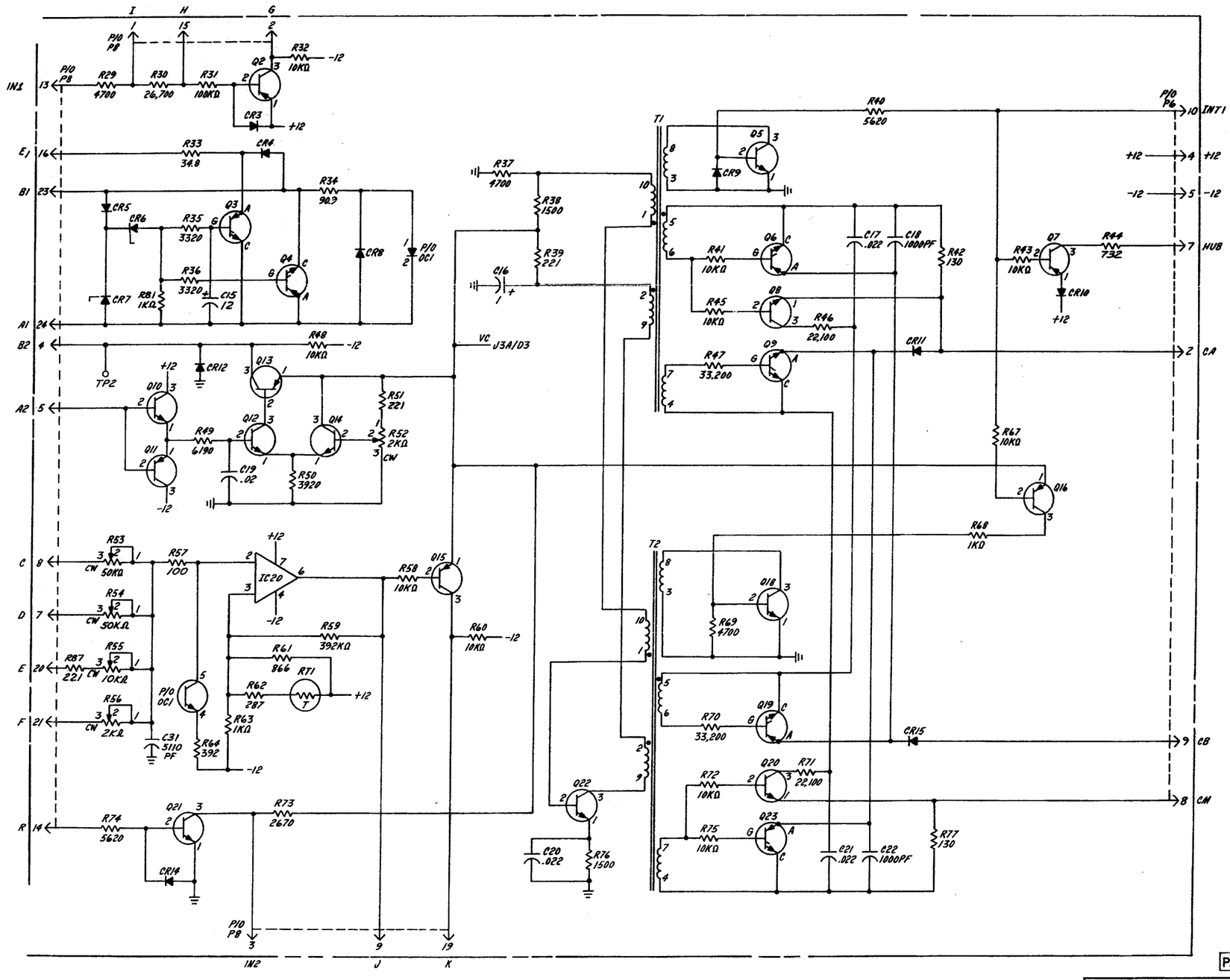
BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U. S. A.

PART OF CPS 3

CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS



PART OF CPS 3

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-J3B

BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

PRINTED IN U.S.A.

SD-73094-01-J3B

PART OF CPS 3

CLOCK, INPUT, OUTPUT AND FILTER CIRCUITS

COMPONENT LIST

CAPACITOR

DESIG	CODE
C5	KS-19774,L1,.01
C6	KS-19774,L1,.01
C7	KS-19774,L1,.01
C8	KS-19774,L1,.01
C9	KS-19774,L1,.01
C10	KS-19774,L1,.01
C11	KS-19774,L1,.01
C12	KS-19774,L1,.01
C13	KS-19774,L1,.01
C14	KS-19774,L1,.01
C15	KS-16390,L14,12
C16	600A
C17	KS-19774,L5,.022
C18	KS-16742,L34,1000PF
C19	570CK,.02
C20	KS-19774,L5,.022
C21	KS-19774,L5,.022
C22	KS-16742,L34,1000PF
C23	KS-19774,L1,.01
C24	KS-19774,L1,.01
C27	KS-20736,L4,.01
C28	KS-20736,L4,.01
C29	602A
C31	KS-16742, L34,5110PF

CONNECTOR

DESIG	CODE
P7	AMP INC., PART NO. 86479-1
P5	AMP INC., PART NO. 86479-2 & 86479-4
P8	AMP INC., PART NO. 86479-7
P6	AMP INC., PART NO. 86479-4

DIODE

DESIG	CODE
CR2	458C
CR3	458C
CR4	426J
CR5	446F
CR6	459E
CR7	426P
CR8	446F
CR9	458A
CR10	448B
CR11	426A
CR12	458C
CR14	458C
CR15	426A

INDUCTOR

DESIG	CODE
L1, L2, L3	BP-2657, 2.4UH, DELEVAN CORP., EAST AURORA, N.Y.

INTEGRATED CIRCUIT

DESIG	CODE
IC4B,C	KS-20968,L9
IC5A,C,D,E,F	KS-20968,L2
IC6B,C,D,F	KS-20967,L6
IC7A,B	TEXAS INST.,SN7473N
IC8A-C	KS-20967,L4

COMPONENT LIST (CONT)

INTEGRATED CIRCUIT (CONT)

DESIG	CODE
IC9A-D	KS-20968,L1
IC10	KS-20968,L8
IC11A,B	TEXAS INST.,SN7473N
IC12	TEXAS INST.,SN7490AN
IC13	TEXAS INST,DMA409 [SEE NOTE 302(Z)]
IC14	TEXAS INST,DMA410 [SEE NOTE 302(Z)]
IC15	TEXAS INST,DMA411 [SEE NOTE 302(Z)]
IC16	TEXAS INST,DMA412 [SEE NOTE 302(Z)]
IC17	KS-20969,L10
IC18	KS-20969,L10
IC19	KS-20969,L10
IC20	FAIRCHILD,741TC

OSCILLATOR

DESIG	CODE
Y1	MICROSONICS,K1087A-1T18,9.600 MHZ
Y2	VECTRON LAB. INC.,231-2405,180.000KHZ
Y3	VECTRON LAB. INC.,231-2405,105.000KHZ

OPTICAL COUPLER

DESIG	CODE
OC1	TEXAS INST, TIL111

POTENTIOMETER

DESIG	CODE
R52	KS-19093,L1A,2KΩ
R53	KS-19093,L1A,50KΩ
R54	KS-19093,L1A,50KΩ
R55	KS-19093,L1A,10KΩ
R56	KS-19093, L1A, 2KΩ

RESISTOR

DESIG	CODE
R12	KS-20616,L1A,10KΩ
R13	KS-20616,L1A,10KΩ
R14	KS-20616,L1A,10KΩ
R15	KS-20616,L1A,10KΩ
R16	KS-20616,L1A,10KΩ
R17	KS-20616,L1A,10KΩ
R18	KS-20616,L1A,10KΩ
R19	KS-20616,L1A,10KΩ
R20	KS-20616,L1A,10KΩ
R21	KS-20616,L1A,10KΩ
R22	KS-20616,L1A,10KΩ
R23	KS-20616,L1A,10KΩ
R24	KS-20616,L1A,3010
R25	KS-20616,L1A,3010
R26	KS-20616,L1A,3010
R27	KS-20616,L1A,3010
R28	KS-20616,L1A,3010

COMPONENT LIST (CONT)

RESISTOR (CONT)

DESIG	CODE
R29	KS-20616,L1A,4700
R30	KS-20616,L1A,26,700
R31	KS-20616,L1A,100KΩ
R32	KS-20616,L1A,10KΩ
R33	KS-20616,L1A,34.8
R34	KS-20616,L1A,90.9
R35	KS-20616,L1A,3320
R36	KS-20616,L1A,3320
R37	KS-20616,L1A,4700
R38	KS-20616,L1A,1500
R39	KS-20616,L1A,221
R40	KS-20616,L1A,5620
R41	KS-20616,L1A,10KΩ
R42	KS-14603,L1C,130
R43	KS-20616,L1A,10KΩ
R44	KS-20810,L1A,732
R45	KS-20616,L1A,10KΩ
R46	KS-20616,L1A,22,100
R47	KS-20616,L1A,33,200
R48	KS-20810,L1A,10KΩ
R49	KS-20810,L1A,6190
R50	KS-20810,L1A,3920
R51	KS-20810,L1A,221
R57	KS-20616,L1A,100
R58	KS-20616,L1A,10KΩ
R59	KS-20616,L1A,392KΩ
R60	KS-20616,L1A,10KΩ
R61	KS-20616,L1A,866
R62	KS-20616,L1A,287
R63	KS-20616,L1A,1KΩ
R64	KS-20616,L1A,392
R67	KS-20616,L1A,10KΩ
R68	KS-20616,L1A,1KΩ
R69	KS-20616,L1A,4700
R70	KS-20616,L1A,33,200
R71	KS-20616,L1A,22,100
R72	KS-20616,L1A,10KΩ
R73	KS-20616,L1A,2670
R74	KS-20616,L1A,5620
R75	KS-20616,L1A,10KΩ
R76	KS-20616,L1A,1500
R77	KS-14603,L1C,130
R80	KS-20616,L1A,3010
R81	KS-20616,L1A,1KΩ
R82	KS-20616,L1A,3010
R83	KS-20616,L1A,3010
R84	KS-20616,L1A,2710
R85	KS-20616,L1A,5620
R86	KS-20616,L1A,1KΩ
R87	KS-20616,L1A,221

TERMINAL

DESIG	CODE
TP1-TP3	MALCO MFR CORP,13009-13

THERMISTOR

DESIG	CODE
RT1	17A

TRANSFORMER

DESIG	CODE
T1	2560D
T2	2560D

COMPONENT LIST (CONT)

TRANSISTOR

DESIG	CODE
Q1	66J
Q2	51A
Q3	TEXAS INST,2N6336
Q4	TEXAS INST,2N6336
Q5	66J
Q6	27B
Q7	51A
Q8	RCA,2N3440
Q9	27B
Q10	66J
Q11	51B
Q12	66J
Q13	51B
Q14	66J
Q15	51A
Q16	51A
Q18	66J
Q19	27B
Q20	RCA,2N3440
Q21	66J
Q22	66G
Q23	27B

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	CP 3

SYMBOL

SHOWN IN FS

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS; CAPACITANCE VALUES ARE IN MICROFARADS; VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. CONNECT PINS OF UNUSED INTEGRATED CIRCUITS AS SHOWN IN THE TABLE.

IC'S	PINS	CONNECT TO
4	1,2	GRD
5	3	GRD
6	11	GRD

HIGHEST CAPACITOR, DIODE, INTEGRATED CKT, RESISTOR AND TRANSISTOR USED ON THIS DRAWING

C31	CR15	IC20	R87	Q23
NOT USED				
C1-C4, C25,C26, C30	CR1	IC1-IC3	R1-R11, R65,R66, R78,R79	Q17

PART OF CPS 3

ISSUE 3A

DATA TEST SET NO. 911NA

SD-73094-01-J3C

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SD-73094-01-J3C

E-74831 (10-71)

CPS 4
PART OF POWER SUPPLY

COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	KS-19774,L5, .1
C2	KS-19774,L1, 1000PF
C3	KS-19774,L5, .1
C4	KS-19774,L5, .1

DIODE

DESIG	CODE
CR1	MOTOROLA, MDA 920A-2

INDUCTOR

DESIG	CODE
L1	BP-2657, 2.4UH, DELEVAN CORP., EAST AURORA, N.Y.

INTEGRATED CIRCUIT

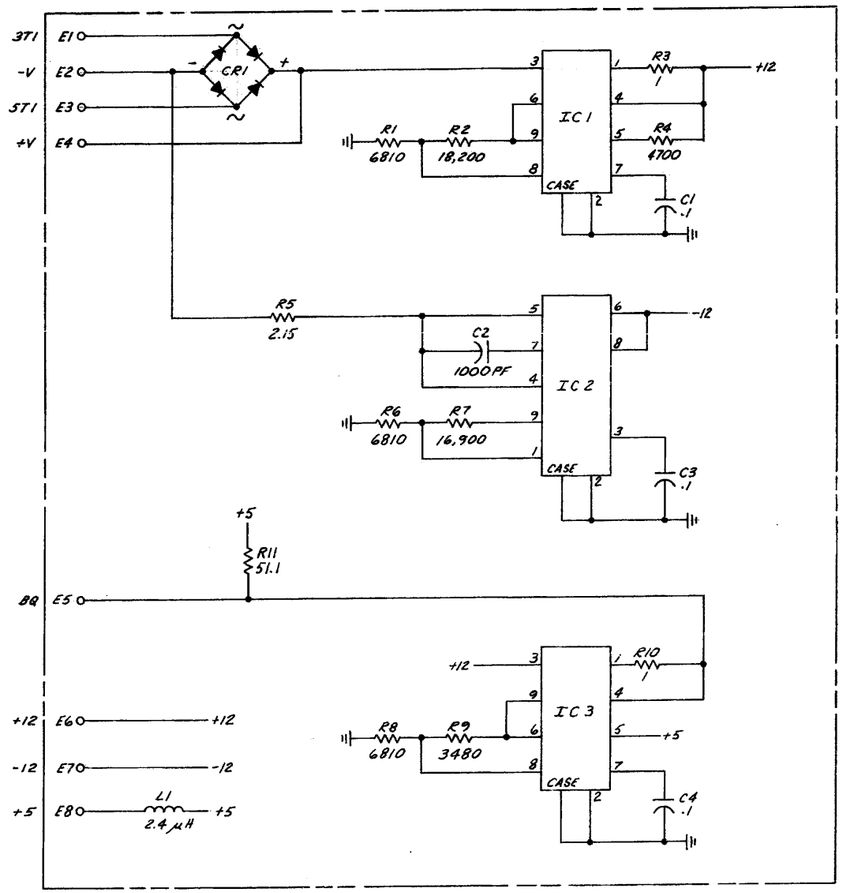
DESIG	CODE
IC1	MOTOROLA, MC1460R
IC2	MOTOROLA, MC1465R
IC3	MOTOROLA, MC1460R

RESISTOR

DESIG	CODE
R1	KS-20616,L1A, 6810
R2	KS-20616,L1A, 18,200
R3	KS-14603,L1A, 1
R4	KS-20616,L1A, 4700
R5	KS-14603,L1A, 2.15
R6	KS-20616,L1A, 6810
R7	KS-20616,L1A, 16,900
R8	KS-20616,L1A, 6810
R9	KS-20616,L1A, 3480
R10	KS-20810,L1A, 1
R11	KS-20810,L1A, 51.1

TERMINAL

DESIG	CODE
E1-E8	MALCO MFG. CORP. 13009-13



MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	CP4

SYMBOL

SHOWN IN FS

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.

CPS 4

ISSUE 2D

DATA TEST SET NO. 911NA

SD-73094-01-J4

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SD-73094-01-J4

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	DRAWN	APPD
1	1	10-31-74	JRA AEZ	PE RCM RTR

SHEET INDEX

CONTENTS	SHEET NO.
SHEET INDEX CIRCUIT NOTES EQUIPMENT NOTES INFORMATION NOTES	1
FS 1 APP FIG. 1	2

CIRCUIT NOTES:

101.

102.

FEATURE OR OPTION	PROVIDE								
	APP FIG.	APP OR WRG	QUANTITY-FACTORY FURNISHED OPTIONS						
			CODE						
			911P						
COMMON EQUIPMENT	1		1						

CIRCUIT NOTES: (CONT)

103.

RECORD OF CHANGES							
CHANGED ON ISS	IF MARKINGS ON SET SPECIFY		SEE NOTE	USE			
	CODE	SERIES		STD	A&M	MD	

SUPPORTING INFORMATION

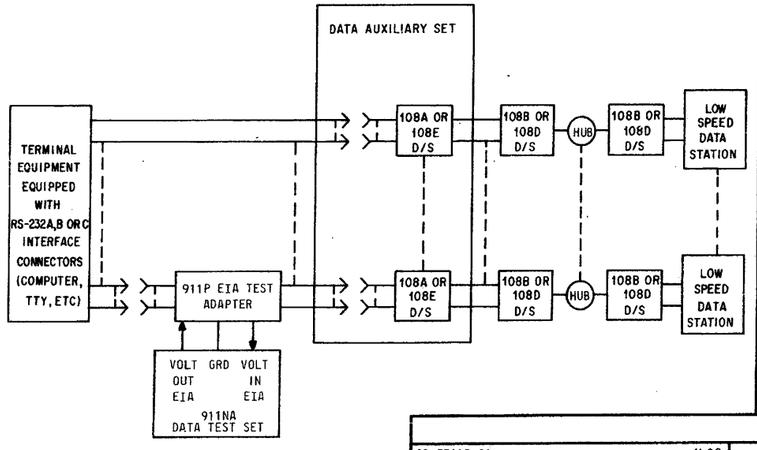
CATEGORY	NO.
EQUIPMENT DRAWING	J79911P
EQUIPMENT DESIGN REQT	J79911

EQUIPMENT NOTES:

201.

INFORMATION NOTES:

301. TYPICAL ARRANGEMENT OF THE 911P EIA TEST ADAPTER.

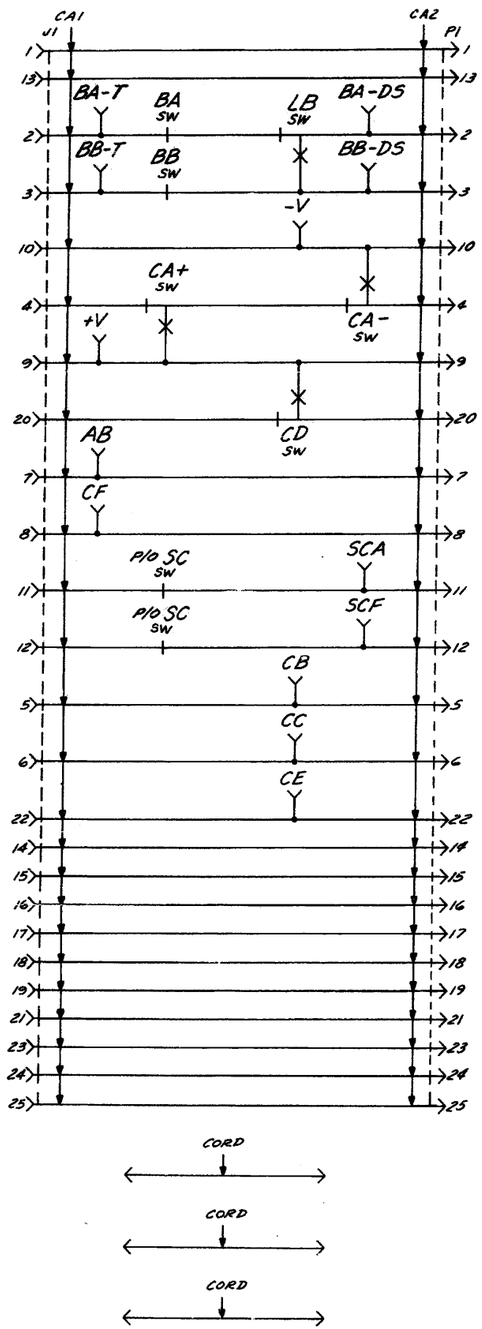


SD-73112-01-1

SD-73112-01 1L02	AT&TCO STANDARD
DATA SYSTEMS STATION EIA TEST ADAPTER NO. 911P FOR USE WITH RS-232A, B OR C INTERFACE CONNECTORS (2)	SD-73112-01-1 2 SHEETS
BELL TELEPHONE LABORATORIES INCORPORATED — DWG SIZE 6S — PRINTED IN U.S.A.	

/

FS 1
EIA TEST ADAPTER



APP FIG. 1

CORD

DESIG	LOC	CODE
[3] —	2G1,2H1	P1N

JACK

DESIG	LOC	CODE
BA-T	2A0	KS-14523,L6
BA-DS	2A1	KS-14523,L7
BB-T	2B0	KS-14523,L6
BB-DS	2B1	KS-14523,L7
-V	2B1	KS-14523,L5
+V	2C0	KS-14523,L2
AB	2C0	KS-14523,L3
CF	2D0	KS-14523,L4
SCA	2D1	KS-14523,L1
SCF	2D1	KS-14523,L1
CB	2D1	KS-14523,L4
CC	2E1	KS-14523,L4
CE	2E1	KS-14523,L4

CORD

DESIG	LOC	CODE
CA1, CA2	2A0,2A1	M25A (MODIFIED)

E/W CONNECTOR

DESIG	LOC	CODE
P1	2A2	KS-19088,L2, E/W KS-19196,L2 HOOD
J1	2A0	KS-19087,L2, E/W KS-19196,L2 HOOD

SWITCH

DESIG	LOC	CODE
BA	2A0	KS-19963,L1
BB	2B0	KS-19963,L1
CA+	2B0	KS-19963,L1
CA-	2C1	KS-19963,L1
CD	2C1	KS-19963,L1
LB	2A1	KS-19963,L1
SC	2D0	KS-19963,L6

ISSUE 1

EIA TEST ADAPTER NO. 911P

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