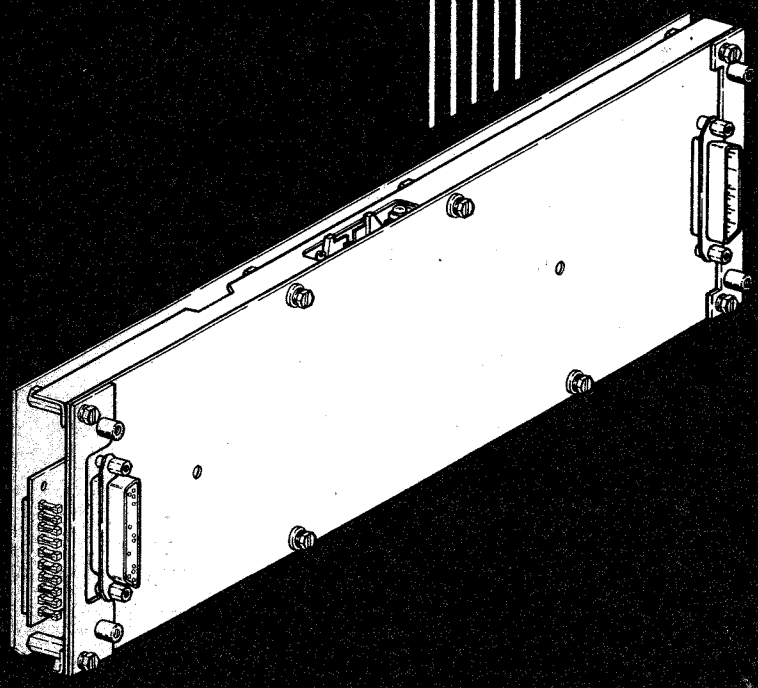
AT&T
Teletype Corporation

REPAIR MANUAL 534

for
INTERFACES
CONTROLLERS
and
MODIFICATION KIT
CIRCUIT CARDS



Associated With

42/43 TERMINALS

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Department 3221
Information: 312/982-2538
TLX 25-4051
TWX 901/223-3611

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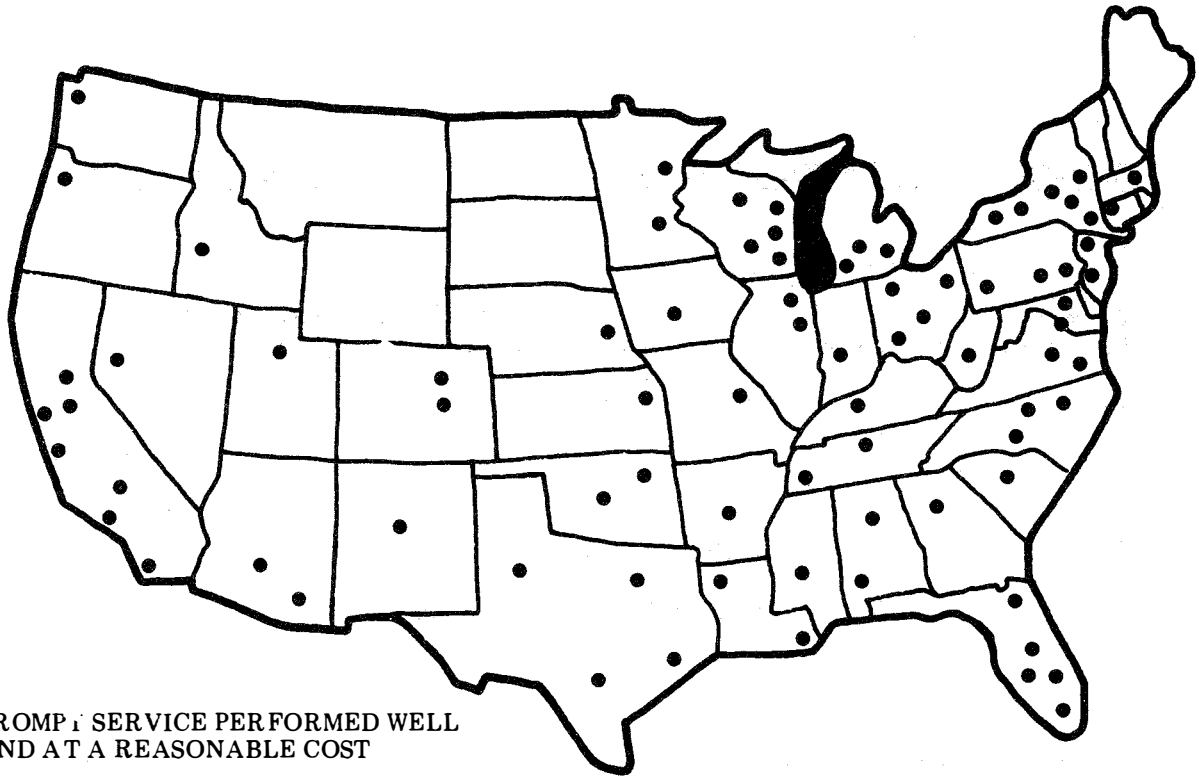

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INTERFACES, CONTROLLERS, AND MODIFICATION KIT

CIRCUIT CARDS ASSOCIATED WITH 42/43 TERMINALS

REPAIR MANUAL

INTRODUCTION

This manual provides repair information for the interfaces, controllers and modification kit circuit cards associated with 42/43 Terminals and includes the answer-back and selective calling modification kits and brief repair of nonpedestal controllers.

This manual is intended for field or shop use and is arranged into various parts that include troubleshooting, circuit descriptions and diagrams, parts and packing and marking. Testing is not included in this manual, therefore interfaces, modification kits and controllers should be tested in an operating teleprinter using the appropriate service manual. Parts information and circuit diagrams only are included for the 410746 SSI interface card and 420301 Telex interface.

Waveforms are included on circuit diagrams and charts are provided for additional trouble isolation using an oscilloscope or volt-ohmmeter. No specially designed tools or shop facilities are required for repair operations.

The circuit diagrams in Manual 385, provides circuit information extracted from this manual. The component layouts, lead designations and circuit diagrams for each circuit are combined into single foldout sheets for the convenience of field or shop personnel when repairing these components.

The components covered in this issue are as follows:

INTERFACES

410382 — Dual EIA/Neutral Interface Circuit Card
410746 — SSI Interface Circuit Card
410754 — Terminal Auxiliary Unit — TAU2
410755 — Terminal Auxiliary Unit — TAU1
420301 — Telex Interface

CONTROLLERS

410231 — 5 Level, SCCAT
410232 — 8 Level, SCCAT
410241 — 5 Level W/4K Buffer, SCCAT
411901 — Controller Without Applications Program Card
411902 — Buffered 43 SR
411904 — Buffered 42 SR
411905 — Buffered 43 SC
411906 — Buffered 42 SC
411907 — Buffered 42 SR INTF W/EF*
411908 — Buffered 42 SC W/USP*
411909 — Buffered 43 SC EC
411910 — Buffered 43 SR W/ER

MODIFICATION KITS

430899 — APL Alternate Font Modification Kit
430900 — Answer-Back Modification Kit
430910 — Selective Calling Modification Kit
430920 — Weather Font Modification Kit
430969 — Weather Font Modification Kit
454668 — Electronic Top of Form Modification Kit

*SR — Send Receive
INTF — International Font
W/EF — With Enhanced Features
SCCAT — Single Card Controller
SC — Selective Calling
W/USP — With Unshift On Space
EC — Enhanced Contention
ER — Enhanced Retrieve

Spare parts for repair are available from Teletype Corporation. Service personnel should be properly trained and have access to the spares before attempting repair of these units.

REPAIR MANUAL FOR INTERFACES, CONTROLLERS AND MODIFICATION KIT CIRCUIT CARDS ASSOCIATED WITH 42/43 TERMINALS

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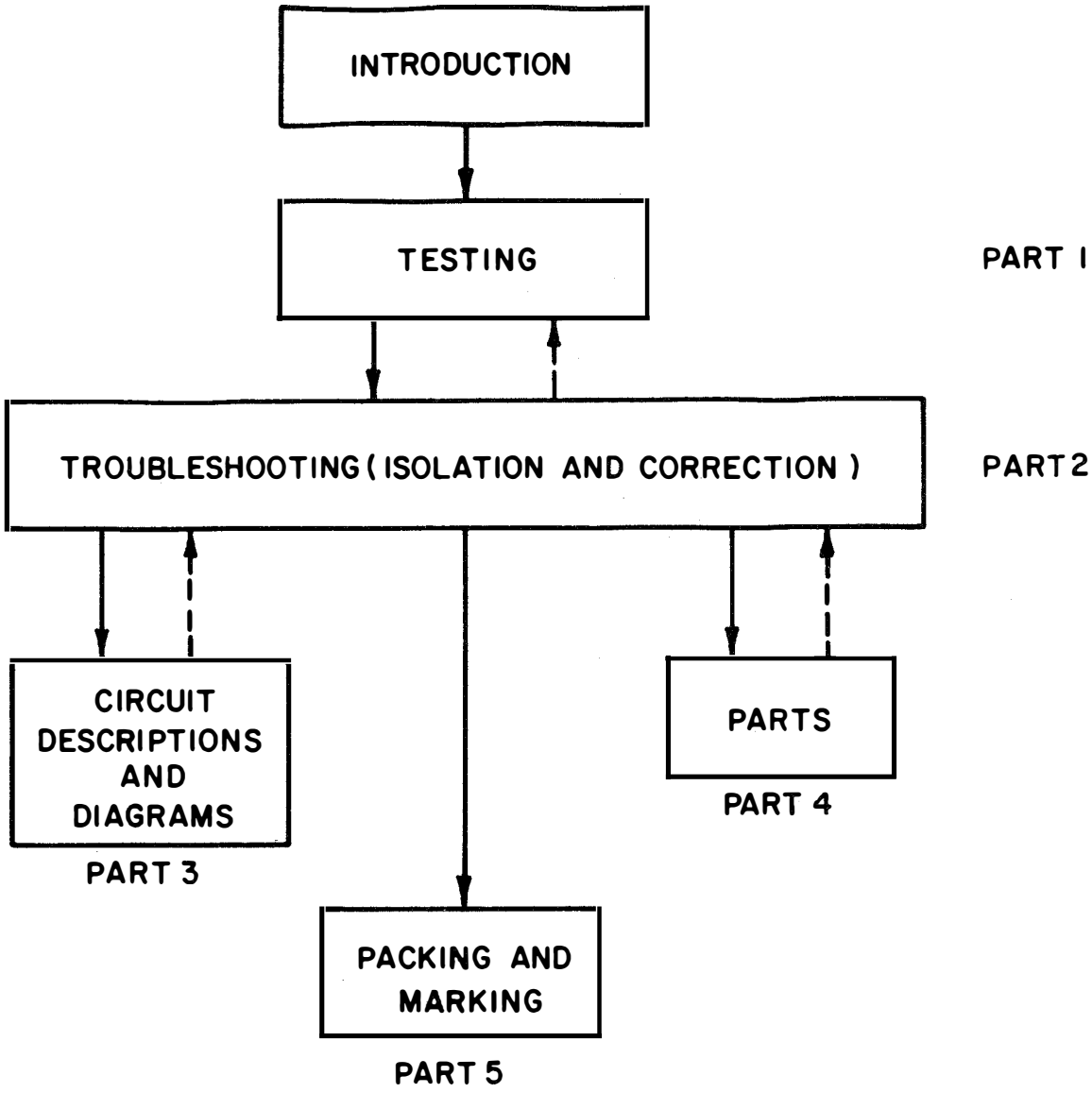
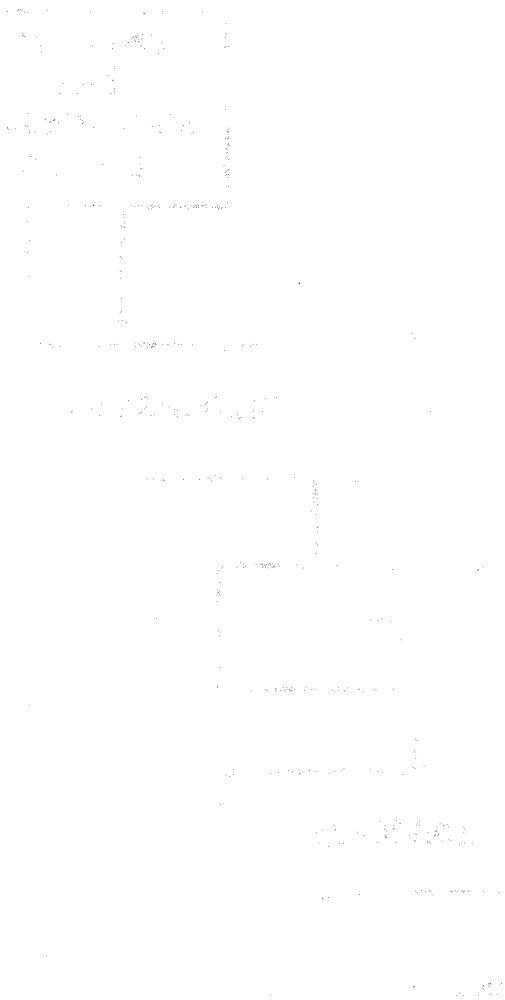
The Task Flow Chart below illustrates the intended repair activities and the associated manual parts.

TASK FLOW CHART





BASIC TELEPRINTER BLOCK DIAGRAM AND INTERFACING

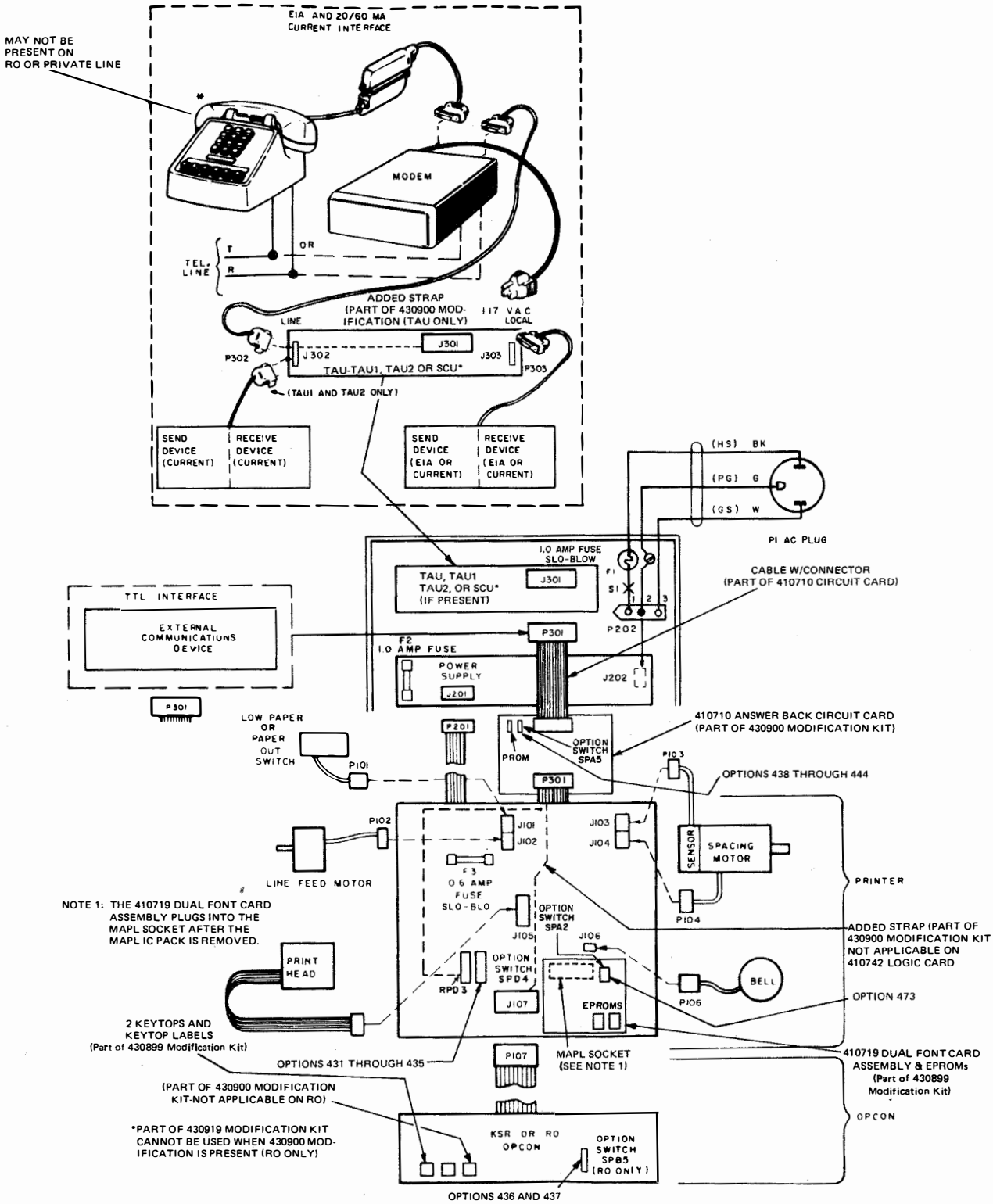


FIG. 3–BASIC 43 8-LEVEL TELEPRINTER STATION BLOCK DIAGRAM

BUFFERED TABLETOP TELEPRINTER BLOCK DIAGRAM AND INTERFACING

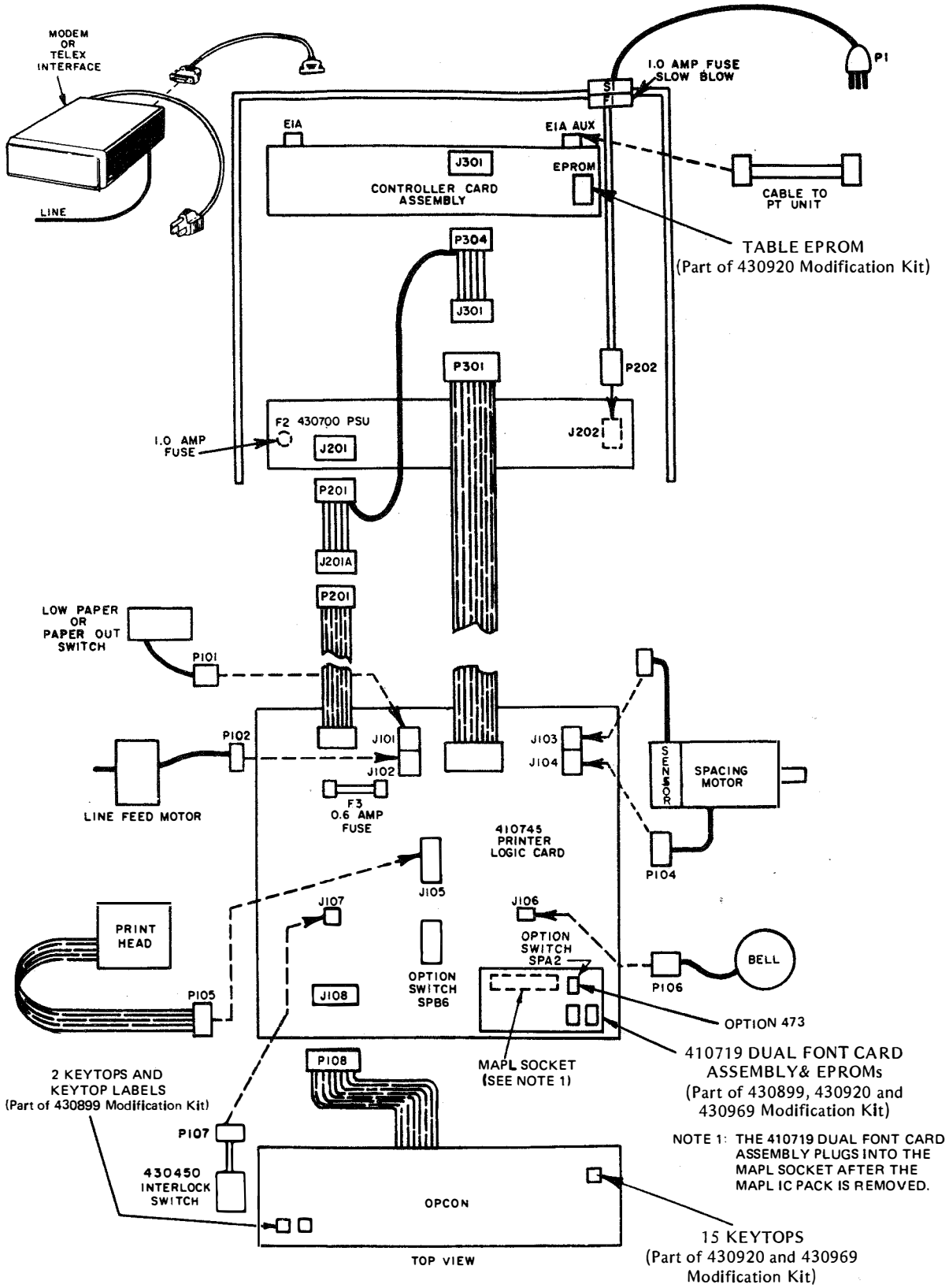


FIG. 4–BUFFERED 43 8-LEVEL TELEPRINTER STATION BLOCK DIAGRAM

PART 1 — TESTING

A. GENERAL

Refer to the appropriate service manual or specification for testing information. In the service manual or specification, testing of all major components is performed as part of a completely assembled terminal and troubleshooting therein is based on isolation of troubles to the major components. The 43 Teleprinter test arrangement shown in PART 2 may be used for testing if a completely assembled teleprinter is not available.

Note: When ordering replaceable parts or components, unless otherwise specified, prefix each part number with the letters "TP" (ie, TP411952).

Source Documents for Testing

The list below indicates the interfaces, modification kits, and controllers and their associated service manuals or specifications:

COMPONENT		SERVICE MANUAL OR SPECIFICATION NUMBER	DESCRIPTION
410382	Terminal Auxiliary Unit — TAU3	Manual 538	Basic 42 KSR and ASR
410746	SSI Interface Circuit Card	Manual 406	Buffered 43 KSR
410754	Terminal Auxiliary Unit — TAU 2	Manual 369	Basic KSR and RO
410755	Terminal Auxiliary Unit — TAU1	Manual 369	Basic KSR and RO
420301	Telex Interface	51048S	Installation Instructions
430899	APL Alternate Font Modification Kit	51063S	Installation Instructions
430900	Answer-Back Modification Kit	Manual 369	Basic KSR and RO
430910	Selective Calling Modification Kit	50962S	Installation Instructions
430920	Weather Font Modification Kit	51062S	Installation Instructions
430969	Weather Font Modification Kit	51062S	Installation Instructions
454668	Electronic Top of Form Modification Kit	51053S	Installation Instructions
411901	Controller Assembly	51049S	Configuration and Assembly
411902	Controller Assembly	Manual 406	Buffered 43 KSR
411904	Controller Assembly	Manual 425	Buffered 42 KSR andASR
411905	Controller Assembly	Manual 468	Buffered 43 Selective Calling
411906	Controller Assembly	Manual 482	Buffered 42 Selective Calling
411907	Controller Assembly	Manual 425	Buffered 42 KSR and ASR
411908	Controller Assembly	Manual 482	Buffered 42 Selective Calling
411909	Controller Assembly	Manual 468	Buffered 43 Selective Calling
411910	Controller Assembly	Manual 406 (Issue 3)	Buffered 43 KSR

PART 2 — TROUBLESHOOTING

CONTENTS PAGE

CONTENTS PAGE

A. GENERAL

This part provides troubleshooting information for the components listed on Page 2-1.

Check and verify proper static circuit resistance of defective circuit cards before connecting them to the teleprinter, to prevent overloading the power supply and blowing the fuse when power is turned on.

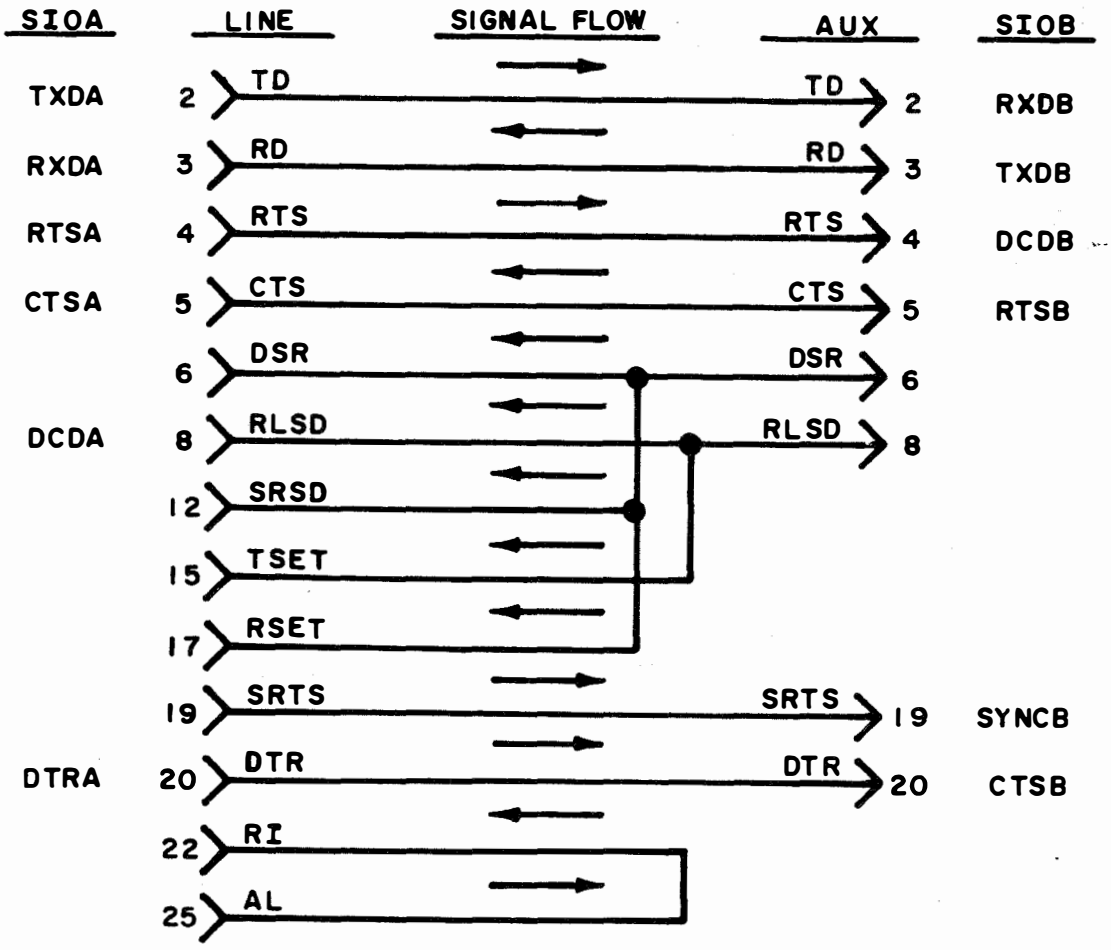
Use meter RX1 scale when making resistance readings. Resistance readings shown are approximate and may be higher or lower than those specified, depending on meter used.

Verify proper operating voltages are present and correct before replacing integrated circuit packs.

Note: When ordering replaceable parts or components, unless otherwise specified, prefix each part number with the letters "TP" (ie, TP410055).

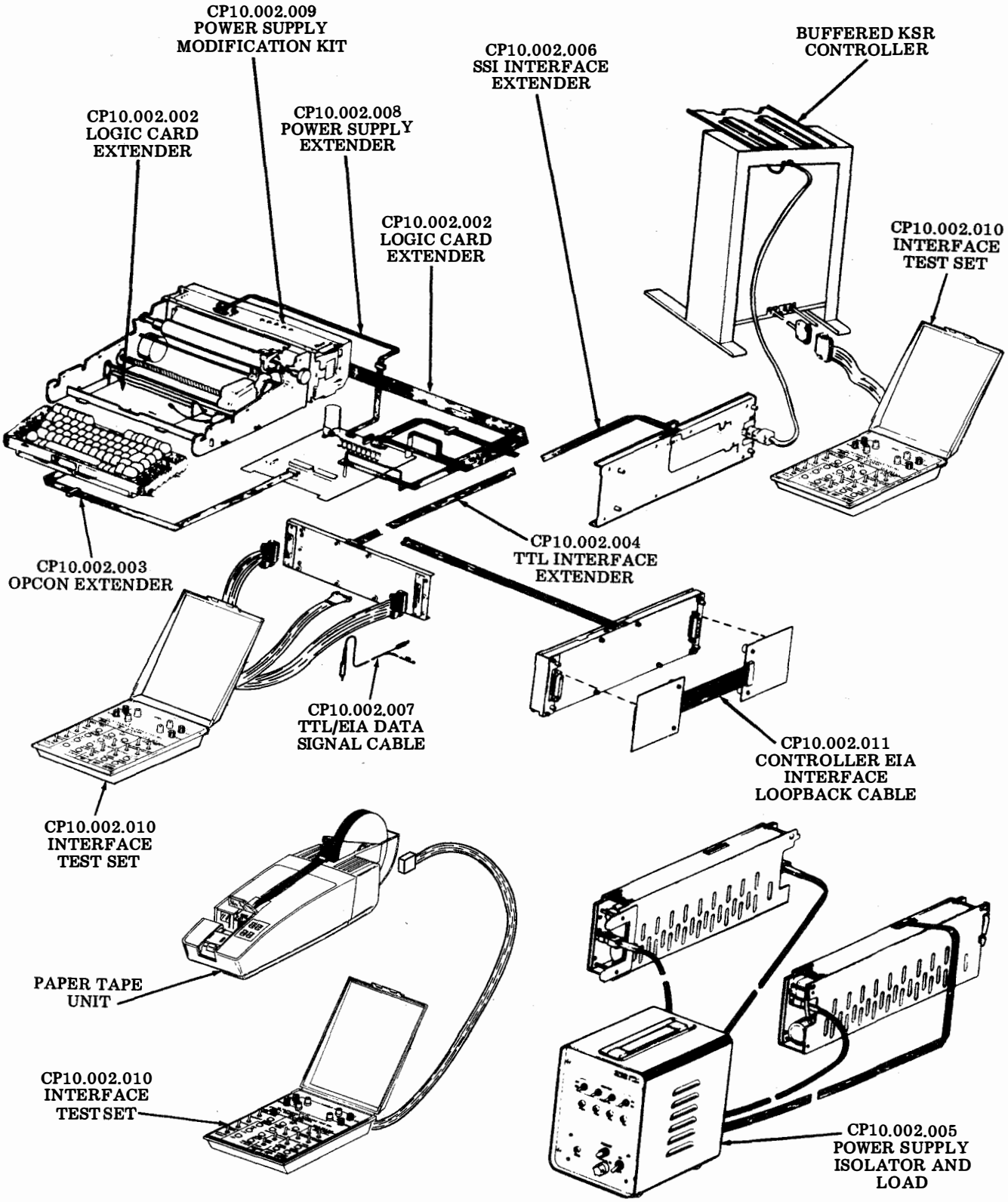
The 43 Teleprinter Test Arrangement may be used in conjunction with the testing and troubleshooting parts in this manual. Contact Teletype Corporation Custom Systems Division, 312-982-2000, for test equipment ordering information.

The EIA Loopback Test for early design controller assemblies requires the connection of a special loopback cable between the two ports. A diagram of the CP10.002.011 loopback cable is shown below.



EIA INTERFACE LOOPBACK CABLE

A. GENERAL (Contd)



43 TELEPRINTER TEST ARRANGEMENT

B. 410382 DUAL EIA/NEUTRAL INTERFACE — TAU3 TROUBLESHOOTING

Troubleshooting Guide for Current Interface

QUESTION	YES	NO
1. Does the Send Current increase from 5 ma to maximum current when $\overline{DTR}$ J103-5 turns on, 0 V?	Go to 2.	Go to 1a.
1a. Is 0 V present at MLB12-11 when $\overline{DTR}$ is on?	Go to 1b.	Check MLB10-12, MLB10-2, MLB11-4 and MLB12-11.
1b. Is 0 V present at MLB9-8?	Go to 1c.	Replace MLB9.
1c. Is +12 V present at cathode of CR8?	Go to 1d.	Check MLB7, Q6, CR7, CR8.
1d. Is 5 ma current present in Send Loop?	Check MLB6 and Q3.	Go to 1e.
1e. Is +5 V present at MLB5-2?	Check MLB5, Q4, Q5, CR3-CR5.	Replace MLB9.
2. Is data properly transmitted?	Go to 3.	Go to 2a.
2a. Does MLB9-8 toggle when characters are sent?	Check MLB6, Q3.	Check MLB10-12, MLB12-11, MLB9-8.
3. Is current present in Receive Loop?	Go to 4.	Go to 3a.
3a. Is forward voltage palarity present at TB1+ and TB1-?	Check MLB1, MLB2, Q1, CR1.	Go to 3b.
3b. Is reverse voltage palarity present at TB1+ and TB1-?	Check MLB3, MLB4, Q2, CR2.	External connection or loop voltage problem.
4. Is RD (Receive Data) J103-17 +5 V when forward current is present in Receive Loop?	Go to 5.	Go to 4a.
4a. Is MLB11-14 0 V when forward current is present in Receive Loop?	Go to 4b.	Replace MLB2.
4b. Is MLB13-6 +5 V?	Replace MLB12, MLB8.	Replace MLB11, MLB13.
5. Is RD J103-17 +5 V when reverse current is present in Receive Loop?	Go to 6.	Go to 5a.
5a. Is MLB11-7 0 V when reverse current is present?	Go to 5b.	Replace MLB4.
5b. Is MLB13-6 +5 V?	Replace MLB12, MLB8.	Replace MLB6, MLB13.

B. 410382 DUAL EIA/NEUTRAL INTERFACE – TAU3 TROUBLESHOOTING (Contd)

Troubleshooting Guide for Current Interface (Contd)

QUESTION	YES	NO
6. Is $\overline{DSR}$ J103-15 +5 V when forward Receive Current is present and ST1 is in the normal position?	Go to 7.	Go to 6a.
6a. Is MLB13-2 +5 V?	Go to 6b.	Check MLB3-5, MLB1-5, MLB13-8 through 13.
6b. Is MLB13-1 +5 V?	Check MLB13-3, MLB12-8, MLB10-4.	Replace MLB8, MLB12.
7. Is $\overline{DSR}$ J103-15 0 V when reverse receive current is present and ST1 is in the normal position?	Go to 8.	Go to 7a.
8. Is trouble present but not defined?	Undefined Trouble - Refer to Circuit Description and Diagrams, etc.	Review initial indication of trouble.

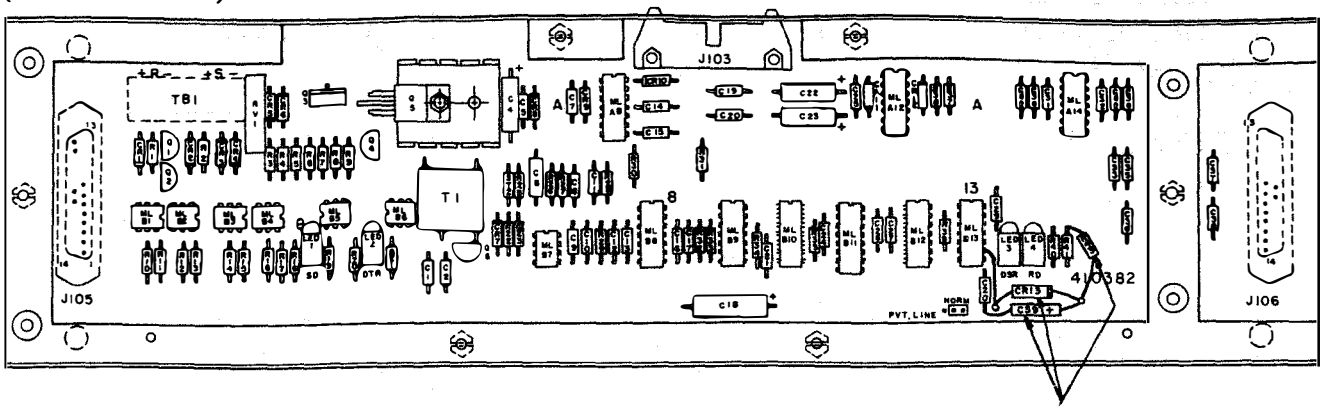
Troubleshooting Guide for RS-232 — EIA Interface

QUESTION	YES	NO
1. Is DTR J105 pin 20 on (+12 V) when $\overline{\text{DTR}}$ J103 pin 5 is on 0 V?	Go to 2.	Check MLB10-2, MLB11-4, MLA8-8.
2. Is $\overline{\text{DSR}}$ J103 pin 15 on (0 V) when DSR J105 pin 6 and DCD pin 8 are on +12 V?	Go to 3.	Go to 2a.
2a. Is MLB12-6 0 V?	Go to 2b.	Check MLB8-3 and MLB8-6.
2b. Is MLB13-2 +5 V?	Check MLB13-3, MLB12-8, MLB10-4.	Check MLB13-8 and 11, CR13, C39.
3. Is $\overline{\text{CTS}}$ J103-12 0 V when J105-5 CTS is on +12 V?	Go to 4.	Replace MLB8.
4. Is data properly sent?	Go to 5.	Check MLB10-12, MLB11-2, MLA8-3.
5. Is data properly received?	Go to 6.	Check MLB8-8, MLB12-3.
6. Is trouble present but not defined?	Undefined Trouble — Refer to Circuit Descriptions and Diagrams, etc.	Review initial indication of trouble.

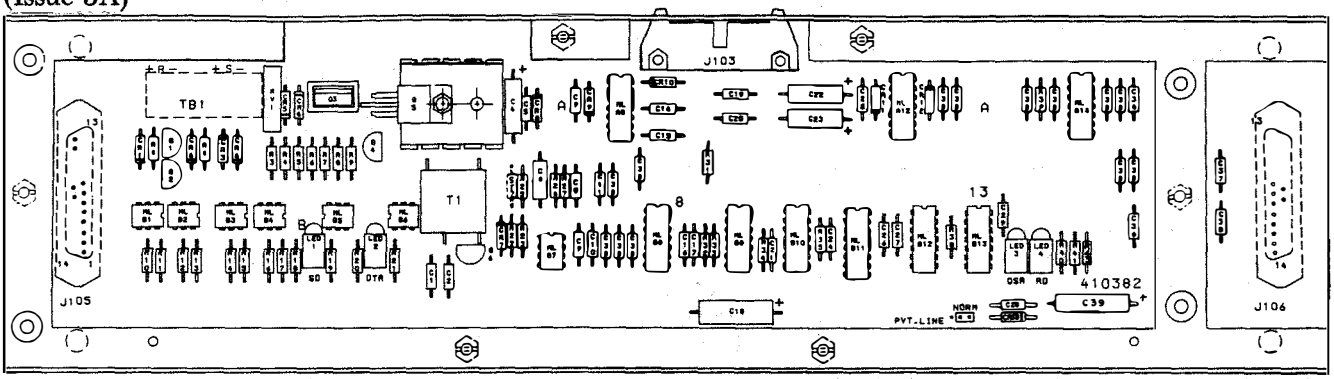
B. 410382 DUAL EIA/NEUTRAL INTERFACE — TAU3 TROUBLESHOOTING (Contd)

410382 Terminal Auxiliary Unit — TAU3 Component Layout

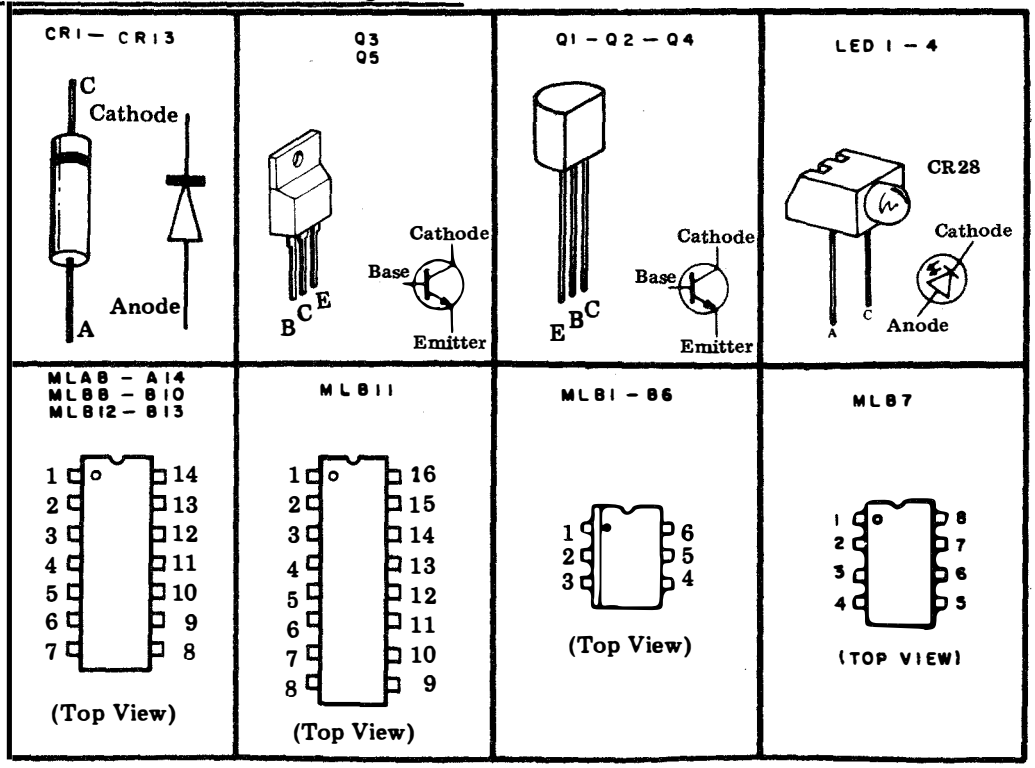
(Issue 1B and 2A)



(Issue 3A)



Component Identification and Lead Designation



Semiconductor In-Circuit Static Forward Resistance

COMPONENT		RESISTANCE (Approx)
CR1-CR6		28 Ohms
CR7-CR12		30 Ohms
LED 1-4		110 Ohms LED On
Q1-Q2	B-E	30 Ohms
	B-C	30 Ohms
	E-C	32 Ohms
Q3	B-E	30 Ohms
	B-C	30 Ohms
	E-C	60 Ohms
Q4	B-E	32 Ohms
	B-C	32 Ohms
	E-C	40 Ohms
Q5	B-E	28 Ohms
	B-C	28 Ohms
	E-C	70 Ohms
Q6	B-E	30 Ohms
	B-C	30 Ohms
	E-C	100 Ohms

COMPONENT		RESISTANCE (Approx)
MLB1-B3	1-2	60 Ohms
	4-6	50 Ohms
	5-6	40 Ohms
	4-5	40 Ohms
MLB2-B4	1-2	55 Ohms
	4-6	50 Ohms
	5-6	40 Ohms
	4-5	40 Ohms
MLB5	1-2	60 Ohms
	4-6	50 Ohms
	5-6	40 Ohms
	4-5	70 Ohms
MLB6	1-2	60 Ohms
	4-6	50 Ohms
	5-6	40 Ohms
	4-5	30 Ohms

Static Circuit Resistance — RX1 Scale (See Note)

CONNECTOR TERMINAL		REFERENCE POINT		RESISTANCE (Approx)	
				LO	HI
J103-13	(+12 V)	J103-9	(Logic Gnd)	115 Ohms	10K Ohms
J103-11	(-12 V)	J103-9	(Logic Gnd)	Infinity	Infinity
J103-7	(+5 V)	J103-9	(Logic Gnd)	25 Ohms	130 Ohms

Note: Take resistance reading, reverse meter leads and take second resistance reading.

C. 410754 TERMINAL AUXILIARY UNIT — TAU2 TROUBLESHOOTING

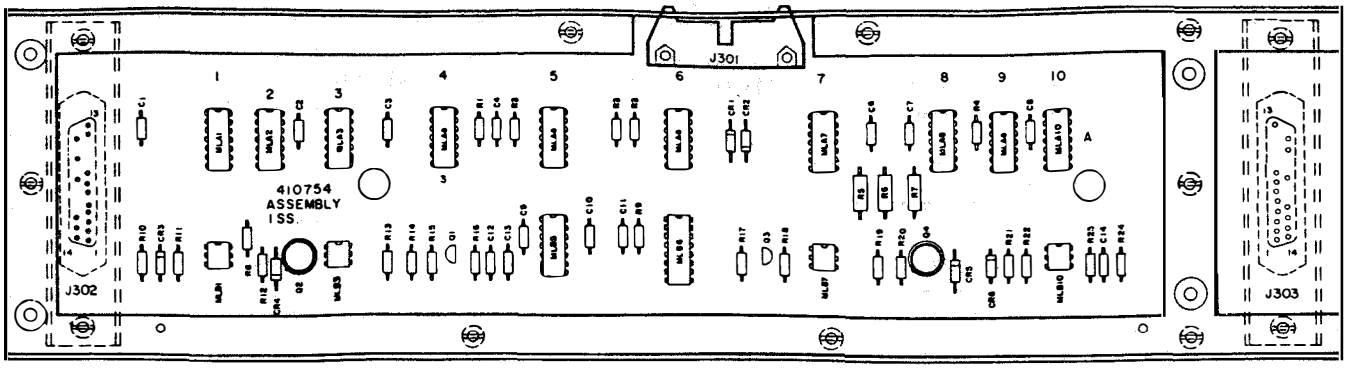
Troubleshooting Guide

QUESTION	YES	NO
1. Does DATA indicator on opcon light in Loopback mode?	Go to 2.	Go to 1a.
1a. Is Data Terminal Ready pin 20 Line Interface on, +12 V?	Go to 1b.	Go to 1c.
1b. Is TTL Interface Data Ready pin 15 on, 0 V? (Line Interface Data Set Ready pin 6, Clear to Send pin 5 and carrier Detect pin 8 on, 0 V?)	Go to 2.	Go to 1d.
1c. Is MLA10-2, 0 V?	Check MLA10-3. Check MLB5-6 Check CR1 and CR2.	Check MLA9-6. Check CR1 and CR2.
1d. Is MLA3-2, 0 V?	Check MLA1-11. Check MLA3-3.	Check MLA1-6 and 8. Check MLA3-6.
2. Are characters entered from the opcon printed in the Full Duplex Loopback mode?	Go to 3.	Go to 2a.
2a. Are data signals present and correct on Send Data, Line Interface pin 2?	Go to 2c.	Go to 2b.
2b. Is 0 V present on MLA3-13?	Check MLA5-4, MLA 4-11 and MLB5-3.	Check MLA5-11, MLA9-3 and MLB6-15.
2c. Are data signals present and correct at MLA7-4?	Go to 2d.	Check MLA5-12, MLA7-11. MLA1-3 and MLB6-6.
2d. Is 0 V present on MLA6-6?	Check MLA7-6, MLA6-8, MLA5-8, MLA6-3, MLA5-6 and MLA7-3.	Check MLA5-10, MLA7-8, MLA9-3 and MLB6-15.
3. Does auxiliary device receive data properly?	Go to 4.	Go to 3a.
3a. Is MLA4-4, +5 V in the Local mode?	Go to 3b.	Check MLA3-8.
3b. Is MLA4-9, +5 V in the Line mode?	Check MLB5-11, MLA4-6, MLA4-8 and MLA6-11. Go to 3c.	Check MLA5-4.

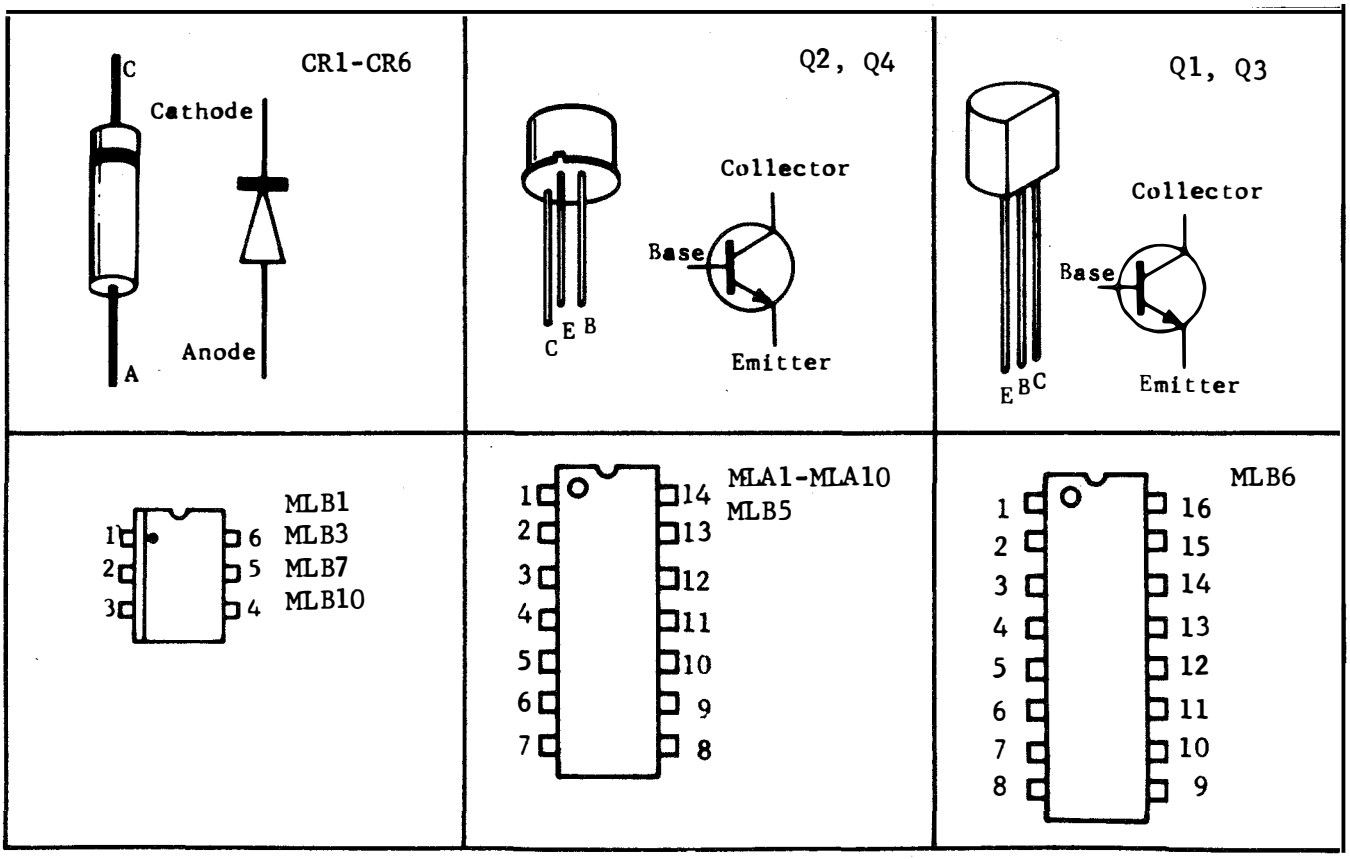
QUESTION	YES	NO
3c. Is auxiliary receive device using current loops?	Check MLB6-10 and 12, Q3, MLB7, Q4 and CR5.	Check MLA8-6 and MLB5-8.
4. Does auxiliary device send data properly?	Go to 5.	Go to 4a.
4a. Are data signals present and correct at MLA5-10?	Check MLA6-6, MLA4-3 MLA6-3 and MLA7-3.	Check MLA9-3, MLB6-15, MLB10, and CR6.
5. Is data properly received by the line current device?	Go to 6.	Check MLB6-2, MLB6-4, Q1, MLB3, Q2 and CR4.
6. Is data printed when sent from the line current send device?	Go to 7.	Check MLA7-11, MLB6-6, MLB1 and CR3.
7. Is trouble present but not defined by Questions 1 through 6?	Undefined trouble — refer to Circuit Descriptions and Diagrams, etc.	Review initial indication of trouble.

C. 410754 TERMINAL AUXILIARY UNIT — TAU2 TROUBLESHOOTING (Contd)

410754 Terminal Auxiliary Unit — TAU2 Component Layout



Component Identification and Lead Designation



Semiconductor In-Circuit Static Forward Resistance

COMPONENT	RESISTANCE (Approx)	COMPONENT	RESISTANCE (Approx)
CR1	32 Ohms	MLB1 1-2	48 Ohms
CR2	32 Ohms	4-6	48 Ohms
CR3	35 Ohms	5-6	40 Ohms
CR4	32 Ohms		
CR5	32 Ohms	MLB3 1-2	65 Ohms
CR6	35 Ohms	4-6	48-75 Ohms
		5-6	40-48 Ohms
Q1 B-E	36 Ohms		
B-C	36 Ohms	MLB7 1-2	65 Ohms
		4-6	48-75 Ohms
Q2 B-E	32 Ohms	5-6	40-48 Ohms
B-C	32 Ohms		
		MLB10 1-2	48 Ohms
Q3 B-E	36 Ohms	4-6	48 Ohms
B-C	36 Ohms	5-6	40 Ohms
Q4 B-E	32 Ohms		
B-C	32 Ohms		

Static Circuit Resistance — RX1 Scale (See Note)

CONNECTOR TERMINAL	REFERENCE POINT	RESISTANCE (Approx)	
		LO	HI
J301-7 (+5 V)	J301-9 (Logic Grd)	28 Ohms	110 Ohms
J301-13 (+12 V)	J301-9 (Logic Grd)	8K Ohms	Infinity
J301-11 (-12 V)	J301-9 (Logic Grd)	Infinity	Infinity

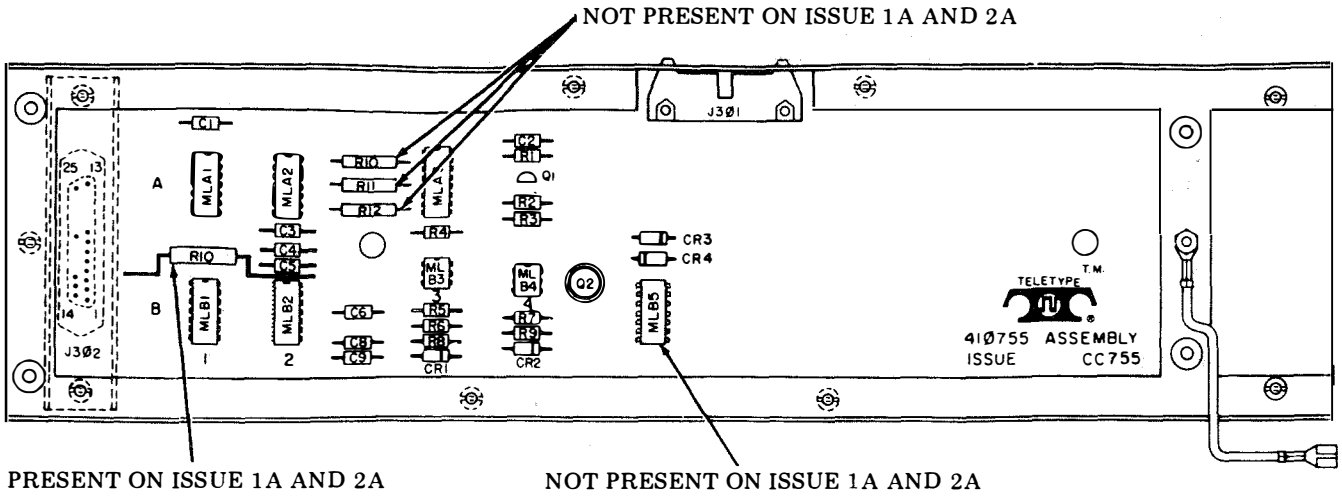
Note: Take resistance reading, reverse meter leads and take second resistance reading.

D. 410755 TERMINAL AUXILIARY UNIT — TAU1 TROUBLESHOOTING

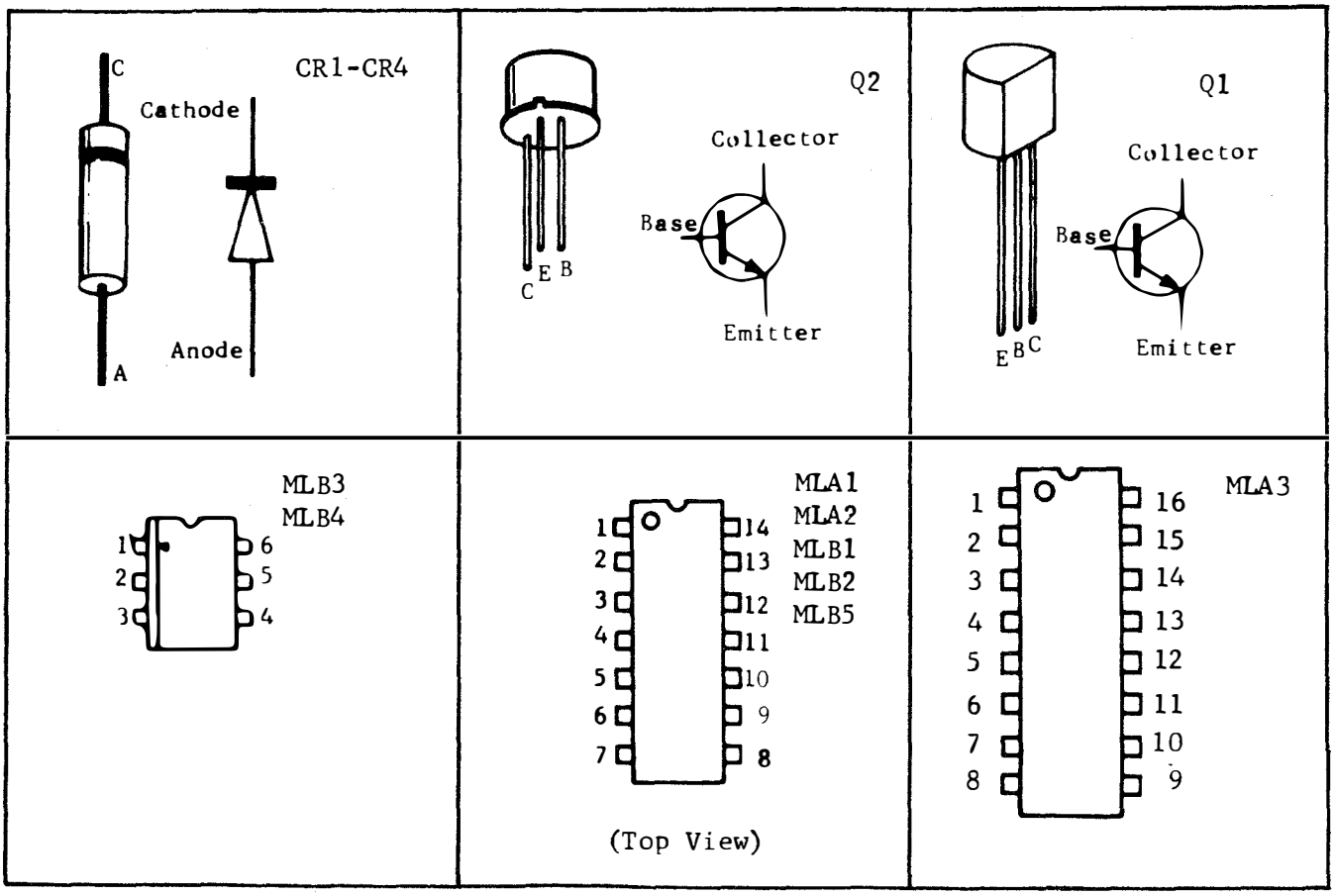
Troubleshooting Guide

QUESTION	YES	NO
1. Does DATA indicator on opcon light in Loopback mode?	Go to 2.	Go to 1a.
1a. Is Data Terminal Ready pin 20 line interface on, +12 V?	Go to 1b.	Replace MLB2.
1b. Is TTL interface Data Ready pin 15 on, 0 V? (Line interface Data Set Ready pin 6, Clear to Send pin 5, and Carrier Detect pin 8 on, 0 V)	Go to 2.	Check MLA2-6. Check MLB1-3, 8 and 11. Check MLA1-8 and 11.
2. Does printer respond properly to keyboard operation in Loopback mode?	Go to 3.	Check MLB2-3. Check MLB1-4. Check MLA1-3.
3. Is terminal used in current loop application?	Go to 4.	Go to 6.
4. Is data properly sent?	Go to 5.	Check Transmit Current Loop circuit: MLA3-12 and 15, Q1, MLB4, Q2 and CR2.
5. Is data properly received?	Go to 6.	Check Receive Current Loop circuit: CR1, MLB3, MLA3-2 and MLA1-3.
6. Is trouble present but not defined?	Undefined trouble — refer to Circuit Descriptions and Diagrams, etc.	Review initial indication of trouble.

410755 Terminal Auxiliary Unit — TAU1 Component Layout



Component Identification and Lead Designation



D. 410755 TERMINAL AUXILIARY UNIT — TAU1 TROUBLESHOOTING (Contd)

Semiconductor In-Circuit Static Forward Resistance

COMPONENT	RESISTANCE (Aprox)	COMPONENT	RESISTANCE (Approx)
CR1	35 Ohms	MLB3 1-2	48 Ohms
CR2	32 Ohms	4-6	48 Ohms
CR3	32 Ohms	5-6	40 Ohms
CR4	32 Ohms		
		MLB4 1-2	65 Ohms
Q1 B-E	36 Ohms	4-6	48-75 Ohms
B-C	36 Ohms	5-6	40-48 Ohms
Q2 B-E	32 Ohms		
B-C	32 Ohms		

Static Circuit Resistance — RX1 Scale (See Note)

CONNECTOR TERMINAL	REFERENCE POINT	RESISTANCE (Approx)	
		LO	HI
J301-7 (+5V)	J301-9 (Logic Grd)	30 Ohms	150 Ohms
J301-13 (+12V)	J301-9 (Logic Grd)	16K Ohms	Infinity
J301-11 (-12V)	J301-9 (Logic Grd)	Infinity	Infinity

Note: Take resistance reading, reverse meter leads and take second resistance reading.

E. 430900 ANSWER-BACK MODIFICATION KIT TROUBLESHOOTING

410710 Answer-Back Circuit Card Troubleshooting

Troubleshooting Guide

QUESTION	YES	NO
1. Is answer-back message generated under any conditions?	Go to 2.	Go to 1a.
1a. Are characters entered from the keyboard printed in the Full Duplex Loopback mode?	Go to 1d.	Go to 1b.
1b. Are send data signals present and correct at MLB9-8?	Go to 1c.	Check MLB9-8. Check MLB3.
1c. Are received data signals present and correct at MLB9-11?	Go to 1d.	Check MLB9-11, MLC11-12, MLC6-10 and MLC6-13.
1d. Is MLC7-8, +5 V when answer-back message is to be generated?	Go to 1f.	Go to 1e.
1e. Is MLC10-6, +5 V?	Check MLC10-6. Check MLC7-8.	Check MLB1-7, MLA2-6 and MLC1-8.
1f. Is the clock present and correct at ML10-10?	Go to 1g.	Check MLA10. Check MLB11-3.
1g. Is MLB9-2, +5 V?	Go to 1j.	Go to 1h.
1h. Is MLB6-5, +5 V?	Go to 1i.	Check PROM (MLA4).
1i. Is MLC5-9, +5 V?	Check MLB5-8 Check MLC5-10	Check MLB3.
1j. Is pulse generated on MLB3-23 when MLC10-13 goes to +5 V?	Go to 1k.	Check MLC10-3 and 11.
1k. Is pulse generated on MLC5-2 when MLC7-3 goes to 0 V?	Check MLB4, MLC4 and MLA4.	Check MLC6-1, MLB5-3 and 6, and MLC5-2.
2. Is answer-back message generated on auto-answer (SW5 closed)?	Go to 3.	Check MLC12, MLB12, MLA13-6, MLC13-1, MLB11-11, MLB6-8 and 11 SW5.
3. Is answer-back message generated when "ENQ" is received?	Go to 4.	Check "ENQ" decoder circuit check MLB3.

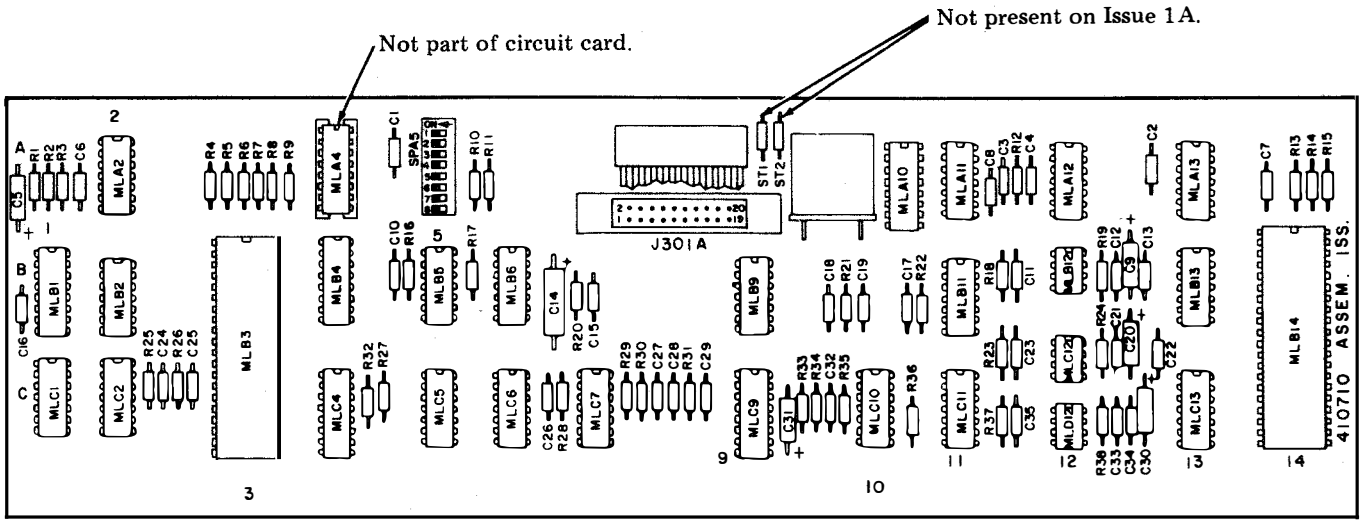
E. 430900 ANSWER-BACK MODIFICATION KIT TROUBLESHOOTING (Contd)

410710 Answer-Back Circuit Card Troubleshooting (Contd)

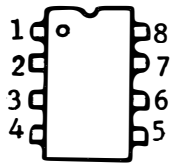
Troubleshooting Guide (Contd)

	QUESTION	YES	NO
4.	Is answer-back message generated when "Here Is" is sent from keyboard?	Go to 5.	Check "Here Is" decoder circuit. Check MLB14.
5.	Does answer-back message print when in Half Duplex mode (SW3 closed).	Go to 6.	Check MLC5-6, MLB5-11, MLB9-11 and SW4.
6.	Is trouble present but not defined by Questions 1 through 5?	Undefined trouble — refer to Circuit Descriptions and Diagrams, etc.	Review initial indication of trouble.

410710 Answer-Back Circuit Card Component Layout

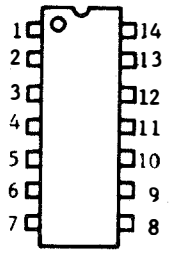


Component Identification and Lead Designation



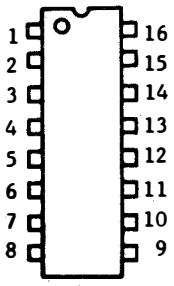
(Top View)

MLB12
MLC12
MLD12



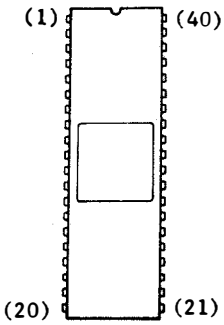
(Top View)

MLA2
MLA11-MLA13
MLB2
MLB5-MLB11
MLB13
MLC1
MLC2
MLC5-MLC7
MLC10
MLC11
MLC13



(Top View)

MLA4
MLA10
MLB1
MLB4
MLC2
MLC9



(Top View)

MLB3
MLB14

Static Circuit Resistance — RX1 (See Note)

CONNECTOR TERMINAL	REFERENCE POINT	RESISTANCE (Approx)	
		LO	HI
J301A-7 (+5 V)	J301A-9 (Logic Grd)	22 Ohms	65 Ohms
J301A-13 (+12 V)	J301A-9 (Logic Grd)	Infinity	Infinity
J301A-11 (-12 V)	J301A-9 (Logic Grd)	Infinity	Infinity

Note: Take resistance reading, reverse meter leads and take second resistance reading.

F. 430910 SELECTIVE CALLING MODIFICATION KIT TROUBLESHOOTING

410718 Selective Calling Card Troubleshooting

The Selective Calling Unit (SCU) must be coded with two answer-back characters (Option 448b), the others must be factory optioned (SP B2 switches 1, 2 and 4 OFF and switch 3 ON). Refer to Specification 50962S.

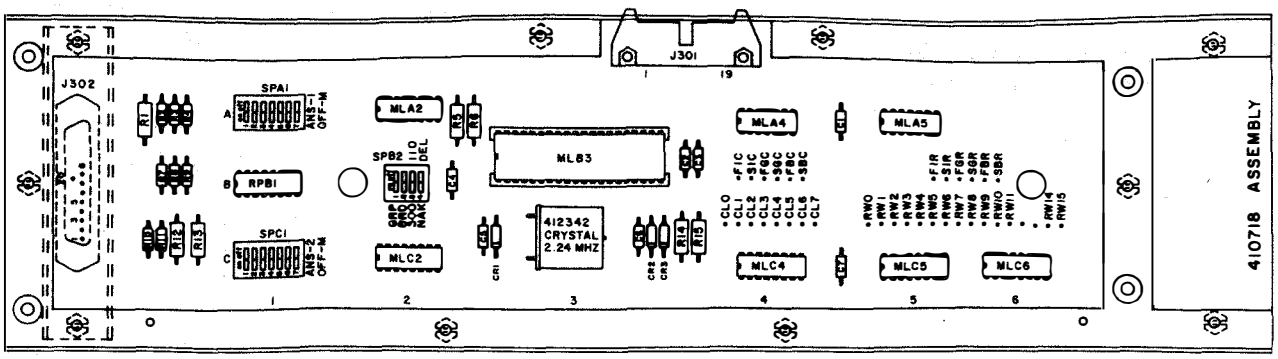
Troubleshooting Guide

QUESTION	YES	NO
1. After power up, is negative AB generated after receipt of ETX character?	Go to 2.	Check Option 448b. Check MLA2. Check MLC2. Check MLB3.
2. Is positive AB generated after receipt of EOT character?	Go to 3.	Check MLA2. Check MLC2. Check MLB3.
3. With cover raised, is negative AB generated after receipt of EOT?	Go to 4.	Check strap on logic card. Check MLA5. Check MLB3.
4. Is station selected after receipt of EOT and CDC character? (TERM READY key flashes on and DATA key blinks off and then on steady).	Go to 5.	Check CDC Coding on SCU. Check MLA4. Check MLC4, MLC5 and MLC6. Check MLB3.
5. Is received message printed without error?	Go to 6.	Check MLB3.
6. Is error flag set after receipt of message with parity error?	Go to 7.	Check MLB3.
7. Does printing occur while in Interrupt mode?	Check MLB3.	Go to 8.
8. Can error flag be set by sending at wrong speed?	Go to 9.	Check MLB3.
9. Can error flag be cleared by receipt of EOT?	Go to 10.	Check MLB3.

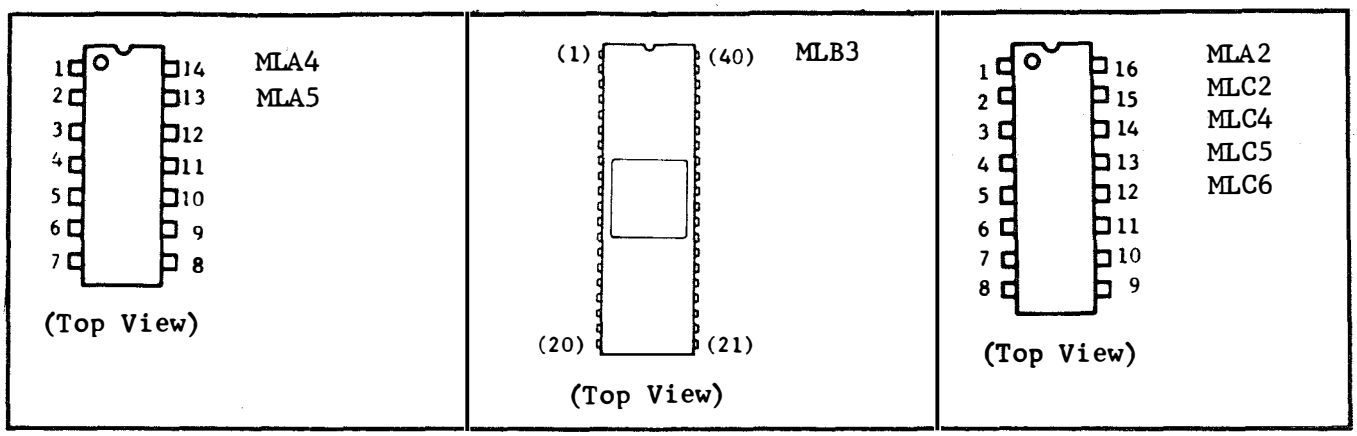
QUESTION	YES	NO
10. Is station blind to CDC in Passive mode? (No AB sent.)	Go to 11.	Check MLB3.
11. Is positive AB sent after receipt of Group CDC?	Go to 12.	Check group CDC coding. Check MLA4. Check MLC4, MLC5 and MLC6. Check MLB3.
12. Is positive AB sent after receipt of Broadcast CDC?	Go to 13.	Check Broadcast CDC coding. Check MLA5. Check MLC4, MLC5 and MLC6. Check MLB3.
13. Is trouble present but not defined by questions 1 through 12.	Undefined trouble — Refer to Circuit Descriptions, Diagrams, etc.	Review initial indication of trouble.

F. 430910 SELECTIVE CALLING MODIFICATION KIT TROUBLESHOOTING (Contd)

410718 Selective Calling Unit Circuit Card Component Layout



Component Identification and Lead Designation



Static Circuit Resistance — RX1 Scale (See Note)

CONNECTOR TERMINAL	REFERENCE POINT	RESISTANCE (Approx)	
		LO	HI
J301A-7 (+5 V)	J301A-9 (Logic Grd)	28 Ohms	110 Ohms
J301A-13 (+12 V)	J301A-9 (Logic Grd)	Infinity	Infinity
J301A-11 (-12 V)	J301A-9 (Logic Grd)	Infinity	Infinity

Note: Take resistance reading, reverse meter leads and take second resistance reading.

G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING

General

The controller assemblies used in the Buffered 42 and 43 Teleprinters are Z80 microprocessor based. Limited repair of these controllers can be performed using the LED indicator and the SPA7 switches in the Self-Test mode and WDP 0552. In depth shop level repair using a Z80 In-Circuit-Emulator, WDP 0552, and Shop Manual 478 should be performed by properly trained service personnel to isolate troubles not covered in this manual.

The SPA7 switches common to all these controllers function as follows when the self-test switch is depressed: (refer to the Controller Self-Test Flow Chart on Page 2-28).

(1) Early design controllers (410761 circuit card Issue 8A or earlier) with a part number other than 412413 or later in the MLA7 firmware EPROM location.

Switch 1 — determines if switches 4, 3 and 2 will affect self-test routine.

Switch 2 — determines if the EIA Loopback Test will be performed. EIA loopback cable must be present to perform test successfully. (Refer to 2-2.)

Switch 3 — determines if the Applications Program Card Test will be performed.

Switch 4 — determines if the SSI Test will be performed.

(2) Late design controllers (410761 circuit card Issue 9A or later) with Part Number 412413 MLA7 firmware EPROM or later.

Switch 1 — determines if switch 4 will affect self-test routine (see Note).

Switch 2 — not used - EIA Loopback Test cannot be performed.

Switch 3 — not used - If Applications Program Card is present, test will be performed — if Applications Program Card is not present, test will not be performed.

Switch 4 — determines if the SSI Test will be performed.

Note: If switch 1 is ON, the self-test switch is not depressed, the Applications Program Card not present and power is turned ON, the teleprinter will enter the Typewriter mode.

G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Self-Test Description for all Fully Assembled Controllers (All Switches ON) Issue 5A through 10A

With all SPA7 switches ON and the self-test switch depressed, the controller will function as follows:

(1) When the self-test switch is depressed, the LED will turn OFF (if not already off) for 1/2-second then turn ON.

(2) The LED will flash two times when the firmware EPROM MLA7 and first RAM Test are successfully completed.

(3) The LED will flash two times when the second RAM Test is successfully completed.

(4) The LED will flash two times when the first CMOS RAM Test is successfully completed.

(5) The LED will flash two times when the second CMOS RAM Test is successfully completed.

(6) The LED will flash six times when the CTC, SIO, SSI and Applications Program Card Test are successfully completed.

(7) The LED will then:

(a) Flash once more and turn OFF (411904 controller with 411959 Applications Program Card).

(b) Turn ON (all other controllers).

SELF-TEST TABLE 1

STEP	1	2	3	4	5	6	7
LED	TURNS OFF FOR 1/2 SECOND THEN TURNS ON	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 6 TIMES	FLASHES ONCE MORE OR TURNS ON
TEST	START UP ROUTINE	FIRMWARE EPROM AND RAM	RAM	CMOS	CMOS	CTC, SIO, SSI, APPLICATIONS PROGRAM CARD	END OF SELF-TEST

Self-Test Description (Early Design Controllers (410761 circuit card Issue 5A through 8A) Applications Program Card Not Present)

With SPA7 switches 1 and 3 OFF and 2 and 4 optional, the Applications Program Card not present and the self-test switch depressed, the controller will function as follows:

(1) When the self-test switch is depressed, the LED will turn OFF (if not already off) for 1/2-second then turn ON.

(2) The LED will flash two times when the firmware EPROM MLA7 and first RAM Test are successfully completed.

(3) The LED will flash two times when the second RAM Test is successfully completed.

(4) The LED will flash two times when the first CMOS RAM Test is successfully completed.

(5) The LED will flash two times when the second CMOS RAM Test is successfully completed.

(6) The CTC and SIO Tests will be performed.

(7) If SPA7 switch 4 is ON the SSI Test will be performed.

(8) Since SPA7 switch 3 if OFF, the Applications Program Card Test is skipped.

(9) If SPA7 switch 2 is ON, the EIA Loopback Test will be performed. (EIA interface loopback cable must be present. Refer to 2-2.)

(10) The LED will flash six times when the CTS, SIO and optional SSI and EIA Loopback Tests are successfully completed.

(11) The LED will then flash 10 or 21 times then turn ON.

SELF-TEST TABLE 2

STEP	1	2	3	4	5	6	7	8	9	10	11	12
LED	TURNS OFF FOR 1/2 SECOND THEN TURNS ON	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	—	—	—	—	FLASH 6 TIMES IF STEPS 6, 7, 8 AND 9 PASSED.	FLASHES ONCE MORE OR TURNS ON	FLASHES 10 OR 21 TIMES THEN TURNS ON
TEST	START UP ROUTINE	FIRMWARE EPROM AND RAM	RAM	CMOS	CMOS	CTC SIO	SSI IF SPA7-4 IS ON	SKIP APPLICATIONS PROGRAM CARD TEST	EIA LOOPBACK* IF SPA7-2 IS ON	—	END OF SELF-TEST	FUNCTION OF FIRMWARE EPROM

*EIA interface loopback cable must be present to successfully complete test.

G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Self-Test Description (Late Design Controllers (410761 circuit card Issue 9A and 10A) Applications Program Card Not Present)

With SPA7 switches 1, 2 and 3 OFF and 4 ON, the Applications Program Card not present and the self-test switch depressed, the controller will function as follows:

(1) When the self-test switch is depressed, the LED will turn OFF (if not already off) for 1/2 second then turn ON.

(2) The LED will flash two times when the firmware EPROM MLA7 and first RAM Test are successfully completed.

(3) The LED will flash two times when the second RAM Test is successfully completed.

(4) The LED will flash two times when the first CMOS RAM Test is successfully completed.

(5) The LED will flash two times when the second CMOS RAM Test is successfully completed.

(6) The LED will flash six times when the CTC, SIO and SSI Tests are successfully completed.

(7) The LED will then flash 10 or 21 times then turn ON.

SELF-TEST TABLE 3

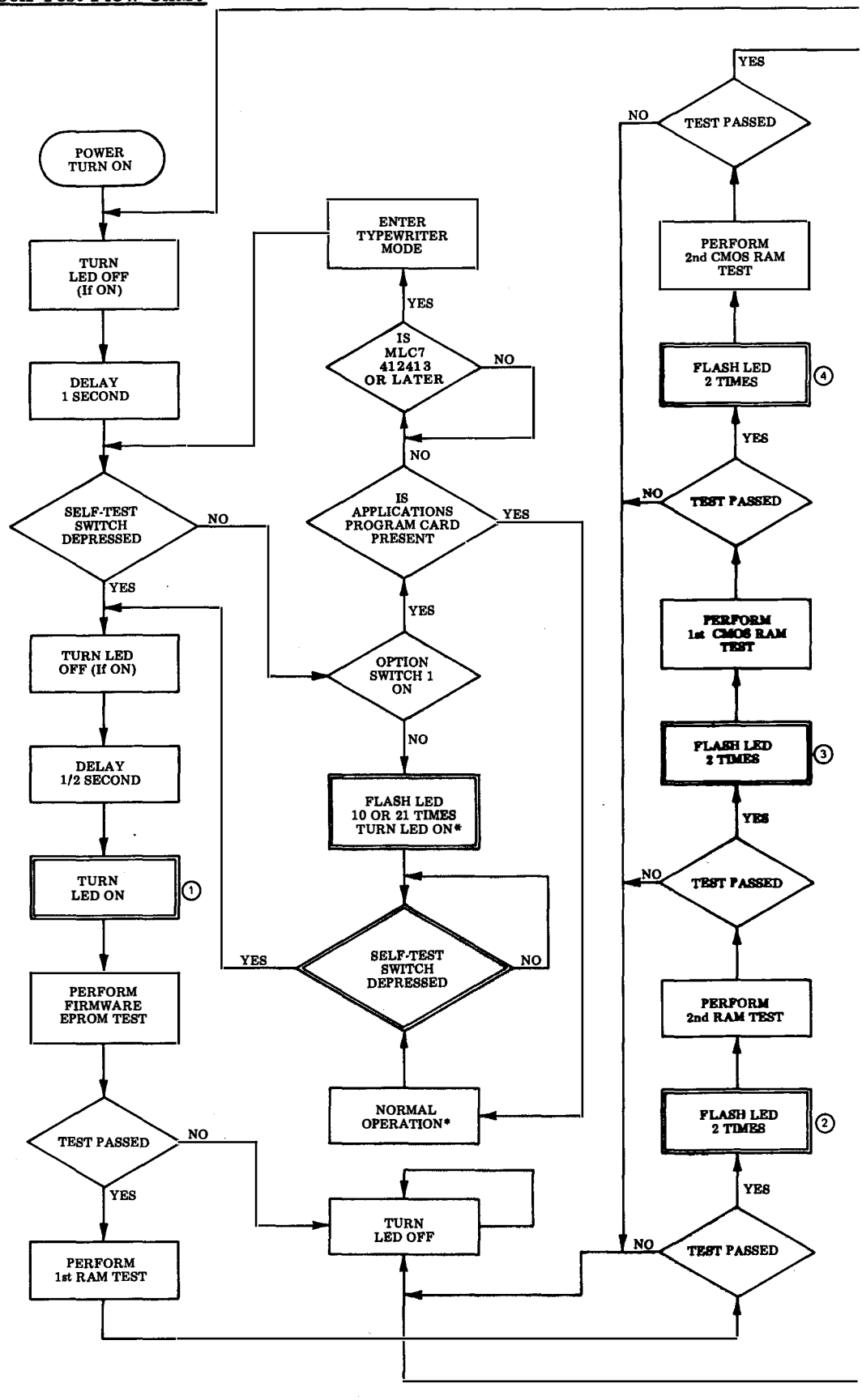
STEP	1	2	3	4	5	6	7	8
LED	TURNS OFF FOR 1/2 SECOND THEN TURNS ON	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 2 TIMES	FLASHES 6 TIMES	FLASHES ONCE MORE OR TURNS ON	FLASHES 10 OR 21 TIMES THEN TURNS ON
TEST	START UP ROUTINE	FIRMWARE EPROM AND RAM	RAM	CMOS	CMOS	CTC SIO SSI*	END OF SELF–TEST	FUNCTION OF FIRMWARE EPROM

*The SSI Test will be bypassed in SPA7 switch 4 is OFF.

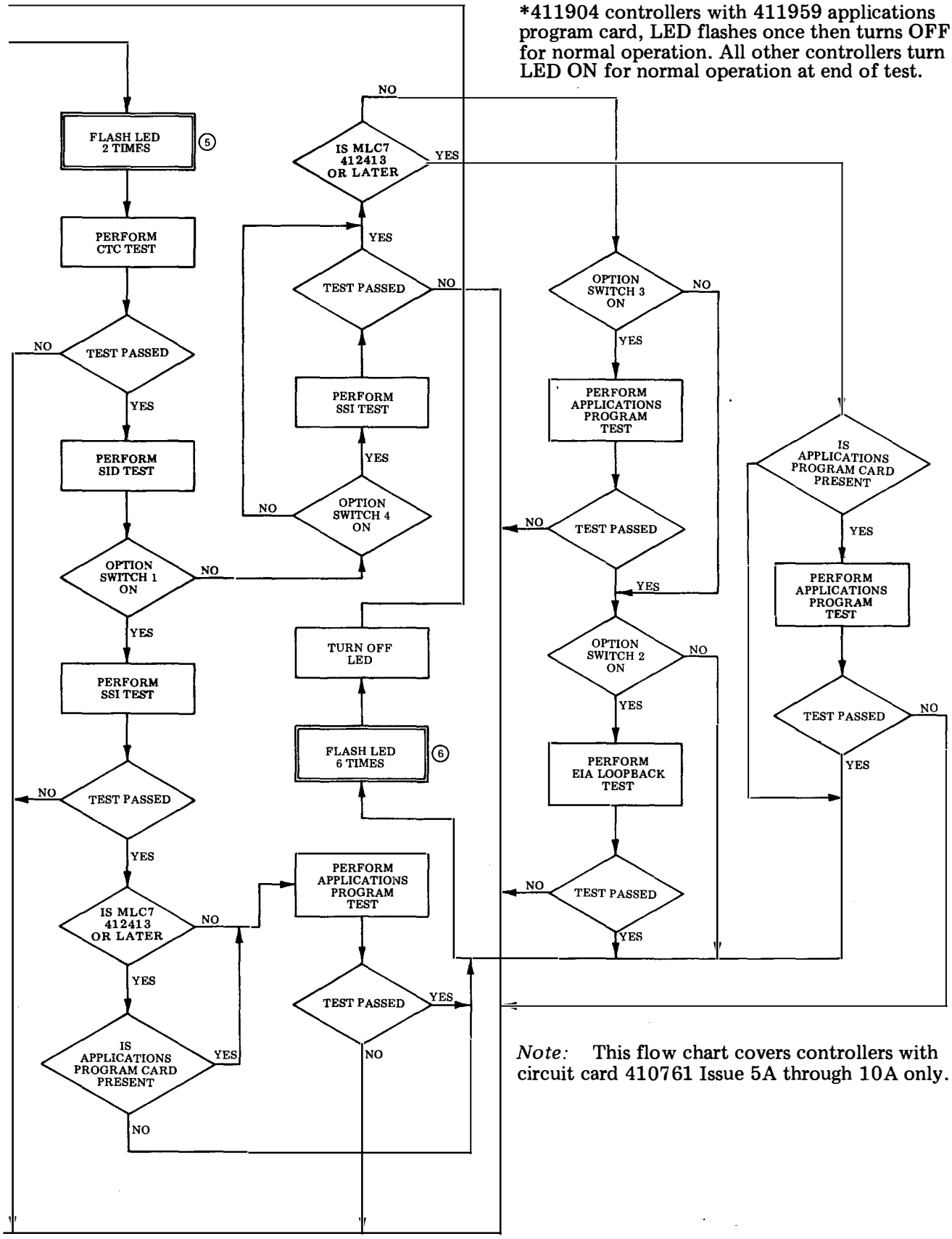
NOTES:

G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Controller Self-Test Flow Chart



*411904 controllers with 411959 applications program card, LED flashes once then turns OFF for normal operation. All other controllers turn LED ON for normal operation at end of test.



Note: This flow chart covers controllers with circuit card 410761 Issue 5A through 10A only.

G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Brief Troubleshooting Guide (Self-Test) (Refer to Page 2-28 and 2-29.)

QUESTION	NO	YES
1. Does LED turn OFF (if not already off) then turn ON when self-test switch is depressed?	Replace MLC4 (750 card), check clock circuits and Z80 control circuits using WDP 0552. Go to 10.	Go to 2.
2. Does LED fail to flash two times at end of first RAM Test?	Go to 3.	Replace MLC7 (761 card). Check firmware and RAM control circuits using WDP 0552. Go to 10.
3. Does LED fail to flash two times at end of second RAM Test?	Go to 4.	Check RAM circuitry using WDP 0552. Go to 10.
4. Does LED fail to flash two times at end of first CMOS RAM Test?	Go to 5.	Replace MLC5, MLC6 (761 card). Check CMOS RAM control circuitry using WDP 0552. Go to 10.
5. Does LED fail to flash two times at end of second CMOS RAM Test?	Go to 6.	Replace MLC5, MLC6 (761 card). Check CMOS RAM control circuitry using WDP 0552. Go to 10.
6. Does LED fail to flash six times at end of CTC, SIO, SSI and Applications Program Test?	Go to 9.	Go to 7.
7. Remove Applications Program Card, operate SPA7 - 1, 2 and 3 OFF and 4 ON. Repeat Self-Test. Does LED now fail to flash six times at end of CTC, SIO and SSI Test?	Replace Applications Program Card.	Go to 8.
8. Operate SPA7 - 4 OFF. Repeat Self-Test. Does LED now fail to flash six times at end of CTC and SIO Test?	Replace MLB5 (750 card).	Replace MLD5, MLA4 (750 card). Check CTC and SIO circuitry using WDP 0552. Go to 10.

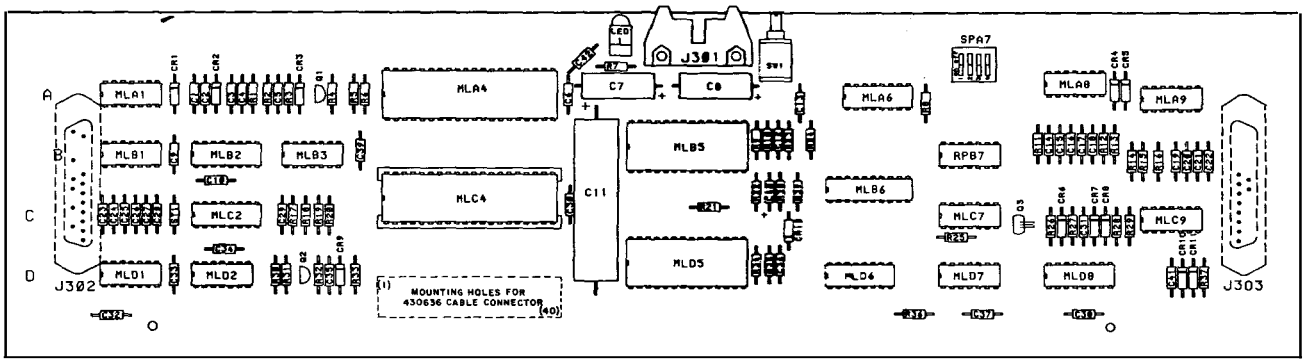
	QUESTION	NO	YES
9.	Late Design Controllers (410761 Circuit Card Issue 9A or greater) — Remove MLC7* and place Early Design EPROM TP part no. 404999, 407551 or 404992 into MLC7 socket.		Replace MLA4 (750 card).
	Operate SPA7 - 1 and 3 OFF, and 2 and 4 ON. Place loop-back cable on controller interface connectors. Repeat Self-Test.	Replace MLC7 if removed in 9.	Check SIO and EIA interface circuitry using WDP 0552. Replace MLC7 if removed in 9.
	Does LED now fail to flash six times at end of EIA Loop-back Test?	Go to 10.	Go to 10.
10.	Is trouble present but not defined or corrected in 1-9?	Review initial indications of trouble.	Refer to WDP 0552 or Shop Manual 478 and WDP 0552.

*Late design MLC7 EPROMs do not contain self-test routine for EIA Loopback Test. By temporarily placing an early design MLC7 EPROM into MLC7 socket, this EIA Loopback Test may be performed.

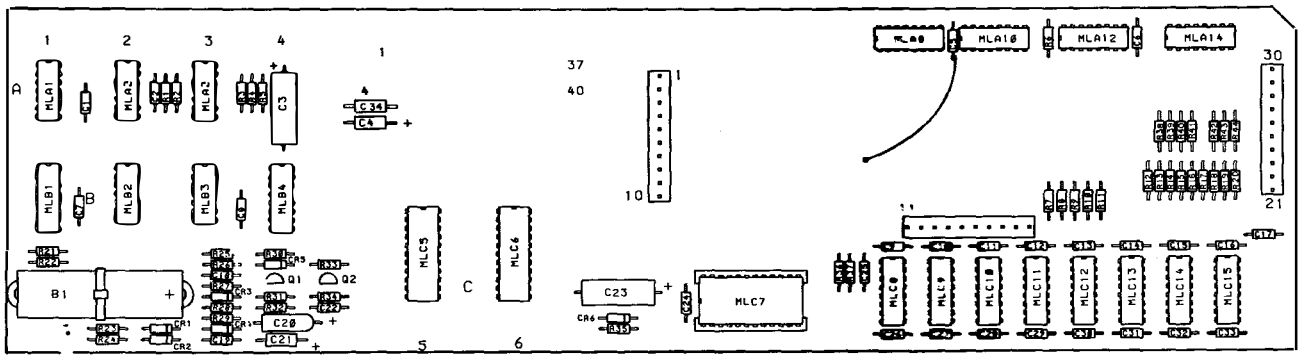
G. 411901 THROUGH 411910 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Circuit Card Component Layout

410750 Circuit Card Assembly



410761 Circuit Card Assembly



Note: MLA4, MLB5, MLC4 and MLD5 on 410750 Circuit Card Assembly are the only components specified in the Brief Troubleshooting Guide.

MLC5, MLC6, MLC7 on 410761 Circuit Card Assembly are the only components specified in the Brief Troubleshooting Guide.

H. 410231, 410232 AND 410241 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING

General

The controller assemblies used in the Basic 42 and 43 Teleprinter are 280 microprocessor based. Limited repair of these controllers can be performed using the LED indicator in the self-test mode and WDP 0553.

Self-Test Description

(1) With the PRINTER TEST (Model 43) HERE IS or SEARCH (Model 42) key depressed on SPD4-SW2 (Printer Logic Card) in the ON position and Teleprinter Power Switch operated from OFF to ON the controller LED and keyboard ALARM lamp will turn on.

(2) The LED will flash two times when the FIRMWARE and APPLICATIONS PROGRAM EPROMs and RAM Tests are successfully completed.

(3) The LED will flash two times when the first CMOS RAM Test is successfully completed.

(4) The LED will flash two times when the second CMOS RAM Test is successfully completed.

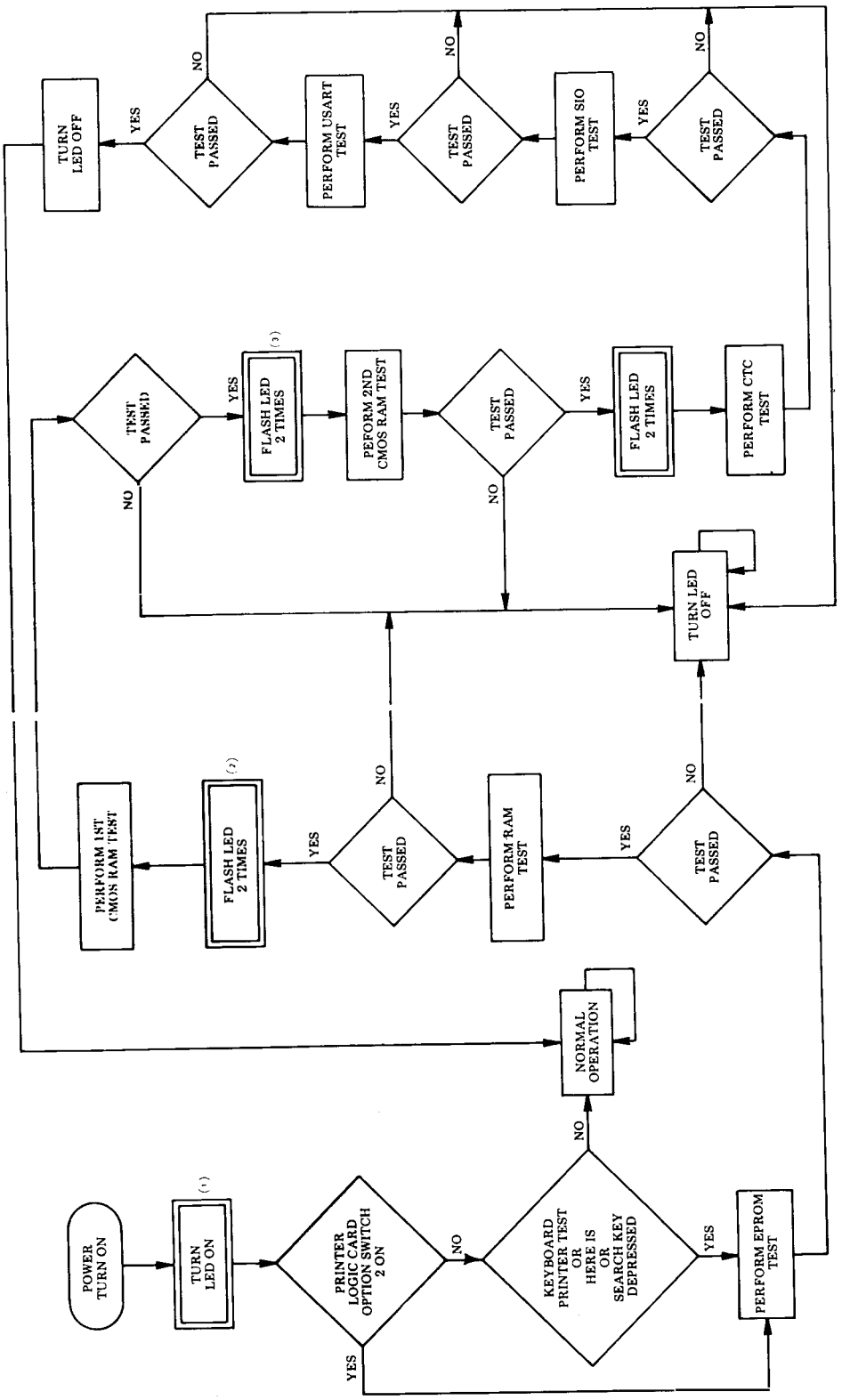
(5) The LED will flash six times when the CTC, SIO and USART Tests are successfully completed.

H. 410231, 410232 AND 410241 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

SELF-TEST TABLE

STEP	1	2	3	4	5
LED	Turns On	Flashes 2 Times	Flashes 2 Times	Flashes 2 Times	Flashes 6 Times
TEST	Start Up Routine	Firmware & Applications EPROM & RAM	CMOS	CMOS	CTC, SIO, USART

Controller Self-Test Flow Chart



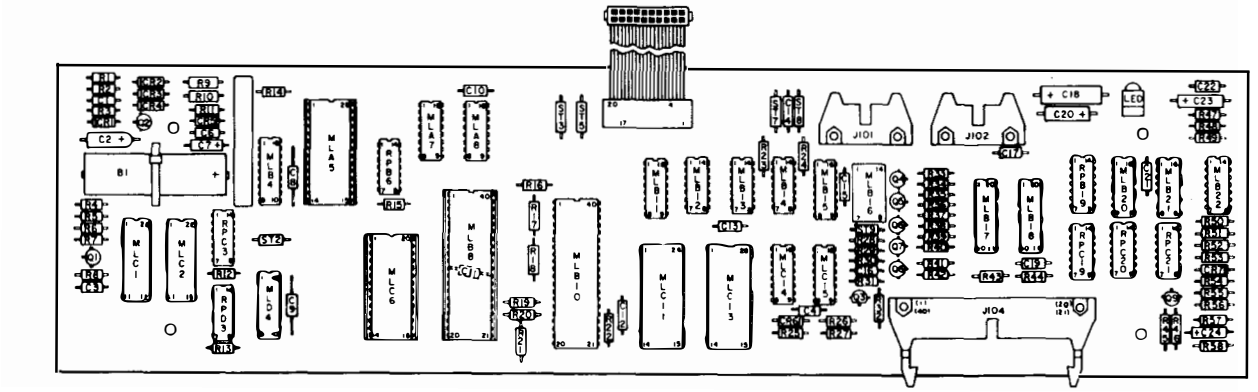
H. 410231, 410232 AND 410241 CONTROLLER ASSEMBLY LIMITED TROUBLESHOOTING (Contd)

Brief Troubleshooting Guide (Self-Test) (Refer to Page 2-28 and 2-29)

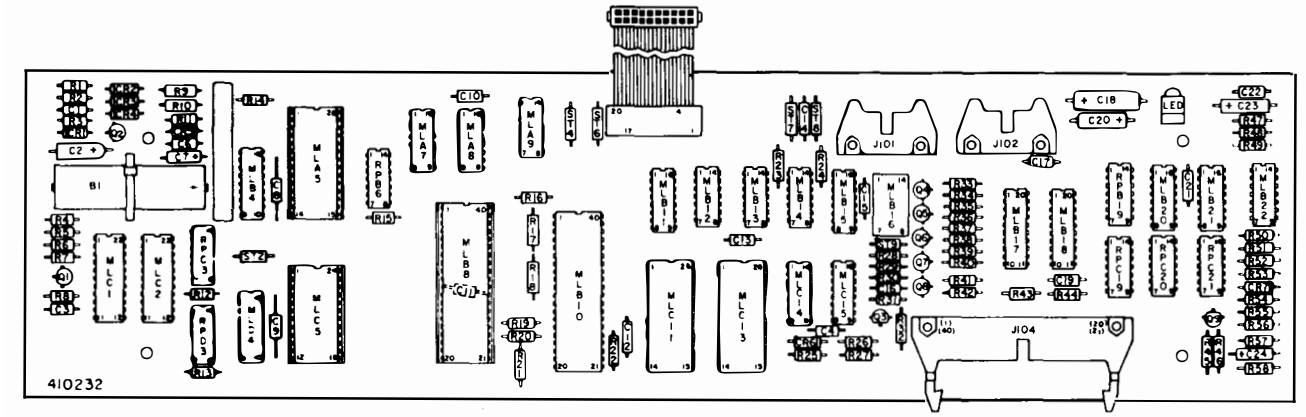
QUESTION	NO	YES
1. Does LED turn ON when power is turned on?	Replace MLB8. Check clock circuits and Z80 CPU control circuits using WDP 0553.	Go to 2.
2. Does LED fail to flash two times at end of EPROM and RAM Test?	Go to 3.	Replace EPROM - MLA5, MLC5, MLC6 if present. Check EPROM and RAM control circuits using WDP 0553. Replace RAM - MLB4, MLD4 (231 and 232 cards) MLC5, MLC6 (241 card).
3. Does LED fail to flash two times at end of first CMOS RAM Test or second CMOS RAM Test?	Go to 4.	Replace MLC1 and MLC2. Check CMOS control circuitry using WDP 0553.
4. Does LED fail to flash six times at end of CTC, SIO, and USART Test?	Go to 5.	Check CTC, SIO and USART circuitry using WDP 0553.
5. Is trouble present but not defined or corrected in 1-4?	Review initial indication of trouble.	Refer to WDP 0553.

Circuit Card Component Layout

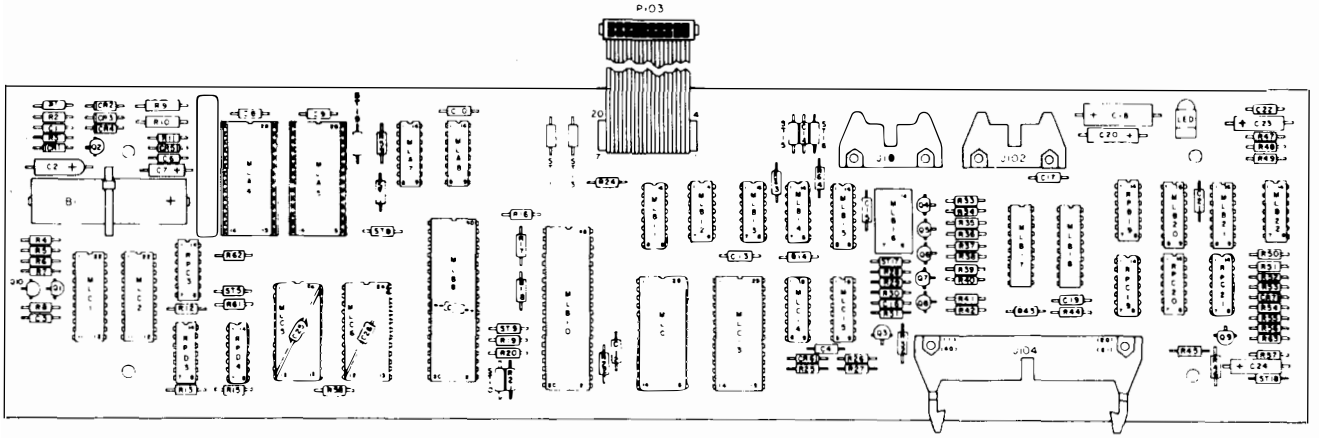
410231 Controller Assembly



410232 Controller Assembly



410241 Controller Assembly



PART 3—CIRCUIT DESCRIPTIONS AND DIAGRAMS

CONTENTS PAGE

A. GENERAL

This part provides circuit descriptions and combined schematic and troubleshooting circuit diagrams for interfaces used in and with 42/43 Terminals.

Note: When ordering replaceable parts or components, unless otherwise specified, prefix each part number with the letters "TP" (ie, TP410055).

Waveforms and voltage levels are shown on the diagrams wherever possible to aid in troubleshooting and understanding of the circuit theory. Circuit descriptions refer to coordinates on the schematic, ie, (C2) to locate the circuit being described.

For additional troubleshooting information associated with these circuit drawings, refer to PART 2 — TROUBLESHOOTING which includes:

- Troubleshooting charts.
- Tables for dynamic and static VOM measurements.
- Illustrated layouts of circuits and physical location of component and connector leads.

For part number identification of components and unit codes shown on circuit diagrams refer to PART 4 — PARTS.

Most numbers shown on various leads, components and connectors on the circuit drawings are not actually marked on the equipment. They are required for identification purposes when referring to other parts of the manual.

The circuit diagrams in this part (with added information on circuit layouts and physical location of component leads from PART 2) are also available as a separate package of diagrams with each major component on a single sheet. The package of diagrams can be ordered from Teletype Corporation as Circuit Diagrams Manual 385.

B. CIRCUIT DESCRIPTIONS

410754 TERMINAL AUXILIARY UNIT — TAU2

1. Local Mode Operation

With $\overline{\text{Terminal Ready}}$ off, J301-5 (D1) the input ot MLA5-3 is +5 V which disables gates MLA4-11 (D6) and MLA4-8 (E4). Data Terminal Ready J302-20 (E8) is held off via EIA drives MLB5-6. With DTR off, the data set holds the Receive Data lead J302-3 (E8) in the marking state.

With $\overline{\text{TR}}$ off, MLA4-6 (E4) is enabled, allowing data to be transmitted from the keyboard to an auxiliary receiving device via RDA J303-3 (G4).

With $\overline{\text{TR}}$ off, MLA4-3 (E1) is enabled allowing data to be received from a local auxiliary send device via J303-2 (G3) and subsequently forwarded to the printer via the RD lead J301-17 (F1). Also data can be transmitted from the auxiliary sender to the printer and an auxiliary receiver. MLA3-11 couples the data to the auxiliary RD lead.

Apply a ground signal to the printer ON/OFF lead, J303-17 (G2) results in a MARK hold on the RD lead J301-17.

The Characters-Per-Second output from the terminal J301-4 (F1) provides a means of changing the operating speed of the auxiliary devices. The signal is derived from the printer CPS switch.

2. On-Line Mode Operation

With $\overline{TR}$ on. 0 V gates MLA4-11 (D6), MLA4-8 (F4) and MLA6-8 (E2) are enabled. With DTR on to the data set a line connection can be made. When the data set handshaking is completed, the inputs; Data Set Ready J302-6 (E8), Clear to Send J302-5 (F8) and Carrier Detect J302-8 (F8) will all be on causing $\overline{TAU}$ Ready to turn on, thus allowing the terminal to send and receive data from the line.

From an EIA standpoint the auxiliary interface looks like a data set to an auxiliary device. The auxiliary device controls the DTR lead by applying a signal to MLA9-4 (G4) which when on permits a low signal on MLA10-3 (E6). The DTR signal to the data set is modulated through this OR gate. MLA7-6 is biased to provide an "ON" condition to MLA10-2 to satisfy an open circuit condition.

A TR or Auxiliary DTR off signal presents a high to MLB5-4 resulting in DTR going off to the data set.

When operating on-line, the duplex signal input J301-14 (F1) enables or disables MLA6-6 (E3). In the Full Duplex mode MLA6-6 is held low and the data from the auxiliary send device is inhibited from the printer and the auxiliary receive device.

3. Current Interface

The characteristics of the Line and Auxiliary 20/60 mA current Send and Receive Interfaces are like the TAU1 interfaces. Refer to the TAU1 Circuit Description and Digaram. Optical isolators MLB3 and MLB1 comprise the auxiliary transmitting and receiving current interface respectively.

P302 pins 4, 5, 6 and 8 must be strapped when using 20/60 mA current interface at the line connector. Pin 3 must be strapped to pin 4 when using RCI interface at the line connector. P303 pins 2 and 8 must be strapped when using RCI auxiliary current interface.

410755 TERMINAL AUXILIARY UNIT — TAU1

1. EIA Line Operation

When $\overline{\text{Terminal Ready}}$ J301-5 (B1) is 0 V, Data Terminal Ready J302-20 (B8) is +12 V, permitting line operation. When the data set handshaking is completed, the inputs; Data Set Ready J302-6, Clear to Send J302-5 and $\overline{\text{Carrier Detect}}$ J302-8 (D8) will be +12 V causing TAU ready J301-15 (D1) to turn on, 0 V, thus allowing the terminal to send and receive data from the line.

The $\overline{\text{Send Data}}$ lead J301-19 (B1) is pulled to +5 V via R2. When a space is being transmitted this lead goes to 0 V; EIA driver MLB2-3 (C8) then presents +12 V on the Send Data lead J302-2 (C8). The Receive Data lead J302-3 (E8) gpes tp +12 V when a space is received. MLB1-6 goes to 0 V and is gated with MLA-1 (E2) and presents 0 V to the Receive Data lead J301-17 (E1).

The $\overline{\text{Analog Loop}}$ lead J301-3 (D1) is 0 V in the Analog Loop mode. This signal drives MLB2-6 to +12 V turning on Analog Loop J302-25 (D8) and also turns on $\overline{\text{TAU Ready}}$ J301-15.

Capacitor C6, C8 and C9 prevent the maximum instantaneous voltage change from exceeding 30 volts/ microseconds.

Diodes CR3 and CR4 protect the EIA driver from overheating if all four EIA outputs are shorted to ±15 volts while the power to the driver is off.

B. CIRCUIT DESCRIPTIONS (Contd)

410755 TERMINAL AUXILIARY UNIT — TAU1 (Contd)

2. Transmit Current Interface

The send circuitry converts a Mark (Hi) and a Space (Lo) signal to a current-no current interface by switching the optical isolator light emitting diode (LED) through transistor Q1 (C3).

The LED controls the optical photo transistor which in turn drives transistor Q2 (C5). With the optical isolator off, Q2 is off, therefore no current flows in the loop between pins J302-14 and 13 (B8). A no current condition constitutes a Space.

When the LED is switched ON the optical transistor is turned on supplying base drive to Q2 which in turn switches on. Current flows in the loop constituting a Mark.

The current must be supplied from an adjustable 20 to 60 mA external current source at 12 V to 125 V open circuit. The positive side of the line must be connected to J302-14 and the negative side to J302-13. The 150 V zener diode, CR2, protects Q2 from transient line voltages.

3. Receive Current Interface

When no current is flowing in the receive current interface J302-16 and 15 (F8), the LED MLB3-1 is off. The optical transistor is off and +5 V is applied to CMOS inverter MLA3-3 representing a Space.

With the current flowing in the receive current loop, the LED is turned on which causes the optical transistor to turn on, thus applying 0 V to CMOS inverter MLA3-3 representing a Mark. Diode CR1 protects the optical LED and resistor R8 limits the voltage applied across the diode.

P302 pins 4, 5, 6 and 8 must be strapped when using the current loop. Pin 3 must be strapped to pin 4 when using the receive current interface.

410710 ANSWER-BACK CIRCUIT CARD

1. Power Turn On

On power turn on MLB1 (D10) provides a 12 millisecond power on reset pulse; MLB1-7 goes low, MLA2-6 goes high. MLC1-8 (D11) goes low and resets latches MLC10-4 (F9) and MLB6-1 (C7). After power on reset, the TBMT lead MLB3-22 (E5) is high and the counter MLB4, MLC4 (D1) is reset.

2. System Clock

The clock circuit consists of a programmable bit rate generator MLA10 (D7), crystal, R21, C18 and C19. The output of the bit rate generator MLA10-10 is 300 baud or 110 baud depending on the position of the CPS keyswitch on the printer keyboard. Actual output frequency = 16 times the baud rate.

3. Manual Initiation

Operation of the "V — HERE IS" key on the printer keyboard while the control key is held depressed causes the generation of the SYN character. From the $\overline{SD}$ lead J301A-19 (F1) this character is fed to the Receiver Serial Input MLB14-20 (C10). This UART converts serial data to parallel data and sends the parallel data to the "Here Is" decoder. When a SYN character is detected NAND gate MLA12-8 (A10) goes low. If the "Here Is" option switch (SPA5-SW7) is set in the ON position, the low generated is ac coupled to set that latch MLC7-8, MLC10-6 (F8).

MLC7-8 goes high and enables the counter MLB4-1, MLC4-1 (D1), triggers the 24 millisecond one shot MLC9 (F7) and through two gate delays provides a high on MLC10-10 (F10). MLB9-2 (F10) is high because the transmit buffer is empty. After the 24 millisecond delay MLB9-1 goes high. This puts a high on MLC10-1 and 2 (C1) which generates a one microsecond negative going pulse on the Transmit Data strobe lead of the UART MLB3-23. The data D0-D6 at the first address of the PROM MLA4 (D3) gets loaded into the transmit buffer and MLB3-22 (E5) goes low. This puts a low on MLC6-3 (C8) and a high on MLB5-4 and 5 (D3) and a one microsecond positive going pulse on MLB4-2 and MLC4-2 (D1). This advances the counter to address one. The data in the transmit buffer gets shifted to the output holding register to be transmitted serially.

When this happens, the transmit buffer is empty and MLB3-23 (D5) gets strobed again and takes the data at the second address and loads it in the transmit buffer. Meanwhile, the UART is being clocked at the selected speed and data is being sent out serially on the TSO lead of the UART MLB2-25 (D5). This sequence of TBMT going high and low continues to advance the counter and strobe the UART until a control bit (low) is detected on MLA4-9 (D4) which sets the latch MLB6-6, MLB6-3 (C7) and prevents the counter from advancing further and also prevents the UART from being strobed. At the same time MLB6-3 is gated with TBMT and transmitter end of character MLB3-24 (E5). When all the characters of the answer-back are transmitted out, MLC7-6 (D8) goes low which causes MLC6-4 to go low and triggers MLB1 (D9) to reset the answer-back circuit.

The answer-back message is gated with the Half/Full Duplex lead and if the local copy switch SPA5-SW4 is on and if the set is in the Half-Duplex mode, a local copy of the answer-back will be obtained. In order to prevent any garbling of the local copy of the answer-back in the Analog Loop mode the RD lead is blinded during the time the answer-back message is being transmitted.

4. Automatic Answering

SPA5-SW6 must be set ON with sets equipped with a TDU. Where the set is placed in the Auto Answer mode, Terminal Ready J301A-5 (F1) is activated. This triggers the six second timer MLC12 (E8) and MLC12-3 goes high for six seconds and then goes back low.

If the automatic answer-back switch SPA5-SW5 is optioned on, when the calling station goes from the Local to the Data mode, $\overline{\text{Terminal Ready}}$ and $\overline{\text{TAU/TDU Ready}}$ turn on and both the six second MLC12 (E8) and one second MLB12 (E10) timers get triggered and prevent the calling station from triggering its own answer-back.

Since the $\overline{\text{TAU/TDU ready}}$ lead has been activated, the answering stations one second timer gets triggered MLB12-2 (E10). At the end of one second MLB11-11 (G10) goes from low to high. A one millisecond negative going pulse on MLC7-12 sets the latch which in turn starts the answer-back sequence.

SPA5-SW6 must be set OFF with sets not equipped with a TDU. If the automatic answer-back switch SPA5-SW5 is optioned on when the calling station goes from Auto Answer to the Data mode, TAU/TDU Ready gets activated and the one second timer gets activated. This puts a high on MLB12-3 for one second and a high on MLB11-13. MLB11-12 is low and therefore the calling station does not trip its own answer-back.

At the answering station at the end of the ring, MLD12-2 (G8) gets triggered and MLD12-3 goes high for six seconds. This puts a high on MLB11-12. When $\overline{\text{TAU/TDU Ready}}$ turns on MLB12-3 goes high for one second. At the end of one second, MLB11-11 goes from low to high and sets the answer-back latch and starts the answer-back sequence.

The Request-to-Send auxiliary connection P301A-10 (F6) from the TAU2 card provides blinding of the ENQ detection circuit so that the answer-back is not tripped by an ENQ that appears in a tape being sent by the auxiliary reader. If SPA5-SW3 is ON and whenever the RTS (AUX) lead goes high and the set is in the Half-Duplex mode, MLC1-6 (F2) will be held marking and an ENQ from the RT set will not trip the answer-back. However, if an ENQ is received from the line, RTS (AUX) will be low and allow the detection of the ENQ and trip the answer-back.

B. CIRCUIT DESCRIPTIONS (Contd)

410710 ANSWER-BACK CIRCUIT CARD (Contd)

5. Response to ENQ

Upon receipt of an "ENQ", MLC1-6 sends it to MLB3-20 (D5). The serial data is converted to parallel data D1-D7 and sent to the ENQ decoder. When an ENQ is decoded, MLC2-8 (A7) goes low and if SPA5-SW8 is set ON, the answer-back latch gets set which starts the answer-back sequence.

410718 SELECTIVE CALLING CIRCUIT CARD

1. Power Turn On

After power up, the SCU enters the Passive mode. The Terminal Ready flag (TR) will be set and the RO is disconnected from the line.

2. Description of Terminal I/O Leads (Connector J301)

The following leads provide logic card to SCU interfacing:

Terminal Ready — (TR from terminal, pin 5) TR is ON (0 Volts) to MLA5, pin 11.

Interlock Switch — (ISW from terminal, pin 20) The interlock switch is closed (0 V) when the printer cover is closed and goes to +5 V when the printer cover is open. The voltage is applied to MLA5, pin 12.

TAU Ready — (DR to terminal pin 15) ON (0 V) when Data Set Ready, Carrier Detect and Clear to Send signals from data set are ON.

Receive Data — (RD to terminal pin 17) Serial binary data appears on this lead from the data set only after the SCU has received a CDC, sent a positive response and received an STX character.

3. Description of Line I/O Leads (Connector J302)

The following leads provide SCU to line interfacing:

Transmitted Data — (TD From SCU PIN 2) Serial binary data is transmitted to the data set over this lead from the SCU answer-back at the selected baud rate. In the idle condition, the signal is "MARK" hold to the data set.

Receive Data — (RD To SCU PIN 3) Serial binary data is received on this lead from the associated data set at a specific baud rate corresponding to mark-space signals serially transmitted from a remote Terminal via a data set.

Request To Send — (RTS From SCU PIN 4) A signal to the data set that when "ON" conditions it to transmit carrier and must remain on during the send interval. The RTS lead goes "ON" approximately 500 ms before the answer-back is transmitted.

Clear To Send — (CTS From SCU PIN 5) A signal derived in the data set that when in the "ON" condition indicates the data set is ready to transmit data.

Data Set Ready — (DSR To SCU PIN 6) A signal from the data set that when "ON" indicates the data set is connected to the communication channel.

Data Carrier Detect — (CD To SCU PIN 8) This signal goes "ON" when the data set is in the Data Mode and it has detected data carrier. When "OFF" the receive data lead is in the "MARK" hold condition.

Data Terminal Ready — (DTR From SCU PIN 20) This lead is conditioned on at all times.

4. SCU Operation

Serial data is received at J302 pin 3, through the voltage divider R10, R11 and into pin 33 (RD) of MLB3. The serial data is converted to parallel data on MLB3 pins 4 through 7 (RD7—RD1). MLC5 and MLC6 decode bits 1, 2, 3 and 4 of the ASCII code and their sixteen outputs are row zero through fifteen (RW0—RW15). MLC4 decodes bits 5, 6 and 7 of the ASCII code and the eight outputs are columns zero through seven, (C0-C7). MLA4 and MLA5 contain the six 2-input NOR gates that decode the column and row of any ASCII character programmed. The characters programmed appear on the output of the NOR gates as a positive pulse (150 to 200 microseconds wide) when the CDC characters received match the characters programmed.

J301 pin 5 TR lead is low when the RO is ready to receive. J301 pin 20 interlock lead is low when the RO cover is closed. These two low signals are applied to NOR gate MLA5 pins 11 and 12, the output on MLA5 pin 13 is high to MLB3 pin 13. J301 pin 15 is the TAU ready lead and is low when the line EIA interface is satisfied. This low from MLB3 pin 12 causes the RO to go to the Data mode.

Switch packs SPA1 and SPC1 are used to program the two answer-back characters. SPA1 is used for the first character and SPC1 is used for the second character. SW1 — SW7 correspond to bit 1 — bit 7 on both switches and a Mark corresponds to the switches being off. SPA1 and SPC1 are connected to the input of two multiplexers (MLA2, MLC2) and resistor pack RPB1 is used for pullups. The outputs of MLA2 and MLC2 are connected to the input of MLB3 pins 22-28. Pin 29 of MLB3 is an I/O signal that does the following: When SW4 is OFF, the signal acts as an output and when it is low the first character of the answer-back is selected, then it goes high to select the second character of the answer-back. When SW4 is ON, pin 29 acts as an input lead. The first programmed character of the answer-back is sent plus the character ACK which is internally programmed in the MOS pack. The answer-back characters are serially transmitted by pin 35 of MLB3. Pin 34 of MLB3 is the Request to Send lead which controls carrier of the data set. When a CDC is recognized by MLB3, RTS goes high immediately and stays high for 700 ms. The two answer-back characters are transmitted after RTS has been high for 490 ms.

Switch Pack SPB2 contains four option switches that do the following:

SW1 — ON	Group Answer-Back
SW1 — OFF	No Group Answer-Back
SW2 — ON	Broadcast Answer-Back
SW2 — OFF	No Broadcast Answer-Back
SW3 — ON	300 Baud one stop bit
SW3 — OFF	110 Baud two stop bits
SW4 — ON	First and second answer-back characters programmed for positive reply. First answer-back character programmed and delete for a negative reply.
SW4 — OFF	First answer-back character programmed and ACK for positive reply. First answer-back character programmed and NAK for negative reply.

B. CIRCUIT DESCRIPTIONS (Contd)

410038 TELEX INTERFACE CIRCUIT CARD

1. Interface to BSR Set

All signals at this interface (connector B3) are EIA RS 232-C compatible. A positive signal level represents a "Space" or "On" condition. A negative signal level represents a "Mark" or "Off" condition. The following is a list of the EIA leads used:

Pin No.	Description
1	Frame Ground
2	Send Data — SD
3	Receive Data — RD
6	Data Ready — DR
7	Signal Ground
20	Terminal Ready — TR
25	Test

Terminal Ready (TR) from BSR Set — Pin 20 (F1)

Neutral Mode: An "Off" condition on TR will cause the neutral send signal loop to be in the idle condition (neutral loop current limited to 5 mA). An "On" condition on TR will allow the neutral send signal loop to have the full amount of current flowing (no current limiting). A private line option will force the assembly to act as if TR were "On".

Polar Mode: TR will have no effect on circuit operation.

Data Ready (DR) to BSR Set - Pin 6 (EI)

Neutral Mode: DR will latch "Off" when a forward (idle) current at the receive signal loop has been detected. DR will latch "On" when a reverse (connect) current has been detected. A private line option will keep DR "On".

Polar Mode: DR will be "Off" if the assembly is properly optioned. If the assembly is optioned for private line (not meant to be used in the Polar mode), DR will be "On".

Receive Data (RD) to BSR Set — Pin 3 (EI)

Neutral Mode: A "Space" on RD will indicate that the receive signal loop has no current flowing. A "Mark" will indicate that the signal loop has current flowing in either polarity.

Polar Mode: A "Space" on RD will indicate that the receive signal loop has a forward current flowing. A "Mark" will indicate that the signal loop has a reverse current flowing (or a no current condition — not normal).

Send Data (SD) from BSR Set — Pin 2 (G1)

Neutral Mode: A "Space" on SD will cause the neutral send signal loop to open. A "Mark" will cause the signal loop to close.

Polar Mode: A "Space" on SD will cause the polar send signal loop to be spacing (positive or forward polarity). A "Mark" will cause the signal loop to be marking — negative or reverse polarity.

Test from BSR Set — Pin 25 (G1)

Neutral Mode: When the assembly is properly optioned for Test, an "On" condition applied to Test will cause the current loop to be in the forward (idle) condition. An "Off" applied to Test will cause the current loop to be in the reverse (connect) condition. During normal on-line operation, test will have no effect.

Polar Mode: Test will have no effect on circuit operation in either the Normal or Test modes.

2. Interface to Telex Lines

The signals at this interface (terminal block TB1) are isolated from any voltage reference. The signal leads are the following (F11):

Polar Send +
Polar Send -
Neutral Send +
Neutral Send -
Receive +
Receive -

Polar Send — The assembly provides the loop power for the send side of the polar interface. The open circuit voltage is 140 ± 18%. The maximum load current is 40 mA. Option switches are used to select for current limiting (20 or 35 mA) or a fixed resistance (510 or 2900Ω).

Neutral Send — The assembly opens and closes the loop power provided by the network exchange. It will also current limit the loop current to 5 mA in the idle condition.

Receive — The assembly detects the presence of current flowing in the loop (polarity sensitive). The loop current must not exceed 66 mA. For Polar mode operation, internal circuitry can be optioned to limit the loop current (20 or 35 mA).

3. Logic Circuitry

The logic circuitry handles data and control signals and it capable of being reconfigured for one of two basic modes of operation — Polar and Neutral. Multiplexer MLA4 (E4) does the circuit reconfiguring. When switch SP1-2 is closed (neutral), an output Y is the same as its A input (input B has no effect). When SP1-2 is open (polar), and output Y is the same as its B input (input A has no effect). An oscillator circuit has been included for self-exercise purposes. It is initiated by closing switch SP1-3 (G3). This connects the oscillator to the send data lead. The waveform generated will be squarewave with approximately a 6 ms period. The LED's indicate the status of their respective EIA signal leads. If an LED is on, its EIA signal is a "Space" or "On" conditon.

Neutral Mode: In the Neutral mode the IF and IR signals (Idle Forward and Idle Reverse) control the state of the DR (Data Ready) latch. When IR is low the DR latch is set (MLA3-11 low) (F3). When IF is low MLA4-4 will be low causing the DR latch to reset (MLA3-14 high). The state of the DR latch is ignored in private line application because SP1-1 is closed forcing data ready on. In non-private line applications when data ready is turned on, the terminal responds by turning terminal ready on. This causes MLA3-6 (F3) to go high, forcing MLA5-3 (F5) high and allows MLA6-11 to go low. The low on MLA6-11 (TRN) causes the 5 mA idle line current limit circuitry to be bypassed allowing the loop to go to full current. In private line application, (SP1-1 closed) TRN is held low. Receive data at P3-3 is a Mark when either RR (receive reverse) or RF (receive forward) is low. RF is low when a forward current is detected in the receive current loop. RR is low when a reverse current is detected in the receive current loop. When send data (P3-2) is a "Mark", NS (neutral send) at MLA6-8 (G6) is low which closes the neutral send loop. Test controls PS (polar send) for use during Neutral mode testing. When test if off PS is low thereby putting a negative (reverse) polarity on the polar send loop.

B. CIRCUIT DESCRIPTIONS (Contd)

3. Logic Circuitry (Contd)

Polar Mode: Receive data is a "Mark" when RR is low or when both RF and RR are high. Data Ready is held "Off" unless SP1-1 is closed (private line option which holds Data Ready "On"). Terminal Ready has no effect except LED 4 will indicate its status if SP1-1 is open. A "Mark on send data puts a low on PS (reverse loop). This is basically a level shifter. A negative voltage on send data results in a negative voltage at the polar send loop. Test has no effect in the Polar mode. TRN and NS are held low (MLA4) for testing purposes.

4. Current Loop Circuitry

The current loop circuitry isolates the current loops from the logic (EIA) circuitry using seven optical isolators (MLB5-B9B). MLB9A and B (E7) detect loop current in the forward direction MLB8A and B detect loop current in the reverse direction. MLB8B and MLB9B are used to detect reverse and forward idle line current (nominal 5 mA). MLB8A and MLB9A are used to detect reverse and forward data current. The threshold of the data detectors can be changed from approximately 2 mA (used in the Polar mode) to approximately 9 mA (used in the Neutral mode) via straps ST3 and ST4 (F8). When straps ST3 and ST4 are in the 9 mA position, resistors R56 and R57 are placed in parallel with the LEDs in the data detectors thereby shunting approximately 9 mA of current. CR24, CR26-28, R44-46, C3-4 and ST2 will limit the receive loop current to 20 or 35 mA depending on the position of ST2. Switch SW1 will bypass this circuitry for applications that have external current limiting (neutral). CR23, CR25, R42-43 and Q1-2 limit the current through the isolator LEDs to approximately 18 mA. MLB7 controls Q5 (F9) which will bypass the neutral send 5 mA idle circuitry (R40-41 and Q7-8). A low on TRN will turn Q5 on to bypass the idle circuitry. TRB+, TRB- provide the DC bias required for this circuitry (12V). MLB6 controls Q6 (G9) which opens and closes the neutral send loop. A low on NS closes the loop. NSB+, NSB- provide the DC bias required for this circuitry (12V). CR19-22 (E10) form a rectifying bridge for the neutral send circuitry. MLB5 controls the polar send circuitry which provides a polar (+ or -) voltage from a single-ended power source (VP+, VP-). It acts as an electronic DPDT switch to reverse both leads of the polar power supply. A low on PS turns off Q9 ($\bar{C}7$) which allows Q10 and Q11 to be on. Q10 turns off Q12 (C9) which turns off Q13. Q11 connects VP- to the output (PSS) and also turns on Q14 which connects VP+ to the current loop reference. The output voltage is negative with respect to the reference (polar send+ < polar send-). A high on PS allows Q9 to be on which turns off Q10 and Q11. With Q11 off, Q14 is also off. Q10 being off allows $\bar{Q}12$ to be on which connects VP- to the reference. Q12 also turns Q13 on which connects VP+ to the output (PSS).

The output voltage is now positive with respect to the reference (polar send+ > polar send-). CR15-18, R29-31, Q15-16 and ST1 will limit the polar send current to approximately 20 mA or 35 mA depending on the position of ST1 and switch SW2. Switch SW2 selects between current limiting or a fixed resistance. Switch SW3 selects between two different fixed resistances (510 or 2900 Ω.). Varistors RV1-3 protects the assembly from abnormal voltages that may be present on the current loop lines. Switches SW4-6 select for normal (on-line) operation or for loopback testing (off-line). When SW4-6 are in the Test position, receive, neutral send and polar send are disconnected from the Telex Lines and are tied together in a closed loop. Switches SW2-3 are not functionable in the Test mode. The current limiting circuitry is always used. In the Neutral mode, polar send provides the loop power (polarity is determined by the EIA Test lead - see Fig. 3). In the Polar mode, the neutral send circuitry is always closed and the 5 mA idle is bypassed (see Fig. 4).

5. Power Supply Circuitry

This circuitry takes the appropriate ac voltages supplied through connectors P1 and P2 (C3) and develops the dc voltages required by this assembly. R53-54 and CR30-31 provide shunt voltage regulation for the $\pm$ 12 V supply (limits the maximum voltage to $\pm$ 13 .0 V). Voltage regulator VR1 (C4) regulates the 5.0 $\pm$ 5% V supply. TRB+, TRB- and NSB+, NSB- are unregulated bias supplies (9.0 to 17.5 V). VP+, VP- is the polar send loop power supply (99.5 to 163.5 V). CR29 limits the voltage to a maximum of 208.0 V to protect against transient overvoltage conditions.

410382 DUAL EIA/NEUTRAL INTERFACE CIRCUIT CARD — TAU3

1. Basic Function

The 410382 circuit card assembly provides the SCCAT based Model 42 Terminal (4220) with a main interface consisting of either an EIA RS-232C interface or a neutral current loop interface. A secondary or "AUX" EIA interface is provided to allow interfacing the Reperforator/Transmitter (R/T) unit to the terminal. The main EIA interface is intended for operation with a modem. Both EIA interfaces are terminated in standard EIA type connectors which are mounted to the noncomponent side of the circuit card. The neutral current loop interface, which functions in parallel with the main EIA interface, provides operation on all known neutral current loops such as those provided by the Telex network. Loop connections are made via a terminal block located on the noncomponent side of the circuit card.

2. EIA Interfaces

The EIA signals to and from the 410382 circuit card will be +3 V to +25 Vdc to represent an "ON" condition for control signals and a "SPACE" for data signals. An "OFF" or "MARK" condition is represented by a voltage level of -3 V to -25 Vdc. Following is a list by pin numbers of the signals present at both EIA connectors:

The main EIA interface shifts the logic level signals from the controller (J103), to EIA level signals for application to a modem (J105). It also shifts the EIA level signals from the modem to logic level signal required by the controller.

SD (Send Data) from the controller at J103 pin 19 (B3) is a mark when high and a space when low. The signal is inverted at MLB10-12 and is applied to MLB9-4 (C3). MLB9-6 will be low when SD is spacing thereby illuminating LED 1. The inverted SD signal is inverted again at MLB11-2 (B4) and applied to EIA driver MLA8 on pin 2. MLA8-3, which is connected to the main EIA connector (J105 pin 2), will be approximately +12 V for a space and -12 V for a mark. The $\overline{\text{DTR}}$ (Data Terminal Ready) signal at J103 pin 5 (C3) functions identically as the SD signal. LED 2 will be illuminated when $\overline{\text{DTR}}$ is active. J105 pin 20 will be approximately +12 V when $\overline{\text{DTR}}$ is on and approximately -12 V when $\overline{\text{DTR}}$ is off. The remaining three signals from the controller, $\overline{\text{SRTS}}$ (Secondary Request to Send), $\overline{\text{RTS}}$ (Request to Send) and $\overline{\text{AL}}$ (Analog Loop) are applied directly to their respective EIA drivers.

The CTS (Clear to Send), DSR (Data Set Ready), DCD (Data Carrier Detect) and RD (Receive Data) from the modem are applied via J105 to MLB8 (D5) which shifts the EIA levels to logic levels. The outputs of MLB8 at pins 11, 3 and 6 will be low when the CTS, DSR and DCD signals are active (approximately +12 V) and high when inactive (approximately -12 V). The output at MLB8-8 (D5) will be high when RD is a mark and low when a space. The output of the CTS receiver (MLB8-11) is applied to the controller via J103 pin 12. The outputs of the DSR and DCD receivers (MLB8-3 and 6) are applied to MLB12-4 and 5. When these two inputs are low, the output at MLB12-6 will go low forcing MLB13-3 high.

If ST1 (D4) (Normal/Private Line) is in the "Normal" position, MLB12-8 will be high, placing a low on J103 pin 15 via MLB10-4. Additionally MLB10-6 will go low illuminating LED 3. Should ST1 be in the "Private Line" position, MLB12-8 will be high regardless of the state of the signal at MLB12-10. The $\overline{\text{DR}}$ (Data Ready) signal at MLB13-2 is generated by the receive side of the neutral current loop circuitry and is used to control the $\overline{\text{DSR}}$ output to the controller when the neutral current loop circuitry is selected as the main interface. The output of the RD receiver at MLB8-8 drives MLB12-1. MLB12-3 (D4) will follow the condition of pin 1 since the RD input at MLB12-2 is low until driven by the receive side of the neutral loop interface. MLB12-3 drives the RD output to the controller via J103 pin 17 and will be low for a space and high for a mark. In addition, this signal is double inverted by MLB10-10 and 8 (E4) and will illuminate LED 4 when RD to the controller is spacing.

The auxiliary EIA interface which terminates at J106 (C3) provides a means of interfacing the Reperforator/Transmitter (R/T) unit to the terminal controller. This interface operates independently and provides only level shifting. Signal polarities are the same as those on the main EIA interface.

B. CIRCUIT DESCRIPTIONS (Contd)

410382 DUAL EIA/NEUTRAL INTERFACE CIRCUIT CARD — TAU 3 (Contd)

3. Neutral Current Loop Interface Circuitry

The neutral current loop interface maintains 2500 V dc isolation from the EIA and logic circuitry, and frame ground. The send side of the interface will operate within an open circuit voltage range of 10 to 276 V dc and a closed circuit current of 16 to 72 mA in either a half or full duplex configuration. In addition, it will limit loop current to approximately 5 mA when in the idle condition. The receive side of this interface will detect both the idle (5 mA) condition and the full loop current (15 mA or greater) condition. The receive loop current must be externally limited to 72 mA.

The neutral current loop interface is the alternate main interface for the 410382 circuit card. The function of the receive circuitry is to detect idle and data loop current in both the forward and reverse direction. The function of the send circuitry is to open and close the loop in response to a mark/space command and to set the loop current to 5 mA in the idle condition.

Optical isolator MLB1 (E7) detects idle loop current in the forward direction whereas MLB3 (F7) detects idle loop current in the reverse direction. When reverse idle current is detected, MLB3-5 will go low thereby setting the Data Ready Latch at MLB13-13 (E6). The latch output at MLB13-8 will go low which is the alternate source for the main $\overline{\text{DSR}}$ signal to the controller. When forward idle current is detected, MLB1-5 will go low causing the Data Ready Latch to reset. Optical isolator MLB2 (E7) detects forward data current and isolator MLB4 detects reverse data current in the loop. Resistors R1 and R3 shunt approximately 9 mA of loop current from the optical isolators.

Resistors R2 and R4 limit the forward and reverse loop current through the optical isolators to approximately 20 mA. The remaining loop current is passed by Q1 and Q2. When a forward loop current of 15 mA or greater is flowing, MLB2-5 will go low. MLB4-5 will be low when a reverse loop current of 15 mA or greater is flowing. These outputs are double inverted by MLB11 and gated at MLB13. The output at MLB13-6 is the alternate source for the RD signal to the controller.

Timer MLB7 (C6) with its associated components is set to free run at approximately 20 kHz with a duty cycle of about 70%. This timer in conjunction with Q6, T1 and associated components form a dc to dc converter with 2500 Vdc isolation from primary to secondary. The voltage at the secondary of T1 is rectified by CR 8 and filtered by C4 and C5. The output is approximately 12 Vdc and is used as an isolated bias power supply for the neutral loop send circuitry. The SD signal from the logic circuitry is connected to MLB9-2. When SD is a mark, MLB9-3 will be high turning off the LED in optical isolator MLB5. The 5 mA idle current limit circuit consisting of Q4, Q5 and R6 is enabled via R7. When SD is spacing, this circuitry is disabled since the transistor in MLB5 is turned on. The $\overline{\text{DTR}}$ signal from the logic circuitry is connected to MLB12-13 and is gated with the SD signal on MLB12-12. MLB12-11 will go low when both $\overline{\text{DTR}}$ and SD are low. This low causes MLB9-8 to go high turning off the LED in optical isolator MLB6. The send switch (Q3) is turned on via R9 thereby allowing full loop current to flow. When either $\overline{\text{DTR}}$ or SD go high, the transistor in MLB6 is turned on thereby turning Q3 off preventing the flow of loop current. A full wave bridge consisting of CR3 through CR6 allows the send circuitry to operate with reverse polarity applied at TB1. RV1 protects the send circuitry from transient voltage surges.

410719 DUAL FONT CIRCUIT CARD

1. Basic Function

The 410719 dual font card is used in conjunction with a 43 printer logic card to provide the necessary logic for alternate font capability in pin and friction feed printers. The card is a daughter card that plugs into the 40 pin socket normally occupied by the MAPL MOS chip on the logic card.

2. Detailed Circuit Description

MLB1(XFC/2) is a 64 pin MOS chip whose circuitry is derived from the MAPL3 logic and is designed to accept parallel input data on a demand basis and in turn generates the line feed motor, carriage motor, print head and bell signals for the matrix printer mechanism. In addition to these functions, the XFC/2 also provides control and timing to access external EPROMs containing print character font data. The internal font option inputs have been eliminated.

Eleven outputs of MLB1, C1 to C3 and A0 to A7, are provided to address ROMs MLB2 and MLB3. RPA3 provides the necessary pulldown resistors for the open-drain devices. RD0 to RD9 are the nine inputs that are utilized to accept print character font data from MLB2 00 to 07 and MLB3 output 00.

SPA2

SW1: EXTERNAL FONT TEST
OFF - first font (first 1K address of ROM)
ON - second font (second 1K address of ROM)

SW2: FONT SELECT
ON - external font mode
OFF - internal font mode

SW3: EXTENDED EXTERNAL FONT
OFF - upper 7/lower 7 print levels
ON - all 9 print levels

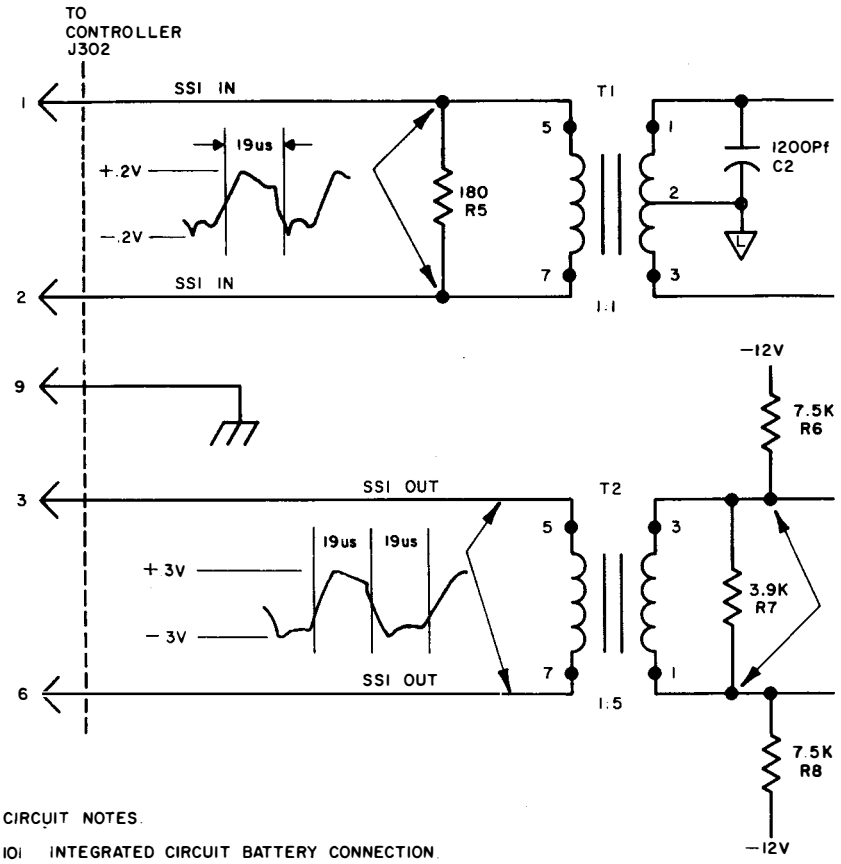
SW4: PRINT LEVEL 9 CONTROL
OFF - level 9 driven by ROM
ON - level 9 always zero

The FS lead provides a means of forcing the XFC/2 device to derive print character data from an external ROM. With FS=0, XFC/2 will be forced to the external font mode. With FS=1, the XFC/2 will power-up in the internal font mode and respond to SHIFT-OUT and SHIFT-IN characters received via D0 - D7 inputs to enable external or internal font mode respectively.

C. CIRCUIT DIAGRAMS

1. 410746 SSI Interface Circuit Card

410746 SSI INTERFACE CIRCUIT CARD



CIRCUIT NOTES:

101 INTEGRATED CIRCUIT BATTERY CONNECTION

TYPE	DESIGNATION	+5V	-5V
LINEAR	404239 (239)	3	12

INFORMATION NOTES:

201 ALL RESISTORS 1/4 WATT AND RESISTANCE VALUE IN OHMS, UNLESS SPECIFIED

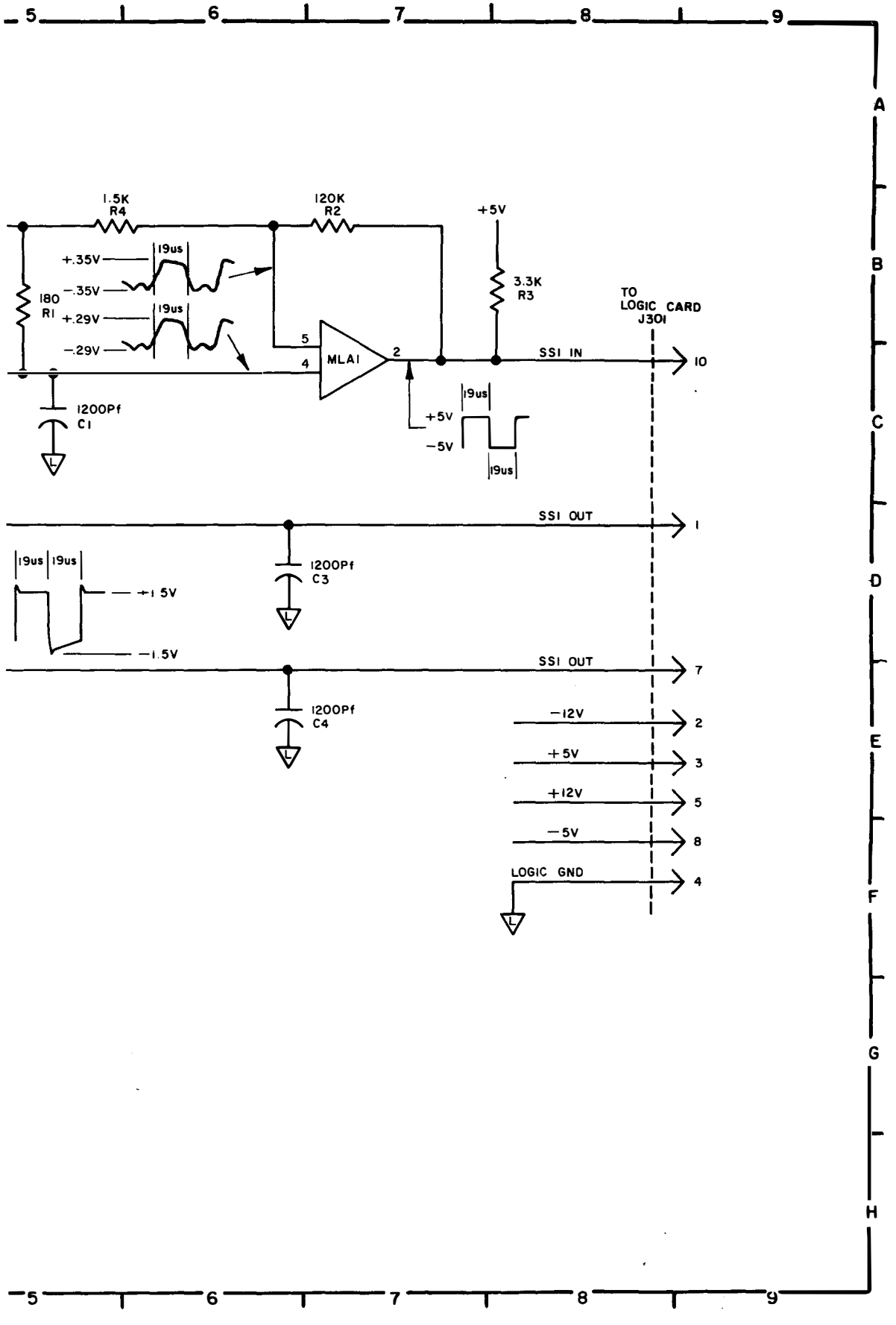
202 ——→ INDICATES MALE TERMINAL

203 GROUND DESIGNATION

LOGIC GROUND (+5V, -5V, -12V RETURNS)

CHASIS GROUND

204 PINS 1, 6, 7, 8, 9, 10, 11, 12, 13 AND 14 OF MLAI ARE ALL CONNECTED TOGETHER ON ISSUE 3A.


5
6
7
8
9
A
B
C
D
E
F
G
H
1.5K
R4
120K
R2
+5V
3.3K
R3
TO
LOGIC CARD
J301
+.35V
19us
-.35V
180
R1
+.29V
19us
-.29V
5
4
MLA1
2
SSI IN
10
1200Pf
C1
+5V
19us
-5V
19us
SSI OUT
1
19us
19us
+1.5V
-1.5V
1200Pf
C3
SSI OUT
7
1200Pf
C4
-12V
2
+5V
3
+12V
5
-5V
8
LOGIC GND
4

C. CIRCUIT DIAGRAMS (Contd)

2. 410754 Terminal Auxiliary Unit — TAU2

CIRCUIT NOTES:

101. VOLTAGE VOLTAGE RANGE

+12V	+10.8 TO 13.2
+5V	+4.5 TO 5.5
-12	-10.8 TO 13.2

102. INTEGRATED CIRCUIT BATTERY CONNECTIONS:

PART NO.	TYPE	DESIG.	+12 V	+5 V	GND	-12 V
335529	LINEAR	MLA1, A9		14	7	
474032	TTL	MLA2, A3, A7, A10		14	7	
474000	TTL	MLA4		14	7	
474004	TTL	MLA5		14	7	
474008	TTL	MLA6		14	7	
335528	LINEAR	MLA8, B5	14			1
335522	OPT. ISOL.	MLB1, B10				
326801	OPT. ISOL.	MLB3, B7				
404049	CMOS	MLB6		1	8	

INFORMATION NOTES:

201. ALL RESISTORS 1/4 WATT AND RESISTANCE VALUE IN OHMS, UNLESS SPECIFIED.

202. ALL CAPACITOR VALUES IN MICROFARADS, UNLESS SPECIFIED.

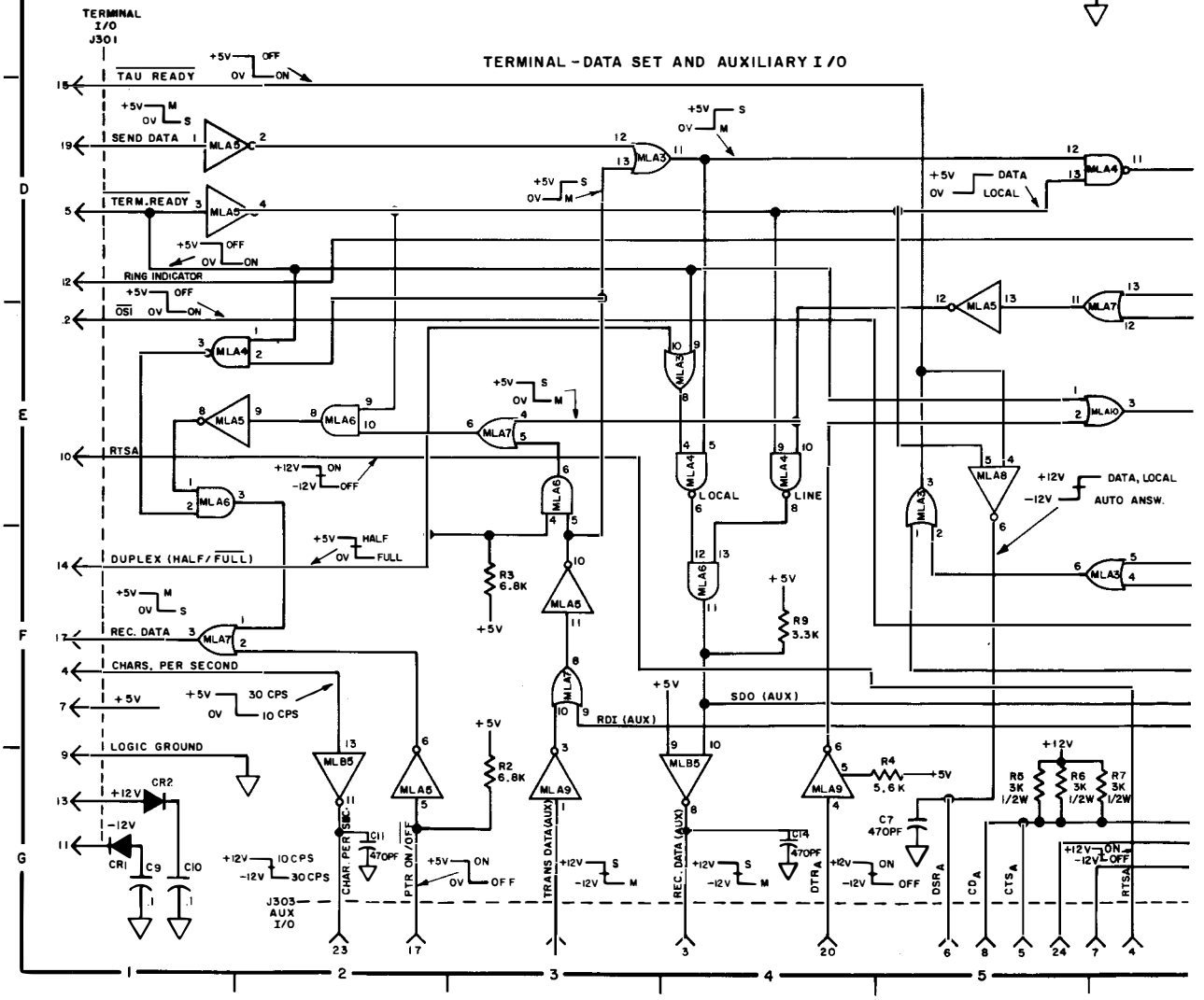
203. INDICATES FEMALE TERMINAL.
INDICATES MALE TERMINAL.

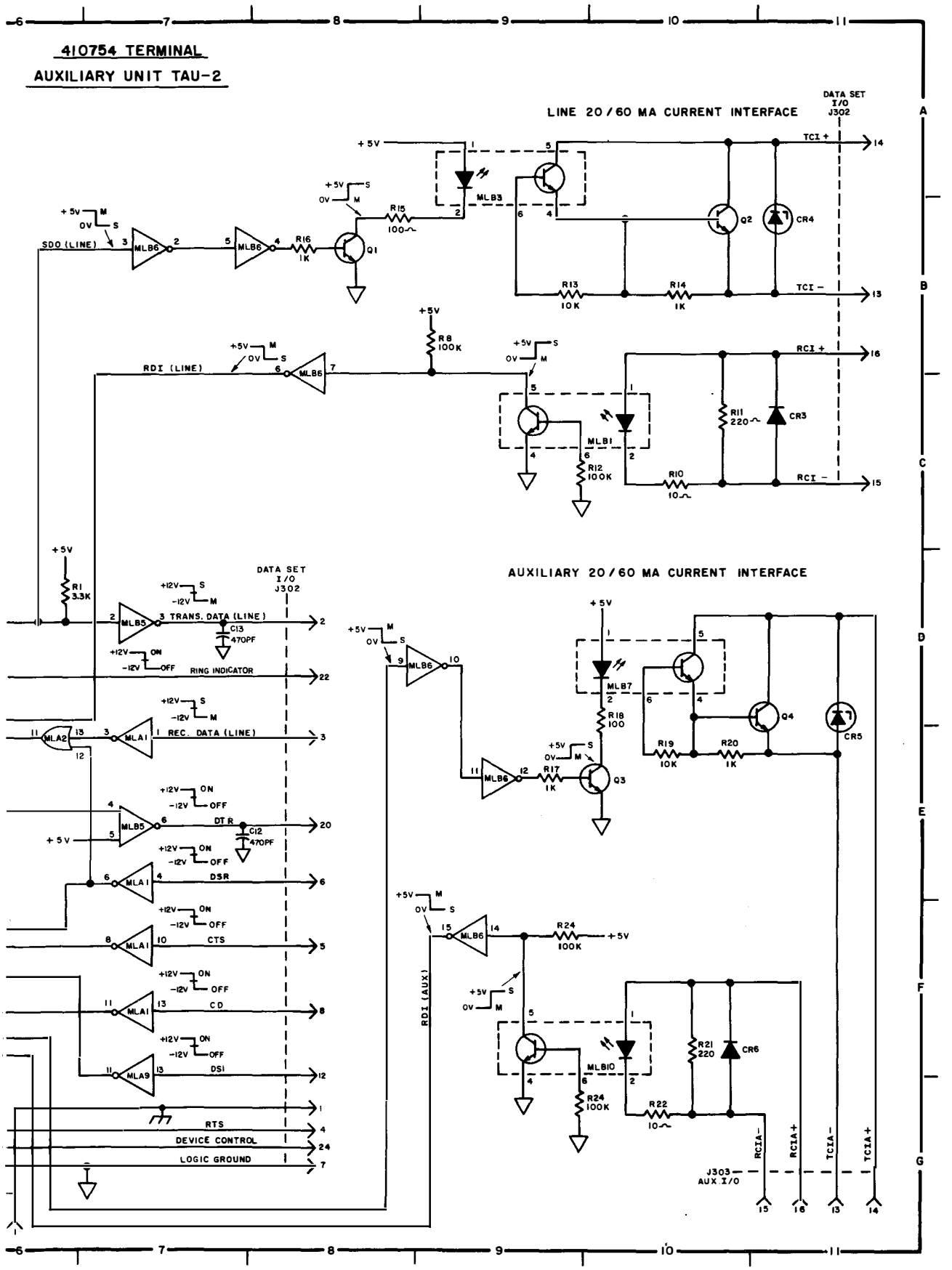
204. LOGIC DESIGNATION
INDICATES PACKAGE PIN NO.
INDICATES LOCATION ON CIRCUIT CARD

205. P302 PINS 4,5,6 AND 8 MUST BE STRAPPED WHEN USING 20/60 MA CURRENT LOOP AT THE LINE CONNECTOR. PIN 3 MUST BE STRAPPED TO PIN 4 WHEN USING RCI INTERFACE AT THE LINE CONNECTOR.

206. P303 PINS 2 AND 8 MUST BE STRAPPED WHEN USING RCI AUX. CURRENT LOOP.

207. STRAP P303 PINS 7 AND 17 TO BLIND RECEIVED DATA TO THE PRINTER.




410754 TERMINAL
AUXILIARY UNIT TAU-2
LINE 20/60 MA CURRENT INTERFACE
DATA SET I/O J302
AUXILIARY 20/60 MA CURRENT INTERFACE
SDO (LINE)
RDI (LINE)
TRANS. DATA (LINE)
REC. DATA (LINE)
RING INDICATOR
DTR
DSR
CTS
CD
DSI
RTS
DEVICE CONTROL
LOGIC GROUND
RDI (AUX)
TCI +
TCI -
RCI +
RCI -
J303 AUX I/O
RCIA-
RCIA+
TCIA-
TCIA+